Class-F push-pull totem-pole power amplifier

for 5G base stations

Master Thesis Microelectronics

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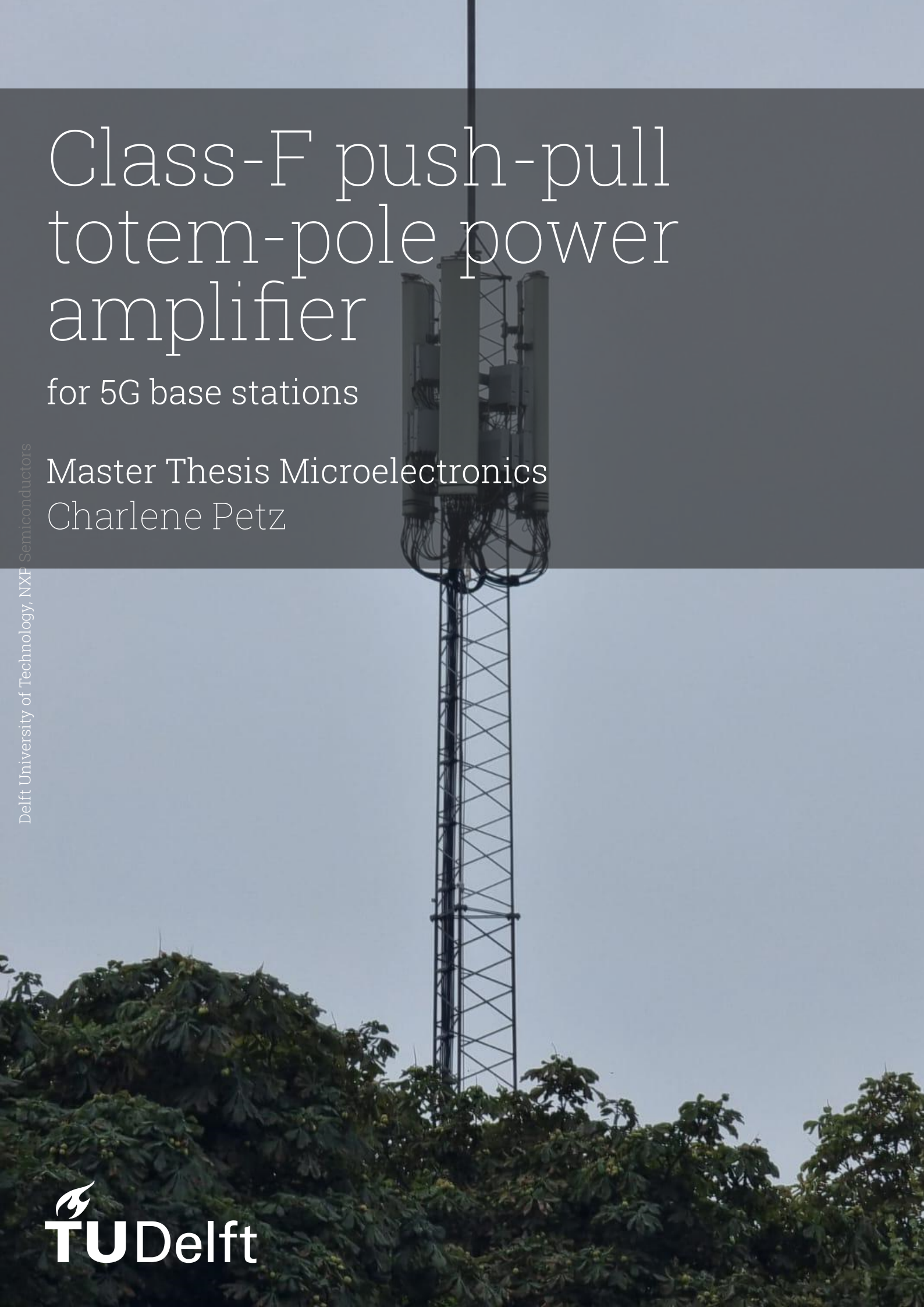

TU Delft

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by

Charlene Petz

to obtain the degree of Master of Science
at the Delft University of Technology

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To my father, who inspired me to study electrical engineering,
to my mother, who has always given me her unconditional support,
and to my boyfriend, who has never left my side.

Abstract

As 5G is rapidly growing, wireless communication systems require wideband, compact and highly efficient power amplifier modules (PA) to drive the base station antenna arrays. Doherty PAs are implemented in most base stations. The final stage in these power amplifier modules has high supply voltages (28-50 V) to generate a high output power of >20 W at reasonable output impedance levels. This work replaces the 'classical' single-ended cascode PA to drive the Doherty PA, with a series push-pull (or totem-pole) PA to increase the efficiency and bandwidth of the driver. The series push pull designs can reach peak efficiencies of 70.7%, which is about 10 percentage points higher than the efficiency of the single-ended PA. To ensure that a fair comparison is made between the designs, the series push-pull designs operate at 5 V and 10 V supply, in order to generate an output voltage swing of 5 V and 10 V respectively. This is compared to the single-ended PA with a 5 V supply and 10 V output swing. Simulation results show that the series push-pull design does indeed increase the efficiency of the driver whilst having minimal AM-AM distortion (<1 dB) at the design frequency of 3.6 GHz.

Contents

Nomenclature

Abbreviations

Abbreviation	Definition
AM	Amplitude modulation
AM-AM	AM to AM distortion
AM-PM	AM to PM distortion
BJT	Bipolar junction transistor
BW	Bandwidth
H2	Second harmonic
H3	Third harmonic
HV	High voltage
IMD3	Third-order intermodulation distortion
IMN	Input matching network
IP3	Third-order intercept point
LV	Low voltage
OIP3	Third-order output intercept point
OMN	Output matching network
PA	Power amplifier
PAE	Power added efficiency
PM	Phase modulation
RF	Radio-frequency
RMS	Root mean square

Symbols

Symbol	Definition	Unit
C	Capacitance	[F]
C_{fb}	Feedback cacpacitor	[F]
C_{μ}	Parasitic capacitance between collector and base	[F]
C_{omn}	Capacitor in the output matching network	[H]
C_{out}	Total parasitic output capacitance of the push-pull PA	[F]
C_{π}	Parasitic capacitance between base and emitter	[F]
f	Frequency	[Hz]
f_d	Design frequency	[Hz]
f_{max}	Maximum oscillation frequency	[Hz]
f_T	Transit frequency	[Hz]
G_p	Power gain	[dB]
G_t	Transducer gain	[dB]
I	Current	[A]
I_C	Collector current	[A]
I_{int}	Intrinsic current	[A]
k	Coupling factor of the transformer	[-]
kf	Stability factor	[-]
L	Inductance	[H]
L_{bias}	Inductor in the biasing circuit	[H]

Symbol	Definition	Unit
L_{choke}	RF choke inductor	[H]
L_{fmr}	Transformer inductance	[H]
L_{imn}	Inductor in the input matching network	[H]
L_{leak}	Transformer leakage inductance	[H]
L_{omn}	Inductor in the output matching network	[H]
M	Mutual inductance	[H]
M	Transistor multiplier	[-]
P	Power	[dBm],[W]
P_{DC}	DC power from supply	[dBm],[W]
P_{in}	Input power from source	[dBm],[W]
P_{out}	Output power	[dBm],[W]
$P_{out,1dB}$	Output power at 1 dB compression	[dBm],[W]
$P_{out,avg}$	Average output power	[dBm],[W]
Q	Quality factor	[-]
R	Resistance	[Ω]
R_{in}	Input resistance as seen towards the input signal transformer	[Ω]
R_L	Load resistance after the output matching network	[Ω]
R_{load}	Load resistance as seen from the output of the transistors towards the output matching network	[Ω]
R_p	Parallel resistance	[Ω]
r_{par}	Parasitic resistance inductor	[Ω]
$r_{par,fmr}$	Parasitic resistance transformer	[Ω]
R_S	Input source resistance	[Ω]
R_s	Series resistance	[Ω]
R_{stb}	Resistor used to increase stability	[Ω]
V	Voltage	[V]
V_b	Biasing voltage	[V]
V_{bias}	Biasing voltage	[V]
V_C	Collector voltage	[V]
V_{DC}	Supply voltage	[V]
V_E	Emitter voltage	[V]
$V_{in,0deg}$	Sinusoidal input signal with 0° phase shift	[V]
$V_{in,180deg}$	Sinusoidal input signal with 180° phase shift	[V]
V_{knee}	Knee voltage	[V]
V_{out}	Output voltage signal between the push-pull transistors before the output matching network	[V]
$V_{out,final}$	Output voltage after the output matching network	[V]
V_T	Thermal voltage	[V]
Z	Impedance	[Ω]
Z_{in}	Input impedance as seen towards the input signal transformer	[Ω]
Z_L	Load impedance after the output matching network	
Z_{load}	Load impedance as seen from the output of the transistors towards the output matching network	[Ω]
Z_p	Parallel impedance	[Ω]
Z_s	Series impedance	[Ω]
Δ	Variation/deviation	[-]
η_c	Collector efficiency	[%]
$\eta_{c,peak}$	Peak collector efficiency	[%]
$\eta_{c,pP1dB}$	Collector efficiency at 1 dB compression	[%]
ω_d	Design frequency	[rad/s]

1 Introduction

In recent years, 5G has dominated headlines worldwide. Before the 5G network became available to consumers in 2020 [2], mobile phone companies had already introduced "5G-ready" phones even though countries had very little to no 5G coverage yet. Now, three years later, most populated areas are covered by a 5G network [7] and it is widely in use.

1.1. Motivation

Radio-frequency (RF) power amplifier (PA) modules are widely used in 5G wireless communication systems to drive antenna arrays in base stations. These modules generally contain Doherty power amplifiers which need to be driven, see Fig. 1.1. Currently, a "conventional" single-ended cascode PA is used as driver. However, to improve the linearity, bandwidth and efficiency of the driver, the following idea is proposed: a class-F PA based on a series push-pull power amplifier design, also known as a totem-pole PA due to the stacking of the transistors.

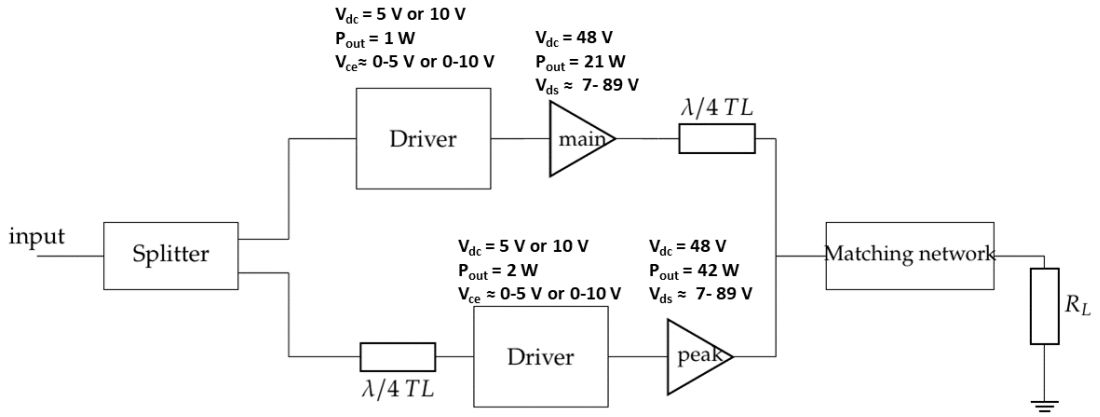


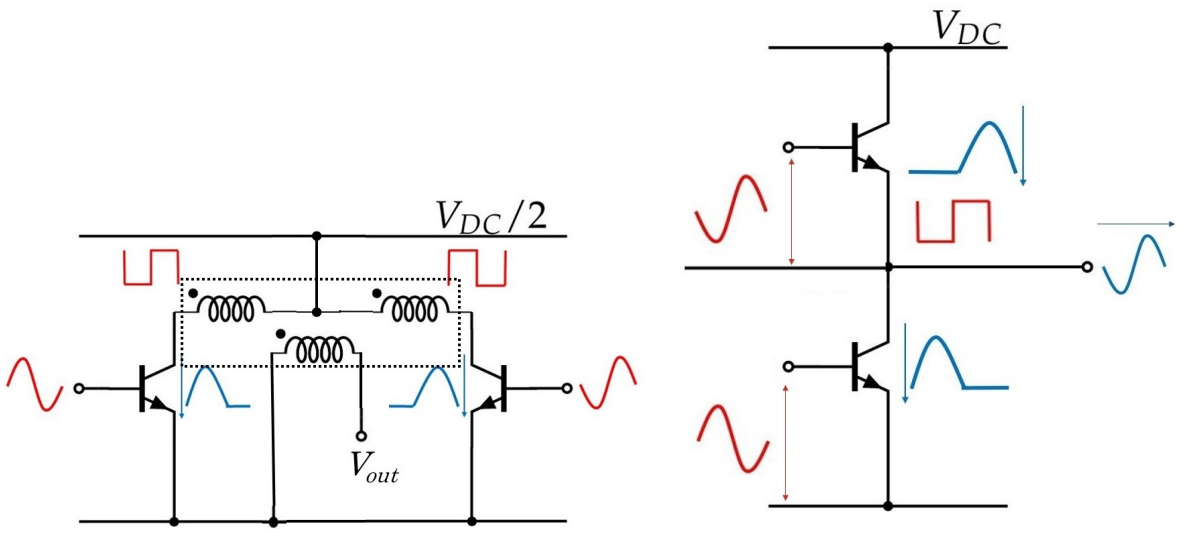
Figure 1.1: Doherty power amplifier including the pre-drivers. V_{dc} indicates the supply voltages, P_{out} the output power delivered by the amplifiers and V_{out} indicates the approximate voltage swings of the output.

Fig. 1.1 shows that two drivers are required. One to drive the main amplifier and one to drive the peaking amplifier of the Doherty. Both drivers are the same in design but scaled 1:2 between the driver

for the main amplifier and the driver for the peaking amplifier.

At low frequencies, push-pull amplifiers commonly consist of a combination of NPN and PNP transistors. This complementary push-pull PA has the advantage that no input balun is required. At RF frequencies, PNP transistors are less commonly available [12] and much slower than NPN transistors. Thus only NPN transistors [5] are used, see Fig. 1.2b.
The push-pull amplifier comes in two variants: a series push-pull and a parallel push-pull, see Fig. 1.2a. The benefit of a series push-pull compared to the parallel push-pull is that no output balun is required. However, since an NPN-only push-pull is designed, the input signal must be split into a 0° and a 180° input signal. This phase splitter can consist of:

- a phase-splitting transistor
- a shunt-regulated push-pull topology
- an input balun



(a) Parallel push-pull with voltage (red) and current (blue) waveforms. The inductors are magnetically coupled.

(b) Series push-pull with voltage (red) and current (blue) waveforms

Figure 1.2: Comparison between parallel push-pull (left) and series push-pull (right)

The series push-pull amplifier also has some benefits compared to the single-ended PA:

- The single-ended cascode PA has a choke inductor connected between V_{DC} and the transistor output, which may cause a slight drop in V_{DC} and introduce RF losses due to the parasitic resistance of the inductor.
- In the push-pull PA, the even harmonic tones do not need to be filtered using even harmonic traps, which simplifies the circuit, increases the bandwidth and reduces the RF loss of the output matching network.
- As both transistors contribute equally in terms of power and gain (both transistors act as common-emitter stages), the output voltage amplitude is limited to $V_{DC}/2$, ensuring that the voltage over the transistors will not peak beyond the breakdown voltage, hence increasing the reliability of the circuit.

Fig. 1.3 shows a simplified circuit of the single-ended power amplifier and Fig. 1.4 shows a simplified schematic of the proposed series push-pull amplifier. The output matching network (OMN) includes impedance matching and harmonic tuning if necessary.

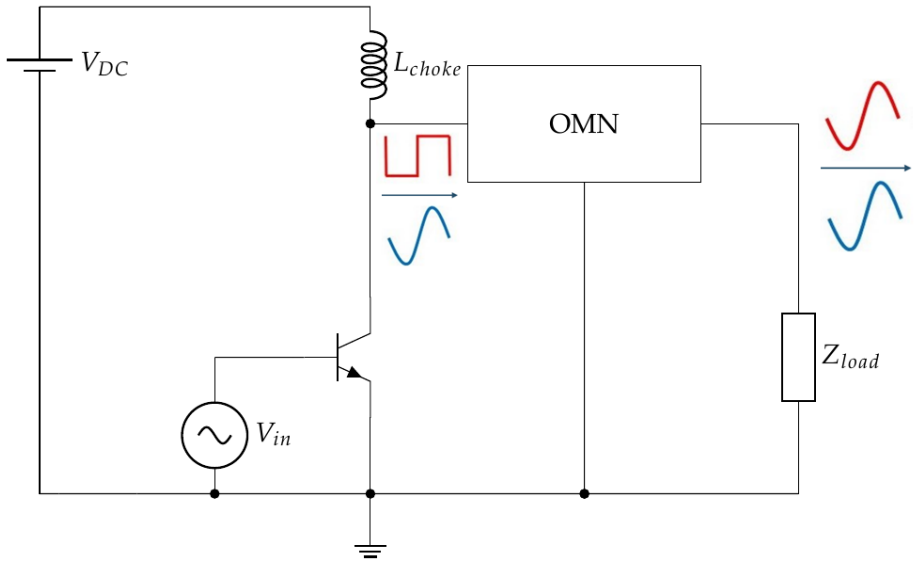


Figure 1.3: Simplified schematic of the sinlge-ended PA design.

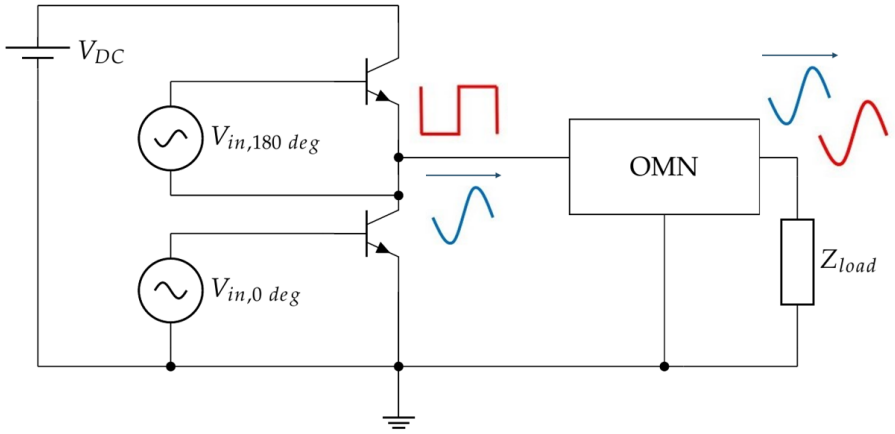


Figure 1.4: Simplified schematic of the proposed push-pull PA.

1.1.1. Class-F Power Amplifier

When designing an amplifier, multiple amplifier classes are taken into consideration. Typically, transistors operate as a current source or as a switch, resulting in linear and switching amplifiers respectively. Tab.1.1 [10] gives a short overview of the various linear and switching amplifier classes and their theoretical maximum efficiencies. As the table shows, all switching amplifiers can reach a maximum theoretical efficiency of 100%, although they typically achieve efficiencies of <85% [9, 10].

Table 1.1: Amplifier classes and their theoretical maximum collector efficiency.

Class	Maximum collector efficiency (%)	Mode of operation	Conduction angle (°)
A	50	current source	360
AB	50-70	current source	180-360
B	78.5	current source	180
C	78.5 - 100	current source	0-180
D	100	switch	50
E	100	switch	50
F	100	switch	50

In class-F operation, harmonic tuning at the output shapes the output waveform to increase the efficiency. The amplifier shows odd harmonics in the output voltage as shown in Fig. 1.5, assuming that the even harmonics are not present.

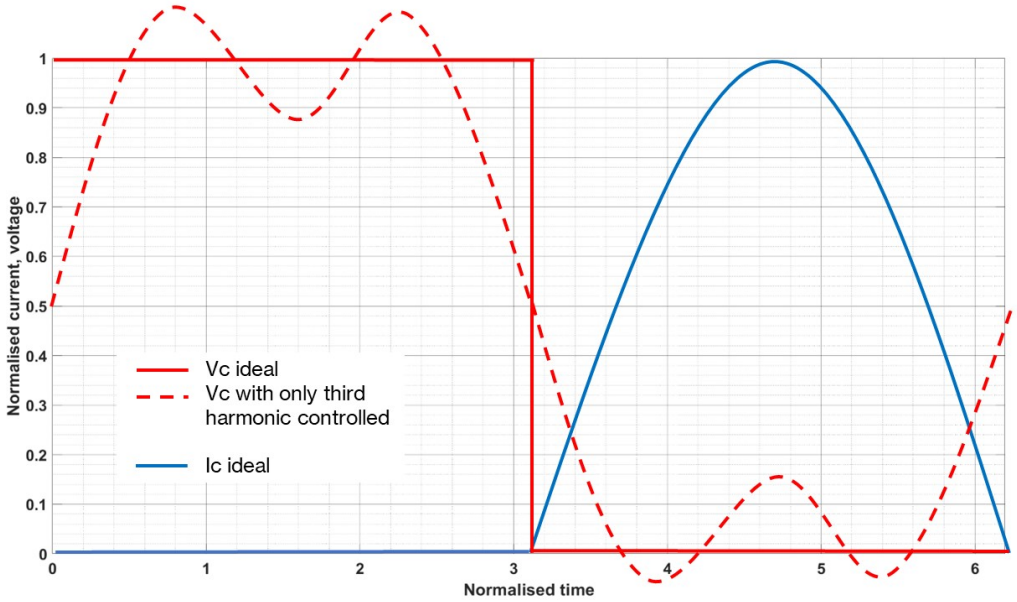


Figure 1.5: Output waveform class F [8]

In the push-pull topology, the even harmonics are already filtered out without the use of additional circuitry at the output, thus only the odd harmonics are present at the output voltage. Ideally, an infinite number of harmonics (n = ∞) is tuned out resulting in a square-wave output voltage, as shown in Fig. 1.6, but for practical reasons, harmonic tuning is usually performed up to the fifth harmonic.

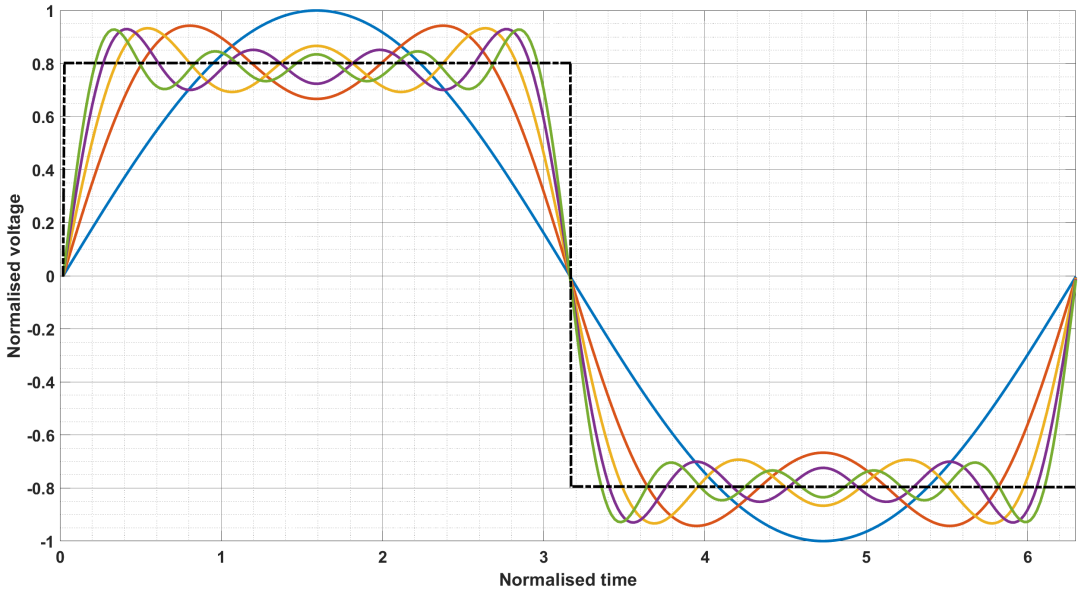


Figure 1.6: The building of a square wave [6] by tuning out the odd harmonics up to the 9th harmonic. The black line indicates the ideal square-waveform for n = ∞.

1.2. Aim of Research

This work aims to design a series push-pull power amplifier with high bandwidth and efficiency with an operating frequency of 3.6 GHz. A supply voltage of 5 V is available on the chip and therefore a design will be made with a 5 V voltage supply. Because the current single-ended PA has an output voltage amplitude equal to V_{DC} = 5 V, a fair comparison would be to design a series push-pull PA with an output voltage amplitude of 5 V as well. This would mean that V_{DC} should be 10 V as the output voltage amplitude of a push-pull PA is $V_{DC}/2$. The push-pull designs will be compared to the conventional single-ended design, to evaluate whether the push-pull design is indeed better in terms of efficiency and bandwidth. Tab.1.2 shows the design specifications of the amplifier.

Table 1.2: Design specifications of the push-pull totem-pole PA.

Parameter	Specification
Design frequency f_d (GHz)	3.6
Bandwidth (GHz)	1.0
$P_{out,1dB}$ (dBm) (1 dB compression)	30
Power gain (dB)	15
$\eta_{c,P1dB}$ (%)	80
AM-AM max (dB)	1.00
IMD3 (dBc)	-40 @ $P_{out,avg}$=22 dBm and 1 MHz tone-spacing
OIP3 (dBm)	42

The third order intercept point (IP3) is typically around 10 dB higher than the 1 dB compression point, as follows from Equation (1.1) [11].

$$\frac{A_{IP3}}{A_{1dB}} = \sqrt{\frac{4}{0.435}} = 9.6\ dB \approx 10\ dB \tag{1.1}$$

As the output power at 1 dB compression is 30 dBm, the OIP3 can be estimated to be around 30 dBm + 10 dB = 40 dBm. This is assuming that the output is only determined by the third harmonic. In reality, other harmonics are present as well, thus the OIP3 is slightly higher than 40 dBm. Therefore, the OIP3 should be around 42 dBm. Taking an average output power of 22 dBm, IMD3 can be estimated using Equation (1.2) [11].

$$OIP3 = P_{out,avg} - \frac{IMD3}{2} \rightarrow IMD3 = 2 \cdot P_{out,avg} - 2 \cdot OIP3 = 2 \cdot 22 - 2 \cdot 42 = -40\ dBc \tag{1.2}$$

The amplifier should have a 1 GHz bandwidth, of which the 3.4 GHz to 3.8 GHz frequency band is the most important. The bandwidth is determined based on the -3 dB points of the S21 parameter.

The circuits' efficiency is calculated as the collector efficiency. The collector efficiency determines the maximum efficiency at P_{1dB} that the circuit can deliver excluding post-PA losses from the output matching network and without considering input matching. Equation (1.3) shows the calculation of the collector efficiency.

$$\eta_c = \frac{P_{out}}{P_{DC}} \tag{1.3}$$

1.3. Outline of Thesis

A brief outline of the thesis is given below.

- Chapter 2 describes the design process of the single-ended and series push-pull power amplifiers. It includes intermediate simulations and the results of the design.
- Chapter 3 shows the simulation results of the completed designs, and compares them to one another. The simulations consist of a single-tone simulation and a two-tone simulation. One driver design is chosen based on the simulation results.
- Chapter 4 gives a conclusion on this work and recommendations for future work.

2

Design Considerations

This chapter elaborates on the choices made during the design of the circuit. First, the available transistors are discussed and a suitable transistor is chosen. Then the overall design is shown and simulated. To account for the temperature increase during operation, all simulations are done in a 100 degree Celsius temperature environment without self-heating of the transistors.

2.1. Single-Ended (Cascode) PA

The conventional single-ended cascode PA uses a combination of a high-voltage transistor and a low-voltage transistor in a cascoded configuration. The HV transistor is connected to the output, shielding the LV transistor from high peak voltages. An inductor is applied between the supply and the HV transistor, which functions as an RF choke and is also used to tune out the output capacitance of the PA as well as the capacitive loading of the H2-trap. In contrast to the push-pull amplifier, this PA does not suppress even harmonic tones, and thus a second harmonic trap is added to the output. A third harmonic notch can be added if necessary. A simplified version of the schematic is shown in Fig. 2.1.

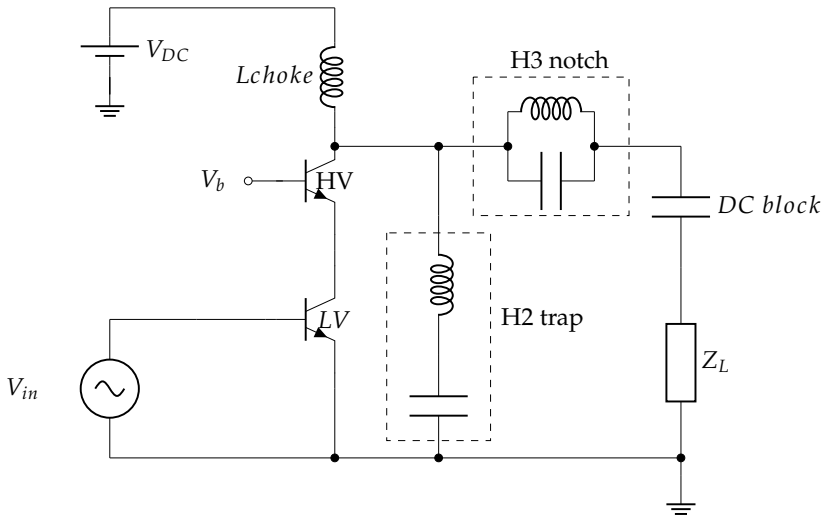


Figure 2.1: Simplified schematic of the conventional cascoded PA, excluding input matching network and transistor biasing.

The design of the single-ended PA is discussed simultaneously with the design of the series push-pull PA, as the design steps are similar.

2.2. Series Push-Pull PA

The main component of the PA is the push-pull totem-pole structure of the power amplifier. For comparison, multiple structures are made:

- 2x HV push-pull V_{DC} = 5 V (Fig. 2.2)
- 2x HV push-pull V_{DC} = 10 V (Fig. 2.2)
- 2x LVLV push-pull V_{DC} = 5 V (Fig. 2.3a)
- 2x LVHV push-pull V_{DC} = 10 V (Fig. 2.3b)

Fig. 2.2 shows the series push-pull design using 2 HV transistors and either a 5 V of 10 V supply voltage.

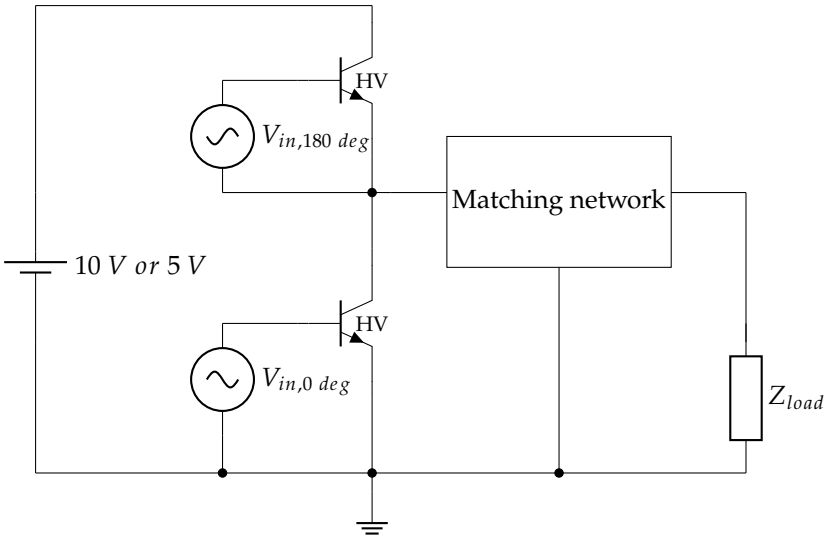
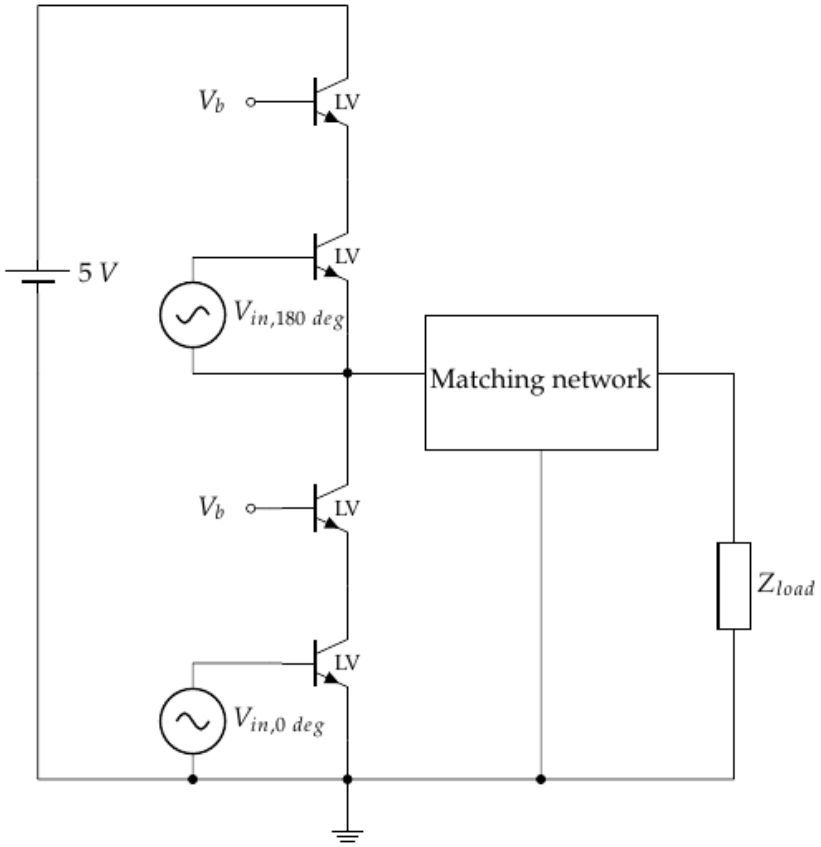
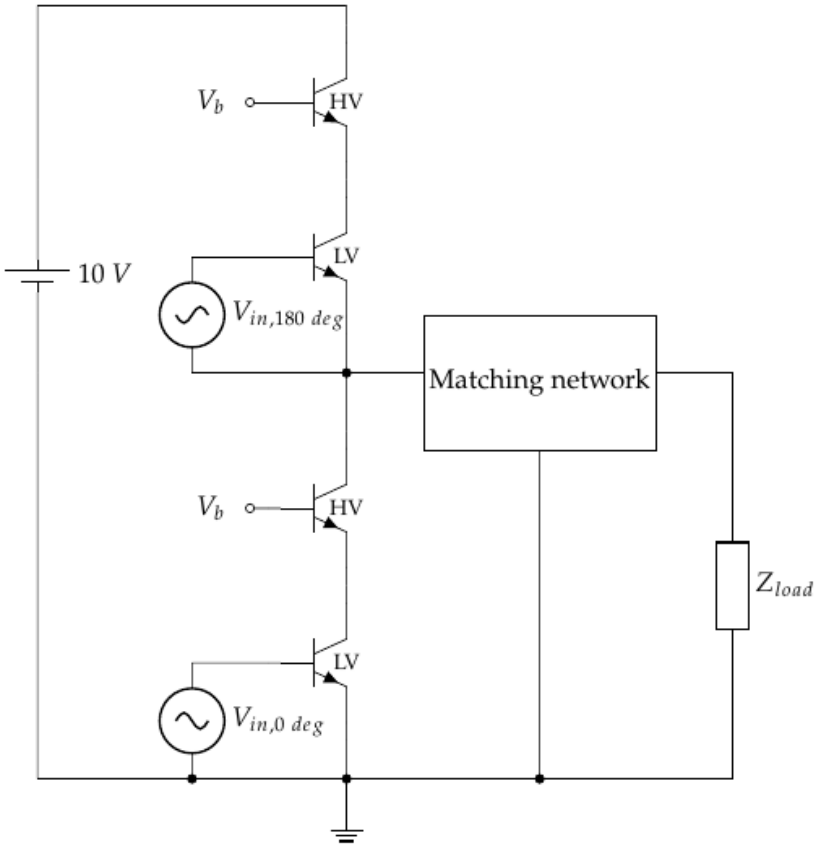


Figure 2.2: Series push-pull with 2 HV transistors, excluding input matching network and transistor biasing.

Fig. 2.3a shows the series push-pull design using 2x LVLV cascoded transistors and a 5 V supply. This would distribute the 5 V_{pk-pk} output over the 2 cascoded LV transistors, ensuring that they do not exceed their breakdown voltage.
Fig. 2.3b shows a similar design but with an LV and HV transistor in cascoded configuration. Because the HV transistor allows for a higher peak-to-peak output voltage, a 10 V supply voltage is used.



(a) 2x LVLV push-pull



(b) 2x LVHV push-pull

Figure 2.3: 2x LVLV (top) and 2x LVHV (bottom) push-pull, excluding input matching network and transistor biasing.

The following components of the circuits are discussed separately:

- Initial output matching network
- Transistor sizing
- Linearity
- Input balun
- Final output matching network
- Input matching network

2.3. Initial Output Matching Network

As the output power and voltage are known, an initial output matching network (I.OMN) can already be designed for the initial design process. This output matching network is used as a starting point for the design and does not include the transistor's output capacitance. The I.OMN is later modified to incorporate more components, leading to the final OMN discussed in Section 2.4.2.

2.3.1. Required Load Resistance

The supply voltage influences the amplitude of the output voltage swing of the amplifier. The output voltage determines the required load impedance of the amplifier to meet the 30 dBm output power requirement.

The single-ended cascode PA is supplied with 5 V. As its output is connected to the supply voltage via a choke-inductor, the output voltage amplitude can almost be 5 V.

The push-pull amplifiers produce an output voltage amplitude which can almost be half of the supply voltage, as each transistor is supplied with the same voltage and biasing, thus each transistor contributes equally to the circuit.

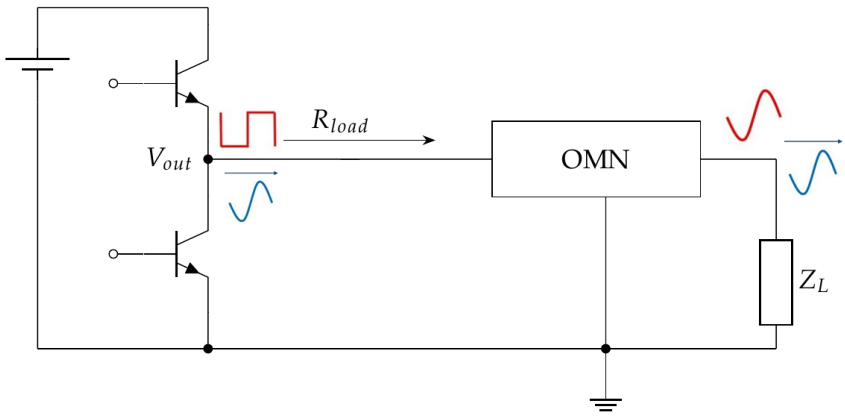


Figure 2.4: Output of the push-pull amplifier with the required load resistance R_{load}.

The load resistance at the output of the push-pull, see Fig. 2.4, is determined by the RMS output voltage. The calculation for R_{load} is done for all 4 circuit topologies. Equation (2.1) shows the calculation for the 2x HV push-pull with a 5 V supply voltage, Tab.2.1 shows the calculated load resistances for all

push-pull circuits.

$$V_{out,RMS} = \frac{4(0.5 \cdot V_{DC} - V_{knee})}{\pi\sqrt{2}} = \frac{4(2.5 - 0.25)}{\pi\sqrt{2}} = 2.0\ V$$
$$R_{load} \leq \frac{V_{out,RMS}^2}{P_{out}} = 4.1\ \Omega \tag{2.1}$$

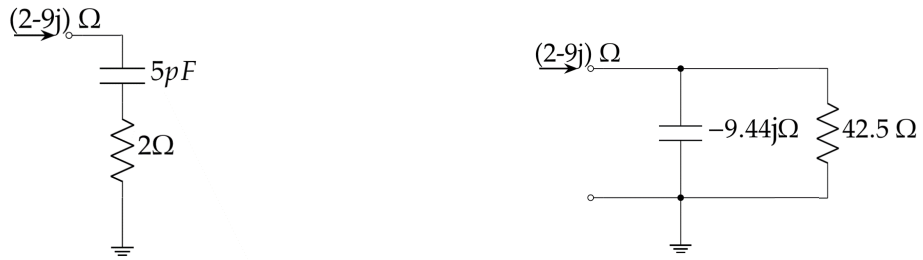
In these calculations, the output power is assumed to be 1W at the output of the transistors, before the output matching network. There is some loss in the output matching network (post-PA loss), thus the power delivered to the load is slightly less than 1W. Assuming a loss of 1.5 dB in the output matching network, the required load resistance is also calculated for an output power of 31.5 dBm, or 1.4 W. The results are shown in Tab.2.1.

Table 2.1: Load resistances of the single-ended PA and the 4 push-pull topologies, with and without power loss in the output matching network.

	V_{knee} (V)	$V_{out,RMS}$ (V)	R_{load} (Ω)	R_{load} with loss (Ω)
1x LVHV 5 V	0.5	4.1	16.4	12.0
2x HV 5 V	0.25	2.0	4.1	2.9
2x HV 10 V	0.25	4.3	18.2	13.2
2x LVLV 5 V	0.5	1.8	3.2	2.3
2x LVHV 10 V	0.5	4.1	16.4	12.0

2.3.2. Load Impedance Z_L

Before a matching network can be designed, the load impedance Z_L has to be determined. The push-pull driver will drive a >20 W LDMOS with input impedance (2 - 9j) Ω. The FET-output stage has an input capacitance of -9j Ω and a gate resistance of 2 Ω. This can be modelled as shown in Fig. 2.5. Fig. 2.5a shows the (2-9j) Ω impedance as a combination of a series capacitor and resistor, which models the real nature of the load. Fig. 2.5b shows the parallel configuration of the load.



(a) Series load impedance. **(b)** Parallel load impedance.

Figure 2.5: Load impedance of (2-9j) Ω at 3.6 GHz, series (left) and parallel (right) equivalent circuits.

2.3.3. Initial Output Matching Network (I.OMN) of the Single-Ended PA

The output matching network of the single-ended PA requires a second harmonic (H2) trap to tune out the second harmonic at the output. Optionally, the third harmonic can be tuned out as well with a third harmonic (H3) trap, but this is initially left out. In case the third harmonics are not suppressed sufficiently in the final design, the third harmonic notch will be added to the circuit. Fig. 2.6 shows the output matching network of the single-ended PA with second harmonic trap.

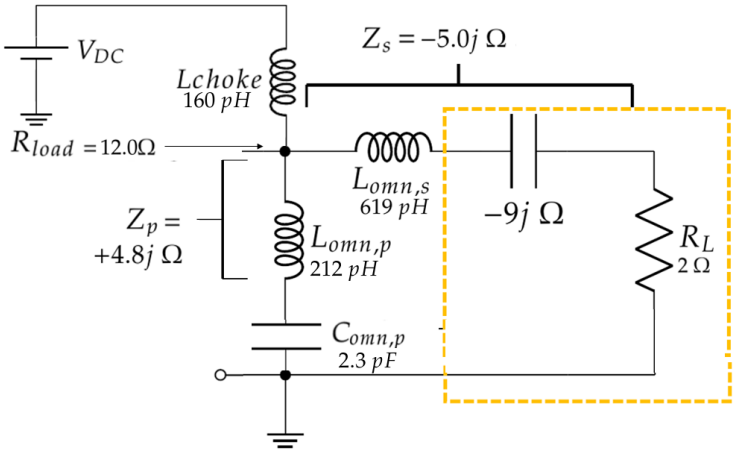


Figure 2.6: Initial matching network of the single-ended PA, with H2 trap.

As previously determined, Z_L = (2-9j) Ω and R_{load} should be 12.0 Ω to account for the post-PA loss. To ensure that the bandwidth of the PA is not limited by the output matching network, the matching network must have an appropriate Q-factor. The matching network is designed using reactive components which have a frequency-dependent impedance, thus limiting the bandwidth of the circuit. The bandwidth can be approached by dividing the design frequency f_d by the Q-factor, as Equation (2.2) shows. To achieve a 1 GHz bandwidth, the Q-factor must be 3.6 or less.

$$Q < \frac{f_d}{BW} = 3.6 \tag{2.2}$$

This output matching network has a Q-factor of 2.5, which is sufficient. The series and parallel impedance can be determined with Q = 2.5:

$$-Z_s = -(Q \cdot R_L)j = -5.0j\ \Omega \tag{2.3}$$

The parallel impedance is determined in Equation (2.4).

$$+Z_p = +\left(\frac{R_{load}}{Q}\right)j = +4.8j\ \Omega \tag{2.4}$$

To remove the second harmonics, a capacitor is placed in series with the parallel inductor $L_{omn,p}$ with its value calculated in Equation (2.5).

$$C_{omn,p} = \frac{1}{(2 \cdot \omega_d)^2 \cdot L_{omn,p}} = 2.3\ pF \tag{2.5}$$

The negative impedance added to the output of the single-ended PA can be tuned out using the choke inductor L_{choke} between V_{DC} and V_{out} with the value calculated in Equation (2.6).

$$L_{choke} = \frac{1}{\omega_d^2 \cdot C_{omn,p}} = 160\ pH \tag{2.6}$$

2.3.4. Initial Output Matching Network (I.OMN) of the Series Push-Pull PA

The matching network of the push-pull PAs is similar in design to that of the single-ended PA, but without the H2 trap as the second harmonics are already removed from the output signal.
Three options are considered for the output matching network, and the output matching network with the best bandwidth and easiest implementation is chosen. The following calculations are shown only for the 2x HV 5 V push-pull topology, where the impedance is transformed to R_{load} = 2.9 Ω as determined in Tab.2.1 to deliver 30 dBm output power to the next stage.

OMN Option 1: LC Matching Network

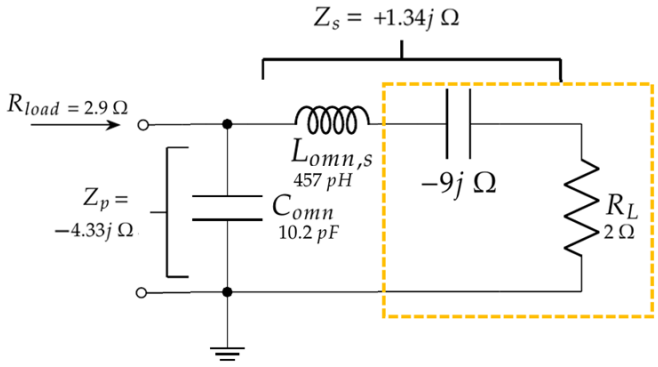
The first option considered is an OMN consisting of a capacitor (C_{omn}) and an inductor (L_{omn}). The Q-factor of this circuit is 0.67 (see Equation (2.2)). The series impedance Z_s of the output matching network takes the -9j capacitance of Z_L into account and is determined in Equation (2.7).

$$+Z_s = +(Q \cdot R_L)j = +1.34j\ \Omega \tag{2.7}$$

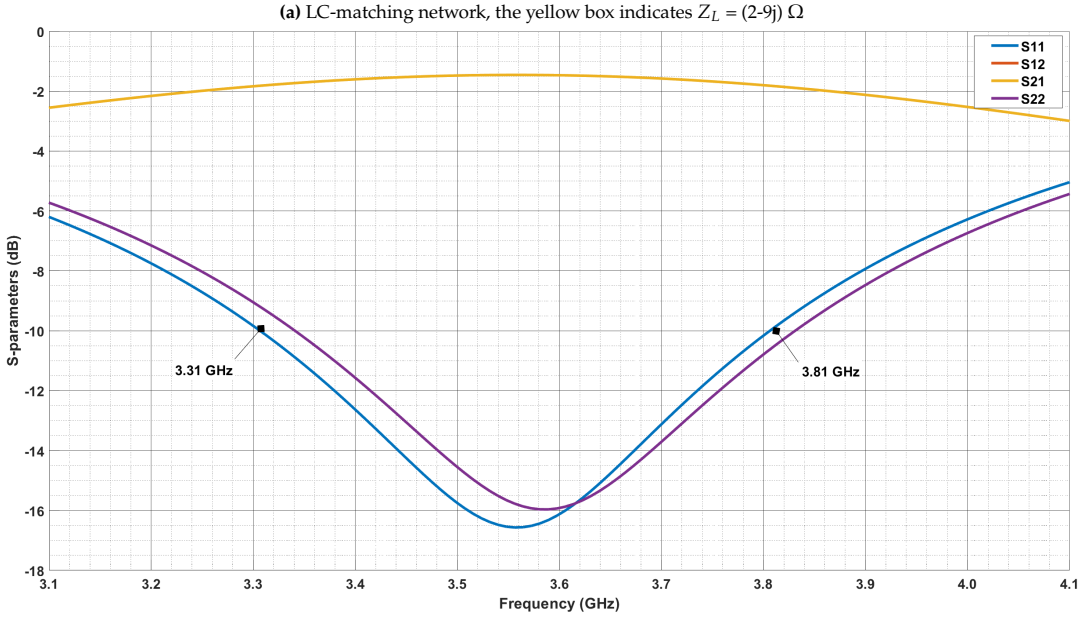
The parallel impedance is determined in Equation (2.8).

$$-Z_p = -(\frac{R_{load}}{Q})j = -4.33j\ \Omega \tag{2.8}$$

The resulting circuit is shown in Fig. 2.7a and its s-parameters are shown in Fig. 2.7b.



(a) LC-matching network, the yellow box indicates Z_L = (2-9j) Ω



(b) S-parameters of the LC-matching network.

Figure 2.7: LC matching network schematic and S-parameters

Fig. 2.7b shows the -10 dB points of S11 at 3.3 GHz and 3.8 GHz, indicating the OMN has a 500 MHz bandwidth.

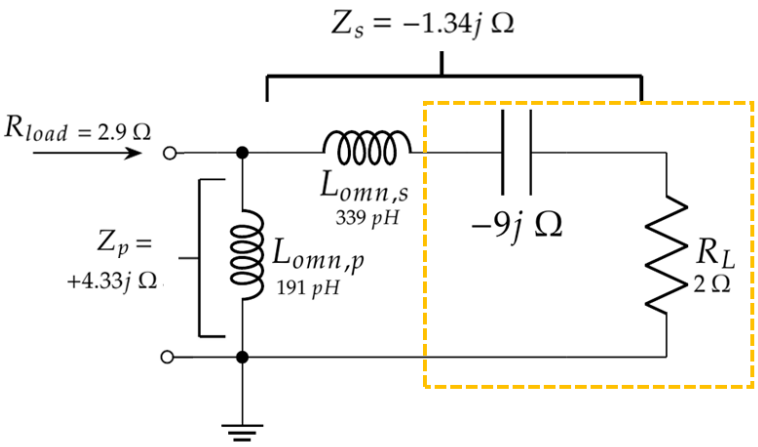
OMN Option 2: L Matching Network

The second OMN considered consists of only inductors. A series inductor ($L_{omn,s}$) and a parallel inductor ($L_{omn,p}$). This circuit is similar to the first OMN, only now the series impedance Z_s is inductive

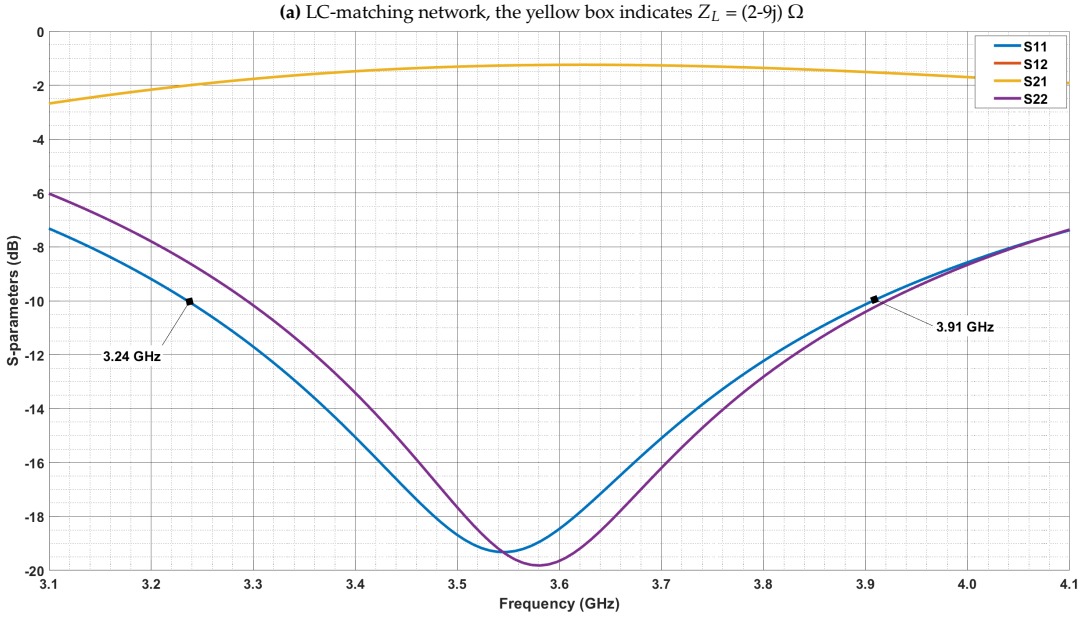
and the parallel impedance Z_p is inductive, resulting in an L-only matching network.

$$\begin{aligned} -Z_s &= -(Q \cdot R_L)j = -1.34j\ \Omega \\ +Z_p &= +\left(\frac{R_{load}}{Q}\right)j = +4.33j\ \Omega \end{aligned} \tag{2.9}$$

The resulting circuit is shown in Fig. 2.8a and its s-parameters are shown in Fig. 2.8b.



(a) LC-matching network, the yellow box indicates Z_L = (2-9j) Ω



(b) S-parameters of the L-matching network.

Figure 2.8: L matching network schematic and S-parameters

Fig. 2.8b shows the -10 dB points of S11 at 3.2 GHz and 3.9 GHz, indicating the OMN has a 700 MHz bandwidth.

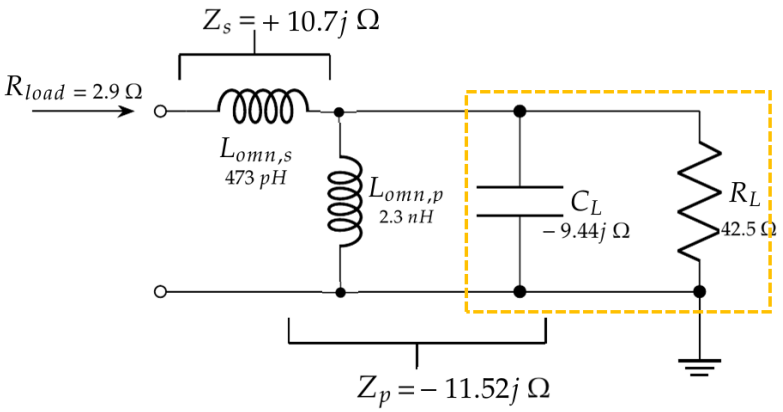
OMN Option 3: L Matching Network

The third OMN also consists of only inductors, but now the parallel equivalent impedance of Z_L is considered (42.5-9.44j) Ω. The Q-factor of this circuit is higher than the previous circuits: 3.69. To reduce this Q-factor, the matching network can be split into two parts, transforming the Z_L impedance to an intermediate impedance, which will in turn be transformed into 2.9 Ω. However, the OMN has been

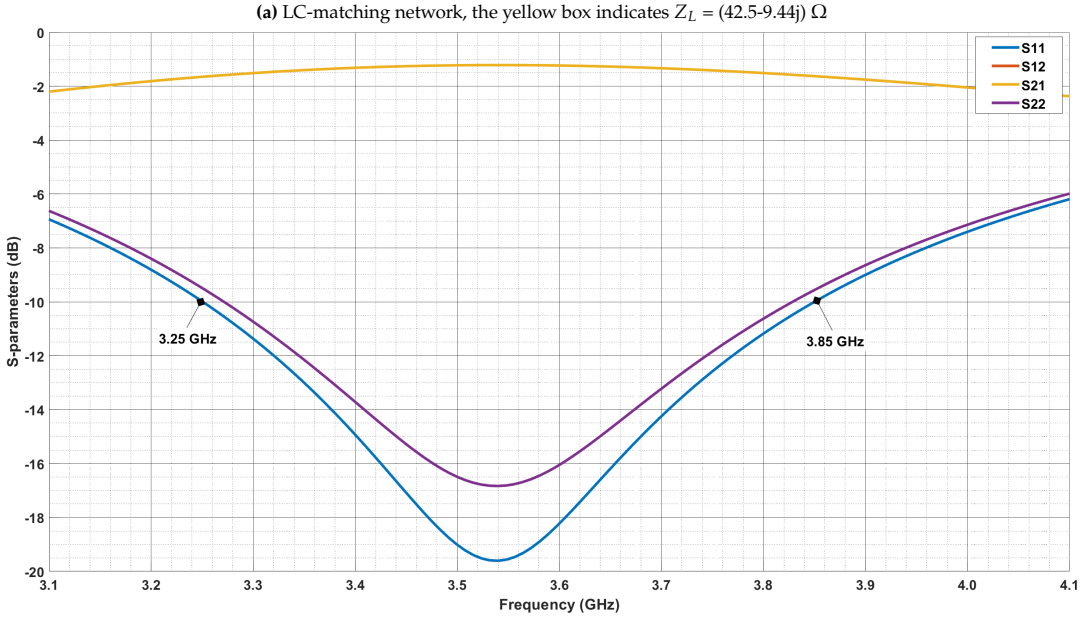
designed with the 3.69 Q-factor.

$$\begin{aligned} +Z_s &= +(Q \cdot R_L)j = +10.7j\ \Omega \\ -Z_p &= -\left(\frac{R_{load}}{Q}\right)j = -11.52j\ \Omega \end{aligned} \tag{2.10}$$

The resulting circuit is shown in Fig. 2.9a and its s-parameters are shown in Fig. 2.9b.



(a) LC-matching network, the yellow box indicates Z_L = (42.5-9.44j) Ω



(b) S-parameters of the L-matching network.

Figure 2.9: LC matching network schematic and S-parameters

Fig. 2.9b shows the -10 dB points of S11 at 3.25 GHz and 3.85 GHz, indicating the OMN has a 600 MHz bandwidth.

I.OMN Comparison and Choice

The bandwidths of the three output matching networks are similar, as Tab.2.2 shows. The table also shows that the first OMN option performs worst in terms of S11 value at the design frequency and bandwidth, thus leaving the L-matching networks as a better choice. Although the third OMN has a much higher Q-factor, its bandwidth and S11 value are similar to the second OMN design. Implementation-wise, the series inductor of the third OMN design can be implemented with a bondwire between the output of this driver and the input of the next stage, while the shunt inductor can be used to bias the input of the next stage.

Table 2.2: Comparison of the three I.OMN designs.

OMN	Q	S11 @f_d (dB)	Bandwidth (MHz)
Option 1: LC	0.67	-16	500
Option 2: L	0.67	-18.5	700
Option 3: L	3.69	-18.3	600

As the third I.OMN design would also be a practical solution, the output matching networks are designed using this topology.

Table 2.3: Inductor values of the I.OMN for all circuit designs

Circuit	R_{load} Ω	Q of the OMN	$L_{omn,s}$ (pH)	$L_{omn,p}$ (pH)
1x LVHV 5 V	12.0	1.6	612	212
2x HV 5 V	2.9	3.69	473	2300
2x LVLV 5 V	2.3	4.2	427	6200
2x HV 10 V	13.2	1.5	875	626
2x LVHV 10 V	12.0	1.6	849	647

2.4. Transistor Sizing

In order for the push-pull to operate and provide sufficient gain to achieve the desired output power, the transistors need to be sized properly.

2.4.1. Biasing and Sizing of the Transistor

Before the transistor can be sized, it needs to be biased. The biasing of the transistor is a trade-off: a higher biasing voltage means the collector current increases as well, and thus the efficiency of the amplifier decreases. However, the transistor is pushed further into linear operation, which decreases the AM-AM and AM-PM distortion.
Fig. 2.10 shows a simplified version of an ideal biasing circuit for the 2x HV push-pull design.

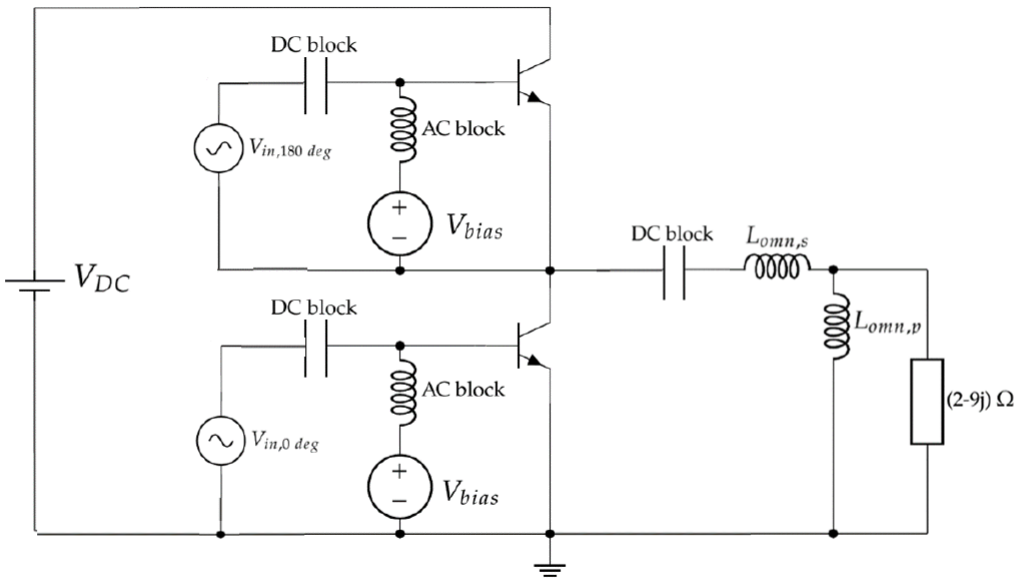


Figure 2.10: The circuit of the 2x HV push-pull design with biasing voltage, excluding input matching network.

Biasing Circuit

The voltage source V_{bias} is not a realistic and practical implementation of the biasing voltage. A practical solution to the biasing of the transistor is shown in Fig. 2.11. Here, a current I_{bias} is set and fed to the transistor Q_{bias}. This transistor is a copy of transistor Q but sized much smaller to reduce the losses in the transistor. The base voltage of Q_{bias} is copied to the base of Q.

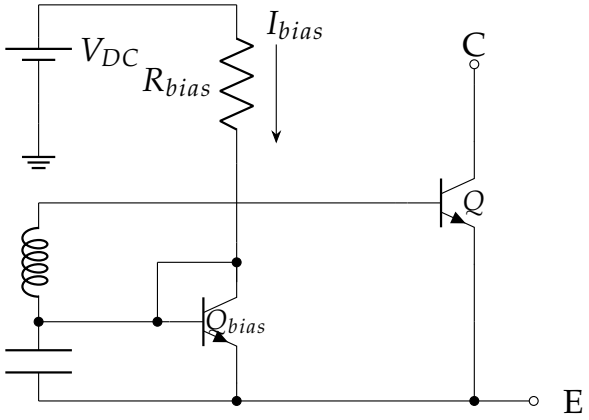


Figure 2.11: Practical implementation of V_{bias}.

In the following simulations, an ideal biasing circuit is used for simplicity, but it is based on Fig. 2.11. Fig. 2.12 shows the ideal biasing circuit used in the simulations of the 2x HV push-pull PAs.

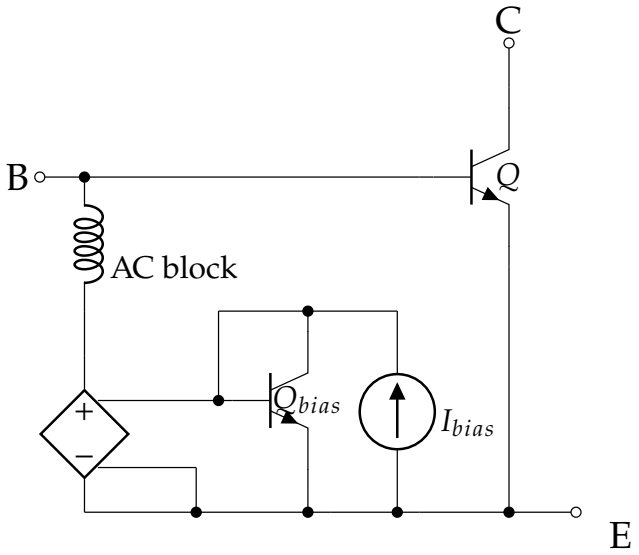


Figure 2.12: Biasing circuit used in simulation. The two transistors are identical, the voltage controlled voltage source has a gain of 1 and I_{bias} is the variable used to bias the transistor.

As the cascoded push-pull PAs require an additional biasing voltage for the top transistor (the transistor that does not receive the input signal), an additional voltage source and the decoupling capacitor are added to the circuit. The resulting circuit can be seen in Fig. 2.13.

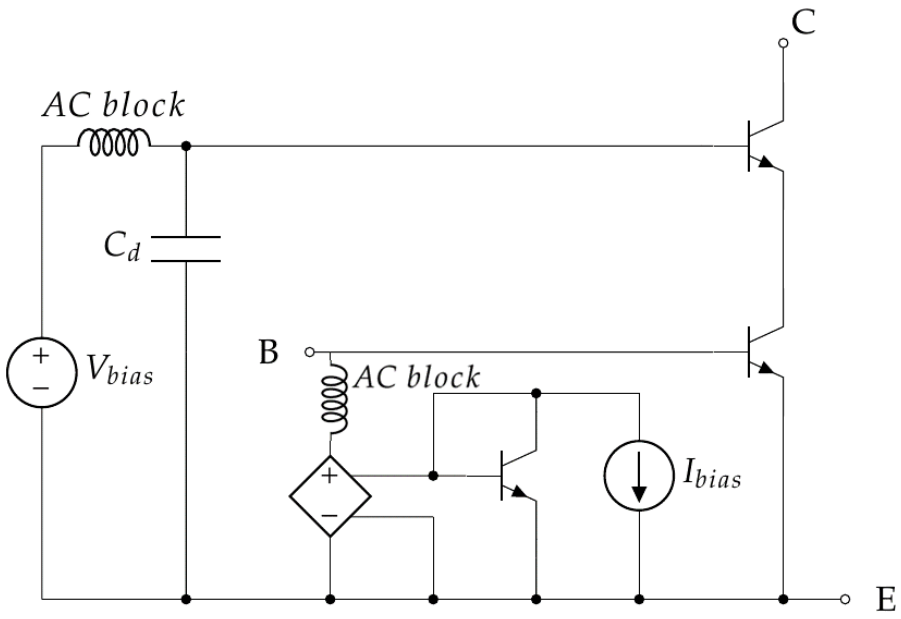


Figure 2.13: Biasing circuit for the cascoded transistors.

Transistor Sizing

All designs are biased and sized in a similar way. The 2x HV push-pull design only needs the biasing I_{bias} at the input of the two transistors. The other designs, however, require an additional biasing voltage to drive the additional two transistors, see Fig. 2.13.

The simulation results of the 2x HV push-pull PA with a 5 V supply are discussed first. This PA has two transistors, each sized equally. Fig. 2.14 shows the voltage at the output V_{out}. Ideally, the voltage has a square waveform swinging from 0 V to 5 V. The difference in output voltage waveform and knee-voltage for varying M can clearly be seen in the figure. A lower multiplier (blue) results in a higher knee-voltage V_{knee} and thus less efficiency, while a large multiplier (yellow) has a lower V_{knee} and therefore its waveform resembles the square waveform the most.

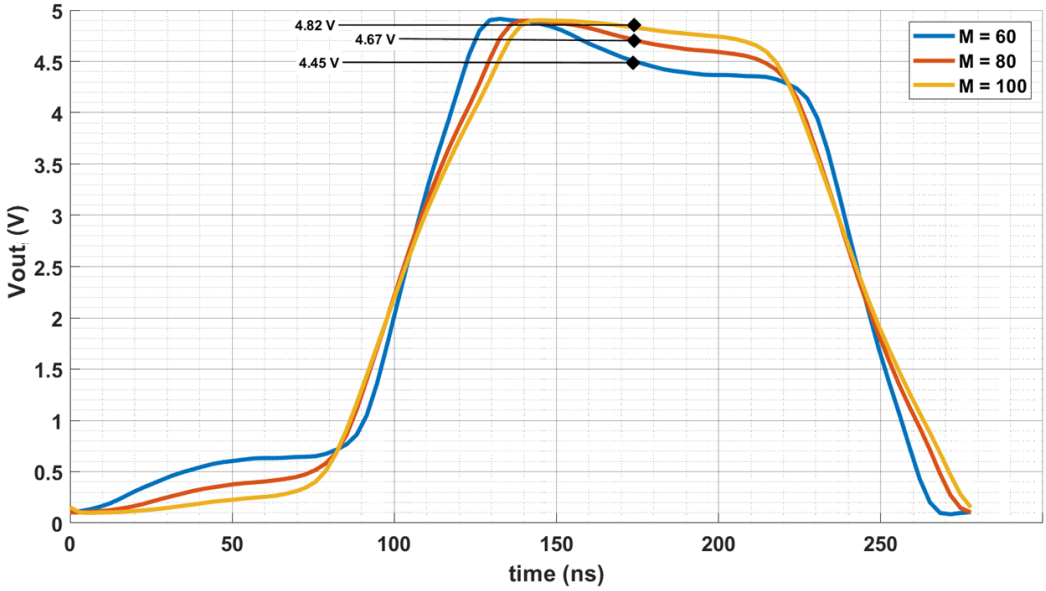
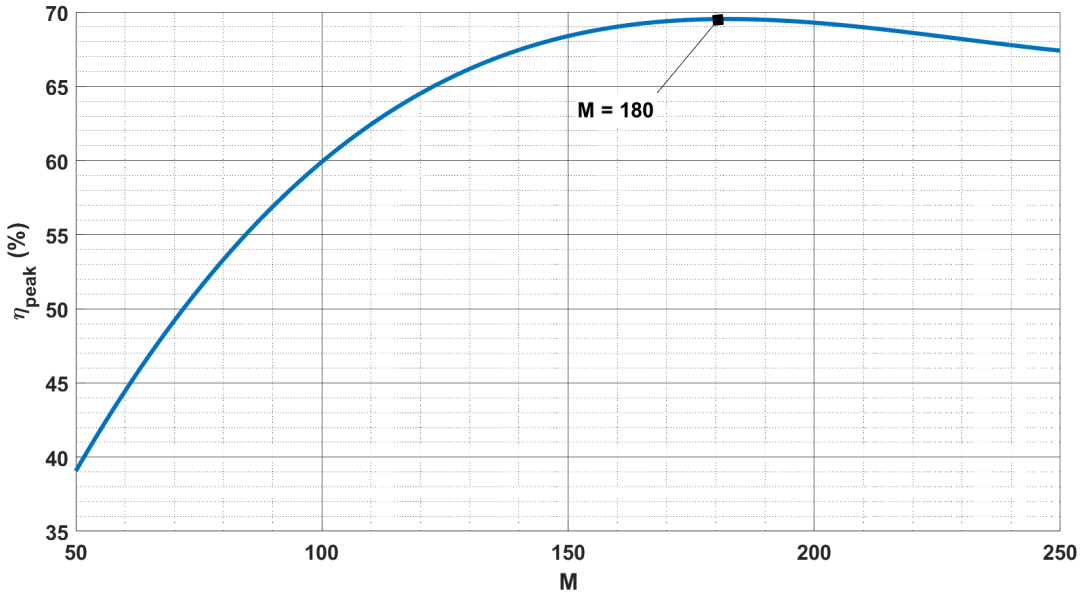
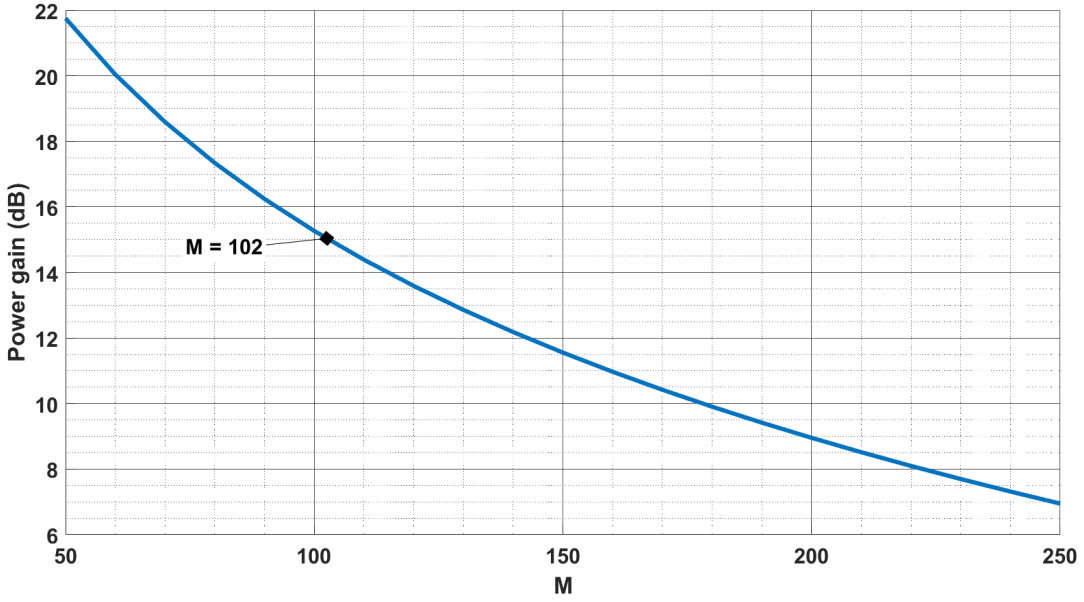


Figure 2.14: 2x HV push-pull with V_{DC} = 5 V and I_{bias} = 80 mA. Transient simulation of V_{out} for 3 values of multiplier M for a sinusoidal input signal. Ideally, V_{out} is a square wave from 0 V to 5 V. A higher M results in a smaller headroom which increases efficiency.

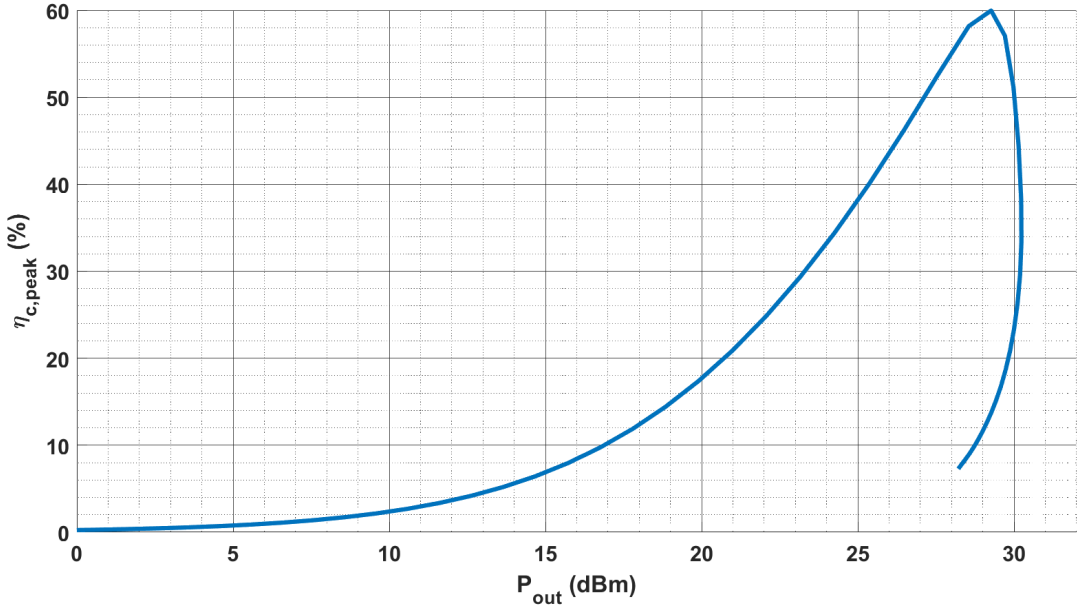
Plotting the peak efficiency against the multiplier shows that there is an optimum for M, see Fig. 2.15a. The lowest possible biasing voltage will result in the highest peak efficiency. For the moment, the biasing current is therefore set to 80 mA. Later in the design process, the current can be increased or decreased if necessary.
The power gain is also dependent on the transistor size as Fig. 2.15b shows. The transistor is sized as large as possible for maximum efficiency, whilst still meeting the specification of 15 dB power gain.



(a) η_{peak} vs. M for $P_{out,max} = 30\ dBm$.



(b) G_p vs. M for $P_{out,max} = 30\ dBm$.



(c) $\eta_{c,peak}$ vs. P_{out} for $I_{bias} = 80\ mA$ and M = 100.

Figure 2.15: η_{peak} and G_p vs. M of the 2x HV 5 V push-pull with $I_{bias} = 80\ mA$.

The cascoded push-pull PA, as well as the single-ended cascoded PA, is sized with multiplier M for the top and bottom transistor, as well as biasing voltage V_{bias}. The values for a power gain of 15 dB and the highest efficiency are chosen.
Tab.2.4 shows the results of the biasing voltages and transistor sizes.

Table 2.4: Variable and parameter values after biasing and sizing the transistors.

Circuit	M_t	M_b	$V_{bias,t}$ (V)	C_d (pF)	G_p (dB)	$\eta_{c,peak}$ (%)	$P_{out,max}$ (dBm)
1x LVHV 5 V	30	120	1.8	18	28.2	55.2	30.2
2x HV 5 V	100	-	-	-	17.7	59.9	29.5
2x HV 10 V	85	-	-	-	16.7	52.4	31.1
2x LVLV 5 V	30	80	1.4	7	15.4	60.4	30.1
2x LVHV 10 V	40	70	1.2	14	18.8	55.5	30.4

These values are mere starting points for the design. As more components are added to the circuit, the transistor size and V_{bias} are modified to achieve high efficiency whilst still meeting all other specifications. The final values will be presented at the end of this work.

2.4.2. Parasitic Output Capacitance

Each transistor has parasitic capacitances which need to be taken into account, as they contribute to the total parasitic capacitance seen at the output C_{out}, see Fig. 2.16. The output capacitance is tuned out at the design frequency by a parallel output inductor L_{po} with value $\frac{1}{\omega_d^2 \cdot C_{out}}$. The output capacitance is largely dependent on the size of the transistors. As the transistor size or multiplier increases, so does the output capacitance.
The parasitic capacitances C_π and C_μ are shown in the hybrid-pi model of the BJT transistor in Fig. 2.17.

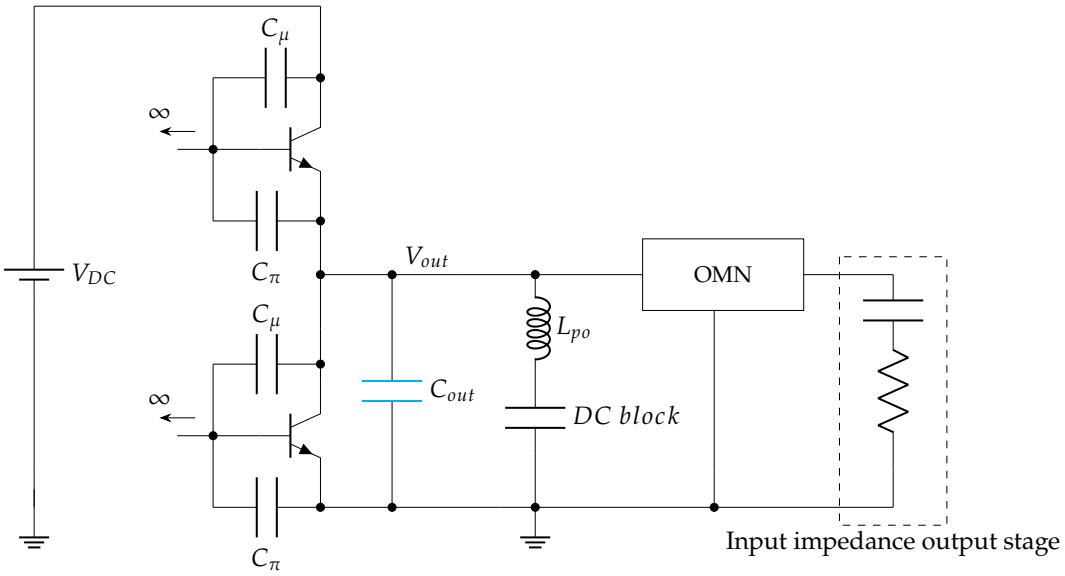


Figure 2.16: Series push-pull PA with parasitic capacitances and parallel output inductor L_{po}. C_{out} (highlighted in blue) represents the total parasitic capacitance at the output of the push-pull stage.

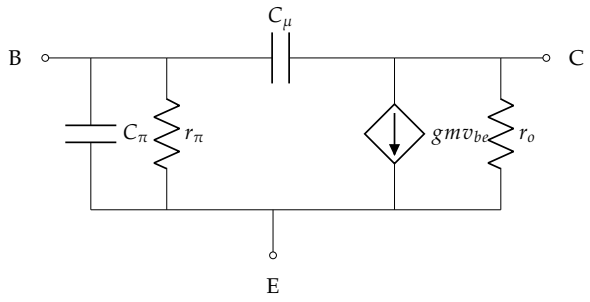


Figure 2.17: Hybrid-pi model of one BJT.

Due to the Miller effect at the output, the parasitic capacitance at the output of one transistor is:

$$C_{par} = \left(1 - \frac{1}{A_v}\right) C_\mu = \left(1 + \frac{1}{g_m(R_{load}//r_o)}\right) C_\mu \tag{2.11}$$

$|A_v| = g_m(R_{load}//r_o) >> 1$. Therefore Eq.2.11 can be approximated to $C_{par} \approx C_\mu$.

In Cadence, C_μ is calculated using a dummy transistor in the circuit, see Fig. 2.18, which copies the collector and emitter voltages of the transistor and measures the collector current. In Fig. 2.18, only the top HV transistor is copied. As both top and bottom transistors are identical, the value of C_μ is the same for both transistors.

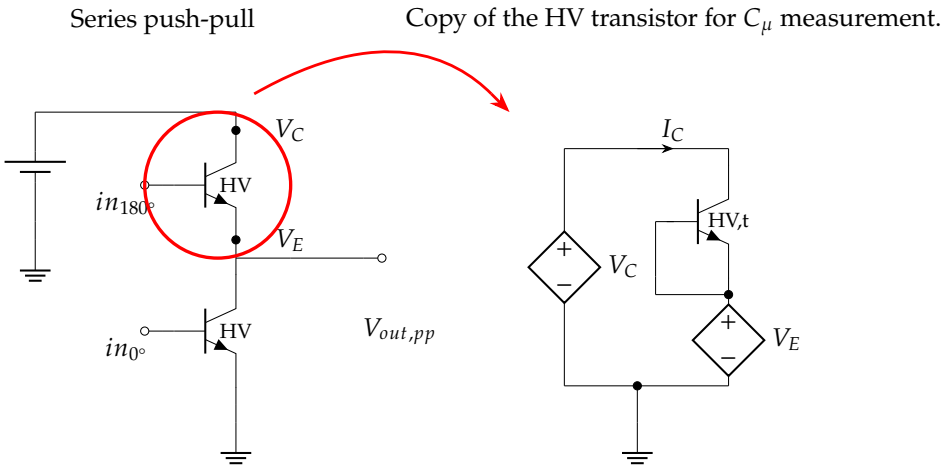


Figure 2.18: Dummy transistor for parasitic output capacitance measurement. The dummy transistor is a copy of the top HV transistor in series push-pull configuration.

Eq.2.12 shows the calculation of the parasitic capacitor of one transistor.

$$C_\mu = \frac{\Im(Y_{HV,t})}{\omega_d} = \Im\left(\frac{I_{C,t}}{V_{C,t}}\right) \cdot \frac{1}{\omega_d} \tag{2.12}$$

2.4.3. Final Output Matching Network

An output inductor can be added to tune out C_{out} at the output of the push-pull amplifier. The parallel output inductor is calculated as in Eq.2.13. Since C_{out} needs to be tuned out for higher harmonics as well, the ideal value of L_{po} is likely smaller than calculated in Eq.2.13. The ideal value is determined at the end of the design by sweeping L_{po}.

$$L_{po} = \frac{1}{(\omega_d^2 \cdot C_{out})} \tag{2.13}$$

The output inductor can be converter to a series equivalent using a Q-factor of 3.6 at most as Eq.2.14 shows.

$$\frac{R_p}{R_s} = 1 + Q^2 \rightarrow R_s = \frac{R_p}{1 + Q^2} \tag{2.14}$$

This series inductance can then be absorbed into the series inductor of the OMN, resulting in Fig. 2.19.

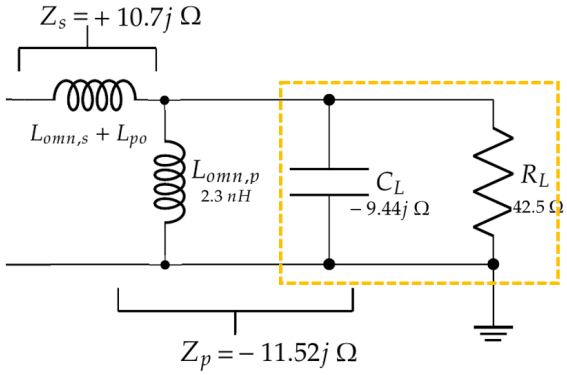


Figure 2.19: Final OMN with L_{po} absorbed into $L_{omn,s}$.

2.5. Linearity

To improve the linearity of the circuit, a feedback capacitor C_{fb} is added between the collector and base of the transistor as Fig. 2.20 shows. As $V_{out,pp}$ varies, V_{CE} over both transistors varies as well, see Fig. 2.21a and Fig. 2.21b. As the voltage V_{BE} is very small and thus negligible, a similar voltage difference is seen over C_{fb} as well. As Fig. 2.21 shows, the waveforms are nearly identical, with a small peak-to-peak voltage difference between Fig. 2.21a and Fig. 2.21b of 20 mV due to the 20 mV peak-to-peak voltage swing of Vbe.

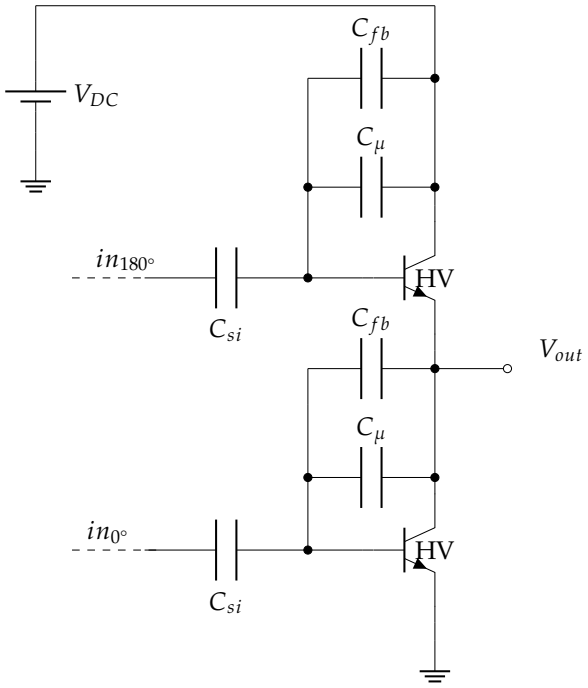
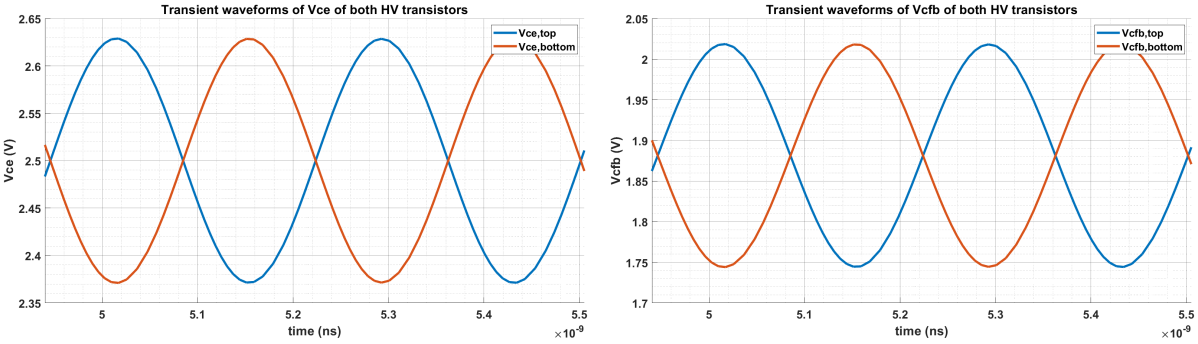


Figure 2.20: C_{fb} and C_μ in parallel.



(a) Transient waveform of Vce of both transistors centred around 2.5 V. **(b)** Transient waveform of Vcfb of both transistors, centred around 1.9 V.

Figure 2.21: Comparison of the voltage over each feedback transistor and the collector-emitter voltage over each transistor.

To obtain a relatively high source impedance, a series input capacitor C_{si} is added between the input signal and the base of each transistor. The ratio $\frac{C_{si}}{C_{fb}}$ also determines the voltage gain of the push-pull stage. To tune out the capacitive reactance of C_{si} at the design frequency, an inductor is placed before the capacitor. C_{fb} is in parallel to the parasitic C_{μ} capacitor as shown in Fig. 2.20, thus their values are added. In all circuit designs, a very small C_{fb} gives the best linearity and efficiency. As the feedback capacitor is much smaller than C_{μ}, C_{fb} can be removed from the circuit. This implies that C_{μ} now functions as the feedback capacitor and C_{si} is tuned to the value of C_{μ} instead. Removing the extra C_{fb} from the circuit results in less output capacitance, thus reducing the value of the output inductor used to tune out the output capacitance. This increases the bandwidth. A parallel input inductor L_{pi} is added to tune out the series capacitor C_{si}, see Fig. 2.22.

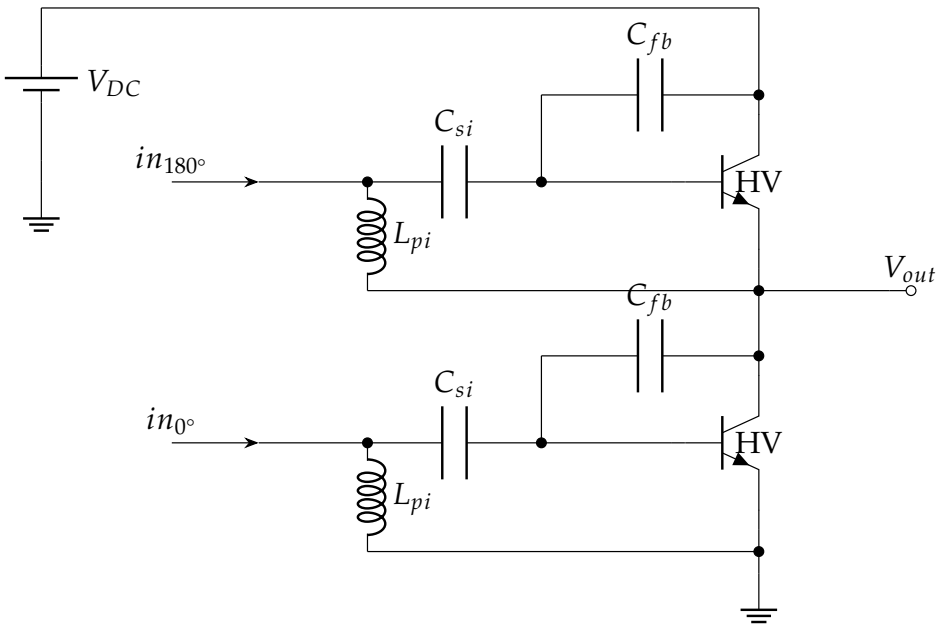


Figure 2.22: push-pull stage showing the feedback capacitors C_{fb}, the series input capacitors C_{si} and the parallel input inductor L_{pi}.

Fig. 2.23 shows the difference that C_{si} makes to the AM-AM and AM-PM distortion. The graph shows that adding the feedback circuit (C_{si} and L_{pi} only, as C_{fb} has been removed for higher efficiency and less output capacitance) indeed reduces both AM-AM and AM-PM distortion.

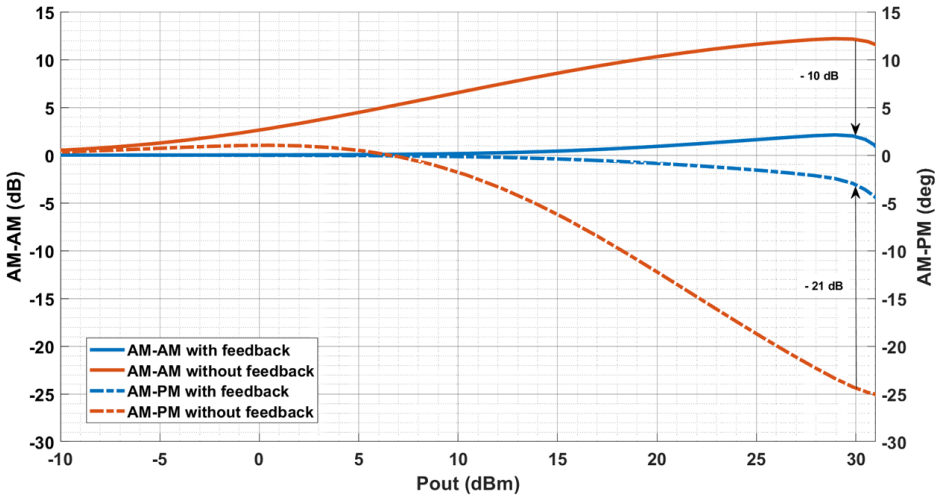


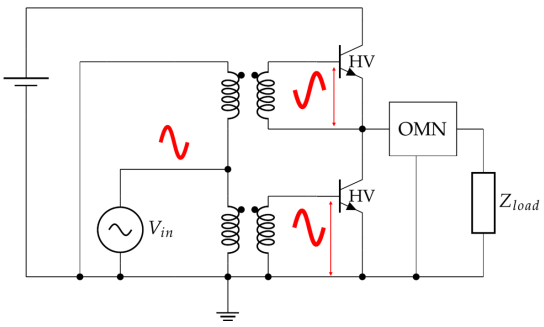
Figure 2.23: Comparison of the AM-AM (solid) and AM-PM (dotted) of the 2x HV push-pull with V_{DC} = 5 V. The new graphs (blue) show the distortion with the feedback circuit and the old (orange) graphs shows the distortion without the feedback circuit.

To further reduce the distortion, particularly the AM-PM distortion, the biasing current of the transistor can be increased. This however also negatively affects the efficiency and power gain of the amplifier. The optimal values are determined after the design of the input balun in the next section.

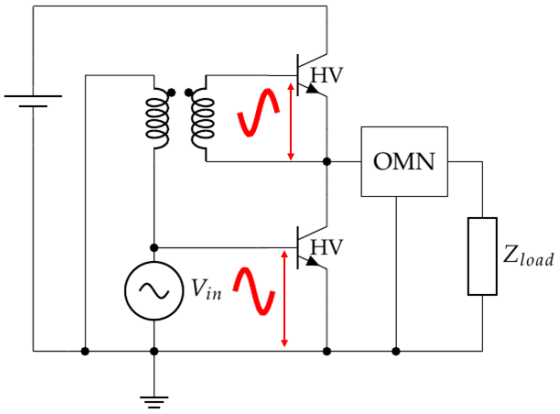
2.6. Input Balun

The NPN-only structure of the push-pull amplifier requires that the input signal to one of the inputs is inverted. To achieve this inversion, a transformer at the input is used. There are two possibilities:

- Use one transformer to invert the signal of the top transistor and connect the bottom transistor directly to the input signal as shown in Fig. 2.24a.
- Use two transformers. The top transformer inverts the signal to the input of the top transistor. The bottom transformer acts as a buffer and relays the input signal to the bottom transistor without inverting it, see Fig. 2.24b.



(a) 2x HV push-pull PA with one input signal transformer. The transformer shifts the input signal with 180° and feeds this to only the top HV transistor. The bottom HV transistor receives the input signal directly from the source.



(b) 2x HV push-pull PA with 2 input signal transformers. The top transformer transforms the input signal by shifting it 180° and feeds it to the top HV transistor. The bottom transformer copies the input signal, such that the bottom transistor receives the same input signal as the source. The two transformers are identical.

Figure 2.24: Two possible ways to transform the input signal.

2.6.1. Transformer Non-Idealities

Due to the limited coupling factor, transformers have various losses which need to be considered when designing them. The transformer is simulated by two inductors with a coupling factor k between them. The limited coupling factor results in a leakage inductor L_{leak} which can be simulated as an inductor in series with the transformer. The value of the leakage inductor is dependent on the transformer value L_{fmr}, as Equation (2.15) shows. Appendix A shows the derivation of the equivalent circuit and leakage inductance of the transformer with the coupling factor.

$$L_{leak} = L_1 \cdot (1 - k^2) \tag{2.15}$$

The transformer is simulated as shown in Fig. 2.25.

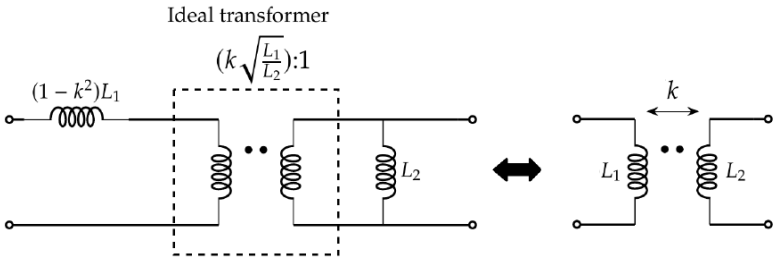


Figure 2.25: Transformer with leakage inductance.

The leakage inductance can be tuned out at the design frequency by adding a series capacitor C_{leak}, which can be calculated as in Equation (2.16).

$$C_{leak} = \frac{1}{\omega_d^2 \cdot L_{leak}} \tag{2.16}$$

The secondary winding L_2 can be used to tune out the series capacitor C_{si} at the base of the input transistor, thus taking over the function of the previously introduced L_{pi}. The value of L_1 can then be determined with Equation (2.17), assuming a coupling factor of 0.6 and keeping the voltage transfer equal to one.

$$k\sqrt{\frac{L_1}{L_2}} = 1 \tag{2.17}$$

A plot of the voltage transfer of the transformer against frequency shows to what extent the leakage inductance can be tuned out using a capacitor (C_{leak}) in series with L_{leak}. Fig. 2.26 shows the voltage transfer measured from the input of the transformer to the output. The voltage transfer at the 3.6 GHz design frequency is -1.02 V/V, which is very close to the ideal value of -1 V/V. Also, the phase is plotted to show that the transformer indeed inverts the input signal, as the transformer has a 182° phase shift.

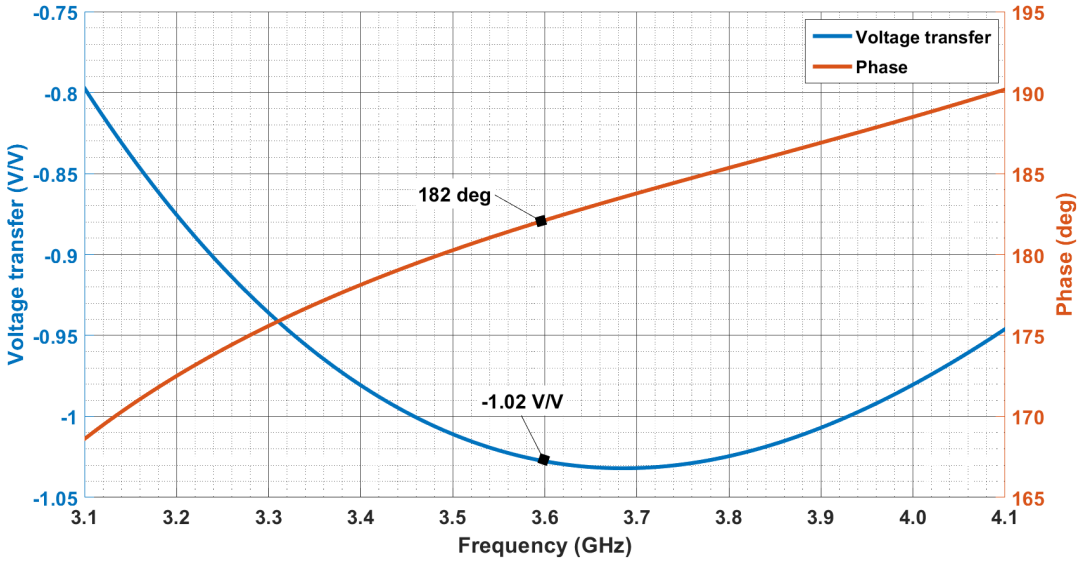


Figure 2.26: Voltage transfer (blue) and phase (orange) of the inverting transformer after tuning out the leakage inductor at the design frequency.

The transformer phase and voltage transfer vary over frequency as Fig. 2.26 shows. Simulations were run for a frequency range of 3.1 GHz to 4.1 GHz. The circuit was simulated with one transformer and two transformers, to see the effects of having only one transformer and thus an offset in one of the transistor input signals. Because Fig. 2.26 shows that the offset is largest for a frequency of 3.1 GHz, Tab.2.5 shows the results of the simulation for 3.6 GHz and 3.1 GHz.

Table 2.5: Comparison of the 2x HV push-pull 5 V circuit with source resistance $R_S = 50\ \Omega$ and one or two input transformers.

No. of transformers	Frequency (GHz)	P_{out} (dBm)	$\eta_{c,peak}$ (%)	PAE (%)	G_p
1	3.6	28.8	53.8	39.6	15.5
	3.1	27.4	42.5	29.6	11.6
2	3.6	29.3	50.0	44.4	15.7
	3.1	26.6	37.4	26.6	11.7

Tab.2.5 shows that one transformer performs only slightly better in terms of efficiency for a frequency of 3.1 GHz. However, at the design frequency, using 2 transformers yields a better PAE. Fig. 2.27 shows the peak PAE vs. output power. As the difference in efficiency is small between 1 and 2 transformers at 3.1 GHz, 2 input transformers are used. This way, the circuit remains fully symmetric.

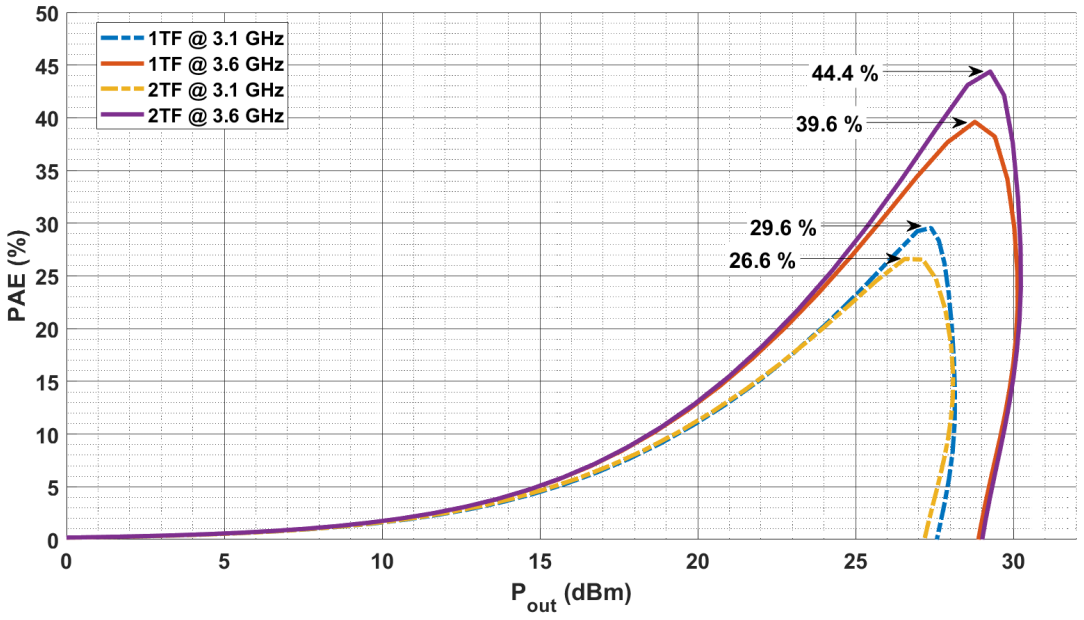


Figure 2.27: PAE vs. output power for 1 and 2 input transformers at 3.6 GHz (solid line) and 3.1 GHz (dotted line).

The ideal value of C_{si}, and thus the values of the coupled inductors is determined by sweeping C_{si} and tuning the other variables, aiming for high efficiency, 15 dB power gain and an AM-AM distortion of 1 dB or less. Tab.2.6 shows the determined value of C_{si} and the AM-AM and AM-PM distortion with and without the feedback circuit. As the circuits have a low input impedance due to the input balun, the source resistance is set to 3 Ω. The 1x LVHV 5 V PA has a source resistance set to 30 Ω, as the cascode amplifier has a higher input impedance. Other variables such as transistor biasing and multiplier are tuned as well, but not included in the table for simplicity. At the end of this work, an overview of all schematics with values is given.

Table 2.6: Series input capacitor and inductor values and simulation results.

Circuit	C_{si} (pF)	AM-AM (dB)	|AM-PM| (°)	η_{peak} (%)	G_p (dB)
1x LVHV 5 V	-	1.10	1.83	55.2	28.2
	1.0	0.90	0.96	56.9	18.9
2x HV 5 V	-	2.13	1.03	59.9	17.7
	14.4	0.82	5.59	63.2	15.3
2x HV 10 V	-	13.0	7.23	52.4	16.7
	28.0	0.53	6.90	56.0	24.5
2x LVLV 5 V	-	1.62	4.22	60.4	15.4
	3.6	0.89	0.92	62.0	18.7
2x LVHV 10 V	-	1.32	1.64	55.5	18.8
	6.6	0.93	4.56	62.12	25.6

2.7. Input Matching Network

Lastly, the input matching network is designed to ensure that the transducer gain matches the power gain. The input impedance is matched to a 50 Ω source resistance. The input impedance is simulated in Cadence. For the 2x HV push-pull with V_{DC} = 5 V, the simulated input impedance Z_{in} of the circuit is (2.9+7.1j) Ω, see Fig. 2.28.

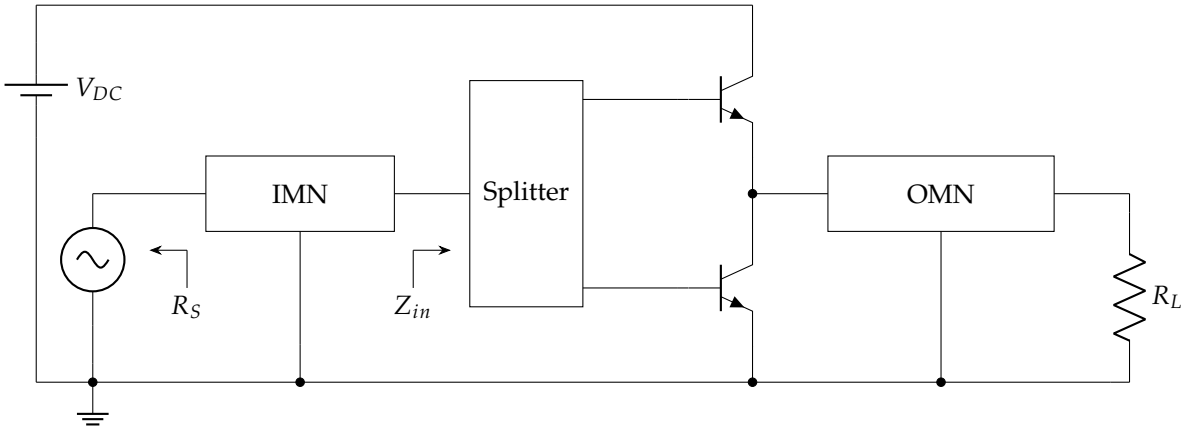


Figure 2.28: Basic overview of the push-pull circuit with the input matching network.

This is matched to a 50 Ω source impedance, see Fig. 2.29. This circuit has a Q-factor of 4.

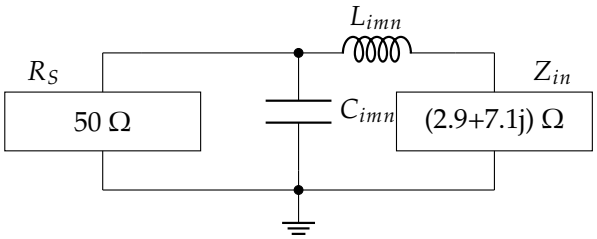


Figure 2.29: Schematic of the input matching network with source resistance and input impedance of the push-pull stage.

Ideally, the IMN has a Q-factor of less than 3.6. This would mean that the matching network needs to be matched to an intermediate impedance such as 13 Ω to meet the specification of Q < 3.6, see Fig. 2.30.

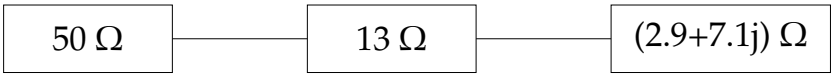


Figure 2.30: IMN in two stages: first matched to 13 Ω, then matched to (2.9+7.1j) Ω. This has a Q-factor of 1.7.

Simulations of the complete push-pull design with both matching networks show that the difference in the -10 dB S11 points between the two matching networks is minimal. For the 2x HV push-pull 5 V, the single-stage IMN has 20 MHz more bandwidth than the two-stage IMN. The efficiency however is much larger for the single-stage compared to the two-stage IMN, namely 72.8 % vs. 67.5 %. Hence, the single-stage IMN is chosen.

For the circuits with a 10 V supply, the Q-factor of the matching network is much higher than 3.6 and therefore these circuits do have a two-stage input matching network to reduce the overall Q-factor. The final IMN and values can be seen in Appendix B.

2.8. Stability

The stability of the circuits is determined by simulating the stability factor *Kf*. In order for the circuit to be stable for any source and load impedance, $Kf > 1.0$ for all frequencies. The orange (dotted) graph in Fig. 2.32 shows the stability factor over a frequency range of 10 KHz to 100 GHz. The stability factor is higher than 10 at the frequencies where no graph is shown. At the design frequency, the stability factor is 1.07, indicating stability at that frequency. In the 190 MHz to 290 MHz frequency range, however, the stability factor plummets below 0. This is likely caused by the 10 nH inductor in the biasing network. To solve this issue, the inductors in the biasing network are given a resistance R_{stb}. To compensate for the voltage drop over the inductor, a resistor R_{stb} is added to the base of the biasing transistor. This results

in the blue graph in Fig. 2.32. As the graph shows, the stability factor around the design frequency remains the same as before, but the issue at 50-80 MHz is solved. There, the stability factor is now well above 1.

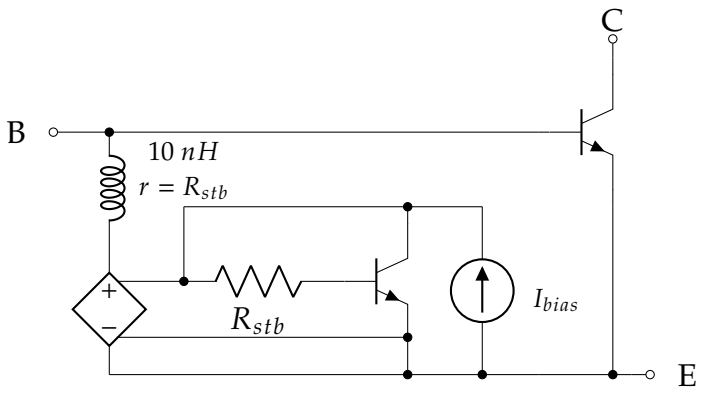


Figure 2.31: Biasing circuit with resistance R_{stb}

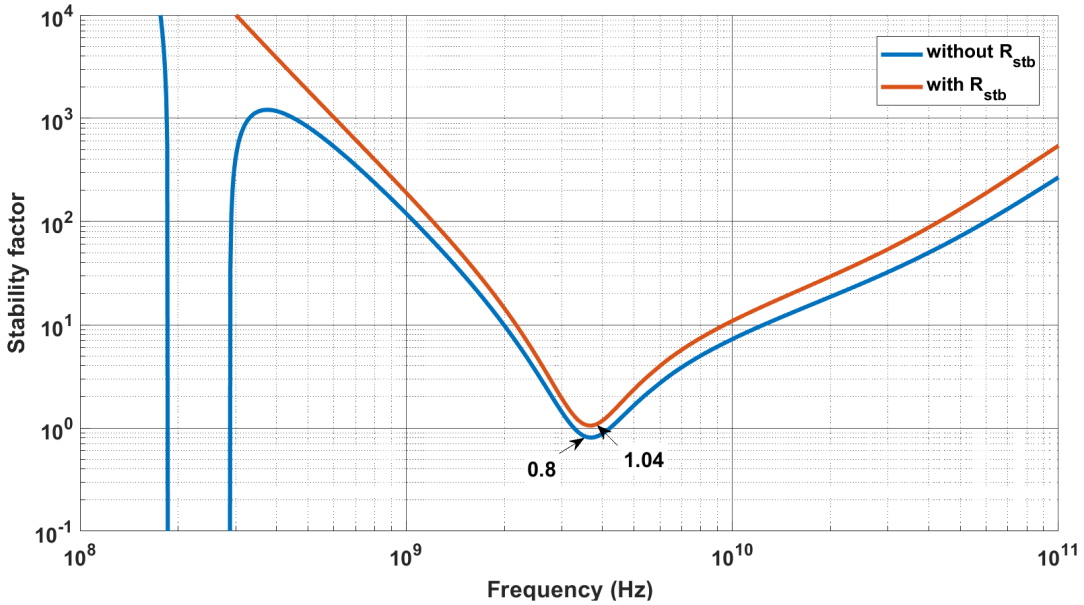


Figure 2.32: Stability factor (Kf) with (blue) and without (orange) resistance in the biasing network

Additionally, the collector efficiency $\eta_{c,P1dB}$ greatly increases as well. The AM-AM is plotted for both cases in Fig. 2.33 and the 1 dB compression point is indicated. Fig. 2.34 shows the collector efficiency $\eta_{c,P1dB}$ vs. output power, and the efficiencies at the 1 dB compression points are shown.

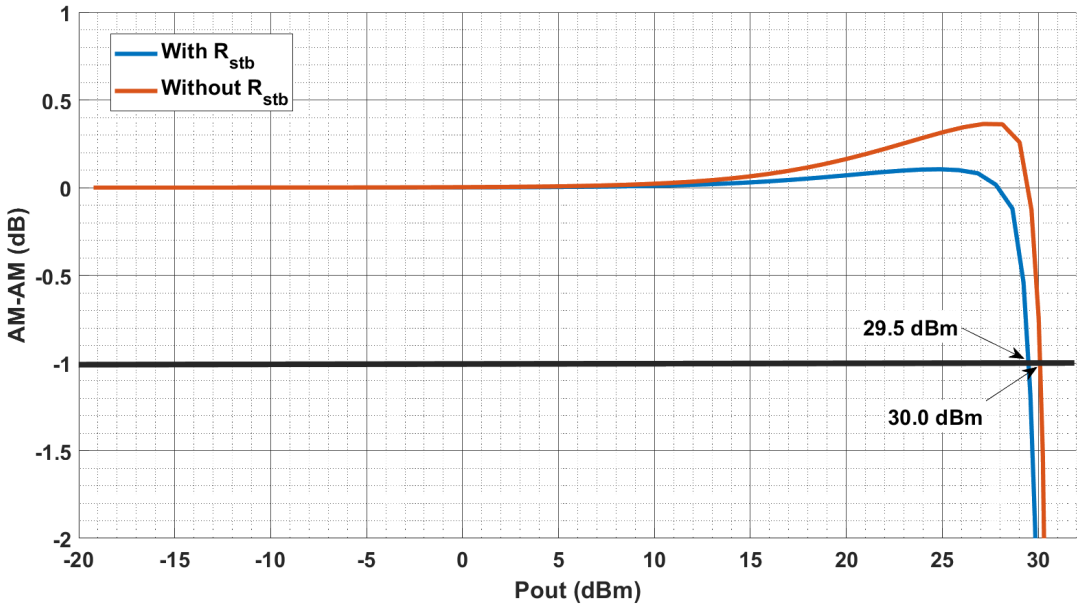


Figure 2.33: AM-AM difference with and without R_{stb}

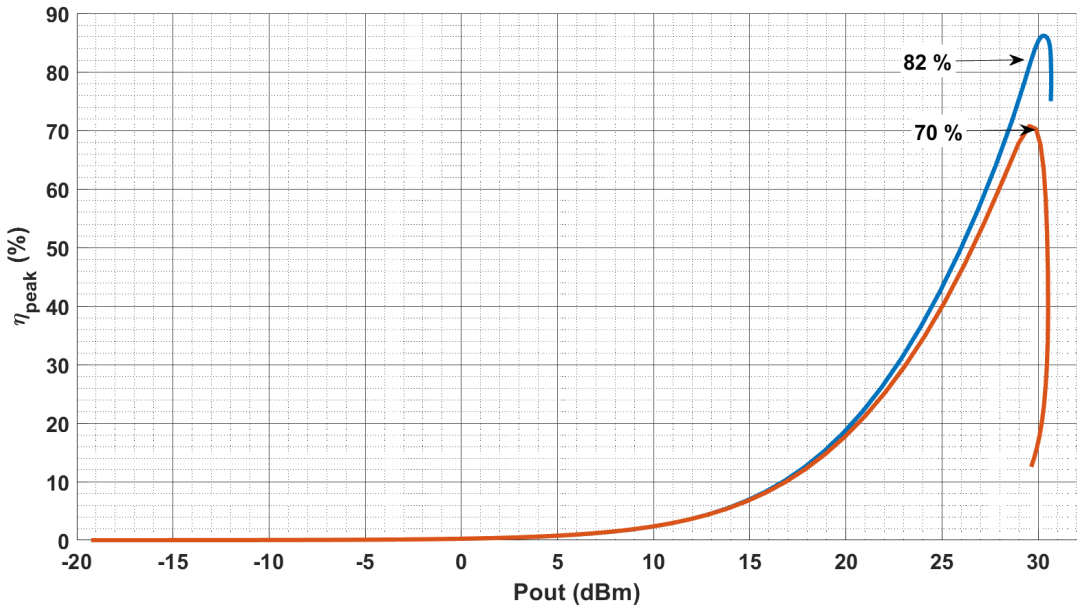


Figure 2.34: $\eta_{c,P1dB}$ difference with and without R_{stb}

This proves that by adding the resistance R_{stb}, the overall efficiency increases while the circuit is stable ($Kf > 1$) for all frequencies. The circuit's efficiency increases as the transistors are dynamically pushed towards class-C operation. As the input power increases, the DC voltage between base and emitter decreases, decreasing the angle of conduction of the transistor.

The linearity and efficiency of the circuit are evaluated for an imbalance in the circuit. To introduce this imbalance, the size of the top HV transistor is varied between 0.5 and 1.5 times the nominal value, while M of the bottom transistor is kept at nominal value. Fig. 2.35 shows the AM-AM distortion for a M_{top}/M_{bottom} ratio of 0.5-1.5. For the circuit to have minimal AM-AM distortion, the ratio should be >0.8. The efficiency plot in Fig. 2.36 supports this. The output voltage swings around 2.5 V (DC output voltage) for the 2x HV 5 V push-pull. However, as the M_{top}/M_{bottom} ratio varies between 0.5 and, the DC output voltage varies between 1.3-3.3 V. For a small imbalance (20%) between the transistor

sizes, the efficiencies and AM-AM distortion barely change compared to no imbalance. Thus, the circuit is not sensitive to small imbalances in transistor size up to 20%.

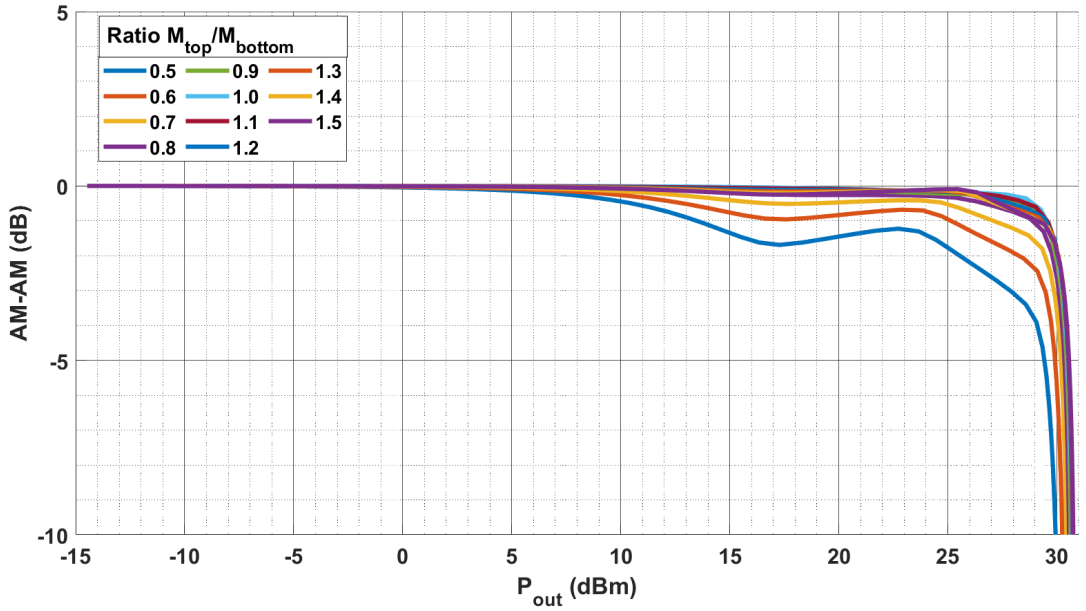


Figure 2.35: AM-AM for deviations in transistor size between top and bottom transistor for the 2x HV 5 V push-pull.

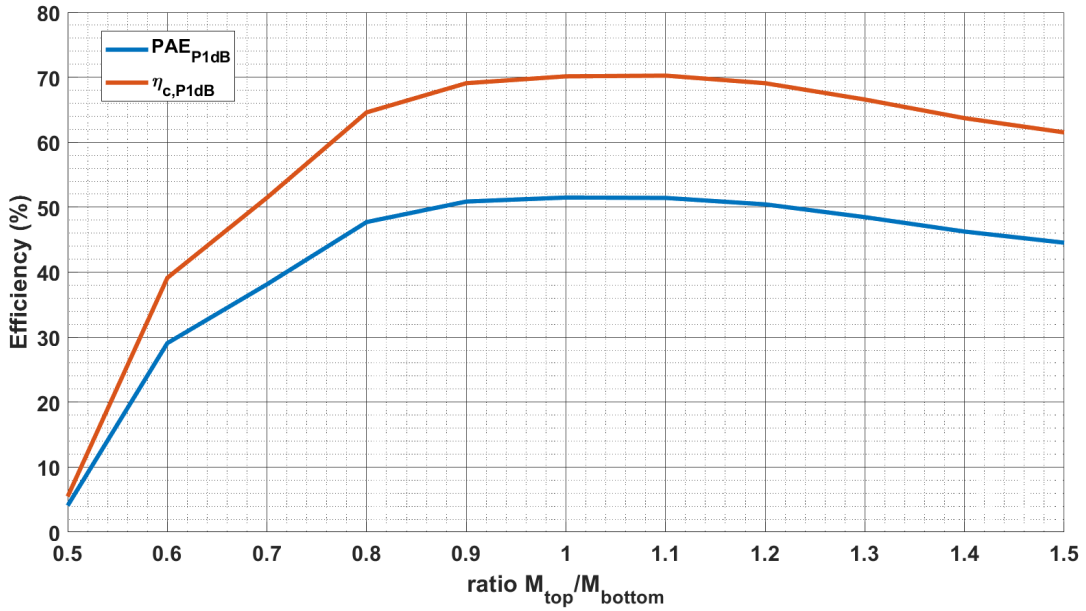


Figure 2.36: Collector efficiency and PAE (at 1dB compression point) for various top-transistor sizes for the 2x HV 5 V push-pull.

Tab.2.7 shows the values of R_{stb} for all circuits and the resulting efficiencies and stability factor.

Table 2.7: R_{stb} values and the resulting efficiencies.

Circuit	R_{stb} (Ω)	P_{1dB} (dBm)	η_{P1dB} (%)	PAE_{P1dB} (%)	Kf
1x LVHV 5 V	110	29.8	62.0	52.9	3.0
2x HV 5 V	105	29.5	70.4	58.5	1.0
2x HV 10 V	29.4	0	48.1	36.19	0.3
2x LVLV 5 V	50	29.8	64.5	64.3	2.0
2x LVHV 10 V	50	30.6	65.1	64.1	2.1

Tab. 2.7 shows that not all designs have a Kf of more than 1. The 2x HV 10 V push-pull design has a stability factor lower than 1 and the 2x HV 5 V push-pull has a stability factor of exactly 1. This indicates that these circuits are not stable for any load, however, as the load impedance is known and set, that does not necessarily mean that this circuit is unstable for its application. To be sure, a transient simulation is performed and the output voltage waveform is plotted in Fig. 2.37 and Fig. 2.38 for the 2x HV 5 push-pull and 2x HV 10 V push-pull respectively. The output voltage is supposed to be a constant square wave, as Fig. 2.37 shows. Fig. 2.38 however, shows that the 2x HV 10 V is unstable in transient simulation.

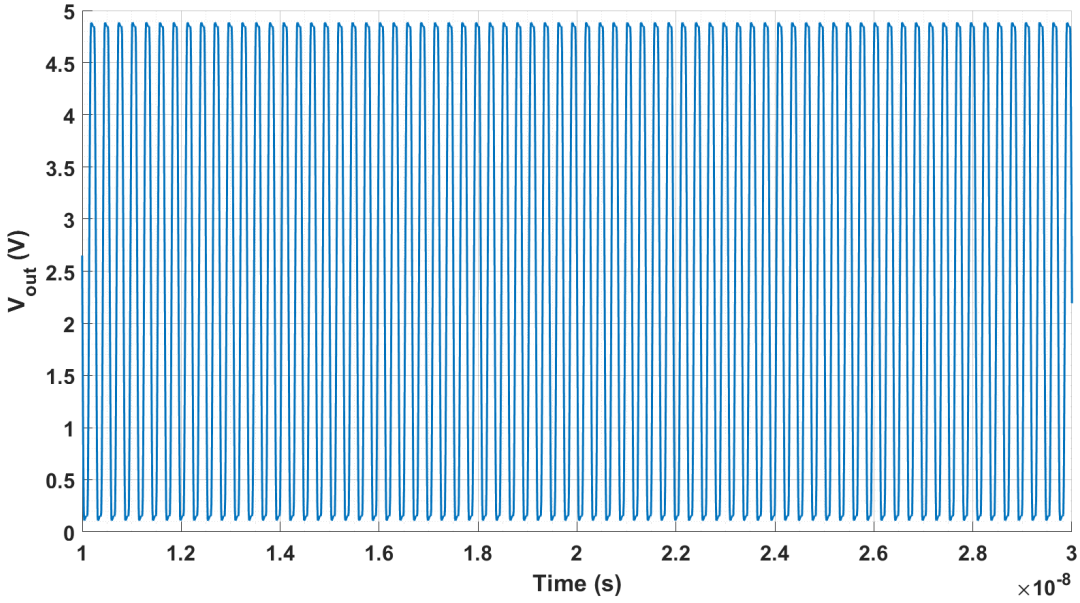


Figure 2.37: Transient simulation of the output voltage of the 2x HV 10 V push-pull design.

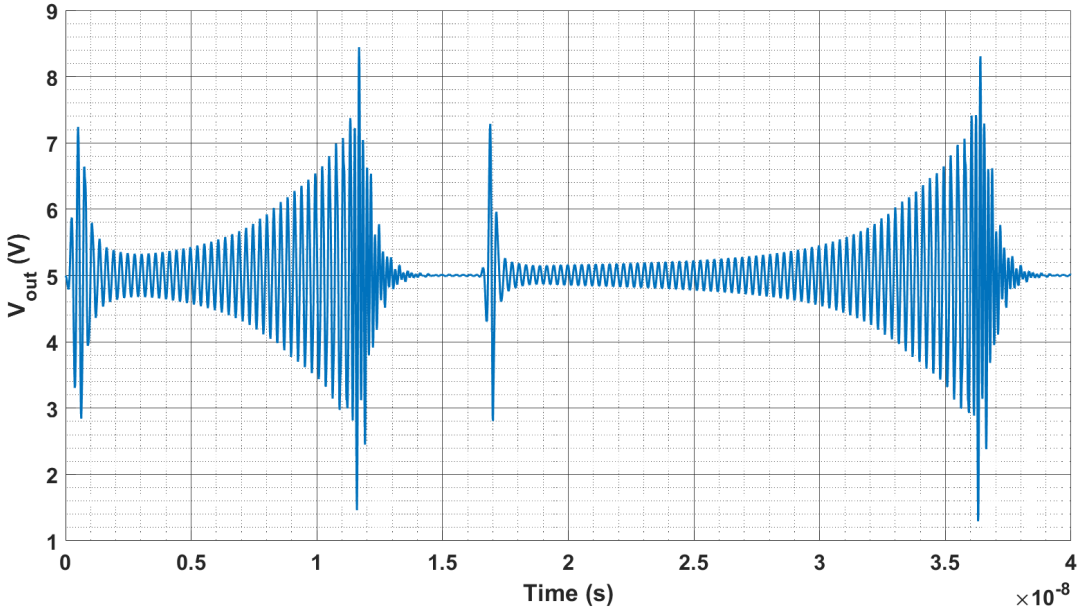


Figure 2.38: Transient simulation of the output voltage of the 2x HV 10 V push-pull design.

A possible cause for this instability could be the high supply voltage, causing the collector-emitter voltage of the transistor to be beyond its collector-to-emitter breakdown voltage (avalanche breakdown). As the circuit is unstable, no further simulations are performed on this design.

3

Simulation results

All push-pull circuit designs and the single-ended PA are simulated and their final results are compared. The complete circuits (from Cadence) and all component values can be seen in Appendix B.
The simulations are split into two sections:

- A single tone simulation at the design frequency of 3.6 GHz, as well as simulations at a centre frequency of 3.1, 3.4, 3.8, and 4.1 GHz to analyse the circuit's behaviour at a 1 GHz bandwidth.
- A two-tone simulation with a centre frequency of 3.6 GHz, and tone spacings of 1 MHz to 1 GHz.

3.1. Single-Tone Simulation at 3.6 GHz Operating Frequency

The four push-pull circuits and the single-ended PA are simulated and the results are compared. Tab. 3.1 gives an overview of the most important results.

Table 3.1: Comparison table between the multiple push-pull designs and the cascoded PA for a design frequency of 3.6 GHz. Inductors have Q=15, the transformers k= 0.6 and Q=10. $\eta_{coll,P1dB}$ does not include the OMN, PAE does include the OMN.

	Spec	1x LVHV 5V	2x HV 5V	2x LVLV 5V	2x LVHV 10V
$P_{out,1dB}$ (dBm)	30	30	29.5	30.6	30.2
$\eta_{coll,peak}$ (%)	80 (aim)	60.8	70.7	65.9	64.7
$\eta_{coll,P1dB}$ (%)	80	60.6	70.1	65.7	63.9
PAE_{peak} (%)	-	38.1	51.8	49.7	48.9
PAE_{P1dB} (%)	-	38.1	51.5	49.5	47.9
Post-PA loss (dB)	-	1.9	1.2	1.2	1.5
AM-AM_{max} (dB)	<1.0	0	0	282m	452m
AM-PM_{max} (dB)	<1.0	5.9	9.8	-633m	-3.8
AM-PM_{1dB} (°)	< 7°	5.5	5.5	-941m	-3.8
Gp (dB)	15	16.5	15.8	18.2	23.1
Gt (dB)	15	6.5	15.7	18.2	23.1
Gv (V/V)	>1	2.5	1.5	1.9	7.0

Tab. 3.1 shows that the peak efficiency is highest for the 2x HV 5 V push-pull PA (71%) for an output power of 29.5 dBm. To increase the output power, the output matching network can be adjusted slightly so the push-pull PA sees a lower load impedance. As expected, the single-ended PA has the largest Post-PA loss of 1.9 dB, due to the extra losses of the choke inductor and the H2-trap in the output matching network. This also affects the efficiency, which is the lowest for this amplifier.
The amplifiers show little to no AM-AM_{max} distortion, which is the maximum positive distortion for output powers between 0 dBm and $P_{out,1dB}$, indicating that the amplifiers are linear. Also, the AM-PM distortion at P_{1dB} falls within specification. However, the AM-PM suddenly increases significantly as the amplifier delivers higher output powers (27 dBm and above). As the AM-PM is often associated with second harmonics [1], the effect of a second harmonic trap between base and emitter of the transistors is

checked. Fig. 3.1 also shows that for the push-pull PAs, the S_{21}-parameter is not sufficiently (<-20 dB) suppressed. The single-ended PA has a second harmonic trap at the output, thus its second harmonic is sufficiently suppressed.

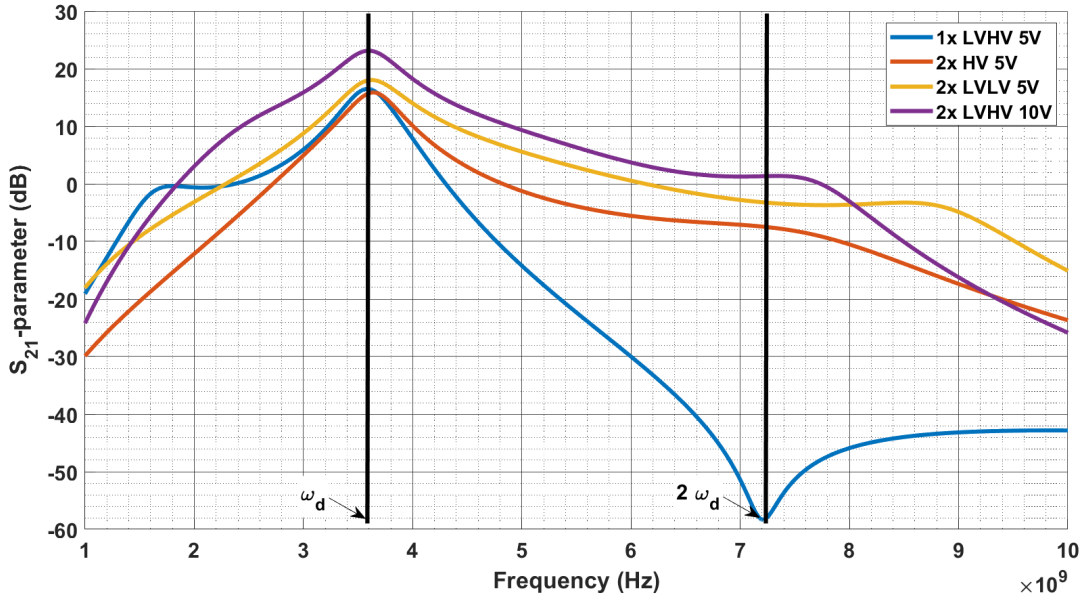


Figure 3.1: S21 parameters of the designs

Fig. 3.2 shows one of the push-pull transistors with its biasing circuit. Indicated by the black box in the H2 trap, with C = 1 pF and L = 489 nH, which are arbitrarily chosen values. The effect of this H2 trap on the AM-PM is shown in Fig. 3.3.The dotted line in Fig. 3.3 shows that the AM-PM indeed decreases as the H2 trap is added.

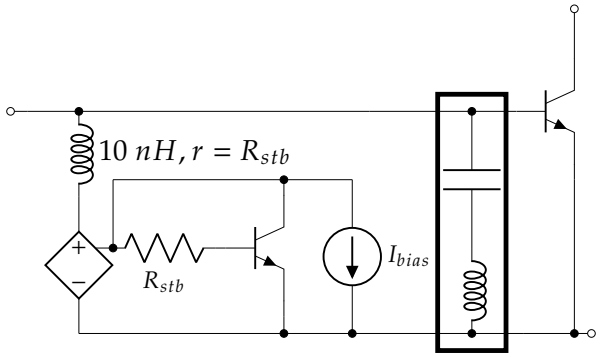


Figure 3.2: H2 trap between base and emitter of the transistor.

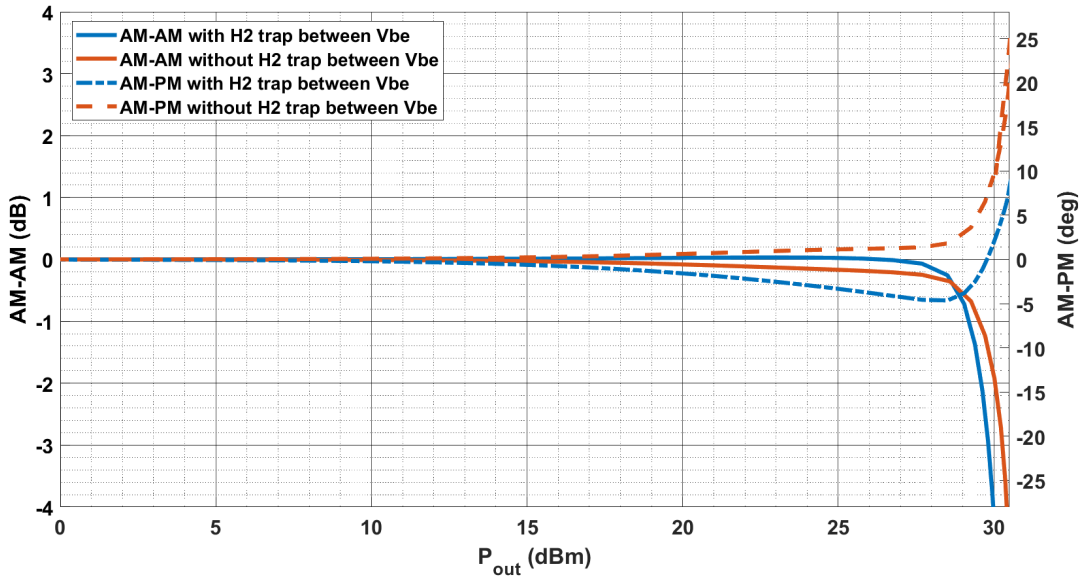


Figure 3.3: AM-AM (solid line, left y-axis) and AM-PM (dotted line, right y-axis) with and without the second harmonic trap between V_{be}.

Because the second harmonic is now eliminated, the peak efficiency of the circuit also increases, as seen in Fig. 3.4.

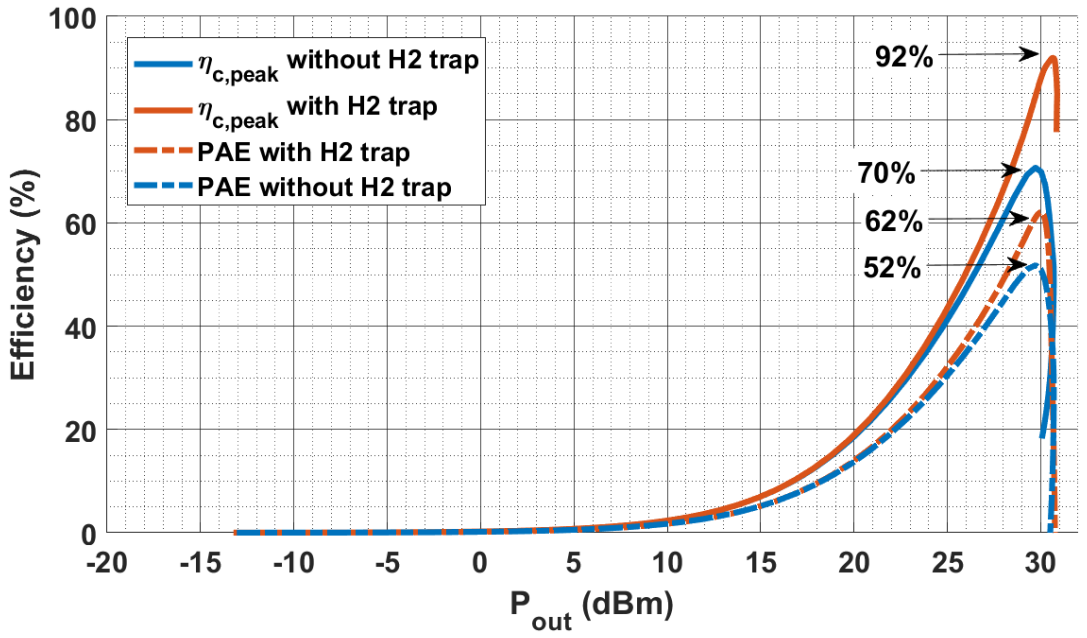


Figure 3.4: AM-AM (solid line, left y-axis) and AM-PM (dotted line, right y-axis) with and without the second harmonic present between V_{be}.

3.2. Single-Tone Simulation at Frequencies of 3.1 GHz to 4.1 GHz

The amplifiers' behaviour over a 400 MHz (6.4-3.8 GHz)and 1 GHz (3.1-4.1 GHz) frequency band is shown in Tab. 3.2. The *worst* values in the frequency band are noted for each amplifier design. Because the designs do not reach an output power of 30 dBm for all frequencies, the AM-AM and AM-PM values are left out. Fig. 3.5 shows the collector efficiency of the PAs against frequency.

Table 3.2: Comparison table between the multiple push-pull designs and the cascoded PA for a design frequencies 3.1, 3.4, 3.6, 3.8 and 4.1 GHz. Inductors have Q=15, the transformers k= 0.6 and Q=10.

	BW (GHz)	1x LVHV 5V	2x HV 5V	2x LVLV 5V	2x LVHV 10V
$Pout_{1dB}$ (dBm)	0.4	29.2	28.7	29.7	29.5
	1.0	29.2	26.6	27.3	26.8
$\eta_{c,peak}$ (%)	0.4	51.0	62.6	56.1	54.9
	1.0	23.3	35.0	35.5	39.9
PAE_{1dB} (%)	0.4	30.5	45.5	42.0	40.8
	1.0	12.5	24.5	26.0	28.2
$AM\text{-}AM_{max}$(dB)	0.4	352m	1.07m	548m	534m
	1.0	1.6	418m	792m	534m
$AM\text{-}PM_{1dB}$(°)	0.4	10.9	8.0	7.2	-7.3
	1.0	10.9	15.0	16.3	-11.2
Gp (dB)	0.4	14.9	14.3	17.2	22.5
	1.0	10.5	11.5	14.7	21.2
Gt (dB)	0.4	13.2	12.6	15.6	21.3
	1.0	5.2	6.8	10.3	16.9

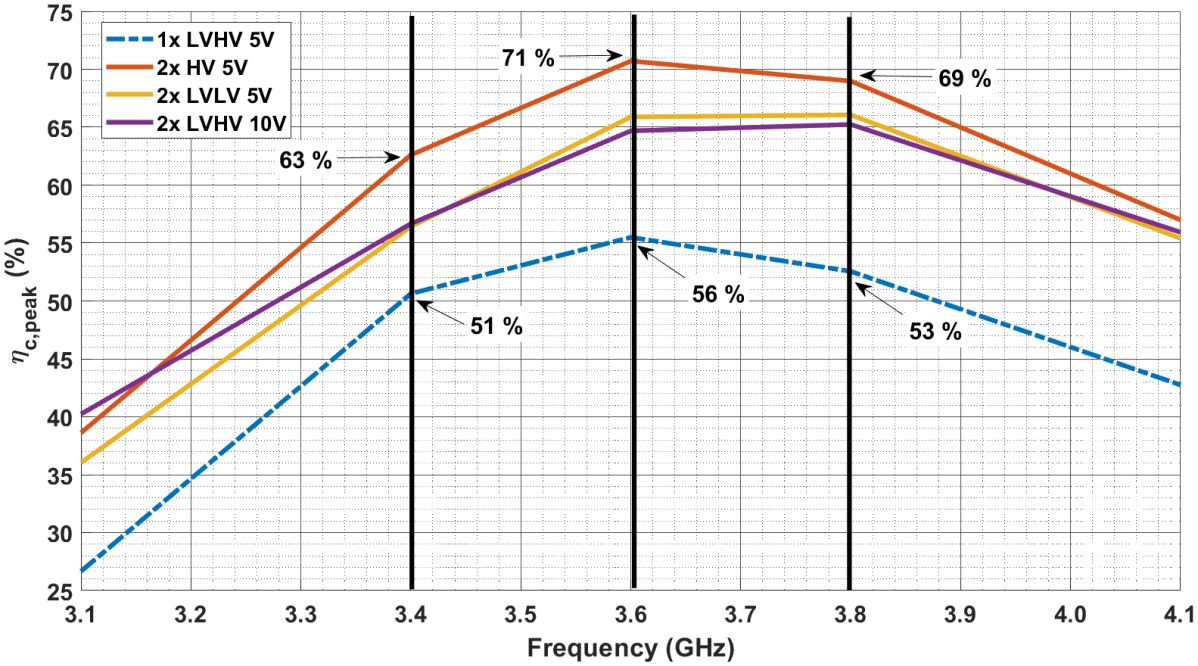


Figure 3.5: $\eta_{c,peak}$ of the designs vs. frequency. The reference single-ended PA is the dashed line.

Fig.3.5 clearly shows that all push-pull designs perform better in terms of efficiency than the single-ended PA in the 3.1-4.1 GHz frequency range. The 2x HV 5 V performs the best overall with a significantly higher efficiency than the other designs. The single-ended PA has the highest loss in the output matching network, which contributes to the low efficiency. Fig. 3.6 shows the output voltage waveform and the intrinsic current of the bottom (LV) transistor. Ideally, V_{out} is a square wave around 5 V and is 0 V when I_{int} flows. The ellipses in the graph show where the output voltage and intrinsic current overlap. Here, power is lost.

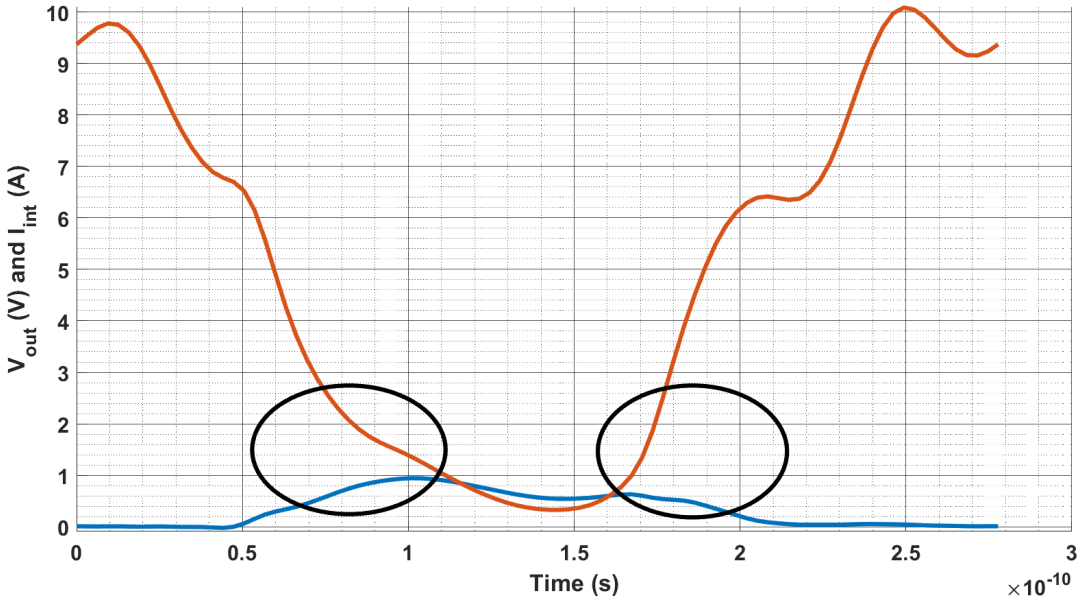


Figure 3.6: Output voltage waveform and collector current of the single-ended PA at maximum efficiency.

The push-pull PAs have a similar voltage and current waveform. The waveforms of the 2x HV 5 V push-pull PA are simulated in Fig. 3.7. The push-pull circuits all have an output voltage which better represents a square wave. Of course, these amplifiers also burn power during switching. However, as the voltage is almost 0 V when the current flows through the amplifier, the losses there are kept to a minimum, in contrast to the single-ended PA, where the voltage only reaches 0 V for a very short moment, although the intrinsic current flows through the transistor for a much longer period. This results in a higher efficiency of the push-pull designs.

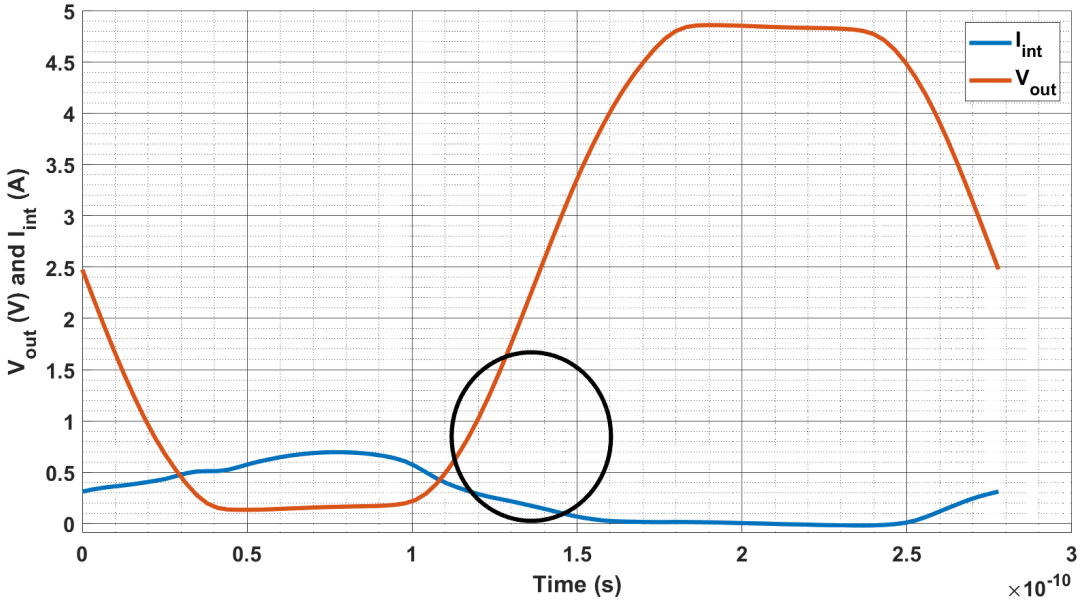


Figure 3.7: Output voltage waveform and collector current of the 2x HV 5V PA at maximum efficiency.

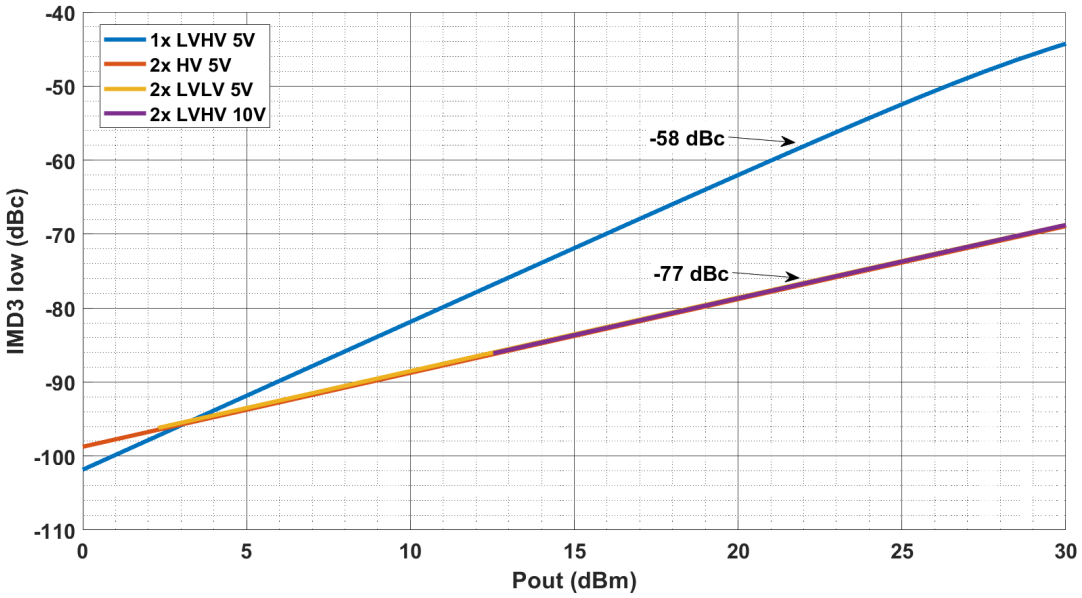
3.3. Two-Tone Simulation

A two-tone simulation was performed for a centre frequency of 3.6 GHz. The simulated tone-spacings are 1 MHz, 10 MHz and 100 MHz - 1 GHz in steps of 100 MHz. Tab. 3.3 shows the IM3 distortion in dBc at an average output power of 22 dBm for the various circuits.

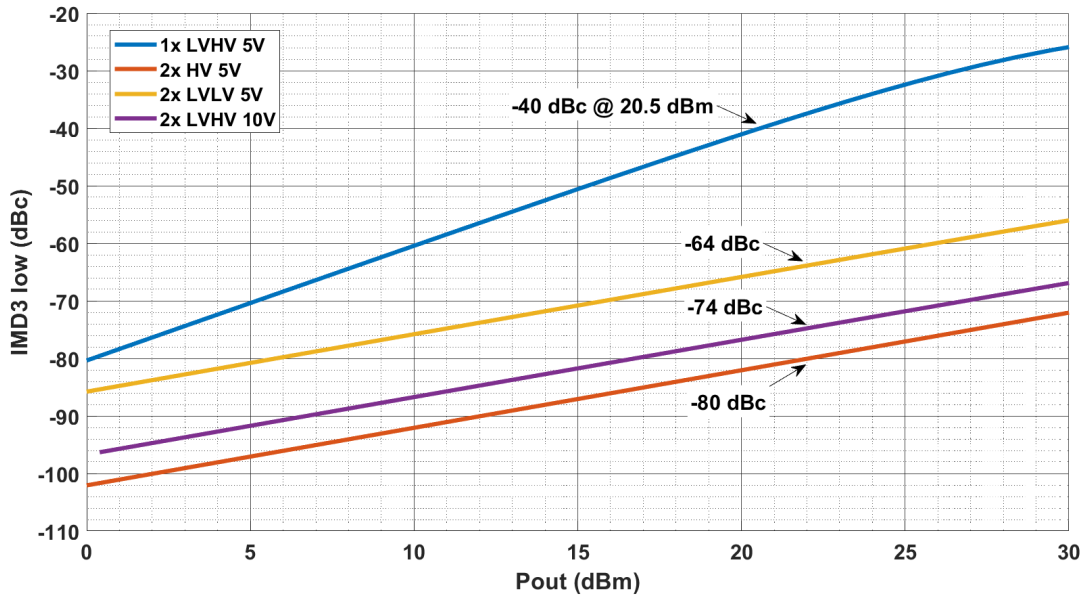
Table 3.3: IMD3 for the low-tone and 1 MHz tone-spacing. Specs: IMD3 = -40 dBc and OIP3 = 42 dBm.

	1x LVHV 5 V	**2x HV 5 V**	**2x LVLV 5 V**	**2x LVHV 10 V**
IMD3 (dBc) @ 22 dBm :				
1MHz tone spacing	-58.1	-76.8	-76.6	-76.7
100 MHz tone spacing	-47.0	-80.7	-68.6	-85.3
OIP3 (dBm)				
1MHz tone spacing	48.0	49.4	49.3	49.3
100MHz tone spacing	42.6	51.1	45.2	53.7

As the IM3 distortion varies with the output power, the IM3 has been plotted against the output power in Figures 3.8a and 3.8b for tone-spacings of 1 MHz and 1 GHz respectively. The IM3 increases with output power. Fig. 3.8a shows that all circuits have an IMD3 far below -40 dBc at 22 dBm output power, thus meeting the specification. For a 1 GHz tone spacing, the single-ended PA has an IMD3 of -38 dBc at P_{out} = 22 dBm.



(a) IM3 vs. Pout for a tone-spacing of 1 MHz



(b) IM3 vs. Pout for a tone-spacing of 1 GHz

Figure 3.8: IM3 (low) vs. Pout for a tone-spacing of 1 MHz (top) and 1 GHz (bottom)

Fig. 3.9 shows the IMD3 low (solid) and high (dashed) tones of all circuits. The IMD3 of the single-ended is much higher than that of the other circuits, yet meets the <-40 dBc specification. Fig. 3.10 shows the absolute difference between the low and the high tones of the IMD3. For the push-pull designs, the difference is at most about 6 dB between the tones. But as the IMD3 is already very low (<-65 dBc), this difference in low and high tones has little significance.

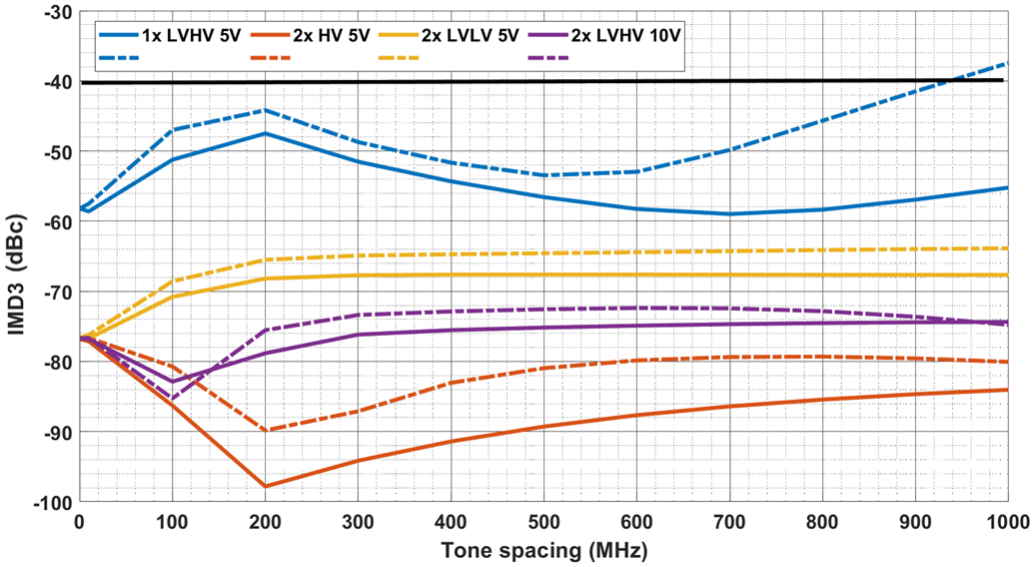


Figure 3.9: IMD3 low (solid) and high (dashed) for an output power of 22 dBm vs. tone spacing.

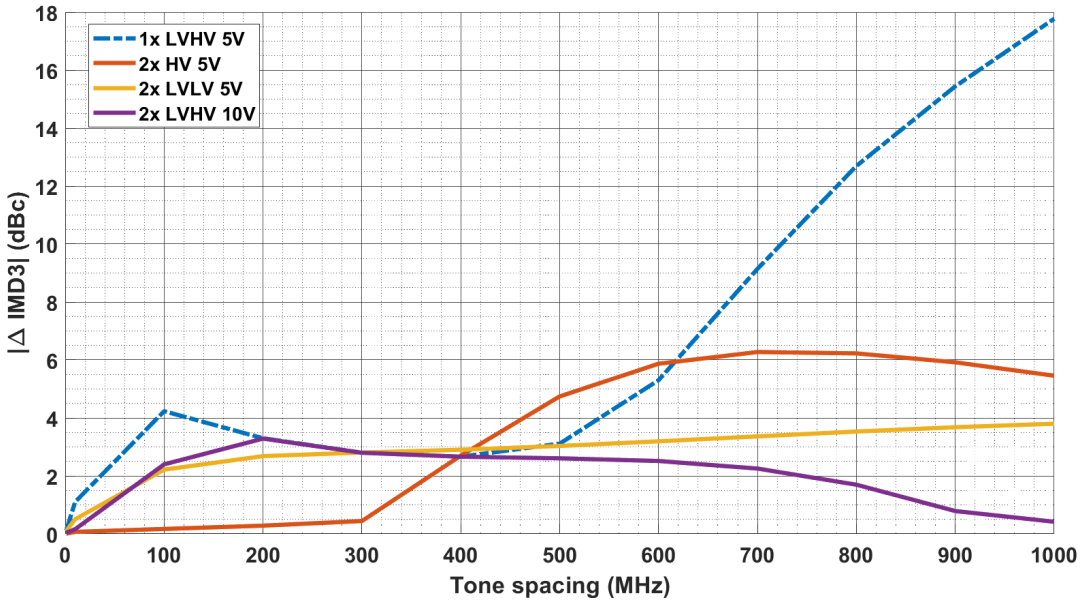


Figure 3.10: The absolute difference between the IMD3 of the low and high tones vs. the tone spacing of the two-tone simulation for $P_{out,avg}$ = 22 dBm

Fig. 3.11 and Fig. 3.12 show the OIP3 low (solid) and high (dashed) values over various tone spacings and the difference between these tones. Also here, the single-ended is the most sensitive to variations in frequency.

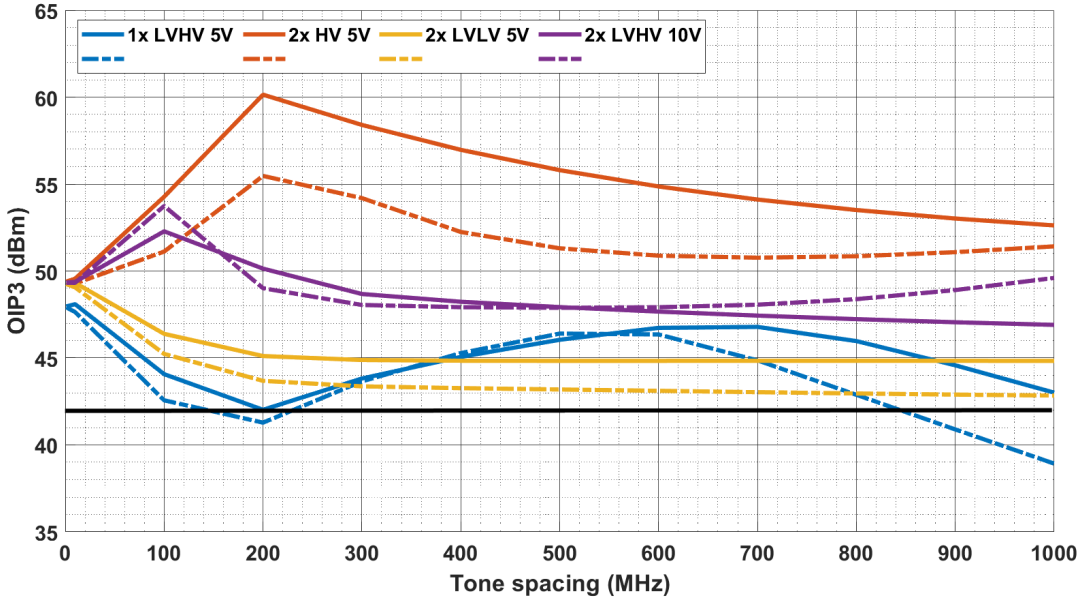


Figure 3.11: OIP3 low (solid) and high (dashed) vs. tone spacing for low (-30 dBm) input power.

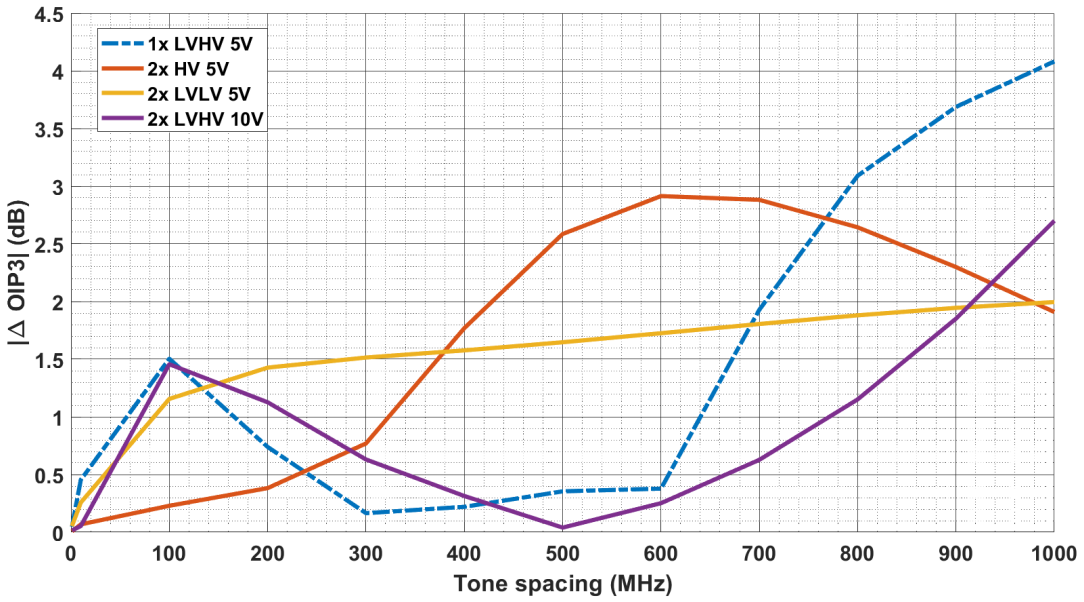


Figure 3.12: The absolute difference in the OIP3 of the low and high tone vs the tone spacing of the two-tone simulation

At and around the 3.6 GHz design frequency, the parasitics in the circuits are tuned out, hence they result in little IMD3 and good OIP3. As the operating frequency deviates from the design frequency, these parasitics are no longer tuned out properly, resulting in more IMD3 and a lower OIP3. The push-pull designs show better OIP3 and IMD3 values.

3.4. Conclusion on Simulation Results

In both the single-tone as well as the two-tone test, the push-pull amplifiers perform better than the single-ended amplifier in terms of linearity and efficiency. The 2x HV 5 V push-pull has the highest efficiency and best IMD3 and OIP3 values amongst the push-pull designs. As this amplifier only has 2 transistors, it has the lowest knee-voltage. The cascode push-pull designs both have a larger knee voltage due to stacking the transistors, causing these designs to be less efficient. The efficiency of the circuits can still be optimised by adding an H2 trap between the base and emitter of the transistor receiving the input signal, however, this H2 trap needs to be wideband (1 GHz).

4

Conclusion and Discussion

This work analyzed the possibility of replacing the single-ended cascoded PA design with a series push-pull totem-pole PA, to improve the bandwidth, efficiency and linearity of the amplifier. The single-ended PA is supplied by a 5 V supply, and thus has an approximate output voltage amplitude of 5 V. In the push-pull configurations that were designed in this work, both transistors receive the same input and each transistor provides equal voltage and gain to the output. They are therefore scaled in such a way that the output voltage of the push-pull configuration is $V_{DC}/2$. Because the 5 V supply is already available on the chip, two push-pull circuits are designed with V_{DC} = 5 V: 2x HV 5 V push-pull and a 2x LVLV push-pull. However, in order to achieve the same approximate 5 V output voltage amplitude as the single-ended cascode, the supply voltage of the push-pull amplifiers must be 10 V. Two designs are made with a 10 V voltage supply: 2x HV 10 V push-pull and a 2x LVHV push-pull amplifier.

Simulation results show that the goal of this thesis is achieved. The push-pull designs perform better than the single-ended PA in terms of efficiency and linearity. This is the case for the design frequency of 3.6 GHz, as well as frequencies ranging from 3.1 GHz to 3.6 GHz. The peak efficiency of the 2x HV 5 V push-pull design is 70.7%, which is around 10 percentage points higher than that of the single-ended PA (60.8%). Efficiencies can be further improved by adding a second harmonic trap between base and emitter of the transistors that receive the input signal.

All inductors have a parasitic resistance, calculated with a quality factor of 15, the coupled inductors forming the input transformers have a Q-factor of 10 and the designs were simulated at a 100°C temperature in order to add some non-idealities to the simulations. However, the biasing circuits are ideal and in reality will contribute to extra losses.

4.1. Discussion and Recommendations for Future Work

Since now a 5 V supply voltage is available on the chip, the circuits with a 5 V supply are also favourable at the moment: the 2x LVLV 5 V and the 2x HV 5 V. However, future work can look into the possibility of using these designs with higher supply voltages, as a 28 V supply is often used for power amplifiers. By stacking the PA designs, the supply voltage can be divided over the PAs in such a way that each PA (consisting of one 2x LVLV 5 V push-pull, or one 2x HV 5 V push-pull) has a 5 V voltage drop. Stacking two PAs would give the possibility of a 10 V supply voltage, stacking 3 PAs would allow a 15 V supply and so on. To be able to use the supply voltage of 28 V, only 3 push-pull amplifiers with a 10 V supply need to be stacked, while 6 5 V-supply amplifiers are needed. Thus future work could analyse the stacking of the 10 V push-pull designs. A challenge could be the 28 V reverse voltage across the collector-substrate junction of the top transistor.

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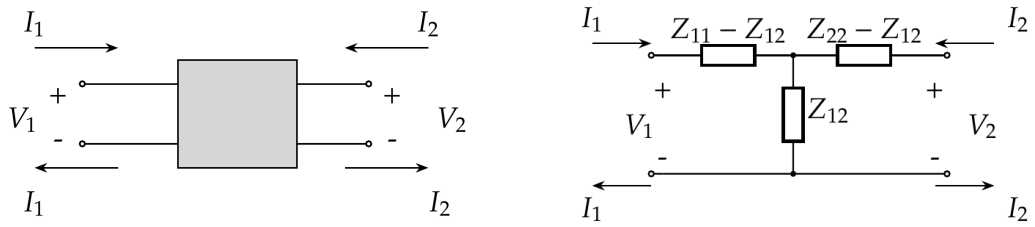
A

Derivation Transformer Equivalent Circuits

A transformer can be considered a two-port network , as shown in Fig. A.1a. Its equivalent circuit for z-parameters is shown in Fig. A.1b. Here, the subscript "1" represents the input, while the subscript "2" represents the output.



(a) Two-port network

(b) Two-port equivalent circuit

Figure A.1: Two-port network and its equivalent circuit

The voltages can be calculated as in equation A.1 [3, 4]

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{A.1}$$

where the z-parameters can be calculated as follows:

$$\begin{aligned} z_{11} &= \left.\frac{V_1}{I_1}\right|_{I_2=0} & z_{12} &= \left.\frac{V_1}{I_2}\right|_{I_1=0} \\ z_{21} &= \left.\frac{V_2}{I_1}\right|_{I_2=0} & z_{22} &= \left.\frac{V_2}{I_2}\right|_{I_1=0} \end{aligned} \tag{A.2}$$

In case the two-port is a transformer with mutual inductance M between inductor L_1 and inductor L_2, it follows that

$$\begin{aligned} z_{11} &= j\omega L_1 & z_{12} &= j\omega M \\ z_{21} &= j\omega M & z_{22} &= j\omega L_2 \end{aligned} \tag{A.3}$$

A transformer with coupling factor k can therefore be modeled as in Fig. A.2, where $k = \frac{M}{\sqrt{L_1 L_2}}$.

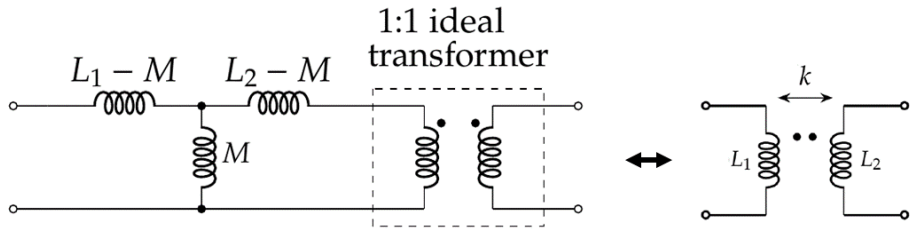


Figure A.2: Equivalent circuit of a transformer derived from the z-parameters.

.
The two-port can also be described using h-parameters, see Fig. A.3 and Equation (A.4).

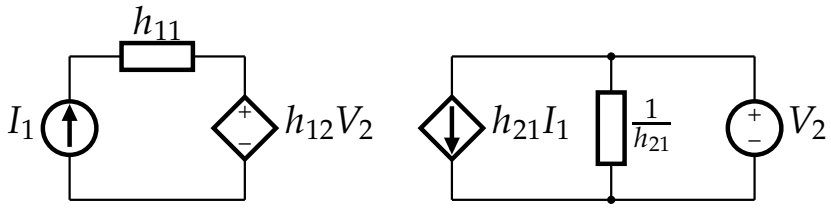


Figure A.3: Equivalent circuit h-parameters

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix} \tag{A.4}$$

where

$$\begin{aligned} h_{11} &= \left.\frac{V_1}{I_1}\right|_{V_2=0} & h_{12} &= \left.\frac{V_1}{V_2}\right|_{I_1=0} \\ h_{21} &= \left.\frac{I_2}{I_1}\right|_{V_2=0} & h_{22} &= \left.\frac{I_2}{V_2}\right|_{I_1=0} \end{aligned} \tag{A.5}$$

From the above equation and Fig. A.2, the h-parameters can be determined.

$$\begin{aligned} h_{11} &= j\omega[L_1 - M + (M//(L_2 - M))] = j\omega(1 - k^2)L_1 \\ h_{12} &= \frac{M}{L_2} = k\sqrt{\frac{L_1}{L_2}} \\ h_{21} &= -\frac{M}{L_2} = -k\sqrt{\frac{L_1}{L_2}} \\ h_{22} &= \frac{1}{j\omega L_2} \end{aligned} \tag{A.6}$$

where $M = k\sqrt{L_1 L_2}$. From here, the equivalent circuit of the transformer can be drawn, see Fig. A.4.

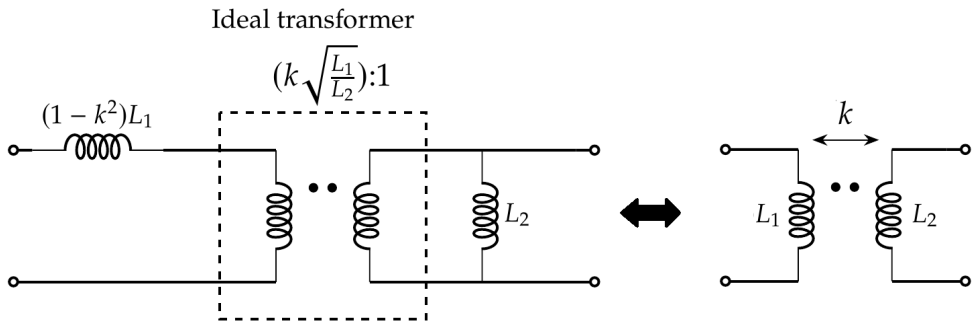


Figure A.4: Equivalent circuit of the transformer.

Alternatively, the inverse h-parameters (also known as the g-parameters) can be determined as well.

B

Cadence Circuits

The final Cadence schematics are shown here with component values in the following order:

- 1x LVHV 5 V single-ended PA (reference design)
- 2x HV 5 V push-pull PA
- 2x HV 10 V push-pull PA
- 2x LVLV 5 V push-pull PA
- 2x LVHV 10 V push-pull PA

The inductors indicated in red are coupled and form the input balun of the circuit. These inductors are given a quality factor of 10. All other inductors have Q = 15.

B.1. 1x LVHV 5 V Single-Ended

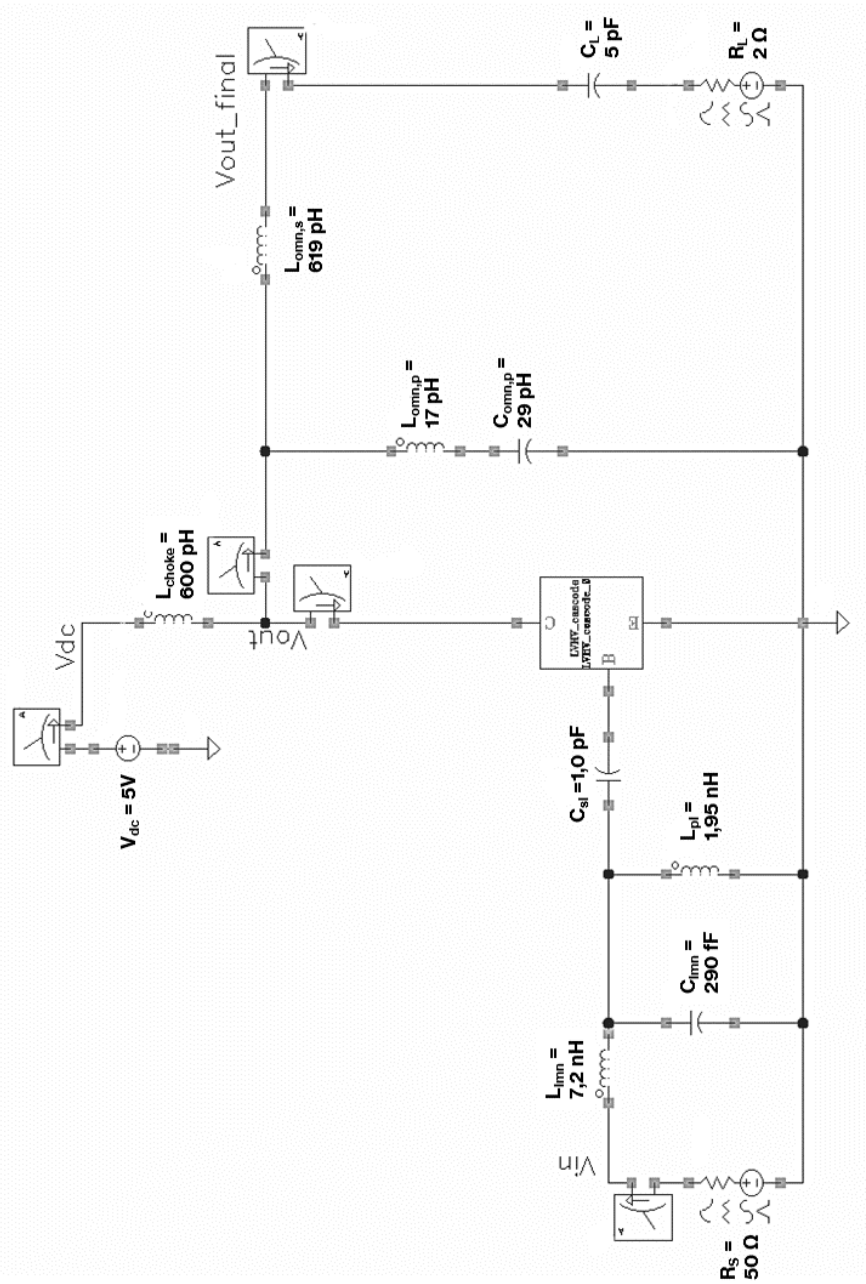


Figure B.1: Cadence schematic of the 1x LVHV 5 V single-ended amplifier with 5 V supply.

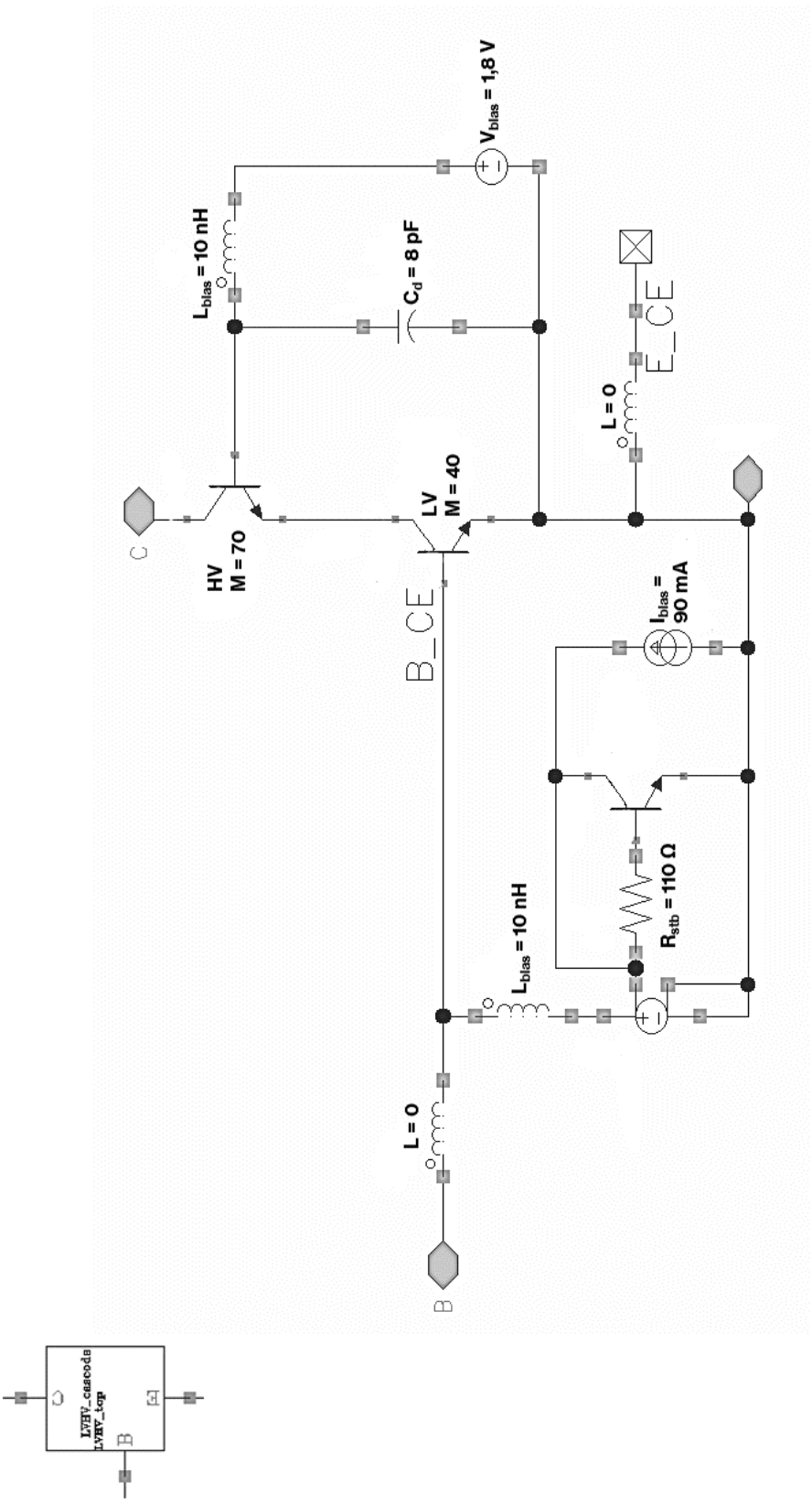


Figure B.2: Cadence schematic of the LVHV 5 V cascoded transistors.

B.2. 2x HV 5 V Push-Pull

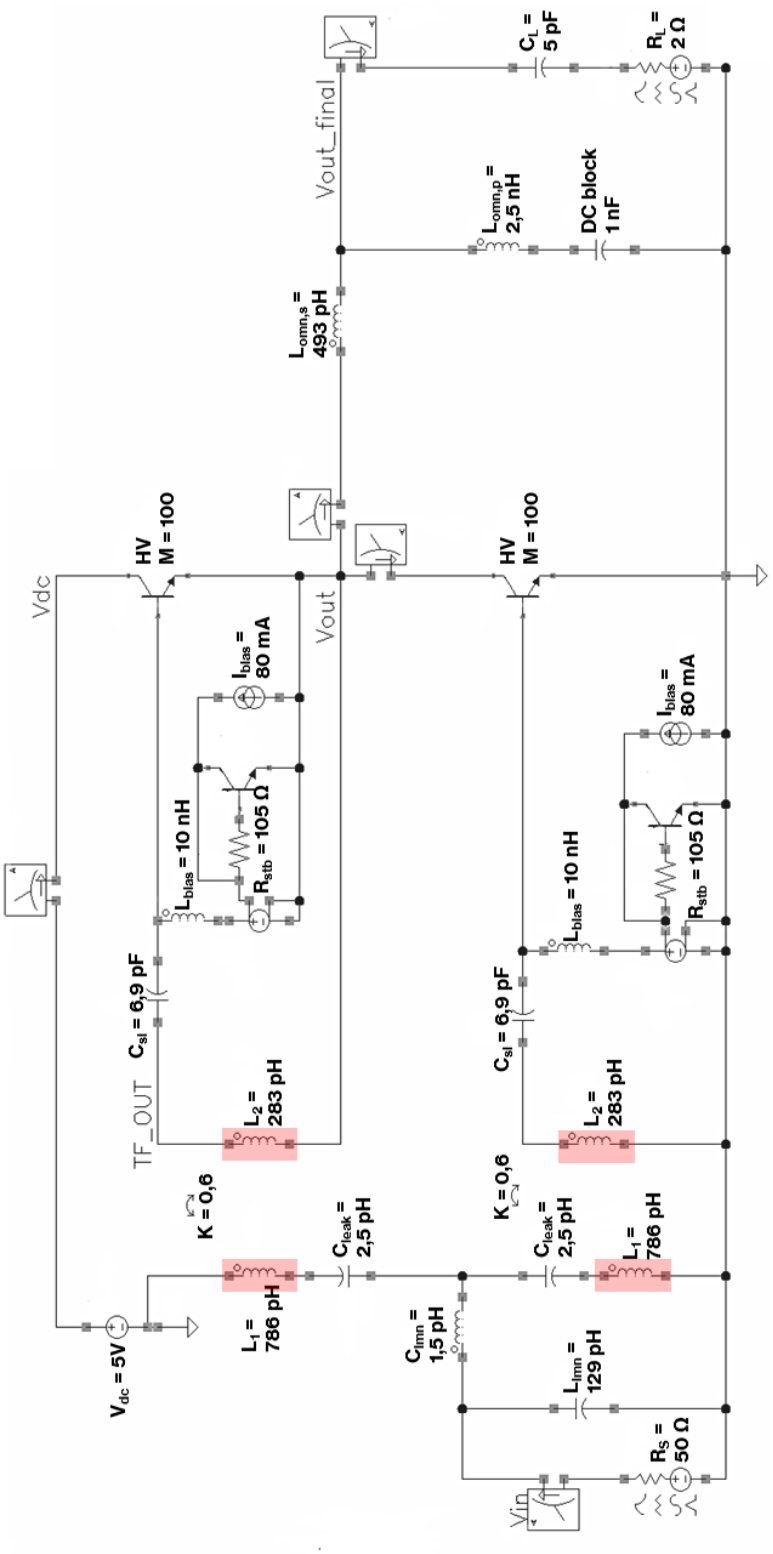


Figure B.3: Cadence schematic of the 2x HV push-pull amplifier with 5 V supply.

B.3. 2x LVLV 5 V Push-Pull

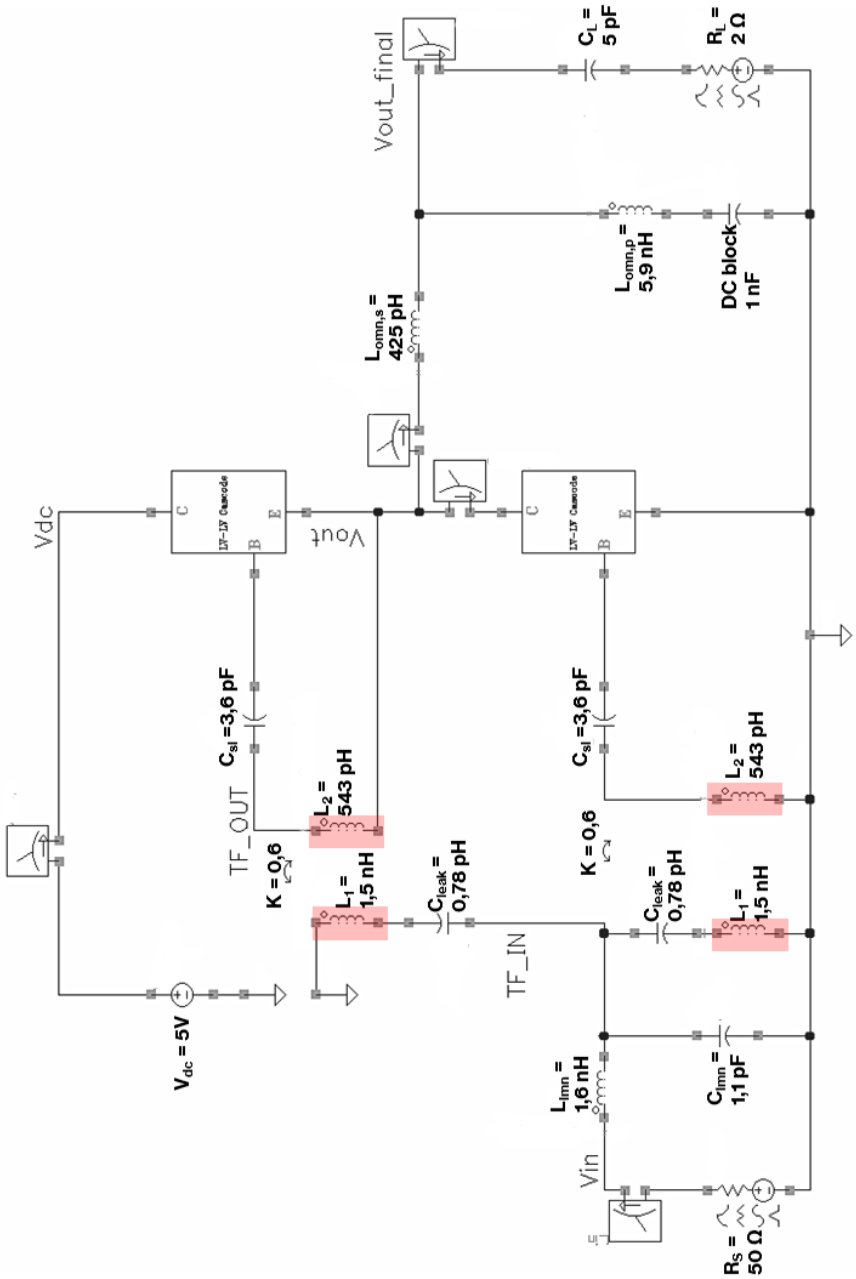


Figure B.4: Cadence schematic of the 2x LVLV push-pull amplifier with 5 V supply.

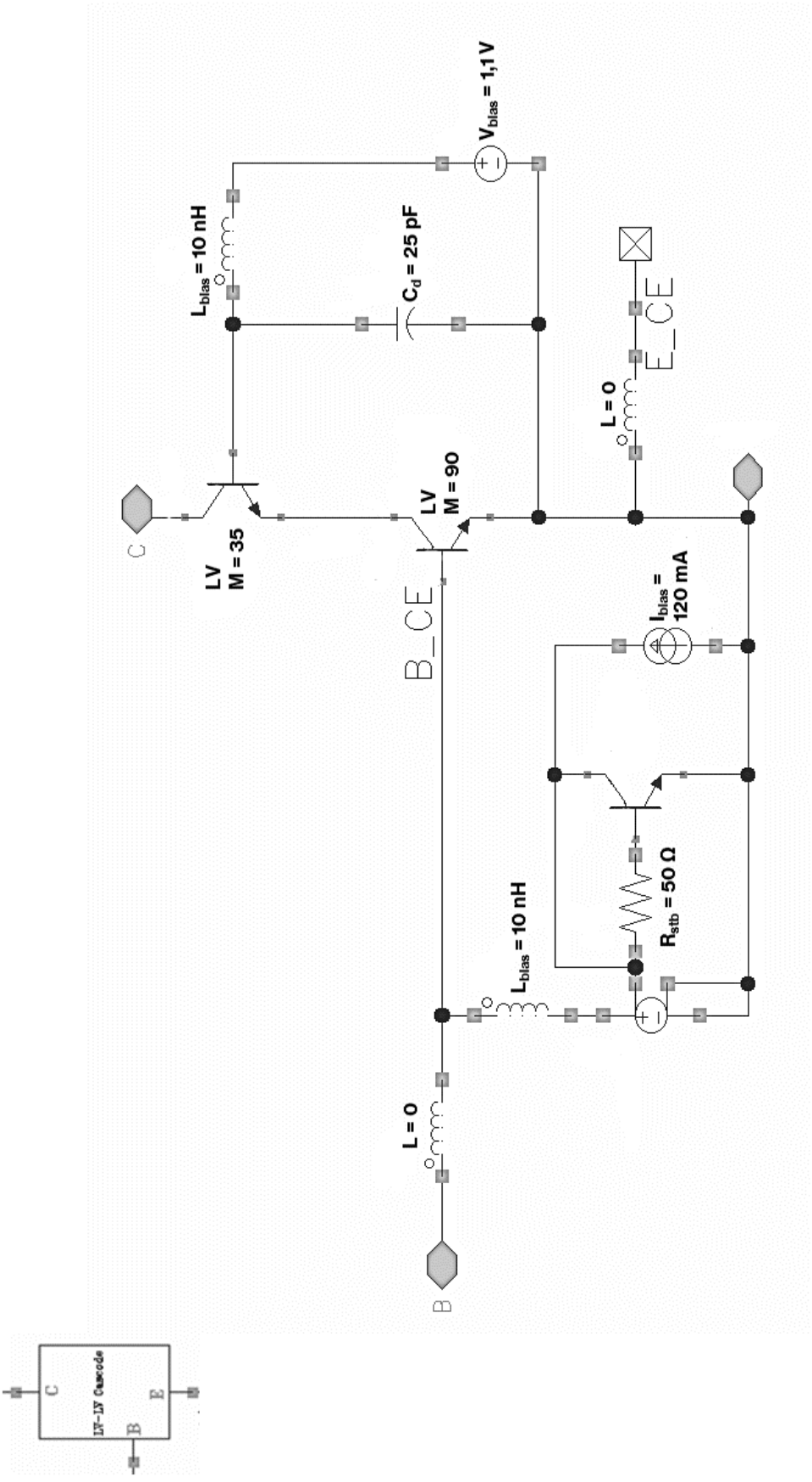


Figure B.5: Cadence schematic of the LVLV 5V cascoded transistors.

B.4. 2x LVHV 10 V Push-Pull

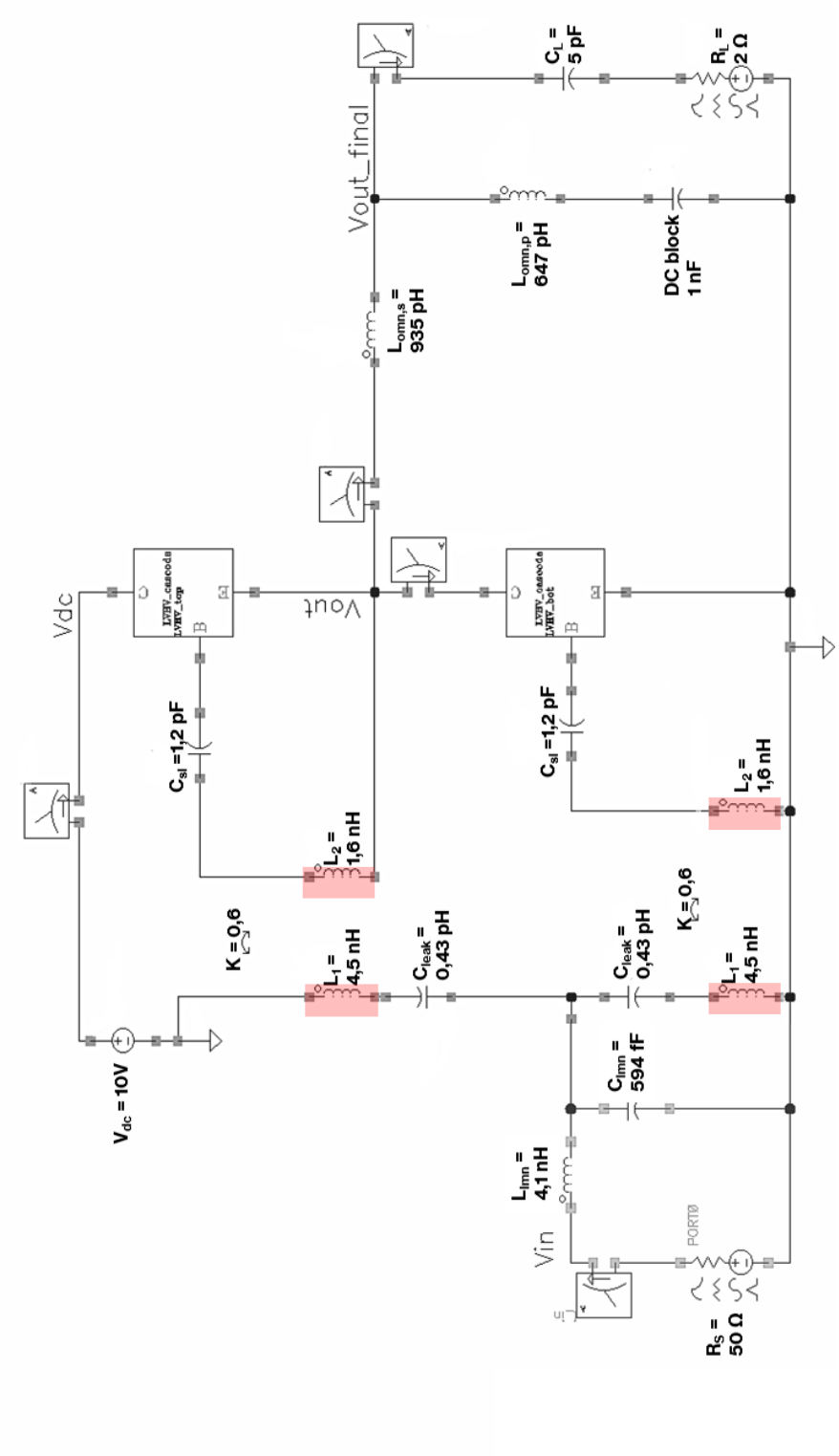


Figure B.6: Cadence schematic of the 2x LVHV push-pull amplifier with 10 V supply.

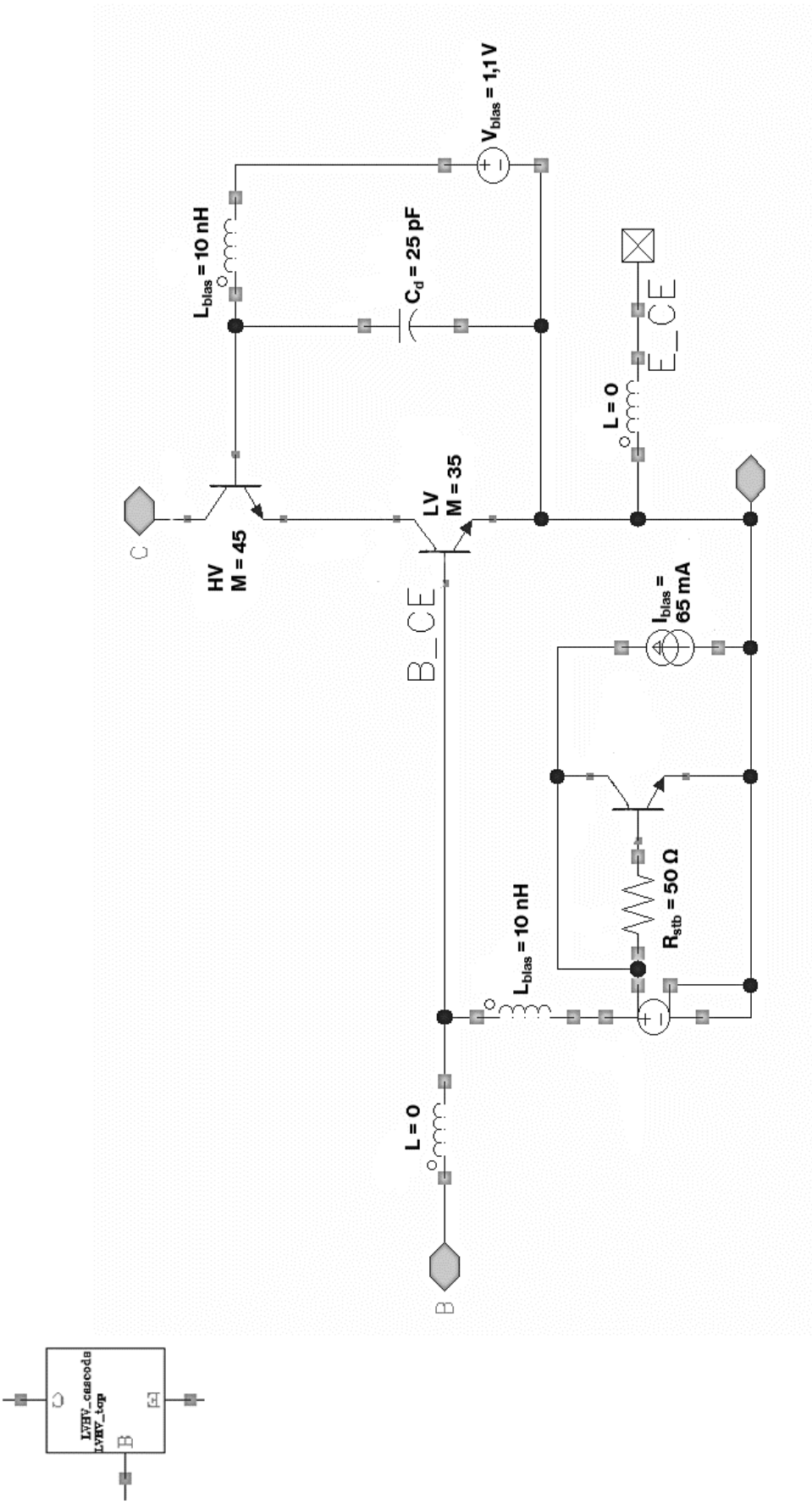


Figure B.7: Cadence schematic of the LVHV 10 V cascoded transistors.