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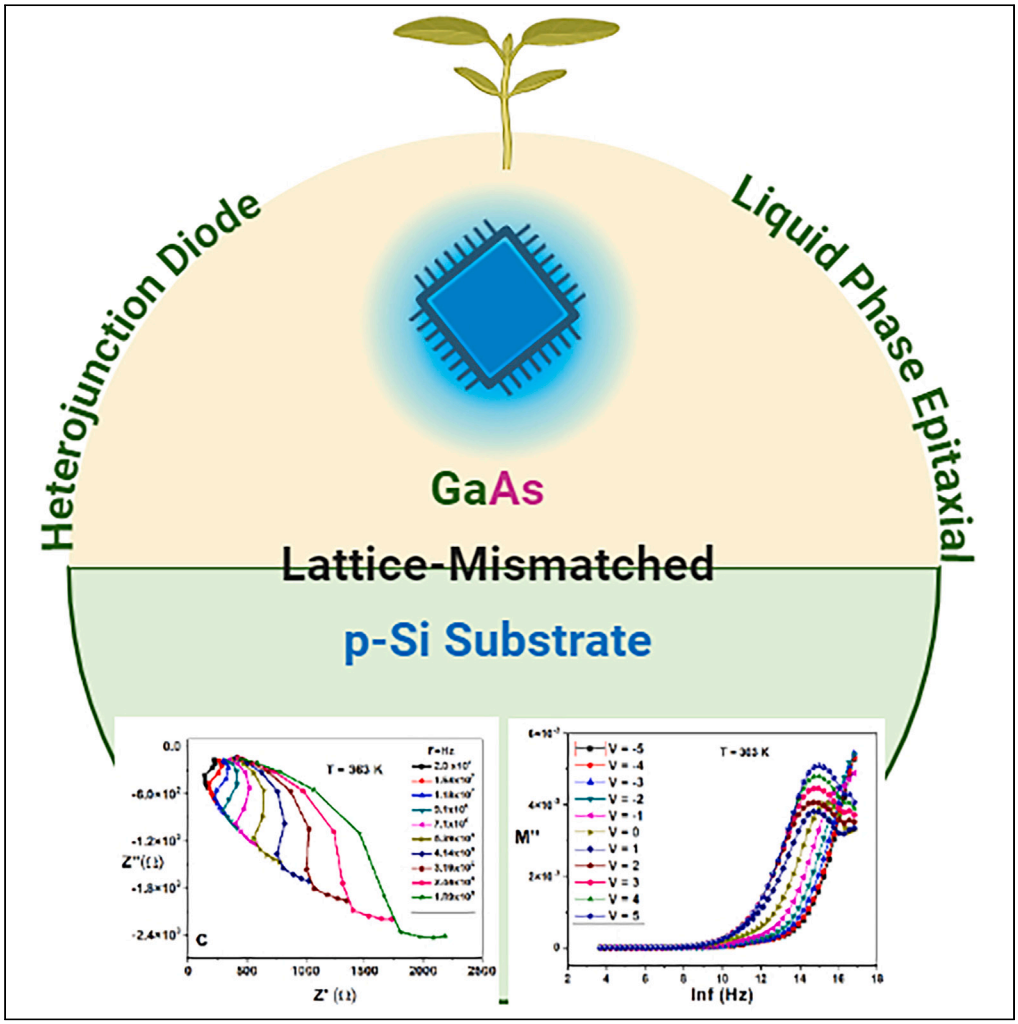

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Highlights

Tailoring dielectric properties through temperature, voltage, and frequency adjustments

Unique dielectric behaviors linked to lattice mismatch in GaAs/Si heterostructures

Liquid phase epitaxial growth of GaAs on silicon reveals novel electrical traits

High-frequency dielectric properties show unprecedented behaviors in GaAs/Si films

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Dielectric properties of epitaxially grown lattice-mismatched GaAs/p-Si heterojunction diode

A. Ashery,[1] A.E.H. Gaballah,[2] Mohamed M.M. Elnasharty,[3] and Mohamed A. Basyooni-M. Kabatas[4,5,6,7,*]

SUMMARY

The current work presents the possibility of tuning the dielectric parameters by changing the temperature, voltage, and frequency. The unusual behavior of some parameters was attributed to the lattice mismatch constant between gallium arsenide (GaAs) and silicon (Si) and the crystal defects between them. In this article, a thin GaAs film has been grown on Si substrates by liquid phase epitaxial (LPE) as n-GaAs/p-Si heterostructure. Despite the lattice mismatch between GaAs and Si, our interest in this article was focused on investigating the electrical and dielectric properties by I-V and C-V measurements. This was distinguished in the behavior of the dielectric properties such as the imaginary part of modules M″, the real and imaginary part of electrical conductivity σ'ac and σ''ac, respectively, which has not been seen before at high frequencies.

INTRODUCTION

Electronic interconnections have replaced optical ones due to their advantages, which include large bandwidth and low power consumption. These are gradually required for high-speed and high-capacity chip-to-chip information transmission.[1,2] Recent efforts have been made to manufacture silicon (Si)-based light sources as an essential component of modern optoelectronic devices.[3,4] Si is known to have an indirect bandgap that allows the employment of a light source on a chip. Although optical communications wavelength was obtained by erbium ions inserted on Si, the performance remains troublesome.[5–8] Germanium is also an indirect bandgap that can be epitaxially grown on Si, producing a pseudo-band gap.[9–11] However, getting a highly effective light source through III-V-founded LEDs is hard. Combining III-V with Si might provide an on-chip light source with excellent efficiency.

Combining III-V with Si has been tried using monolithic and heterogeneous integration techniques. III-V layers straddle Si wafers in heterogeneous integration and are attached by straight wafer bonding or adhesive-aided attachment approaches.[12,13] However, a thin layer between III-V and Si substrate has a slight thermal conductivity in addition to alteration in substrate dimension. Conversely, monolithic integration can offer a combination of large-scale wafers and brilliant thermal conductivity. The optoelectrical device systems used to deposit integrated III-V layers on Si substrates are essential. Mainly, gallium arsenide (GaAs) is often used for optoelectronic devices due to their significant carrier mobility. However, due to thermal expansion coefficients and lattice constants mismatches of GaAs and Si, the TD density of GaAs on Si was high, affecting the quality of the resulting film.[14–16] Various methods have been proposed to improve crystal quality and reduce the dislocation density of GaAs on Si. Current work presents the possibility of tuning dielectric constants by varying the temperature, voltage, and frequency despite the lattice mismatch constant between GaAs and Si and the structure defects between them. In this article, we fabricated thin films of GaAs on Si substrates by liquid phase epitaxial (LPE) as n-GaAs/p-Si heterostructure despite the mismatched lattice constant between GaAs and Si. The electrical and dielectric characteristics are determined by I-V and C-V measurements focused on the properties that, unlike the usual performance due to lattice-mismatched and structure defects, such as the imaginary part of M″ modules, the real and imaginary part of electrical conductivity σ'ac and σ''ac, respectively. The novel phenomenon that has been realized is the presence of a peak in the Modules (M″), the real and imaginary part of electrical conductivity, especially at high frequencies that have not been seen before.

RESULTS AND DISCUSSION

Figures 1A–1F shows the variation of M′ and M″ for Au/GaAs/p-Si/Al heterostructure with the voltage at different temperatures and different constant frequencies (1,216, 2×10^7, 40 Hz) respectively. In Figures 1A and 1B), M″ and M′ increase with decreasing temperature in the negative voltage region, producing peaks at all working temperatures. The peaks shift a little toward the positive voltage with increasing temperatures.

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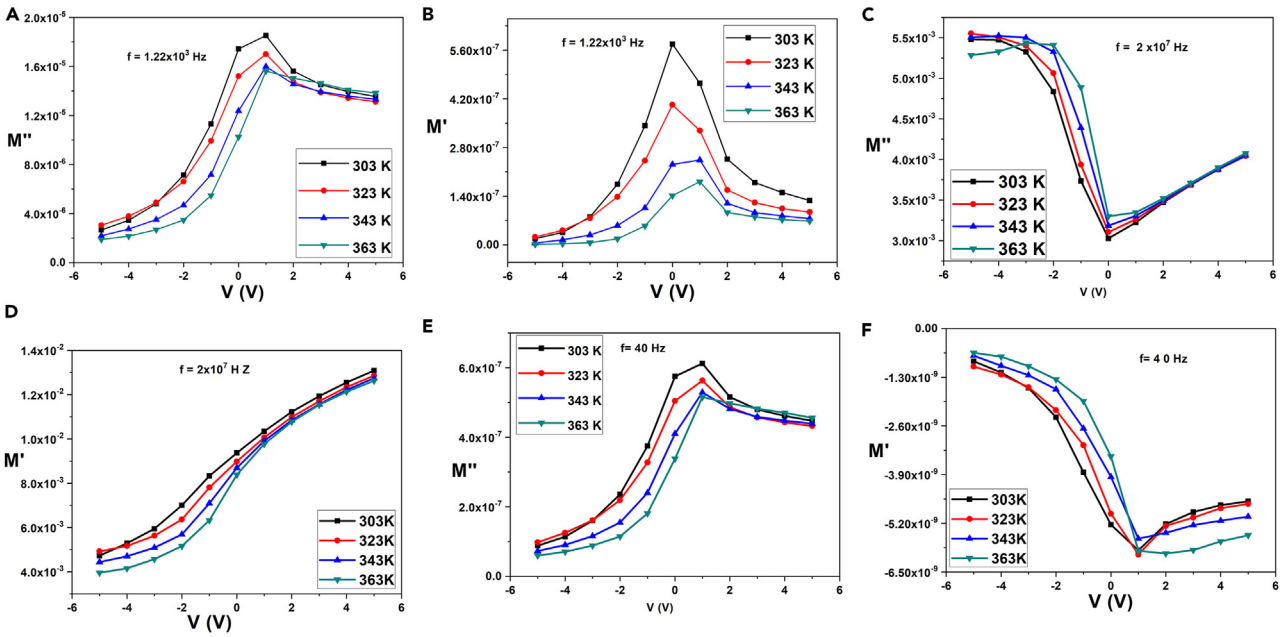

Figure 1. Variation of M′ and M′′′ for Au/GaAs/p-Si/Al heterostructure with voltage at different temperatures and constant frequencies

(A–F) Shows the variation of M′ and M″ for Au/GaAs/p-Si/Al heterostructure with voltage at different temperatures and constant frequencies (1,216 Hz, 2 × 10^7 Hz, 40 Hz). M″ and M′ increase with decreasing temperature in the negative voltage region, producing peaks at all temperatures. Peaks shift toward positive voltage with increasing temperatures. M′ and M″ behaviors are analyzed at different frequencies.

Still, the decrease in M′ is seen more than M″. Figures 1C and 1D shows the variation of M″ and M′ with the voltage at frequency 2 × 10^7 Hz; M″ increased in both voltage regions, while M′ shows a linear increase at the same frequency in both voltage regions. Figures 1E and 1F at frequency 40 Hz, M″ has the same behavior seen in Figure 1A at 1,216 Hz, but its value decreases with decreasing frequency from 18 × 10^{-5} to 6 × 10^{-7}. Also, M′ has a behavior similar to M″ at 2 × 107 Hz, but with negative values. At minor frequencies, M′ declines from 0. 012 to 1E-9; this approves the elimination of electrical polarity, while at high frequencies, the values decrease due to electrical polarity. Similar findings were presented in the literature.[17,18] This conduct can be credited to dielectric relaxation mechanisms that are somewhat subtle to frequency rather than the voltage in this area.[19–21] From previous studies, M′ and M″ can be tuned easily according to their desired application.

Figures 2A–2F display the variation of M″ and M′ with *ln*(f) at different temperatures and voltages. In all figures, M″ and M′ remains nearly zero at low frequencies, increasing linearly at mid and high frequencies. However, some findings have not been studied before, where M″ demonstrates peaks at high frequencies at voltages 5 v and 0 v as seen in Figures 2A and 2E. With decreasing voltages, the values of M′ decrease, as shown in Figures 2B, 2D, and 2F. This mechanism indicates that by increasing frequency, the energy of the charge carriers increases, which originates and increases the time of relaxation (r). This behavior of relaxation time (τ) is correlated with certain grains and grain borders in the MS assembly. Still, the difference in the frequency-dependent dielectric factors can be explained by the τ. Once the frequency of an external electric field is greater than the frequency of relaxation, the interfacial dipoles do not signify the alternative sign and, therefore, cannot donate to the dielectric constant. These performances are attributed to the polarity increasing with growing frequency in the Au/n-GaAs/p-Si/Al diodes.

The variance of M′ and M″ with the voltage at various frequencies at room temperature is shown in Figures 3A–3D. In Figures 3A and 3B, M′ increases with frequency from 1 × 10^{-8} at 40 Hz to 0.012 at 2 × 10^{-7}, while at low frequencies, M′ increases with voltage-producing peaks for all frequencies with a maximum at zero voltage and moves to the negative voltage region, M′ at high frequencies. M″ increases with rising frequencies and voltage for low frequencies, as shown in Figures 3C and 3D. Still, in high frequencies, some anomalies are seen in the behavior of M″, where it increases in reverse voltage and decreases in forwarding voltage as shown in Figure 3D. Such performance of M′, M″ vs. V schemes can be credited to the presence of the specific density delivery at border states of GaAs/Si interface.[22–24]

The variation of M″ and M′ with frequencies at different voltages and temperatures are given in Figures 4A–4F. It is known that the performance of M″ and M′ remains constant at low frequencies while it is linearly increased for all working voltages at mid and high frequencies. The innovation is that M″ increased linearly, allowing peaks that increase in turn while increasing the positive voltages at high frequencies. The increase in polarization with increasing frequency in the Au/n-GaAs/p-Si/Al diodes[22] is due to these actions.

The variance of the real and imaginary parts of ac conductivity σ′ac and σ″ac, respectively, with the voltage for Au/n-GaAs/p-Si/Al at various constant frequencies is shown in Figures 5A–5F. In the positive voltage regions, the behavior of σ′ ac approximately remains constant but increases in the negative region; its values increase with temperature and change with frequency as follows: (16 × $10^{-4,}$ 4 × 10^{-4}, 11 × 10^{-5}) (40, 2×10^7, 1216) Hz as seen in Figures 5B, 5D, and 5F. With the variety of frequencies, the σ″ ac has a different behavior; its values remain

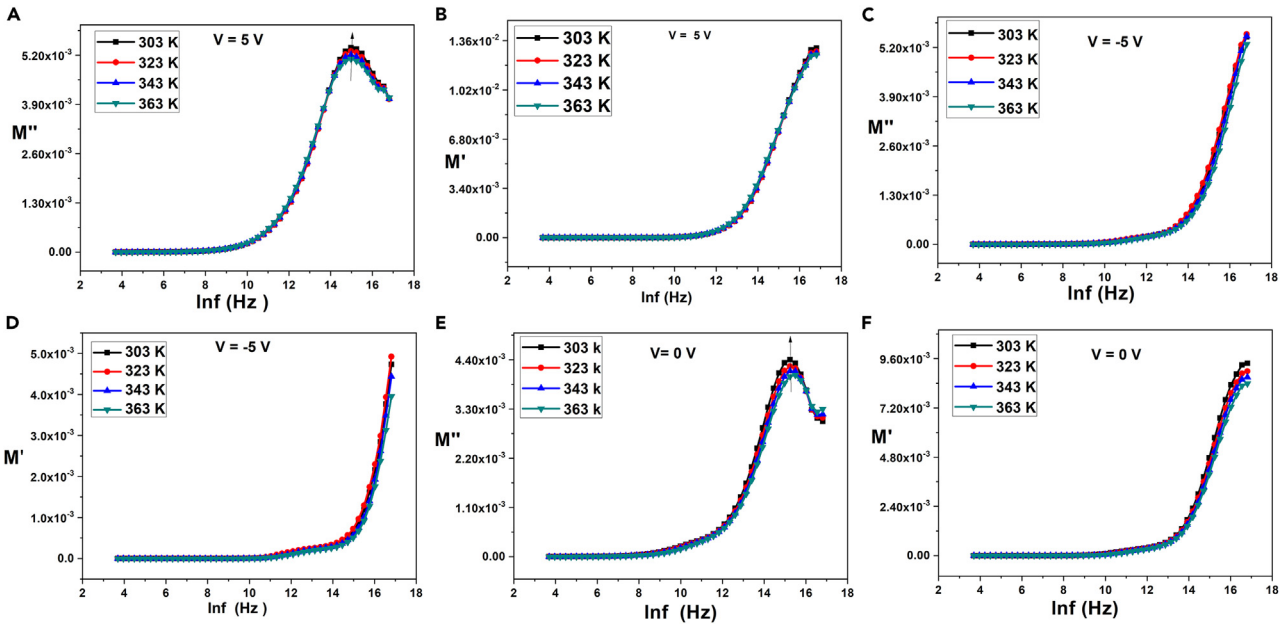

Figure 2. Variation of M″ and M′ with ln(f) at different temperatures and voltages

(A–F) Displays the variation of M″ and M′ with ln(f) at different temperatures and voltages. M″ and M′ remain nearly zero at low frequencies, increasing linearly at mid and high frequencies. Peaks are observed at high frequencies and specific voltages.

without changing in the forward voltage at 40 Hz but increase with increasing voltage in the reverse region, taking a positive value equal to 4×10^{-6} as shown in Figure 5A. The σ''ac rises in both parts of the voltage at frequency = 2×10^{-7} with greater values in the forward region. As highlighted in Figure 5E, the σ''ac values increase with temperature at frequency 1,216 Hz in the two positive and negative voltage areas, with values varying from -2.5×10^{-7} to -2.5×10^{-5}.

The material conductivity mechanism varies with many variables, such as frequency, temperature, voltage, surface treatment, thin-film width of oxide, barrier height between layers, etc. Thus, adequate knowledge of a specific voltage, temperature, and frequency variation is difficult to locate. After that, a similar analysis was carried out for many parameters, such as a broader shift in voltage, frequency of ac signs, temperature, etc.) that could help expose the materials' electrical properties. After that, the hopping process, which affects the electrical conductivity of ac, occurs in the forbidden bandgap by hopping charges.[25]

Figures 6A–6F shows the variation of σ'ac and σ''ac with frequency at different temperatures and different constant voltages. The σ'ac values increase with temperature, but their values overlap at all temperatures at specific frequencies, as shown in Figure 6B. In contrast, their value reaches a maximum of 14×10^{-4} at V = −5 V Figure 6F shows that at all temperatures, all curves overlapped, reaching a median value of 25×10^{-6} S cm less than Figures 6B and 6D. In Figures 6A, 6C, and 6E, the σ''ac is unchangeable at low and mid frequencies, while at high frequencies, it increases linearly with negative values. Still, a new phenomenon has been found in Figures 6A and 6C, where all curves split for all temperatures, creating small peaks at a particular high frequency.

Like other dielectric factors, the ac conductivity values display frequency-independent behavior generated at minor and mid frequencies and rise brusquely at high frequencies. The explanation for the sudden increase in conductivity at high frequencies[26] may be tunneling, hopping of charges, or free band conduction. The highest value of ac conductivity was 0.08 S cm at voltage −5 V, which decreased with voltage increase.

The variance of σ'ac and σ''ac with the voltage at various frequencies at room temperatures for the Au/n-GaAs/p-Si/Al structure is shown in Figures 7A and 7B. σ'_{ac} and σ''_{ac} behavior is opposite; σ'ac increased with increasing frequencies, but σ''ac decreased with increasing either the frequencies or the voltage producing peaks at a voltage equal to −1 V. Still, its positive voltage value is higher than the negative, as shown in Figure 7B σ'ac increased from positive to negative and reached a maximum value in the negative region.

The variance of σ'ac and σ''ac with frequency at various voltages and temperatures is shown in Figures 8A–8F. The new phenomena described previously are replicated again with more proof; the curves overlapped at high frequencies, splitting shaped peaks for all voltages is a new phenomenon and collected another time as shown in Figures 8A, 8C, and 8E. The σ' ac values increase in the entire voltage (−5 V to 5 V), and the phenomenon is repeated by appearing curves at high frequencies for all voltages and temperatures, as illustrated in Figures 8B, 8D, and 8F.

Total electrical conductivity σ'_{tot} dependent on frequency for Au/n-GaAs/p-Si/Al heterojunction at several temperatures are shown in Figure 9. It was given from the following equation.[27]

$$\sigma_{tot} = \varepsilon_0 \omega \varepsilon_2 + \sigma'_{ac} + \sigma'_{dc} \quad \text{(Equation 1)}$$

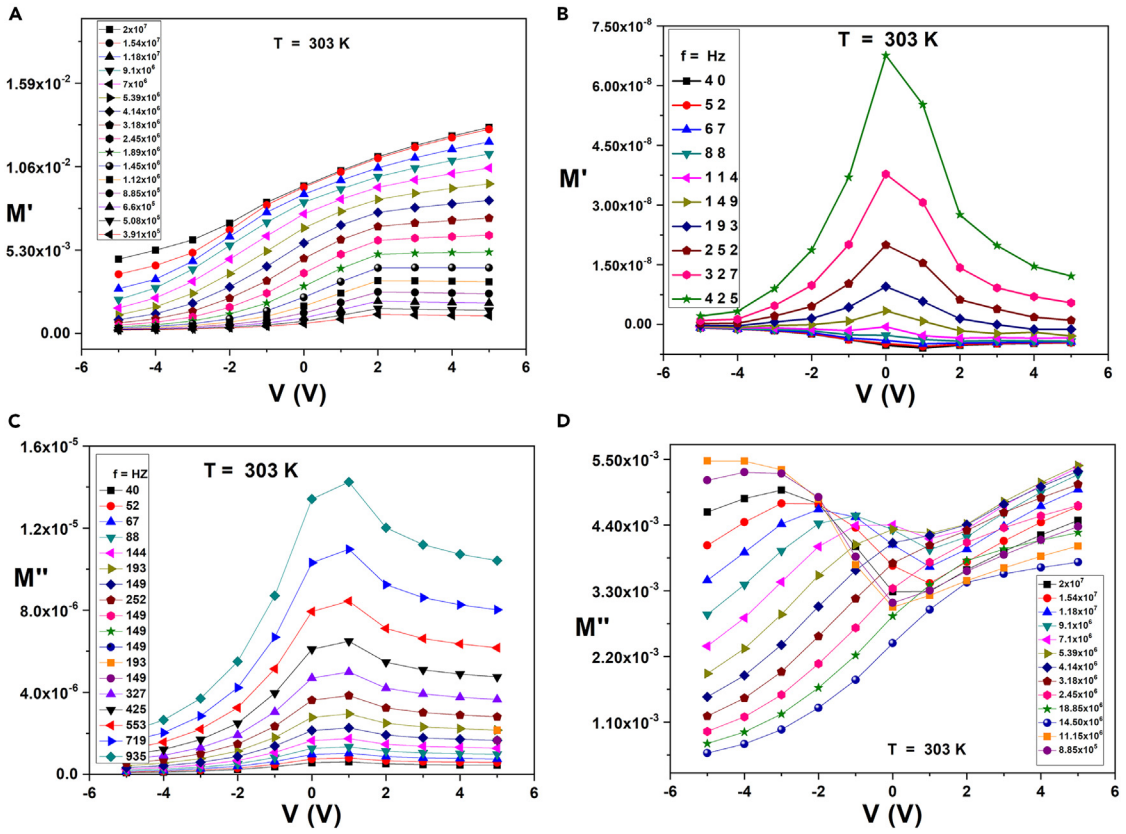

Figure 3. M′ and M″ versus voltage at different frequencies at room temperature

(A–D) M′ and M″ versus voltage at different frequencies at room temperature. M′ increases with frequency from 1 × 10^-8 at 40 Hz to 0.012 at 2 × 10^7 Hz. M″ increases with rising frequencies and voltage for low frequencies, showing anomalies at high frequencies.

where ε_2 is the dielectric loss, σ'dc is DC conductivity agreeing to nothing frequencies, and σ'ac is ac conductivity; by way of the frequency rises, the σ' ac rises as the polarization deduced. The increase in σ'ac leads to rising the swirling current in device,[28] which might be credited to the slight decrease in the (R_s) series resistance of the studied device.[29] The dependence of σ'_{tot} on frequencies is separated into three parts (I, II, and III) by dissimilar slopes, with low, middle, and high frequencies correspondingly, such dependency was explained by Jonscher's power law,[30] $\sigma'_{ac} = A\omega^s$ where A is a temperature-reliant constant, ω is the angular frequency, and S is the exponent of the frequency with $0 < s < 1$. In the low-frequency part (I), the conductivity increases linearly as the frequency increases. By fitting the curves in this part, the obtained values of the exponent s are less than unity and reduced from 0.5 to 0.3 with the rise of temperature. This performance of s with temperature has been detected for dissimilar kinds of thin films.[31] The conductivity shows a linear relationship with frequency in parts (II and III). In this section, the intentional values of s were found to be in the 0.98 to 0.9 range. As shown in Figure 9, the s value and temperature difference suggest that the associated barrier hopping model (CBHM) may be the transfer mechanism in these two sections (Figure 9A–9C).

The formalism of electric modulus (M) and impedance are related to each other to determine the diverse microscopic procedures responsible for local dielectric relaxations and long-range conductions.[32,33] Indeed, the M is vital for electrical relaxation procedures and is founded on capacitance influence. Complex electric modulus follows the Nyquist scheme shown in Figures 10A–10C. The semicircle arch from the left-hand side agrees with the influence of grain border capacitance C_{gb} at minor frequency, then the arc on the right side agrees with the influence of grain capacitance C_{gb} at high frequency; it is evident that the radius of the arc increases with increasing voltages, especially in positive and negative voltages. This designates that the detected semicircle arcs in Figures 10A–10C are credited to the influence of grain and grain border effect.[34,35]

The complex impedance measurement of the Au/n-GaAs/p-Si/Al at various frequencies and different constant temperatures is shown in Figures 11A–11D, the semicircle component at a low frequency corresponding to the grain boundary.[36–38] A corresponding circuit, assumed in Figure 10D, has modeled the impedance system.

The depletion layer capacitance for Au/n-GaAs/p-Si/Al can be stated as[23]:

$$C = \left[\frac{q\varepsilon_s\varepsilon_0 A^2 N_D}{2}\left(V_{bi} - \frac{kT}{q}V_r\right)\right]^{1/2} \quad \text{(Equation 2)}$$

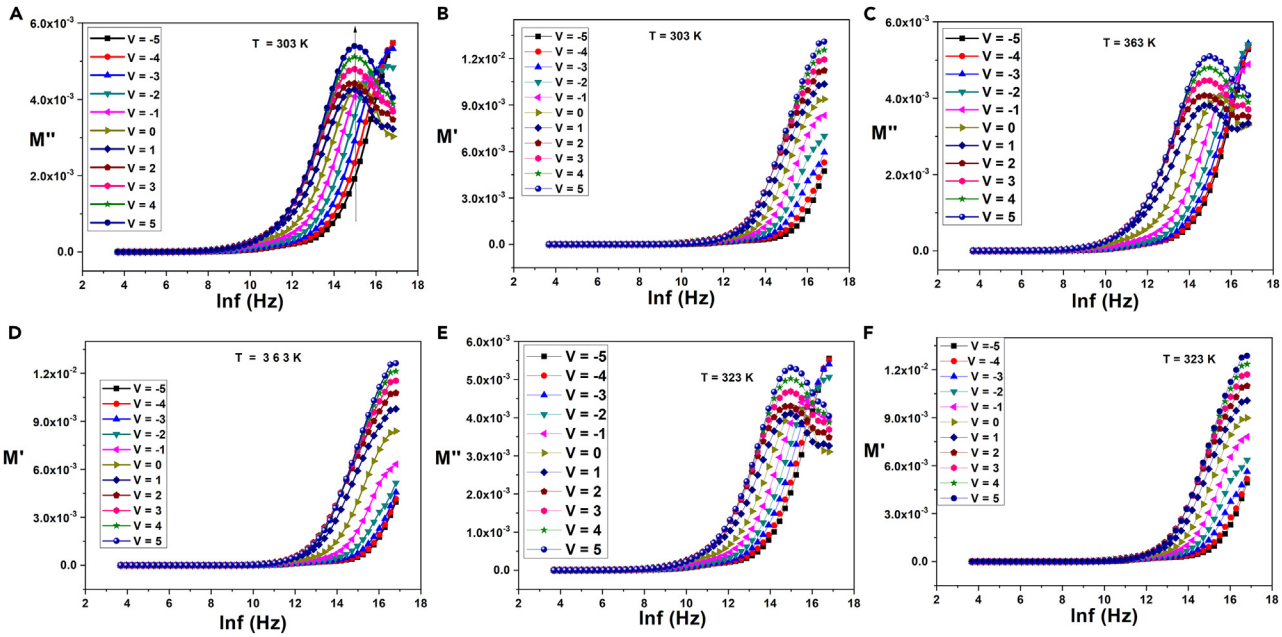

Figure 4. M″ and M′ versus ln(f) at different voltages and temperatures

(A–F) M″ and M′ versus ln(f) at different voltages and temperatures. M″ and M′ remain constant at low frequencies, increasing linearly at mid and high frequencies, with peaks at high frequencies and specific voltages.

Therefore, specific chief electrical factors such as V_{bi}, E_F, and Φb(C-V) can be calculated from the lined fragments of C^{-2}-V schemes for every frequency by Equation 3.[39]

$$C^{-2} = \frac{2\left(V_{bi} - \frac{kT}{q}V_r\right)}{q\varepsilon_s\varepsilon_0 A^2 N_A} \quad \text{(Equation 3)}$$

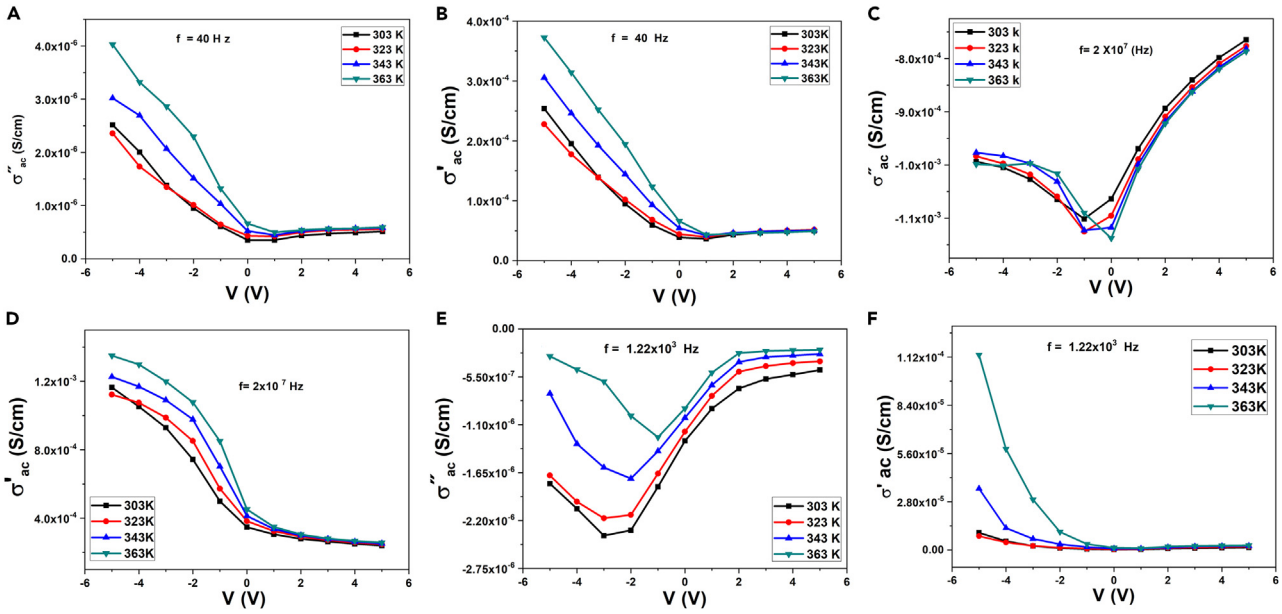

Figure 5. σ′ac and σ″ac versus voltage at different temperatures and constant frequencies

(A–F) σ′ac and σ″ac versus voltage at different temperatures and constant frequencies. σ′ac remains constant in positive voltage regions, increasing in negative regions. σ″ac behavior changes with frequency and temperature.

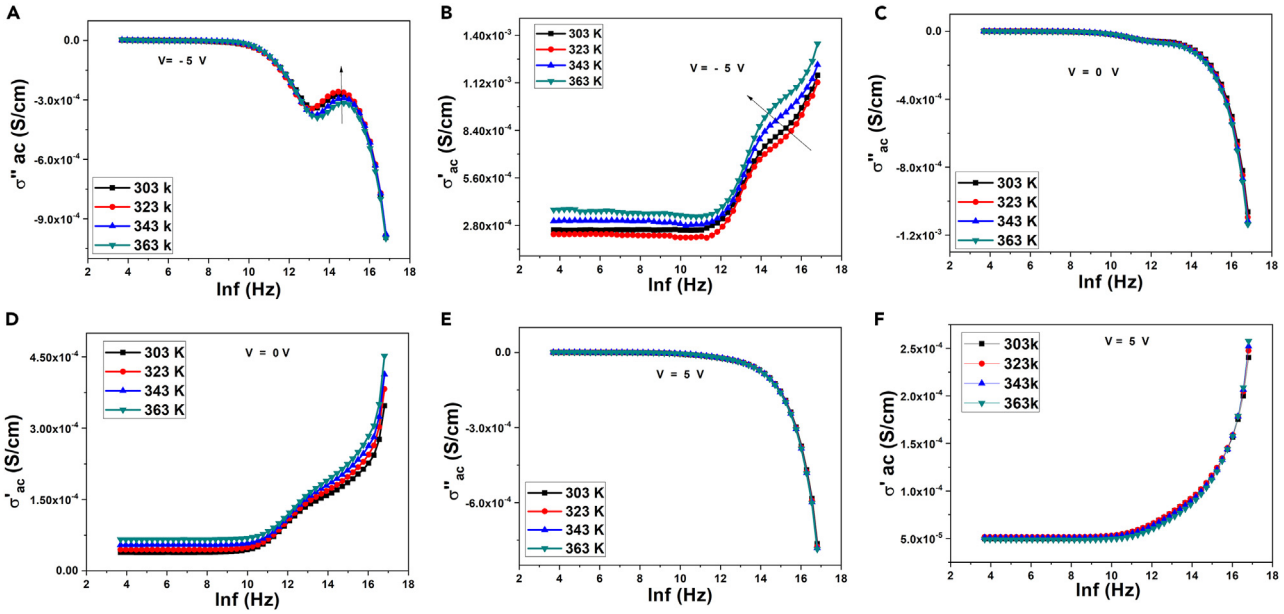

Figure 6. Variation of σ′_ac and σ″_ac with frequency at different temperatures and constant voltages

(A–F) Shows the variation of σ′_ac and σ″_ac with frequency at different temperatures and constant voltages. σ′_ac values increase with temperature, overlapping at specific frequencies. σ″ac shows a linear increase with frequency, displaying new peaks at high frequencies.

where, V_{bi} is the build-in voltage agreeing to interrupt voltage, V is the practical bias voltage, ε_o is the dielectric constant of space (8.85×10^{-14}F/cm), while ε_s is the dielectric constant of Si, which has the value (11.8), A is the area, N_A is the doping concentration of acceptor. Figure 12. C^{-2}-V scheme has a linear region at each frequency in the voltage range between (2V to −2V). Consequently, the amount of V_o and N_A were created from the interrupt and grade of the lined part of the C^{-2}-V scheme for every frequency, and its values are summarized in Table 1.

The surface and interfacial states are extra active on the C^{-2}-V scheme. In this circumstance, the investigational value of N_A can be significantly lower than its theoretical value, which might be stated as the following.[22,23,40–42]

$$C_2 > \frac{N_A(exp.)}{N_A(thor.)} = \frac{\varepsilon_i}{\varepsilon_i + q\delta N_{ss}} \quad \text{(Equation 4)}$$

Hence, the amount of the barrier height Φb(C-V) might be obtained from Equation 4 as follows.

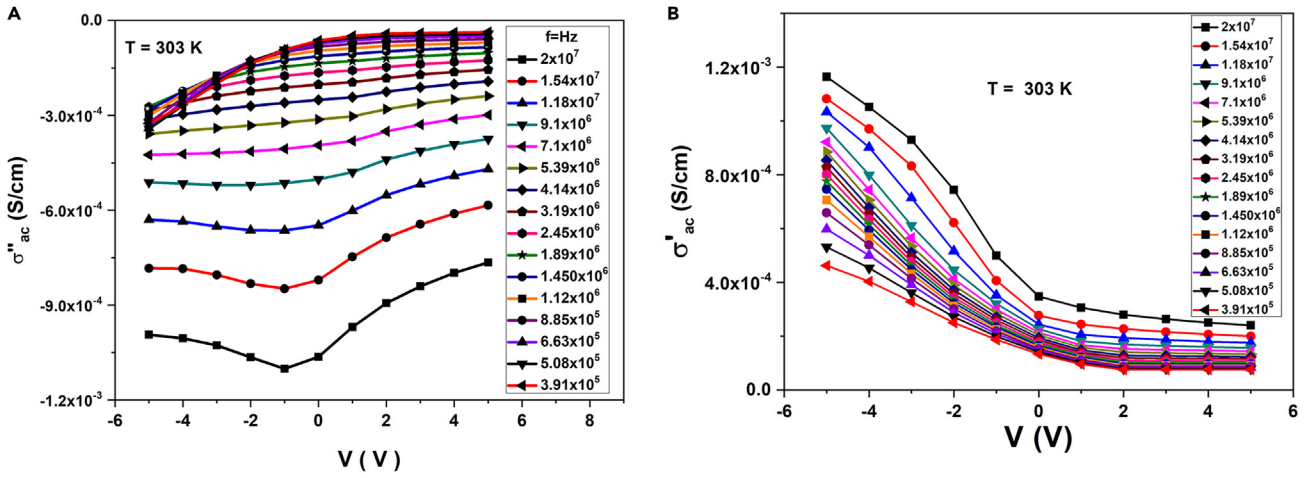

Figure 7. σ′_ac and σ″_ac versus voltage at different frequencies at room temperature

(A and B) σ′_ac and σ″_ac versus voltage at different frequencies at room temperature. σ′ac increases with increasing frequencies, while σ″ac decreases with increasing frequencies or voltage, producing peaks at specific voltages.

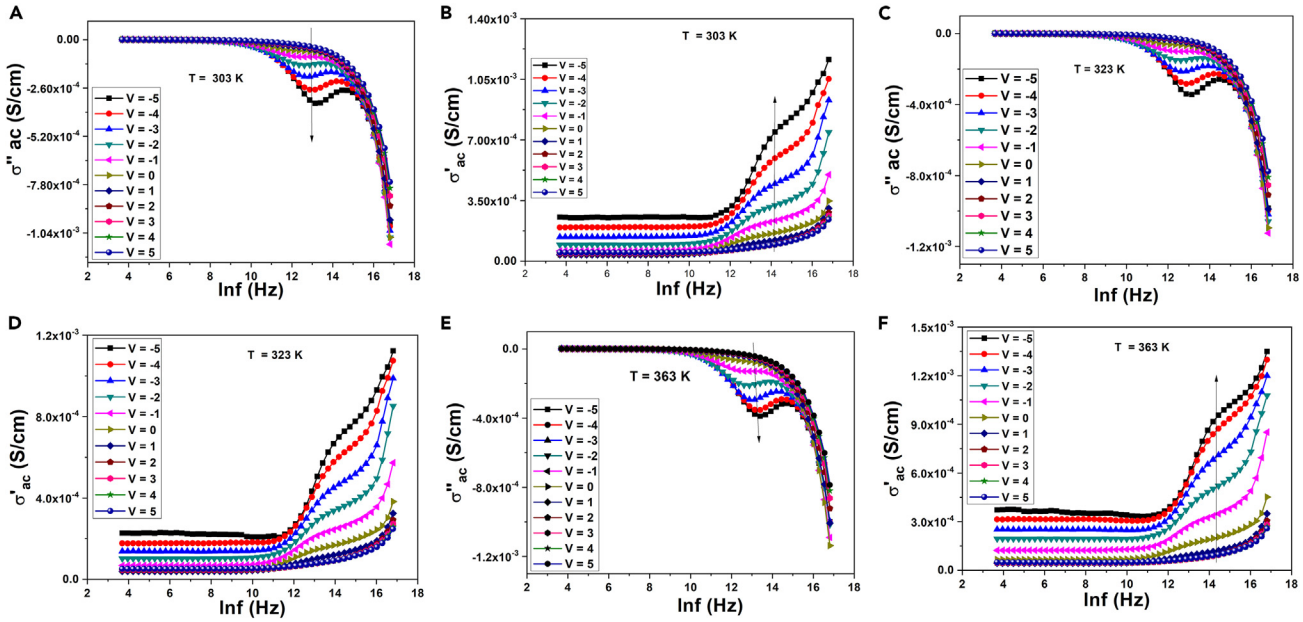

Figure 8. σ'_ac and σ''_ac versus ln(f) at different voltages and constant temperatures

(A–F) σ'_ac and σ''_ac versus ln(f) at different voltages and constant temperatures. σ'ac values increase across all voltages, with peaks at high frequencies.

$$\phi_b = c_2 V_0 \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right) = V_D + E_F \qquad \text{(Equation 5)}$$

where N_V is the real density of states in the Si valence band, and E_F is the Fermi level.[41]

The value of N_{ss} for the assembly is given by Equation 4. The obtained trial values of Φb(C-V) and E_F from the C^{-2}-V schemes for all frequencies are summarized in Table 1. In Figures 13 and 14, the amount of Φb(C-V) and the value of E-Fermi are functions of frequency; Φb(C-V) and E_F values increase with increasing frequency. The Hill-Coleman method[22] is used to evaluate the quantity of N_{ss} as a function of frequency. Rendering this process, the sum of N_{ss} for each frequency could be obtained by the following equation from the peak values of G/ω-V C-V schemes at room temperature:

$$N_{ss} = \frac{2}{qA}\left[\frac{(G/\omega)_{max}}{\left(\frac{(G/\omega)_{max}}{C_{0x}}\right)^2 + (1 - (C_m/C_{0x}))^2}\right] \qquad \text{(Equation 6)}$$

where the amount of Gm/ω and C_m is the measured conductance and capacitance, which agree to its peak values.

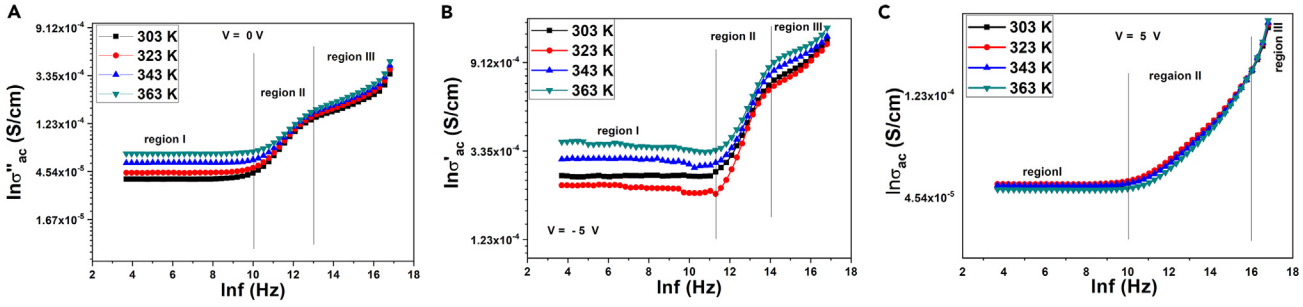

Figure 9. Frequency dependence of σ'_tot at different temperatures of the Au/n-GaAs/p-Si/Al heterostructure

(A–C) Frequency dependence of σ'_tot at different temperatures of the Au/n-GaAs/p-Si/Al heterostructure. σ'_tot increases linearly at low frequencies, with different slopes in mid and high frequencies.

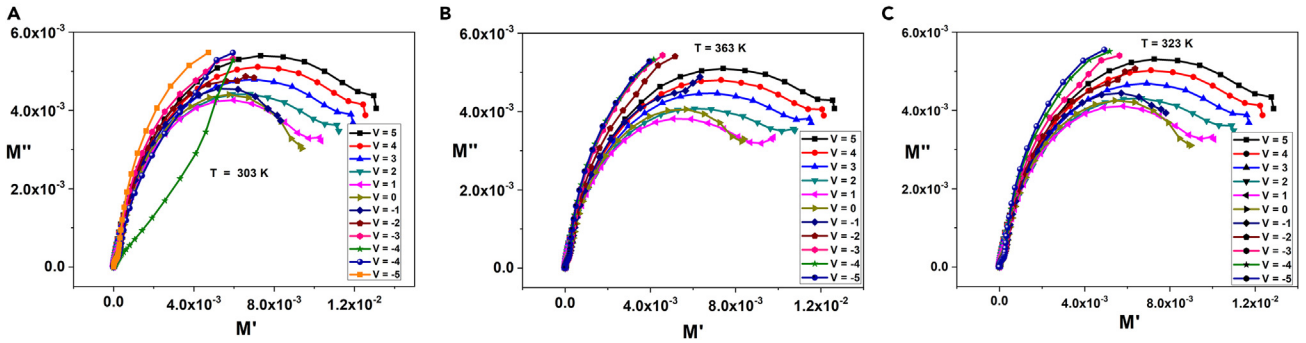

Figure 10. M″ versus M′ at different voltages and constant temperatures

(A–C) M″ versus M′ at different voltages and constant temperatures. Semicircle arcs represent grain boundary effects, with arc radius increasing with voltage.

The amount of interfacial thin-film capacitance (C_{ox}) can be found from the G/ω and C values at robust accumulation area for adequately high frequency as the subsequent equation.

$$C_{0x} = C_m\left[1 + \left(\frac{G_m}{\omega C_m}\right)^2\right] \quad \text{(Equation 7)}$$

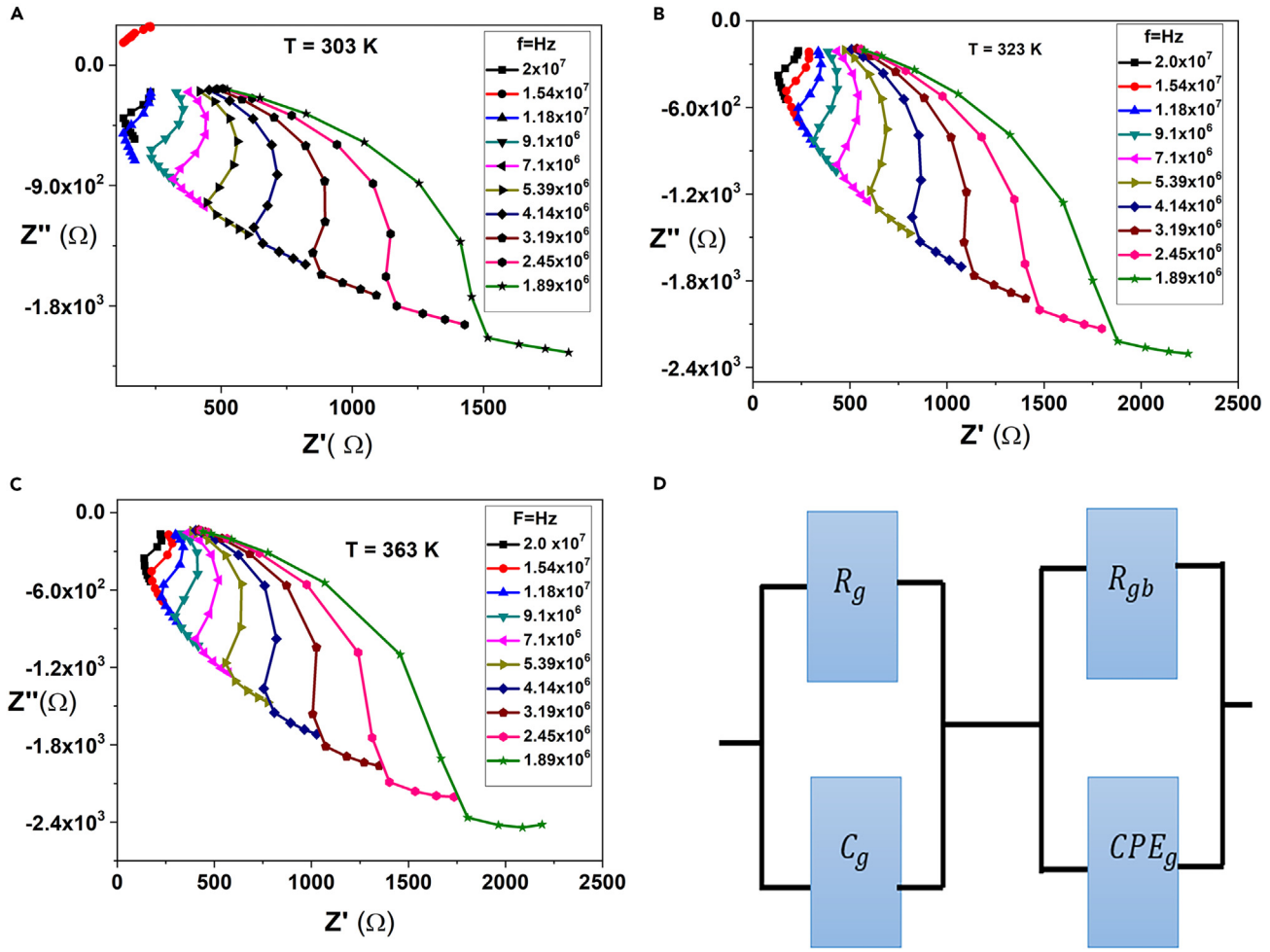

Figure 11. Z″ versus Z′ at different frequencies and constant temperatures

(A–D) Z″ versus Z′ at different frequencies and constant temperatures. Semicircle components correspond to grain boundary effects, modeled by the equivalent circuit.

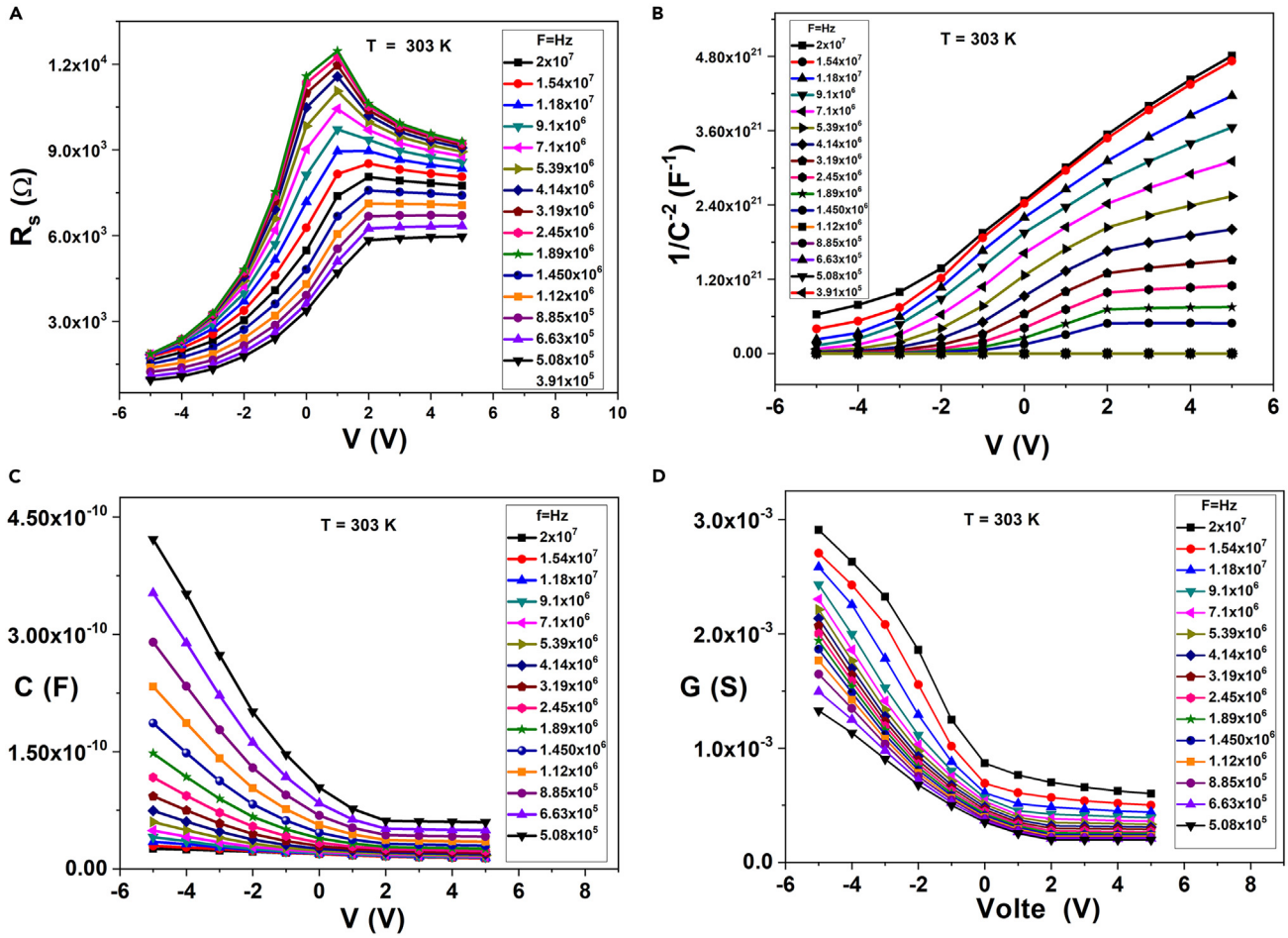

Figure 12. Rs, 1/C-2, C, G versus V at Different Frequencies and Room Temperature

(A–D) Rs, $1/C^{-2}$, C, G versus V at different frequencies and room temperature. Linear regions at each frequency indicate barrier height and doping concentration values.

$$qAN_{ss} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1} \quad \text{(Equation 8)}$$

The C_m and Gm/ω have the behavior shown in Figures 12C and 12D, so the quantities of N_{ss} were separately designed by the Hill Coleman method for each peak and given in Figure 15. The amount of N_{ss} strongly depends on frequency; the impact of the passivation effect of the interfacial layer as thin oxide thin films is such a small value of N_{ss}.

The investigational CLF-CHF capacitance approach is another way to compute the voltage based on the N_{ss} profile.[15,20] The N_{ss}-V method for the Au/n-GaAs/p-Si/Al is accepted in Figure 16, where the capacitance measured at low and high frequencies is measured in CLF and CHF. The interfacial thin-film capacitance is Ci, and the region and A are the areas.

As indicated in Figure 16, the amount of N_{ss} decreases with rising applied voltage. The advantage of this way is that numerous features of the thin film interface can be very quickly and accurately intentional. The values found by N_{ss} from many methods are in agreement with each other, and their order is reasonably suitable for such devices. All these test results show that the N_{ss}, Rs, and interfacial thin film are extra active on the impedance measurements. Therefore, they should be taken into account when making electrical parameter measurements.

Conclusion

Tuning the dielectric constants in terms of the behavior by controlling the temperature, voltage, and frequency are presented. The appearance of new performance for some particular parameters was attributed to the structural defects and lattice mismatch constant between GaA and Si and here focused on properties remarkably dissimilar from the usual performance due to the lattice-mismatched and crystal defects. This was obvious in the performance of the dielectric properties such as the imaginary part of modules M″, the real and imaginary part of electrical

Table 1. The numerous parameters extracted from the C^{-2}-V curves for Au/n-GaAs/p-Si/Al Schottky diode

Frequency (Hz)	2×10^7	1.89E+06	1.05E+05	12,900	1,581	935	425	114
N_c (cm^{-3})	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}	2.81×10^{19}
N_v (cm^{-3})	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}	1.05×10^{19}
$N_A = N_D$ (cm^{-3})	4.50×10^{11}	1.05×10^{12}	3.21×10^{14}	9.54×10^{15}	1.59×10^{19}	1.06×10^{20}	7.95×10^{21}	1.19×10^{24}
V_0 (V)	4.50	1.45	3.67	2.55	1.70	1.60	1.60	1.10×10^{-1}
V_d (V)	4.53	1.48	3.70	2.58	1.73	1.63	1.63	1.36×10^{-1}
E-Fermi (eV)	0.44	0.42	0.27	0.18	−0.01	−0.06	−0.17	−0.30
Φ_b (eV)	4.96	1.89	3.96	2.76	1.72	1.57	1.45	−0.17
C_{0x} (F)	4.79×10^{-11}	3.41×10^{-19}	2.12E-09	1.57×10^{-8}	1.28×10^{-7}	2.17×10^{-7}	4.74×10^{-7}	1.75×10^{-6}
d_{OX} (nm)	2.33×10^7	3.27×10^6	5.26×10^5	7.09×10^4	8.68×10^3	5.14×10^3	2.35×10^3	6.36×10^2
N_{ss} ($eV^{-1}cm^{-2}$)	2.90×10^{11}	1.65×10^{11}	1.11×10^{12}	7.52×10^{12}	6.11×10^{13}	1.03×10^{14}	2.15×10^4	8.32×10^{14}
R_s (Ω)	6.63×10	9.85×10	2.85×10^2	3.12×10^2	3.11×10^2	3.12×10^2	3.12×10^2	3.16×10^2
Y_m (cm)	9.02×10^{-3}	6.04×10^{-3}	2.10×10^{-3}	1.90×10^{-3}	1.91×10^{-3}	1.90×10^{-3}	1.89×10^{-3}	1.88×10^{-3}
E_m (V/cm)	9.25	8.01	2.23×10^2	1.01×10^3	3.38×10^4	8.49×10^4	7.34×10^5	2.36×10^6
W_d (cm)	3.82×10^2	1.42×10^2	1.29×10	1.98	3.95×10^{-2}	1.48×10^{-2}	1.72×10^{-3}	3.67×10^{-5}
$\Delta_{\Phi b}$ (eV)	3.37×10^{-5}	3.14×10^{-5}	1.66×10^{-4}	3.53×10^{-4}	2.04×10^{-3}	3.23×10^{-3}	9.50×10^{-3}	1.70×10^{-2}

The numerous parameters extracted from the C-2-V curves for Au/n-GaAs/p-Si/Al Schottky diode.

conductivity σ'ac and σ''ac, respectively. The new phenomena that have seemed are the presence of a peak in the Modules (M″), the real and imaginary part of electrical conductivity. These σ'''ac at high frequencies have not been seen before in the research related to that matter.

Limitations of the study

This study presents novel findings on tuning dielectric constants by controlling temperature, voltage, and frequency. However, it is limited by the lack of quantitative analysis of structural defects and lattice mismatches between GaA and Si. The observed phenomena were specific to particular conditions, and high-frequency behaviors need further exploration. Future research should address these aspects to enhance the understanding and applicability of these findings.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

- KEY RESOURCES TABLE
- RESOURCE AVAILABILITY

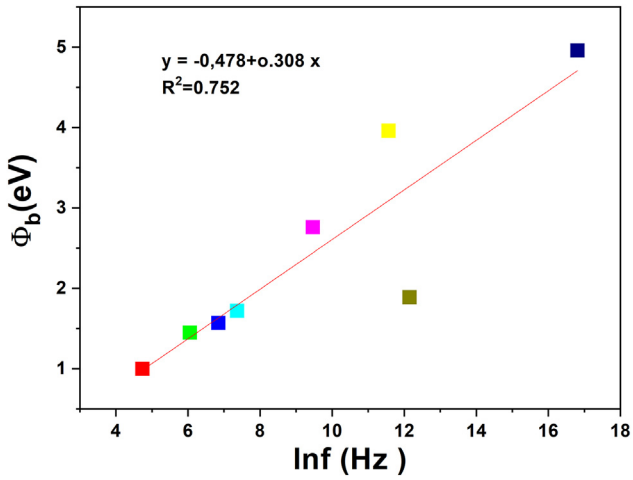

Figure 13. Barrier height versus ln(f) for Au/n-GaAs/p-Si/Al

Barrier height versus ln(f) for Au/n-GaAs/p-Si/Al. Barrier height values increase with frequency.

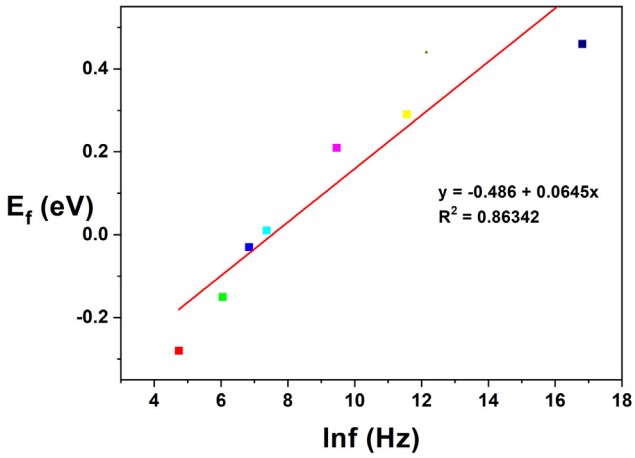

Figure 14. E_F versus ln(f) for Au/n-GaAs/p-Si/Al

E_F versus ln(f) for Au/n-GaAs/p-Si/Al. E_F values increase with frequency.

- Lead contact
- Materials availability
- Data and code availability

- EXPERIMENTAL METHOD DETAILS

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Not available.

AUTHOR CONTRIBUTIONS

A.A. contributed to conceptualization, data curation, methodology, and visualization. A.E.H.G. contributed to conceptualization, data curation, methodology, writing – original draft, and writing – review & editing. M.M.M.E. contributed to data curation, investigation, visualization, and methodology. M.A.B.-M.K. contributed to visualization, writing – original draft, and writing – review & editing.

DECLARATION OF INTERESTS

The authors declare no competing interests.

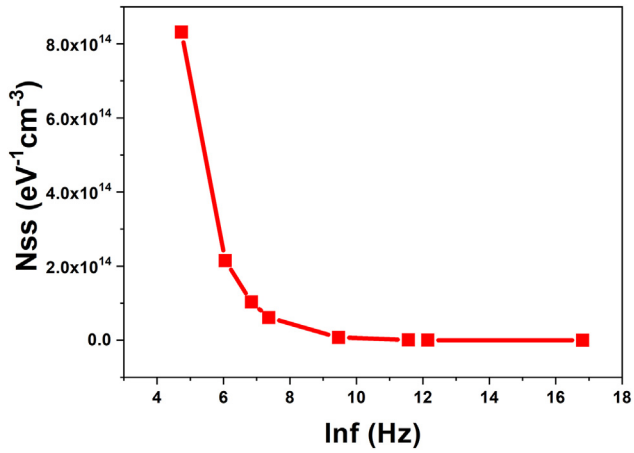

Figure 15. N_{ss} versus ln(f) for Au/n-GaAs/p-Si/Al

N_{ss} versus ln(f) for Au/n-GaAs/p-Si/Al. N_{ss} values depend on frequency and passivation effects of interfacial layers.

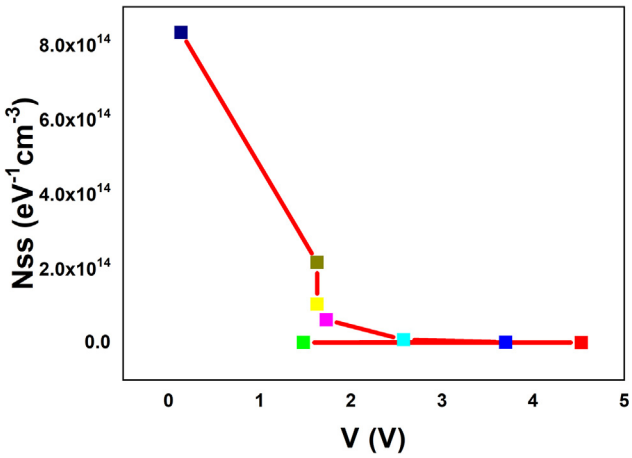

Figure 16. N_{ss} versus voltage for Au/n-GaAs/p-Si/Al

N_{ss} versus voltage for Au/n-GaAs/p-Si/Al. N_{ss} values decrease with increasing applied voltage.

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STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals, peptides, and recombinant protiens		
P-type monocrystalline silicon substrates	Sigma-Aldrich	647705
Hydrofluoric acid	Sigma-Aldrich	695068
Gallium arsenide (small pieces 3 mm)	Sigma-Aldrich	215-114-8
Indium solution	Sigma-Aldrich	1.19504

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Dr. Mohamed A. Basyooni-M. Kabatas (m.kabatas@tudelft.nl & m.a.basyooni@gmail.com).

Materials availability

This study did not generate new unique reagents.

Data and code availability

- This paper does not report original code.
- Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

EXPERIMENTAL METHOD DETAILS

We manufactured the GaAs/p-Si structure using liquid phase epitaxial growth technology. First, we obtained P-type monocrystalline silicon substrates, each 300 μm thick, from Sigma-Aldrich. These substrates were cleaned with a dilute solution of hydrofluoric acid (10% acid to 90% water) to remove silicon dioxide from their surfaces. Gallium arsenide (GaAs) was then dissolved in an appropriate solvent, such as indium, to create a supersaturated GaAs solution within a boat designed for liquid phase epitaxy at approximately 900°C. The silicon substrate was then positioned under the supersaturated GaAs solution, and the temperature gradually decreased at a rate of 1°C per minute. As a result, a thin film of GaAs was deposited on the silicon substrate, forming the GaAs/p-Si structure.[43]