FM Transceiver for Wireless Communication

Audio and Intermediate Frequency Amplifiers

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Challenge the future

TU Delft

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FACULTY OF ELECTRICAL ENGINEERING, MATHEMATICS
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ELECTRICAL ENGINEERING PROGRAMME

Abstract

The goal of this bachelor graduation thesis is to design, simulate and create a prototype for a wireless FM transceiver system, making use of only basic electronic components: resistors, capacitors, inductors, diodes and transistors. This thesis describes the design process of three subsystems of the FM wireless transceiver system: a microphone amplifier, an intermediate frequency amplifier and a speaker amplifier. In order to make design decisions, study went into the functionality of the bipolar transistor and a variety of amplifier classes, which is described in this thesis. The three main designs and its sub-designs go through a number of design iterations in order to fulfill all requirements. Creating design schematics and simulations of the operation of the designs are done with the program *Advanced Design System (ADS)* of company Keysight. Designs are tested for waveform abnormalities, gain, bandwidth, total harmonic distortion (THD), input impedance, step responses and power when needed. The results show that almost all designs reach the design requirements, only the bandwidth of the speaker amplifier is short of the requirement. All designs show low THD for the bandwidth and the input signal voltage range of operation. Due to lack of time the prototype could not have been finished and be tested yet. However a plan has been made to create and test the prototype, which will be discussed in the defence of this thesis.

Preface

Over the last two months the six of us students have tried to build a FM transceiver from scratch using only the basic components. The design process and results are presented in this document as well as two other theses. The project did not only give us the opportunity to create an FM transceiver it also give us a much better understanding of some fundamental concepts in electrical engineering along with more experience in the design process. This is the reason why many of us were interested in the project. As the group responsible for designing the audio and intermediate frequency amplifiers we feel like the project was very valuable, since we feel like we gained a lot of knowledge and are happy with the results.

This project would never have been possible without the help of Marco Pelk, Masoud Babaie, and Morteza Alavi. Although they are very busy with their own work in the RF department of microelectronics at the TU Delft, their doors were always open if we needed help. Thank you for offering this project to us and helping us gain the most out of it. Furthermore we want to thank Ioan Lager for organizing the bachelor graduation project. We feel like the bachelor graduation project has been a highlight in our study and a valuable end to a challenging but interesting bachelor. We also want to the thank the rest of our group members: Ruben van Baarle, Gilbert Hardeman, Darshan Ramlal and Jasper van Vliet for being excellent team members and joining us in this last journey of the bachelor. Lastly we want to thank our friends and families for helping us completing the bachelor Electrical Engineering. We could not have done it without you.

Ivor Bas - Victor Hoedemaker, August 27, 2019, Delft

Contents

Chapter 1

Introduction

Sometimes the best way to learn and understand a new technology is to strip it down to the bones and start from the beginning. Nowadays the world is filled with highly advanced technologies, one of them being wireless radio frequency technology. To understand the principles, one should understand its building blocks. This is why this bachelor thesis project has been set up.

1.1 Project goal

The goal of this bachelor project is to understand and ultimately be able to design an FM transceiver using only the basic electronic building blocks: capacitors, inductors, resistors, diodes and transistors. Integrated circuits are not allowed in this project. The project is completed by a group of six people, split into subgroups of two. Each subgroup is responsible for their own part on the transmitter (TX) and receiver (RX) side of the transceiver system. Figure 1.1 shows an overview of the transceiver system.

The specifications goals of the FM transceiver are as follows.

- The operational frequency range should be from 88 MHz to 108 MHz.
- The transmission distance between RX and TX should be larger than 5 meters.
- Competitive efficiency for TX and decent sensitivity for RX should be achieved.

Some design specifications were agreed upon within the group. The DC power supply, connected to the entire system, is set to 12 V. This happened to be enough to reach sufficient gain in each design. Overall bipolar transistors were used rather than MOSFET transistors due to the low operating voltages of the MOSFET. An electret microphone is used as the input source for the system and an 8 Ohm speaker is used as the load. The system is made for audio transmission with a bandwidth of 20 Hz to 20 kHz. A lower bandwidth could have been chosen since at first only human voice audio will be transmitted, which has a lower bandwidth. However, designing the system for the full audible spectrum turned out to be as easy to design, since only the lower bandwidth limitation is a problem, and allows for full spectrum audio transmission in the future. To create design schematics and simulate the operation of the designs, the program *Advanced Design System (ADS)* of company Keysight was used. Schematics and simulations displayed in the thesis are also exported from this program.

1.2 Existing radio transceiver technology

Current FM transceivers utilize digital signal processing. Building upon the concept of digital processing, today's transceiver radio systems use relatively more advanced modulation techniques of frequency (and amplitude) modulation. Digital systems provide high reliability and a higher signal to noise ratio. An example of a digital implementation of frequency modulation would be frequency shift keying (FSK). This modulation type uses different frequencies, added to a carrier frequency, to represent discrete signal values

(bits) instead of continues values. Such a digital radio system would also involve analogue to digital and digital to analogue converters [1]. The FSK technique is attractive for short range communication between two or more ”digital” devices. For example in smart cities or applications of IoT [2].

Long range audio broadcasting FM and AM is being replaced by DAB+ (Digital Audio Broadcasting) [3]. This broadcasting type involves orthogonal frequency division multiplexing (OFDM) modulation. In OFDM the available bandwidth is split into multiple frequency bands to carry separate signals simultaneously over a single medium. The sub-carrier frequencies are orthogonal to each other, which means that interference between the multiple frequency bands is eliminated.

1.3 Thesis outline

This thesis will describe the design process and prototype development of the Microphone amplifier stage, which is the first stage of the TX, the Intermediate Frequency (IF) amplifier of the RX and the Speaker amplifier stage, which is the last stage of the RX. Study about the operation of bipolar transistors and amplifier classes has been done and is described in separate chapters. Each following chapter describes the characteristics of a main or sub design circuit, followed by the design steps and concluded by the simulation results of that circuit. Finally the entire circuit transceiver is shown. Due to lack of time, the prototype of the complete design will be constructed and tested after the completion of this thesis.

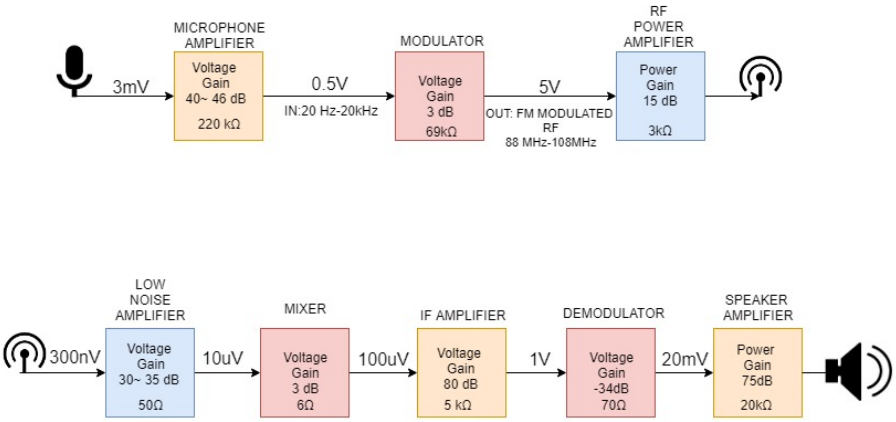

Figure 1.1: Block diagram of the transceiver system with signal levels, input impedances and gain indicated per block.

Chapter 2

Bipolar junction transistor

The Bipolar Junction Transistor (BJT) is a semiconductor device used for switching or amplifying a signal. The BJT is produced in two different types: the NPN type and the PNP type. The transistor type states the configuration of the doped semiconductor materials within the device, 'N' for negatively doped material (n-type) and 'P' for positively doped material (p-type). In figure 2.1 both types of BJT can be seen. The BJT has three terminals connected to each semiconductor type in the device: the base, the collector and the emitter. The current that flows into the collector terminal of the BJT, can be controlled by the voltage across the base and the emitter terminal of the BJT.

2.1 Working principle

Semiconductor materials are known for their non-linear voltage current ratio. This can be observed in a diode, a device with two doped material types connected, a p-type and n-type material. This creates a junction in the middle of the two material types. In figure 2.2 the ideal non-linear behaviour of a diode can be seen. This figure shows that in reversed biasing mode ($V_a < 0$), the reversed current through diode is exponentially dependent on forward-bias voltage V_a but at some point will reach the small reverse-saturation current represented by $-J_s$. When the diode is forward biased ($V_a > 0$), the diode current density J is an exponential function of the forward-bias voltage V_a. In reality the diode current reaches a cross-over point when the forward-voltage reaches the internal barrier potential of the diode. This barrier potential is also called the threshold voltage of the diode and is usually around 0.7 V for silicon transistors.

In a BJT there are three doped material types connected, either in NPN or PNP configuration as can be seen in figure 2.1. This creates two junctions in between the three material types, the base-emitter junction and the base-collector junction. Each can be forward or reverse biased. This principle allows for four operating regions for the BJT shown in figure 2.3.

When the base-emitter and the base-collector junctions are both reverse biased, the BJT operates in the Cuttoff region. In this operating mode all the currents in the BJT are zero.

When the base-emitter junction becomes forward biased, while the base-collector junction remains

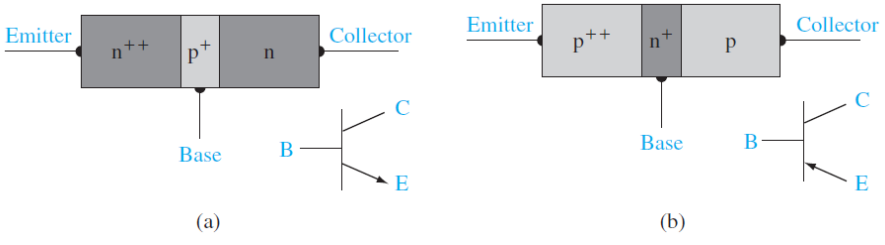

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Figure 2.1: Block diagrams and circuit symbols of (a) NPN and (b) PNP bipolar transistors. [4]

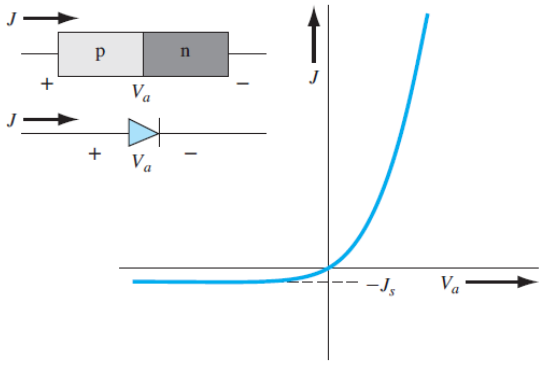

Figure 2.2: Ideal I-V characteristic of a PN junction diode. [4]

reverse biased, an emitter current will flow. The current flowing into the base results in a collector current. The BJT now operates in forward active mode.

When both the base-emitter and base-collector junctions are forward biased, the BJT operates in the Saturation region. In this operating mode the collector current is not controlled anymore by the base-emitter voltage.

The fourth operating mode of the BJT occurs when the base-emitter junction is reverse biased and the base-collector junction is forward biased. This is called the inverse active region. In this operating region the roles of the collector and emitter within the BJT are reversed. However because BJT devices are asymmetrical, the inverse active and forward active characteristics are not the same. [4].

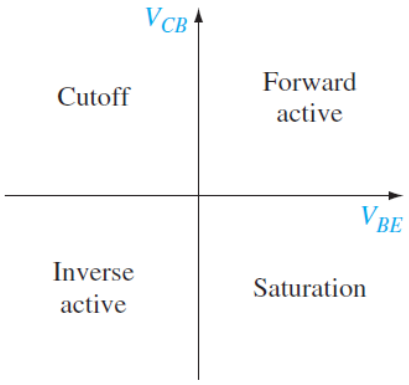

Figure 2.3: Four junction conditions for the four operating modes of a BJT. [4]

2.2 Models

In order to understand the behaviour of a BJT within a circuit, it can be replaced by an equivalent model. A lot of equivalent BJT models exist. One of them, the Hybrid-Pi model, being popular for it's functionality for low-frequency as well as high-frequency signal analysis. This model will be discussed and used for design analysis.

2.2.1 Hybrid-Pi model

The Hybrid-Pi model is a small-signal equivalent circuit used to analyze the amplification behaviour of a bipolar transistor, biased into the active region. Because it is a model used for BJTs that amplify time-

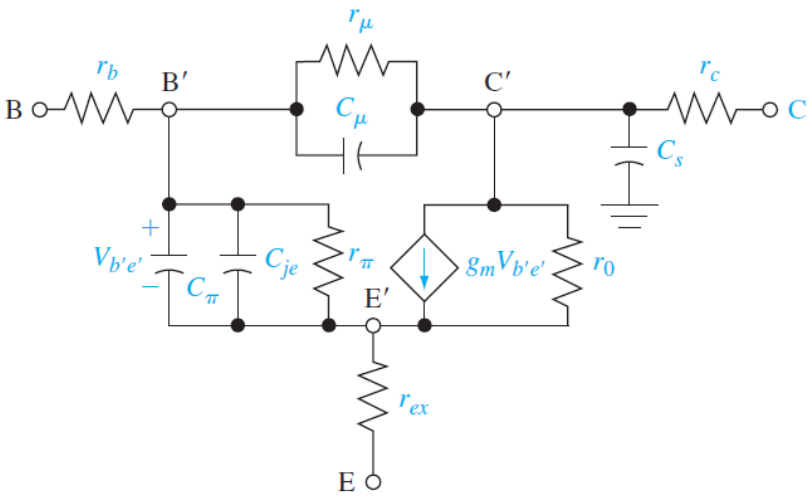

Figure 2.4: Hybrid-Pi equivalent circuit. [4]

varying signals, it takes into consideration the small-signal admittance parameters of the BJT device. In figure 2.4 the Hybrid-Pi equivalent circuit can be seen. The letters C, B and E note the external terminals of the BJT, while C', B' and E' point out the idealized internal collector, base and emitter regions. [4]

To start with r_b which is the series resistance between the external base terminal and the internal base region. The B'-E' junction is forward biased, therefore C_π is the junction diffusion capacitance and r_π is the junction diffusion resistance. These are in parallel with the junction capacitance C_{je}. The series resistance between the external emitter terminal and the internal emitter region is represented by r_{ex}.

The series resistance r_c is the resistance between the external collector terminal and the internal collector region and C_s represents the reverse-biased collector-substrate junction capacitance. The current source represents the voltage controlled collector current, controlled by the internal base-emitter voltage. The resistance r_0 represents the Early effect. [4]

The reverse-biased junction capacitance C_μ and reverse-biased junction resistance r_μ represent the equivalent circuit of the reverse-biased B'-C' junction. [4]

2.2.2 Simplified hybrid-pi model

To take into account all the parameters of the Hybrid-Pi equivalent circuit, usually a computer is needed to analyze a transistor design. In order to do hand calculations on transistor designs, a simplified version of the Hybrid-Pi equivalent circuit has been made shown in figure 2.5. This equivalent circuit only takes into account the most important factors of the complete Hybrid-Pi model and leaves out all extremely high or low value elements. In this thesis only for low frequency applications is designed so C_π is ignored, because of its high impedance. The resistance r_π is defined as follows:

$$r_\pi = \frac{\beta}{g_m} \tag{2.1}$$

With conductance g_m being defined as the DC collector current I_c divided by the thermal voltage V_T:

$$g_m = \frac{I_c}{V_T} \tag{2.2}$$

As shown in figure 2.5 the collector current I_c is set by the current source $g_m V_{be}$. This corresponds to the collector current I_c being equal to the base current I_b as shown in equation 2.3.

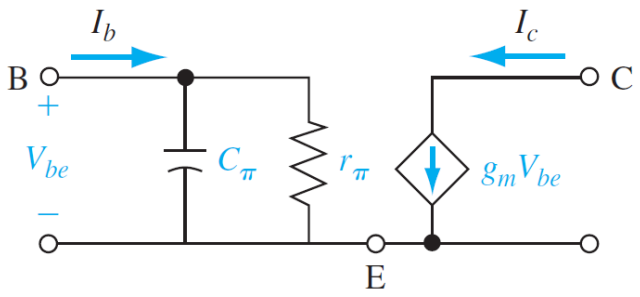

Figure 2.5: Simplified Hybrid-Pi equivalent circuit. [4]

$$\begin{aligned} I_c &= g_m V_{be} \\ &= g_m I_b r_\pi \\ I_c &= \beta I_b \end{aligned} \tag{2.3}$$

Emitter current I_e is equal to the sum of the base current I_b and the collector current I_c. In equation 2.4 is shown that because I_b is relatively low due to high current gain β, the emitter current I_e is approximately equal to the collector current I_c.

$$\begin{aligned} I_e &= I_b + I_c \\ &= \frac{1}{\beta} I_c + I_c \\ &= (\frac{1}{\beta} + 1) I_c \\ I_e &= \frac{\beta + 1}{\beta} I_c \\ I_e &\approx I_c \end{aligned} \tag{2.4}$$

2.3 Basic BJT configurations

The BJT is commonly used in three kind of single-stage configurations, each with there own properties. When designing a BJT circuit, one of these can be used as a starting point.

2.3.1 Common emitter

The common emitter amplifier configuration uses the base port as an input and the collector port as an output. The emitter is used as the common port and is connected to either the DC voltage supply or the ground. In figure 2.6 the common emitter setup can be seen. The common emitter configuration can be used as a voltage amplifier since it offers high voltage gain compared to the other configurations. The current gain is the BJT current gain β.

2.3.2 Common collector

The common collector amplifier configuration uses the base port as an input and the emitter port as an output. The collector is used as the common port and is connected to either the DC voltage supply or the ground. In figure 2.6 the common collector setup can be seen.

2.3.3 Common base

The common base amplifier configuration uses the emitter port as an input and the collector port as an output. The base is used as the common port and is connected to either the DC voltage supply or the ground. In figure 2.6 the common base setup can be seen.

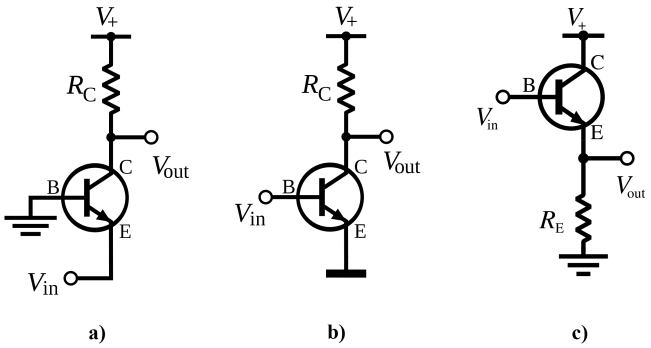

Figure 2.6: Circuit diagrams of (a) common base, (b) common emitter and (c) common collector configurations. (This vector image was created with Inkscape by userOmegatron.This W3C-unspecified circuit diagram was created with the Electrical Symbols LibraryThis vector image was created with Inkscape, andthenmanuallyreplaced., CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=2802630)

	Common emitter	**Common collector**	**Common base**
Voltage gain	$-g_m R_c$	1	$g_m R_c$
Current gain	β	β	1
Input impedance	r_π	βR_e	$\frac{1}{g_m}$
Output impedance	R_c	$\frac{1}{g_m}$	R_c

Table 2.1: Basic properties of common emitter, common collector and common base topologies.

2.4 Transistor biasing

Depending on the application, it can be useful for the BJT to be operating in a point within the Active region. This operating point or quiescent point (Q-point) can be set by biasing the BJT with a biasing network. By putting a constant base-emitter and collector-emitter voltage that is above the threshold values on the BJT, it can be ensured to always operate in the Active region, as long as the signal voltage superimposed on the constant voltage does not go below the threshold values. The disadvantage of biasing is that the BJT is always conducting and therefore always dissipating energy, even when no input signal is present. There are several ways to create a bias network. Five of them will be discussed here. An NPN common emitter BJT configuration is used to explain the different kinds of biasing.

2.4.1 Fixed base biasing

Fixed Base biasing is done by using a resistor Rb between the supply voltage rail and the base of the BJT. The DC current I_b through the resistor R_b, will remain constant given a constant supply voltage. A constant current I_b results in a fixed Q-point. However this way of biasing is dependent on the DC current gain β of the BJT. Because β is different for every BJT and also sensitive to the temperature of the device, it makes this way of biasing less robust.

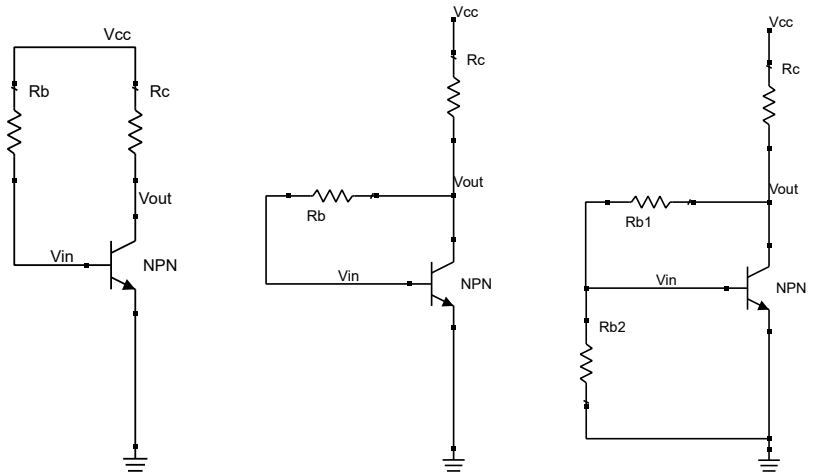

Figure 2.7: Fixed base (left), collector feedback (middle) and dual feedback (right) BJT biasing.

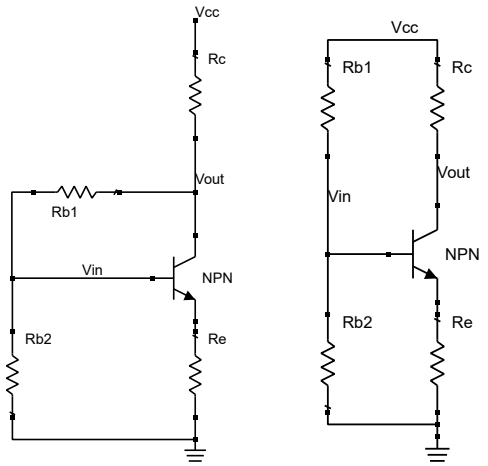

Figure 2.8: Emitter feedback (left) and voltage divider (right) BJT biasing.

2.4.2 Collector feedback biasing

Collector feedback biasing is done by connecting a resistor Rb between the collector and the base of the BJT. The voltage across the feedback resistor Rb determines the bias DC current I_b into the base of the BJT. When the collector current I_c now for example becomes larger, the collector voltage V_c becomes smaller, decreasing the voltage across the feedback resistor R_b, decreasing the bias current I_b, resulting in a smaller I_c. Because of the feedback, I_c is kept stable resulting in a stable Q-point. However when using this feedback bias network, an unstable DC current gain β will still result in an unstable Q-point.

2.4.3 Dual feedback biasing

Dual Feedback biasing is done by adding another resistor R_{b2} to the collector feedback network. This resistor R_{b2} is connected between the BJT base and the ground.

2.4.4 Emitter feedback biasing

Emitter feedback can be added to the previously mentioned feedback network by adding the feedback resistor Re. The feedback resistor R_e is connected between the emitter of the BJT and ground. When collector current I_c increases, the emitter current I_e increases, raising the emitter voltage V_e, thereby lowering the

base to emitter voltage drop, which decreases base current I_b, resulting in a decrease of I_c. In this setup the Q-point is stabilized by both R_e and R_{b1}.

2.4.5 Voltage divider biasing

With voltage divider biasing the BJT is biased by using a voltage divider network at the base. This biasing method provides high stability by independence of current gain β. Feedback resistor Re is added for extra stability of the Q-point.

2.5 BJT topologies

To create a higher current gain in a circuit several transistor stages can be used. In this section an overview of two very common transistor topologies will be given the Darlington ad Sziklai transistor, which are very common typologies in amplifier circuits [5]. More advanced topologies can further improve efficiency [6]. In this paper a three stage transistor topology is used to increase efficiency at a cost of extra total harmonic distortion.

2.5.1 Darlington transistor

The Darlington transistor consists of two transistors of the same type. For a NPN Darlington transistor two NPN transistors. The topology of a NPN Darlington transistor can be seen in figure 2.9, the PNP Darlington transistor can be seen in figure 2.10. A typical current response can be seen in 2.11.

Since the base current and the collector current of the first transistor is fed to the base of the second transistor the total current gain is very large.

$$\beta_{Darlington} = \beta_{Q1}\beta_{Q2} + \beta_{Q1} + \beta_{Q2} \tag{2.5}$$

BJTs have parasitic capacitances between each junction. In the Darlington or Sziklai transistor an emitter and base are connected to each other. The high input impedances of each transistor create a RC circuit with a high time constant, τ. The slow discharge time will extend the turnoff time of the Darlington transistor. For a higher frequency this can become a problem and would affect efficiency. To ensure a fast discharge time of the RC circuit and thus turnoff time of the BJT a resistor can be added to create a lower time constant. A downside to the Darlington transistor is that the transistor needs a biasing of 2 V_{be} from base to emitter.

$$\begin{aligned} V_c &= V_s \cdot e^{\frac{-t}{RC}} \\ \tau &= R \cdot C \end{aligned} \tag{2.6}$$

2.5.2 Sziklai transistor

The Sziklai transistor consists of two different transistors. For the NPN Sziklai transistor, seen in figure 2.12, a NPN transistor drives a PNP transistor and for the PNP Sziklai transistor, seen in figure 2.13, a PNP transistor drives a NPN transistor. A typical current response can be seen in 2.14. Since the base current of the first transistor is not fed to the base of the second transistor the overall current gain is a bit lower than the Darlington configuration. However a benefit of the Sziklai transistor is that both stages use a PNP and NPN transistor causing a more equal gain for both topologies when the β of the NPN differs from the β of the PNP. Another benefit is the biasing. A biasing voltage between the emitter and base of one V_{be} is needed. The collector emitter voltage drop is the same as in the Darlington configuration since there are still two transistors that need to be turned on.

$$\beta_{Sziklai} = \beta_{Q1}\beta_{Q2} + \beta_{Q1} \tag{2.7}$$

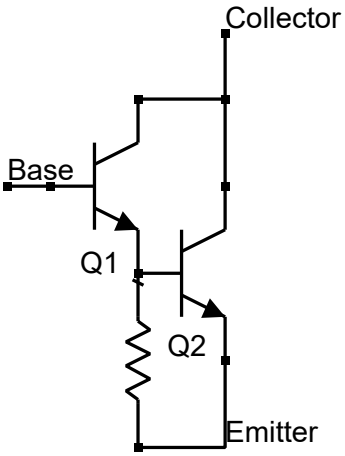

Figure 2.9: Circuit diagrams of a NPN Darlington transistor

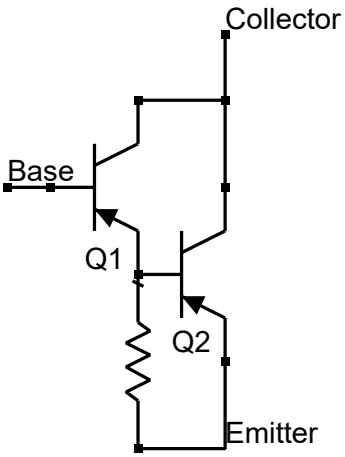

Figure 2.10: Circuit diagrams of a PNP Darlington transistor

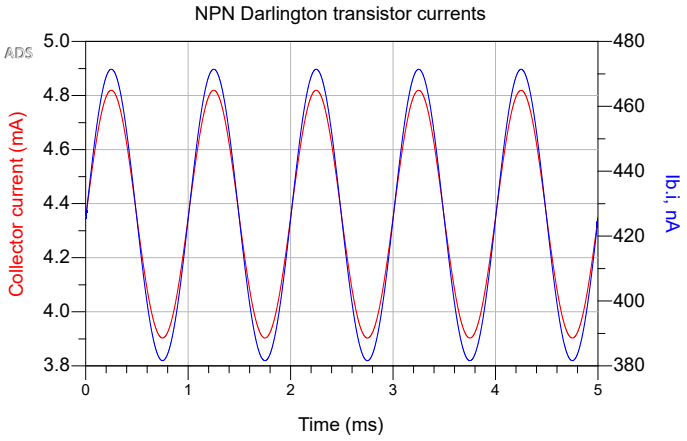

Figure 2.11: Typical currents of a NPN Darlington transistor

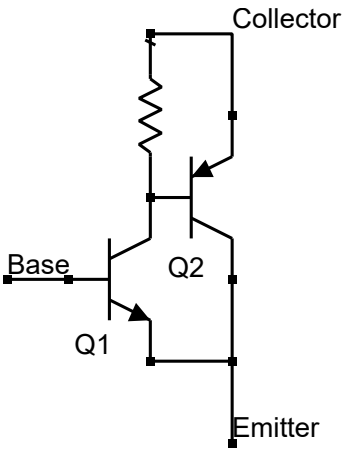

Figure 2.12: Circuit diagrams of a NPN Sziklai transistor

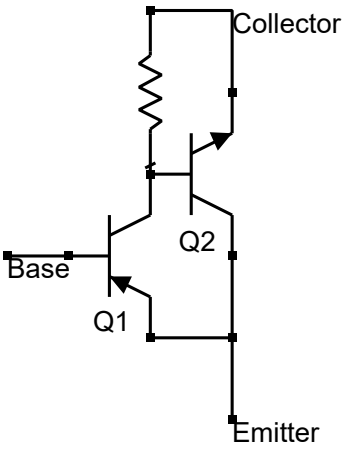

Figure 2.13: Circuit diagrams of a PNP Sziklai transistor

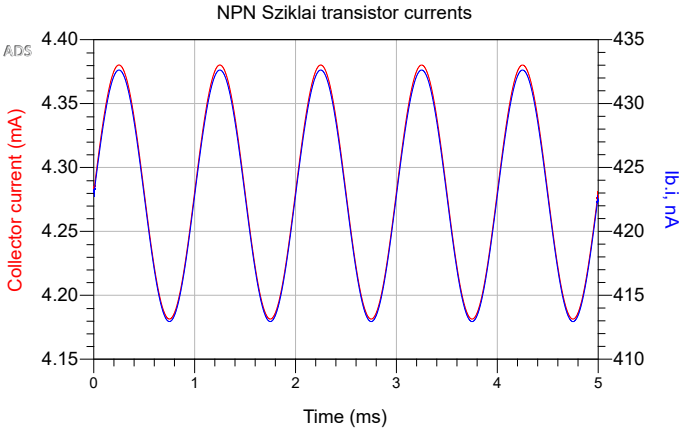

Figure 2.14: Typical currents of a NPN Sziklai transistor

Chapter 3

Amplifier classes

Because the BJT can be implemented in many different configurations and operating modes to create an amplifier, multiple amplifier classes are defined. Each of these classes excel in either gain, linearity, power efficiency or frequency dependency. It is therefore wise to pick the right class when designing a certain amplifier. This chapter will discuss the amplifier classes that are relevant for designing the Microphone Amplifier, IF Amplifier and Speaker Amplifier. In table 3.1 an overview of the classes can be seen.

3.1 Class-A

A class-A amplifier is an implementation of the common emitter configuration. The transistor is biased in order to amplify the whole range of the input signal. If the transistor is not biased, the signal will not be amplified if it falls below the threshold voltage of the transistor. This amplifier design is simple and has a linear amplification but the efficiency is low because the transistor is always conducting, even when there is no source signal.

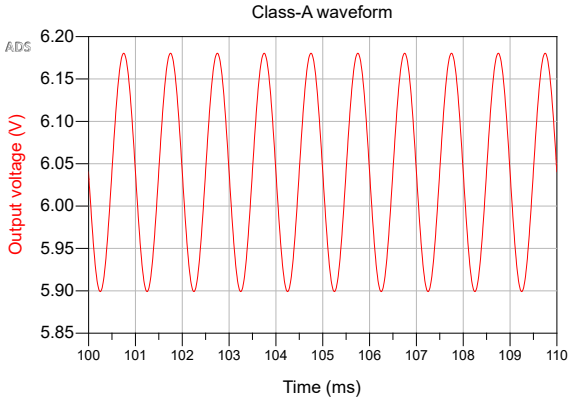

Figure 3.1: Class-A amplifier waveform

New techniques have been found to improve the efficiency of the class-A amplifier. One of them is a new circuit model to guide the design of a class-A amplifier by accurately estimating the optimum load resistance [7]. Finding the optimum load resistance ensures that a maximum power output can be achieved.

Another way to improve the efficiency is to power the amplifier with alternative supplies instead of the usual linear power supply. One study describes using a flyback DC-DC converter to power a class-A audio tube amplifier [8]. However using this alternative flyback power supply only showed a 2.5 % efficiency improvement and similar noise levels as the linear power supply.

Another topology uses a triple transistor configuration for small signal amplification [9]. Having a tunable frequency response in the audible spectrum, makes the circuit suitable for radio applications. It can

be used as a preamplifier stage providing amplified output for a 1uV - 10mV range of AC input signal with a frequency range of 41Hz - 250KHz with significantly low total harmonic distortion (THD).

3.2 Class-B

To improve the efficiency of a class-A amplifier, a topology with two transistors can be used, one amplifies the positive part of the signal and the other amplifies the negative part of the signal. This is called a class-B or push-pull amplifier. Because the transistors are switched off half of the time, the efficiency is improved. With a class-B amplifier the input signal is amplified with a lot of distortion. This is due to the face that the transistors have a certain threshold voltage they need between the base and emitter in order to conduct current. The part of the signal around 0V will therefor not be amplified. This type of distortion is called crossover distortion.

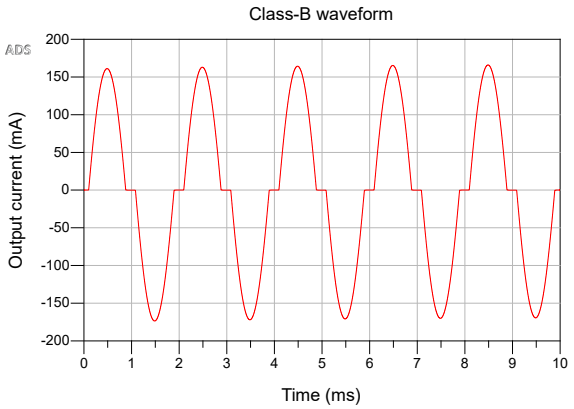

Figure 3.2: Class-B amplifier waveform

3.3 Class-AB

The B class amplifier can be improved by always applying the threshold voltage to the base of both transistors. If the two transistors in a class-B amplifier are biased it's called a class-AB amplifier. The class-AB amplifier is more efficient than a class-A but has less distortion than a class-B. If the biasing is done correctly the distortion zone is eliminated. In practice there will still be some crossover distortion because of non perfect biasing. Another problem can arise with the class-B and class-AB amplifiers. If the transistors or other components of the complementary circuits are not exactly the same, the negative and positive part of the source signal will not be amplified in the same way, creating more distortion.

3.4 Class-C

A class-C amplifier is an amplifier with a class-A topology but only conducts for half of the duty cycle. This creates a lot of distortion in the form of harmonics but keeps the frequency of the signal intact. Therefore it can be used in RF transmitters.

3.5 Class-D

In a class-D amplifier the transistors are used as switches instead of linear amplifiers. This causes the analogue signal to be converted into pulses that represent the original signal with some form of modulation. The main advantage of class-D amplifiers is the power efficiency. Because the transistors are used as

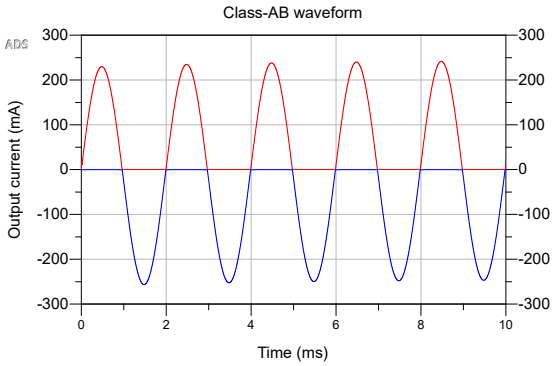

Figure 3.3: Class-AB amplifier waveform

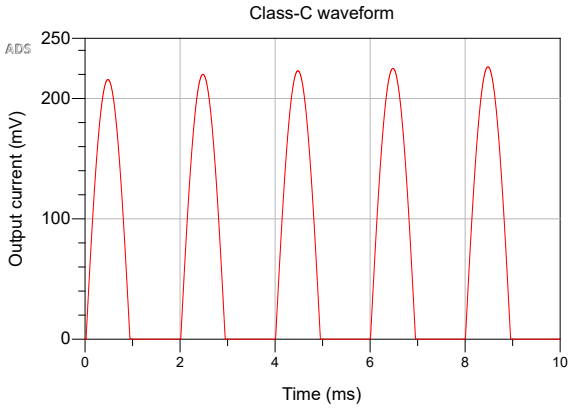

Figure 3.4: Class-C amplifier waveform

switches, they can always operate in the lowest resistance mode. Another benefit of the class-D amplifier is that it can amplify a digital signal directly.

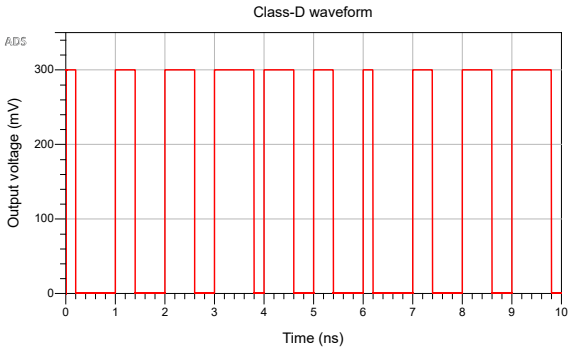

Figure 3.5: Class-D amplifier waveform

3.6 Class-XD

Cambridge Audio recently developed a new class of audio amplifiers: the XD class [10]. It tries to combine the power efficiency from a class-AB with the linearity of a class-A amplifier. It adds a voltage to the bias of the class-AB design. Doing so allows the crossover point of the amplifier to be shifted to a point where

the audio distortion is not audible to the human ear. Making it more efficient than a class-A amplifier with lower distortion than a class-AB amplifier.

3.7 Overview

In table 3.1 an overview of the discussed amplifiers can be seen. The table assumes a properly designed amplifier, if not properly biased and designed every amplifier can become very power inefficient and can add a lot of distortion.

Amplifier Class	**Signal Distortion**	**Power Efficiency**
A	Small, higher for a large output signal	Low
B	High crossover distortion	Medium
AB	Small crossover distortion	Medium
C	very high, adds harmonics	High
D	Distortion due to timing errors and switching capability	Very high
XD	Small crossover distortion at an inaudible point	Medium

Table 3.1: Overview of the discussed amplifier classes

Chapter 4

Voltage buffer

A voltage buffer is a circuit that recreates the voltage that is set on the input of the circuit, at the output of the circuit. By doing so it creates a voltage transfer independency between the previous and the next stage. A BJT transistor version of such a circuit is called an emitter follower or a common collector circuit, on which the input is fed to the base and the output is taken from the emitter. The collector is common and is therefore hooked up to the DC supply voltage or ground. Ideal characteristics of an emitter follower are high input impedance and low output impedance.

The Microphone Amplifier (Chapter 5) and Intermediate Frequency Amplifier (Chapter 6) stages are used to create a large signal gain. The signal gain of these stages are dependent on the source and load impedances. Ideally the source impedance should be zero and the load impedance infinite, creating maximum gain. If this is not the case a voltage buffer can be added to the input or output of the amplifier stage to create these ideal source or load impedances.

4.1 Design requirements

The following design requirements were set for the voltage buffer.

- Bandwidth of 20 Hz to 20 kHz
- Steady voltage gain of 1 (0 dB) over a the set bandwidth
- Steady voltage gain of 1 (0 dB) over a high voltage range
- High input impedance
- Low output impedance

The voltage buffer should recreate the voltage at the input to the output, without distortion. Therefore with a DC supply voltage of 12 volt, a voltage of 6 volt is desired at the emitter to optimize for maximum output swing and prevent clipping if possible. The collector current should be high enough for the BJT to provide a high current gain β but low enough to prevent unnecessary power dissipation.

4.2 Topology

As mentioned before, a common collector BJT topology is used for designing the voltage buffer. In chapter 2.1 is shown that the common collector topology has an input to output voltage gain of 1 which is ideal for a voltage buffer. To bias the voltage buffer a fixed base biasing is used, discussed in chapter 2. Although this is not the most robust way of biasing, it results in a higher input impedance of the voltage buffer, as will be used later to make assumptions. A higher input impedance is preferred because the voltage buffer will be less dependent on the source resistance as will be shown later. In figure 4.1 the circuit topology can be seen.

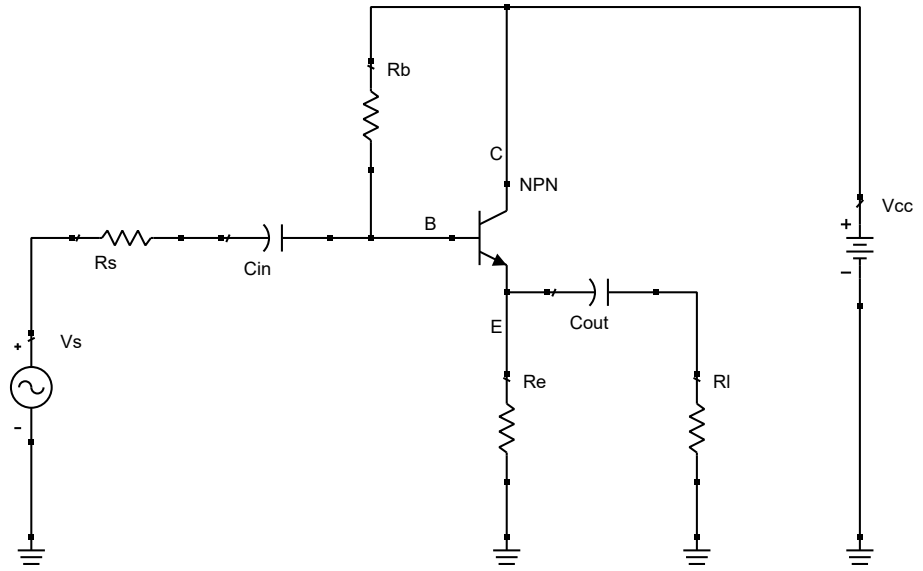

Figure 4.1: Circuit diagram of the voltage buffer.

4.3 Analysis

In order to design the voltage buffer circuit, the circuit has to be analyzed for large signal behaviour concerning the biasing network and small signal behaviour for calculating input impedance, output impedance and voltage gain.

4.3.1 Biasing network

In figure 4.2 a large signal DC analysis of the buffer is shown. For this DC analysis all capacitors are seen as open circuits. By applying Kirchhoff's voltage law, the DC supply voltage can be set equal to the voltage drop across the bias resistor R_b, plus the base-emitter voltage, plus the voltage drop across the emitter resistor R_e. Because the buffer has to be optimized for maximum voltage swing, the emitter voltage can be set to half the DC supply voltage. Now the only unknown variable in the equation is the voltage across the bias resistor R_b.

$$\begin{aligned} V_{cc} &= V_{R_b} + V_{be} + V_{Re} \\ V_{cc} &= V_{R_b} + V_{be} + V_e \\ V_{R_b} &= V_{cc} - V_{be} - V_e \end{aligned} \tag{4.1}$$

The DC collector current should be high enough to allow for the AC current swing on the input and high enough to get a significantly high current gain. However a large collector current will result in high power dissipation within the transistor. An optimum can be derived using the transistor datasheet. From equation 2.4 the emitter current can be calculated from the collector current and the DC current gain of the transistor. Knowing the emitter current and the emitter voltage, the emitter resistor R_e can be calculated.

$$\begin{aligned} R_e &= \frac{V_e}{I_e} \\ R_e &= \frac{\frac{V_{cc}}{2}}{(\frac{\beta+1}{\beta})I_c} \end{aligned} \tag{4.2}$$

Using equation 2.3 the base current can be calculated from the collector current and the DC current

gain. Knowing the base current and the voltage across resistor R_b from equation 4.1, the bias resistor R_b can be calculated.

$$\begin{aligned} R_b &= \frac{V_{R_b}}{I_b} \\ R_b &= \frac{V_{cc} - V_{be} - V_e}{(\frac{1}{\beta})I_c} \end{aligned} \tag{4.3}$$

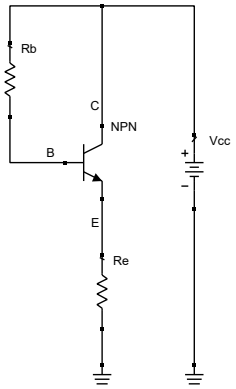

Figure 4.2: Circuit diagram used for large signal analysis of the voltage buffer.

4.3.2 Input and output impedance

From the AC small signal analysis of the circuit which is shown in figure 4.3, the input and output impedance of the circuit can be derived.

The input impedance, as seen from the source voltage and source resistance into the circuit, is equal to the equivalent resistance of the base resistance R_b parallel to the resistance seen from the base terminal into the circuit. This includes r_π and the equivalent resistance of R_e parallel to R_l. Because the currents i_b through r_π and i_e through $R_e//R_l$ are not the same, these resistances cannot be seen as series resistances. In order to do so, the voltage over resistance $R_e//R_l$ has to be written as a function of i_b, rather than i_e. This results in a transformed resistance which is in series with r_π. The transformed resistance R_{t1} is calculated in equation 4.4.

$$\begin{aligned} v_{out} &= i_e(R_e//R_l)) \\ &= (i_c + i_b)(R_e//R_l)) \\ &= i_b(\beta+1)(R_e//R_l)) \\ R_{t1} &= \frac{v_{out}}{i_b} = (\beta+1)(R_e//R_l) \end{aligned} \tag{4.4}$$

Next the input impedance can be calculated as can be seen in equation 4.5. Assuming β is very high so $(\beta+1) \approx \beta$, $(R_e//R_l) >> \frac{1}{g_m}$ and $R_b >> \beta(R_e//R_l)$.

$$\begin{aligned} Z_{in} &= R_b//(r_\pi + R_{t1}) \\ &= R_b//(r_\pi + (\beta+1)(R_e//R_l)) \\ &= R_b//(\frac{\beta}{g_m} + (\beta+1)(R_e//R_l)) \\ &\approx R_b//(\frac{\beta}{g_m} + \beta(R_e//R_l)) \\ &\approx R_b//\beta(\frac{1}{g_m} + (R_e//R_l)) \\ &\approx R_b//\beta(R_e//R_l) \\ Z_{in} &\approx \beta(R_e//R_l) \end{aligned} \tag{4.5}$$

The output impedance, as seen from the load resistance R_l into the circuit, can be seen as the equivalent resistance of the emitter resistance R_e parallel to the resistance left of the emitter terminal. The latter can be derived by writing the voltage across these resistances as a function of i_e instead of i_b, as done reversed earlier with the input impedance. An equation for the transformed resistance R_{t2} can be derived as shown in equation 4.6.

$$\begin{aligned} v_{in} &= i_b(R_s + r_\pi) \\ &= \frac{i_e}{\beta+1}(R_s + r_\pi) \\ R_{t2} &= \frac{v_{in}}{i_e} = \frac{R_s + r_\pi}{\beta+1} \end{aligned} \tag{4.6}$$

Next in order to derive the output impedance it is again assumed that β is high so that $(beta + 1) = \beta$. Also it is assumed that the base resistance $R_b >> R_s$ and $R_b >> r_\pi$. The base resistance R_b can thus be seen as an open circuit, as very little current will flow into it. The derivation of the output impedance can be seen in 4.7.

$$\begin{aligned} Z_{out} &= R_e//R_{t2} \\ &\approx R_e//(\frac{R_s + r_\pi}{\beta}) \\ &\approx R_e//(\frac{R_s + \frac{\beta}{g_m}}{\beta}) \\ &\approx R_e//(\frac{R_s}{\beta} + \frac{1}{g_m}) \\ Z_{out} &\approx \frac{R_s}{\beta} + \frac{1}{g_m} \end{aligned} \tag{4.7}$$

4.3.3 Voltage gain

The voltage gain of the buffer can also be derived from the small signal analysis of figure 4.3. The output voltage is equal to a voltage drop of the input voltage over the resistances $R_e//R_l$ and the transformed resistance R_{t2}, derived earlier in equation 4.6. From this the voltage gain can be derived as can be seen in equation 4.8. It is assumed that $(\beta+1)(R_e//R_l) >> (R_s + r_\pi)$. It can be seen that the voltage gain is approximately unity, as would be expected.

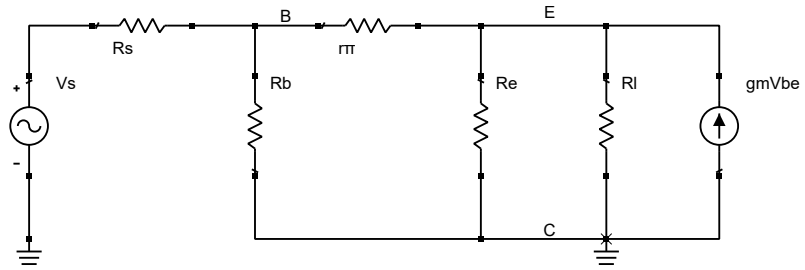

Figure 4.3: Circuit diagram used for small signal analysis of the voltage buffer.

$$
\begin{aligned}
v_{out} = v_{ec} &= v_s \frac{(R_e//R_l)}{R_{t2} + (R_e//R_l)} \\
A_v = \frac{v_{out}}{v_s} &= \frac{(R_e//R_l)}{\frac{R_s + r_\pi}{\beta+1} + (R_e//R_l)} \\
&= \frac{(\beta+1)(R_e//R_l)}{(R_s + r_\pi) + (\beta+1)(R_e//R_l)} \\
A_v &\approx \frac{(\beta+1)(R_e//R_l)}{(\beta+1)(R_e//R_l)} = 1
\end{aligned}
\tag{4.8}
$$

4.4 Component choice

The voltage buffer circuit has been designed with an 2n3904 NPN BJT. It is connected to a V_{cc} of 12 V. The emitter voltage of the circuit is set to 6 V, which is half the V_{cc}, to allow for maximum signal swing. A collector current of 1 mA has been chosen to allow for high current gain and low power dissipation. Using these values, the values for resistors R_e (equation 4.2) and R_b (equation 4.3) can be calculated. Table 4.4 gives an overview of all the buffer components.

Component	**Value**
Vs (amplitude, frequency)	1 V, 1 kHz
Rs	50 Ω
Cin	100 uF
Cout	100 uF
NPN	2n3904
Rb	620 kΩ
Re	6 kΩ
Rl	10 kΩ
Vcc	12 V

Table 4.1: Component list of the Voltage buffer.

Chapter 5

Microphone amplifier

The Microphone Amplifier is the first stage in the TX and amplifies the audio signal coming from a microphone. This is a small amplitude signal which is why the microphone amplifier needs significant voltage gain. The microphone amplifier should add low to no distortion to the signal. Distortion directly effects the quality of the sound and because it is the first stage in a signal chain, any distortion will be amplified further on in the signal chain, decreasing the signal to noise ratio. As described in the introduction (Chapter 1), an electret microphone is used as an input source.

5.1 Design requirements

For designing the microphone amplifier, the following requirements were set.

- Bandwidth of 20 Hz to 20 kHz
- Steady voltage gain of at least 100 (40 dB) over the set bandwidth
- Steady voltage gain of at least 100 (40 dB) for low voltage inputs
- Adjustable voltage gain
- Be able to handle a source impedance of 2.2 kΩ
- Be able to drive a load impedance of 20 kΩ

The microphone amplifier should be able to produce a high voltage gain of at least 100 and should add as little distortion as possible to the input signal when amplifying. The gain should be adjustable to be able to tune to the maximum output value of the microphone without letting the signal clip. The amplifier should be able to handle the high source impedance of the microphone and a high load impedance, which is the input impedance of the Modulator stage.

5.2 Topology

Because low distortion is crucial for this stage, using table 3.1 the amplifier is chosen to be a class-A amplifier. This means the amplifier needs a biasing network so it is always operating in forward active mode. The microphone amplifier should act as a voltage amplifier. As shown in chapter 2, a common emitter topology is the best option to start designing a voltage amplifier. From the analysis of the common emitter topology in chapter 2 can be seen that the gain of the system is directly controlled by the value of resistance R_c. However increasing the resistance R_c, also increases the voltage drop over resistor R_c, decreasing the potential swing of the output signal. The biasing circuit of the amplifier was chosen to be a voltage divider biasing using an emitter feedback resistor for extra stability of the Q-point. In figure 5.1 the topology of the class-A amplifier as a microphone amplifier can be seen.

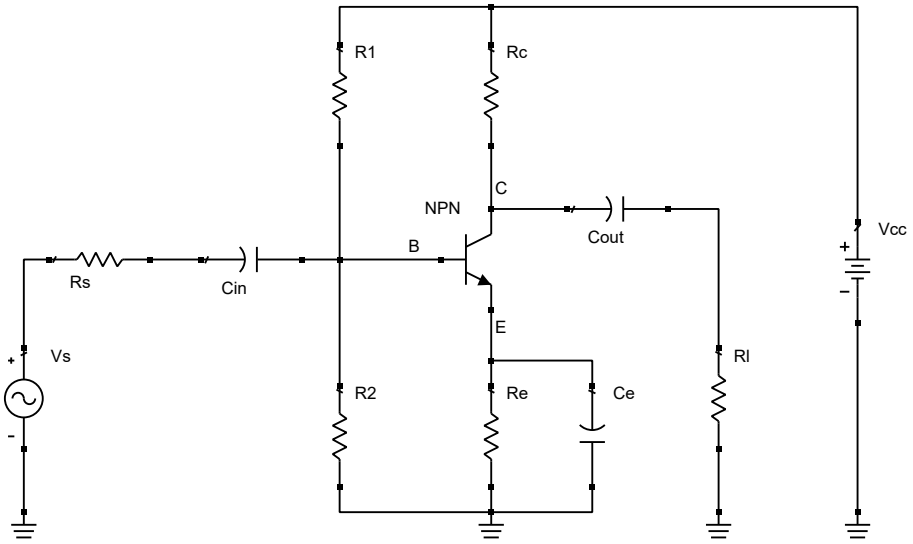

Figure 5.1: Circuit diagram of the microphone amplifier.

5.3 Analysis

In order to design the microphone amplifier circuit, it has to be analyzed for large signal behaviour concerning the biasing network and small signal behaviour for calculating input impedance, output impedance and voltage gain.

5.3.1 Biasing network

Figure 5.2 shows the DC large signal analysis of the microphone amplifier. All capacitors are considered as DC open circuits.

As said before an emitter feedback resistor is used to increase stability of the Q-point as described in chapter 2. In order to compensate these potential instabilities, there should be a certain voltage across the resistor R_e. Making this voltage too large will decrease the potential voltage swing at the output. However making the voltage across R_e too small will decrease the stabilizing effect of the resistor. For this design it is therefore said to be ten percent of the DC supply voltage. Dividing this voltage over the emitter current, which is approximately the chosen collector current, gives then the value for R_e.

$$\begin{aligned} V_{R_e} &= V_e = \frac{1}{10} V_{cc} \\ R_e &= \frac{V_{cc}}{10 I_e} \\ R_e &\approx \frac{V_{cc}}{10 I_c} \end{aligned} \tag{5.1}$$

To make resistors R_1 and R_2 work as a voltage divider, as much DC current as possible flowing through R_1 should also flow through R_2. It should therefore be prevented that too much current flows into the base of the BJT. This can be done by analyzing the voltage over resistor R_e as a function of the base current I_b instead of the emitter current I_e. By doing this an equivalent resistor of R_e can be derived which stands in parallel with resistor R_2. The derivation can be seen in equation 5.2. Now by stating that less then ten percent of the current flowing through resistor R_1 should flow into the base of the BJT, it can be said that resistor R_2 should be less then ten percent of the equivalent resistance of R_e. This gives the expression for resistor R_2 as shown in 5.3.

$$\begin{aligned} V_{R_e} &= I_e R_e \\ V_{R_e} &= (\beta + 1) I_b R_e \\ R_{e,eq} &= \frac{V_{R_e}}{I_b} \approx \beta R_e \end{aligned} \tag{5.2}$$

$$\begin{aligned} R_2 &= \frac{1}{10} R_{e,eq} \\ R_2 &= \frac{\beta}{10} R_e \end{aligned} \tag{5.3}$$

Using Kirchhoff's voltage law, the voltage at the base can be set equal to the voltage across resistor R_e plus the base-emitter forward voltage of the BJT. The voltage divider network at the base of the BJT, consisting of resistors R_1 and R_2, should then create this voltage at the base of the BJT. Knowing the value for resistor R_2, an expression for resistor R_1 can be made as can be seen in equation 5.4.

$$\begin{aligned} V_b &= V_{R_e} + V_{be} = V_e + V_{be} \\ \frac{R_1}{R_1} &= \frac{V_{R_1}}{V_{R_2}} = \frac{V_{cc} - V_b}{V_b} \\ R_1 &= \frac{V_{cc} - V_b}{V_b} R_2 \\ R_1 &= \frac{V_{cc} - (V_e + V_{be})}{(V_e + V_{be)}} R_2 \\ R_1 &= \frac{0.9 V_{cc} - V_{be}}{0.1 V_{cc} + V_{be}} R_2 \end{aligned} \tag{5.4}$$

The collector resistor R_c can be used to set the DC voltage offset at the output of the amplifier. However as will be shown later, resistor R_c also determines the gain of the amplifier. This is why it is chosen for R_c to be variable to be able to optimize between these characteristics. However if maximum output voltage swing is desired, Kirchhoff's voltage law can be used to set the voltage over resistor R_c, plus the collector-emitter voltage of the BJT, plus the voltage across resistor R_e to be equal to the DC supply voltage as can be seen in equation 5.5. The voltage across resistor R_e can be taken from equation 5.1. The collector-emitter voltage should be at least the collector-emitter saturation voltage as indicated in the datasheet of the BJT, for the BJT to operate in the forward active region. To optimize for maximum output voltage swing, the output voltage V_c should be half of the available voltage in the loop. Given the chosen collector current I_c, an equation can now be derived for resistor R_c.

$$\begin{aligned} V_{cc} &= V_{R_c} + V_{ce} + V_{R_e} \\ V_{R_c} &= V_{cc} - V_{ce} - 0.1 V_{cc} \\ V_{R_c} &= 0.9 V_{cc} - V_{ce} \\ R_c &= \frac{V_{R_c}}{2 I_c} \\ R_c &= \frac{0.9 V_{cc} - V_{ce}}{2 I_c} \end{aligned} \tag{5.5}$$

5.3.2 Voltage gain

Figure 5.3 shows the AC small signal analysis of the microphone amplifier. All capacitors are seen as AC short circuits. From this analysis circuit, the input (V_s) to output (V_{ce}) voltage gain is derived as can be seen in equation 5.6.

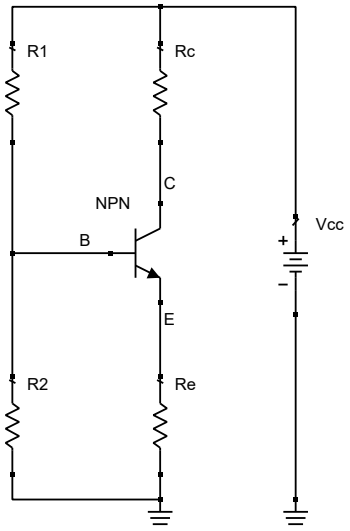

Figure 5.2: Circuit diagram used for large signal analysis of the microphone amplifier.

$$
\begin{aligned}
v_{out} = v_{ce} &= -g_m v_{be}(R_c//R_l) \\
v_{be} &= \frac{R_1//R_2//r_\pi}{R_s + R_1//R_2//r_\pi} v_s \\
A_v = \frac{v_{out}}{v_s} &= -g_m \frac{R_1//R_2//r_\pi}{R_s + R_1//R_2//r_\pi}(R_c//R_l) \\
A_v &= -\frac{I_c}{V_T}\frac{R_1//R_2//r_\pi}{R_s + R_1//R_2//r_\pi}(R_c//R_l) \\
A_v &= -\frac{I_c}{V_T}\frac{1}{R_s(\frac{R_1 r_\pi + R_2 r_\pi + R_1 R_2}{R_1 R_2 r_\pi}) + 1}\frac{R_c R_l}{R_c + R_l}
\end{aligned}
\tag{5.6}
$$

From the voltage gain derivation of equation 5.6, three design flaws can be noticed. The first one is that the voltage attenuates highly when the source resistance is relatively high compared with the parallel resistors between base and emitter. The second flaw is that the gain can only be controlled by resistor R_c if the load resistance is much higher than the resistance of R_c. The third is that the voltage gain depends on the collector current I_c. If the AC fluctuation superimposed on the DC current I_c fluctuates too much, the voltage gain will fluctuate, therefore the amplifier will not amplify linearly. The last flaw is only an issue when the signal source creates these relatively high current fluctuations. When the input voltage amplitude is relatively low, the amplifier amplifies linearly. The first two flaws indicate that the class-A amplifier demands the source resistance to be as low as possible and the load resistance to be as large as possible.

5.3.3 Improved design

To improve the previous design's dependency on the source and load resistance, an improved design has been made using voltage buffers. The voltage buffer, as described in chapter 4, has a very low output impedance which would be an ideal source resistance for the class-A amplifier. Also the voltage buffer has a very high input impedance which would be an ideal load resistance for the class-A amplifier. So by connecting a voltage buffer to the the input and another one to the output of the class-A amplifier, it eliminates the gain attenuation by the source and load resistances and the amplifier gain becomes a function of only the resistance R_c as can be seen in equation 5.7. The improved circuit topology can be seen in figure 5.4.

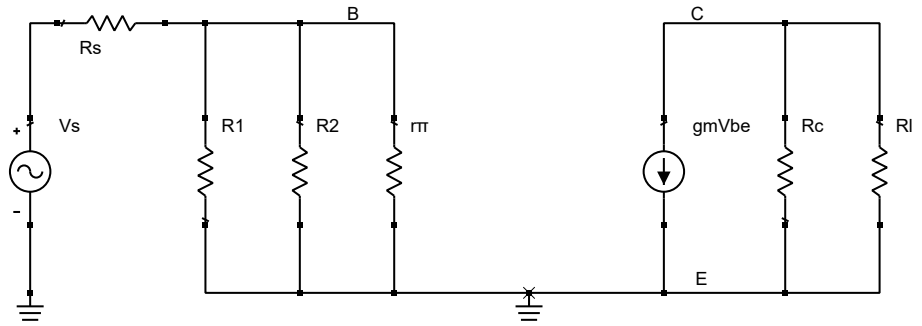

Figure 5.3: Circuit diagram used for small signal analysis of the microphone amplifier.

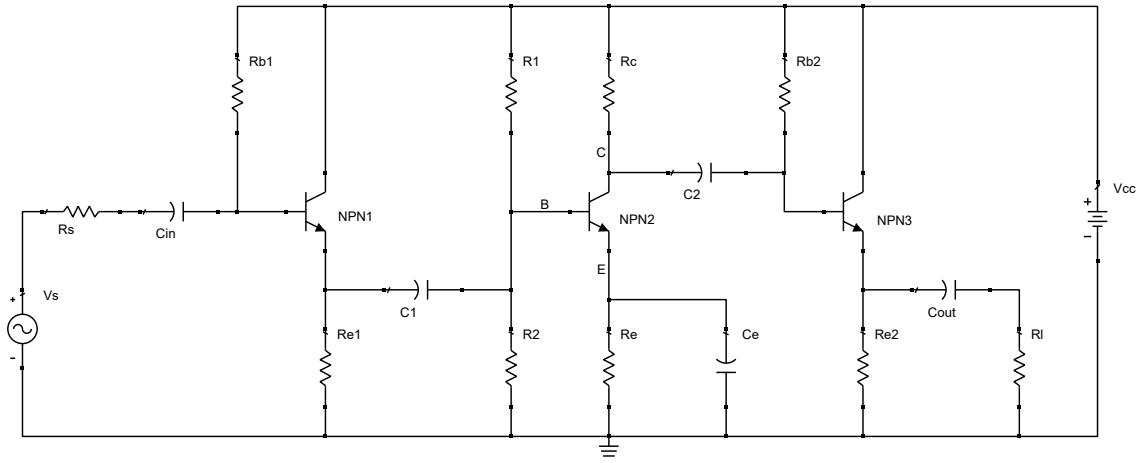

Figure 5.4: Improved design circuit diagram of the microphone amplifier.

$$A_v = -\frac{I_c}{V_T} R_c \tag{5.7}$$

5.3.4 Input and output impedance

Because of the voltage buffers at the input and output of the system, the input and output impedances of the microphone amplifier will be similar to those of the voltage buffer.

5.3.5 Microphone

As an input source the AOM-6738P-R electret microphone from Projects Unlimited will be used. The datasheet [11] shows the microphone has an impedance of 2.2kΩ and a bandwidth of about 30 Hz to 20 kHz with a sensitivity of -38 dB. Using an average sound pressure level of a human voice speaking at normal volume, a rough estimation of 3 mV can be assumed as the input voltage amplitude when simulating. The operating voltage of the microphone is 1.5 V which can easily be branched from the DC power supply using a voltage divider network.

5.4 Component choice

The component choice overview for the Microphone amplifier design of figure 5.4, can be seen in table 5.4. For this amplifier the 2n3904 NPN BTJ was chosen because it is easily available and easily fulfills the

specifications of the amplifier. The collector currents through each of the transistors is set to 1 mA for it is high enough for the device to function properly and low enough to not unnecessarily waste power. The capacitors were chosen to allow for the bandwidth of 20 Hz to 20 kHz.

Component	**Value**
Vs (amplitude, frequency)	3 mV, 1 kHz
Rs	2.2 kΩ
Cin	100 uF
C1	100 uF
C2	100 uF
Cout	100 uF
NPN1	2n3904
NPN2	2n3904
NPN3	2n3904
Rb1	620 kΩ
Rb2	620 kΩ
Re1	6 kΩ
Re2	6 kΩ
R1	73 kΩ
R2	14 kΩ
Rc (adjustable)	8 kΩ
Re	1.2 kΩ
Ce	620 uF
Rl	10 kΩ
Vcc	12 V

Table 5.1: Component list of the Microphone amplifier.

Chapter 6

Intermediate frequency amplifier

The Intermediate Frequency (IF) amplifier is the middle stage of the RX side of the transceiver. It sits in between the Intermediate Frequency Mixer and the Detector and is mainly used to provide a large amount of gain. The large gain of this stage should compensate for the power loss of the signal transmission through the air.

6.1 Design requirements

For designing the IF amplifier, the following design requirements were set.

- Bandwidth of 100 kHz on a center frequency of 4 MHz
- Steady voltage gain of at least 10000 (80 dB) over a the set bandwidth
- Steady voltage gain of at least 10000 (80 dB) for low voltage inputs
- Adjustable voltage gain
- Able to drive 70 Ω load impedance

The IF amplifier should be designed to have an adjustable voltage gain which can reach 10000 to compensate for the signal loss during transmission. It needs to be adjustable to be able to adjust the gain in case of lower transmission losses and thus less gain is needed. The amplifier should also include bandpass filtering to filter out high and low frequency noise and prevent as much signal reflections as possible to reflect back into the previous stage. The bandpass should pass the signal modulation bandwidth of 100 kHz on the IF center frequency of 4 MHz. It is important that the IF amplifier has an as steady as possible voltage gain over the said frequency, to prevent as much amplitude modulation noise as possible. This is important because the Demodulator stage, which comes after the IF amplifier, is sensitive to amplitude modulated signals and will demodulate it into noise. The IF amplifier should also work with a load impedance of 70 Ω since that is the input impedance of the Demodulater stage after the IF amplifier.

6.2 Topology

To realize the voltage gain of the IF amplifier stage, a common emitter configuration is used as class-A amplifier. The amplifier therefore needs a biasing network to make the BJT operate Forward Active mode. By connecting a parallel inductor-capacitor circuit at the the collector of the BJT, it adds the purpose as active bandpass filter to the amplifier. The circuit topology can be seen in figure 6.1. A single LC circuit bandpass results in a single resonance peak transfer. As can be seen in figure 6.1, a resistance R_t is added in parallel to the LC tank (L_t and C_t) at the collector of the BJT. This is to be able to control the gain of the amplifier as well as the quality factor (Q-factor) of the resonance peak, which will be made clear when analyzing the circuit. Resistor R_t will be made variable in the final design.

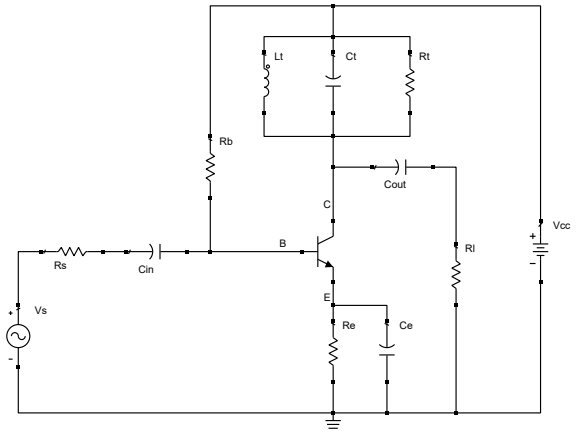

Figure 6.1: Circuit diagram of the bandpass amplifier.

6.3 Analysis

In order to design the IF amplifier circuit, it has to be analyzed for large signal behaviour concerning the biasing network and small signal behaviour to determine the voltage gain and frequency transfer of the amplifier.

6.3.1 Resonant frequency, Q-factor and impedance of parallel LCR circuit

The resonance frequency of the bandpass filter depends on the values for the inductor L_t and the capacitor C_t. The equation for the resonance frequency can be seen in equation 6.1. [12]

$$\begin{aligned} \omega_0 &= \frac{1}{\sqrt{LC}} \\ f_0 &= \frac{1}{2\pi\sqrt{LC}} \end{aligned} \tag{6.1}$$

The Q-factor of a resonant circuit is the ratio of its resonant frequency to its bandwidth. A higher Q-factor means a lower bandwidth and a higher amplitude peak in the bandpass transfer. The Q-factor equation can be seen in equation 6.2. [12]

$$\begin{aligned} Q &= \frac{\omega_0 R}{L} = \omega_0 RC \\ &= R\sqrt{\frac{C}{L}} \end{aligned} \tag{6.2}$$

The impedance of a parallel LC network can be derived as shown in equation 6.3. Using equation 6.1, the impedance of the parallel LC network can be written as a function of radial frequency ω and the radial resonant frequency ω_0. [12]

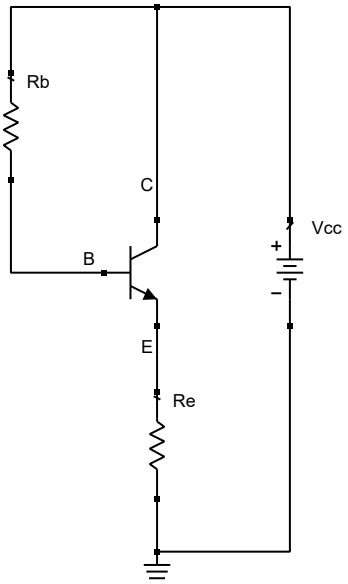

Figure 6.2: Circuit diagram used for large signal analysis of the bandpass amplifier.

$$
\begin{aligned}
Z_{(\omega)} &= \frac{Z_{L(\omega)} Z_{C(\omega)}}{Z_{L(\omega)} + Z_{C(\omega)}} \\
&= \frac{j\omega L \frac{1}{j\omega C}}{j\omega L + \frac{1}{j\omega C}} \\
&= -j \frac{\omega L}{\omega^2 LC - 1} \\
&= -j \frac{1}{C} \frac{\omega LC}{\omega^2 LC - 1} \\
&= -j \frac{1}{C} \frac{\omega}{\omega^2 - \frac{1}{LC}} \\
&= -j \frac{1}{C} \frac{\omega}{\omega^2 - \omega_0^2}
\end{aligned}
\tag{6.3}
$$

When the LC circuit is in resonance, by definition the impedances of the inductor and the capacitor are equal. Therefore the impedance of the parallel LC network at resonance becomes infinite which can be seen in equation 6.4. [12]

$$
\lim_{\omega \to \omega_0} Z_{(\omega)} = \lim_{\omega \to \omega_0} -j \frac{1}{C} \frac{\omega}{\omega^2 - \omega_0^2} = \infty \tag{6.4}
$$

6.3.2 Biasing network

For this amplifier the biasing was chosen to be a fixed base biasing with added emitter feedback resistor. In figure 6.2 a large DC signal analysis of the bandpass amplifier. For this DC analysis all capacitors are seen as open circuits and the inductance is seen as a short circuit.

The voltage across the emitter feedback resistor R_e and the value for the resistor itself are defined the same as in the Microphone amplifier design 5.1. By changing R_e the emitter current of the BJT can be set.

Knowing the DC current gain of the BJT, which can be found in the datasheet, the base resistor R_b can be calculated in the same way as done in the Voltage buffer design 4.3.

6.3.3 Voltage gain

In figure 6.3 a small signal AC circuit diagram of the bandpass amplifier can be seen. From this diagram the voltage gain can be derived as can be seen in equation 6.5. Because the input signal is oscillating with the LC resonance frequency, it is assumed for the derivation of the voltage gain that the impedance of the LC circuit is very high as explained in equation 6.4. The LC circuit is therefore seen as an open circuit.

From derivation 6.5 can be seen that the voltage gain A_v becomes attenuated by a large source resistance R_s and a small load resistance R_l. To remove the voltage gain dependency on the source and load resistances, it is assumed that the source resistance is much smaller than the parallel resistance between the base and the emitter terminal of the circuit ($R_s << (R_b//r_\pi)$) and that the load resistance is much larger than the LC parallel resistor ($R_l >> R_t$). The gain can than be controlled by R_t.

$$\begin{aligned} v_{out} = v_{ce} &= -g_m v_{be}(R_t//R_l) \\ &= -g_m v_s \frac{(R_b//r_\pi)}{R_s + (R_b//r_\pi)}(R_t//R_l) \\ A_v = \frac{v_{out}}{v_s} &= -g_m \frac{(R_b//r_\pi)}{R_s + (R_b//r_\pi)}(R_t//R_l) \\ &\approx -g_m(R_t//R_l) \\ A_v &\approx -\frac{I_c}{V_T}R_t \end{aligned} \tag{6.5}$$

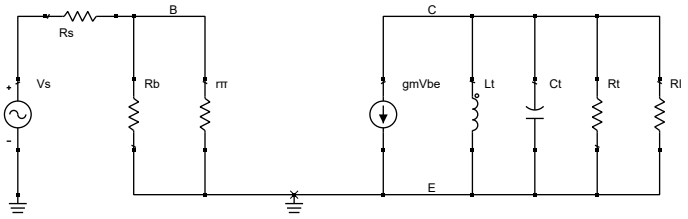

Figure 6.3: Circuit diagram used for small signal analysis of the bandpass amplifier.

6.3.4 Improved design

From simulation results of the previously discussed circuit, was found that it is quite impossible to reach a voltage gain of 10000 with only one transistor stage. Also as can be seen in equation 6.5 the voltage gain depends on the source and load impedances. To address these problems another bandpass amplifier was added to the circuit along with voltage buffers to isolate the bandpass amplifiers from each other and from the source and load impedances. Together this forms the complete IF amplifier circuit which can be seen in 6.4.

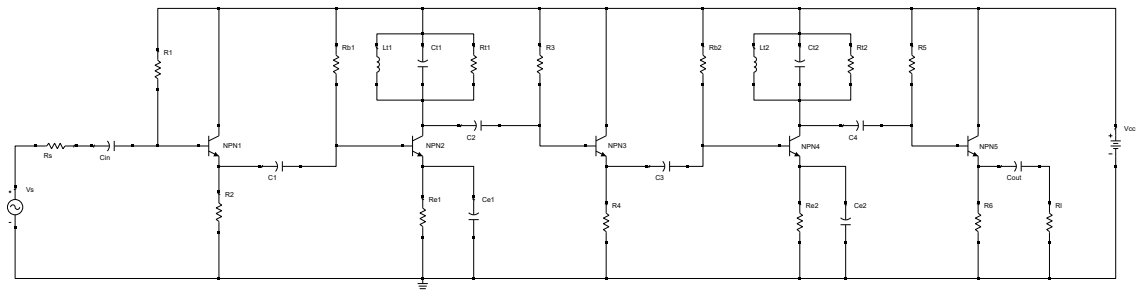

Figure 6.4: Circuit diagram of the IF amplifier.

This circuit makes use of two bandpass filters with two resonance peaks. When the resonance peaks are slightly shifted from each other, by altering the inductance or capacitance values, the combined bandpass transfer can be made more flat. This is preferred over a single peak transfer because it introduces less amplitude variation on the input signal, which results in less noise at the output of the Demodulator stage. The gain and the steepness of each peak can be controlled by the resistances R_t1 and R_t2. On the prototype, these resistance values can be varied by making use of variable resistors.

6.4 Component choice

The component overview of the IF design in figure 6.4, can be seen in table 6.4. A collector current of 20 mA was chosen for the bandpass amplifiers and 10 mA for the buffers. This is to increase the gain and stabilize the buffers, which tend to get nonlinearities in the transfer when a low load impedance is driven. Again the 2n3904 is used for all NPN BJTs since it functions for all the device specifications.

Component	Value
Vs (amplitude, frequency)	10 uV, 4 MHz
Rs	5 kΩ
Cin	10 nF
C1	10 nF
C2	10 nF
C3	10 nF
C4	10 nF
Cout	10 nF
NPN1	2n3904
NPN2	2n3904
NPN3	2n3904
NPN4	2n3904
NPN5	2n3904
R1	62 kΩ
R2	600 Ω
R3	62 kΩ
R4	600 Ω
R5	62 kΩ
R6	600 Ω
Rb1	50 kΩ
Re1	60 Ω
Ce1	100 nF
Lt1	2.2 uH
Ct1	727 pF
Rt1 (adjustable)	1 kΩ
Rb2	62 kΩ
Re2	60 Ω
Ce2	100 nF
Lt2	2.2 uH
Ct2	642 pF
Rt2 (adjustable)	2.6 kΩ
Rl	70 Ω
Vcc	12 V

Table 6.1: Component list of the IF amplifier.

Chapter 7

Feedback amplifier

The feedback amplifier is the first stage of the speaker amplifier. It is a voltage amplifier with feedback for a linear response. This amplifier needed to be designed because a class-AB amplifier was used for the speaker amplifier. A class-AB amplifier is a voltage follower and the demodulator has a low output voltage. In order to deliver enough power to the speaker the voltage has to be boosted to a significant amplitude. The microphone amplifier is not linear anymore on this output amplitude and therefore it could not be used for this stage.

7.1 Design requirements

The main requirement of the feedback amplifier is to boost the voltage for the speaker amplifier, and have minimal distortion. The design goals and specifications for the amplifier were set as follows.

- A minimal output voltage amplitude of 2 V
- A minimal input voltage amplitude of 20 mV
- Minimal distortion
- Gain of 100
- Bandwidth of 20 Hz to 20 kHz
- High input impedance
- Drive a load of about 5 kΩ

The design requirement of the feedback amplifier is to have a linear amplification and to have at least a 4 V peak to peak output signal. Although up to 10 V peak to peak is also a possibility. This is because the speaker amplifier will have a maximum voltage swing of around 4V when the supply voltage is center tapped and a maximum voltage swing of 10V when the supply voltage is not center tapped. Since the input voltage is a few millivolts, the gain should be 100 or higher. A Gain of 100 was set as the design goal since the input amplitude was estimated at 20 mV to 40 mV by the group that designed the demodulator. The High input impedance creates a better transfer. This design should not waste unnecessary energy but linear amplification is more important. The input impedance of the next stage is about 5kΩ.

7.2 Topology

For the design of the feedback amplifier a class-A amplifier was tweaked with negative feedback and a current source. In the total harmonic distortion (THD) simulation of the microphone amplifier seen in figure 9.2, it can be seen that the distortion of a normal class-A amplifier would be too high for the input

voltage of the feedback amplifier. The current source was needed to make the voltage amplifier linear and the feedback was needed to control the gain. A voltage buffer is also placed on the output and input of the amplifier. The topology can be seen in figure 7.1.

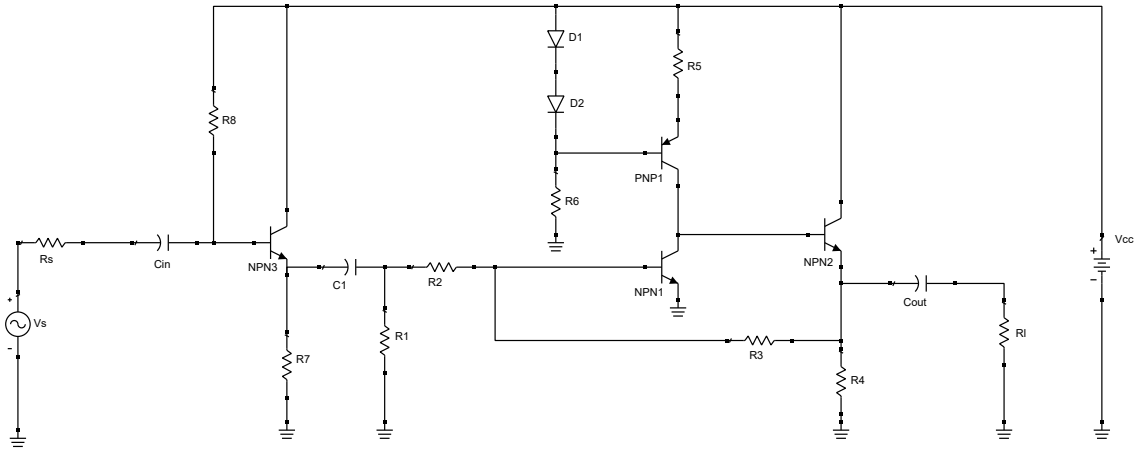

Figure 7.1: Circuit feedback amplifier with buffer

An ideal current source is not a real component. A non-ideal current source was made with a PNP transistor, the analysis of this circuit can be found in equation 7.1. The current source has two functions. The first is to create a constant current through the class-A amplifier, the second is to provide a large gain. The gain of the class-A amplifier is dependant on the collector resistance. A current source has a very high impedance and therefore will provide a very large gain. This gain is then controlled with a feedback circuit after the buffer. If this feedback circuit was not implemented the output of the class-A amplifier would always clip since the gain is too high. The feedback network consists of 2 resistors, the ratio between these resistors create the gain of the amplifier, the analysis of this small feedback network can be found in equation 7.2.

With this design all the resistors for the normal class-A amplifier can be removed. The emitter resistance is not needed anymore since a very stable current is provided to the collector of the transistor. The collector current is not needed anymore since a high impedance is provided by the current source. Finally the biasing of the transistor in the class-A amplifier is done by the feedback network. Therefore the biasing resistors can also be removed.

The final buffer needs an emitter resistance to decouple the output from ground. The value of this resistor is not really important but should not be too low in order to limit the collector current in the buffer. To ensure the output of the last buffer is at 6 V for no input an extra resistor is placed at the end of the feedback network the analysis can be found in equation 7.3. This is needed in order to create maximum voltage swing at the output. The buffer does not need to be biased anymore with an external biasing network, since a current source is placed on the collector of the Class-A amp and base of the buffer. If the buffer is not supplied with enough voltage to turn on the class-A amplifier, the current source will need to supply a higher voltage, otherwise the constant current cannot flow.

7.3 Analysis

In the next section an analysis will be done of the final design. First the current source will be analyzed after which the rest of the circuit will be analyzed.

7.3.1 Current source

A current source is not a real device. However a non-ideal current source can be made with 2 diodes, 2 resistors and a PNP transistor. One of the diodes supplies the voltage drop V_{be} to the NPN transistor and the other diode supplies a fixed voltage drop over the resistor R_1 in order to create a fixed current. The last resistor R_2 is used to create a current through the diodes and therefore allow a voltage drop.

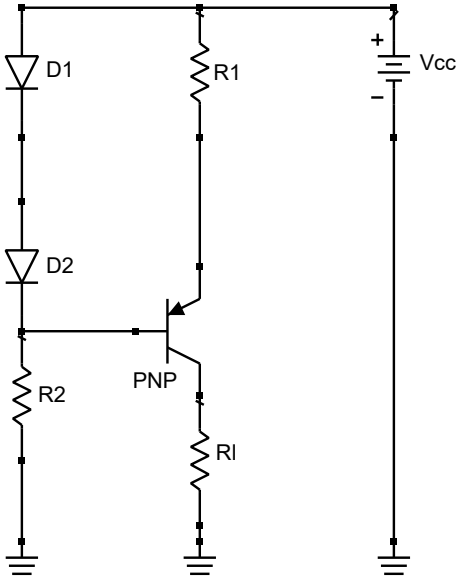

Figure 7.2: Circuit of the current source

$$\begin{aligned} V_{R_1} &= V_{D1} + V_{D2} - V_{be} \\ V_{R_1} &= V_{D1} \end{aligned} \tag{7.1}$$

Because of the limited supply voltage the current supplied by the current source will collapse if the load becomes too high. The limitations of the circuit are shown in figure 7.3.

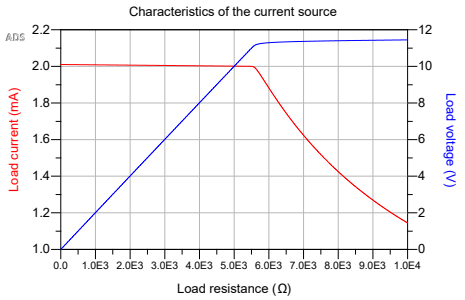

Figure 7.3: Limitations of the current source

7.3.2 Feedback network

The feedback network feeds the output of the amplifier back to the input. This reduces fluctuations in the output. It will be analyzed using a simplified circuit seen in figure 7.4 where the current source is replaced with an ideal current source and capacitors. In this AC analysis capacitors and voltage sources are shorted although this is not visible in the figure. It is also assumed that the base current of the transistors

is negligible. The gain will be analyzed in equation 7.2. Finally an analysis of the DC emitter voltage will be done in **??**. It is also visible form the equations that R_4 does not play a significant role in the amplifier response. However if it were completely removed the output voltage would be grounded.

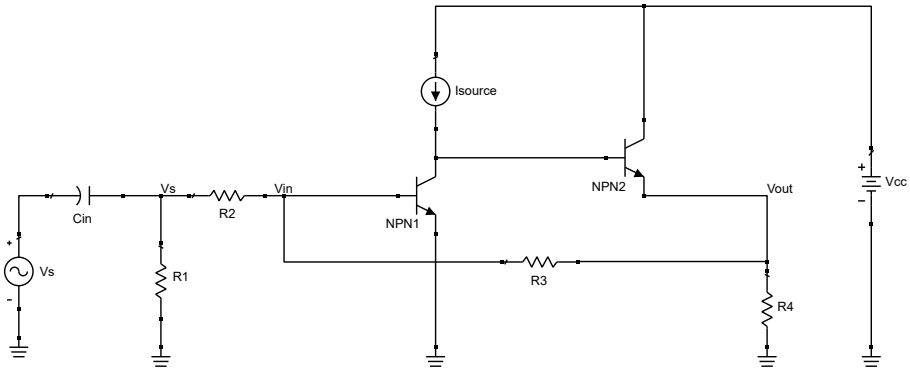

Figure 7.4: Simplified feedback amplifier circuit

$$\begin{aligned} \frac{v_{in}}{R_2} &= \frac{-v_{out}}{R_3} \\ \frac{v_{out}}{v_{in}} &= -\frac{R_3}{R_2} \end{aligned} \tag{7.2}$$

$$\begin{aligned} \frac{V_{out} - V_{be}}{R_3} &= \frac{V_{be}}{R_1 + R_2} \\ V_{out} &= V_{be}(\frac{R_3}{R_1 + R_2} + 1) \end{aligned} \tag{7.3}$$

7.4 Component choice

This design operates at a relatively low frequency. The currents through all the transistors are not high. For the NPN transistor in the amplifier and the buffer 2n3904's were used and for the PNP a 2n3906 was used.

For R_5 150Ω was used. this resulted in about 3.5 mA from the current source.

For the diodes the 1N4148 were chosen since they are widely available, reliable and low cost.

The capacitors need to behave like a short circuit for 20Hz and a DC block. A value of 100μF was sufficient.

For R_6 a value of 10kΩ was used. This resistor needs to limit the current through the diodes but also needs to leave enough current for the base of the PNP transistor.

For R_4 a value of 10kΩ was used. This resistor needs to limit the emitter current.

R_3 and R_2 were set to 20kΩ and a variable resistance around 100 Ω respectively. This should supply a gain of 100 but R_2 can be tuned to create a higher gain.

R_1 was set to 2.5kΩ to create a 6V DC output voltage.

7.4.1 Component list

The final feedback amplifier can be seen in figure 7.1. The components are listed in table 7.4.1

Component	Value
C_{in}	100 μF
C_1	100 μF
C_{out}	620 μF
R_1	2.5 kΩ
R_2	140 Ω (variable)
R_3	20 kΩ
R_4	10 kΩ
R_5	150 Ω
R_6	10 kΩ
R_7	6 kΩ
R_8	620 kΩ
R_l	5 kΩ
NPN_1	2N3904
NPN_2	2N3904
NPN_3	2N3904
PNP_1	2N3906
D_1	1N4148
D_2	1N4148
V_{cc}	12 V

Table 7.1: Component list of the feedback amplifier.

Chapter 8

Speaker Amplifier

The speaker amplifier is split into two parts, the feedback amplifier, discussed in chapter7 and a class-AB amplifier discussed in this chapter. The speaker amplifier is used to amplify a signal to power a speaker. It should have a large power gain since an information signal, the audio signal, is directly used to power the speaker. Usually speakers have a very low impedance and therefore speaker amplifiers should deliver a large current to create sufficient power. A Class AB-amplifier was used since it can deliver a large current and still be efficient. The voltage amplification of the signal is performed by the feedback amplifier, which is needed since the demodulator weakens the voltage significantly and a class-AB amplifier is a voltage follower.

8.1 Design requirements

The main requirement of the speaker design is to drive a speaker with a powerful enough signal, and recreate the input signal of the microphone with an audible volume. To achieve this, the following design goals and specifications were set to the class-AB amplifier.

- A minimum of 250 mW output power for an 8 Ω load
- Bandwidth of 20 Hz to 20 kHz
- High efficiency
- High current gain
- High input impedance
- Minimal distortion

A target of 250 mW was chosen because this was the lowest power rating for a speaker that could be find. A load of 8 Ω was chosen since it is a usual speaker impedance. To achieve the power rating to such a low load a high current gain is required. The amplifier should also have a reasonable efficiency. A percentage is not specified but efficiency should be considered in every design choice. The amplification of the signal should be as linear as possible and should not add a lot of distortion. A high input impedance is desired to achieve a better transfer of the input signal. Finally a bandwidth of 20 Hz to 20 kHz is desired, to follow the complete system requirements.

8.2 Topology

The final design of class-AB amplifier uses two Sziklai transistors and other improvements to make the amplifier more stable, linear and efficient. The class-AB topology was used since it can be very efficient when designed properly and has a high current gain. The Sziklai transistors were used to improve total

harmonic distortion, improve the input impedance and create a better voltage follower. The input was split in order to create a more linear amplification and the power supply was center tapped in order to create a more efficient design.

8.2.1 Previous designs

In this subsection the design process will be explained. The final design can best be understood if the previous designs, with all of their flaws, are discussed. The design choices of the previous designs will also be explained in this section.

AB-Class amplifier

The first thing that needs to be chosen in the design of the speaker amplifier is the amplifier type. A class-AB was chosen since it has minimal crossover distortion if designed correctly. A good efficiency can also be achieved with this class type. Using the feedback amplifier directly would result in a more linear amplification but with a low efficiency. Heat dissipation would become an issue. A class-B and class-XD amplifier were also considered but not chosen. Class-B provides a better efficiency but adds a lot of crossover distortion to the signal. Class-XD is a more complex version of class-AB and a lot less literature can be found on this amplifier, making it an unsuitable amplifier class for this project.

Diode and transistor biasing

For the first design of the class-AB amplifier the NPN and PNP transistors were biased with two diodes, as shown in figure 8.1. This is an effective way of biasing since the diodes provide a constant voltage drop of around 0.7 V. Other resistors were used in order to limit the current through the diodes to prevent energy dissipation.

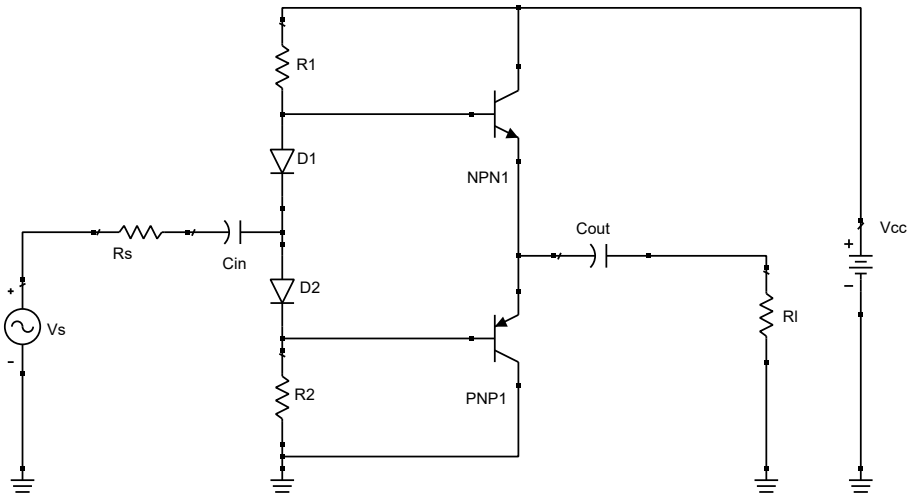

Figure 8.1: Topology of the class-AB amplifier with diode biasing

However problems arise using the biasing method of this design. Using the basic diodes, the voltage drop is smaller than the voltage that was needed to bring both transistors in saturation. This caused the transistors to stay in the resistive region when no input was applied. When an input was applied, a small part of the signal was needed to bring the transistors in saturation. This makes the amplifier more efficient but it does generate some crossover distortion as shown in figure 8.2 and figure 8.3. Since the amplifier does not provide a lot of power, it was decided that some efficiency could be sacrificed for less distortion of the output.

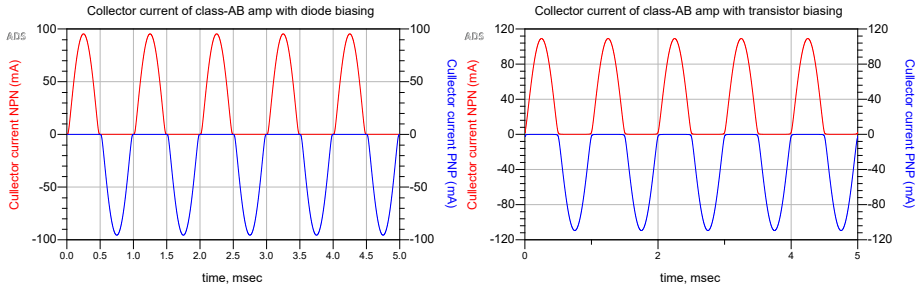

Figure 8.2: Collector currents of two class-AB designs

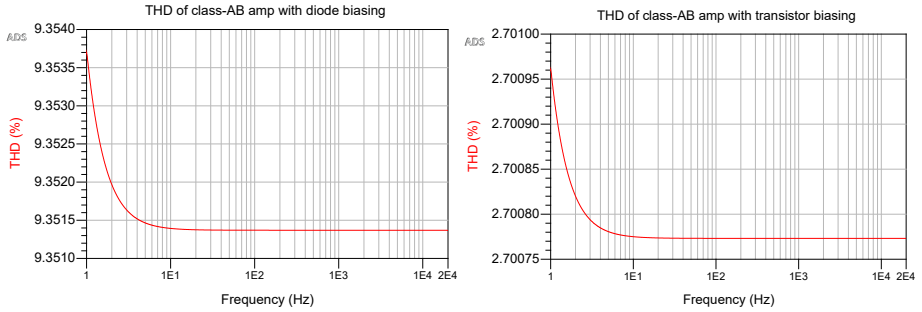

Figure 8.3: Total harmonic distortion of two class-AB designs

The next generation of the class-AB amplifier is shown in figure 8.4. The design still uses diodes but with a larger voltage drop than the 0.7 V of the normal diode. There are diodes available with larger voltage drops of 1 V or 1.5 V. However this would be too much. If a V_{be} of 1 V or 1.5 V is applied, the transistor operates in the saturation region with a high base current and therefore a very large collector current. This makes the class-AB amplifier perform with the efficiency of a class-A amplifier.

Emitter resistances were added to limit the collector current. When a collector current is flowing, a

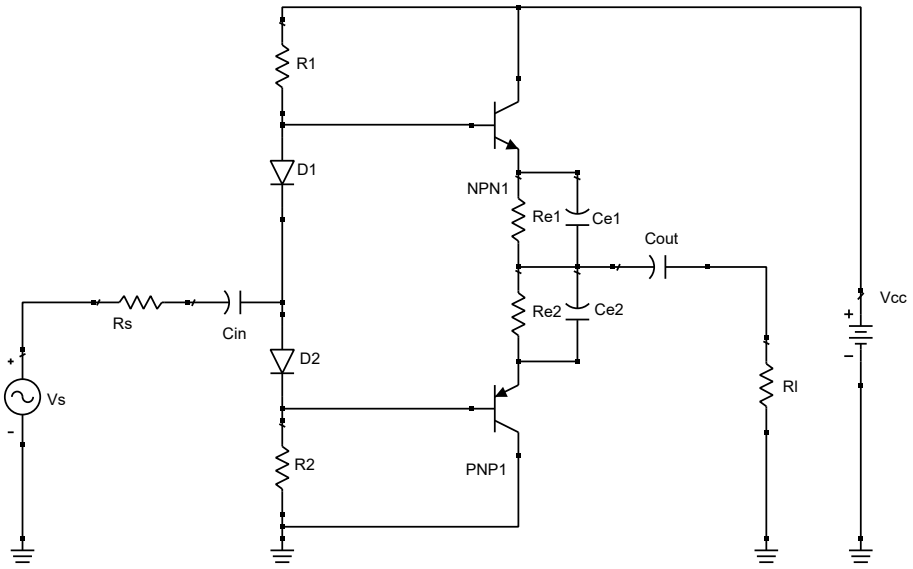

Figure 8.4: Topology of the class-AB amplifier with emitter resistance and capacitance

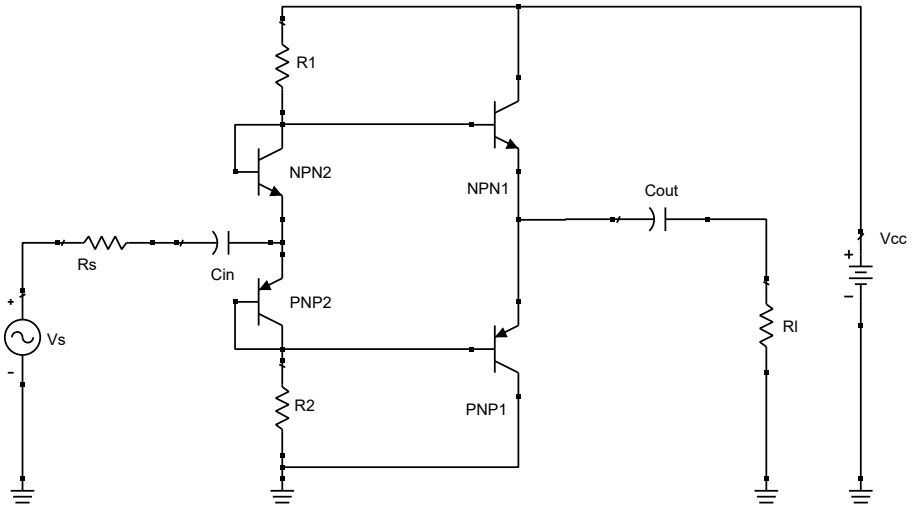

Figure 8.5: Topology of the class-AB amplifier with transistor biasing

voltage drop over R_e is created and V_{be} becomes smaller. This causes the base current and collector current to drop significantly. A larger resistance means a smaller V_{be}, which is desired. However if R_e is too large, the transistors are in the resistive region and this causes crossover distortion.

The capacitors were added in order to create a short circuit for the AC current flowing though the transistors, similar to the C_e in the A-Class amplifier. If these are not added, the current gain of the circuit is lowered and a lot of energy is wasted in the circuit.

Another method of biasing is shown in figure 8.5. If the diodes are replaced with the same transistors that are already used for the design, the collector and base are connected to each other. They then function as a diode. With the resistors R_1 and R_2 the current through these diode functioning transistors can be chosen. This current should be large enough to barely bring them in saturation mode. Since the V_{be} of the amplifying transistors are the same as the bias transistors the amplifying transistors are in the same region. Furthermore the transistors should be thermally matched. If this is done the thermal influence on V_{be} is not an issue anymore. This design has no crossover distortion as can be seen in figure 8.2.

This design would be enough to create a good class-AB amplifier, however there are still some aspects of this design that limit the efficiency.

First of all, the biasing topology is a current mirror, therefore the DC collector current also flows through the biasing resistors and the transistors. Ideally this current should be lower than the collector current since it is wasted energy. Another problem arises when the biasing resistors R_1 and R_2 are large. When this happens simultaneously with a large input amplitude, there is not enough base current for the amplifier to follow the input voltage and clipping occurs at the output as can be seen in figure 8.6. This is unacceptable and the biasing resistors should be lower, further increasing the DC currents and power loss in the design. This design also is not a perfect voltage follower, especially when the input was large the output voltage was a scaled version of the input and the theoretical maximum output voltage of $V_{cc} - V_{be}$ was only achieved with an input that was much higher.

Darlington design

In the next design the amplifying NPN and PNP transistors are replaced with two NPN and PNP transistors in Darlington configuration. This approach had both pros and cons.

The current gain of the Darlington pair is very high thus the biasing resistors can be very high. The lim-

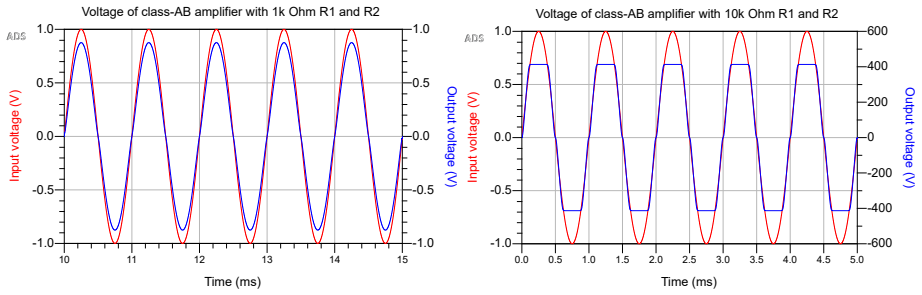

Figure 8.6: Voltage characteristics of the class-AB design

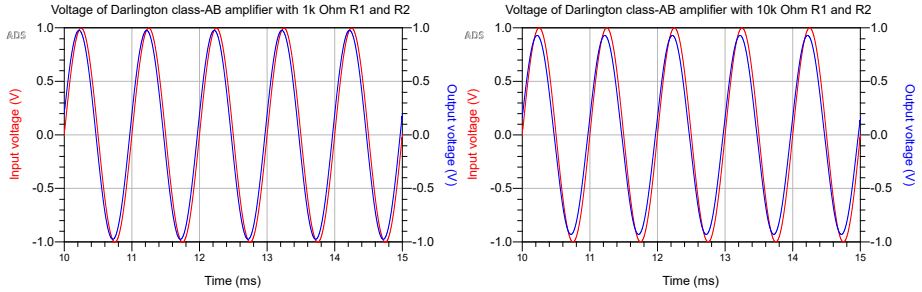

Figure 8.7: Voltage characteristics of the Darlington class-AB design

ited base current is not a problem anymore as can be seen in figure 8.7 compared to 8.6. This topology also proved to be a near perfect voltage follower since the β of the Darlington pair is very high. Both of these aspects of the topology increase efficiency. The input impedance is significantly higher due to the large β and the higher biasing resistors, this is shown in figure 8.8. However there is also a disadvantage. Since there are now two amplifying transistors, the biasing voltage needs to be twice as high. The maximum voltage swing of the amplifier has therefore been decreased. This reduces efficiency since a larger voltage drop is created over the transistors. This topology was still deemed more efficient since the maximum voltage swing of the single transistor topology was only achieved with a very low biasing resistor and thus a large waste current.

For the first iteration of the design two biasing transistors were used for each Darlington pair. These transistors were used as diodes and were not put into saturation because that would create a too large V_{be} over the Darlington pair. This topology works in a simulator with a very low current through the biasing transistors. However in a real life situation the temperature of all the 4 biasing transistors is different and changes. The temperature affects the V_{be} drop and therefore the biasing is not stable.

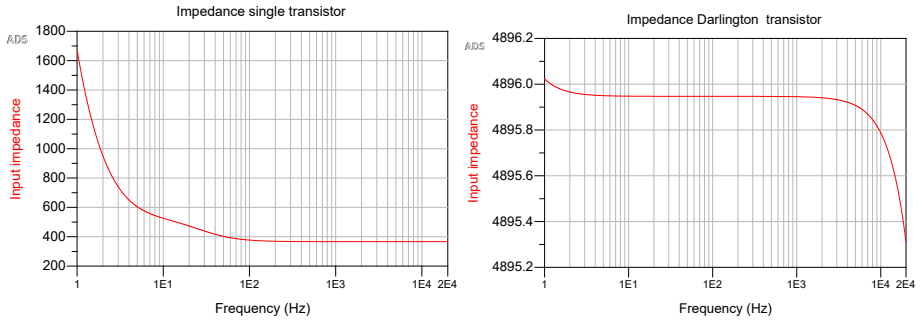

Figure 8.8: Input impedance of different topologies

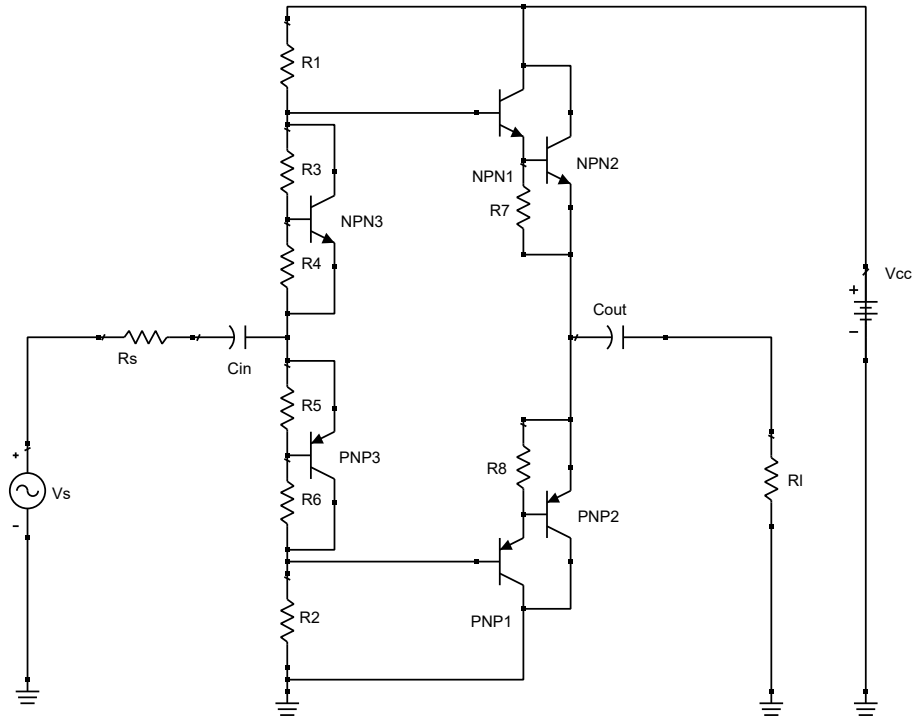

Figure 8.9: Topology of the Darlington AB-Class amplifier

To fix this issue a new biasing method was used of one transistor and two resistors. The current through the resistor connected to emitter and base is determined by the constant V_{be}. This current can only come from the second resistor and therefore the voltage drop can be chosen by varying the resistance of the resistors. If these resistors are variable it is even possible to tweak the biasing in the prototype which would be very useful. This iteration of the class-AB amplifier is shown in figure 8.9

There is another issue that might occur with the Darlington configuration. Different transistors are used in a class-AB amplifier. An NPN and an PNP. Although if chosen correctly the transistors are very similar. They are different devices and therefore might respond differently to temperature or have a different β. In a normal class-AB this is not a problem but with Darlington the β of the transistors are multiplied and any imperfection will be amplified.

Sziklai design

Another topology can be used for the amplifying transistors. A Sziklai configuration can be used, with this topology an NPN transistor drives an PNP transistor for the NPN transistor replacement. For the PNP replacement a PNP transistor drives an NPN transistor. The benefit of this transistor topology over a Darlington is that the β of the NPN and PNP are multiplied by each other and therefore both the NPN and PNP replacement. therefore they will have the same β and any manufacturing offset between the complementary transistors will be ignored.

With the Sziklai topology the biasing cannot be done with only transistors or diodes. Only the first transistor in the Sziklai pair needs to be biased and this transistor should not be in saturation mode, it only needs to deliver a very small current to the second transistor. If biased with a diode or transistor the DC collector current would be way too high.

In the Sziklai design shown in figure 8.10, the biasing was done with a tunable circuit of 2 resistors and

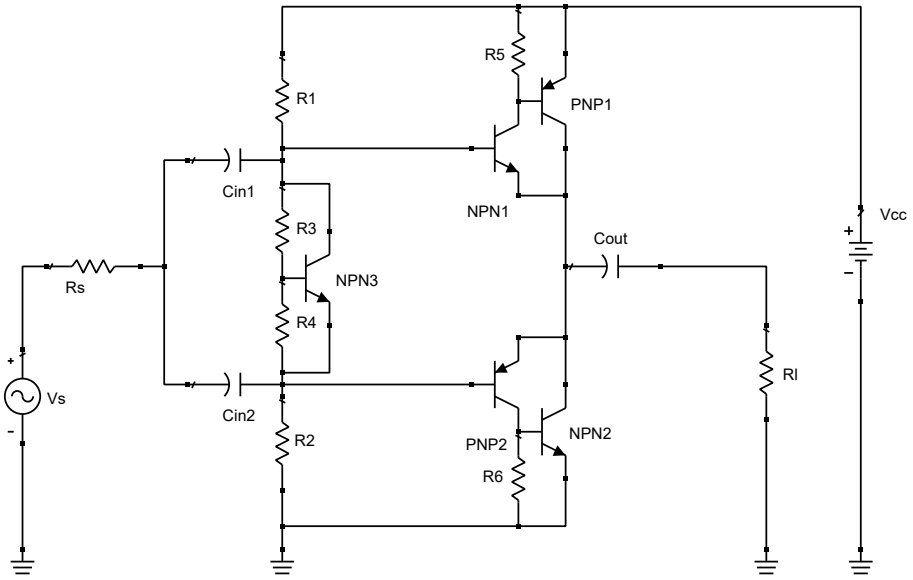

Figure 8.10: Topology of the Sziklai AB-Class amplifier

one transistor. This way the biasing can be changed in the prototype.

For the power supply of the class-AB amplifier at first the normal V_{cc} was used. However if the input signal of the class-AB amplifier is not close to the maximum voltage swing of the amplifier the extra voltage that the power supply gives only leads to dissipation in the transistors. Since the output amplitude of the speaker amplifier did not reach 5 V but could reach 2 V it was decided to center tab the power supply and supply the amplifier with $\frac{V_{cc}}{2}$.

A different design topology with a split input was also needed. For the Sziklai topology one biasing circuit is used. If the input is not split, the output of the feedback amplifier would get weakened by the biasing circuit before it would reach one of the transistors. This would cause a better amplification of either the positive or negative part of the input signal. To omit this problem the input was split and in each branch a DC-block was added.

Final design

The final design shown in figure 8.11 is a combination of the Sziklai class-AB amplifier design and the feedback with buffers in between. The feedback amplifier is needed to boost the voltage of the signal and the buffers are needed to minimize the effects of the input and output impedances of the amplifier and previous stage. It is possible the combine the two amplifiers for a design with less components. This was not done due to added complexity and design time.

The R_5 of the a class amplifier was made variable. This is because the input signal is still unknown. Maximal voltage swing is desired for the output signal of the a class amplifier. If R_5 is made higher the gain of the amplifier becomes higher, if it is made lower the voltage swing can become larger. A more precise explanation can be read in the chapter5

8.3 Analysis

In the next section a theoretical analysis of the class-AB amplifier will be done. The analysis of the buffers and feedback can be found in chapters 4 and 7. First the biasing of the circuit will be explained in the DC

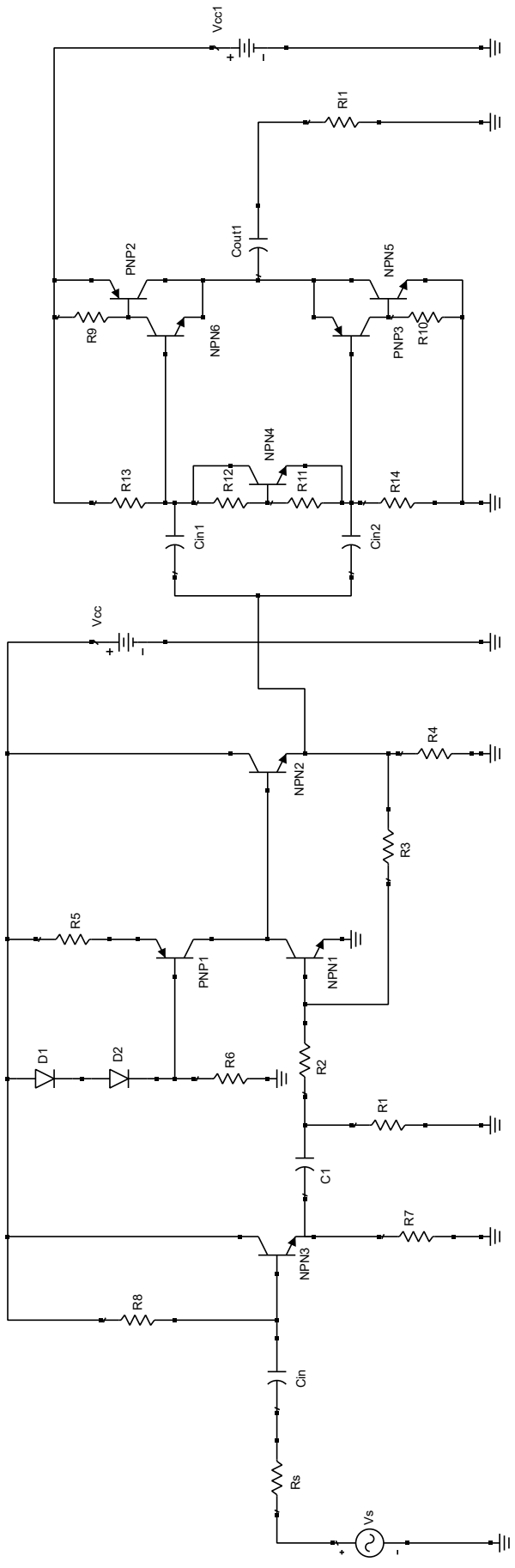

Figure 8.11: Topology of complete speaker amplifier

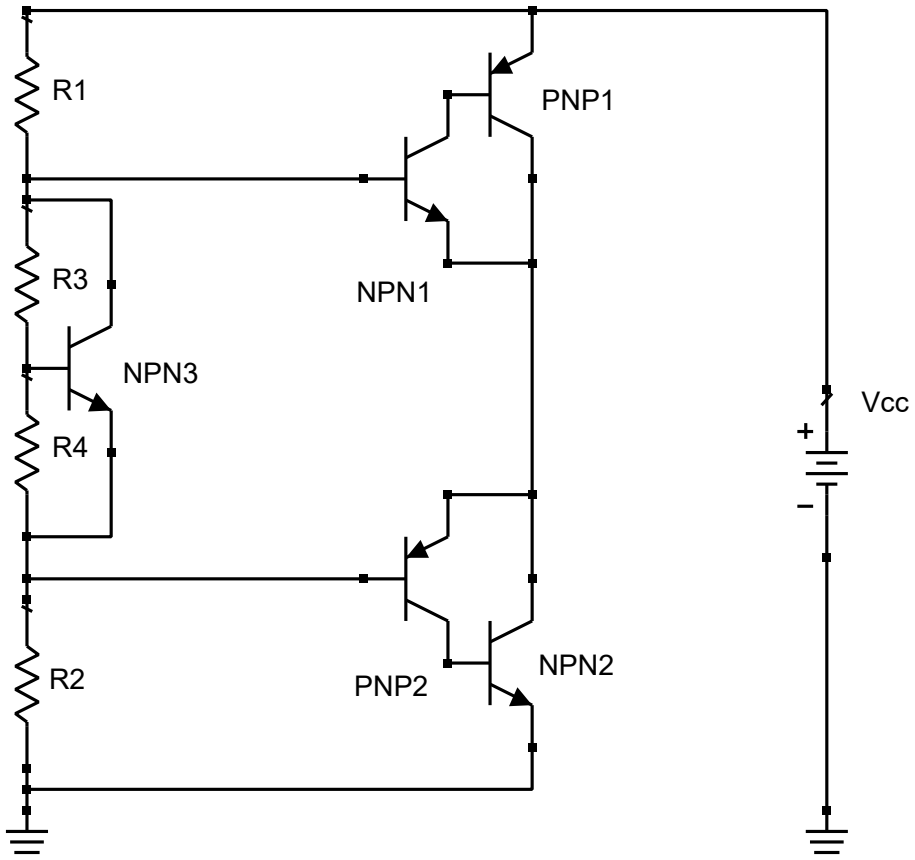

Figure 8.12: DC model of the class-AB amplifier

analysis, then the response to an AC input signal will be explained in the AC analysis. The voltages are oriented from top to bottom or left to right, which corresponds to the direction of the currents.

8.3.1 DC analysis

For the DC analysis the components names are shown in figure 8.12. The capacitors can be considered as an open circuit for the DC analysis since DC cannot pass through a capacitor no matter the value.

First the biasing circuit consisting of R_3, R_4 and NPN_3 will be analyzed and the total voltage drop will be given in R_3, R_4 and V_{be}. V_{be} is a constant value for the transistor and is around 0.7V. The base current of a transistor is almost zero. This will be assumed in the calculations. KVL states the V_{be} is equal to the V_{R_4}.

$$\begin{aligned} I_{R_4} &\approx I_{R_3} \\ V_{bias} &\approx V_{R_4}(1 + \frac{R_3}{R_4}) \\ V_{bias} &\approx V_{be}(1 + \frac{R_3}{R_4}) \\ V_{bias} &= V_{be_(NPN_1)} + V_{eb_(PNP_2)} \end{aligned} \tag{8.1}$$

The benefit of this small biasing circuit becomes clear: the voltage drop can be determined by the ratio of R_3 to R_4. Since the transistors NPN_1 and PNP_2 are complementary, the voltages $V_{be_(NPN_1)}$ and

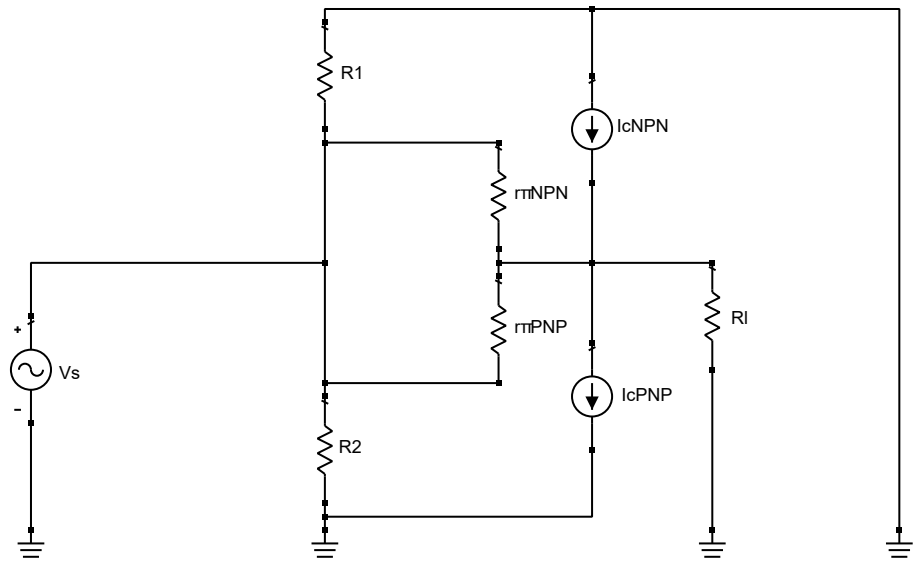

Figure 8.13: AC model of the class-AB amplifier

$V_{eb_{(PNP_2)}}$ are equal.

The maximum voltage swing of the class-AB amplifier can also be explained in the DC analysis of the amplifier. In order for the amplifier to conduct current $V_{be_{(NPN_1)}}$ and $V_{eb_{(PNP_1)}}$ must be around 0.7 V. $V_{cb_{(NPN_1)}}$ and $V_{bc_{(PNP_1)}}$ can drop to almost 0.

$$V_{R_l max} \approx V_{cc} - V_{be(NPN_1)} - V_{eb(PNP_1)} \tag{8.2}$$

8.3.2 AC analysis

After the biasing analysis is done and the circuit is properly biased, the output signal can be modeled as a function of the input. The AC model shown in figure 8.13, can be derived from 8.10. In an AC analysis the capacitors can be shorted, given they have a large enough capacitance. DC voltage sources can be shorted. The biasing circuit is also bypassed because the two input capacitors are shorted, this causes the top and bottom of the biasing circuit to be one node in the AC model. The Sziklai transistors are modeled as one transistor with high β.

The output voltage will be modeled as a function of the input voltage. The power can then be derived from the fixed load. In the analysis it is assumed that only one transistor is always on. This is the case when the circuit is properly biased. When a transistor is in the off state the corresponding current source becomes an open circuit since no current can pass through it. This forces the current provided by the other transistor into the load.

$$
\begin{aligned}
I_b &= \frac{V_{in} - V_{out}}{R_\pi} \\
R_\pi &= -\frac{\beta}{g_m} \\
g_m &= -\frac{I_c}{V_t} \\
R_\pi &= -\frac{\beta V_t}{I_c} \\
I_b &= \frac{(V_{in} - V_{out}) I_c}{V_t} \\
V_{out} &= V_{in} - V_t
\end{aligned}
\tag{8.3}
$$

The analysis shows that the voltage following behaviour of the device is in an ideal situation not dependant on β or R_L. However the transistors need a certain base current to deliver the collector current for the desired output voltage. A higher β causes less base current to be needed. The transistors also can handle only a finite amount of collector current, therefore if the load becomes too low, the output voltage cannot follow the input voltage.

8.4 Component choice

The transistors, resistors and decoupling capacitors need to be chosen. In this section an explanation will be given for each choice. The component names of figure 8.10 are used in this section.

8.4.1 Transistors

First of all the transistors need to be chosen, A high collector current can be expected if the input voltage is high. During the design stage of the class-AB amplifier, it was still uncertain what the input of the device was going to be and of the power supply was going to be center tapped. When maximum voltage swing is achieved, 5 V amplitude, the maximum current through the 8 Ω load is 625 mA. In order to handle this large current the BC337 for NPN and BC327 for PNP were chosen. The transistors have a maximum I_c of 800 mA and are complementary devices. In order to keep the β of the Sziklai transistors the same all the transistors in Sziklai configuration were equal, even though the first transistors deliver a very small current.

8.4.2 Resistors

The resistors R_1 and R_2 need to be large in order to minimize wasteful current. However if they are too large the circuit will not be properly biased and not enough base current will be available. From simulations it was found that resistors of 10 kΩ had a sufficient performance.

For the resistors R_5 and R_6 a value of 1 kΩ was used. This reduces the time constant of RC network significantly since R_π is not the only resistance anymore. The capacitance of the Sziklai transistor is not certain, a lot of data-sheets provided different values but all were around a few picofarads resulting in a time constant of a few nano seconds.

8.4.3 Biasing circuit

The biasing circuit requires a constant voltage drop. The voltage drop should eliminate crossover distortion but should not waste energy. The resistor R_4 was chosen at 5 kΩ. This makes sure the current is not too large while simultaneously creating a stable voltage drop. R_3 was made variable around 5 kΩ in order to tweak the biasing in the prototype. In simulations a value of 5 kΩ resulted in the best biasing. For the transistor a 2n3904 was chosen. Almost every transistor would be sufficient since only a constant V_{be} is needed. This transistor was needed for other designs and was the cheap and therefore a good option.

8.4.4 Speaker

For the speaker the visaton BF 32 - 8 Ohm will be used. The datasheet [13] shows the speaker has an impedance of 8Ω and a bandwidth of 150 Hz to 20 kHz and a power rating of 2 watt. The speaker has a smaller bandwidth than the design goal. However a better speaker would be too expensive for this project.

8.4.5 Component list

The final class-AB amplifier is shown in figure 8.10. The components are listed in table 8.4.5

Component	**Value**
C_{in1}	100 μF
C_{in2}	100 μF
C_{out}	620 μF
R_1	10 kΩ
R_2	10 kΩ
R_3	6 kΩ (variable)
R_4	5 kΩ
R_5	1 kΩ
R_6	1 kΩ
R_l	8 Ω
NPN_1	BC337
NPN_2	BC337
NPN_3	2n3904
PNP_1	BC327
PNP_2	BC327
V_{cc}	6 V

Table 8.1: Component list of the Feedback buffer.

Chapter 9

Results and discussion

In this chapter the results of each sub and main design are shown and discussed.

9.1 Voltage buffer

The voltage buffer is simulated with the component values shown in table 4.4 and the circuit design shown in 4.1. In figure 9.1 the simulation results of the voltage buffer can be seen. The voltage waveforms show that the output voltage follows the input voltage without any time delay or phase shift. The input impedance as derived in chapter 4, is 300 kΩ which is high as expected. The bandwidth of the buffer is about 100 MHz. It is this because it is only limited to the input and output capacitors and the internal capacitance of the transistor which are very low. The voltage gain is almost 1 over the entire range of 20 Hz to 20 kHz. It can be seen that the voltage gain stays steady until the input voltage amplitude reaches a voltage of about 5 V, which is the maximum amplitude that can be reached with a DC voltage supply of 12 V. The THD of the device also stays very low until the 5 V threshold is reached or the input frequency reaches the end of the frequency band.

9.2 Microphone amplifier

The Microphone amplifier simulations are done with the component values shown in 5.4 and the circuit design shown in 5.4. The simulation results of the microphone amplifier can be seen in 9.2. From the waveform simulations can be seen that the voltage is amplified to the output with a phase shift of 180 degrees. The gain, which is adjustable from about 40 dB to 45 dB, is steady on the range of 20 Hz to 20 kHz. The total -6 dB bandwidth of the Microphone amplifier reaches from 4 Hz to 4.3 MHz. The lower cutoff frequency of the bandwidth is determined by the decoupling capacitors while the upper cutoff frequency is determined by the internal capacitance of the BJT. From the *Voltage gain over input voltage* plot can be seen that above an input voltage of 15 mV the voltage gain starts to drop. A similar result can be seen in the *THD over input voltage plot* where the THD reaches a significantly high percentage after 15 mV. This is due to the non linear output of the Microphone amplifier when an input signal with too large of an amplitude is amplified, as discussed in chapter 5. Further can be seen that for a steady input voltage amplitude the THD reaches a steady maximum value of 1.7 % over the entire bandwidth. The input impedance reaches a steady value of 220 kΩ over the range of 20 Hz to 20 kHz. In figure 9.7 the voltage step response of the Microphone amplifier can be seen. From the figure can be seen that when a step of 3 mV is applied to the input, to output reaches an output level of almost -600 mV which is expected with a voltage gain of about -200.

9.3 Intermediate frequency amplifier

The IF amplifier is simulated using the components shown in table 6.4 and the circuit design shown in figure 6.4. The simulation results can be seen in figure 9.3. From the input and output waveforms can be seen that the output takes time to start oscillating and to reach the appropriate gain. Also the input and the output voltage and current are slightly out of phase. This is due to the inductors and capacitors creating a leading or lagging network. The -6 dB bandwidth of the IF amplifier ranges from 3.7 MHz to 4.3 MHz with an adjustable voltage gain. However the carrier signal bandwidth, which ranges from 3.95 MHz to 4.05 Mhz, varies only -0.1 dB relative to the peak. Like the microphone amplifier, also the IF amplifier suffers from distortion when the input voltage amplitude becomes too high. The voltage gain collapses and the THD rises at about an input voltage amplitude of 50 uV. The input impedance ranges from 4700 Ω to 5200 Ω for the frequency range of 3.95 MHz to 4.05 Mhz. In figure 9.7 the step response of the IF amplifier can be seen. From the figure can be seen that as soon as the step activated, the system starts oscillating on the resonance frequency of the LC circuits and eventually becomes stable.

9.4 Feedback amplifier

In this section the simulations of the feedback amplifier will be done. The schematic can be seen in 7.1 and the components are listed in table 7.4.1. The Transient simulations were done with a 1 kHz source and 20 mV amplitude. The frequency sweep simulations were also done with a 20 mV amplitude source.

From the simulation shown in figure 9.4 is clear that our design goals are met. The output voltage was around 2.2V and the voltage gain is around 110. With the variable resistor in the feedback network the amplifier can be set to exactly the right output voltage if the input voltage is between 20mv and 40mv. The total harmonic distortion is also very low, around 1% for the used frequencies and the output waveform is a nice sinus without visible distortion. The THD starts to rise a lot when the input voltage becomes too high, the output voltage swing cannot keep up and the gain also collapses. The bandwidth requirement is also met since the -6 dB point for the output voltage is on 5 Hz and 5 MHz. The THD also stays very low for the whole bandwidth. The current from the current source is also very stable, it has a swing of around 3 μA. The input impedance of the feedback amplifier is also very high. It is important to note however that the gain of the feedback network derived in equation 7.2 should be 143 and instead is 110. This is expected since there is a leakage base current and limited open loop gain. In the step response in figure 9.7 it is visible that the feedback amplifier is a stable amplifier. The amplifier does not start to oscillate and the output converges to a finite value. From the simulations it is clearly visible that the design behaves according to the requirements and is usable in the FM transceiver

9.5 Sziklai class-AB

In this section simulations of the Sziklai class-AB used in the complete speaker amplifier seen in figure 8.10 with the component values seen in table 8.4.5. The transient simulations were done with a 1 kHz source and 2.2V amplitude, the Frequency sweep simulations were also done with 2.2 V amplitude input. No source resistance was modelled since the feedback amplifier has a buffer at the output and therefore a very low output impedance.

From the simulations shown in figure 9.5, 9.8 and figure 9.7 it is is visible that The current gain is very high, 470 at higher frequencies in the audible spectrum. The amplifier is a near perfect voltage follower and has a voltage gain of almost 1, as is expected from the analysis. The NPN and PNP transistors alternate each other very well, helping with a low THD and high efficiency. The input impedance is also high which is good for the transfer. The bandwidth is from 50 Hz to 15 MHz. Not the desired 20 Hz. This can be audible on a high quality speaker. The THD rises very fast for larger voltages since the amplifier output clips at larger voltages. For high frequencies the THD also becomes very high. This can be due to transistor imperfections. The efficiency is 57 % not a very competitive efficiency but a good result for the low distortion. The output power is 286 mW high is above the desired 250 mW, but not with a large margin.

9.6 Speaker amplifier

In this section simulations of the complete speaker amplifier can be seen. A topology of the full speaker amplifier can be seen in figure 8.11. The components are listed in table 8.4.5 and 7.4.1. The simulations were done with a 20 mV source. And the transient simulations were done with a frequency of 1 kHz and 20 mV amplitude.

From the simulations shown in figure 9.6 and figure 9.8 of the complete speaker amplifier is is clearly visible that the designs work together. Bandwidth is decreased to a range of 300 Hz. This is again audible on high quality speakers but also becomes an issue on lower quality speakers. The output power stays almost the same with an output of 276 mW and efficiency of 55.5 %. The power gain of the whole system is 75 dB. This is obtained by multiplying the voltage and current. This gain is very high but that is to be expected since the input impedance of the speaker amplifier is very high and the input very low. The THD is also still very low with the design combined. It is important to note that the system does need a bit of start up time, this is visible in the current waveform. The system is also stable as can been seen in the step response 9.7. The complete amplifier does need more time to settle after a step input.

9.7 Improvements

Since there was a finite amount of design time there are still improvements that could have been implemented. The microphone amplifier could have been designed in the same manner as the feedback amplifier to eliminate distortion for higher amplitude input voltages. The same holds for the IF amplifier. The feedback in the speaker amplifier is taken from the input of the Sziklai class-AB. It would have been better to have a feedback network from the output of the speaker amplifier to the input of the speaker amplifier, since there is still an amplifier without feedback in this design. The power efficiency and output power could also have been improved if the supply voltage was not center tapped and the gain of the input voltage had been boosted. Because a lot of the group designs changed frequently over time, it was hard to design for specific goals. Time and effort could have been saved, if the groups could have been in agreement faster about design choices. An extra difficulty in establishing these design choices was the lack of understanding of the modules. Each group had to research the module and this made it difficult to set realistic goals from the beginning.

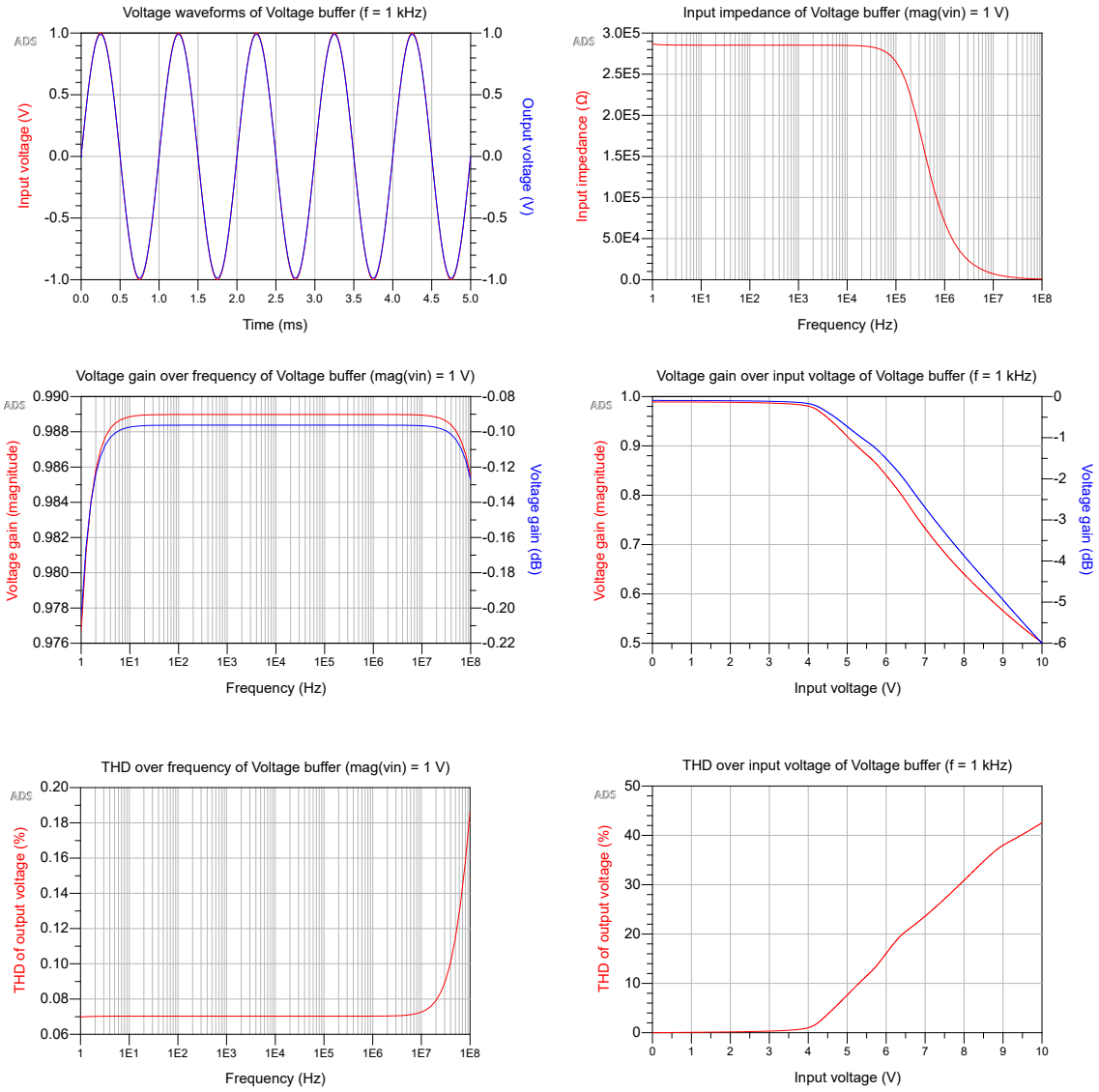

Figure 9.1: Simulation results of the Voltage buffer.

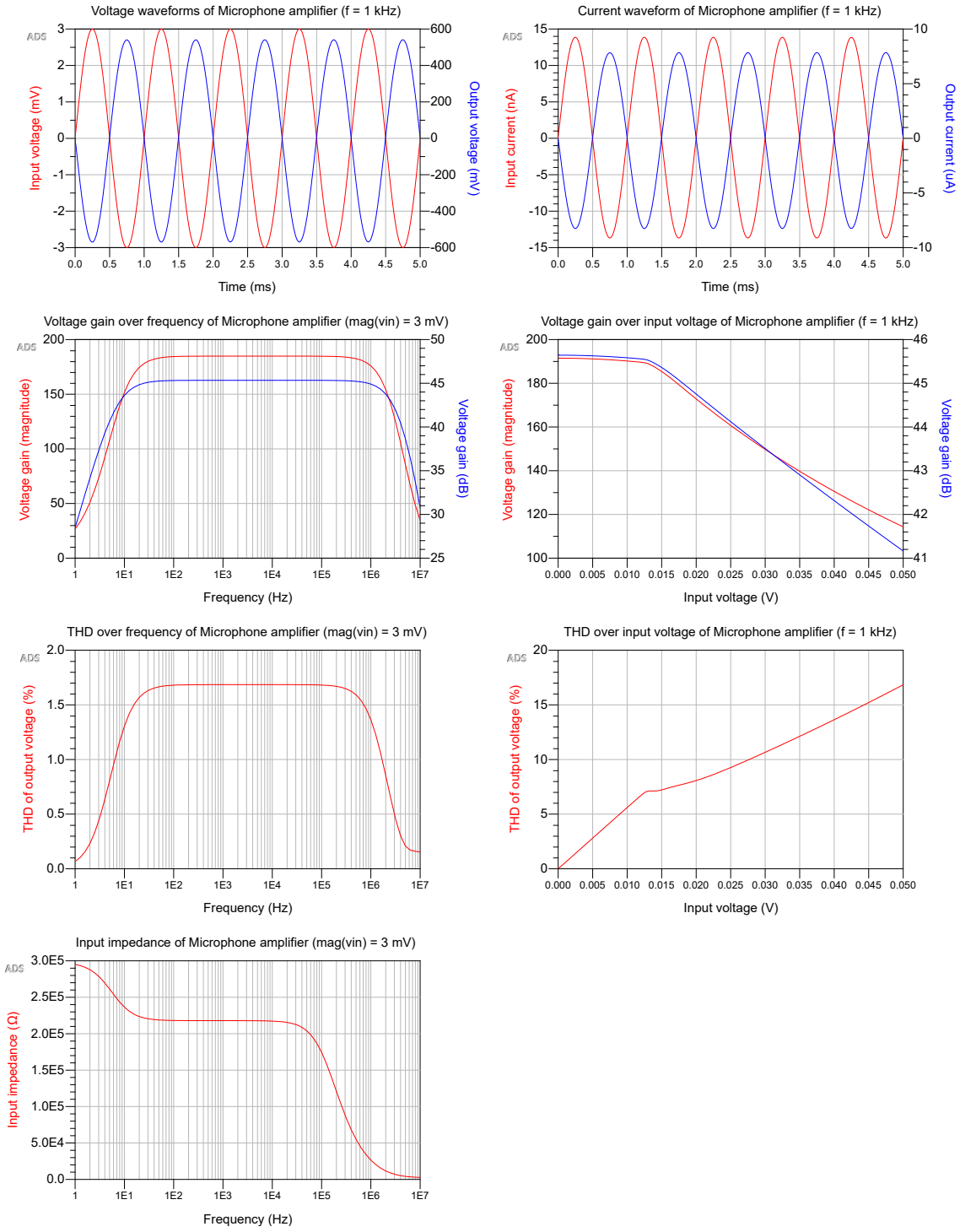

Figure 9.2: Simulation results of the Microphone amplifier.

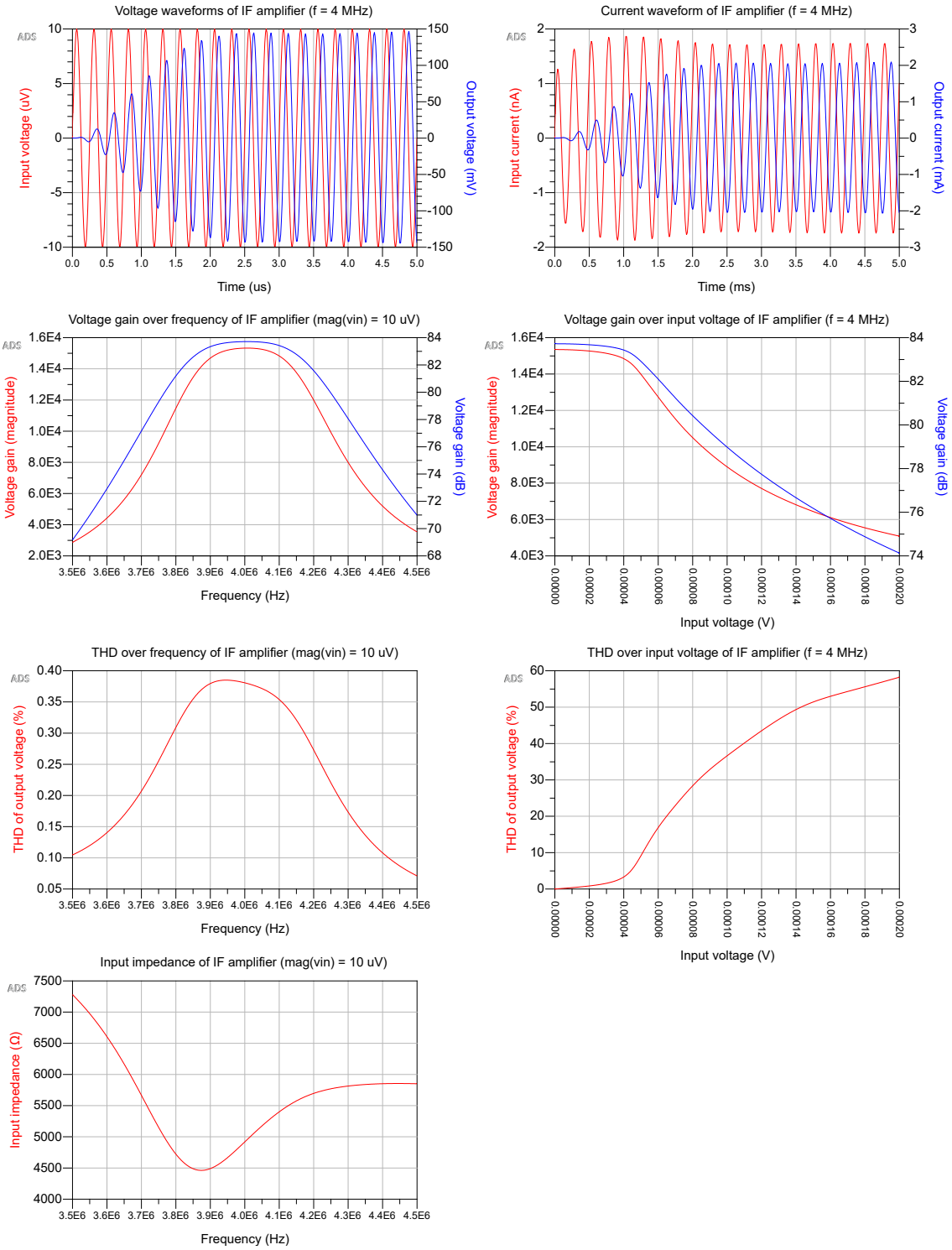

Figure 9.3: Simulations results of the IF amplifier.

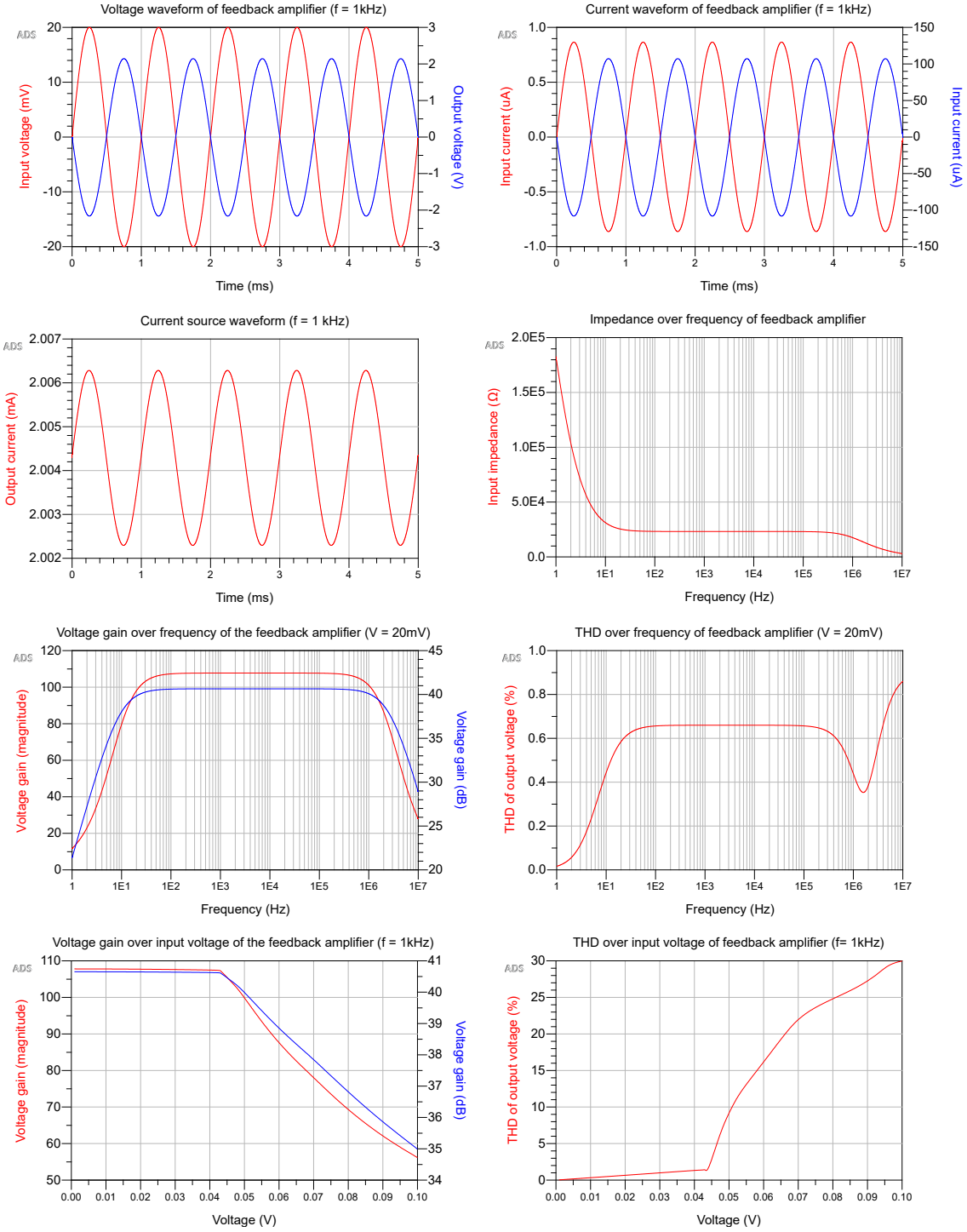

Figure 9.4: Simulations of the feedback amplifier

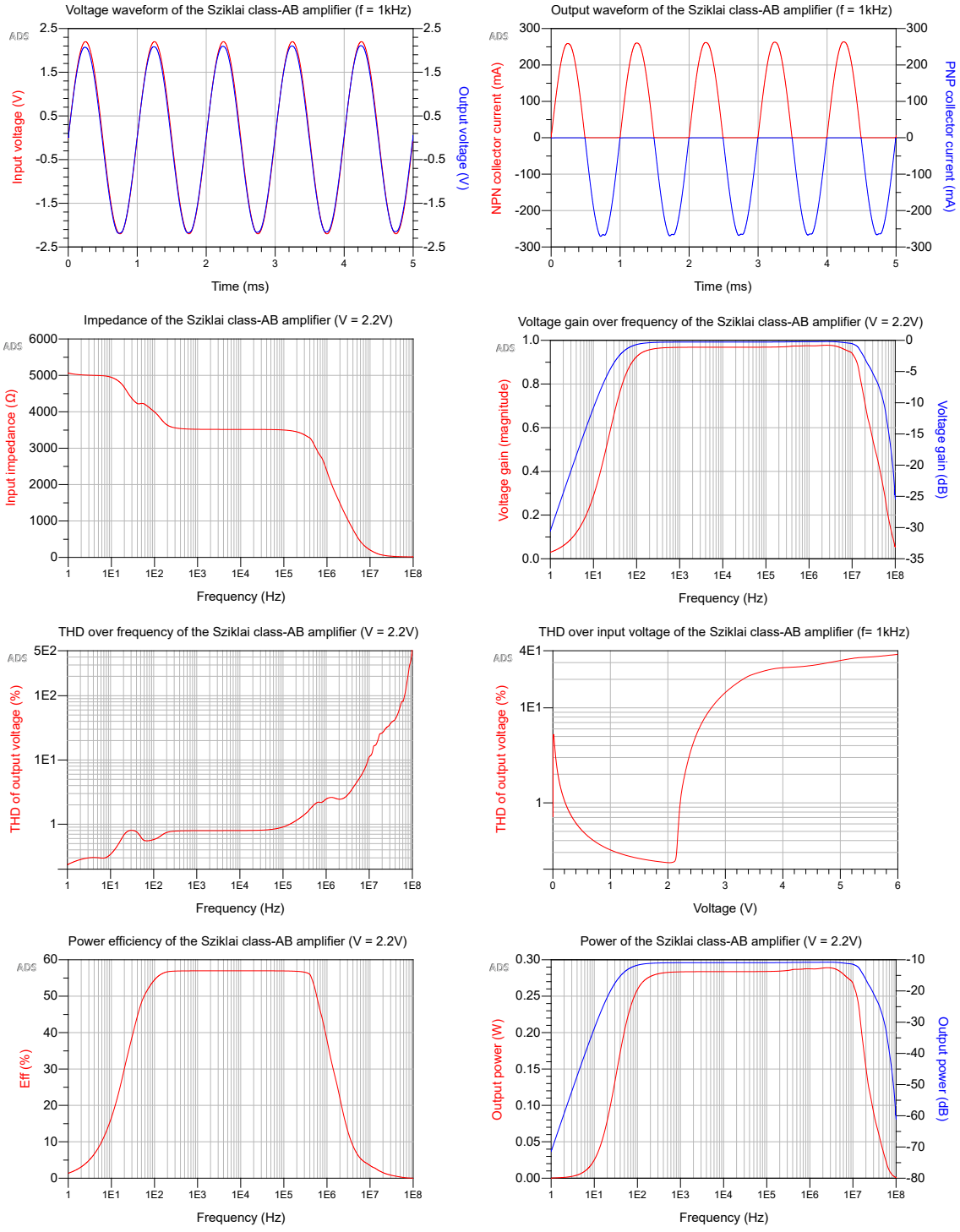

Figure 9.5: Simulations of the Sziklai class-AB amplifier

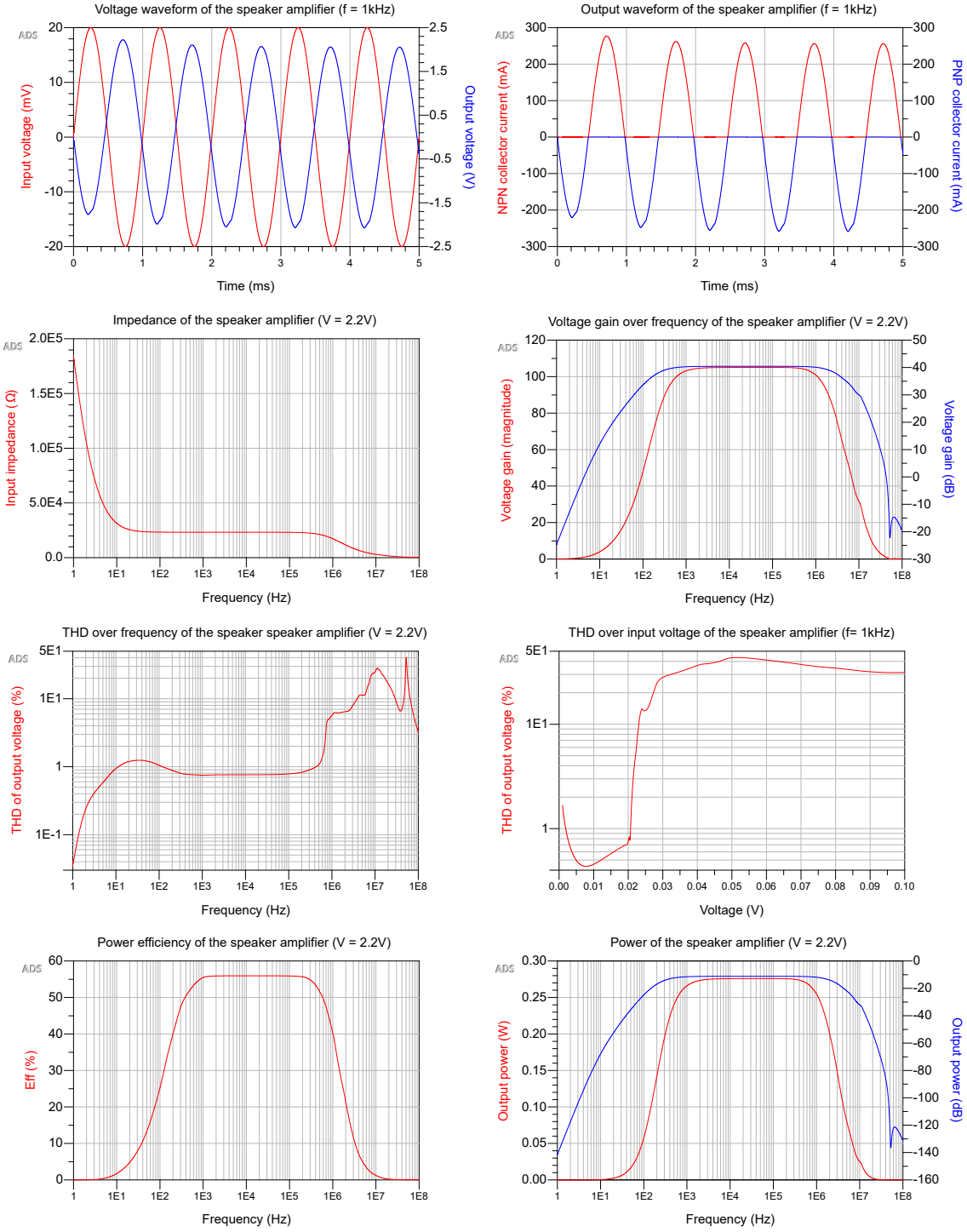

Figure 9.6: Simulations of the speaker amplifier

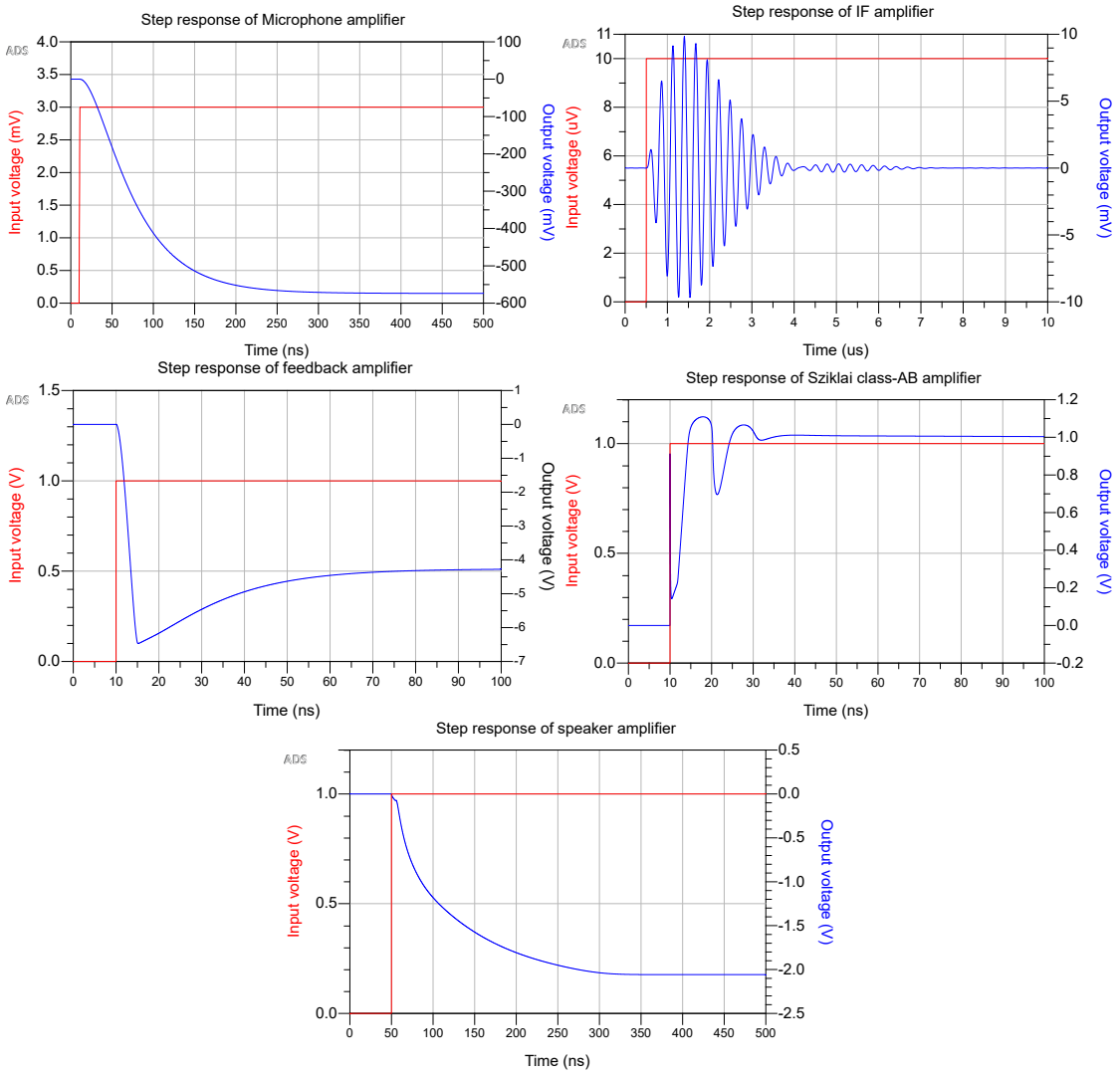

Figure 9.7: Step response of the amplifiers

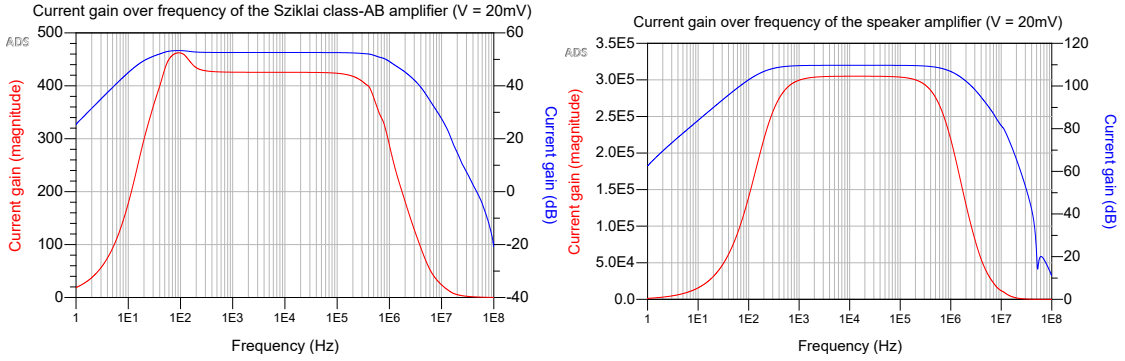

Figure 9.8: Current gain of the Sziklai class-AB and speaker amplifier

Chapter 10

Prototype

During the writing of this thesis the components to build the circuit prototypes were ordered, however the soldering of the circuits started after the hand-in deadline of this thesis. This thesis was therefore graded while most designs were not build yet and measurements were not done. The measurements were done after the thesis deadline and were shown in the thesis defence. In this chapter the prototype building and testing approach will be discussed. The prototype measurements results were added to this chapter after the thesis defence and completion of the project.

10.0.1 Building

For prototype building a prototyping PCB was used. A breadboard was considered for easily interchangeability of components but would not be sufficient for testing since it adds a lot of parasitic capacitance to the circuit, which will alter the behaviour of the circuit. Thus a prototyping PCB was chosen on which the components will be soldered, which adds building time, makes components hard to swap and might damage components.

10.0.2 Measurement setup

The measurements will be done in the Tellegen hall of the TU-Delft with the hardware that is available. The following measurement plan has been established.

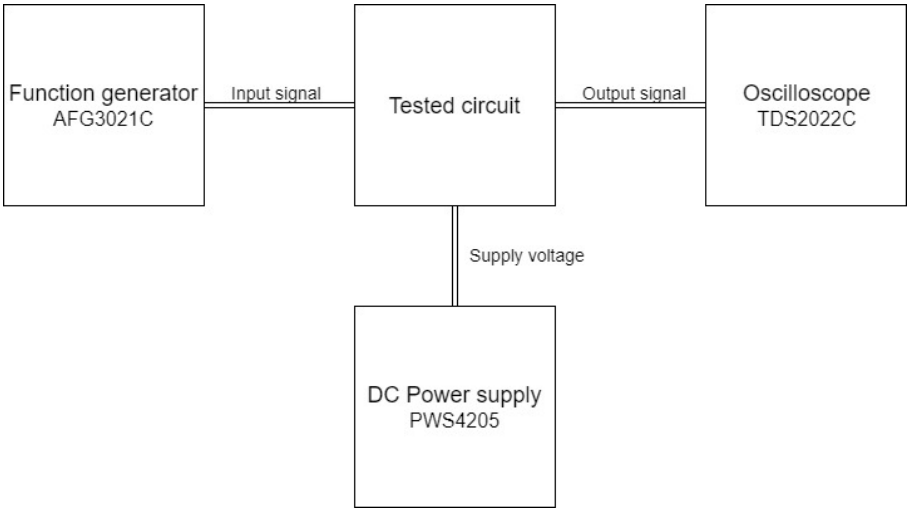

Figure 10.1: Setup for prototype testing

For each single amplifier discussed in this report, different input signals will be tested. In table 10.0.2 these signals and the supply voltages are shown.

Tested circuit	Input signal amplitude	Input signal bandwidth	Supply voltage
Microphone	Audio signal	20 Hz - 20 kHz	1.5 V
Microphone amplifier	1 mV - 5 mV	20 Hz - 20 kHz	12 V
Intermediate frequency amplifier	10 uV	3.95 MHz - 4.05 MHz	12 V
Feedback amplifier	10 mV - 40 mV	20 Hz - 20 kHz	12 V
Sziklai class-AB amplifier	1 V - 3 V	20 Hz - 20 kHz	6 V

Table 10.1: Prototype test signals.

For the next test the microphone amplifier will be adjusted to have a suitable gain for the microphone output voltage. A simple resistive voltage divider is also needed to bias the microphone and let both modules work on the same supply voltage. The Feedback amplifier gain will also be adjusted depending on the output signal of the detector and maximum voltage swing of the Sziklai class-AB amplifier. After these tests are done and the modules behave similar to the simulations, the amplifiers will be connected to other stages in the FM transceiver and new tests will be conducted. These next tests will be set up according to which modules work properly and therefore there is no point in already planning these measurement.

10.0.3 Prototype testing results

In this section the results of the prototype measurements will be discussed. This section was added after the thesis defence and completion of the project.

Microphone amplifier

The created prototype of the microphone amplifier was measured in the following ways. The linearity of the gain was tested by applying a range of voltages to the input of the circuit, thereby measuring the output voltage. The input voltage was increased until the output signal started clipping. For this measurement an input signal frequency of 1 kHz was used. To test the bandwidth of the circuit, a frequency sweep from 1 Hz to 20 kHz was applied to the input signal of the circuit. For this measurement an input voltage was used of 10 mV. Results of this measurement were captured on video and shown in the thesis defence. It showed a linear response on the tested bandwidth. Finally a Fourier analysis was done on the output signal, using an input signal of 1 kHz and 10 mV.

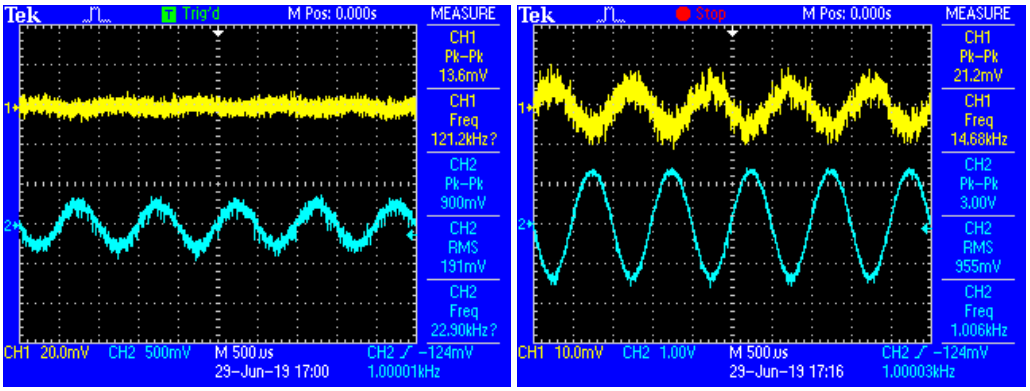

Figure 10.2: Input voltage (yellow) and output voltage (blue) during microphone amplifier voltage sweep (left 2 mV pk-pk input, right 10 mV pk-pk input)

In figure 10.2 and figure 10.3 the measured input and output voltages during the voltage sweep can be seen. The right measurement in figure 10.3 shows that the circuit starts clipping at too high of an input

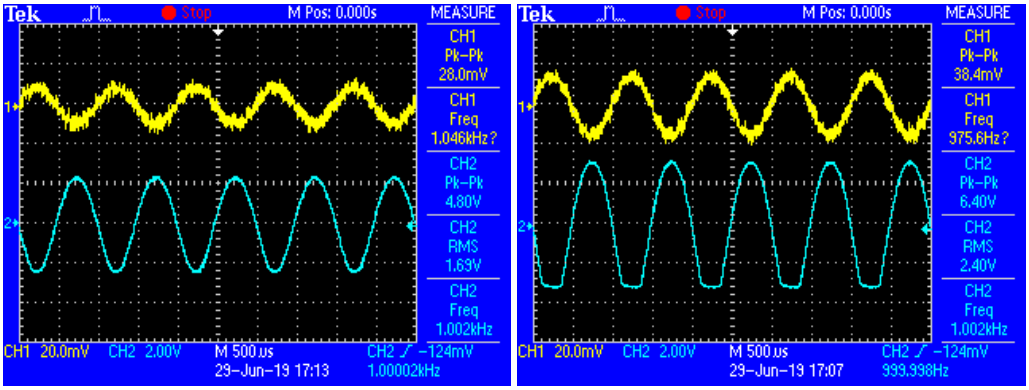

Figure 10.3: Input voltage (yellow) and output voltage (blue) during microphone amplifier voltage sweep (left 18 mV pk-pk input, right 30 mV pk-pk input)

voltage. The 2 mV pk-pk input gives an output of 900 mV pk-pk which comes down to a gain of 450. The 10 mV pk-pk input gives an output of 1.2 V pk-pk which comes down to a gain of 120. The 18 mV pk-pk input gives an output of 4.2 V pk-pk which comes down to a gain of 233. These measurment results do not show a linear gain, which was partly expected from the simulation results of figure 9.2.

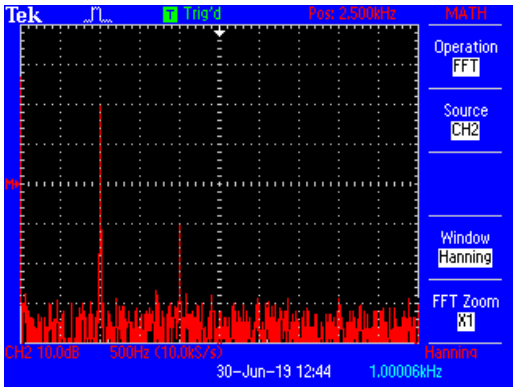

Figure 10.4: Fast Fourier Transform of output signal with 1 kHz input signal and pk-pk voltage of 10 mV

In figure 10.4 the fast fourier transform (FFT) measurement result can be seen. From this figure can be seen that the fundamental tone of 1 kHz is clearly present as well as the 2 kHz harmonic. Anything higher is not present in the measurement which means there is little to no harmonic distortion.

Intermediate frequency amplifier

The prototype of the intermediate frequency amplifier could not have been made functional before the time limit of the thesis defence. No meaningful data could be measured from the prototype and therefore none is included in this section.

Feedback amplifier

After the feedback amplifier was assembled it was measured according to the design specifications. A function generator applied a 20mv amplitude signal on the prototype and the output was measured with an o oscilloscope. To ensure the amplifier worked on the whole bandwidth a sweep of 20Hz to 20kHz was done. The maximum gain was also determined by lowering the input voltage and increasing the output signal until it clips. The measurements can be seen in figure 10.5 and 10.6.

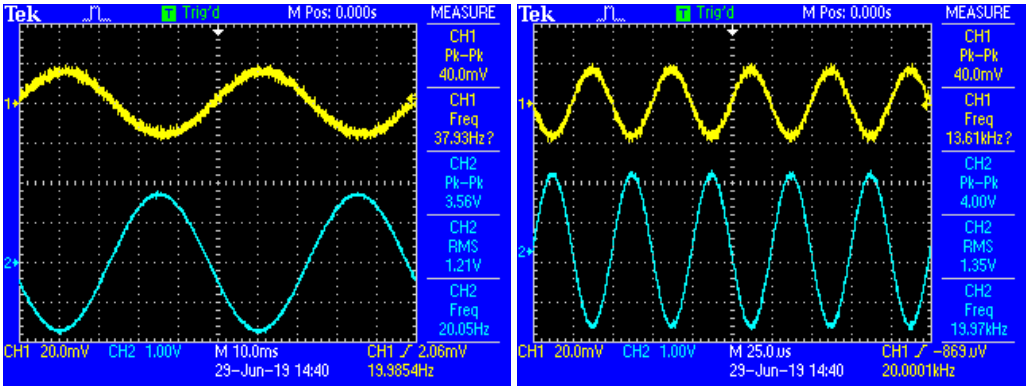

Figure 10.5: Bandwidth measurements for feedback amplifier prototype

From the measurements in figure 10.5 it is visible that the amplifier has a linear gain of 100 on the whole bandwidth it was designed for. This is expected since the simulations show the same result for an even broader bandwidth.

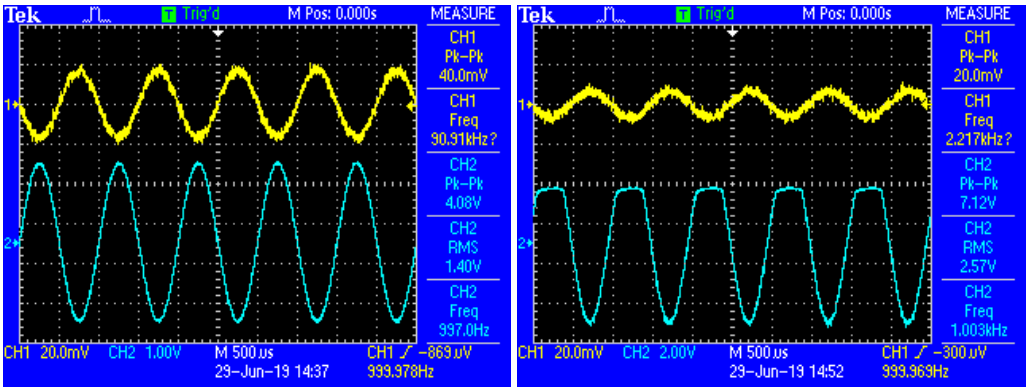

Figure 10.6: Gain measurements for feedback amplifier prototype

From the measurements in figure 10.5 it can be seen that the amplifier can delivered a lot more gain than 100, A gain of 350 was reached before it started to clip and the bottleneck of the amplifier was the clipping of the output.

Class-AB amplifier

The class-AB amplifier was assembled and measured in the following way. First a bandwidth measurement was done for the expected input voltage. This was done with a sweep in order to see if the amplifier showed unexpected behaviour for a frequency in the designed bandwidth and with two separate measurements on 20Hz and 20kHz. Next a measurement was done for the maximum output voltage. The measurements can be seen in figure 10.7 and 10.8.

For the measurements in figure 10.7 It can be seen that the amplifier is a good voltage follower at 20kHz but at 20Hz the amplifier weakened the signal a lot more. The Bandwidth is therefor a bit smaller than designed for.

For the measurements in figure 10.8 the maximum output voltage can be seen. With a higher input voltage of about 5V pk-pk, which the feedback amplifier can deliver, an output voltage of 4,7V was reached. This is close to the simulations and this also makes sure more power can be delivered to the speaker.

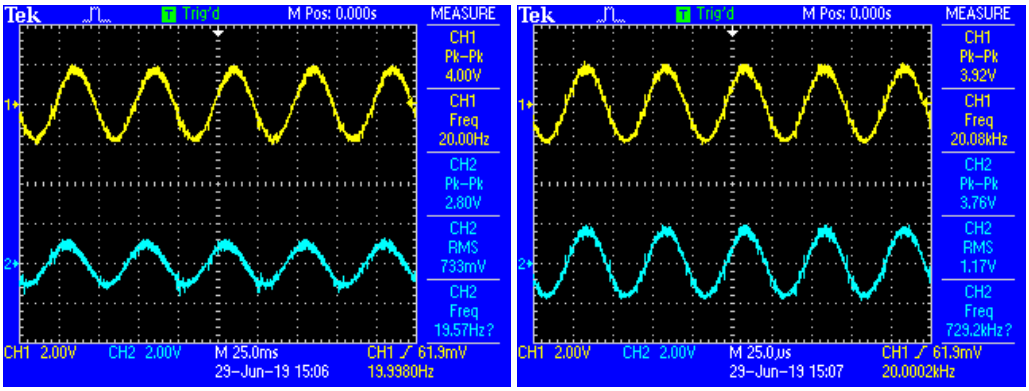

Figure 10.7: Bandwidth measurements for class-AB amplifier prototype

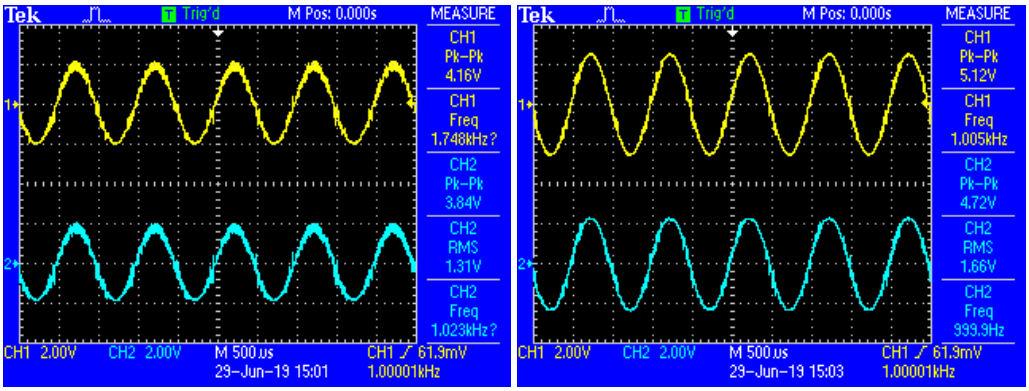

Figure 10.8: Gain measurements for class-AB amplifier prototype

Chapter 11

Conclusion

In conclusion almost all design requirements for all designs are met. The voltage buffer shows stable voltage following characteristics. The microphone amplifier provides more than minimum required voltage gain, which is steady across the bandwidth of operating. However it adds significant distortion for higher input voltages. The intermediate frequency amplifier also provides enough and steady gain for the intermediate frequency band and filters the information signal. This results in a very low distortion percentage, although like in the microphone amplifier, the IF amplifier adds distortion for higher input voltages. The speaker amplifier has a high enough power gain to power a small speaker. Non of the modules add a lot of distortion to the signal within the bandwidth and input voltage range of operation. Only the bandwidth of the speaker amplifier did not meet the design requirement but this does not break the transceiver, it only limits the performance. The prototype has not been tested in real life and a final conclusion about the complete system could therefore not be drawn. However a plan has been setup to create and test the prototype in the near future which will be discussed during the defence of this thesis. The complete transmitter combined with the modules of the other groups is shown in figure 11.1 and the complete receiver is shown in figure 11.2

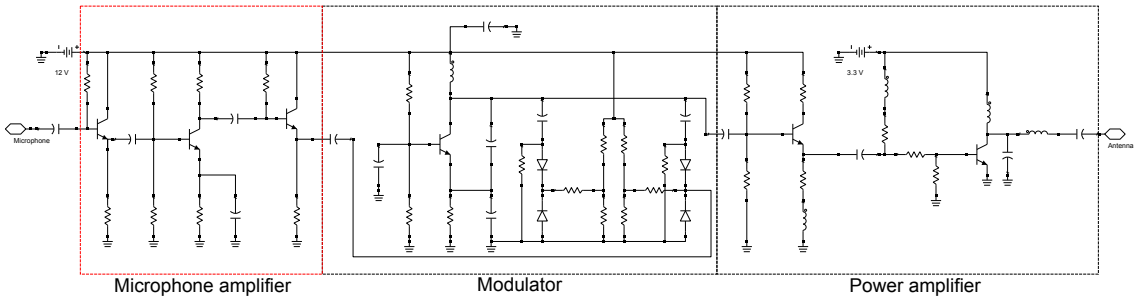

Figure 11.1: The final transmitter circuit

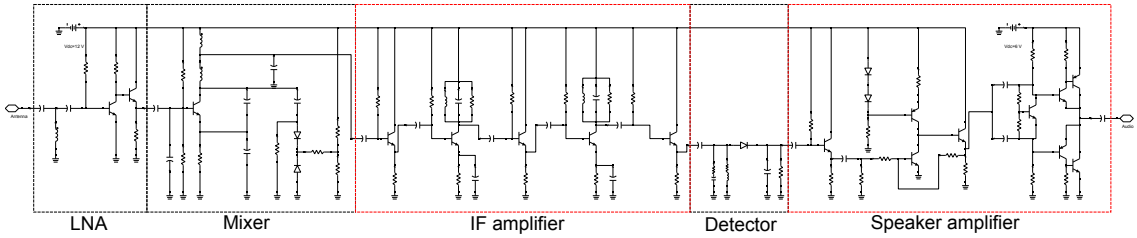

Figure 11.2: The final receiver circuit

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