High-Performance Class-D Audio Amplifiers

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High-Performance Class-D Audio Amplifiers

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Contents

Chapter 1

Introduction

The design of amplifiers began in the early 1900s with the advent of vacuum tubes, and then exploded with the invention of the transistor in 1947. Today, advances in semiconductor manufacturing technology have led to the widespread use of amplifiers, commonly realized as Integrated Circuits (ICs), in electronic systems to amplify signals with frequencies ranging from DC to hundreds of GHz. Among these, audio amplifiers are particularly prevalent in various applications.

The main objective of an audio amplifier is to boost the amplitude of an incoming electrical input signal and deliver a larger signal, with more power to a *loudspeaker*, or more simply, a speaker. The required output power is determined by the end application, and can vary considerably, as shown in Figure 1.1 for several typical applications. From

Figure 1.1: Typical total output power requirements for some applications.

earphones, which require just a few milliwatts, to stadium loudspeakers, which can consume tens of kilowatts, the range of output power levels is huge. Depending on the required power levels, signal amplification can be attained by using a single audio amplifier IC or a module consisting of several ICs and/or discrete components.

1.1 High-Fidelity Audio Amplifiers: Applications and Specifications

The generic block diagram of an audio system is shown in Figure 1.2, together with the associated signal chain. The power required by the various sub-systems is derived from a battery, or the mains, by a power supply unit, together with a number of voltage regulators. Since audio signals are often stored and processed in the digital domain, a digital signal processor (DSP) and a digital-to-analog convertor (DAC) are often parts of the signal chain. The speaker itself can be of different types, as will be discussed in Section 1.3, and varies not only in its absolute power rating, but also in other electrical characteristics. It is either connected to the amplifier directly, or through a network of passive filters and damping circuits.

The architecture of an audio amplifier is mainly determined by considerations such as cost and size, output power, energy efficiency, and audio fidelity, all of which are influenced by the intended application. These considerations will be discussed in the following sections.

1.1.1 Cost and Size

System cost and size reduction is a major goal in the design of audio power amplifiers. This is particularly important in high volume applications such as automotive

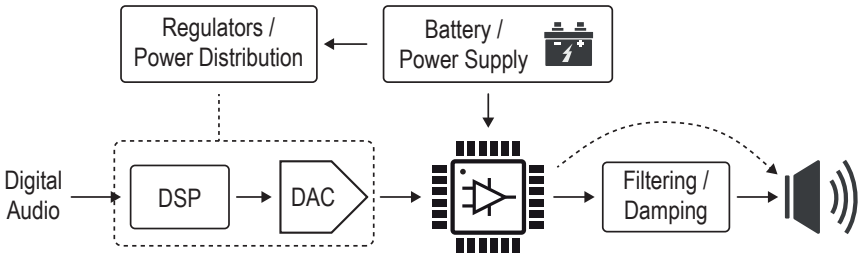

Figure 1.2: Generic block diagram of an audio-amplifier system.

infotainment, since high-end family vehicles may have up to 20 interior speakers, together with the corresponding number of amplifiers [1]. Given the premium on cost and size in automotive applications, it becomes crucial to reduce system size and lower the overall bill-of-materials. This entails minimizing the use of off-chip components, such as passive filters, damping networks, decoupling capacitors, etc; or using cheaper variants. These considerations have driven the development of single-chip audio amplifiers, which integrate multiple functions to save space and reduce costs. Similar constraints are applicable to commercial-grade audio amplifiers, such as those used in portable Bluetooth headphones or in hi-fi stereo/ multi-channel home theatre systems. Despite the inevitable cost and size trade-offs, however, preserving audio performance is non-negotiable, and adhering to target application specifications remains paramount

1.1.2 Power Consumption and Efficiency

Due to internal loss mechanisms, the power dissipation of an audio amplifier consists of the power delivered to the load as well as the power consumed by the amplifier itself. Reducing the latter is one of the main design goals of amplifier designers. In portable devices such as laptops and cell phones, amplifier power is derived from a battery, and so reducing it increases battery life. More fundamentally, much of the power lost in an amplifier results in self-heating. While this is less significant in low-power portable applications, in high-power amplifiers this can be severe, and may require bulky and costly heatsinks to keep operating temperatures within acceptable limits.

Two important metrics used to evaluate audio amplifiers are their power efficiency and idle power consumption. Power efficiency is defined as the ratio of the useful output power delivered to the speaker load to the total power consumption of the system and is important at high output power levels. At lower power levels, idle power consumption, defined as the power consumption with zero input, becomes more meaningful. This is because most audio signals have a high crest factor, between 7–25 dB [2], [3], and thus swing from low to mid amplitudes, rarely reaching full-scale power levels.

1.1.3 Electromagnetic Interference

Electromagnetic emissions from the high frequency switching activity of ICs is unavoidable, and results in electromagnetic interference (EMI) when not addressed. In small enclosures such as automobiles, EMI problems are exacerbated by the need for various systems to communicate with each other, either wirelessly or via long interconnecting cables. Audio amplifiers, specifically the switching Class-D variants (discussed later in Section 1.2), are often major EMI aggressors, since the cables connecting them to the battery and speakers are often unshielded and untwisted due to cost and weight constraints. Limiting EMI becomes critical to ensuring safety and reliability, and hence must be addressed during the design phase of the amplifier. Several

test standards of EMI limits exist, with automotive variants, like [4] and [5], being some of the most stringent.

In comparison, EMI issues in consumer or portable applications are relatively easy to tackle due to shorter interconnects, fewer audio channels, and lower speaker power ratings. Furthermore, the EMI test standards are themselves more relaxed due to the lower risks and less severe consequences of EMI in such applications [6].

1.1.4 Audio Fidelity

In addition to the system design aspects described in preceding sections, other parameters that pertain to the audio fidelity of an amplifier are its dynamic range (DR), linearity, and power supply immunity.

The DR of an amplifier is defined as the ratio between its maximum output signal and its noise floor, and is often expressed in terms of its peak signal-to-noise ratio (SNR). This metric is crucial as it quantifies the span between the quietest and the loudest sounds that the amplifier can reasonably reproduce. Most modern audio amplifiers boast a DR greater than 110 dB, with higher-end amplifiers and DACs even approaching the limits of human hearing (~130 dB) [7].

In contrast, an amplifier's nonlinearity is more of a concern for large amplitude inputs, where distorted output components are more audible and often unpleasant. Nonlinearity is usually quantified by various signal distortion metrics such as Total Harmonic Distortion (THD), Inter-Modulation Distortion (IMD), etc. The noise and distortion performance of an amplifier is often combined into a single convenient metric, the Total Harmonic Distortion and Noise (THD+N).

An amplifier's power supply immunity, represented by its Power Supply Rejection Ratio (PSRR), is also important, as the output of its power supply will always exhibit some variation due to the varying power consumption of its different subsystems or of the amplifier itself. Without adequate PSRR, the various signal and noise components in the supply line can also lead to signal intermodulation distortion and/or a poor noise performance.

1.2 Amplifier Classes

One of the most important metrics of audio amplifiers is their power efficiency, which is primarily determined by their output stage. On this basis, they can be broadly divided into moderately efficient (linear) and highly efficient (switching) amplifiers.

1.2.1 Linear Amplifier Classes and Variants

Linear amplifiers such as Class-A/ AB/ B amplifiers have efficiencies ranging from 33% to ~78% [8]. From a cost perspective, a major benefit of these classes of amplifiers is

the limited number of off-chip passive components they need. Except for a few supply decoupling capacitors, their outputs can be directly connected to a speaker. Additionally, the lack of any high frequency switching activity also makes them the best choice in terms of EMI.

However, the moderate efficiency of linear amplifiers results in significant amounts of wasted power and self-heating. This is not a major issue in low power applications such as driving headphones or speakers with impedance $> 32\Omega$, since the overall power consumption and, thus, the heat generated is also low. However, for low impedance (2Ω to 8Ω) speakers, large heatsinks are often required to limit die temperature and prevent over heating, thereby increasing the overall system size and cost.

1.2.2 Switching Class-D Amplifiers

Compared to linear amplifiers. the biggest benefit of switching, or Class-D amplifiers (CDAs), is their higher power-efficiency, and therefore, lower power consumption and heat generation for the same output power level. This drastically reduces the need for heat sinks, which in some cases, can be eliminated entirely. It also makes CDAs well-suited for use in portable applications and in battery-operated devices such as tablets, smartphones, and laptops.

A CDA derives its superior efficiency from its output stage, shown in a simplified form in Figure 1.3 (a). This consists of low-ohmic, high-power switches (in red) which can switch the output between bipolar supplies ($\pm V_{SUP}$) and thus deliver large currents to the load. The low on-resistance of the output switches ensures low I^2R losses, resulting

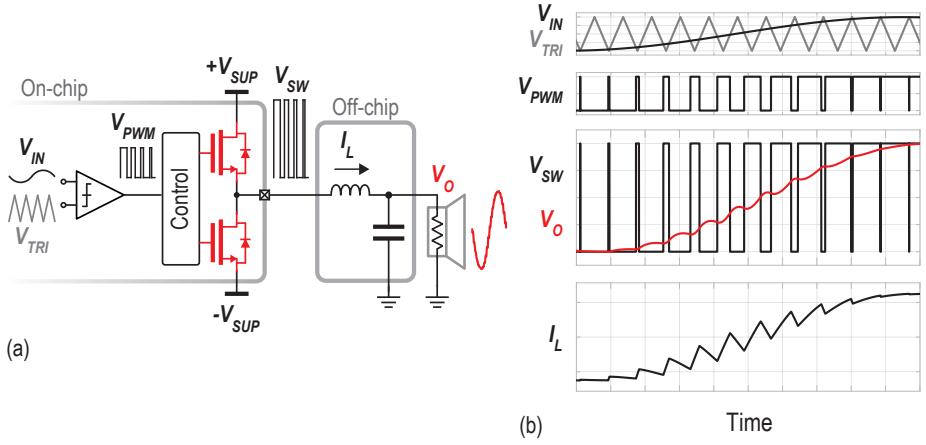

Figure 1.3: (a) Simplified block diagram of a class-D PWM modulated output stage, and (b) time-domain waveforms of the different signals.

in high efficiency. While different modulation schemes exist to control the switches, the most predominantly used one is pulse width modulation (PWM), as illustrated in Figure 1.3 (b), in which an audio signal (V_{IN}) is compared with a high-frequency triangular carrier (V_{TRI}) to generate a PWM signal (V_{PWM}). In the time-domain, the audio information from the input (V_{IN}) is linearly mapped to the duty-cycle of each pulse in the output pulse-train (V_{SW}).

However, the switching activity of the output stage can also be problematic. While the switching signal V_{SW} contains the audio information and can directly be used to drive the speaker (and is often done), it also contains high-frequency intermodulation components at the PWM frequency (f_{PWM}) and its harmonics [9]. Although inaudible, these high-frequency components are undesirable due to the EMI they create, especially in the radio AM band. Therefore, additional passive LC filtering is often required to suppress them, increasing system cost and size. In addition to the EMI issue, the idle power consumption of PWM Class-D output stages is usually larger than that of their Class-AB counterparts. This is because their switching activity means that the gate capacitances of their output devices, which are generally large for low on-resistance, must be repeatedly charged and discharged even when there is no input signal.

Lastly, the output stage of a CDA has poor PSRR and is highly non-linear. Since the output stage periodically connects the load to the supply rails, perturbations in the supply are directly reflected at the output, resulting in poor PSRR. Their non-linearity is caused by non-ideal output pulses, which in turn are due to amplitude and timing errors such as signal-dependent delays, dead-time, signal-dependent IR drops, etc [10]. To suppress these nonidealities, most modern CDAs are used in closed-loop architectures, which improves their linearity and PSRR.

1.3 Speaker Variants

The electrical properties of the speaker that an amplifier is expected to drive will greatly influence its design. While various parameters such as size, efficiency, and output sound pressure level (SPL) define the cost and quality of the speaker, the most important parameter, for the design of audio amplifiers, is its electrical impedance. This in turn is primarily determined by the type of transducer used to convert electrical signals into acoustic sound pressure waves, as well as its mechanical enclosure. Of the different types of speakers, this thesis focuses on optimizing the performance of CDAs for electrodynamic and piezoelectric speakers, whose characteristics are discussed below.

1.3.1 Electrodynamic Speakers

These are the most commonly used speakers in audio applications. Being a very mature technology, they achieve the best acoustic performance and are relatively inexpensive to manufacture in bulk. An electrodynamic speaker consists of a permanent magnet

and diaphragm attached to a movable voice coil, as shown in Figure 1.4 (a). Passing an AC current through the coil then generates a proportional Lorentz force on it, creating mechanical vibrations on the diaphragm, and therefore, sound pressure waves. However, the packaging required for good acoustic quality and proper protection from the environment, as well as the magnet itself, can get quite bulky.

The impedance of an electrodynamic speaker is frequency dependent, and often exhibits resonant modes of vibration due to its mechanical construction. Most high fidelity (hi-fi) speakers are tailored for use in certain audio frequency bands. As examples, the impedance characteristics and the output sound pressure level are shown in Figure 1.4 (b) for a woofer, mid-range, and tweeter respectively [11]–[13]. However, despite their complex impedance and natural resonances in the audio band, for most practical design purposes, it is sufficient to electrically model these speakers as a simple resistive load (R_L) or as a combination of an inductive and a resistive load (R_L+ L).

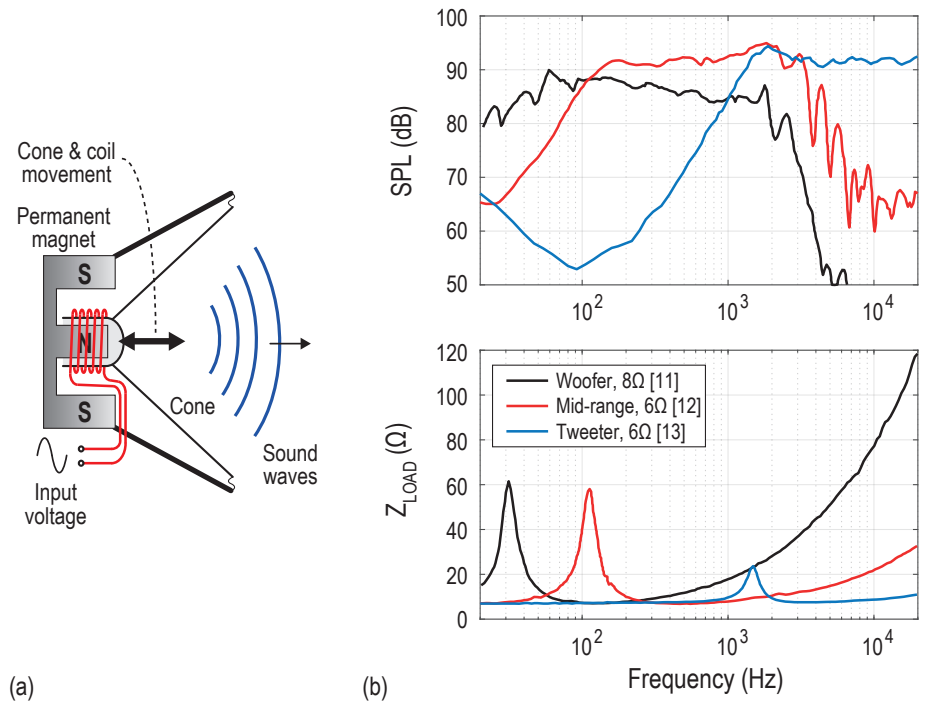

Figure 1.4: (a) Simplified structure and operating principle of an electrodynamic speaker and (b) the output sound pressure level and actual impedance of three commercially available speakers.

1.3.2 Piezoelectric Speakers

The operation of Piezoelectric speakers is based on the inverse piezoelectric effect, wherein, an applied voltage or electric field across a film of piezoelectric crystal or ceramic causes it to deform mechanically, as shown in Figure 1.5 (a). If an AC signal is applied, the resulting deformation can be harnessed to generate pressure waves and produce sound. Traditionally, piezoelectric speakers have been less favored in mainstream hi-fi applications due to the superior sound quality of more established electrodynamic speakers. However, recent advancements have led to more compact designs with a thin form factor, as shown in Figure 1.5 (b). Together with the improved audio quality of some of the newer variants, piezoelectric speakers have started gaining popularity for use in devices with thickness constraints, such as cell phones, tablet computers and flat-screen TVs [14], [15].

The output sound pressure levels achievable with newer piezoelectric speakers can be

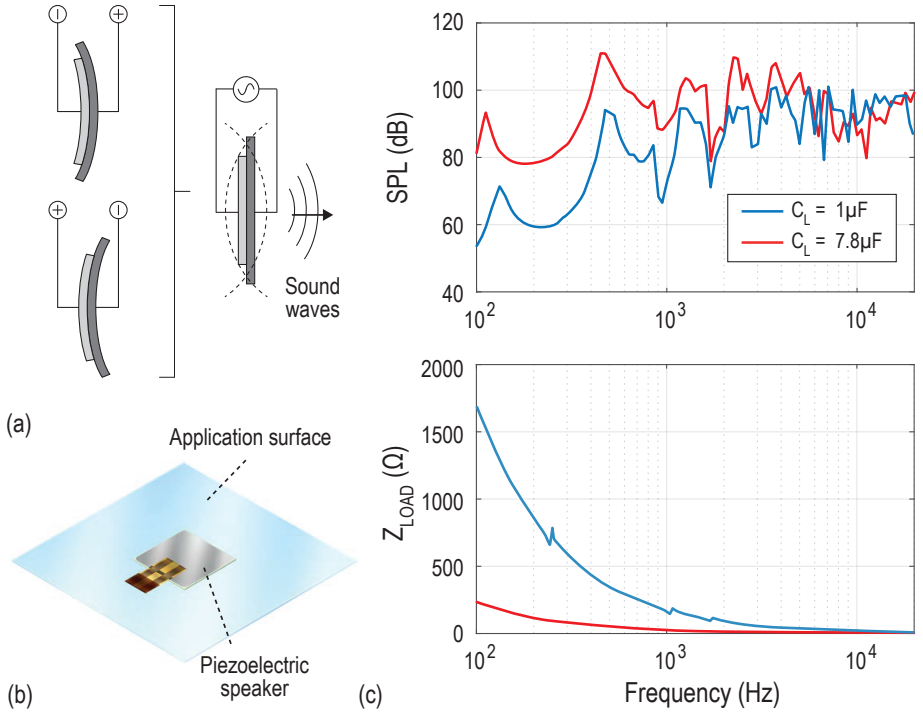

Figure 1.5: (a) Simplified structure and operating principle of a piezoelectric speaker; (b) a piezoelectric speaker from TDK (courtesy of [14]); and (c) the output sound pressure level and actual impedance of two commercially available speakers [14].

quite comparable to those of electrodynamic speakers, especially for frequencies above ~400Hz-1kHz), as shown in Figure 1.5 (c). However, unlike an electrodynamic speaker, the impedance of a piezoelectric speaker is highly capacitive, making it challenging to drive them with the large currents needed to create adequate sound pressure.

1.4 Research Direction and Thesis Objective

CDAs have overtaken Class-AB amplifiers as the preferred choice in most high-power audio applications. Their high power-efficiency enables the use of smaller heat sinks, providing system cost and size benefits. In terms of audio fidelity, they are comparable to Class-AB amplifiers, if not better.

However, the additional passive components needed to mitigate the inferior EMI performance of CDAs reduces the aforementioned cost benefits. To satisfy EMI standards, conventional output stages usually require bulky and costly inductors and capacitors to realize LC filters with low cutoff frequencies (f_{LC} between 20 and 40kHz). While architectural innovations such as the use of multi-level and multi-phase output stages improves the EMI performance of CDAs, they also increase cost, either due to the additional die area of the extra switches required and/or due to the even greater number of passive components [16]–[23]. A more recent approach to tackling EMI in a cost-effective manner involves modulating the input signal to higher switching frequencies. This allows the use of LC filters with higher f_{LC} for a similar degree of EMI suppression, which can then be made with smaller and cheaper components [24]. However, this approach may result in sub-par THD+N and idle power consumption due to the higher switching frequency and narrower pulse-widths.

When it comes to driving a piezoelectric speaker, the off-chip component count increases further due to the additional requirement of a series resistor along with the inductors and capacitors. This resistor, which damps the highly capacitive impedance of the speaker, inevitably not only adds to system cost and size, but also to the power consumption of the system [25], [26].

The objective of this thesis is to develop analog-input CDAs that can achieve high performance in terms of critical metrics such as power consumption and efficiency, EMI, audio fidelity, etc, with the minimum use of off-chip components, thereby ensuring a low system cost. Two prototypes, each for a different application and a different speaker type, are implemented to demonstrate these objectives. The first design is intended for a typical automotive application with an electrodynamic speaker. It is a CDA that satisfies the CISPR 25 EMI standard with a relaxed, and thus low-cost, LC filter (f_{LC} between 100 and 150kHz) while attaining high efficiency and linearity. The second prototype is intended for applications employing piezoelectric speakers. It shows the feasibility of a CDA to drive a capacitive load at high currents without an additional external damping resistor, while still achieving high linearity and low idle-channel power consumption.

1.5 Thesis Organisation

The rest of the thesis is organised as follows. Chapter 2 provides an overview of some of the circuit and architectural developments in CDAs, along with several modulation techniques and feedback topologies. Finally, new hybrid modulation and dual feedback architectures, aimed at reducing the overall cost of the IC and the system, are proposed.

Chapter 3 discusses the hybrid PWM-DSM modulation technique in detail, together with the design of a prototype IC capable of meeting the automotive CISPR 25 class 5 EMI mask in the AM band with relaxed filter requirements without sacrificing on linearity and other performance metrics.

Chapter 4 discusses in detail a dual feedback architecture for CDAs designed for piezoelectric speakers, and shows measurement details of a prototype CDA. It demonstrates that this architecture avoids the need for a power resistor when driving a piezoelectric capacitive load, while achieving high audio fidelity. Chapter 5 presents an improvement on the prototype of Chapter 4, in which an improved feedback chopping technique is proposed to extend the linear range of the amplifier for signals close to the full scale.

Chapter 6 concludes this thesis. A summary of the original contributions in the prototypes are provided along with a brief discussion of what can be done next.

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Chapter 2

Class-D Amplifier Architectures

Compared to other classes of amplifiers, CDAs derive their superior efficiency from their output stages, whose devices operate as low-ohmic switches, rather than as power-consuming current sources. Today, designers can choose between various output stage topologies, modulation schemes, and switching frequencies, with each offering different trade-offs between power consumption, efficiency, EMI performance, and system cost and size. In this chapter, some of the main circuit and architectural techniques used in modern CDAs will be discussed.

2.1 Output Stage and PWM Schemes

A widely used Class-D differential output stage is shown in Figure 2.1. Also known as an H-Bridge due to the arrangement of the switches, the speaker and filter network are connected between the two branches, in a so-called *bridge-tied-load* (BTL) configuration. Despite the need for two additional switches in comparison to the bipolar half-bridge

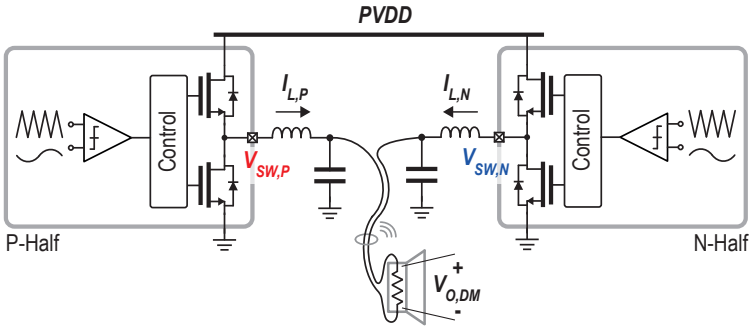

Figure 2.1: A typical full-differential Class-D output stage with bridge-tied-load.

output stage discussed in Chapter 1 (Figure 1.3), an H-bridge offers significant advantages. It simplifies the power supply requirements by operating from a single supply, thus avoiding the need for a more expensive bipolar supply, not only making the system more efficient, but also reducing cost and design complexity. Additionally, the differential output of the H-bridge also improves electromagnetic interference (EMI) performance in comparison to the single ended output of the half-bridge. Moreover, an H-bridge allows each half to be driven by independently generated PWM signals, enabling the use of more flexible and efficient PWM schemes. Among them, fixed frequency AD-PWM and BD-PWM modulation schemes are the most commonly used due to their simplicity [1]. These schemes will be described in the following sections.

2.1.1 Fixed-Frequency AD/ BD - PWM

In AD modulation, the H-bridge shown in Figure 2.1 is operated in a fully differential manner, with the outputs of the two halves $(V_{SW,P/N})$ switching 180º out of phase, as depicted by the waveforms in Figure 2.2 (a). The differential mode (DM) output voltage $V_{SW,DM}$ $(= V_{SW,P} - V_{SW,N})$ then switches between two levels, denoted as ±1FS, where FS refers to the single-sided full-scale output voltage (PVDD), resulting in the largest step-size. The large step size of $V_{SW,DM}$ also results in a DM inductor current $I_{L,DM}$, with proportionately large ripple content. In the frequency domain, the large step-size and ripple content translate into large PWM tones and EMI at the carrier frequency f_{PWM} and its harmonics, as can be seen in the FFTs of $V_{SW,DM}$, $I_{L,DM}$, and the filtered output at

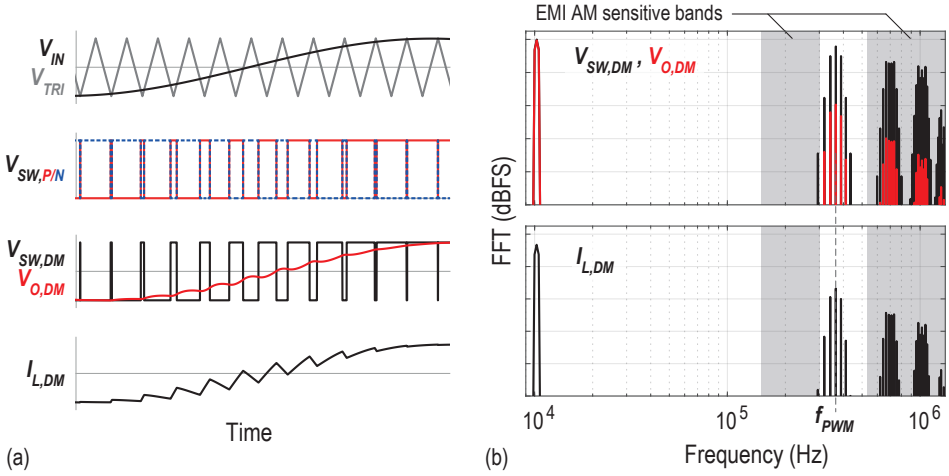

Figure 2.2: (a) Typical time-domain waveforms of an AD modulated PWM CDA; and (b) FFTs of $V_{O,DM}$, $V_{SW,DM}$, and $I_{L,DM}$, along with overlapping EMI sensitive bands.

the load- $V_{O,DM}$ in Figure 2.2 (b). It should be noted that the fully differential switching of AD modulation also results in a fixed common-mode level of 0.5FS (PVDD/2).

EMI is especially problematic when it falls in the AM band (535–1605 kHz). In AD modulated PWM CDAs, the carrier frequency (f_{PWM}) is often set between 300 - 500 kHz to avoid AM-band interference, as illustrated in Figure 2.2 (b). However, adequate suppression of the PWM harmonic tones, which still fall into EMI sensitive regions, is then required. As a result, LC filters are critical components of a CDA output stage, since they help supress the high- frequency DM/CM currents flowing through the cables and thus reduce EMI. However, the required LC filters often have low cutoff frequencies (f_{LC} between 20 and 40 kHz), making them bulky, and thereby leading to significant increases in system size and cost. Therefore, it is desirable to fundamentally reduce the switching activity of the output stage, by either decreasing the amplitude of the PWM components or optimizing the PWM frequency.

EMI due to differential switching can be lowered, by reducing the DM voltage step size, and therefore, the DM ripple current. This can be accomplished by using BD modulation. As illustrated in Figure 2.3 (a), each half of the H-bridge is independently modulated by 180º phase-shifted carrier signals. In this scheme, instead of switching directly between ±1FS every PWM cycle, the output stage creates an intermediate DM transition to 0FS, thereby effectively reducing the DM step size by half compared to AD modulation. For a given LC filter, this also reduces the DM ripple current and EMI generated by half. Furthermore, as can be seen from the waveforms and FFTs shown in Figure 2.3 (b), the PWM tones are present only at even harmonics of f_{PWM}, resulting in

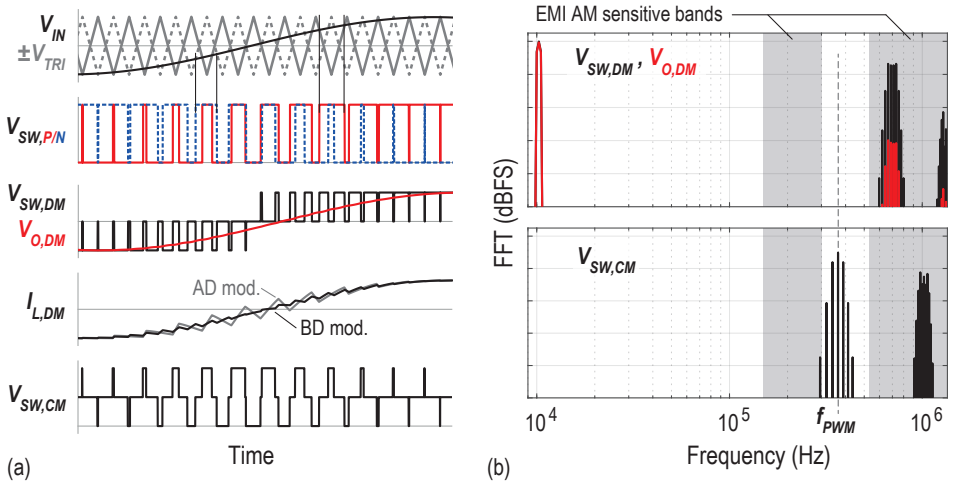

Figure 2.3: (a) Typical time-domain waveforms of a BD modulated PWM CDA; and (b) FFTs of $V_{O,DM}$, $V_{SW,DM}$, and $V_{SW,CM}$, along with overlapping EMI sensitive bands.

even lower high-frequency content at the output of the LC filter. BD modulation is often used in portable low-power applications, in which the use of an LC filter is avoided altogether [2].

However, unlike AD modulation, BD modulation is also associated with CM switching $V_{SW,CM}$ $[= 0.5(V_{SW,P} + V_{SW,N})]$, as illustrated in the time and frequency domain in Figure 2.3. CM switching becomes important when long speaker cables are used because these can act as antennas at high frequencies, exacerbating CM-induced EMI artefacts. Furthermore, with BD modulation, the CM components are present at f_{PWM}, making it less desirable in EMI sensitive applications. In contrast, since AD modulation maintains the CM voltage at a fixed voltage of PVDD/2 (0.5FS), it theoretically eliminates CM artefacts, making it more attractive in many cases.

2.1.2 Push-pull (Ternary) Modulation

When it comes to CM-induced EMI artefacts, Push-Pull (PP) modulation offers an advantage in comparison to BD modulation [3]–[6]. In PP modulation, unlike AD and BD modulation schemes, only one half of the H-bridge switches every PWM cycle depending on the on the polarity of the input signal. This is illustrated by the timing waveforms in Figure 2.4 (a), where the input (V_{IN}) and the carrier signals $(\pm V_{TRI})$ are used to generate the PP modulated output switching signals $(V_{SW,P/N})$, by following the relations given by Equation 2.1,

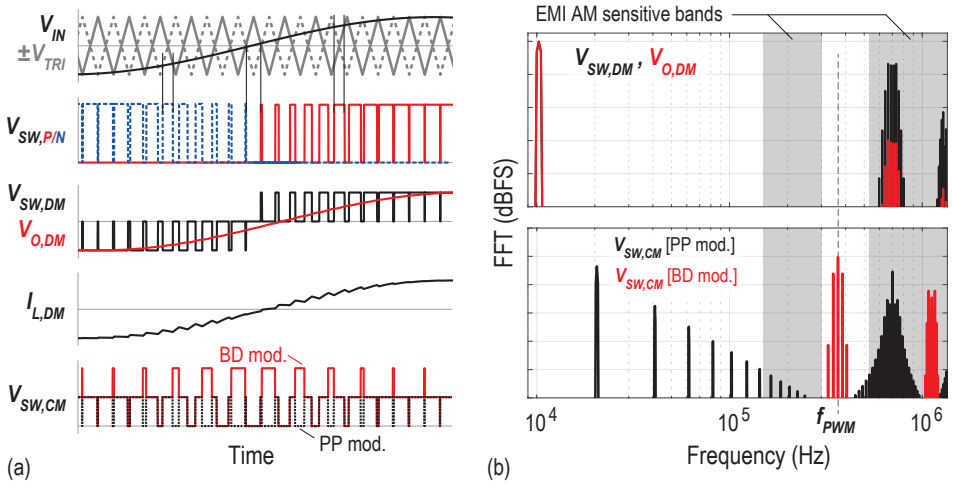

Figure 2.4: (a) Time-domain waveforms of a PP modulated PWM CDA; and (b) FFTs of $V_{O,DM}$, $V_{SW,DM}$, and $V_{SW,CM}$, along with overlapping EMI sensitive bands.

$$\begin{bmatrix} V_{SW,P} & V_{SW,N} \end{bmatrix} = \begin{cases} \begin{bmatrix} 1 & 0 \end{bmatrix} & \dots \text{if } (V_{IN} \geq \pm V_{TRI}) \\ \begin{bmatrix} 0 & 0 \end{bmatrix} & \dots \text{if } (-V_{TRI} < V_{LF,dif} < +V_{TRI}) \\ \begin{bmatrix} 0 & 1 \end{bmatrix} & \dots \text{if } (V_{IN} \leq \pm V_{TRI}) \end{cases}. \tag{2.1}$$

The single-sided switching of PP modulation beneficially decreases the amplitude of the CM switching signal $V_{SW,CM}$ by half, while also increasing the frequency of the CM components to $2f_{PWM}$, as shown in the FFT in Figure 2.4 (b). This allows for more suppression with the same LC filter. On the other hand, the DM switching $V_{SW,DM}$ remains similar to BD modulation, thereby retaining the same benefits of reduced DM ripple current and EMI, due to the reduced step size in comparison to AD modulation. Additionally, with PP modulation, the switching activity during idle operation also reduces, thus further minimising idle-channel power consumption, which gets mainly dominated by gate-charging losses [7].

Despite these benefits, PP modulation is not often used due to the presence of inband components in $V_{SW,CM}$. These components are nonlinearly related to the input signal, creating issues when the output stage is incorporated into a closed loop. In this configuration, finite common-mode rejection in the loop filter leads to CM-DM leakage, causing distortion in the differential-mode output $V_{SW,DM}$. Techniques to address this are discussed in Chapter 4.

In general, low DM and CM output step sizes and ripple currents are desirable for low EMI emissions without the need for altering f_{PWM}. Therefore, instead of using conventional 2-level single-ended output stages, multi-level output stages are often used as they create additional intermediate levels at the expense of employing extra supplies or external components [7]–[12]. Similarly, multi-phase schemes utilize multiple 2-level output stages per single-ended half, each driven in a phase-interleaved fashion to effectively reduce the ripple content in the currents instead of the voltage step size [13], [14]. Some of the pros and cons of these approaches are elaborated below.

2.1.3 Multi-Level PWM

Multi-level output stages, such as those shown in Figure 2.5 (a) (b), create additional voltage levels in each half, thereby reducing the voltage step size, ripple currents, and therefore EMI, at their outputs. In both [7] and [8], additional switches short the outputs of both halves of the H-bridge to create a 0.5FS CM level and a 0 V DM level, thereby producing 3 differential levels. The primary benefit of such a 3-level output stage is that it maintains the same differential output as BD modulation, with all its associated benefits, while keeping the CM output at $V_{SUP}/2$ like AD modulation. This configuration theoretically eliminates all CM related EMI issues, and is often also referred to as No-CM BD modulation.

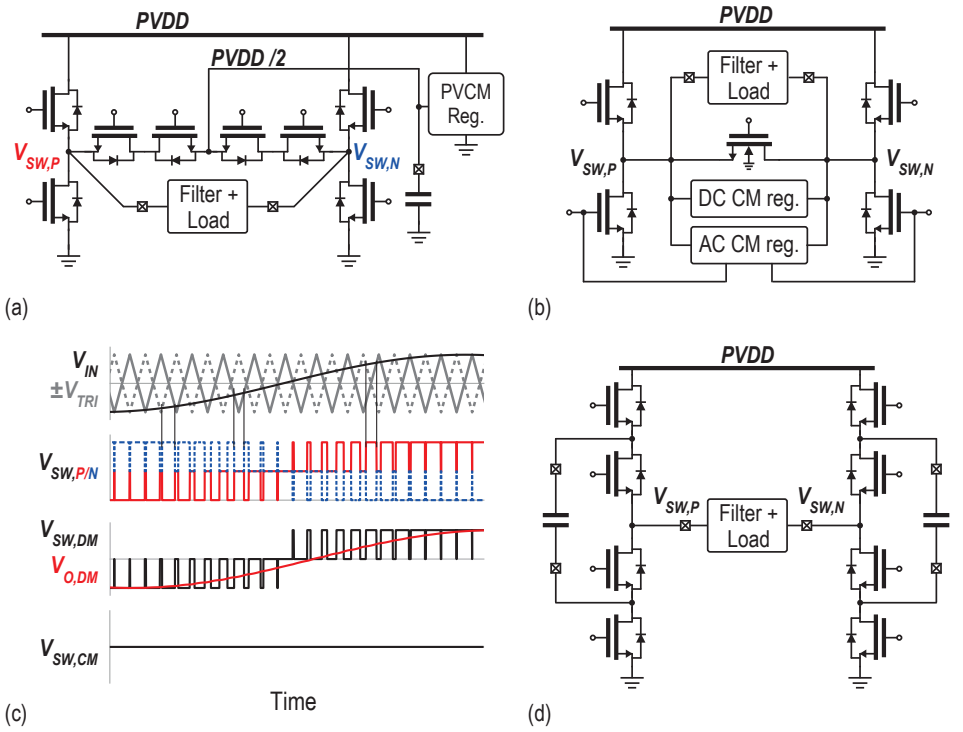

Figure 2.5: (a) and (b) Multi-Level output stages of [3] and [4], respectively; (c) typical time-domain waveforms of a 3-level no-CM BD modulated output stage; (d) output stage of [11] and [12].

In [11], [12] (Figure 2.5 (d)), each output stage produces the intermediate level by means of an off-chip flying capacitor. Such output stages can further lower the differential swing by using appropriately phase shifted carriers to generate 5 levels differentially. This comes at the cost of CM swing, similar to BD modulation, albeit with a reduced amplitude.

2.1.4 Multi-Phase PWM

Multi-phase architectures like [13], [14] use multiple H-bridge output stages, as shown in Figure 2.6 (a), each driven by phase shifted versions of the carrier to effectively reduce the ripple current that flows into the speaker cables, and therefore the resulting EMI. As illustrated by the phase-shifted AD-modulated output waveforms, although the ripple current in each branch ($I_{L1/2,DM}$) is equivalent in amplitude and frequency to a single

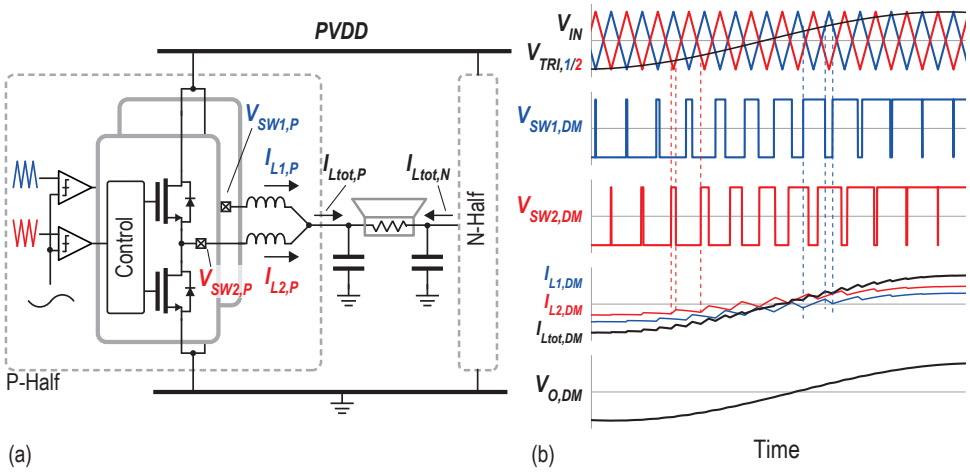

Figure 2.6: (a) Multi-phase output stage in [14]; (b): typical time-domain illustration of ripple current reduction with phase-shifted output stages.

output stage, the effective summation current ($I_{Ltot,DM}$) after the inductors is reduced, and is equivalent to the current profile of the multi-level output stage in the preceding section. Furthermore, the phase of the carriers in different branches also influences the number of DM and CM levels, thereby allowing for a trade-off between DM and CM EMI performance.

However, all the above multi-level / phase architectures require additional on-chip switches, as well as off-chip components such as inductors and capacitors, and/or supplies and thus increase overall cost and system size.

2.2 Switching Frequency and Negative Feedback

In addition to multi-level/multi-phase architectures, the PWM switching frequency can also be optimized to help improve EMI compatibility. There are trade-offs to this however, depending on the architecture of the modulation scheme involved, some of which are discussed below.

2.2.1 PWM Frequency Optimization

Observing the EMI sensitive bands in Figure 2.7 (a), it becomes apparent that by setting the carrier frequency above the AM band (~1.7MHz), potential EMI issues from the PWM tones at f_{PWM} and its harmonics can be avoided. Additionally, increasing f_{PWM}

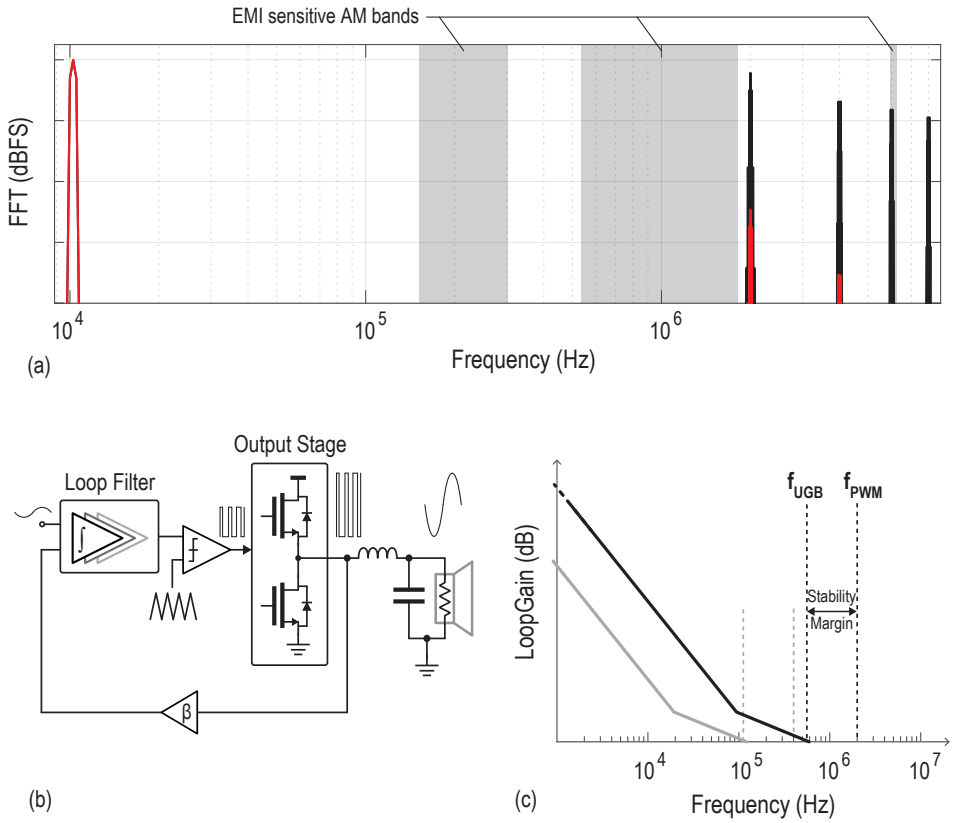

Figure 2.7: (a) FFT with $f_{PWM} = 2$ MHz and its effect on EMI sensitivity; (b) Simplified block diagram of a closed-loop CDA; (c) Effect of increasing f_{PWM} on the loop gain and UGB.

enables the use of an LC filter with a higher cutoff frequency for the same audio-band attenuation, which then permits the use of smaller and cheaper components. To the best of the author's knowledge, this approach was first implemented in [15], in a bid to reduce overall system cost.

In addition to addressing EMI concerns, it is also crucial to manage other nonidealities of a CDA's output stage, such as its non-linearity and poor supply immunity, as discussed earlier in Chapter 1. Therefore, irrespective of the modulation scheme and switching frequency used, a CDA is almost always implemented with a high-gain loop filter before the modulator and the output stage, as shown by the simplified block diagram

in Figure 2.7 (b). The loop gain helps suppress the non-linearity of the output stage within the audio-band, which arises due to switching and timing nonidealities, and also improves the power supply rejection (PSR) of the output stage. However, in such a closed-loop architecture, the switching frequency also limits the loop filter's unity-gain frequency (f_{UGB}) needed to ensure large-signal loop stability. Intuitively, the slew rate of the loop filter's output must be less than that of the triangular carrier used for PWM modulation. For a 2-level AD-modulated PWM Class-D amplifier, this condition is met when,

$$f_{UGB} < \frac{f_{PWM}}{\pi}, \tag{2.2}$$

where f_{UGB} is the unity gain frequency of the loop-filter [16]. With BD modulation, and other multi-level / multi-phase output stages that necessitate multiple PWM carrier phases, the effective switching frequency (f_{SW}) can be defined as $f_{SW} = N \cdot f_{PWM}$, where N represents the number of PWM phases required. In such cases, Equation 2.2 becomes,

$$f_{UGB} < \frac{f_{SW}}{\pi}. \tag{2.3}$$

Thus, increasing f_{PWM}, and consequently f_{SW}, enables higher loop-gain in the audio band as illustrated in Figure 2.7 (c), effectively resulting in better suppression of output-stage nonidealities.

However, the use of higher carrier and switching frequencies also increases the dynamic and switching losses of the output stage, and in addition, forces it to generate narrower pulses for large amplitude input signals. While switching loses can be managed with properly optimized switch sizes, mitigating the non-linearity that arises due to non-ideal slew-rate limited pulses requires higher loop gain.

2.2.2 PDM - ΔΣ Modulation

Pulse-density-modulation (PDM), using a 1-bit delta–sigma modulator (ΔΣM), can also be used to drive a 2-level output stage [17]. A simplified block diagram of the combination of a 1-bit ΔΣM with a Class-D output stage is shown in Figure 2.8 (a). Since the minimum pulse width for a 1-bit ΔΣM is defined by its sampling frequency (f_S), this can be set low enough to prevent slew-rate induced non-linearity.

However, using a 1-bit ΔΣM also comes with several challenges. Instead of producing PWM tones and intermodulation components at fixed frequencies, the high-frequency switching energy manifests itself as shaped quantization noise, which can create potential EMI issues due to its wideband nature as shown by the FFTs of a 1-bit ΔΣM's output in Figure 2.8 (b), before and after the LC filter. Furthermore, a 1-bit ΔΣM does not have a well-defined switching frequency, and the average switching frequency can vary quite a lot as a function of the output amplitude [17]. Lastly, a high order loop filter is often required to ensure a sufficient suppression of in-band quantization noise, without

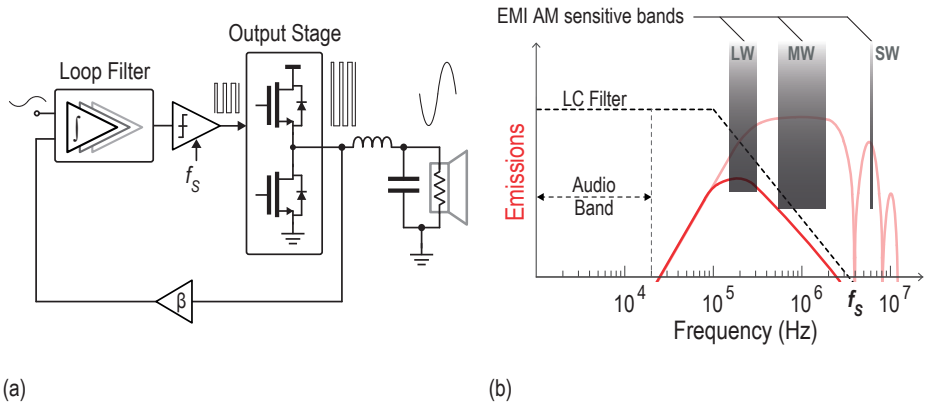

Figure 2.8: (a) Simplified block diagram of ΔΣM CDA; (b) Effect of wideband quantization noise on EMI with and without LC filtering.

drastically increasing f_S. However, this directly translates into to a limited stable input range and high out-of-band (OOB) quantization noise.

In [17], the average switching frequency is lowered and controlled by adding a signal-dependent hysteresis to the quantizer of a ΔΣM. However, it still generates out-of-band energy in the AM-band. Moreover, to maintain large signal stability the loop filter is also dynamically switched from 7th order (for low in-band quantization noise) to 2nd order, which complicates the design and degrades large-signal THD+N.

To explore these trade-offs, a Class-D amplifier with a hybrid ΔΣM-PWM modulation scheme is proposed in Chapter 3. It attempts to retain the linearity associated with 1-bit ΔΣM, while drastically improving the EMI performance in comparison. The prototype achieves state-of-the-art linearity over a wide output power range, while meeting the CRISPR-25 standard with a relaxed LC filter without additional off-chip components.

2.3 External Components

CDAs typically require external passive components to provide necessary filtering and damping to maintain efficiency, minimize EMI, and meet the specific system specifications. They are also versatile in driving various speaker loads, irrespective of the modulation schemes and switching frequencies employed. Traditionally utilized with electrodynamic speakers, CDAs are now increasingly favoured as the primary driver for piezoelectric speakers. The following sections delve into specific off-chip configurations for different speakers and applications.

2.3.1 Filter-less Driving of Electrodynamic Speakers

While passive LC filters are frequently utilized in EMI-sensitive or high-power audio applications, they are avoided in portable and low power applications. In such cases, the inductive properties of the speaker load are used to attenuate high-frequency currents. This attenuation is further complemented by the use of BD or multilevel modulation schemes to guarantee compliance with EMI limits [2], [3].

2.3.2 Off-Chip Filtering and Damping with Piezoelectric Speakers

Driving a piezoelectric speaker presents unique challenges due to its highly capacitive impedance. Typical configurations to drive a piezoelectric capacitive load using Class-AB or Class-D amplifiers are shown in Figure 2.9. In the case of Class-AB amplifiers, an external power resistor is typically introduced in series with the load to mitigate excessive transient currents and prevent amplifier instability. However, this method is highly inefficient, due to the power dissipated in the resistor and the inherent inefficiency of Class-AB amplifiers. Consequently, this approach is usually restricted to smaller loads (< 1.5µF) [18], [19].

CDAs offer higher efficiency, especially with larger load currents. Nonetheless, to comply with EMI constraints and minimize conduction losses, the integration of at least

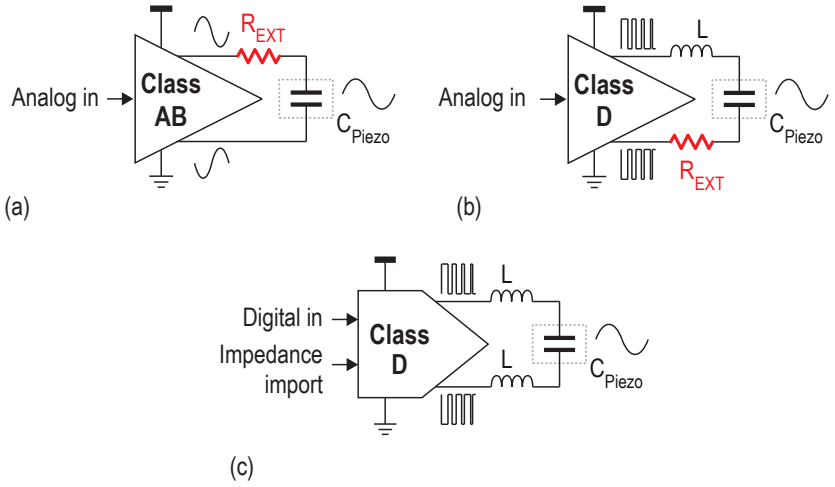

Figure 2.9: Existing approaches to drive a capacitive piezoelectric speaker- (a) Class-AB amp. + external resistor, (b) Class-D amp. + external resistor, and (c) Class-D amp. + calibration.

one inductor is necessary to form an LC filter with the load. Furthermore, an external power resistor is still needed to curb excessive currents at the LC resonance frequency due to out-of-band harmonics [20], [21]. To eliminate the external damping resistor, [22], a digital-input Class-D piezoelectric speaker driver (Figure 2.9 (c)), relies on foreground calibration to modify the input signal using a priori information about LC filter impedance. This prevents current overshoots but increases system complexity.

2.3.3 Resistor-less Driving of Piezoelectric Speakers

A more power-efficient strategy to dampen the LC resonance involves the use of a current feedback (CFB) loop to emulate the behaviour of a damping resistor. However, conventional methods necessitate the use of an external current transformer to sense the amplifier's output current, increasing system cost and preventing a fully integrated CMOS solution [23], [24].

Resistor-less LC resonance damping can also be achieved by using active on-chip circuits that consume significantly less power. To see how this can be done, the ideal block diagram shown in Figure 2.10 (a) can be analysed. It consists of an ideal amplifier with a gain G, that is loaded by a series combination of a load capacitance CL, a filtering inductor L, and a damping resistor R. The transfer function from the input V_{IN} to the output V_O on the load capacitance can then be expressed as,

$$\frac{V_O}{V_{IN}} = G \cdot \frac{1}{\left(\frac{s}{\omega_n}\right)^2 + \left(\frac{s}{Q \cdot \omega_n}\right) + 1} = G \cdot \frac{1}{(LC_L)s^2 + (RC_L)s + 1}, \tag{2.4}$$

where $\omega_n \left(= \sqrt{\frac{1}{LC_L}}\right)$ and $Q \left(= \frac{1}{R}\sqrt{\frac{L}{C_L}}\right)$ represent the LC resonance frequency and the quality factor of the tank, respectively.

Looking at the network driving the load impedance Z_L $(= sL + sC_L)$, the external resistance R and output load current I_O adds an IR drop to the amplifier's output voltage V_{Amp}, leading to a voltage V_R $(= V_{Amp} - I_O R)$ across Z_L. As shown in Figure 2.10 (b), this voltage can be replicated by using an active transimpedance amplifier with a transimpedance gain of R in feedback around a unity gain stage. This maintains the same transfer function from V_{IN} to V_R and V_O.

Further simplification can be achieved by shifting the TIA's feedback to the input [Figure 2.10 (c)], adjusting its transimpedance gain to $K = R/G$, and combining the ideal gain stage G and unity buffer. Essentially, this network has the same output resistance of R at V_R as (a), resulting in identical LC resonance damping and quality factor as in Equation 2.4. This is accomplished by sensing the load current and providing a current feedback (CFB) path across the amplifier.

A practical implementation of this architecture consists of a closed-loop CDA that also incorporates a voltage feedback (VFB) factor $\beta_{VFB}(= 1/G)$, as shown in Figure 2.10 (d). Thus, the final architecture involves two feedback paths: a VFB path for setting the

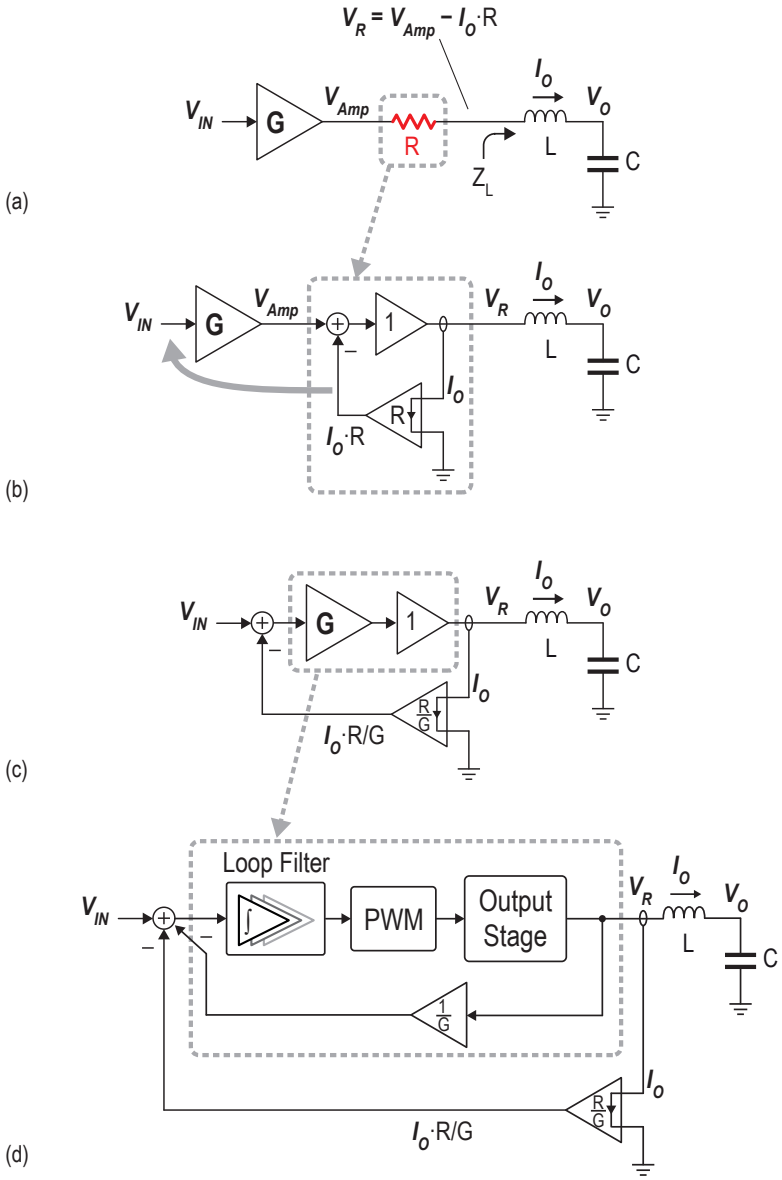

Figure 2.10: (a)-to-(d) Resistor to resistor-less transformation using an additional current feedback loop around a conventional amplifier.

closed-loop gain of G and a CFB path for providing LC resonance damping. The main idea here is to substitute the external resistor with an on-chip CFB network, significantly reducing power consumption, system cost, and size. A more detailed examination of this approach is presented in Chapters 4 and 5, along with implementation details and measurement results of a silicon prototype.

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Chapter 3

A Low EMI Hybrid ΔΣM-PWM Class-D Amplifier for Automotive Applications

As discussed in Chapter 2, the AM band EMI of a Class-D amplifier (CDA) can be significantly reduced by increasing the PWM frequency ($f_{PWM} > 2$ MHz), which also reduces the size and cost of the off-chip LC filter. Further reductions can be achieved by the use of multi-level and multi-phase output stages, but this comes at the expense of both silicon area and off-chip components.

This chapter describes a 28W CDA for automotive applications that employs a relatively high switching frequency ($f_{PWM} = 2$ MHz) and a hybrid multibit ΔΣM-PWM scheme to achieve high linearity as well as low EMI in the AM-band. An overview of the fully-differential, analog-input CDA is shown in Figure 3.1. It consists of a 3rd order loop filter, followed by a multi-level quantizer, whose output is then applied to a PWM generator that drives a 2-level output stage. The use of a multibit quantizer reduces out-of-band (OOB) noise, and consequently EMI, compared to the use of a one-bit modulator, while the PWM generator facilitates the use of a conventional two-level output stage. A prototype achieves state-of-the-art linearity over a wide output power range, while meeting the CISPR-25 EMI standard with a relaxed, low-cost LC filter, and no additional off-chip components.

3.1 Modulator Architecture

In this work, as shown in Figure 3.1, a multilevel ΔΣ to PWM converter is used to directly drive a conventional H-bridge [1]. An (N+1) level quantizer converts the loop filter output into a multilevel digital output at a sample rate f_S, which is then converted into a two-level signal by a PWM generator operating at a higher clock frequency

This chapter is based on the journal paper: S. Karmakar *et al.*, "A 28 W, −102.2 dB THD+N Class-D Amplifier Using a Hybrid DSM PWM Scheme," in *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3146-3156, Dec. 2020.

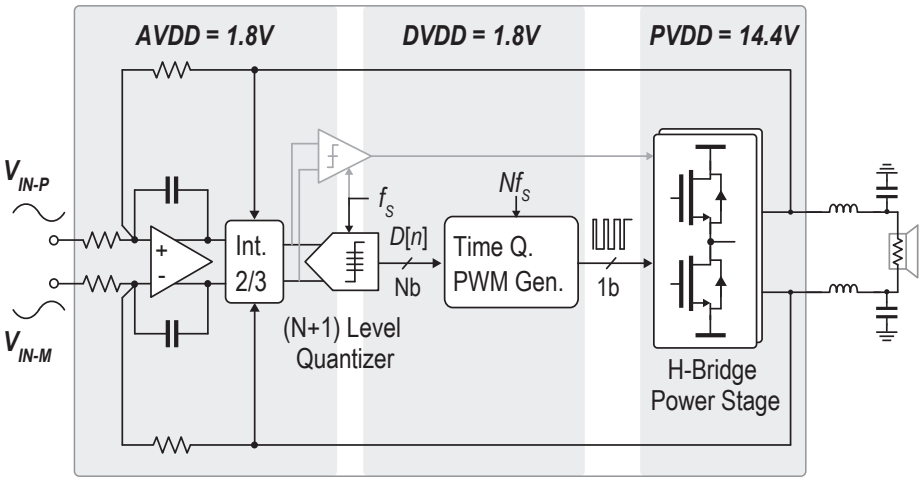


Figure 3.1: Simplified block diagram of the fully differential CDA.

$f_{CLK} = N \cdot f_S$. The case when $N = 4$ is illustrated in Figure 3.2, where 5 (=N+1) different two-level PWM pulses with a sampling period t_S ($= 1/f_S$) generate five different average values, each of which corresponds to a different level of the 5-level quantizer. The main considerations that inform the choice of N and f_S are the LC filter cutoff frequency and its tolerance, the desired in-band SQNR, and the narrowest pulse width that the output stage can faithfully reproduce. Each of these considerations will be discussed in detail below.

3.1.1 Modulation Scheme and Sample-Rate - f_S

There are two ways of concatenating the aforementioned pulse shapes to generate PWM sequences from a digital word (D[n]). As illustrated in Figure 3.3, consistently generating all the 1s (or 0s) first within a sampling period t_S results in a single-sided (SS) uniformly sampled PWM (UPWM) signal at a carrier frequency $f_{PWM} = f_S$ [2]. However, as illustrated in the last waveform in Figure 3.3, alternately reversing the order of the bits results in a double-sided (DS) signal, which halves f_{PWM}, as well as the associated switching activity and switching losses. In this work, to ensure some margin between the upper edge of the AM band (535 kHz - 1.7 MHz) and the main PWM tone, while avoiding excessive switching losses, f_{PWM} is set to 2 MHz, making $f_S = 4$MHz with DS modulation.

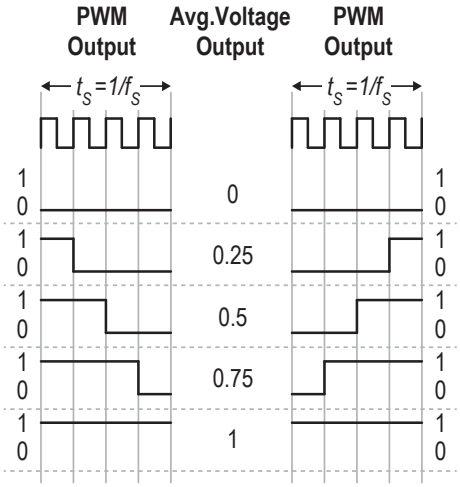


Figure 3.2: Generation of time-quantized PWM pulses using a higher clock rate.

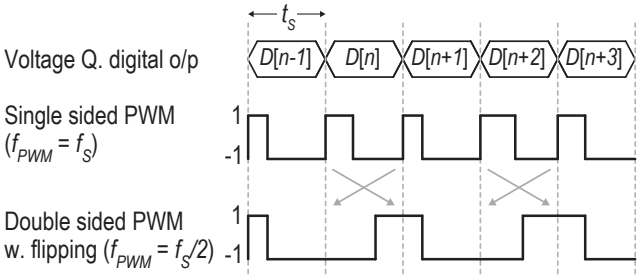


Figure 3.3: Time-domain signal path from quantized digital outputs to normalized PWM signals.

3.1.2 EMI, LC Filter Cutoff Frequency - f_{LC} and Tolerance

Since EM emissions are mainly caused by common-mode (CM) signals, each half of the H-bridge is driven in anti-phase, thus maintaining a constant CM voltage at the output nodes [3], [4]. Figure 3.4 (a) shows the simulated EMI spectrum for different modulation schemes with a relaxed LC filter cutoff frequency ($f_{LC} = 100$ kHz). It can be seen that a conventional 2-level ΔΣM generates a large amount of OOB noise and barely meets the CISPR 25 EMI requirements. By increasing the number of quantization levels to 21

and using the hybrid modulation technique, the OOB noise is significantly reduced and converted into PWM tones. In this design, $f_{CLK} = 80$ MHz clock positions the PWM tone at 2 MHz. Also, by using DS instead of SS modulation, the amplifier switches at half the frequency for the same OOB noise.

It is worth pointing out that while 2-level ΔΣM appears to (just) satisfy the EMI requirements, this will not be the case in the presence of LC filter spread (up to ±15%). As shown in Figure 3.4 (b), this results in significantly more DM-to-CM EMI leakage. Under the same conditions, the 21-level hybrid modulator still satisfies the EMI

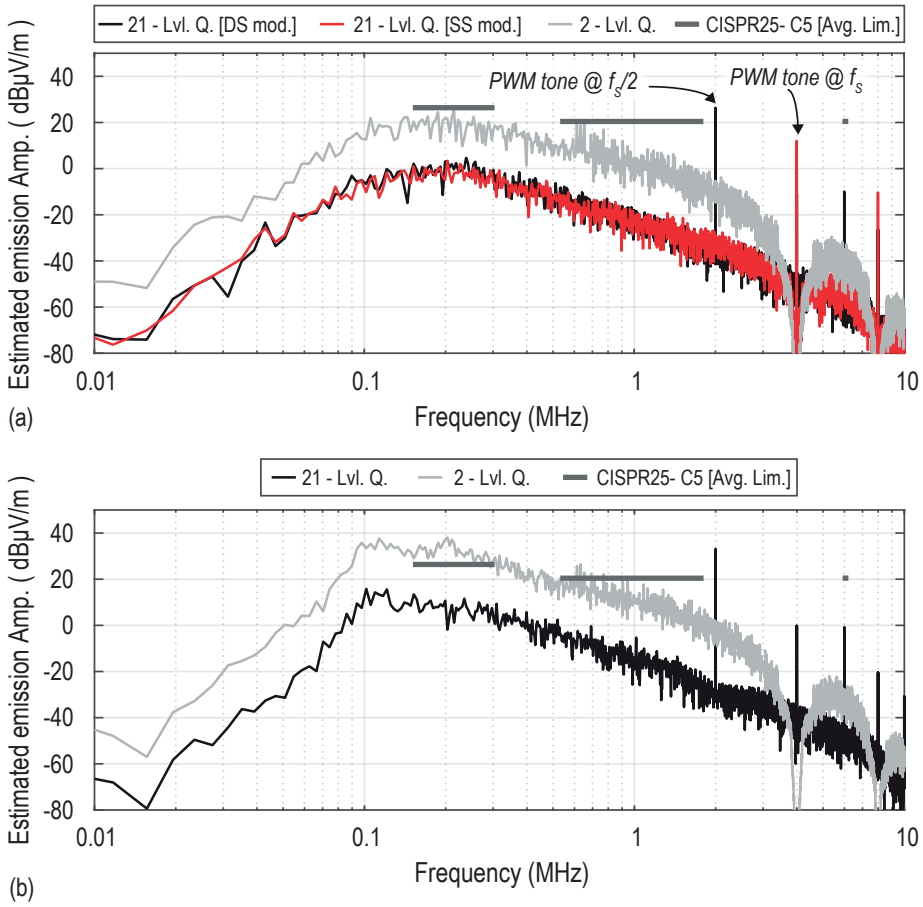


Figure 3.4: Simulated estimates out-of-band emission- (a) Comparison of the various modulation schemes; (b) Effect of ±15% LC mismatch on both the 21-level (DS) hybrid modulation and the conventional 2-level ΔΣM.

requirements with an acceptable margin. Furthermore, f_{LC} can be made even higher, if tighter component tolerances can be guaranteed. Some margin is still required, since the mismatch and timing skew between the two halves of the H-bridge will also lead to some differential mode (DM)-to-CM leakage, which will be further exacerbated by the use of non-twisted differential cables. While the amplifier's power supply connections also produce EMI, local supply decoupling is enough to reduce this to negligible levels. Compared with [5], the increased switching frequency means that sufficiently high in-band loop gain can be achieved even with a 3rd order loop filter. As a result, the 21-level modulator achieves an in-band SQNR of ~122dB and a maximum stable amplitude (MSA) to ~97% FS, which are both significantly larger than the 1-bit case. The end result is a thermal-noise limited design with a high dynamic range.

3.1.3 Pulse Width Limitation and Quantizer Non-Uniformity

The multilevel voltage and time quantization scheme described above uniformly distributes 21 bipolar steps (0.1FS each) across the full scale in both voltage and time domains, as illustrated in Figure 3.5. The minimum pulse width (12.5 ns) is then determined by $f_{CLK} = 20 \cdot f_S = 80$ MHz. In our design, however, the finite slew rate of the HV output stage and the propagation delay of the driving logic limit minimum pulse widths to about 16ns (typical), which worsens across PVT. This can be accommodated by decreasing either N or f_S, at the expense of more OOB noise. However, since audio signals typically have a high crest factor (7 - 25 dB) [6], [7], they rarely reach FS levels. Therefore, a more pragmatic approach is to make the quantizer nonuniform at high input levels. This can be done by removing the ±[0.8;0.9]FS quantization levels (indicated in grey in Figure 3.5), thus relaxing the minimum pulse width requirement by 3x to 37.5ns.

Although this choice reduces the total number of levels from 21 (uniform) to 17 (non-uniform), the resulting 16-bit thermometric code cannot be used directly. The original 21 level uniform quantizer inherently generates a 20-bit thermometric code which could then be sequentially output by the PWM generator at $20 \cdot f_S$. With the 17-level non-uniform quantizer, the loss of 4 bits, corresponding to the output of the comparators at ±[0.75;0.95], needs to be compensated to ensure that the PWM symbols have the same length as before.

Consider the case where the input lies between 0.7FS and 1FS. Since the comparator at 0.85 essentially determines if the quantizer output is at 0.7FS or 1FS, 2 additional bits are added at the end of the sequence, depending on the comparator's output, thus accommodating for the loss of the output bits of the now absentee comparators at 0.75 and 0.95 (indicated in red in Figure 3.5). Similarly, for the negative signals, 2 bits are added at the start of the sequence, depending on the output of the comparator at -0.85, accommodating for the loss of the output bits of the comparators at -0.75 and -0.95. This effective 0/1 padding maintains a throughput of 20 bits despite the use of non-uniform quantization. This approach only lowers the linear modulation range slightly (to ~93%) and negligibly increases OOB noise (due to the increased step size) for signals near FS.

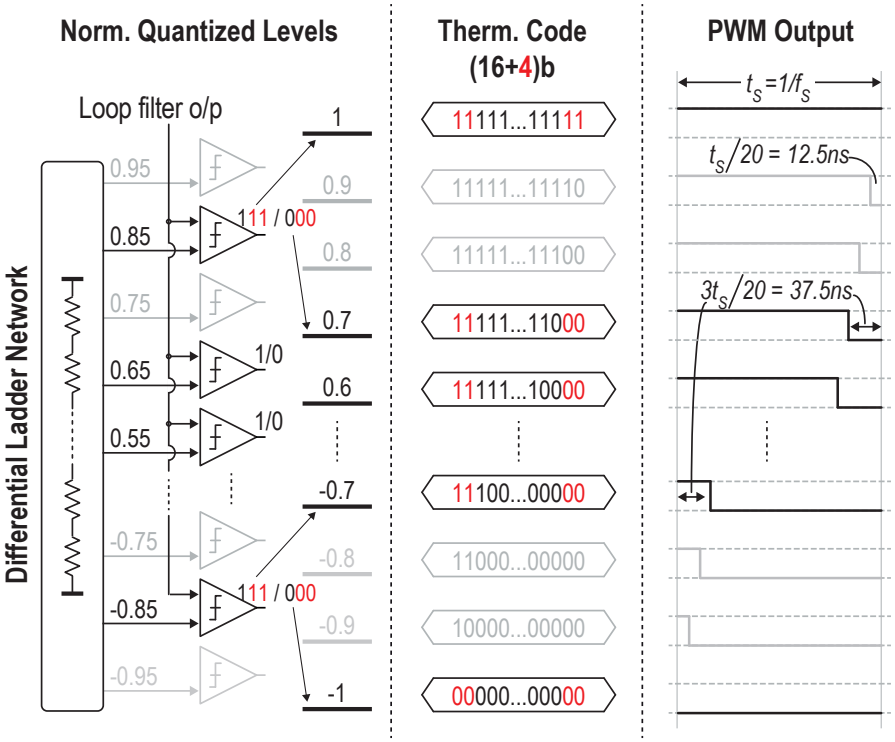


Figure 3.5: Limiting the pulse-width at extremely high modulation index by making the quantizer non-uniform.

3.2 Low-Voltage Circuits

The digital logic and analog circuits such as loop filter integrators and quantizer are built using area and power efficient 1.8 V devices. The detailed implementation of these circuits is discussed below.

3.2.1 17-Level Quantizer

As illustrated earlier (Figure 3.5), a flash ADC is well suited for implementing the quantizer, since it outputs a thermometer code that can directly be transmitted to the output stage, keeping the loop delay minimum. Although much more power hungry than e.g., a SAR ADC, its power contribution is negligible compared with that of the power stage. Dual-difference comparators [8] are used to implement the quantizer, since the

loop filter outputs, described in the next section, and the references are fully differential.

Nonlinearity in the quantizer itself arises due to the mismatch of the unit elements of the reference ladder and the offsets of the 16 comparators. The reference values are scaled to limit the swing of the loop filter output and ensure high linearity, while having a sufficiently large LSB step size (V_{LSB} ~ 102 mV) to relax the offset requirements of the comparators. Overall, the ladder references have a 3σ spread limited to ~400 μV, and the offset spread is limited to ~ 40 mV. In the worst case, the loop gain preceding the quantizer is high enough to maintain an SQNR above 120 dB. To compare the performance of the hybrid modulator with that of a 1-bit ΔΣM, an extra 1-bit comparator was also realised.

3.2.2 Fully Differential 3rd Order Loop Filter

As shown in Figure 3.6 (a), the modulator employs a 3rd order filter. An NTF with optimally placed zeros and an out-of-band gain of 1.8 results in high MSA, low OOB quantization noise, and high loop-gain across the entire audio band [8]. The loop filter is realized as a cascade of highly linear active-RC integrators in a feedback (CIFB) configuration. Direct input feed-ins to the outputs of the first two integrators suppress the audio band component at their outputs and significantly relax their linearity requirements.

Due to their low-voltage coefficients, p-poly resistors, and high density MIM capacitors are used to realize the various RC time constants. The noise in the audio band is primarily dominated by the 1st integrator, with the input resistors $R_{IN}(= 20k\Omega)$ accounting for ~52% of the total noise, while OTA1 and the feedback resistors RFB add another ~43%. The input resistance is a compromise between noise considerations and the requirements on the driving capability of a preceding DAC. The feedback resistors set a closed loop gain of 8× (18 dB). To compensate for RC process spread, (~30%), the capacitors are made 2-bit trimmable that are trimmed manually (once) by observing the OOB-shaped noise content.

The OTAs used in the loop filter (Figure 3.6 (b)) employ a 2-stage feedforward topology to provide the required gain. A capacitively coupled input feedforward path to the second stage ensures sufficient phase margin and high GBW [9]. Together, the three integrators draw 1.8 mA from the analog supply ($AVDD$ = 1.8V). After trimming, the filter's overall loop gain at 20kHz is > 76 dB across PVT, as shown in Figure 3.7. It is worth mentioning that the high loop gain also suppresses the adverse effects of clock jitter, which manifests itself in the output pulses as duty cycle errors and degrades audio performance [10]. In this design, up to 1 ns RMS clock jitter ($f_{CLK} = 80$ MHz) can be tolerated while maintaining 120 dB SQNR.

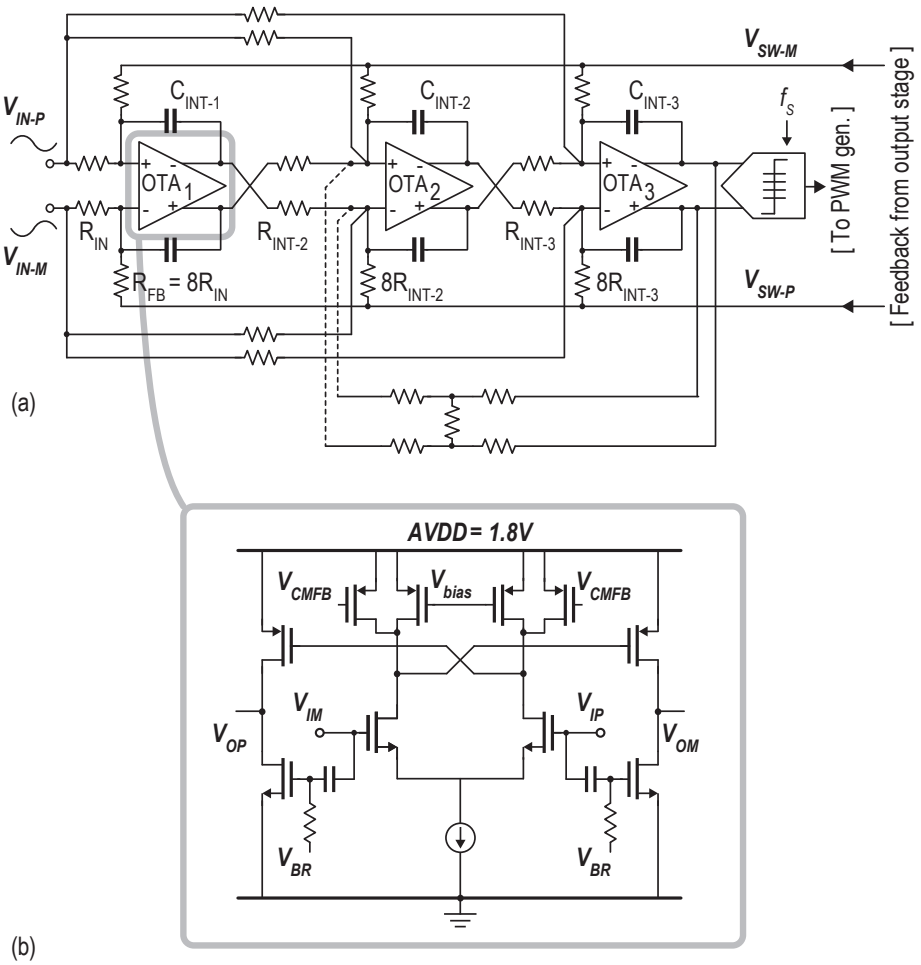


Figure 3.6: (a) Simplified schematic of the fully differential loop filter; (b) Simplified schematic of the OTA.

3.3 Output Power Stage

The output power stage consists of a fully differential H-bridge structure and is capable of driving a 4 Ω BTL. Figure 3.8 shows the output power stage along with associated driving circuits, with half of it depicted in detail. The primary output switches are

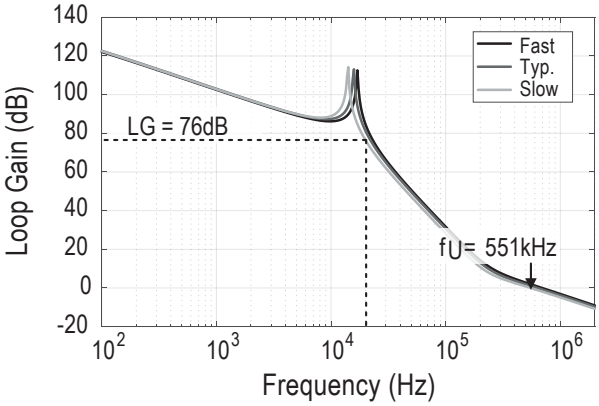


Figure 3.7: Loop gain of the loop filter across process after trimming.

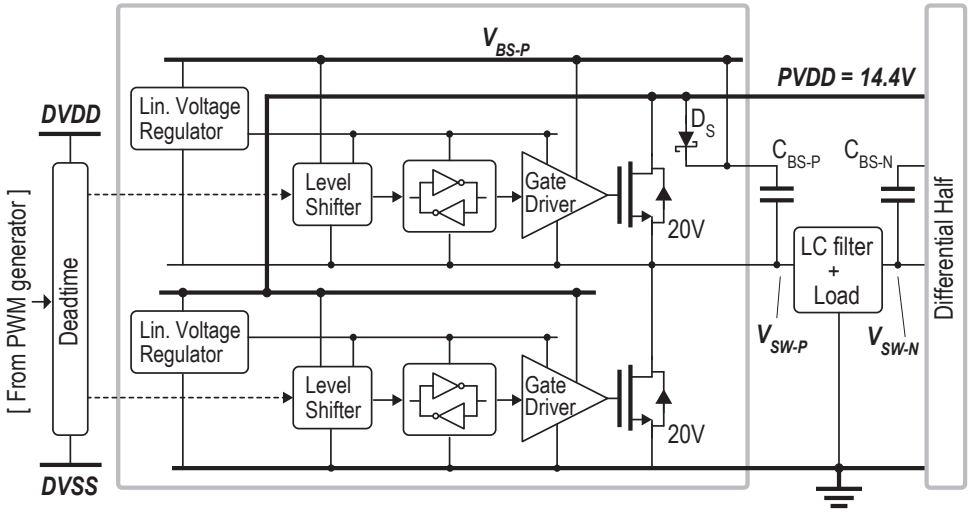


Figure 3.8: Simplified block diagram of the output power stage.

laterally diffused 20 V NMOS (N-LDMOS) transistors. The output power stage is responsible for > 95% of the total quiescent power consumed in the chip. Several factors contribute to the overall power dissipation in the output power stage [7], [11]; the most dominant ones being conduction loss due to the on resistance of the output

transistors (R_{ON}) and switching loss due to charging / discharging of gate capacitances (C_G). At high power levels, conduction loss dominates due to the large output current. Therefore, all output transistors ($M_{H/L}$) are sized for an R_{ON} of ~100 mΩ at 100°C to obtain an efficiency ~90% close to FS. In addition, the gate charge loss accounts for ~18% of the total losses. It is not worth increasing the output transistor size to further reduce R_{ON}, as this would result in a large die area and higher idle power consumption, which is dominated by switching loss. While all the high-voltage LDMOS devices have a high $V_{DS,MAX}$ rating, the sensitive nature of their gate oxides limits the maximum allowable V_{GS} to 5.5 V. To ensure that the gate voltages will never exceed this limit, linear voltage regulators are used to generate a localized 4.8 V supply to power all the circuits associated with driving the output switches [11]. This also provides sufficient de-coupling from supply and ground bouncing.

3.3.1 Linear Voltage Regulators

The R_{ON} of the output devices is relatively insensitive to V_{GS} variations, provided it has sufficient overdrive (> ~3V), and hence, a closed-loop regulation for the gate-driver supply [11] is not required. Instead, an open-loop structure, illustrated in Figure 3.9 (a), offers a more area- and power-efficient solution by eliminating the requirement for a high-voltage error amplifier for each regulator. Among the four regulators required, two of them are referenced from the HV switching nodes ($V_{SW\text{-}P/N}$), while the other two are referenced from the HV ground (*PVSS*) and so must be able to handle significant ground bouncing. To avoid the need for generating four separate HV local references, a single 1.2 V reference from a clean ground (*AVSS*) is used to generate a reference current over a resistance R. This current gets mirrored with a 1:1 ratio and is used to generate a local 4.8V reference (V_{4R}) over a scaled resistor (4R) within each of the regulators. V_{4R} is then mirrored across an output decoupling capacitor (C_{Decoup}) of 12 pF, by maintaining equal current densities across $M_{1\text{-}3}$, providing a regulated output voltage $V_{REG} = V_{4R}$. The push–pull source-follower architecture provides a low output impedance, which, together with a C_{Decoup}, result in a relatively clean V_{REG} by sinking/sourcing large transient currents during switching activities. Figure 3.9 (b) shows the output waveforms of both the high/low side regulators ($V_{REG\text{-}HS/LS}$) together with the V_{GS} of the high-/low-side output switches and the switching node V_{SW}. The typical case and variations across PVT are represented in black and grey, respectively. The various V_{REG}s exhibit transient fluctuations of less than 250 mV across PVT, and thus guaranteeing safe operation of the output devices and associated circuits.

Random mismatch in the resistors and current mirrors causes an additional variation of ~180mV in V_{REG} (Figure 3.9 c)), which results in a negligible RON spread of ~1 mΩ. The low-side regulators are powered directly from the high voltage rail (*PVDD*), while the boot-strapped voltages ($V_{BS\text{-}P/N}$) are generated by using internal Schottky diodes (DS) and off-chip capacitors ($C_{BS\text{-}P/N}$) to power the high-side regulators.

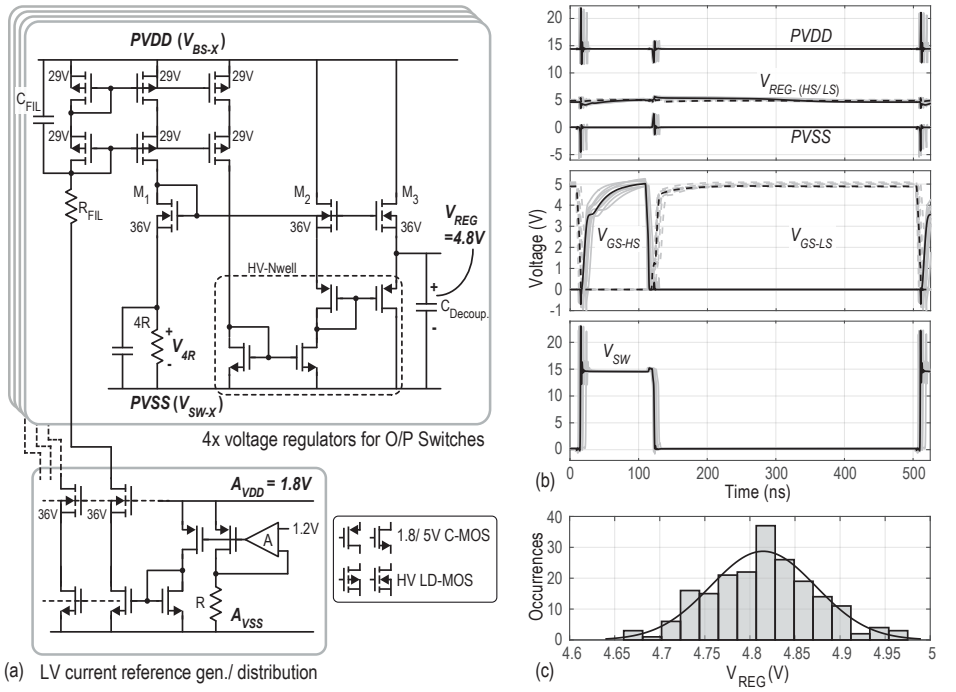


Figure 3.9: (a) Schematic of the linear voltage regulators for the gate-driving circuits; (b) output waveforms of the regulated voltage, V_{GS} of the switches and the output switching node, across process and temperature; (c) Monte Carlo spread in V_{REG} due to component mismatch.

3.3.2 Level Shifters and Gate Drivers

Level shifters are used to transmit the signals from the digital domain ($DVDD = 1.8$ V) to their respective high-voltage domains. High immunity from supply and ground bouncing can be attained by using a two-step approach similar to [11]. As shown in Figure 3.10, complimentary digital signals, initially referred to a relatively clean *DVSS*, are first up-shifted to *PVDD* (V_{BS}) and then down-shifted to the output transistor's reference node *PVSS* (V_{SW}). The fully differential structure and large headroom between *DVSS* and *PVDD* (V_{BS}) and between *PVDD* (V_{BS}) and *PVSS* (V_{SW}) makes this signal transmission robust to high common-mode ringing and prevents output latch errors. A pulsed constant bias current, with a typical on duration of15 ns, enables the level shifter shortly before a switching signal arrives at $D_{IN+/-}$, resulting in low average quiescent current.

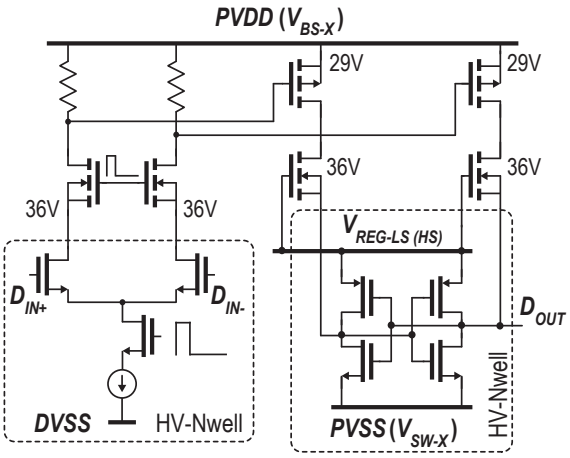


Figure 3.10: Schematic of the 2-step level shifter.

Gate drivers, as shown in Figure 3.11 (a), are required to reliably charge/discharge the gates of the output transistors. In general, the pull-down strength of a gate driver has to be sufficiently larger than the pull-up strength to avoid cross conduction [12]. However, simply using a strong pull-down would cause an excessive amount of ringing due to large di/dt in the parasitic inductances of the bonding wire. To avoid this situation, a weak pull-down (M_1) first discharges the gate, after which, the stronger pull-down (M_2) is activated. The associated gate driving signals are illustrated in Figure 3.11 (b). For charging the gate, a pull-up using a 36V N-LDMOS (M_4) is first activated to charge to gate up to roughly V_{REG-VT} directly from *PVDD* (V_{BS}). A PMOS (M_3) is then turned on to supply the remaining charge from the regulator. This reduces the regulator loading, reducing the transients on its output voltage. A minimal dead time of 7ns (with ~$\pm$15% variation across process and temperature) ensures no cross-conduction without causing a noticeable degradation in audio performance.

3.4 Implementation Devices and Protection

Due to bond-wire inductance, the high switching currents in the output stage can cause substantial substrate bounce (in the order of several volts). To prevent unwanted substrate coupling, sensitive low-voltage blocks are placed in high-voltage N-wells biased at 5.5 V. As shown in Figure 3.12, deep P-wells within the N-wells serve as the local ground (*AVSS* / *DVSS*) for their respective supply domains.

All HV LDMOS devices are realized in large isolation N-wells to achieve their

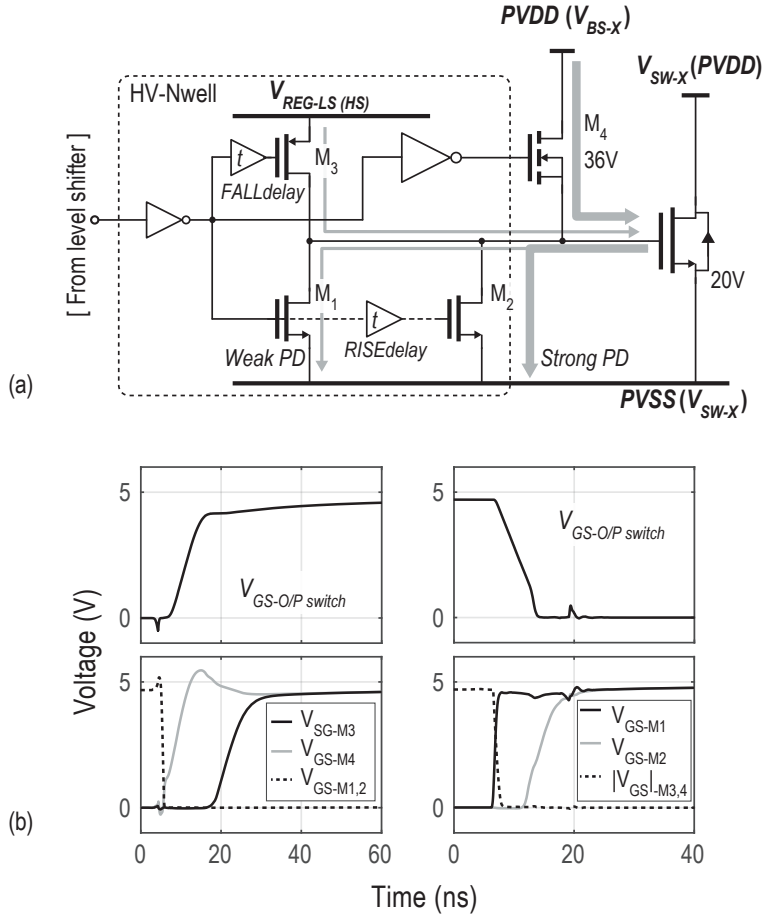


Figure 3.11: (a) Schematic of the gate driver; (b) associated gate driving signals and delays for turn-on/off phases.

ratings, making them area inefficient for small aspect-ratio transistors. Hence, wherever appropriate ($V_{DS} < 5$ V), low-voltage CMOS devices (5 V) are used. These are clubbed together in a single floating HV N-well [indicated by the black-dashed boxes in Figures 3.9, 3.10 and 3.11], with the deep P-well acting as the local reference ground.

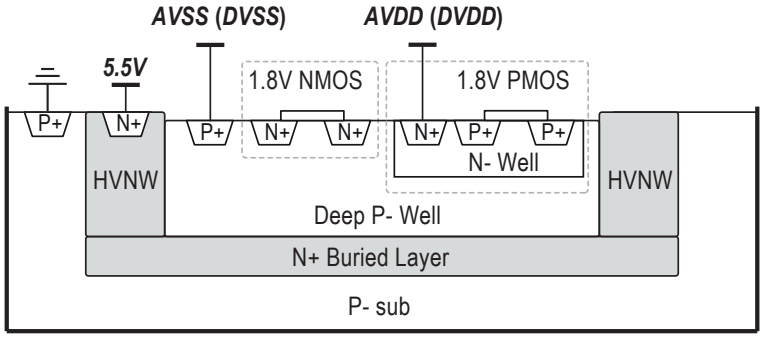


Figure 3.12: Simplified cross-section of the HV N-well used for 1.8V device isolation.

3.5 Measurement Results

The prototype hybrid CDA is realized in a TSMC 180 nm BCD bulk process, as shown in Figure 3.13. It occupies an active area of 4.8mm^2, with the high voltage switches in the output power stage taking up 40% of the area, while the loop filter, whose area is dominated by the integration capacitors, takes up another 27%. The amplifier can drive a 4 Ω load and is powered from three separate supplies: *AVDD* / *DVDD* = 1.8 V, and

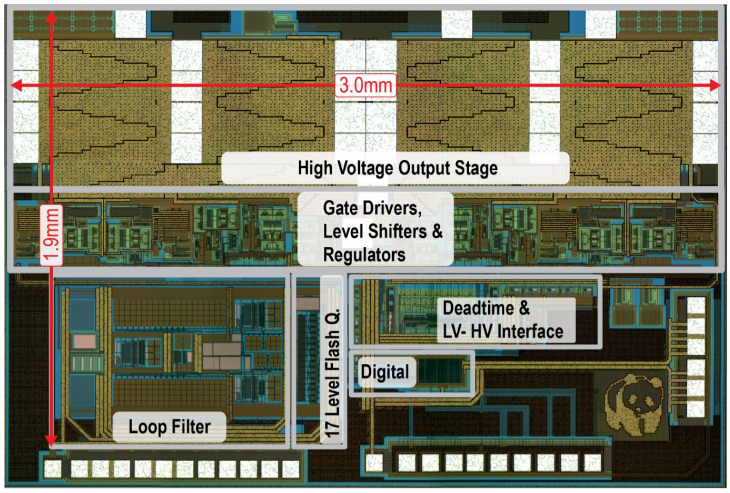


Figure 3.13: Die-micrograph of the prototype Class-D amplifier.

PVDD = 14 V. The main external components are the supply de-coupling capacitors (2 × 100 μF) and the LC filter with a cutoff frequency f_{LC} =100 kHz (L = 2.2 μH, C = 1.15 μH). During idle-channel operation, the amplifier draws 17mA from *PVDD*, which is primarily due to gate charging losses, and conduction losses due to the ripple current. Audio measurements were done using an Audio Precision APX-555 in combination with an AES17 filter.

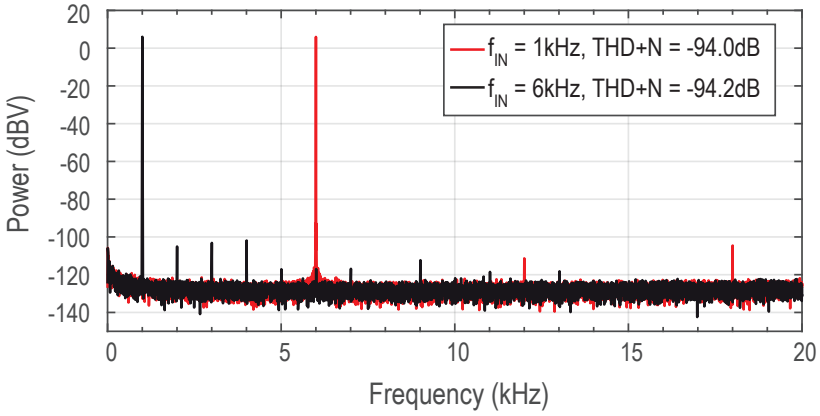


Figure 3.14: FFT at 1 W output power across a 4 Ω load.

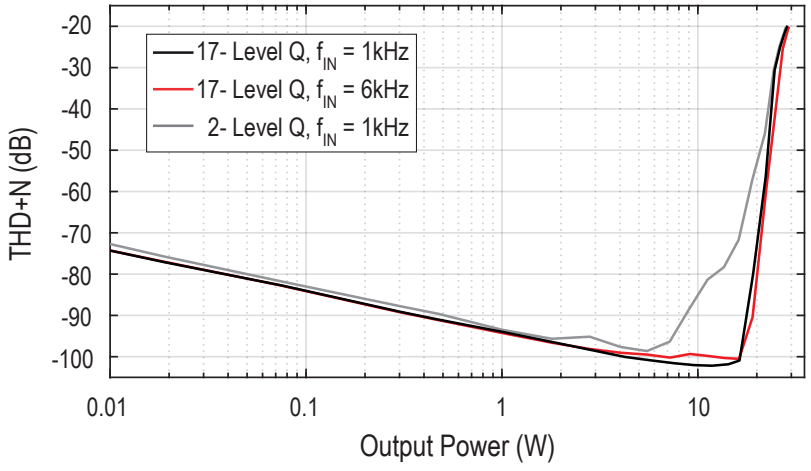


Figure 3.15: THD+N across output power.

Figure 3.14 shows the measured performance of the CDA when a 4 Ω load is driven at 1 W. A noise-limited THD+N of −94.0 and −94.2 dB is achieved at input frequencies of 1 and 6 kHz, respectively. Across output power levels (Figure 3.15), the amplifier achieves a peak THD+N of −102.2 and −100.5 dB, for input frequencies of 1 kHz and 6 kHz, respectively, while maintaining a THD+N < −80 dB for output power levels as high as 20 W. When a 1-bit quantizer is used, the modulator overloads at significantly lower power levels (> 8W). In the 17-level mode, the amplifier has an A-weighted output noise of 31 μV_{RMS} and a dynamic range of 110.6 dB (A-wt.).

Figure 3.16 shows the measured efficiency of the amplifier across output power levels. It attains a peak efficiency of 91% at its full power of 28 W and maintains an efficiency of > 90% beyond 20 W.

EMI measurements were conducted in accordance with the CISPR 25 Class 5 standard. The setup included a 12 V battery supply and a 4 Ω load connected to the amplifier using 1.5-meter long unshielded and untwisted cables. These measurements covered the frequency band from 150 kHz to 30 MHz, following the guidelines specified in [13]. Figure 3.17 (a) shows the average radiated emission in the frequency band for different modes and scenarios. In the absence of any spread in the off-chip LC filter components, both the multilevel and 2-level modes are able to satisfy the EMI limits. However, there is hardly any margin for the 2-level mode. To assess the effect of component tolerances, additional series/parallel combination of Ls and Cs was used to induce a ±15% spread over a nominal f_{LC} =100 kHz. In this case, while the emission for the 2-level mode exceeds limits, the 17-level mode still maintains 6 dB margin. In the case of tighter component tolerances, the cutoff frequency may be relaxed further, as shown in Figure 3.17 (b), where an f_{LC} of 150 kHz without mismatch still maintains 10 dB of

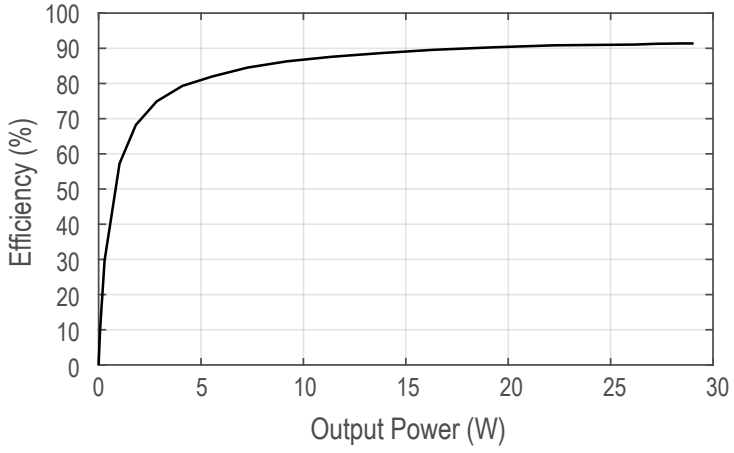
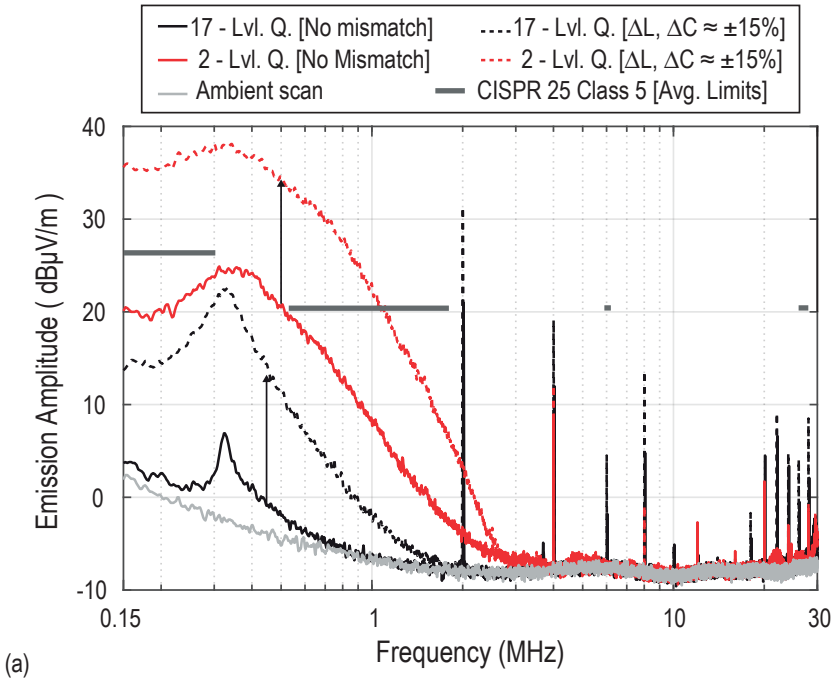
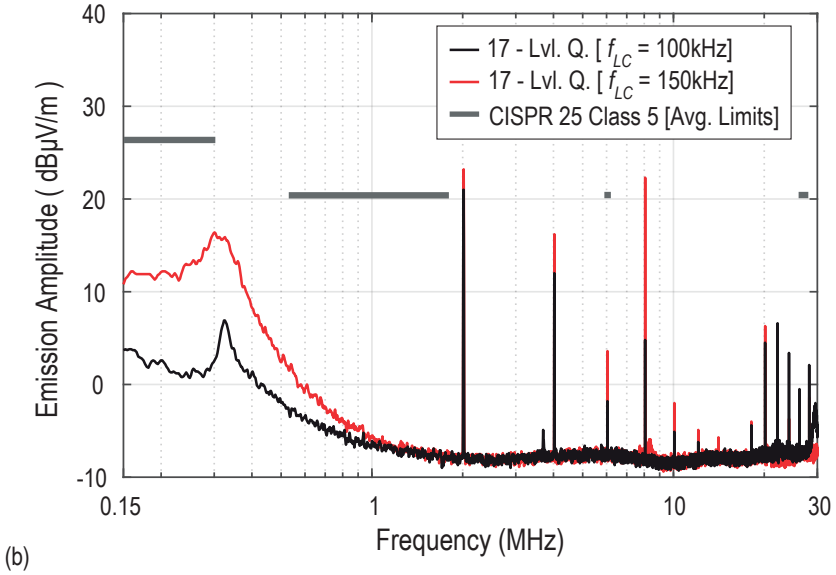


Figure 3.16: Efficiency of the amplifier across output power.



(a)



(b)

Figure 3.17: Measured EMI of the Class-D amplifier: (a) w/ and w/o ±15% mismatch in L and C and a mean $f_{LC} = 100$ kHz; (b) effect of further relaxing the LC cutoff frequency to $f_{LC} = 150$ kHz (w/o mismatch).

margin.

Figure 3.18 shows the measured PSRR of the amplifier when its supply is perturbed by a 1 V_{RMS} sine wave, swept across frequency. At low frequencies, the PSRR is 70 dB and is mainly limited by the matching of the resistors. Toward the edge of the audio band, a PSRR > 60 dB is maintained. A comparison of the performance of this amplifier with other state-of-the-art designs is shown in Table 3.1.

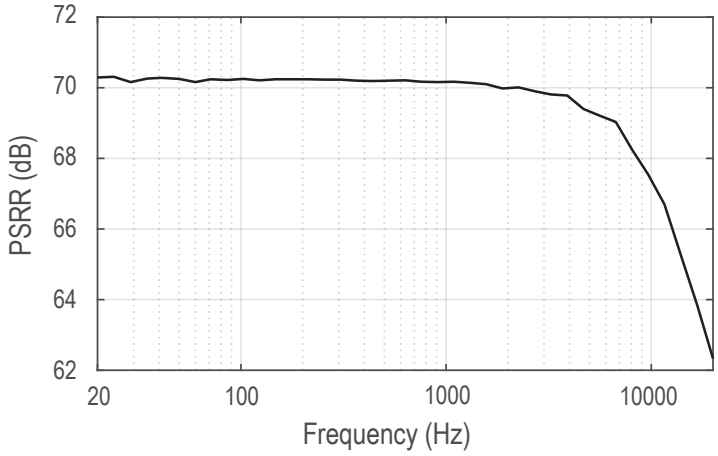


Figure 3.18: PSRR of the amplifier across supply perturbation frequency.

3.6 Conclusion

A CDA incorporating a hybrid ΔΣM-PWM modulation scheme is presented. Multilevel quantization using ΔΣM followed by time-quantized PWM generation drastically reduces the out-of-band EM emission compared with a 1-bit ΔΣM CDA, allowing the use of a relaxed LC cutoff frequency with relaxed component tolerances. The high sampling rate enables a high loop gain, which together with a robust output stage ensures high linearity across a wide output power range. Overall, the CDA achieves the state-of-the-art performance with a peak THD+N of -102.2 dB and a peak efficiency greater than 90%. In addition, it is shown that the LC cutoff frequency can be pushed as high as 150 kHz to satisfy the CISPR 25 average EMI limit [150 kHz–30 MHz], while still maintaining some margin.

One drawback of this approach is that the quantization noise added by ΔΣM inherently limits the cut-off frequency of the LC filter. An alternative way of meeting the EMI requirements in the AM band would be to use conventional AD/BD PWM operating at a sufficiently high frequency [19]. The non-linearity introduced by the slew-rate limitations

Table 3.1: Performance summary and comparison.

Parameter	This work	Schinkel [14]	Lee [15]	Hoyerby [16]	TAS6424 [17]	Gaalaas [5]	Cope [18]
Modulation Scheme	**Hybrid ΔΣ-PWM (Analog In.)**	PWM [MP] (Digital In.)	PWM [ML] (Analog In.)	PWM [ML] (Analog In.)	PWM (Digital In.)	ΔΣ (Analog In.)	PWM (Digital In.)
Supply	**14.4V**	25V	2.5-5V	24V	14.4V	12V	8-20V
Load	**4Ω**	4Ω	8Ω	4Ω	4Ω	6Ω	8Ω
THD+N (f_{IN} = 1kHz, P_O = 1W)	**0.002%**	0.004%	~0.0025%	~0.0095%	0.02%	~0.0032%	0.0029%
Peak THD+N (f_{IN} = 1kHz)	**0.00078%**	~0.0037%	0.0023%	0.003%	~0.015%	~0.0032%	0.0013%
Output Noise (A wt.)	**31μVrms**	34μVrms	-	-	42μVrms	50μVrms	20.5μVrms
P_{O-MAX} (10% THD)	**28W**	80W	10W	70W	27W	10W	20 W
Efficiency	**91%**	>90%	91%	90%	86%	88%	90%
Switching Freq.	**2.0MHz**	0.4MHz	0.7MHz	0.165-0.6MHz	2.1MHz	< 0.7MHz	0.4MHz
Comp. Count [L, C] Values	**2L, 2C 2.2μH, 1.1uF**	4L, 2C -	- -	- -	2L, 2C 3.3μH, 1uF	2L, 2C 15μH, 1uF	2L, 2C -
LC filter cutoff	**100kHz**	~40kHz	-		88kHz	41kHz	-
Quiescent Current	**17mA**	12mA	3.5mA	2.9mA	~40mA		20.52mA
PSRR (20-20kHz)	**70-62dB**	~100-60dB (88dB @100Hz)	~88dB (@217Hz)	-	~75-57dB	~68-39dB	80-50dB
Area/ Channel	**4.8mm²**	-	6.4mm²	6.7mm²	-	10.1mm²	-
Process	**180nm BCD**	140nm BCD SOI	180nm BCD	180nm BCD	-	600nm BCD	180nm BCD

of the output stage could then be mitigated by increasing the loop gain, among other techniques.

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Chapter 4

A Class-D Piezoelectric Speaker Driver with Resistor-Less LC Resonance Damping

This chapter presents a Class-D audio amplifier tailored for capacitive piezoelectric speaker loads. As briefly described in Chapter 2, it employs a dual voltage/current feedback topology to effectively damp LC resonance without the need for an external damping resistor, therefore reducing the associated cost, and size, and power consumption. Additional power savings are attained through the utilization of a push-pull modulated output stage. The chapter elaborates on the architectural and circuit-level techniques used to mitigate the non-idealities of the voltage and current feedback networks, as well as the push-pull modulation scheme. At the end, measurement results of a prototype, taped out in a BCD 180 nm process, are presented. It can drive a 4 μF load with a peak current of 4.4 A, and achieves an idle power consumption of 122 mW, a peak THD+N of -91 dB, and approximately 3.5 W power saving compared to systems employing an external resistor.

4.1 Dual-Feedback Modulator Architecture

In Chapter 2, an intuitive explanation is provided of how the dual voltage/ current feedback structure can be used to achieve the output impedance that emulates the role of a series R in an LCR network. However, to get a better understanding of how the dual-loop structure affects the overall system in terms of noise, distortion, degree of damping (or STF flatness), etc, it is better to consider its operation in the frequency domain.

This chapter is based on the journal paper: S. Karmakar *et al.*, "A -91 dB THD+N, Class-D Piezoelectric Speaker Driver Using Dual Voltage/Current Feedback for Resistor-Less LC Resonance Damping," in *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3726-3735, Dec. 2022.

4.1.1 Voltage and Current Feedback Paths

Figure 4.1 (a) shows a simplified block diagram of a Class-D amplifier with a dual voltage/current feedback network. The forward path consists of a high gain loop filter H(s), a PWM modulator, and an output stage loaded by an undamped LC filter with a cutoff frequency of f_{LC}. The voltage feedback (VFB) path, shown with a feedback factor (β_{VFB}), is kept unity-gain for simplicity. An on-chip current sensor uses a small sense resistor (R_S) to convert the load current (I_{Load}) into a voltage, which is then amplified by a gain K using a voltage gain amplifier to provide an effective current feedback (CFB) path. The output of the CFB path (V_{CFB}) is then given by:

$$V_{CFB} = K \cdot (I_{Load} R_S) . \tag{4.1}$$

Since $I_{Load} = V_{SW}/Z_{Load}$, where V_{SW} and Z_{Load} denote the switching node output voltage and the load impedance seen from V_{SW} respectively, a V/V feedback factor (β_{VFB}) for the CFB path can be defined as,

$$\beta_{CFB} = \frac{V_{CFB}}{V_{SW}} = \frac{R_S \cdot K}{Z_{Load}}. \tag{4.2}$$

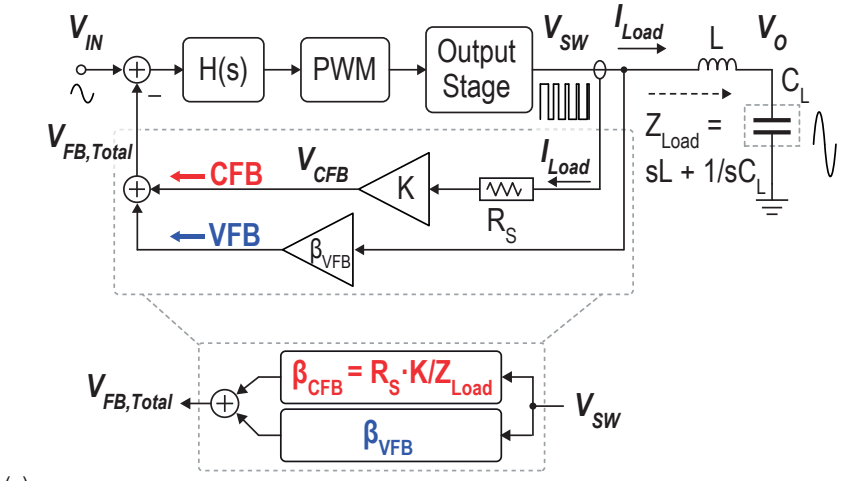
As shown in Figure 4.1 (b), the magnitude of β_{CFB} peaks at f_{LC} due to the presence of Z_{Load}, which is the undamped series combination of L and C_L. Setting an appropriate gain K allows $|\beta_{CFB}|$ to become larger than $|\beta_{VFB}|$ around f_{LC}, thereby creating a peak in the overall feedback factor $\beta_{Total} = \beta_{VFB} + \beta_{CFB}$. This effectively translates into a notch in the closed loop gain of the Class-D amplifier (G_{CL}), which can be approximated as:

$$G_{CL} = \frac{V_{SW}}{V_{IN}} \sim \frac{1}{\beta_{Total}}. \tag{4.3}$$

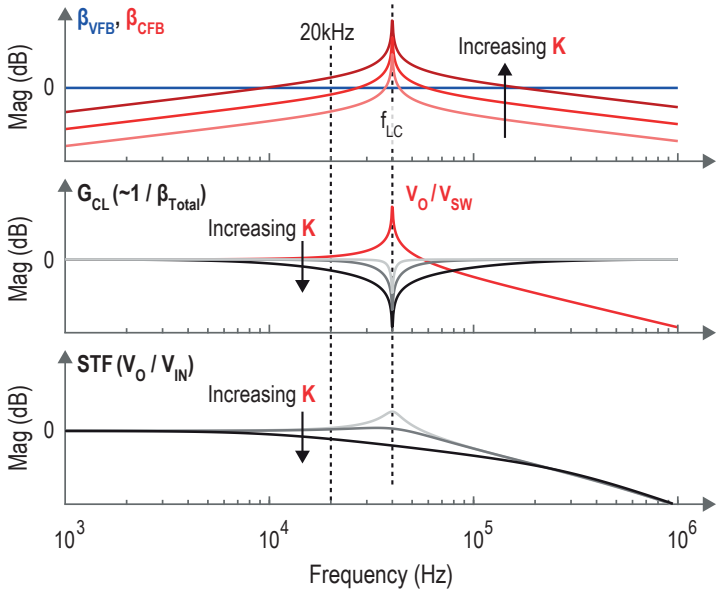
Together, the cascade of G_{CL} and the LC filter transfer function (V_O/V_{SW}) results in a damped signal transfer function (STF).

Although a larger gain K provides greater damping, it also reduces the flatness of the amplifier's STF within the audio band, and increases the impact of any nonlinearity in the CFB path on the linearity of the overall feedback. Increasing f_{LC} further allows for more flexibility in the choice of K for adequate damping, while also ensuring that the VFB path dominates the STF in the audio band (20 Hz- 20 kHz).

For large signal stability of the closed-loop Class-D amplifier, as mentioned in Chapter 2, the loop unity gain bandwidth ($f_{UGB,loop}$) should be $< f_{SW}/\pi$ with a near 1st order roll-off at $f_{UGB,loop}$. The additional CFB path doesn't affect this much, since at frequencies much above f_{LC}, the VFB path dominates the CFB path, making the stability criteria for the loop filter similar to those of a conventional closed-loop Class-D amplifier.



(a)



(b)

Figure 4.1: (a) Simplified block diagram of dual voltage/ current feedback topology, and (b) magnitude response illustrating resistor-less LC damping.

4.1.2 Push-Pull Modulation and Load Current Sensing

An H-bridge output stage is used to drive a bridge-tied-load (BTL), which consists of the series combination of a single inductor L and the load capacitor C_L, as shown in Figure 4.2. The output stage is driven using a Push-Pull (PP) modulation scheme [1]–[4], to reduce power consumption. In PP modulation, only one half of the H-bridge switches while the other half remains grounded, as illustrated in Figure 4.3. The control signals - $\Phi_{P/N}$ for each half of the output stage are generated in the low-voltage (LV) domain by comparing the differential output of the loop filter ($V_{LF,dif}$ in Figure 4.2), with a pair of 180° phase-shifted triangular carriers ($\pm V_{TRI,dif}$). Due to the level-shifting required between the LV and HV domains, and the additional gate drivers, there is a propagation delay (t_{delay}) between $\Phi_{P/N}$ and the HV switching nodes $V_{SW,P/N}$.

As explained in Chapter 2, PP modulation retains the same benefits of BD modulation with respect to reduced ripple current and associated losses due to the reduced step size, while also reducing idle-channel gate-charging losses due to reduced switching activity. However, the single-sided switching of $V_{SW,P/N}$, results in CM switching $V_{SW,CM}$ $[= 0.5(V_{SW,P} + V_{SW,N})]$ at the output, which contains inband components that are nonlinearly related to the input. The consequences and techniques to address them are discussed in Section 4.1.4.

The CFB path, as shown in Figure 4.1, requires load current sensing. In CDAs, this is typically done with sense resistors, with on-chip sense resistors being preferred over external resistors due to easier integration and lower costs. However, positioning the

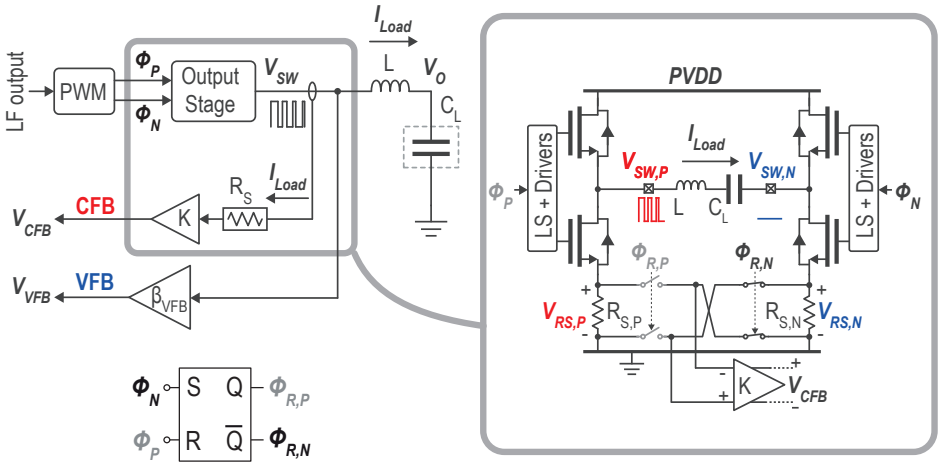


Figure 4.2: Simplified schematic of the PP modulated output stage with low-side sense resistors and readout amp, generation of controls signals of the CFB network switches.

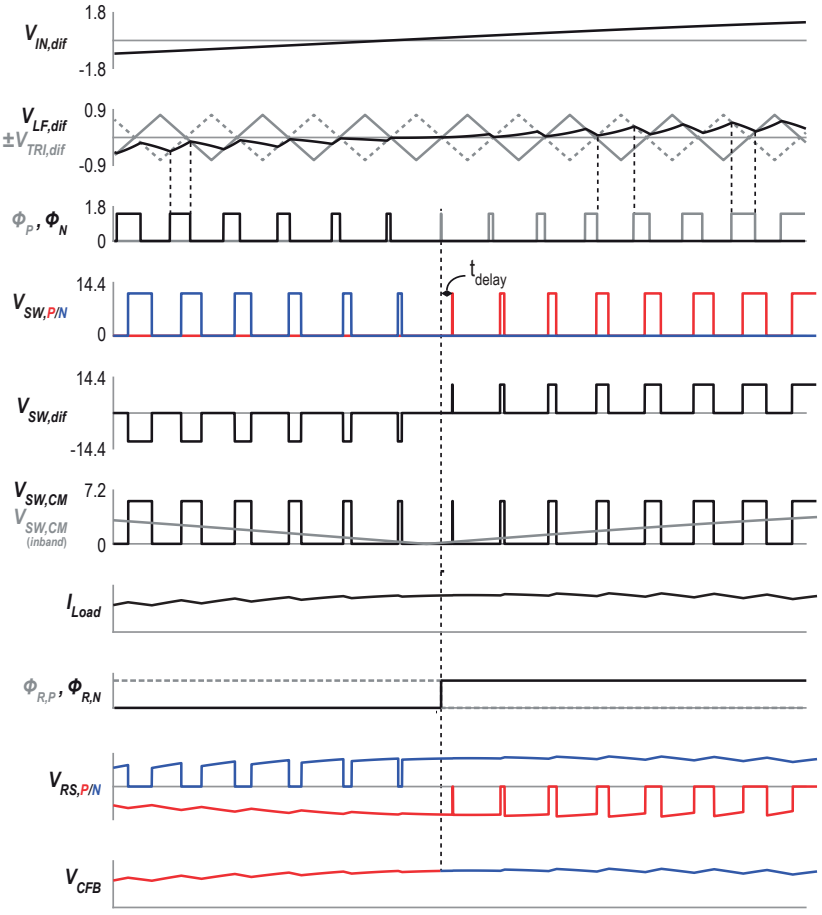


Figure 4.3: Time domain waveforms illustrating the push-pull modulation scheme and the operation of the CFB readout network.

sense resistors in series with the outputs of the H bridge ($V_{SW,P/N}$) would then require the associated readout amplifiers to handle the large high-frequency CM signals caused by the PWM switching activity at these nodes. In this work, low-side current sensing, with sense resistors $R_{S,P/N}$ positioned below the low-side output switches (Figure 4.2), is employed to indirectly sense the load current, as in [5], [6]. Since the sensed current is fed back to the signal path, a continuous-time current-sensing scheme with adequate linearity is required. This is not possible with BD modulated output stages, due to the overlapping off-state of both low-side switches every PWM cycle, and the presence of

other switching non-idealities. PP modulation is beneficial in this regard, since one half of the H-bridge avoids high-frequency PWM switching and instead remains grounded. As illustrated in Figure 4.3, when $V_{IN,dif}$ is negative, $V_{SW,P}$ remains grounded while $V_{SW,N}$ is switching, and therefore, I_{Load} can be sensed by connecting the readout amplifier across $R_{S,P}$. When the polarity of the audio signal changes and $V_{SW,P}$ starts switching, the read-out amplifier is connected to $R_{S,N}$, thereby providing a quasi-continuous readout of I_{Load}. The control signals of the CFB switches- $\Phi_{R,P/N}$ (in Figures 4.2 and 4.3) are generated by an SR-latch that is triggered by the $\Phi_{P/N}$, avoiding the need for a separate zero-crossing detector. The propagation delay (t_{delay}) between $\Phi_{P/N}$ and $V_{SW,P/N}$ ensures that the CFB switches always transition between $R_{S,P/N}$ when both H-bridge halves are grounded. Furthermore, the transition time is less than 1 ns, thereby minimizing any current-sensing glitches. Low-side current sensing further relaxes the input CM swing requirements of the readout amplifier (~$\pm$100 mV around 0 V).

However, both the CFB and VFB paths introduce distortion, and solutions to address this issue are discussed in the following.

4.1.3 CFB Path Nonlinearity Suppression

Since the load current readout is now a quasi-continuous measure of two different sense resistor voltages, the overall linearity of the CFB path is limited by their relative matching. Furthermore, the combination of self-heating and their intrinsic temperature dependence causes the voltage drop across the current sensing resistors to be a nonlinear function of load current amplitude and frequency. To avoid the need for complicated calibration and trimming techniques to suppress these errors, a relatively straightforward approach is proposed.

As the CFB path is primarily required to damp the LC resonance at f_{LC}, its gain in the audio band can be reduced. This, in turn, will mitigate the effect of its non-idealities in this band. This is achieved by closing the CFB loop around the 2nd integrator of the loop filter. As shown in Figure 4.4 (a), this can be done with the help of an additional low-pass (LP) filter with a cutoff frequency at $f_{C,CFB}$, and rescaling the DC gain K to

$$K' = K \cdot \left(\frac{f_{UG,Int1}}{f_{C,CFB}} \right), \tag{4.4}$$

where $f_{UG,Int1}$ is the unity-gain frequency of the 1st integrator. The overall s-domain transfer function of the CFB readout network is then given by,

$$\frac{V'_{CFB}}{V_{RS}} = K' \cdot \left(\frac{1}{1 + \frac{s}{\omega_{C,CFB}}} \right), \tag{4.5}$$

where ω terms correspond to frequencies in rad/sec. Referred to the 1st integrator's input, the transfer function above is given by,

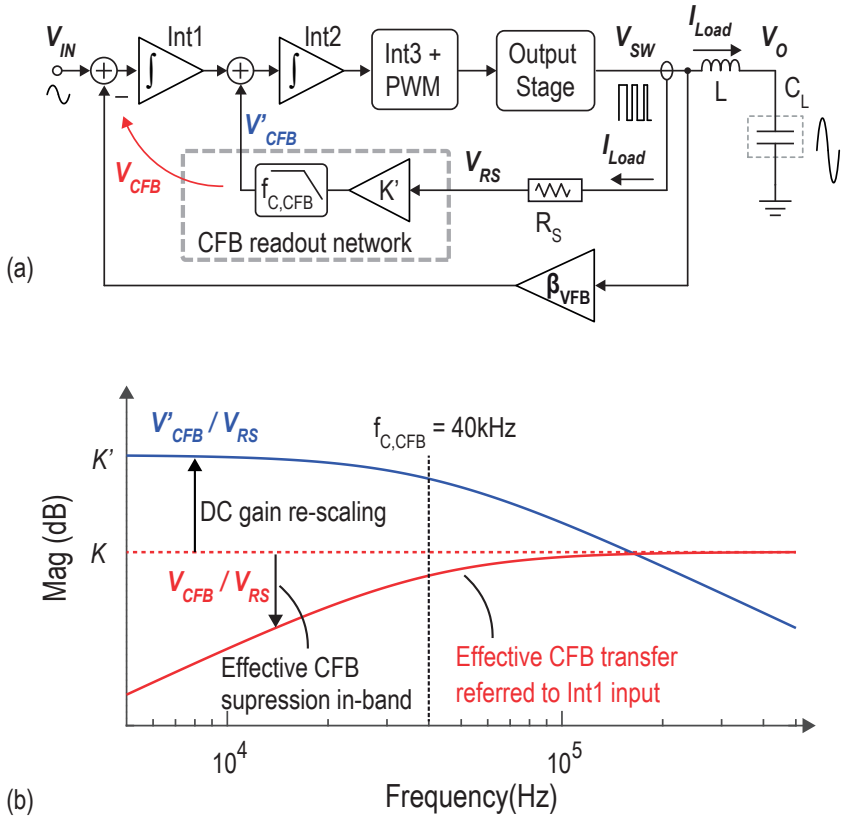


Figure 4.4: (a) Simplified block diagram illustrating the CFB network and non-ideality suppression, and (b) magnitude response of CFB to Int2 and referred to Int1.

$$\frac{V_{CFB}}{V_{RS}} = \left(\frac{V'_{CFB}}{V_{RS}}\right) \Big/ \left(\frac{\omega_{UG,Int1}}{s}\right) = K \cdot \left(\frac{\frac{s}{\omega_{C,CFB}}}{1+\frac{s}{\omega_{C,CFB}}}\right). \tag{4.6}$$

This is a high-pass filter, which ensures that CFB non-idealities are suppressed for input frequencies less than $f_{C,CFB}$, as illustrated in Figure 4.4 (b). Figure 4.5 (a) shows the effect of the CFB gain (K) on LC peaking suppression when f_{LC} =80 kHz, which is an often used cut-off frequency in Class-D amplifiers switching at MHz frequencies [7]–[9]. It can be seen that, although the audio band filtering of K slightly reduces damping efficacy, it can be recovered by increasing K. Figure 4.5 (b) shows the linearity of an

ideal amplifier in the presence of a 0.05% mismatch between $R_{S,P/N}$, which can be achieved by careful layout and proper sizing. The two graphs demonstrate that, to attain a certain damping in the presence of CFB path nonlinearity, it is better to go for a larger K e.g. 2.5 with audio band filtering, than a smaller K e.g. 1.25 without filtering.

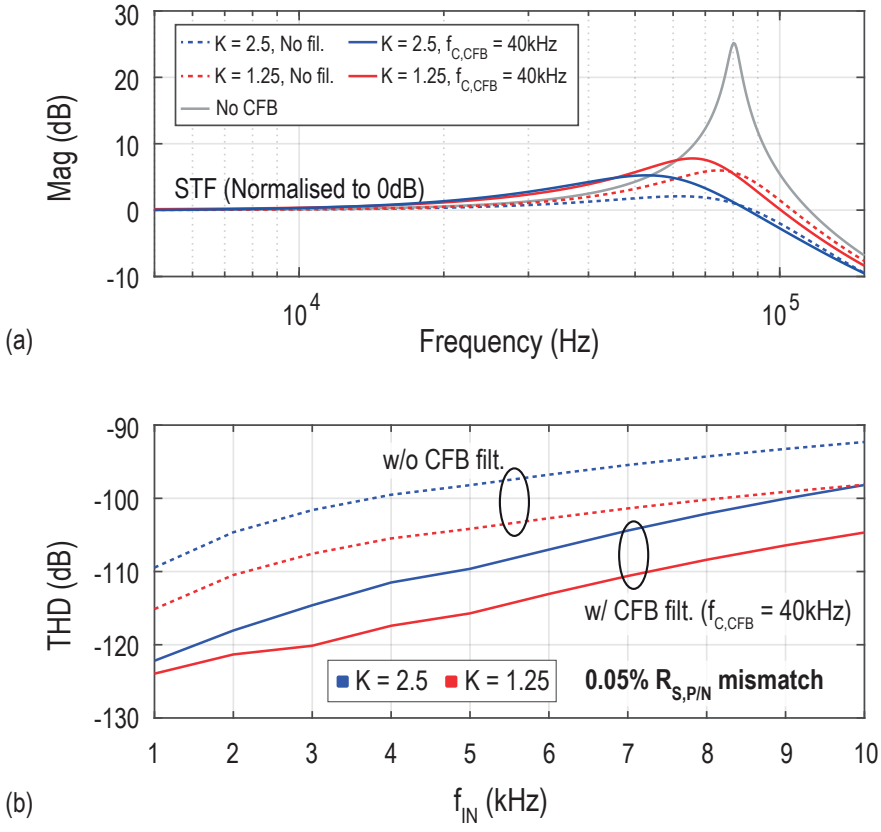


Figure 4.5: (a) Simulation results ($\beta_{VFB} = 1/8$, $C_L = 4\mu$F, $R_{S,P/N} = 20$ mΩ) illustrating- (a) the effect of effective CFB gain- K on the LC peaking in the STF (norm. to 0dB), and (b) improvement in THD with audio band CFB filtering.

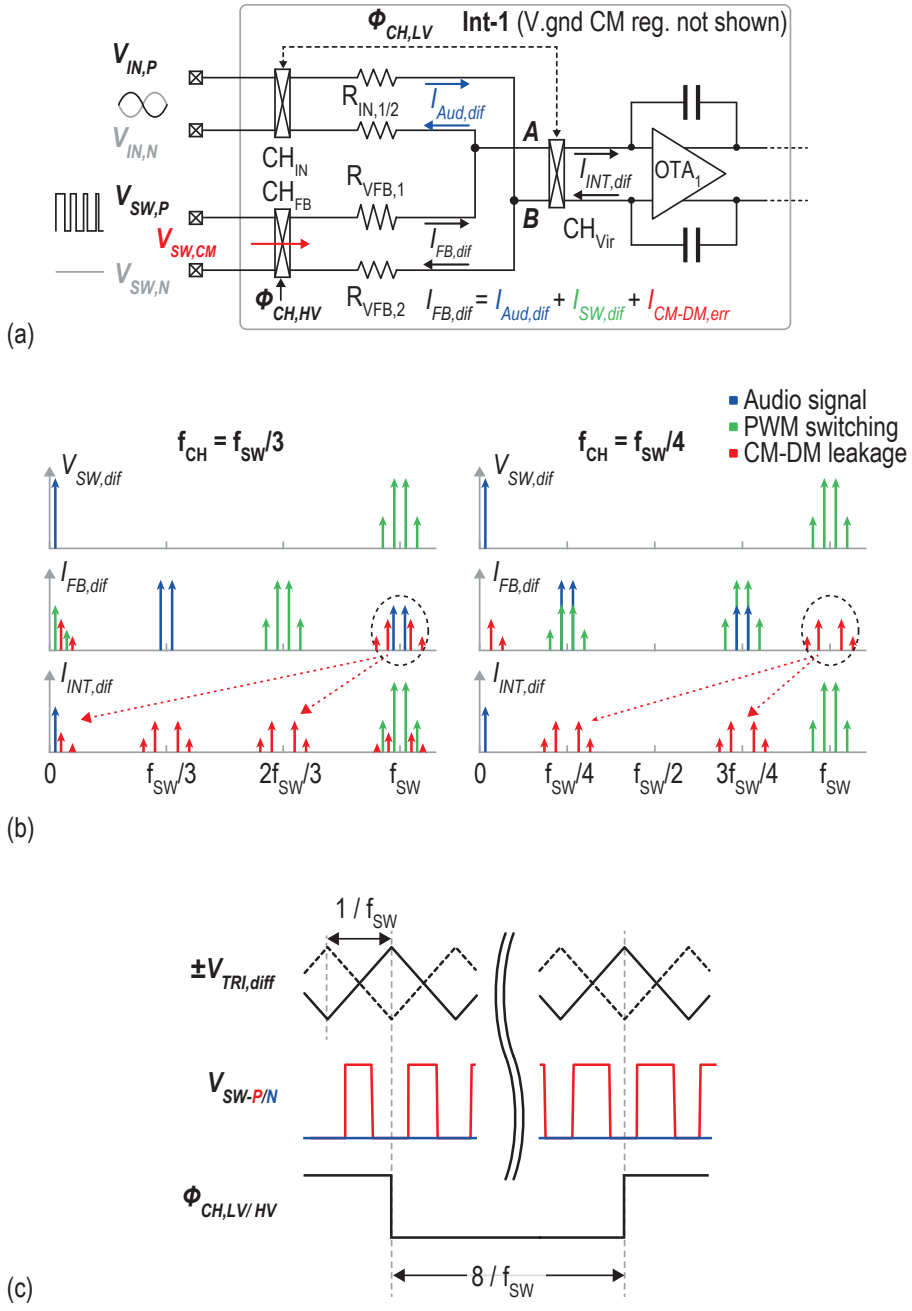


Figure 4.6: (a) Simplified block diagram of the 1st integrator and associated signals, (b) frequency domain behavior of chopping in presence of mismatch, and (c) chopping phases w.r.t. switching nodes.

4.1.4 VFB Path Nonlinearity Suppression

Although PP modulation is beneficial for low power consumption, the single-sided switching of $V_{SW,P/N}$ creates a significant amount of CM signal ($V_{SW,CM}$ in Figure 4.3) at the output. $V_{SW,CM}$ not only comprises of high- frequency components at the PWM switching frequency (f_{SW}) and its harmonics, but also distorted low-frequency components in the audio band. Any mismatch in the 1st integrator's input stage or the feedback resistor pairs (R_{IN} and R_{VFB}) will reduce its CMRR, thus causing the distorted audio band CM content to leak into the differential-mode (DM) feedback path and degrade THD. In a conventional AD/BD modulated output-stage, since the low-frequency component of $V_{SW,CM}$ is just a DC signal, the effects of CM-DM leakage within the audio band can be mitigated by a CM regulation loop [10]. However, this is not possible with PP modulation, due to the inherent low frequency components of $V_{SW,CM}$. Therefore, in this work, choppers are employed to dynamically match the R_{IN} and R_{VFB} pairs, and thus mitigate CM-DM leakage.

A simplified block diagram of the 1st integrator with choppers around $R_{IN,1/2}$ / $R_{VFB,1/2}$ is shown in Figure 4.6 (a). Due to the mismatch between $R_{VFB,1/2}$ a distorted DM feedback error current ($I_{CM\text{-}DM,err}$) is created by the nonlinear CM output voltage $V_{SW,CM}$. Since $V_{SW,CM}$, and therefore $I_{CM\text{-}DM,err}$, have content both in the audio band and around f_{SW} (and its harmonics), f_{CH} must be chosen to avoid modulating components of $I_{CM\text{-}DM,err}$ into the audio band. The frequency domain activity is shown in Figure 4.6(b). Ideally, the DM switching output of the Class D amplifier ($V_{SW,dif}$) only consists of a linear audio signal (blue) and PWM switching sidebands at f_{SW} (green). If this is chopped at an odd subharmonic of f_{SW} (e.g. $f_{CH} = f_{SW}/3$), the upmodulated audio feedback current ($I_{Aud,dif}$) overlaps with error tones of $I_{CM\text{-}DM,err}$ (red) at f_{SW} (circled). The latter will thus be modulated to the audio band by the chopper at the integrator's virtual ground (CH_{Vir}). In comparison to chopping an AD modulated output stage [14], where both $V_{SW,CM}$ and $I_{CM\text{-}DM,err}$ have negligible content in the audio band, the distortion due to $I_{CM\text{-}DM,err}$ foldback in PP modulation can be significant. This is avoided by chopping at an even subharmonic of f_{SW} (e.g. $f_{CH} = f_{SW}/4$), as the resulting foldback is now outside the audio band. Furthermore, this choice ensures that the chopping transitions always occur when both $V_{SW,P/N}$ are grounded as shown in Figure 8(c), minimizing the output-stage-state dependent delays and glitches of the HV feedback choppers [11]. To avoid the adverse effects of a high chopping frequency, such as clock feed-through and charge injection at the 1st integrator's virtual ground, while also maintaining an adequate margin from the audio band edge, f_{CH} was set to 125 kHz ($= f_{SW}/16$) in this work.

4.2 Circuit Implementation

Figure 4.7 shows a simplified top-level schematic of the proposed CDA. The output stage is powered from PVDD (14.4 V) and switches at $f_{SW} = 2$ MHz. Except for the output stage, the feedback chopper (CH_{FB}), and the input switches of the CFB network, all other blocks operate at LV, and are realized using area and power-efficient 1.8 V devices. They include a fully-differential 3rd order loop filter, a virtual ground CM regulator for Int1, the CFB network feeding into Int2, and a PP PWM modulator that generates the control signals for the HV output stage and the CFB interface switches.

4.2.1 Loop Filter and Int-1 Virtual Ground CM Regulator

A 3rd order loop filter is realized with a cascade of active-RC integrators in a feed-forward (CIFF) configuration, to create high loop gain around the output stage. The unity-gain frequency of the loop, $f_{UG,Loop}$, is 570 kHz, which satisfies the stability criteria ($f_{UG,Loop} < f_{SW}/\pi$) [12]. At this frequency, the CFB path gain is significantly lower than the VFB path gain, allowing the CDA to handle a sufficiently high f_{LF} (~ 200 kHz) without compromising on loop stability (phase margin > 50°) and thereby making it robust to f_{LF} spread. A closed-loop gain of 8x is set by R_{IN} and R_{VFB}. High density MIM capacitors are used to realize the RC time constants. They are made 2-bit trimmable to compensate for the RC process spread.

As shown in Figure 4.8, the single sided switching of $V_{SW,P/N}$ also creates a non-linear CM signal at the 1st integrator's virtual ground $V_{vir,CM} = (V_{vir+} + V_{vir-})/2$, which can swing from ~0.8 V to ~1.6 V in the absence of any regulation (shown in grey). This non-linearity in $V_{vir,CM}$ then leaks into the loop filter due to CM-DM leakage induced non-linear currents in C_{INT1} in the presence of any mismatch in integrating capacitors (C_{INT1}) or a finite CMRR in OTA_1, degrading the overall THD at the output. To relax the matching constraints on C_{INT1} and improve the CMRR of OTA_1, a separate virtual ground CM regulator is used, as shown in Figure 4.7. It detects $V_{vir,CM}$ through $R_{CM,in}$ and regulates it by sinking / sourcing currents through $R_{CM,out}$ to a fixed DC value- $V_{CM,ref}$ (~1.1 V), as shown by the black waveform of $V_{vir,CM}$ in Figure 4.8. The loop gain and bandwidth of the CM regulation loop are optimized to ensure a fast and accurate settling of $V_{vir,CM}$ during the high-frequency switching of $V_{SW,P/N}$, also illustrated in the zoomed-in inset. Additionally, the CM regulation loop also reduces the input CM swing requirements on OTA_1 drastically. To relax the matching constraints of the $R_{CM,in}$ and $R_{CM,out}$ pairs, they are also dynamically matched by connecting them before CH_{Vir}. Capacitor pairs $C_{CM,in}$ and $C_{CM,out}$ enable a fast transient response.

The noise of the Class-D amplifier is mainly dominated by R_{IN} (20 kΩ), the noise of OTA_1, and $R_{CM,out}$. While the contribution of $R_{CM,out}$ can be reduced by increasing its resistance, the swing required ($V_{O,CM,reg}$ in Figures 4.7 and 4.8) at the output of A_{CM} would increase. Therefore, as a tradeoff between noise and swing, $R_{CM,out}$ is set to 25 kΩ.

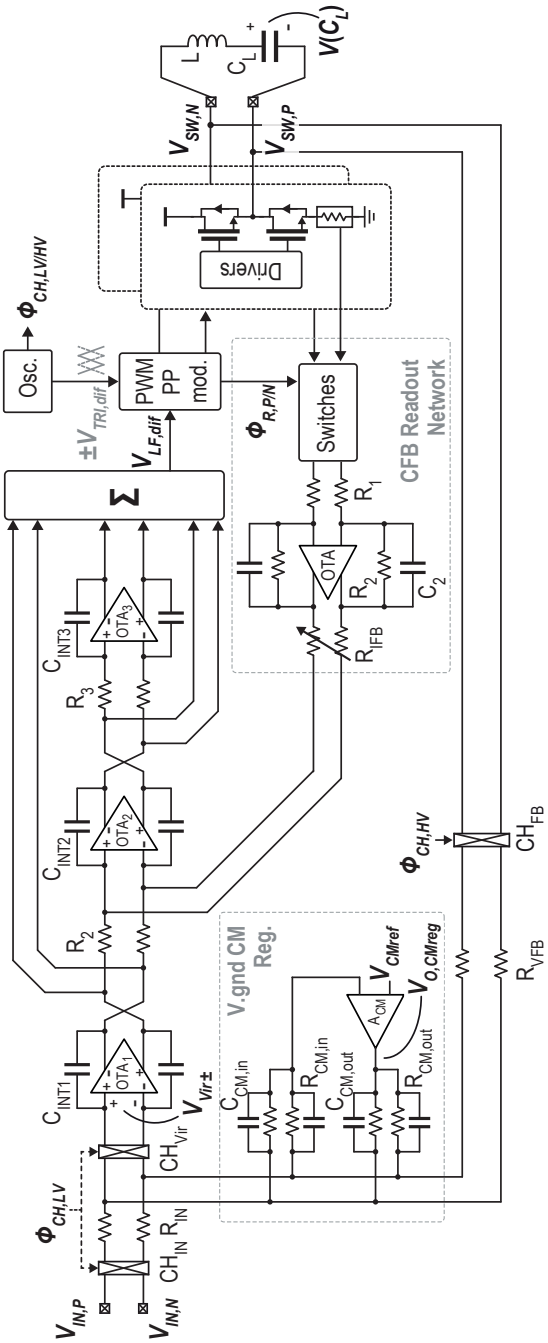


Figure 4.7: Schematic of the loop filter and CFB readout network.

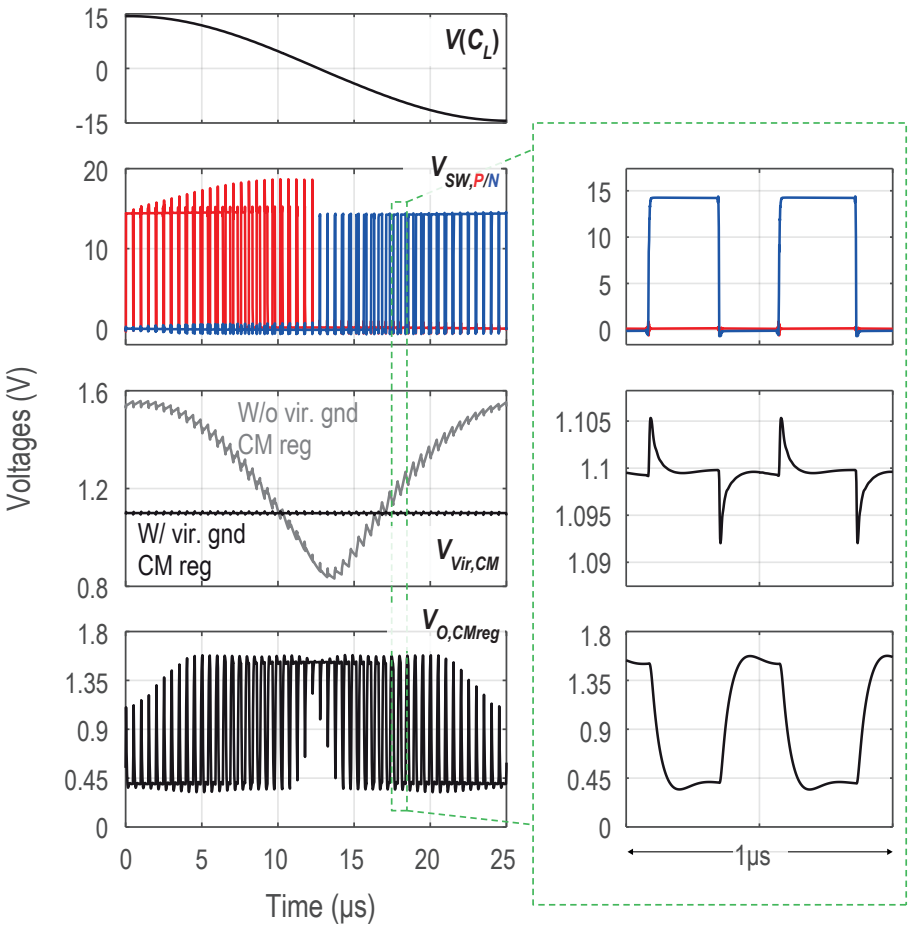


Figure 4.8: Effect of the single-sided switching on the first integrator's virtual ground CM voltage with and without the virtual ground CM regulator.

4.2.2 Choice of R_S and CFB Readout Network

In this work, diffusion resistors ($R_{S,P/N}$ ~20 mΩ) are used to sense the load current. they are sized to satisfy current-density limits, while ensuring adequate voltage linearity across the expected range of load currents. Compared to diffusion resistors, metal resistors have significantly lower sheet resistance (lower area) and better voltage linearity. However, their temperature dependence is much larger, leading to greater CFB non-linearity due

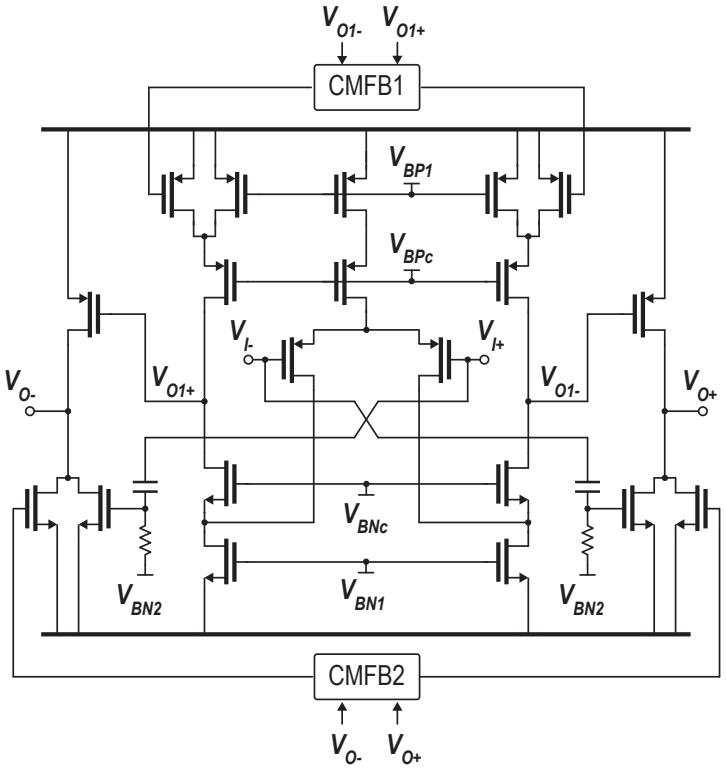


Figure 4.9: Schematic of the two-stage OTA used in the CFB network.

to self-heating. Despite their lower temperature dependence, poly-silicon resistors were not used due to their larger sheet-resistance.

The choice of effective CFB gain K is a trade-off between the non-linearity of the CFB path and the amount of damping required, as shown in Figure 4.5. As a compromise between the two, K is programmable between 1.25 and 2.5, which limits the LC damping to ~4 to 8 dB for a 4 μF capacitive load. Figure 4.7 shows the implementation of the CFB path around 2nd integrator (Int2) using an active-RC filter. The DC scaled passband gain- K' from Equation 4.5 is set by R_2, R_1, and R_{IFB}, while the low-pass filter cutoff at 40 kHz is set by R_2, C_2. K' is made programmable by adjusting the feedback current into Int2 with R_{IFB}. A two-stage OTA, shown in Figure 4.9, is used to achieve a high inband gain and linearity while satisfying the input and output swing requirements. It comprises of a conventional PMOS input folded-cascode input stage, to handle the low CM input, along with a Class-A biased output stage that provides adequate output swing.

A feed-forward compensation network, realized by capacitively coupling the inputs to the inputs of the second stage, ensures stability [13].

Chopper Network

The HV chopper (CH_{FB}) uses 20 V LDMOS devices to handle the 14.4 V signals swings at $V_{SW,P/N}$ [11]. The design of CH_{FB}, and those of the peripheral circuits required to drive the HV switches, are adopted from [11]. The choppers at the input (CH_{IN}) and virtual ground (CH_{Vir}) use 1.8 V devices. Both of them are bootstrapped to achieve adequate linearity and avoid the use of unnecessarily large switches which would then cause significant charge injection and clock feed-through [11].

4.3 Measurement Results

A prototype resistor-less Class-D piezoelectric speaker driver was fabricated in a 180 nm BCD process. Figure 4.10 shows a die micrograph of the prototype, which occupies 7 mm^2. It is powered from 14.4 V / 1.8 V (*PVDD* / *AVDD*) supplies and drives a 4 μF capacitor in series with a 1.1μH inductor (f_{LC} ~75kHz). During idle-channel operation, the amplifier consumes 122.4 mW / 9mW from *PVDD* / *AVDD*. Of the total power consumption, the additional sense resistors and CFB readout network consume $<$ 1% and ~0.6%, respectively.

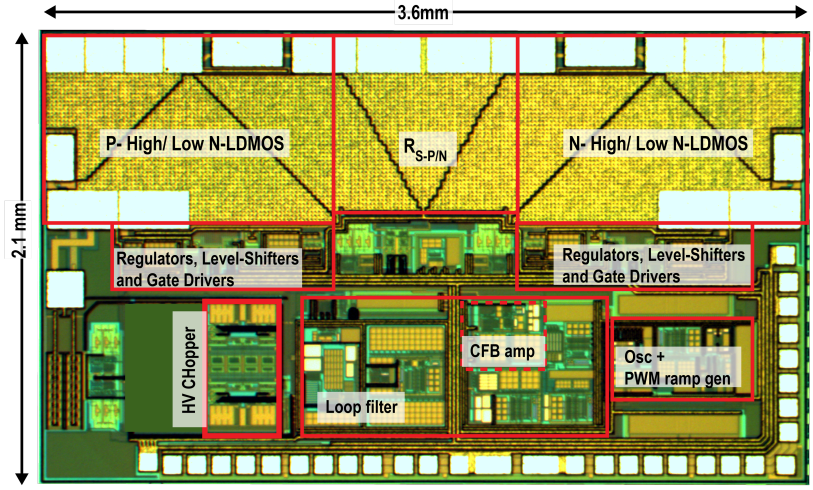


Figure 4.10: Die-micrograph of the prototype Class-D piezoelectric speaker driver.

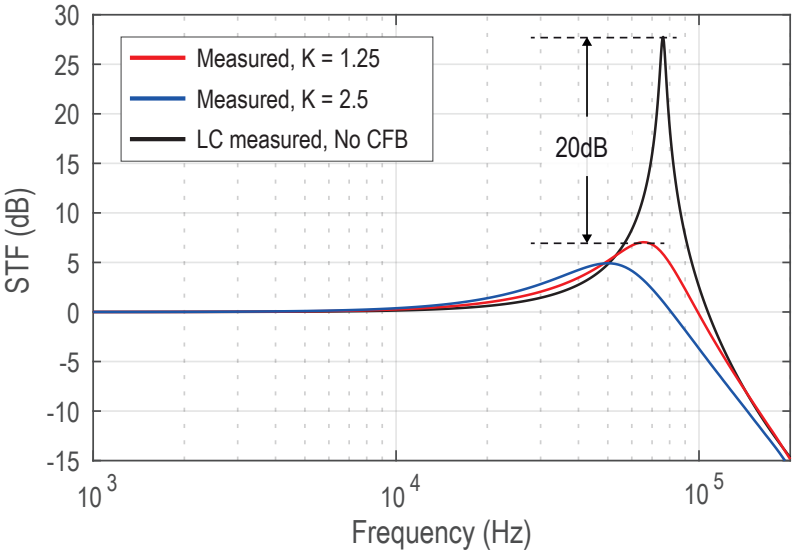


Figure 4.11: Effect of CFB on the LC peaking in the STF (normalized to 0dB).

All audio measurements were performed using an Audio Precision APX-555 in combination with an AES17 filter. Figure 4.11 shows the efficacy of the dual voltage/current feedback topology in damping the LC resonance. An impedance analyzer was used to extract the undamped LC transfer on the test PCB itself. Two CFB gain settings, corresponding to effective CFB gains of $K = 1.25$ and $K = 2.5$, show that the STF peaking can be suppressed by 20 dB and 22 dB respectively.

Figure 4.12 shows the measured output spectrum when driving the 4 μF load with a 5 V_{RMS} signal for a $K = 1.25$ and $K = 2.5$. For an input frequency of 1kHz, the THD+N is -86.8 dB / -86.5 dB for $K = 1.25$ / 2.5. Due to the smaller load current at this frequency, the linearity is primarily limited by the HV choppers in the VFB path. With the larger load current at f_{IN} = 6 kHz, the CFB path also contributes to nonlinearity. The THD+N in this case is -90.9 dB / -85.4 dB for $K = 1.25$ / 2.5. Figure 4.13 shows the THD+N across output amplitude for input frequencies of 1 kHz and 6 kHz for both the CFB gains. With $K = 1.25$, the THD+N peaks at -87.3 dB and -91.1 dB for a 1 kHz and 6 kHz input frequency respectively. With the higher CFB gain of K =2.5, the peak THD+N numbers are similar to $K = 1.25$. However, at amplitudes close to FS (V_O ~ 7-8 V_{RMS}) for the larger load currents with the 6 kHz input frequency, the THD+N with $K = 1.25$ is ~ 8 dB better than with $K = 2.5$, thus demonstrating a better linearity due to the lower CFB gain. The reduction in THD+N for $K = 2.5$ in this case is primarily attributed to the self-heating of $R_{S,P/N}$. Figure 4.14 shows the THD+N

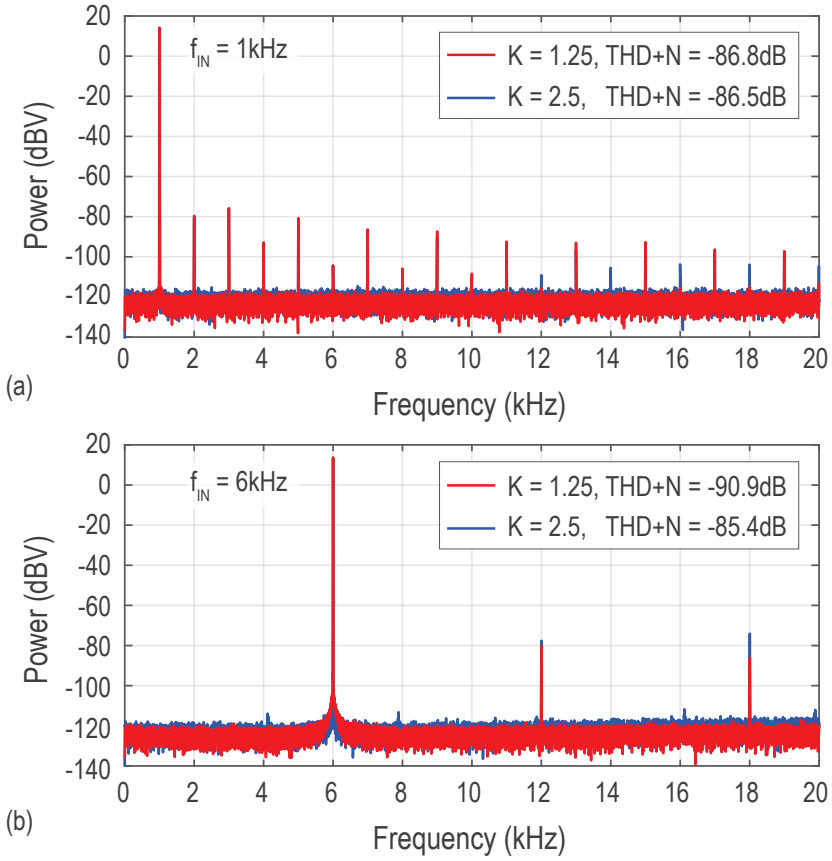


Figure 4.12: FFT at $V_O = 5$ V_{RMS} for (a) $f_{IN} = 1$ kHz, and (b) $f_{IN} = 6$ kHz.

across frequency for a fixed V_O = 5 V_{RMS}. Beyond 10 kHz, the THD+N is purely noise limited. The amplifier has an A-weighted output noise of 45 μV_{RMS} and a dynamic range of 106.5 dB (measured using a -60 dBFS input).

Figure 4.15 shows the measured power consumption of the amplifier when driving the 4 μF load with different input frequencies. It can deliver a peak current of 4.4 A_P, which corresponds to V_O = 10.2 V_{RMS} (FS) at an input frequency of 12 kHz. In this situation, the amplifier consumes 4.9 W, which is mainly dominated by the conduction and switching losses of the amplifier. As per simulations for the same condition, the sense resistors account for 8-10% of the total power consumption. To get an estimate of the power savings achieved in comparison to a conventional Class-D amplifier with a series R_{EXT}, the power losses were emulated for resistors that provide the same damping

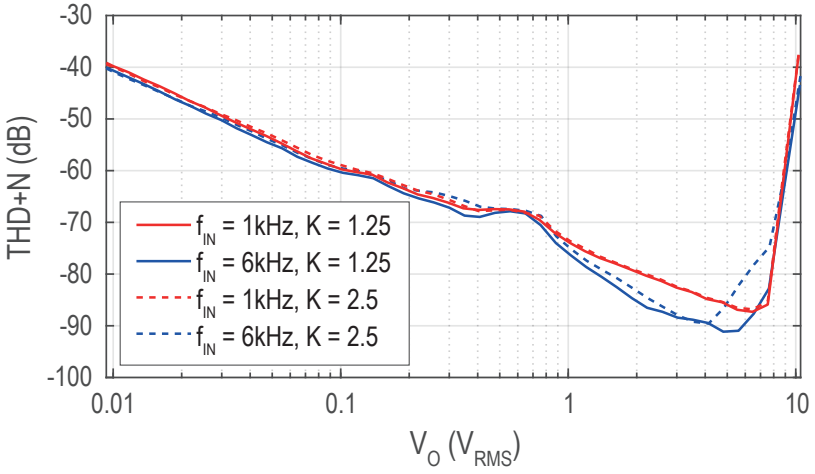


Figure 4.13: THD+N across V_O.

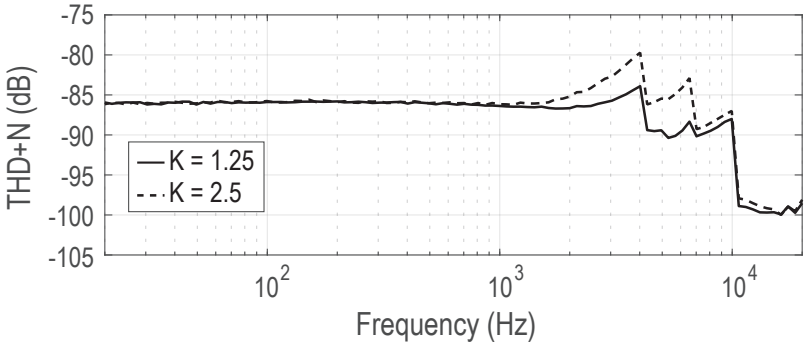


Figure 4.14: THD+N across frequency ($V_O = 5\text{V}_{\text{RMS}}$).

as the CFB gains used. An additional power of ~1.9W and ~3.5W is then lost in a R_{EXT} = 0.2 Ω ($K =$ 1.25) and $R_{EXT} =$ 0.35 Ω ($K =$2.5), respectively. Due to the capacitive loading, the power consumption decreases with decreasing frequency.

Figure 4.16 shows the PSRR of the amplifier (7 samples) when the supply is perturbed by a 1 V_{RMS} sinewave across frequency. Due to chopping, the amplifier's PSRR is insensitive to the mismatch of the R_{IN} / R_{FB} pairs. Although the relatively large spread in PSRR at low frequencies is not well understood, possible causes include an over-estimation in the degree of matching in the HV chopper devices, along with off-chip component variations across different daughter-boards for the 7 samples. The

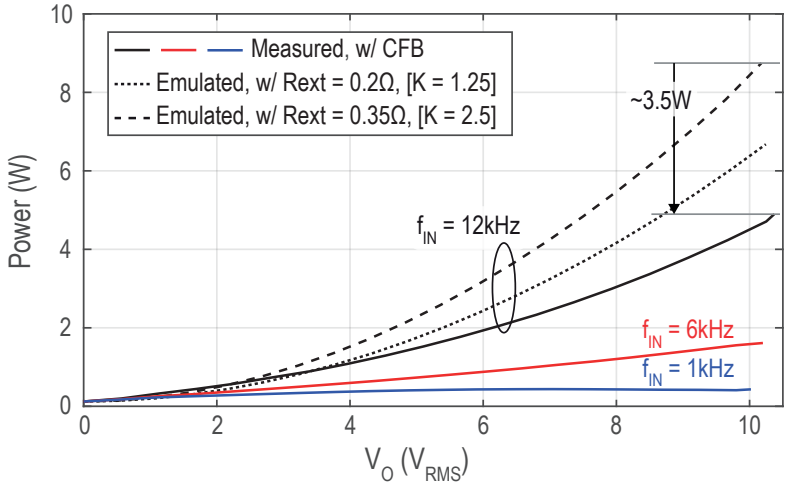


Figure 4.15: Power consumption vs V_O and f_{IN} for $C_L = 4\ \mu$F.

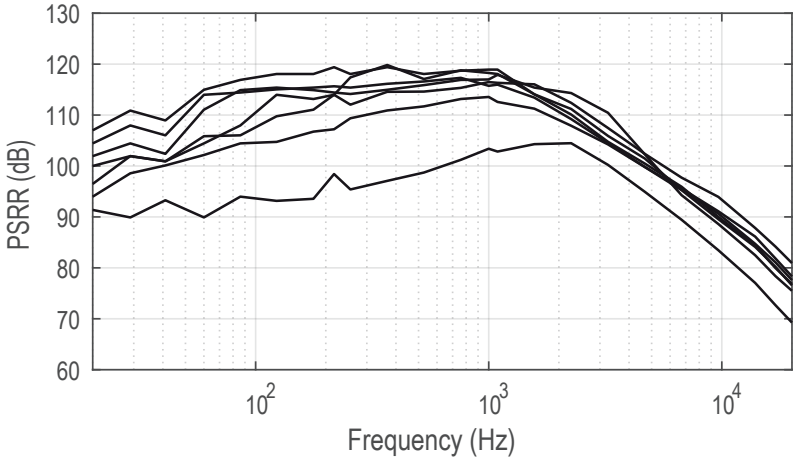


Figure 4.16: PSRR of the amplifier (7 samples).

PSRR roll-off beyond 1 kHz is attributed to limitations in the measurement setup, such as a finite CMRR of the analyzer and on-board asymmetric coupling from supply to the output nodes. Overall, for all 7 samples, the PSRR is $>$ 100dB at 1kHz and $>$ 68dB in the entire audio band.

A comparison of the performance of this amplifier with other state-of-the-art designs

is shown in Table 4.1. Among all the piezoelectric speaker drivers, it uses the minimum number of off-chip components, while being capable of driving a 4 μF capacitive piezoelectric speaker load.

4.4 Conclusion

A resistor-less Class-D piezoelectric speaker driver using a dual voltage and current feedback topology is presented. Current feedback enables resistor-less LC resonance damping, thereby enabling a low power system at reduced cost. In addition, a push-pull modulated output stage lowers the power consumption of the amplifier itself. Linearity is improved by employing chopping in the voltage feedback loop and suppressing the current feedback loop gain in the audio band. The amplifier can deliver 4.4 A_P while

Table 4.1: Performance summary and comparison.

Parameter	**This work**		DRV5825P [14]		LM48560 [15]	MAX9788 [16]	TPA2100P1 [17]
Architecture	**Analog in, Class-D**		Digital in, Class-D		Analog in, Boost + Class-H	Analog in, Boost + Class-G	Analog in, Boost + Class-D
			1 channel	2 channel			
Supply (V)	**14.4**		12	24	3.6	3.6	3.6
Piezo Load (µF)	**4**		1	4	1.5	1	1
Resistor-less	**Yes**		Yes		No	No	No
Configuration	**L + C_L**		2L + 2C + C_L		R + C_L	R + C_L	R + L+ C_L
I_Q (mA)	**8.5**		37	130	4	8	5
P_Q (mW)	**122.4**		444	3120	14.4	28.8	18
THD+N_{PEAK} (dB) (f_{IN} = 1k)	**-87.3 (K=1.25)**	**-86.8 (K=2.5)**	-77.0	-77.6	-66.0	-94.0	-66.0
THD+N_{PEAK} (dB) (f_{IN} = 6k)	**-91.1 (K=1.25)**	**-89.5 (K=2.5)**	-	-	-	-	-
Dynamic Range (dB) [A-wt.]	**106.5**		111 (24V supply)		-	106	-
SNR (dB) [A-wt.]	**105.8**		111 (24V supply)		98	108	94
Output noise (µVrms) [A-wt.]	**45**		45		134	-	-
Peak Current (A)	**4.4**		7.5	15	2.8*	1.4*	1.2*
Power Consumption (W) (C_L = 4µF, f_{IN} = 10kHz, V_O = 10V_{RMS})	**3.5**		-	13.9	-	-	-
Power Consumption (W) (f_{IN} = 1kHz, V_O = 7V_{RMS})	**0.44 (R_{EXT} = 0Ω)**		0.46* (R_{EXT} = 0Ω)	3.2* (R_{EXT} = 0Ω)	0.75* (R_{EXT} = 10Ω)	0.35* (R_{EXT} = 10Ω)	0.14* (R_{EXT} = 10Ω)
PSRR (dB) (20- 20kHz)	**> 68**		72 (f_{Supply} = 1kHz)		> 50	> 58	> 80

* Estimated from plots

consuming 122 mW during idle operation. Lastly, it achieves a competitive DR, output noise, and PSRR.

4.5 References

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Chapter 5

A Class-D Piezoelectric Speaker Driver Using a Quadrature Chopping Scheme

As was shown in the previous chapter, by employing dual voltage/current feedback topology, the output impedance of a Class-D amplifier (CDA) can be designed to damp LC resonance, eliminating the need for an external damping resistor and therefore reducing its associated power consumption, cost and size. This is combined with push-pull modulation, to minimize idle power consumption, and chopping, to ensure a good PSRR and THD. However, due to the large difference in the input and output signal swings (1.8 V / 14.4 V), the output choppers are realized with high-voltage (HV) devices, while the input choppers are realized with low-voltage (LV) devices. This, in turn, inevitably results in a timing skew of a few ns between their chopping transitions, which degrades both the noise and the large signal THD of the amplifier. In [1], a replica-based timing skew correction for the HV choppers is proposed, but circuit mismatch limits the residual timing skew to hundreds of picoseconds. In this work, a skew-insensitive chopping is proposed to reduce this to tens of picoseconds.

5.1 Quadrature Chopping Scheme

Figure 5.1 shows the architecture of the proposed CDA. It consists of dual voltage/current feedback to damp the LC filter in a power-efficient manner [2], a 3rd order loop filter to achieve high audio band loop gain, a resistive feedback network to define a closed-loop gain of 8x, and the proposed quadrature chopping scheme (QCS). To understand the benefits of QCS, details regarding the output stage modulation scheme and the corresponding chopping scheme are elaborated in the following.

This chapter is based on the conference paper: S. Karmakar *et al.*, "A Class-D Piezoelectric Speaker Driver Using A Quadrature Feedback Chopping Scheme achieving 29dB Large-Signal THD+N Improvement," in *Proc. Symp.VLSI Circuits*, 2023, pp. 1-2.

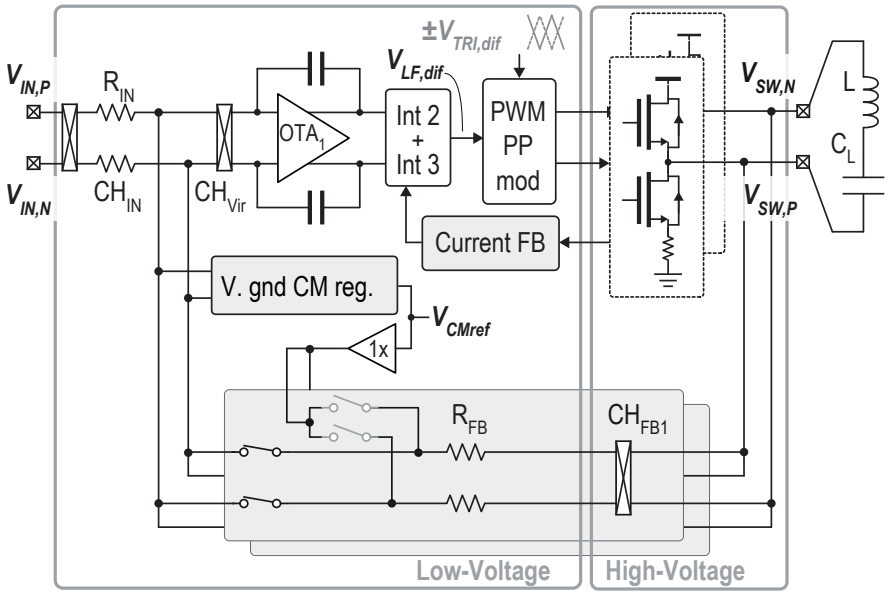

Figure 5.1: Simplified block diagram of the CDA employing dual voltage/ current feedback and a quadrature chopping scheme.

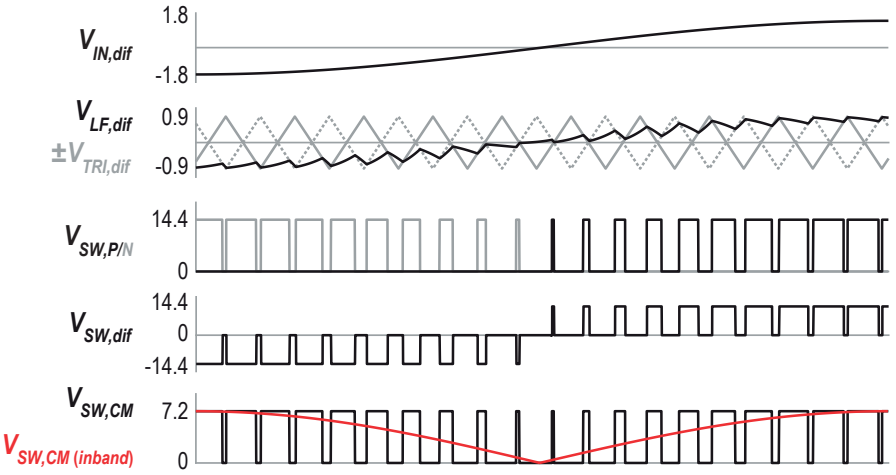

Figure 5.2: Output waveforms of the amplifier with in-band CM content shown in red.

5.1.1 Push-Pull Output Stage and Chopping Frequency- f_{CH}

As discussed in Chapter 4, the CDA employs PP modulation to achieve low idle power [2], which is highly desirable in battery-powered systems. As illustrated by the timing

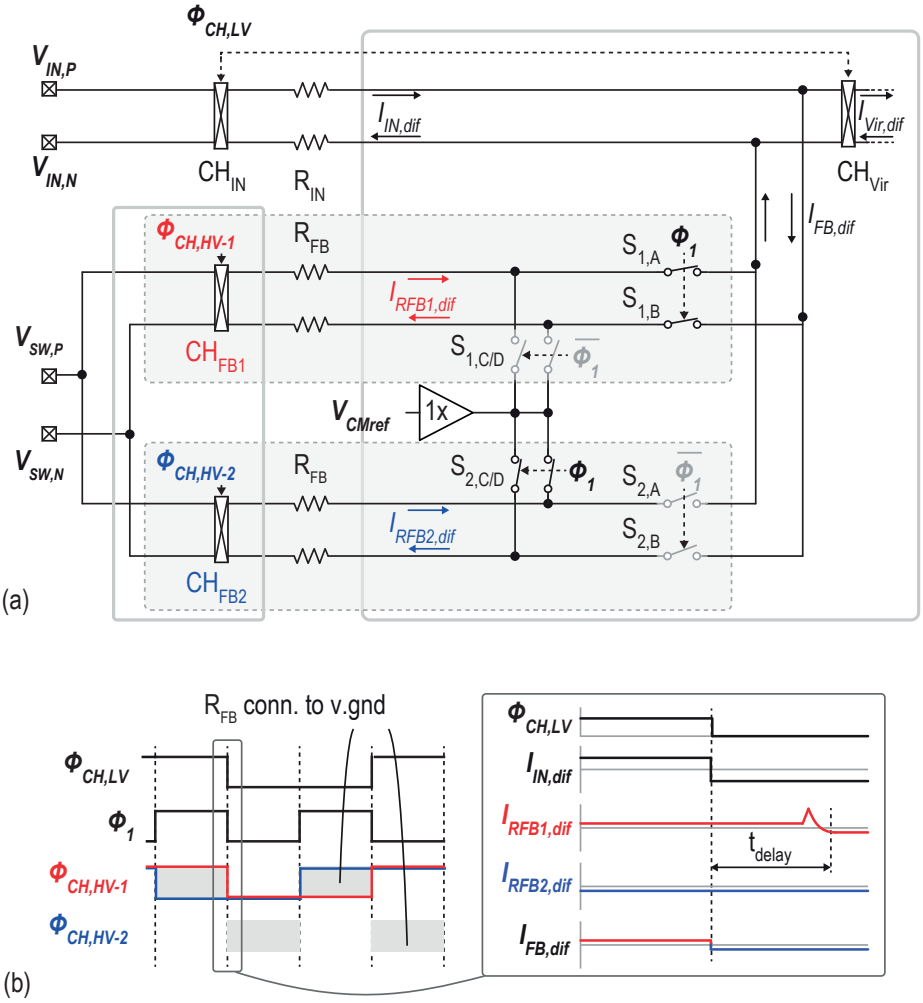

Figure 5.3: (a) Simplified block diagram of the dual HV choppers, and (b) time domain waveforms of associated signals.

waveforms in Figure 5.2, this is because, depending on the polarity of the input signal, only half of the H-bridge switches, reducing gate-charging losses and ripple losses compared to the use of AD modulation [2]. However, for signals near zero-crossings, the modulator produces narrow pulses, resulting in crossover distortion. Furthermore, the single-sided switching creates non-linear CM content both in the audio band and at the switching frequency (f_{SW}). This results in CM-DM leakage in the presence of mismatch between the input / feedback resistor pairs (R_{IN} and R_{FB}) of the 1st integrator and, therefore, in extra distortion. While crossover distortion is suppressed by high loop-gain, chopping is needed to mitigate resistor mismatch.

As was explained in Chapter 4, an effective way of mitigating CM-DM leakage is by chopping the feedback network at an even subharmonic of f_{SW}. Choosing $f_{CH} = 125$ ($f_{CH} = f_{SW}/16$), keeps it low, while maintaining an adequate margin with respect to the audio band edge. However, since the output choppers are made with large HV devices, the resulting delays and glitches will cause large-signal distortion and intermodulation between the audio signal and PWM switching. To minimize these chopping non-idealities in a robust way, QCS is proposed

5.1.2 Quadrature Chopping Scheme

Chopping non-idealities primarily arise because the feedback chopper (CH_{FB}) is realized with large LDMOS (20 V) transistors. Its driving circuits then add extra delay to the switching transitions of CH_{FB} compared to those of CH_{IN} and CH_{Vir}, which are realized with faster core LV (1.8 V) devices. Additionally, the feedback resistors (R_{FB} = 160 kΩ) also introduce delay due to their intrinsic parasitic capacitances. Together, these delays degrade linearity, especially at signals close to full-scale (FS), and also cause high-frequency noise from around $2f_{CH}$ to fold back into the audio band, increasing the noise floor.

QCS was initially proposed in [3], where it is referred to as the fill-in technique, to minimize intermodulation between input signals near harmonics of $2f_{CH}$. Although this is not an issue in the proposed CDA since the input audio signal is sufficiently bandlimited, it can significantly improve the linearity of the PWM signals close to full scale. As shown in Figure 5.3 (a), QCS uses a pair of quadrature phase-shifted choppers and two HV feedback paths to mitigate the effect of the timing skew and delay caused by the HV choppers and the resistors. Both feedback paths are nominally identical and are chopped at the same frequency f_{CH} but with quadrature chopping clocks (Figure 5.3 (b)). Multiplexing switches ($S_{1/2,A/B}$) at the integrator's virtual ground CH_{Vir} only connect a resistor pair to the virtual ground a quarter cycle after it is chopped at $V_{SW,P/N}$, represented by the shaded areas in $\Phi_{CH,HV\text{-}1/2}$ in Figure 5.3 (b). At the same time, the previously connected pair is disconnected to undergo chopping at $V_{SW,P/N}$. This quarter-cycle delay provides ample settling time for any HV chopper-induced transients or overall delays (t_{delay}) in the feedback current. When disconnected from the virtual ground, the feedback network is connected to a separate buffer at the same CM voltage

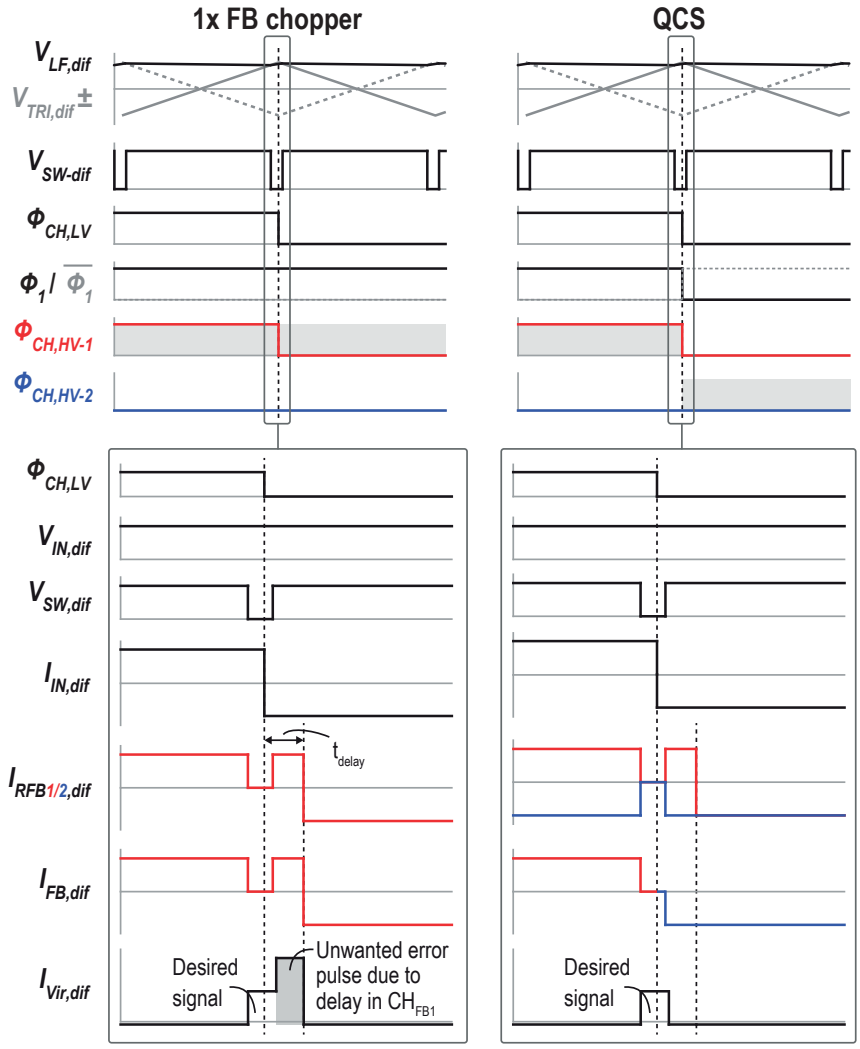

Figure 5.4: Effect of QCS in mitigating errors in feedback current in comparison to a single CHFB, for large signal amplitudes.

as the virtual ground ($V_{CM,ref}$) through switches- $S_{1/2,C/D}$, thereby ensuring a glitch-free feedback current. Consequently, the effective chopping transitions in the feedback path are determined by $S_{1/2,A/B}$, rather than by the HV chopper switches. Since CH_{IN} / CH_{Vir} and $S_{1/2,A/B}$ all use core LV 1.8 V devices, their timing can be accurately matched, and

their intrinsic delay (∼20 ps) is much lower than that of $CH_{FB,1/2}$ (∼2 ns).

The effect of chopping PP modulated PWM signals close to FS is illustrated in the time domain in Figure 5.4. While synchronizing the chopping clock edges with the peaks of $\pm V_{TRI,dif}$ facilitates chopping when both $V_{SW,P/N}$ are low [2], the available time decreases drastically as the input approaches the full-scale (FS). With a single feedback chopper (CH_{FB1}) [2], a delay in the current $I_{RFB1,dif}$ (t_{delay}) would then create a non-linear error pulse in $I_{Vir,dif}$ due to the low-to-high transition of $V_{SW,dif}$ (shaded area in Figure 5.4). This error is eliminated by QCS as the mux swiftly switches over to $I_{RFB2,dif}$, which is already chopped and settled, thereby avoiding any error pulse in the feedback current.

The HV choppers $CH_{FB,1/2}$ are identical, and together with all the peripheral circuits, are adopted from [1]. The buffer provides an output voltage of $V_{CM,ref} \sim 1.1$ V, and sources/sinks currents from the R_{FB} pair disconnected from the virtual ground. The choppers at the input and virtual ground are made using 1.8 V devices and are bootstrapped for adequate linearity and to reduce their size.

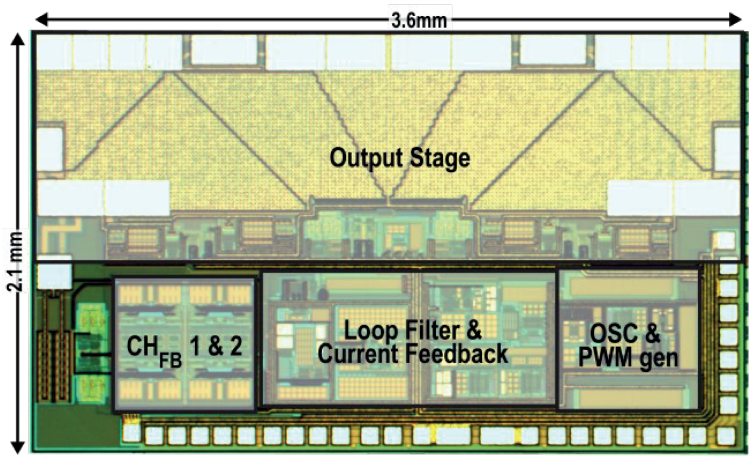

Figure 5.5: Die-micrograph of the prototype Class-D piezoelectric speaker driver.

5.2 Measurement Results

As shown in Figure 5.5, the prototype is designed in a 180 nm BCD process and occupies an active area of 7.1mm^2. The HV and LV chopper networks together occupy 6% of the total active area. The chip is powered from 14.4 V / 1.8 V supplies (PVDD /

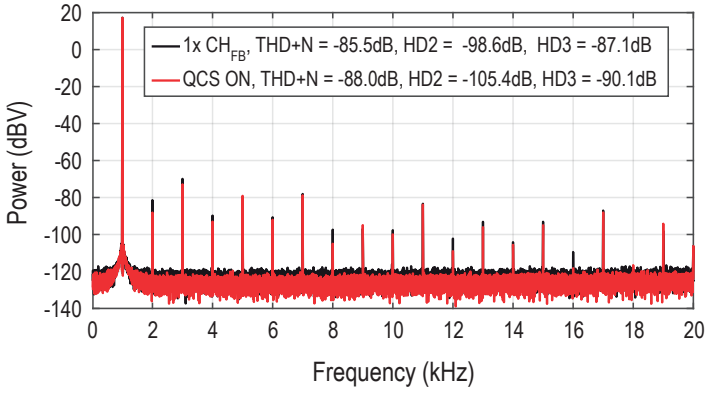

Figure 5.6: FFT of the output for $V_O = 7.5$ V_{RMS} for $f_{IN} = 1$ kHz.

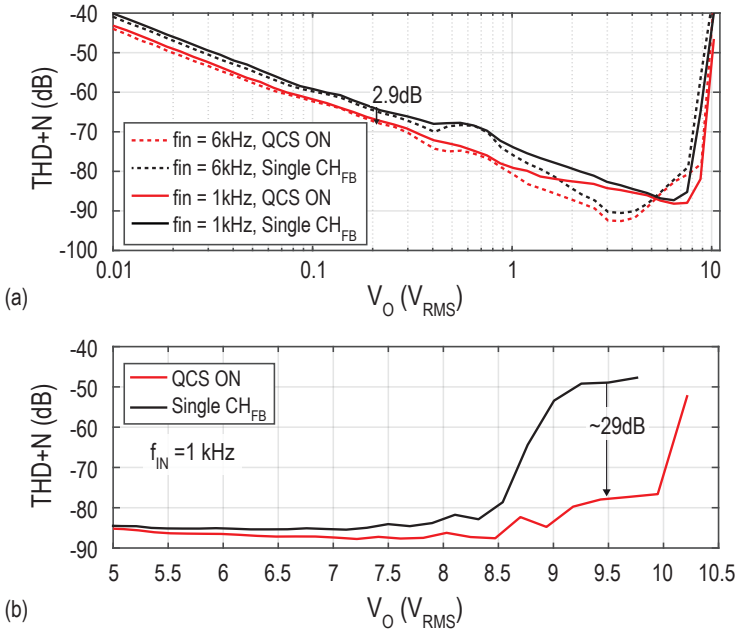

Figure 5.7: (a) THD+N across V_O, and (b) THD+N for signals close to FS.

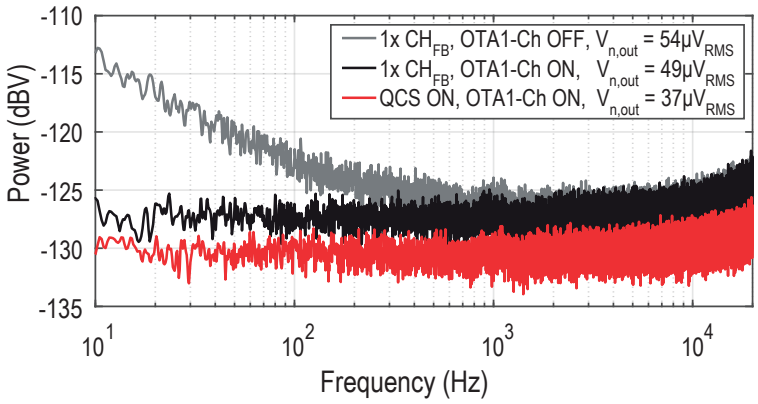

Figure 5.8: Output spectra during idle channel.

AVDD) and is loaded by a 4 μF capacitor in series with a 1.1 μH inductor. During idle operation, the amplifier consumes 8.7 mA from PVDD and 5 mA from AVDD.

Figure 5.6shows the measured FFT spectrum for a 1 kHz input frequency with the QCS technique ON and OFF (using a single CH_{FB}) when delivering 7.5 V_{RMS} output. With QCS ON the THD+N is -88 dB, and with QCS OFF is -85.5 dB. Across output amplitudes, as shown in Figure 5.7 (a), the THD+N improves by 2.9 dB for small signals with QCS enabled, and is mainly attributed to the reduction in noise foldback due to QCS. The amplifier attains a peak THD+N of -88 dB / -92.5 dB for 1 kHz / 6 kHz input with QCS enabled. A significant improvement is seen for larger signal amplitudes as shown in Figure 5.7 (b), the THD+N improves by $\sim$29 dB at an output voltage $\sim$9.5 V_{RMS} with the QCS technique enabled in comparison to using a single CH_{FB}.

Figure 5.8 shows the output noise spectra. With QCS ON, the output noise also improves from 49 μV_{RMS} to 37 μV_{RMS} (A-weighted), due to the reduction in noise folding. Figure 5.9 shows the PSRR of the amplifier to be > 80 dB across the audio band. Table 5.1 summarizes the performance of the proposed piezoelectric driver and compares it with the state-of-the-art. Among the resistor-less piezoelectric speaker drivers, this work achieves the best THD performance and PSRR.

5.3 Conclusion

This paper proposes a robust HV chopping technique for Class-D amplifiers to mitigate the stringent delay requirements in the chopper networks. Thanks to the quadrature chopping scheme, high linearity can be attained across the entire output range. In addition, the amplifier achieves competitive DR, output noise, and PSRR compared to

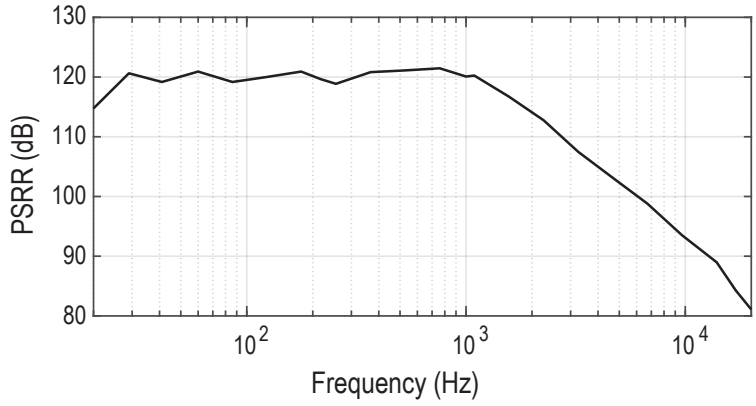

Figure 5.9: PSRR across audio band.

Table 5.1: Performance summary and comparison.

Parameter	**This work**	Karmakar [2]	DRV5825P [4]	LM48560 [5]	MAX9788 [6]	TPA2100P1 [7]
Architecture	**Analog in, Class-D**	Analog in, Class-D	Digital in, Class-D	Analog in, Class-AB	Analog in, Class-AB	Analog in, Class-D
PVDD (V)	**14.4**	14.4	24	15 (Boosted)	10 (Boosted)	10 (Boosted)
Piezo Load (µF)	**4**	4	4	1.5	1	1
Damping Resistor	**No**	No	No	Yes (10Ω)	Yes (10Ω)	Yes (10-20Ω)
I_Q (mA)	**8.7**	8.5	10.9	4	8	4
THD+N_{PEAK} (dB) (f_{in} = 1k)	**-88.2**	-87.3	-77.6*	-66*	-94.0	-65.0
THD+N_{PEAK} (dB) (f_{in} >1k)	**-92.5 (6kHz)**	-91.1 (6kHz)	-76* (5kHz)	-44.4* (5kHz)	-73.6* (10kHz)	-58.1* (10kHz)
THD+N @ 90% FS (f_{in} = 1k)	**-79.8**	-50.9	-56.2*	-46.0*	-63.1*	-64.4*
Output Swing/ FS (%) @ 60dB THD (fin = 1kHz)	**99.5**	86.9	84.9	80*	94*	95.9*
Dynamic Range (dB) [A-wt.]	**108.9**	106.5	111	-	106	-
Output noise (μV_{RMS}) [A-wt.]	**37**	45	45	134	-	120
Peak Current (A)	**4.4**	4.4	7.5	0.47*	1.4*	0.66*
PSRR (dB) (20- 20kHz)	**119 / 80 (217Hz/ 1kHz)**	93 / 68 (217Hz/ 1kHz)	72 (1kHz)	79 / 50 (217Hz/ 1kHz)	77 / 58 (217Hz/ 1kHz)	100 / 80 (217Hz/ 1kHz)

* Estimated from plots

other piezoelectric speaker drivers.

5.4 References

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Chapter 6

Conclusions

In this thesis, the development of high-performance Class-D audio amplifiers for two distinct applications has been explored: automotive audio systems with an emphasis on low EMI, and piezoelectric speaker drivers for more consumer-oriented applications. In both cases, the primary objective was to achieve high performance while minimizing the use of off-chip components, and thereby reducing system cost and size. This chapter encapsulates the primary findings of the research, highlights the original contributions made, and concludes with some proposals for future work.

6.1 Main Findings

Due to their superior efficiency when compared to Class-AB amplifiers, together with improvements in their other specifications, Class-D amplifiers (CDAs) have become ubiquitous in audio applications. However, they still have their drawbacks, mainly in terms of EMI, idle power consumption, and speaker drivability, some of which have been addressed in this work. Some of the main findings are as follows:

- Reducing the EMI of a CDA without increasing its switching frequency always leads to added cost. This is due to the need for additional off-chip components or die area, which are required to reduce the output swing, ripple currents, and radiating electromagnetic emissions. (Chapter 2).
- Alternatively, increasing the switching frequency and/or using a modulation scheme appropriate to the chosen application is relatively inexpensive. A higher switching frequency allows stringent automotive EMI standards like the CISPR-25 to be met with a significantly relaxed LC filter cut-off frequency, thereby lowering the cost and size of the filter. When combined with a hybrid $\Delta\Sigma$-PWM modulation that incorporates a loop filter with a high loop gain, good linearity across the entire input range can also be achieved (Chapter 3).
- CDAs can be readily adopted to drive piezoelectric capacitive loads. A dual feedback architecture, with a secondary current feedback (CFB) loop around a

conventional voltage feedback loop, eliminates the need for a high-power external resistor to damp LC resonance, thereby decreasing cost (Chapter 4).

- A push-pull (PP) modulation scheme reduces idle power consumption. Similar to BD modulation in most ways, PP modulation has the added advantage of facilitating of load current sensing with only low-side current sense resistors. Low-side current sensing also drastically reduces the input common-mode (CM) specification of the associated read-out amplifier as it avoids the high-frequency rail-to-rail switching signal (Chapter 4).

- When driving capacitive loads, the current-feedback (CFB) path needed for LC resonance damping can be optimally implemented by low-pass filtering the sensed current before feeding it into the input of the 2nd integrator of the loop filter. The additional noise and non-linearity of the CFB path is then suppressed by the gain of the 1st integrator, while reasonably maintaining the efficacy of the resistor-less damping approach (Chapter 4).

- With PP modulation, the CM signal of the CDA contains distorted signal components within the audio-band. This causes DM distortion due to the finite CMRR of the feedback network and the 1st integrator. Chopping the input and feedback resistors of the 1st integrator, dynamically matches them and thus improves CMRR and the overall linearity (Chapter 4).

- For a closed-loop CDA, the choice of chopping frequency is often influenced by the modulation scheme applied due to the presence of chopper-induced IMD components. In comparison to AD/ BD modulation, where an odd sub-harmonic of the switching frequency is desired, with push-pull modulation an even-sub harmonic is more beneficial (Chapters 4 and 5).

- If chopping is used to improve the matching of the feedback network of a CDA, the chopping transitions of the HV-choppers at the amplifier's output are always skewed with respect to the LV choppers at the LV input stage of the loop filter, resulting in degraded signal linearity for signals close to full-scale with push-pull modulation. This degradation can be mitigated by employing a quadrature chopping scheme instead (Chapter 5).

6.2 Original Contributions

The primary contributions of this thesis are outlined below. The distinct publications forming components of this thesis are individually referenced, with pertinent chapters also highlighted.

- A hybrid ΔΣ-PWM modulation scheme for CDAs, that employs multi-level non-uniform quantization using a ΔΣM and followed by a time-quantized PWM

generator, to drastically reduce the out-of-band EM emission in comparison to a 1-bit ΔΣM CDA while retaining the linearity benefits of the latter (Chapter 3).

- A high-performance analog-input CDA capable of meeting the CISPR 25 Class 5 EMI average limit in the AM band with 10 dB margin while using small, and thus low-cost, LC filter (150 kHz cutoff frequency), along with exceptional linearity (THD+N < − 100 dB) across a wide range of output power (28 W), efficiency (91%) and PSRR (> 70 dB) (Chapter 3).

- A dual voltage/current feedback topology for closed-loop class-D amplifiers that facilitates LC resonance damping without reliance on an external damping resistor. This resistor-free methodology not only simplifies driving a capacitive piezoelectric speaker load but also results in significant reductions in system power consumption, cost, and size, thereby optimizing the amplifier's overall efficiency and performance (Chapter 4).

- A CFB implementation in a CDA that leverages the switching dynamics of PP modulation and provides a quasi-continuous load current read-out using only low-side current sense resistors. Additional techniques, such as feedback to the 2^{nd} integrator and the incorporation of a low pass filter (LPF), are proposed to ensure minimal addition of noise and distortion by the CFB network with marginal effect on the efficacy of the dual feedback topology (Chapter 4).

- A resistor-less CDA prototype, implemented in a 180 nm BCD process, for piezoelectric speakers that incorporates a push-pull modulation scheme to achieve a low idle power consumption of 122 mW while being able to deliver a peak current of 4.4 A into a 4 μF load. A high-voltage chopping scheme, specific to push-pull modulation, to mitigate linearity degradation induced by input/ feedback resistor pair mismatch, resulting in a peak THD+N of -91 dB (Chapter 4).

- A quadrature chopping scheme for high-voltage (HV) choppers used in CDAs, that greatly improves large-signal linearity compared to conventional single feedback chopping scheme by eliminating the timing skew between low-voltage (LV) and high-voltage choppers. This is demonstrated in a prototype that shows an improvement of large-signal THD+N by 29 dB over the previous version and extends the linear output voltage swing (THD+N < -60 dB) from 86.9% to 99.5% of the full-scale (Chapter 5).

6.3 Future Work

While the work described in this thesis represents a significant step in improving the performance and usability of CDAs, it does not represent the end of this quest. Below are some aspects of this work that could be explored for further improvement.

6.3.1 EMI Emissions

CDAs inherently produce EMI, which cannot be entirely eliminated. However, additional techniques can be explored to further increase the LC cutoff frequency, and thus lower system cost and size. Techniques such as carrier spread-spectrum [1], [2], along with active ripple reduction [3] can be combined with the use of higher switching frequencies to further reduce off-chip LC filter requirements. The trade-off, in this case, is with power consumption and efficiency, which would need to be explored.

6.3.2 Load Current Sensing and Current Feedback

Although load current sensing is generally implemented in CDAs to protect speakers or the output stage devices from over-current conditions, in this work (Chapters 4 and 5), it is employed to establish a secondary current feedback path. This is done indirectly by adding low-side sense resistors to a H-bridge, which only works well with push-pull modulation. Furthermore, the linearity of the sensing is reduced by the mismatch of the sensing resistors and their temperature dependency. Although an additional filter was used to reduce these non-idealities within the audio band, it also slightly decreased the effectiveness of the LC resonance damping.

In this regard, shifting to a more linear current sensing and readout network allows for better LC resonance damping. This can be achieved by using sense resistors positioned at the HV switching output to perform true load current sensing. This approach would also enable device and speaker over-current protection. However, the readout network now would need to handle large, high frequency and HV CM switching. Dynamic temperature sensing and compensation would also be required to suppress self-heating induced non-idealities in current sensing.

6.3.3 HV Choppers

In this work (Chapters 4 and 5), HV choppers are used to dynamically match the input and feedback resistors for better linearity and PSRR. However, the HV devices used to make the choppers occupy significant area. Since resistor mismatch is mainly static, some form of offline calibration to improve the matching could be a cheaper alternative. Assuming the additional circuits would be LV analog or digital blocks, the area and power overhead required would be minimal compared to that of four HV switches. However, the degree of matching that can be availed with static calibration techniques would need to be explored.

6.4 References

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Summary

This thesis describes the development of high-performance Class-D audio amplifiers, outlining their significance in modern audio systems. The primary aim is to reduce the system cost and size associated around Class-D amplifiers by minimizing the use of off-chip components, while ensuring high performance and audio fidelity.

Chapter 1 introduces audio amplifiers as integrated circuits, highlighting their role in amplifying electrical signals to drive loudspeakers in various applications. It outlines the key factors influencing amplifier design, including system cost and size, output power, efficiency, electromagnetic interference (EMI), and audio fidelity. The chapter briefly discusses two major classes of amplifiers- Class-AB and Class-D amplifiers (CDAs), particularly emphasizing the latter for high efficiency benefits on account of the switching output stage. Additionally, it introduces the two types of speakers that the amplifiers in this work are optimized to drive, the conventional electrodynamic speaker and the increasingly popular piezoelectric speaker. The discussion includes the advantages and disadvantages of each speaker type and how their electrical impedances impact amplifier design.

Chapter 2 delves into the architectural and circuit techniques used in modern CDAs, comparing different output stage topologies and modulation schemes, and their impact on high-frequency PWM energy and ripple current — key measures of the amplifier's EMI performance. It introduces conventional AD / BD PWM modulation schemes, highlighting their high frequency PWM characteristics from DM and CM perspectives, before exploring more complicated multi-level and multi-phase architectures that aim to reduce the ripple content and EMI. The trade-offs between these modulation schemes in terms of EMI performance and component requirements are examined. It discusses the benefits of increasing the PWM switching frequency above the AM band (1.7MHz), which then allows for smaller and cheaper LC filters. Pulse-density modulation (PDM) using a 1-bit delta-sigma modulator ($\Delta\Sigma$M) is covered, emphasizing its benefits in terms of linearity and challenges related to wideband quantization noise and EMI. Lastly, the chapter also addresses the adaptability of CDAs for driving various speaker loads, particularly newer piezoelectric speakers, and discusses innovative techniques for damping LC resonance without external resistors, significantly reducing power consumption and system cost.

Chapter 3 outlines the development of a 28 W CDA for automotive applications, employing a hybrid multibit $\Delta\Sigma$M-PWM scheme to achieve high linearity and low EMI in the AM band. The design features a fully-differential 3rd order loop filter, a multilevel non-uniform quantizer, and an H-bridge output stage that operates at a switching frequency above the AM

band. This hybrid modulation technique addresses the limitations of 1-bit delta-sigma modulation, and significantly reducing out-of-band emissions while maintaining high linearity across a broad output power range thanks to the high-gain loop filter. The digital and analog circuits in this design, including the loop filter integrators and quantizer, are designed with low-voltage devices to ensure area and power efficiency. In contrast, the high-power output stage and driving circuits are built with more robust high-voltage devices. This prototype amplifier meets the stringent CISPR-25 EMI standards within the AM band using a relaxed LC filter, while also achieving high linearity, dynamic range, and supply rejection.

Chapter 4 introduces a CDA that incorporates a dual voltage/current feedback (VFB/ CFB) topology, specifically designed to drive capacitive piezoelectric speaker loads without the need for external damping resistors. This dual-loop structure effectively mimics a series resistor in an LCR network, allowing for resistor-less LC resonance damping, thereby reducing cost, size, and power consumption. Load current sensing, used in the CFB path, is implemented using purely low-side on-chip sense resistors, thereby avoiding high-frequency switching issues and simplifying the readout network. This low-side sensing is feasible due to the push-pull modulation scheme, which is advantageous for a low-power design. Techniques such as CFB filtering and chopping are employed to reduce non-idealities like noise and non-linearity in the feedback paths. The prototype, fabricated in a 180 nm BCD process, can drive a 4 μF load with a peak current of 4.4 A and achieves an idle power consumption of 122 mW. Measurement results confirm the system's efficacy in damping LC resonance and maintaining high performance, with significant power savings compared to traditional designs using external resistors.

Chapter 5 builds upon the dual feedback architecture introduced in Chapter 4 by incorporating a quadrature chopping scheme to further enhance the linearity and noise performance of Class-D amplifiers. This technique addresses timing skew issues between low-voltage input choppers and high-voltage output choppers, which can degrade signal linearity and increase noise. The quadrature chopping scheme dynamically matches the timing of the choppers, resulting in significant improvements in large-signal total harmonic distortion (THD) and a reduction in noise foldback into the audio band. The chapter presents measurement results that demonstrate the extension in the linear output of the amplifier to close to 95% the full-scale.

Chapter 6 concludes the thesis by summarizing the key findings and contributions of the research. It highlights the original contributions, including the hybrid PWM-DSM modulation scheme, the dual feedback topology for resistor-less damping of capacitive piezoelectric speaker loads, and the quadrature chopping scheme for further improved linearity and noise performance. The chapter also discusses potential future research directions, such as further optimization of EMI performance through advanced modulation techniques, improved current sensing methods, and enhanced feedback accuracy.

Samenvatting

Deze scriptie beschrijft de ontwikkeling van hoogwaardige klasse-D audioversterkers en belicht hun belang in moderne audiosystemen. Het primaire doel is om de systeemkosten en -grootte gerelateerd aan klasse-D versterkers te verminderen door het gebruik van off-chip componenten te minimaliseren, terwijl hoge prestaties en audiokwaliteit worden gewaarborgd. Hoofdstuk 1 introduceert audioversterkers als geïntegreerde schakelingen en benadrukt hun rol bij het versterken van elektrische signalen om luidsprekers in verschillende toepassingen aan te sturen. Het beschrijft de belangrijkste factoren die de versterkerontwerpen beïnvloeden, waaronder systeemkosten en -grootte, uitgangsvermogen, efficiëntie, elektromagnetische interferentie (EMI) en audiokwaliteit. Het hoofdstuk bespreekt kort twee belangrijke klassen van versterkers: klasse-AB en klasse-D versterkers (CDAs), met bijzondere nadruk op de laatste vanwege de hoge efficiëntievoordelen dankzij het schakelende uitgangsstadium. Daarnaast introduceert het de twee soorten luidsprekers waarvoor de versterkers in dit werk zijn geoptimaliseerd: de conventionele elektrodynamische luidspreker en de steeds populairder wordende piëzo-elektrische luidspreker. De discussie omvat de voor- en nadelen van elk luidsprekertype en hoe hun elektrische impedanties het ontwerp van de versterker beïnvloeden.

Hoofdstuk 2 gaat in op de architectuur en circuit-technieken die worden gebruikt in moderne CDAs, waarbij verschillende topologieën van het uitgangsstadium en modulatieschema's worden vergeleken en hun impact op hoogfrequente PWM-energie en rimpelstroom — belangrijke maatstaven voor de EMI-prestaties van de versterker — worden besproken. Het introduceert conventionele AD / BD PWM-modulatieschema's en belicht hun hoogfrequente PWM-karakteristieken vanuit DM- en CM-perspectieven, voordat het complexere meertraps- en meerfasige architecturen verkent die gericht zijn op het verminderen van de rimpelinhoud en EMI. De afwegingen tussen deze modulatieschema's op het gebied van EMI-prestaties en componentvereisten worden onderzocht. Het bespreekt de voordelen van het verhogen van de PWM-schakelfrequentie boven de AM-band (~1,7 MHz), wat vervolgens kleinere en goedkopere LC-filters mogelijk maakt. Pulstijddichtheidsmodulatie (PDM) met een 1-bit delta-sigma modulator ($\Delta\Sigma$M) wordt behandeld, waarbij de voordelen op het gebied van lineariteit worden benadrukt en uitdagingen met betrekking tot breedband kwantisatieruis en EMI worden besproken. Ten slotte behandelt het hoofdstuk ook de aanpasbaarheid van CDAs voor het aandrijven van verschillende luidsprekerbelastingen, met name de nieuwere piëzo-elektrische luidsprekers, en bespreekt innovatieve technieken voor het dempen van LC-resonantie zonder externe weerstanden, waardoor het energieverbruik en de systeemkosten aanzienlijk worden verminderd.

Hoofdstuk 3 beschrijft de ontwikkeling van een 28 W CDA voor automotive toepassingen, waarbij een hybride multi-bit ΔΣM-PWM schema wordt toegepast om hoge lineariteit en lage EMI in de AM-band te bereiken. Het ontwerp bevat een volledig differentiële derde-orde lusfilter, een meertraps niet-uniforme quantizer, en een H-brug uitgangsstadium dat werkt op een schakelfrequentie boven de AM-band. Deze hybride modulatie-techniek pakt de beperkingen van 1-bit delta-sigma modulatie aan en vermindert aanzienlijk de emissies buiten de band terwijl een hoge lineariteit over een breed uitgangsvermogen bereik wordt behouden dankzij het hoogvermogende lusfilter. De digitale en analoge circuits in dit ontwerp, inclusief de lusfilter-integrators en quantizer, zijn ontworpen met laagspanningscomponenten om ruimte te besparen en energie-efficiëntie te waarborgen. Daarentegen zijn het hoogvermogende uitgangsstadium en de aandrijfcircuits gebouwd met robuustere hoogspanningscomponenten. Deze prototype versterker voldoet aan de strenge CISPR-25 EMI-normen binnen de AM-band met behulp van een simpel LC-filter, terwijl ook hoge lineariteit, dynamisch bereik en voedingsonderdrukking worden bereikt.

Hoofdstuk 4 introduceert een CDA die een dubbele spanning/stroom terugkoppelings (VFB/CFB) topologie omvat, specifiek ontworpen om capacitatieve piëzo-elektrische luidsprekerbelastingen aan te sturen zonder gebruik te maken van externe dempingsweerstanden. Deze dubbele lus structuur bootst effectief een serieweerstand in een LCR-netwerk na, waardoor demping van LC-resonantie zonder weerstanden mogelijk is, en daarmee de kosten, grootte en energieverbruik worden verminderd. Een stroommeting van de belasting, gebruikt in het CFB-pad, wordt geïmplementeerd met behulp van laagzijdige weerstanden op de chip, waardoor problemen met hoogfrequente schakeling worden vermeden en het uitleesnetwerk wordt vereenvoudigd. Deze laagzijdige meting is haalbaar dankzij het push-pull modulatieschema, wat voordelig is voor een energiezuinig ontwerp. Technieken zoals CFB-filtering en hakken worden gebruikt om niet-idealiteiten zoals ruis en niet-lineariteit in de terugkoppelingspaden te verminderen. Het prototype, gefabriceerd in een 180nm BCD-proces, kan een 4 μF-belasting aandrijven met een piekstroom van 4,4 A en bereikt een ruststroomverbruik van 122 mW. Meetresultaten bevestigen de effectiviteit van het systeem bij het dempen van LC-resonantie en het handhaven van hoge prestaties, met aanzienlijke energiebesparingen in vergelijking met traditionele ontwerpen die externe weerstanden gebruiken.

Hoofdstuk 5 bouwt voort op de dubbele terugkoppelingsarchitectuur geïntroduceerd in Hoofdstuk 4 door een quadratuur hak-schema op te nemen om de lineariteit en ruisprestaties van klasse-D versterkers verder te verbeteren. Deze techniek pakt verschillen in timing tussen laagspanningsingangshakken en hoogspanningsuitgangshakken aan, die de signaallineariteit kunnen degraderen en ruis kunnen verhogen. Het quadratuur hak-schema stemt dynamisch de timing van de hakken af, wat resulteert in aanzienlijke verbeteringen in groot-signaal totale harmonische vervorming (THD) en een vermindering van ruisterugplooiing in de audioband. Het hoofdstuk presenteert meetresultaten die de uitbreiding van de lineaire uitgang van de versterker tot bijna 95% van de volledige schaal aantonen.

Hoofdstuk 6 sluit de scriptie af door de belangrijkste bevindingen en bijdragen van het onderzoek samen te vatten. Het belicht de originele bijdragen, waaronder het hybride

PWM-DSM modulatieschema, de dubbele terugkoppelingstopologie voor weerstandloze demping van capacitieve piëzo-elektrische luidsprekerbelastingen, en het quadratuur hakschema voor verder verbeterde lineariteit en ruisprestaties. Het hoofdstuk bespreekt ook potentiële toekomstige onderzoeksrichtingen, zoals verdere optimalisatie van EMI-prestaties door geavanceerde modulatie-technieken, verbeterde stroommeettechnieken en verbeterde terugkoppelingsnauwkeurigheid.

List of Publications

Journal Papers

- **S. Karmakar**, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A −91 dB THD+N, Class - D Piezoelectric Speaker Driver Using Dual Voltage/Current Feedback for Resistor-Less LC Resonance Damping," in *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3726-3735, Dec. 2022.
- T. Rooijers, **S. Karmakar**, Y. Kusuda, J. H. Huijsing, and K. A. A. Makinwa, "A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers," in *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3583-3592, Dec. 2021.
- E. Eland, **S. Karmakar**, B. Gönen, R. van Veldhoven, and K. A. A. Makinwa, "A 440-µW, 109.8-dB DR, 106.5-dB SNDR Discrete-Time Zoom ADC With a 20-kHz BW," in *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1207-1215, April 2021.
- H. Zhang, **S. Karmakar**, L. Breems, Q. Sandifort, M. Berkhout, and K. A. A. Makinwa, Q. Fan, "A High-Linearity and Low-EMI Multilevel Class-D Amplifier," in *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1176-1185, April 2021.
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