MODELLING AND EVALUATION OF CONTACT RESISTANCE IN HIGH-EFFICIENCY C-SI SOLAR CELLS FEATURING CARRIER-SELECTIVE PASSIVATING CONTACTS

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Modelling and Evaluation of Contact Resistance in High-Efficiency c-Si Solar Cells Featuring Carrier-Selective Passivating Contacts

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Abstract

In this thesis, contact resistivity for carrier-selective contacts (CSCs) is evaluated by using finite element simulations TCAD Sentaurus. First, the process of transmission line measurement (TLM) is modelled and validated based on current-voltage (I-V) data comparison between reference experiment and simulation results on polycrystalline silicon (poly-Si) based CSCs. Simulation and experimental data are in a good agreement, thus confirming that the modeling method accurately describes the main physical mechanism. Therefore, the simulation approach is used to evaluate the resistivity of complete contact stack for poly-Si and silicon heterojunction (SHJ) based CSCs. Simulation results reveals that the contact resistivity exhibits a clear dependence on tunneling mechanisms in terms of potential barrier size and band alignment. For poly-Si based CSCs, SiO_2 thickness (potential barrier size) is the prevalent parameter impacting on the contact resistivity. Additionally, proper doping in poly-Si and buried region in c-Si can improve the band alignment, thus the contact resistivity becomes more resilient to the effect of the tunneling barrier. For SHJ based CSCs, low contact resistivity values are achieved with high carrier concentration in TCO and low activation energy in doped thin film silicon layer. In general, low activation energy reduces the potential barrier for carrier transport while high TCO carrier concentration allows a better band alignment. In particular, for p-type contact, high carrier concentration in TCO is crucial to ensure an efficient band alignment for band-to-band tunneling at TCO/doped-layer interface. Additionally, the contact resistance depends also on the bandgap and the thickness of the passivating intrinsic amorphous silicon (i-a-Si:H) as they impact on band alignment and also energy barrier size. Indeed, lower values of contact resistance are calculated for thinner i-a-Si:H and narrow bandgap because the reduction of the potential barrier opposing to hole collection. Finally, the presented simulation platform has the potential and flexibility of predicting the contact resistance for any type of CSC stack in terms of materials and number of layers.

Acknowledgement

The basis for this research originally stemmed from my curiosity for simulation methods of semiconductor device. As the computational tool moves further into the numerical computation, the analysis on complicated carrier behavior and transport mechanism becomes available. There will be a greater need to optimize the efficiency of solar cell with simulation approach. How will I access this method? It is my passion not only to observe, but also to research the feasible ideas.

In truth, I could not make the current achievement without a strong support group. First of all, thanks to my parents, who supported me with love and understanding. Secondly, thanks to my daily supervisor Dr. Paul Procel, who gives me the patient instruction to the whole project. We discussed all the details for my research. He taught a lot about TCAD Sentaurus and helped me solve numerous problems. The accomplishment of this thesis cannot leave his contribution. Thirdly, thanks to my full responsible supervisor Dr. Olindo Isabella, who gives me the opportunity to take part in this project. He guides the progress of project to make sure it can be finished on time. Then, thanks to Aurora, who is another member of the project. She always works with limitless passion and helps me a lot on understanding and programing trap-assisted tunneling (TAT). Moreover, thanks to Gianluca, Luana, Guangtao, Paula, Yifeng, Stefaan. They are always interested in my results and give me a lot of precious advice about presentation. I would appreciate all c-Si cluster team member for emphasis on my results. Finally, thanks to my academic counsellor, Leonie Boortman. She is a kind and warm heart lady and helps me a lot during the whole study in TU Delft.

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List of Symbols

Latin Symbols

d_{poly}	Thickness of poly-Si layer
d_{Ox}	Thickness of SiO_2 layer
d_{bulk}	Thickness of c-Si bulk
d_{doped}	Thickness of thin film silicon layer
$d_{a\text{-}Si(i)}$	Thickness of i-a-Si:H layer
d_{TCO}	Thickness of TCO layer
E_{vac}	Vacuum energy level
E_G E_g	Bandgap
E_{trap}	Difference between the defect level and intrinsic level
E_a	Activation energy
G	Generation rate
g'	Generation rate for excess carriers
l_n, l_p	Widths of depletion
L_C	Contact length
L_d	Contact distance
L_t	Transfer length
N_V	Effective density of state functions in the valence bands
N_d, N_a	Doping concentration in n-type and p-type region
N_{bulk}	Doping concentration in c-Si bulk
N_{poly}	Doping concentration in poly-Si layer
N_{peak}	Peak doping concentration in buried region inside c-Si bulk
N_{doped}	Doping concentration in thin film silicon layer
N_{TCO}	TCO carrier concentration
$n_{i,eff}$	Effective intrinsic density
p, n	Hole and electron concentrations
R	Recombination rate
R_t	Total resistance Rt between two contacts
R_s	Sheet resistance
V_{oc}	Open circuit voltage
W	Wafer width

Greek Symbols

τ_{n0}, τ_{p0}	Excess minority carrier electron and hole lifetime
χ_e	Electron affinity
ϕs	Work function
ϵ_n, ϵ_p	Dielectric constants of n-type and P-type materials

List of Acronyms

a-Si	Amorphous Silicon
c-Si	Crystalline Silicon
CSCs	Carrier Selective Contacts
FF	Fill Factor
IBC	Interdigitated Back Contact
LPCVD	Low Pressure Chemical Vapor Deposition
Nano-Si	Nano-crystalline silicon
Poly-Si	Poly-crystalline silicon
SHJ	Silicon Heterojunction
TAT	Trap Assisted Tunneling
TLM	Transmission Line Measurement
TCO	Transparent Conductive Oxide
LPCVD	Low Pressure Chemical Vapor Deposition

1 Introduction

1.1 Energy Review

According to BP Statistical Review of World Energy published in June 2018[1], global primary energy consumption increased strongly by 2.2% in 2017. The natural gas and renewable energy contribute most share of the increment, meanwhile the proportion of coal in total energy consumption keeps decreasing.

As shown in Figure 1, global primary energy consumption increased by 2.2% in 2017, which is the largest growth since 2013. Renewable power increased by 17% and contributed the second highest increment of energy consumption. The increment of renewable energy consumption reached 69 million tonnes oil equivalent (Mtoe) and built new record in last 10 years. The solar power accounted for 21% of total renewable power and more than 33% of renewables' growth.

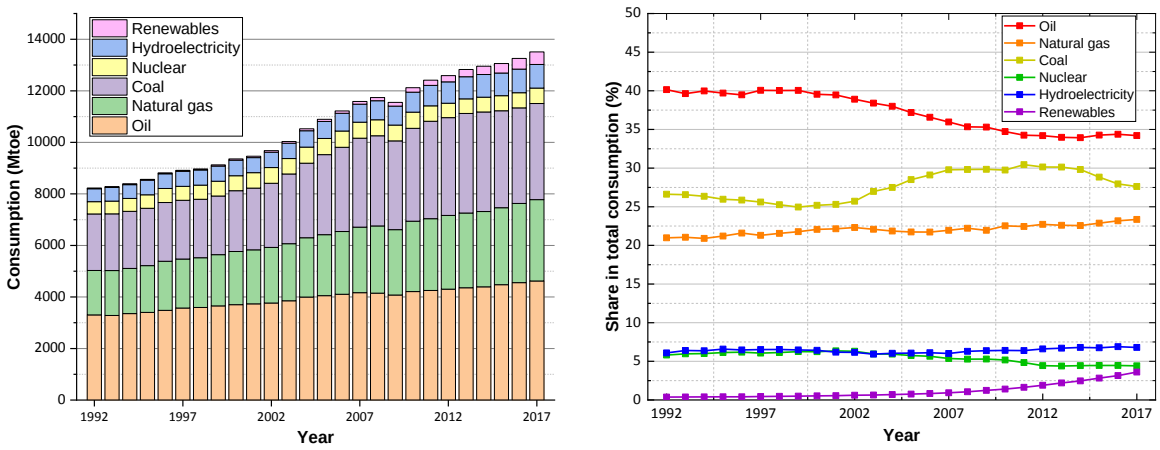

Figure 1 A schematic of the world energy consumption and the share of each energy type, in which the energy type of coal, renewables, hydroelectricity, nuclear energy, natural gas and oil from 1992 to 2017 are indicated[1]

The global electricity generation and the share of different energy type from 1992 to 2017 are shown in Figure 2. It can be seen that oil is still the dominant fuel in the world. Meanwhile the carbon emission keep ascending trends except year 2009, as shown in Figure 3. In order to avoid further impact on environment and eco-economy. Renewable energy resources become preferable selection for sustainable development nowadays.

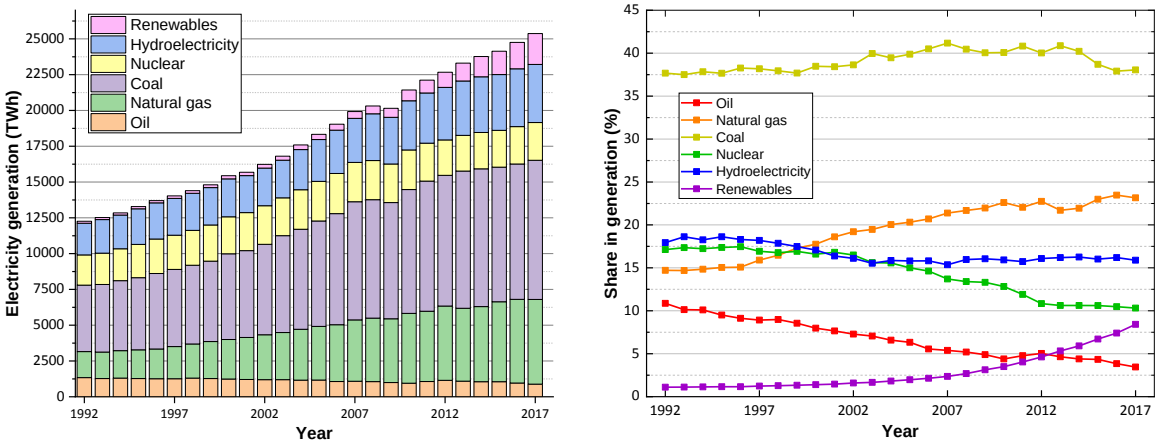

Figure 2 A schematic of the world electricity generation and the share of each energy type, in which the energy type of coal, renewables, hydroelectricity, nuclear energy, natural gas and oil from 1992 to 2017 are indicated[1]

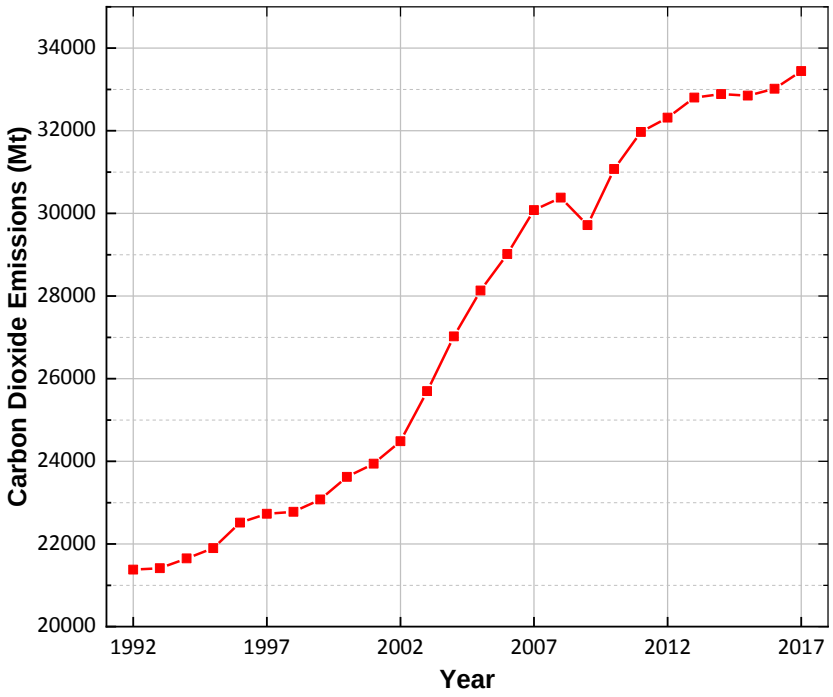

Figure 3 A schematic of the world carbon dioxide emission from 1992 to 2017[1]

From 2000 until now, solar energy has become one of important composition in renewable resources as shown in Figure 4. Global power generation increased by 2.8% in 2017, in which solar power contributed 114 TWh, accounting for 35%.[1] Solar capacity increased by nearly 100 GW last year, in which more than half of the total was built in China. Global solar generation increased by more than one third in 2017. Although the policy support continues reducing the emphasis on solar power, the relevant industry is strongly being stimulated by unpredictable low solar costs. For most projects the auction bids are less than 5 cents/KWh, which is remarkably

low in comparison with the costs a few years ago.[1]

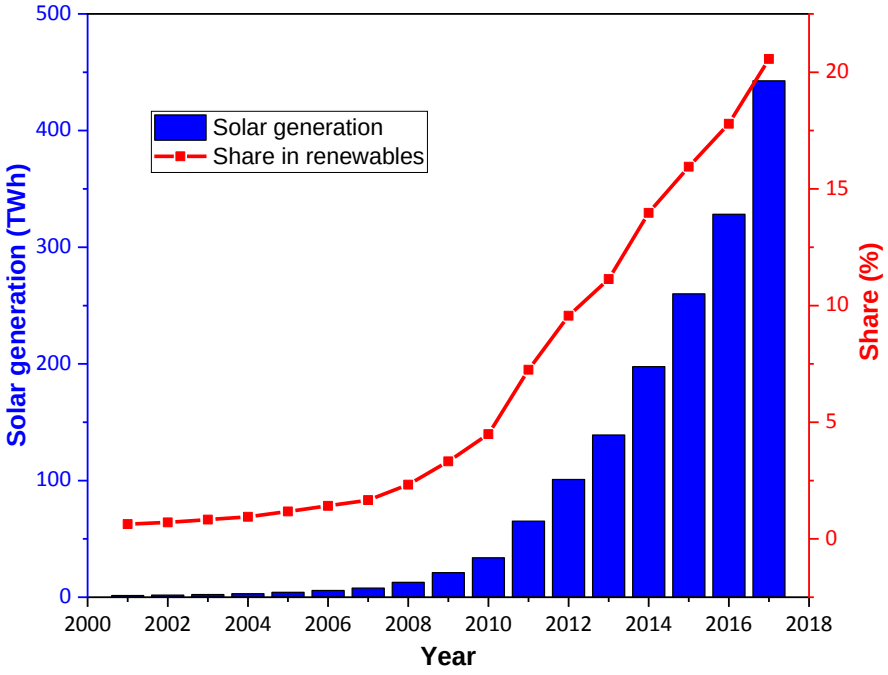

Figure 4 A schematic of the world solar generation and the share in renewable generation from 1992 to 2017[1]

1.2 Solar cell review

In 1839, Alexandre-Edmond Becquerel created the first photovoltaic cell in the world. In his experiment, Becquerel connected silver chloride and platinum electrodes in acidic solution to form a simple solar cell. Voltage and current were generated when the solar cell was illuminated. This phenomenon is called photovoltaic effect, also known as "Becquerel effect".[2] In 1887, Heinrich Hertz discovered photoelectric effect when investigating electromagnetic waves.[3] He noticed that electrodes illuminated with ultraviolet light create electric sparks more easily. In 1954, the first practical silicon solar cell was shown at the National Academy of Science Meeting.[4] These cells are invented by Bell Labs and have around 6% efficiency. The New York Times forecasts that solar cells will eventually lead to a source of "limitless energy of the sun".[5] Until 2010, the highest solar cell efficiency was obtained by Spire Semiconductor, who cooperated with the US National Renewable Energy Laboratory (NREL) on an 18-month incubator project and fabricated a “triple-junction” solar cell with 42.3% conversion efficiency.[6]

Nowadays, crystalline silicon (c-Si) is the dominant semiconductor materials used in fabrication of solar cells.[7] The mature microelectronics industry supports sufficient technologies and equipment to c-Si industry researchers. Moreover, abundant silicon resources are stored in mineral reserves of earth. Nontoxic silicon resources are readily mined and processed as the major production materials for solar cells. Due to

above factors, the c-Si solar cell technology is widely used in large-scale PV market.

The energy conversion efficiency of solar cell is limited by many factors, such as non-absorption of photons caused by spectral mismatch, optical losses caused by front metal shading, recombination losses caused by trap and defects.[8] In order to increase the conversion efficiency of solar cell, new designs of solar cell structures are studied to improve the performance. To reduce the recombination losses, new concepts as point-contacts (PC) and carrier-selective-contacts (CSC) demonstrated outstanding performances in solar cells.[9] In particular, following the PC approach, in 2016, Franklin E, Fong K et al. designed and fabricated a interdigitated back contact (IBC) solar cell with 24.4% efficiency.[10] On the other hand, following CSC approach, Kaneka Corporation fabricated a first practical size (180 cm^2) heterojunction back-contact crystalline silicon solar cell which achieved the highest conversion efficiency of 26.33% in the world.[11] Beside, interdigitated back contact (IBC) concept becomes of particular interest because it take advantage of the complete incident light avoiding front contact shading, since both contacts are in the rear side of the device as shown in Figure 5.

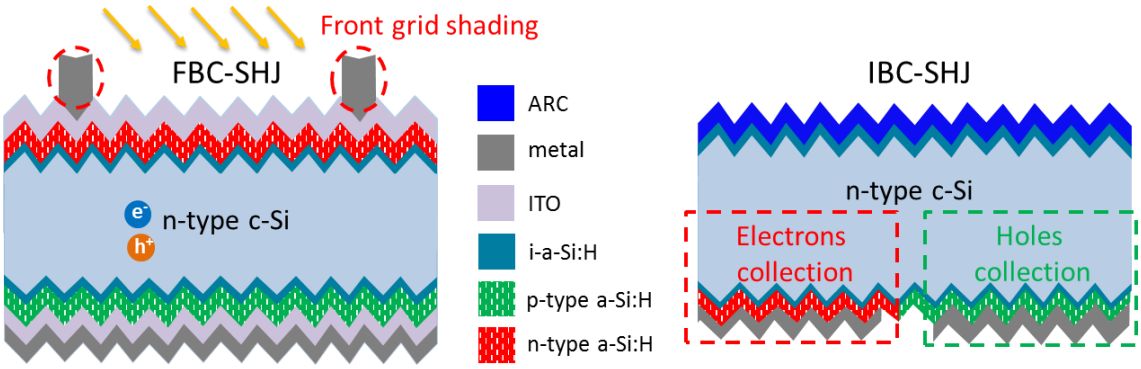

Figure 5 A schematic of the silicon heterojunction (SHJ) solar cell and interdigitated back contact (IBC) solar cell[12]

As shown in Figure 5, the optical performance of IBC c-Si solar cell is excellent due to the absence of front metal shading losses and the simplification of interconnection process at module level. However, in order to obtain the high efficiency of IBC solar cell, a relatively long minority-carrier diffusion length, a good passivation quality at interfaces, and a low front reflectance during fabrication process.[13–15] Technologies of textured surface structure, antireflective coatings (ARCs) depositions, front surface field (FSF) and back surface field (BSF) formation have been developed to reduce the optical and recombination losses in IBC c-Si solar cell. Some researches show that pyramid-textured or nano-textured surface structure can effectively reduce optical losses of front surface.[16] Meanwhile other researches shows that smooth-textured surface structure can effectively lower the surface recombination losses.[17-18] The balance between the texturization types need be weighed to obtain optimal performance. Anti-reflective transparent conductive oxide (TCO) is added during fabrication to reduce the front reflectance of solar cell. In addition, FSF and BSF layers in IBC c-Si solar cell can reduce the recombination losses, lateral resistance

losses, and improve UV light stability.[19-20]

Rolf Brendel and Robby Peibst studied the contact selectivity and efficiency of so-called “passivating selective contacts”.[21] The contact resistivity and recombination parameter are taken into consideration as important factor to determine the efficiency, as shown in Figure 6. It can be seen that recombination parameter aside, the contacts with high efficiency can only been achieved when resistivity is under 1 Ωcm^2. Among this region, polycrystalline silicon based electron and hole selective contacts can achieve very low resistivity around 10^{-3} Ωcm^2. This kind of contact will be discussed in following chapters.

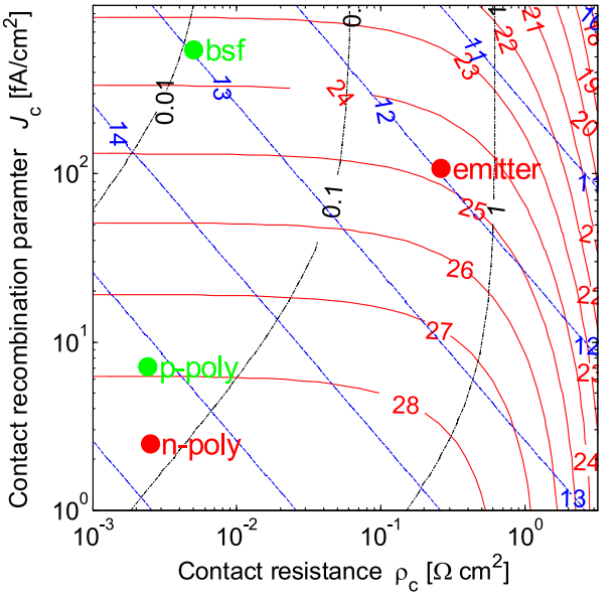

Figure 6 Contact resistivity ρ_c and recombination parameter J_c of a selective contact in a cell with the current–voltage curve determine the cell efficiency in % (solid red line). The selectivity level is indicated with dashed blue line. The red dots represent the electron selective contacts and the green dots denote the hole selective contacts.[21]

1.3 Motivation and outline

In order to obtain the high efficiency of passivating contacts solar cell, a relatively long minority-carrier diffusion length, a good passivation quality at interfaces, and a low front reflectance are required during fabrication process. In addition, the resistivity of contact stack is also an important parameter that affects the fill factor (FF) and external electrical performance of solar cell.

This thesis present a simulation platform allowing to model transfer length method for measuring contact resistance based on TCAD Sentaurus, finite element simulator.[22] Then, the simulation template is used to investigate the dominant physical mechanism affecting contact resistance. In such a work, state-of-the-art models and parameters are used together with ad-hoc drift diffusion model including transport through interfaces as tunneling and thermionic emission. Moreover, exploiting the advantages of this simulation model, different strategies for CSC as

poly-silicon based and silicon hetero-junction are study.

In this chapter, the review of energy and solar cell technology is presented. In **Chapter 2**, the background information of semiconductor physics and transmission line measurement (TLM) is presented. In **Chapter 3**, the numerical tools and simulation models are presented. In **Chapter 4** and **Chapter 5**, the simulation results and analysis of polycrystalline silicon (poly-Si) based passivated contact stack model and silicon heterojunction (SHJ) based passivated contact stack model are presented. In **Chapter 6**, the conclusion of whole project and further recommendation and objective are presented.

2 Background Information

Solar cell is a semiconductor device that transform Sun light into electricity using photovoltaic effect. As shown in Figure 7, the working principle of solar cell includes light absorption, carriers' generation, carriers' separation and collection by means of p-n junction.[23] The p-n junction can be classified as homo-junction or hetero-junction.[8] When a solar cell absorbs irradiation from sunlight, if the photon of which has higher energy than the bandgap of the material, the electron will be activated from valance band to conduction band and form an electron-hole pair. The charge carriers not recombined will be collected by contacts and generate electricity in external circuits. In industrial production, crystalline silicon (c-Si) is the dominant semiconductor materials used in fabrication of solar cells.[24]

In this thesis, TLM experiment process is modelled using TCAD Sentaurus software. Accordingly, a brief description of concepts and models using in this thesis will be introduced in following sections.

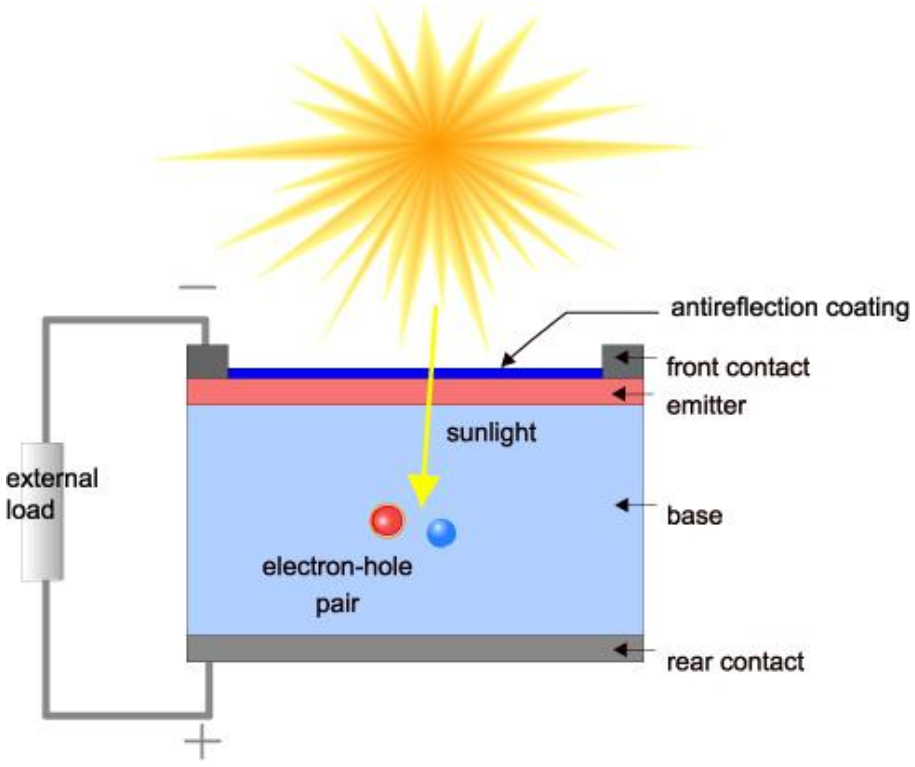

Figure 7 Solar cell structure and working mechanisms[23]

2.1 Semiconductor physics

Understanding the electronic and physics of semiconductors allow an efficient use of such materials for different applications. In crystalline materials, electrons feature

different energies known as electronic band structure. As electrons occupy only discrete energy levels, there is a forbidden energy or band gap energy for electrons. In case of insulators, the forbidden energy is large and electrons from every energy are fixed at surrounding orbitals. In case of metals, such a band gap is very small and electrons move freely within orbitals. In case of semi-conductors, electron are able to be excited by engineering material properties.[25]

Free (unoccupied) states allow the movement of electrons within material. If there is not free states, there is no charge movement. Depending of population of occupied states, electrons can move more easily or not in terms of mobility. If the electron is in the conduction band , it faces more free states and can move easily through them. But, in the valence band, most of the states are occupied, then empty states for electrons denotes for positive charge carriers. Holes move easily on the valence band. Holes and electrons can be introduced in the semiconductor in terms of dopants, thus manipulating Fermi energy level of materials. At equilibrium, if the material feature more holes than electrons, the material is called p-type. On the contrary if the material exhibits more electrons is n-type.[25]

When n-type and p-type semiconductor materials are combined together, the p-n junction is formed. The large carrier concentration gradient. will cause diffusion current, leading electrons from n-type material across the metallurgical junction into p-type material and holes from p-type material transport into n-type material. The diffusion process makes the region close to metallurgical junction depleted of mobile carriers. This region is so called depletion region or space charge region. As shown in Figure 8, an internal electrical field is formed in space charge region, which forces the charge carriers to move opposite the concentration gradient. The drift-diffusion model describes the physics behind. It will be introduced in next section.[8]

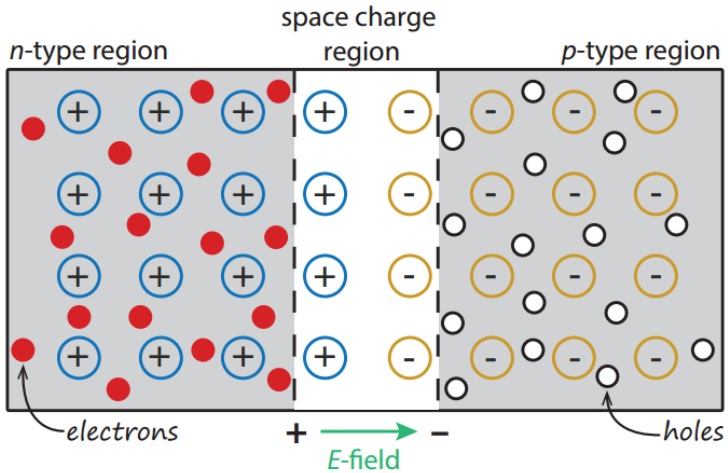

Figure 8 A schematic of p-n junction and space charge region[8]

2.1.1 Drift-diffusion model

The drift-diffusion model is commonly used to describe the feature of semiconductor

devices. It contains a set of equations to explain the fundamental relation of the essential variables of semiconductor devices.

Poisson equation[26] describes the relation among volume charge density ρ, electric potential ϕ, and electric field E. The expression in first dimension is shown by following:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} = -\frac{dE(x)}{dx} \tag{2-1}$$

The first and third term of Eq (2-1) describe the electric field within depletion region by given electric potential. The ϵ_s is the permittivity of the semiconductor. The second and third term relate the excess electron and hole concentration to the internal electric field.

The separate expressions of drift and diffusion current[26] for one-dimension case are shown by following:

$$J_n(x) = en\mu_n E(x) + eD_n \frac{dn}{dx} \tag{2-2}$$

$$J_p(x) = ep\mu_p E(x) - eD_p \frac{dp}{dx} \tag{2-3}$$

Eq (2-2) and Eq (2-3) describes the electron drift and diffusion current and hole drift and diffusion current. Where e is the magnitude of electron charge, D_n and D_p are the diffusion coefficients for electron and hole respectively, μ_n and μ_p are the mobility of electron and hole respectively. The external illumination and applied electric field are considered under steady-state conditions.

Combining Eq (2-1), Eq (2-2) and Eq (2-3), the continuity equations for electron and hole[26] can be written by following:

$$e\frac{dn}{dt} = \nabla J_n + e(G - R) \tag{2-4}$$

$$e\frac{dp}{dt} = -\nabla J_p + e(G - R) \tag{2-5}$$

Where G is the generation rate of charge carrier and R is the recombination rate of charge carrier. Eq (2-4) and Eq (2-5) describe the carrier behavior in low-level injection solar cell device and take the generation and recombination into account.

Through assuming an extrinsic doping semiconductor device with low-level injection, the simplified ambipolar transport equations[26] can be obtained by following:

$$D_n \frac{\partial^2(\delta n)}{\partial x^2} + \mu_n E \frac{\partial(\delta n)}{\partial x} + g' - \frac{\delta n}{\tau_{n0}} = \frac{\partial(\delta n)}{\partial t} \tag{2-6}$$

$$D_p \frac{\partial^2(\delta p)}{\partial x^2} - \mu_p E \frac{\partial(\delta p)}{\partial x} + g' - \frac{\delta p}{\tau_{p0}} = \frac{\partial(\delta p)}{\partial t} \qquad (2\text{-}7)$$

Where δn and δp are the excess minority carrier concentration of electron and hole respectively, g' is the generation rate for excess carriers, τ_{n0} and τ_{p0} are the excess minority carrier electron and hole lifetime.

The equation sets (2-1) to (2-7) can only describe the carrier activities in same material, or in homojunction semiconductors with continuous conduction band and valence band. For the more complex semiconductor with heterojunction, the energy bands are discontinuous. Additional physical models are required to describe the carrier activities inside, which will be discussed in next section. The support of computational resources are involved into numerically solving the inner process of semiconductor in complex conditions.

2.1.2 Transport at hetero-interfaces and materials

In the p-n junctions, if the materials of both sides are same, which means they have same bandgap energy and electron affinity, this kind of p-n junction is so-called homojunctions. For some semiconductor device, the junction is between different materials. These junctions are so-called heterojunctions. Heterojunctions are frequently used in solar cell devices. In 2016, Kaneka Corporation fabricated a first practical size (180 cm^2) heterojunction back-contact crystalline silicon solar cell which achieved the highest conversion efficiency of 26.33% in the world.[11]

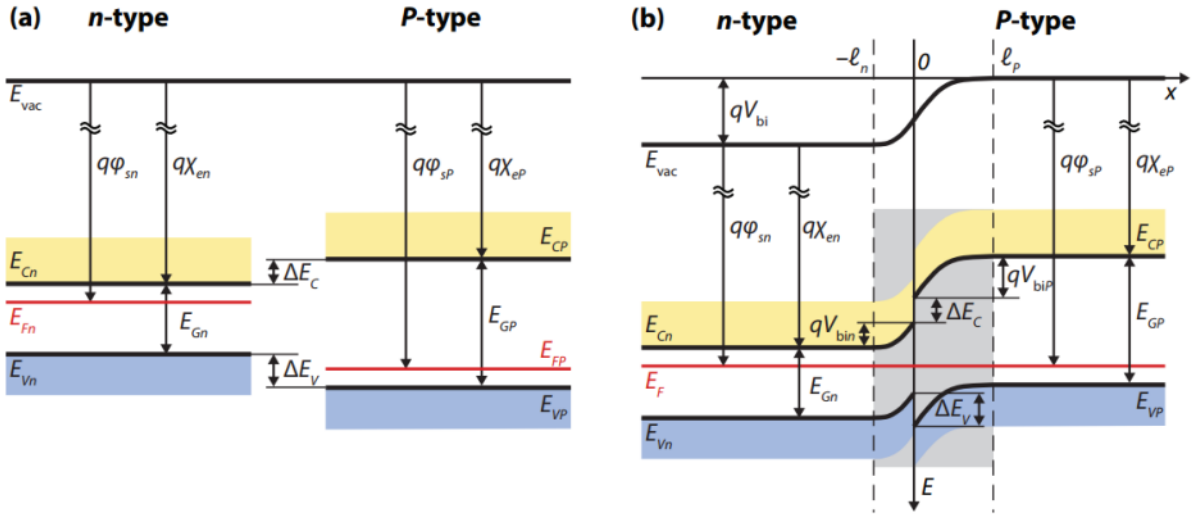

Figure 9 A schematic of energy band diagrams, in which (a) indicates the band diagram of an n-type and a P-type semiconductor with a larger bandgap than the n-type material respectively; (b) indicates the band diagram an n-P heterojunction[8]

The heterojunctions can be classified by four types: n-P junctions, p-N junctions, n-N junctions, and p-P junctions. Materials with lower bandgap energy are indicated by lower-case letter; meanwhile materials with higher bandgap energy are indicated by

upper-case letter.

The band diagrams of the n-type material, P-type material, and the combined n-P heterojunction are shown in Figure 9. As shown in Figure 9 (a), the vacuum energy level E_{vac} is considered as reference. E_{Gn} and E_{GP} indicate the bandgap of n-type material and P-type material respectively. The electron affinities of two materials are also different, indicated by χ_{en} and χ_{eP}, which denotes the potential difference between the conduction band energies of two materials ΔE_C. φ_{sn} and φ_{sP} indicate the work function of two materials, which are the energy difference between vacuum energy level and Fermi levels of two materials. The potential difference between the valence band energies of two materials is denoted as ΔE_V. The following equations[8] can be obtained from Figure 9 (a),

$$\Delta E_C = e(\chi_n - \chi_P) \tag{2-8}$$

$$\Delta E_C + \Delta E_V = E_{GP} - E_{Gn} = \Delta E_G \tag{2-9}$$

where ΔE_G indicates the difference between bandgap energies of two materials.

In Figure 9 (b), the band diagram of n-P heterojunction is shown. Two constraints are used when forming an interface. First, the Fermi level is constant on both sides of the interface under equilibrium condition, as this was the case for homojunctions. Secondly, the vacuum energy should be continuous across the junction. The built-in voltage of the n-P heterojunction can be obtained by the difference of work functions of two materials. [8]

$$V_{bi} = \phi_{sP} - \phi_{sn} \tag{2-10}$$

The expression can be also written as,

$$eV_{bi} = -\Delta E_C + \Delta E_G + k_B T ln\left(\frac{N_{Vn}}{p_{n0}}\right) - k_B T ln\left(\frac{N_{VP}}{p_{P0}}\right) \tag{2-11}$$

Where p_{n0} and p_{P0} indicate the hole concentrations in the n-type and P-type materials respectively; N_{Vn} and N_{VP} indicate the effective density of state functions in the valence bands of the n-type and P-type materials respectively

Same as the homojunctions, the electric field E is largest at the hetero-interface and linearly decreases until the boundary of depletion region. The expression[8] of electric field E can be written as,

$$E_n(x) = \frac{eN_{dn}}{\epsilon_o \epsilon_n}(l_n + x) \quad (-l_n \le x < 0) \tag{2-12}$$

$$E_P(x) = \frac{eN_{aP}}{\epsilon_o \epsilon_P}(l_P - x) \quad (0 < x \le l_P) \tag{2-13}$$

Where N_{dn} and N_{aP} indicate the doping concentration in n-type and P-type region

respectively; ϵ_n and ϵ_P indicate the dielectric constants of n-type and P-type materials respectively. l_n and l_P are the widths of depletion[8], which can be expressed by,

$$l_n = \sqrt{\frac{2\epsilon_o\epsilon_n\epsilon_P N_{aP} V_{bi}}{eN_{dn}(\epsilon_n N_{dn} + \epsilon_P N_{aP})}} \quad (2\text{-}14)$$

$$l_P = \sqrt{\frac{2\epsilon_o\epsilon_n\epsilon_P N_{dn} V_{bi}}{eN_{aP}(\epsilon_n N_{dn} + \epsilon_P N_{aP})}} \quad (2\text{-}15)$$

The total width of depletion region can be expressed by

$$W = l_n + l_P = \sqrt{\frac{2\epsilon_o\epsilon_n\epsilon_P (N_{dn} + N_{aP})^2 V_{bi}}{eN_{dn}N_{aP}(\epsilon_n N_{dn} + \epsilon_P N_{aP})}} \quad (2\text{-}16)$$

As shown in Figure 9, in heterojunction the conduction band and valence band are not continuous. This is due to the different electron affinities and bandgap energies of materials. The discontinuities can result in the barriers for carrier transport. Different transport mechanisms can be used at the hetero-interface, such as diffusion, band-to-band tunneling, trap-assisted tunneling, thermionic emission, and so on.

Based on heterojunction technology, various kinds of contact stack are proposed in order to achieve high efficiency. Carrier selective contact is one of them and will be introduced in following sections.

2.1.3 Recombination mechanisms

Recombination can be classified by bulk recombination and surface recombination. Bulk recombination can happen inside the bulk of semiconductors. For example, impurities can cause trap states within the semiconductor bandgap leading to Shockley-Read-Hall (SRH) recombination. Surface recombination is also important in semiconductors.[27] It can be seen from Figure 10 that there are a lot of dangling bonds on the surface of silicon bulk, which are defects and lead many surface trap states within bandgap. SRH recombination will happen due to these traps.[8]

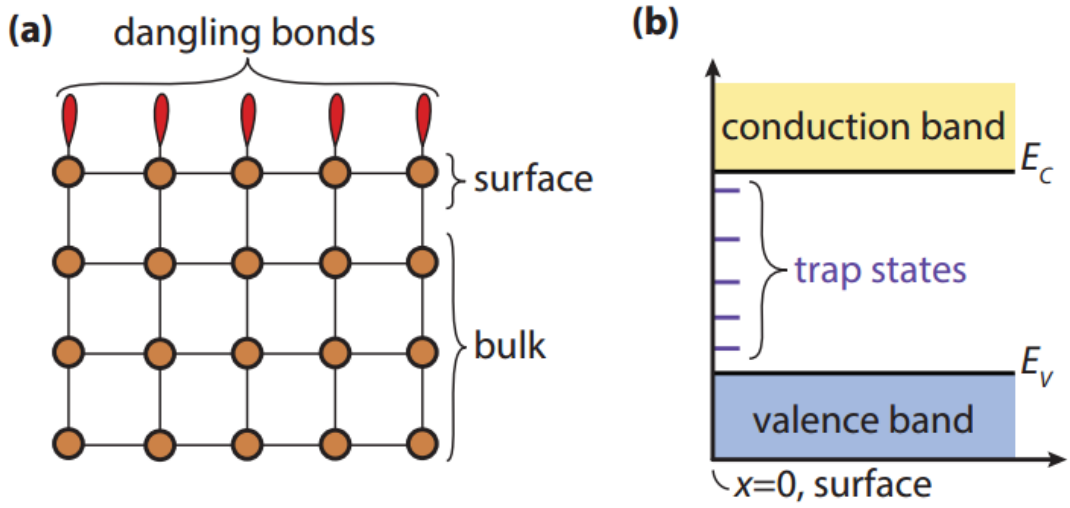

Figure 10 A schematic of (a) dangling bonds (surface defects) on a semiconductor surface and (b) the trap states within the bandgap created by the surface defects[8]

High recombination rate results in low photocurrent and open circuit voltage. In highly-pure silicon solar, the impurities in bulk are very low. The surface recombination will be dominant limits of solar cell efficiency. In order to reach high conversion efficiency, it is important to lower the surface recombination rate. One of the common semiconductor technologies is called passivation. Through depositing a thin layer of a suitable material onto the semiconductor surface, the dangling bonds on the surface can form covalent bonds, so that the surface trap density will be reduced.[28]

Combining heterojunction technology and passivation technology, Carrier-selective contacts present outstanding performance on low recombination and good carrier selectivity.[29]

2.2 Carrier selective contacts

A solar cell, or photovoltaic cell, is an electrical device that converts the energy of light directly into electricity by the photovoltaic effect, which is a physical and chemical phenomenon.[30] The mostly-used form of the solar cell is p-n junction. The absorption of sunlight raises the energy state of electrons and holes in material and generates electron-hole pairs. The generated electrons and holes are influenced by the internal electrical field and collected by contacts. The voltage is built across the contacts.

As discussed in **Chapter 1, Section 1.2**, two crucial factors to determine the efficiency of solar cell are recombination and contact resistivity, as shown in Figure 6. Two ingredients are necessary at the cell level to achieve high efficiency: an excellent interface passivation scheme and efficient carrier-selective contacts.

All solar cells have a high density of defects on its metallic surface that can hardly be

reduced. The high defect density leads high surface recombination and limiting minority-carrier transport through the contact.[29] Passivation is the most common method to solve this problem. In addition, the power generation of solar cell is limited by the contact resistance. When current is extracted from solar cell, the majority-carrier resistance in contact determines the power loss. High fill factor is achieved with uninhibited majority-carrier transport.[29]

Carrier-selective contacts are the technology to achieve low resistivity. The underlying principle is the same as for the more common diffused junctions: blocking one carrier type and conducting the other. The high efficiencies that were achieved with nondiffused passivated selective contacts indicate that they have a better selectivity than diffused junctions.[21] A polysilicon emitter related solar cell achieving both a high V_{oc} = 694 mV and *FF* = 81% was presented in 2014.[31]

Aside from recombination, the way to reduce contact resistivity is the key to improve solar cell efficiency. The interface passivation, doping, band alignment of CSC is studied to investigate the factors that determine the resistivity of contact stack.

In next sections, polycrystalline silicon (poly-Si) based carrier-selective contacts and silicon heterojunction (SHJ) based carrier-selective contacts will be introduced.

2.2.1 Poly-silicon based passivated contacts

In order to obtain high conversion efficiency silicon solar cell, it is crucial to reduce the surface recombination rate at the interface between silicon and metal contacts. Carrier-selective passivating contact is one advanced technology to achieve the goal. The semi-insulating polycrystalline silicon (poly-Si) is one selected material to deposit good passivation on c-Si wafer. A high-temperature stable carrier-selective contact commonly contains a n-type or p-type doped poly-Si layer and a tunneling SiO_2 layer on c-Si wafer.

The common process to fabricate typical poly-Si passivating contacts contains four steps. First, the tunneling SiO_2 layer is formed on both sides of the wafer by a wet-chemical method. Secondly, the intrinsic amorphous silicon (a-Si) is also deposited on both sides of the wafer by means of low-pressure chemical vapor deposition (LPCVD). Thirdly, an ex-situ single-sided doping process is realized using ion-implantation technique. Fourthly, a high temperature annealing step is carried out to activate and drive-in the implanted dopants while also turning the a-Si into poly-Si.[32]

In 2017, an optimized IBC solar cell fabricated by Photovoltaic Materials and Devices group of Delft University of Technology showed excellent passivation and obtained over 22% efficiency. [32]

2.2.2 Silicon heterojunction based passivated contacts

Silicon heterojunction (SHJ) solar cell technology is one advanced solar cell

fabrication process. Compared with other high-efficiency solar cell with sophisticated structures, SHJ solar cells are also good at performance but more cost-saving to qualify for the industrial requirements.[33]

As shown in Figure 5, in a typical SHJ solar cell, the thin intrinsic hydrogenated amorphous silicon (a-Si:H) layers with 5-10 nm thickness are deposited on both sides of an n-type c-Si wafer. The thickness of c-Si wafer is normally 100-160 μm. [33] N-type wafer is preferred due to its better performance on efficiency. After the deposition of the intrinsic a-Si:H layers, the p-type and n-type a-Si:H layers are deposited in the illuminated and the non-illuminated side of the wafer, respectively, with a thickness in the range 5-10 nm for both layers. Afterwards, a transparent conductive oxide (TCO) layer is deposited on top of both the p- and n-type a-Si:H layers. Typically, the front and the back TCO layers have a thickness of 70 nm and 150-200 nm, respectively. The trade-off between efficiency of carrier transport and effect of anti-reflecting coating is required when deciding the thickness of TCO. Finally, metal grids are deposited on both front and back of solar cell. The whole process can be operated under 250 ℃, which reduce the cost of fabrication. The low temperature processing not only requires low temperature budget but also avoids the breakage of thin wafers. The thinner wafers are available for SHJ solar cell.

In 2016, Kaneka Corporation fabricated a heterojunction back-contact crystalline silicon solar cell, which reached the new efficiency record of 26.33% in the world.[11] The Carrier-selective contacts are used to achieve both good passivation and low contact resistance.

In order to investigate the high efficiency carrier selective contacts, a method to measure the specific contact resistance in semiconductor device is necessary. TLM method is proposed for this purpose.

2.3 Transmission Line Model measurement

The transmission line model (TLM) measurement is a convenient method to obtain the specific planar contact resistance. It was proposed by G. K. Reeves and H. B. Harrison in 1982.[34]

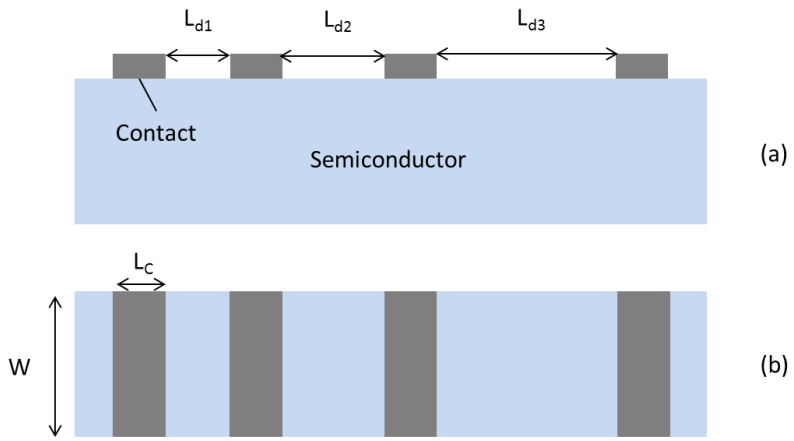

Figure 11 A schematic of TLM experiment setup, in which (a) indicates front view and (b) indicates top view

As shown in Figure 11, an experiment was proposed to study the total resistance R_t between two contacts with width W and length L_C. The two contacts are at the distance of L_d. The total resistance R_t are measured and plotted as a function with increasing distance L_d.

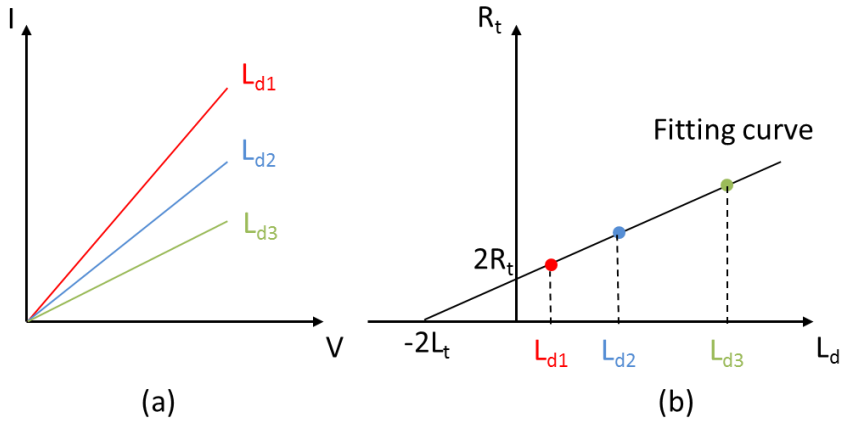

Figure 12 A schematic of (a) measured I – V curve for varying L_d and (b) R_t as function with increasing L_d

As shown in Figure 12 (a), the current-voltage data are measured between every two contacts. Through linear fitting the total resistance R_t can be obtained for varying contact distance L_d. In Figure 12 (b), R_t is plotted as a function with increasing L_d. The scattering R_t data points are fitted by one-dimensional polynomial function. The expression[34] of fitting curve can be written by following.

$$R_t = 2\frac{R_s \cdot L_t}{W} + \frac{R_s}{W}L_d = 2R_C + \frac{R_s}{W}L_d \qquad (2\text{-}17)$$

Where R_C indicates the contact resistance; R_S indicates the sheet resistance of the semiconductor; L_t indicates transfer length; L_C indicates the contact length; W indicates the wafer width. Through the intercept and slope of fitting curve, R_S, L_t, R_C can be obtained. The resistivity ρ_c can be expressed by following

$$\rho_C = R_C L_t \mathrm{W} \tag{2-18}$$

When semiconductor sheet resistance R_S is too small, the $R_t - L_d$ fitting curve will be very flat and intersect with X-axis at very negative point. A huge value of L_t will be obtained, even larger than the contact length L_C in this condition. The correction factor coth(L_C/L_t) is taken into account to solve this problem. The corrected expression[35] is shown by following.

$$R_t = 2\frac{R_s \cdot L_t}{W}\coth\left(\frac{L_C}{L_t}\right) + \frac{R_s}{W}L_d = 2R_C\coth\left(\frac{L_C}{L_t}\right) + \frac{R_s}{W}L_d \tag{2-19}$$

As shown in Figure 13, when L_t is smaller than half of L_C, the value of correction factor is close to 1 and has no impact on results. When L_t is larger than L_C, correction factor will increases and make R_C decrease. The value of ρ_c is corrected in appropriate magnitude.

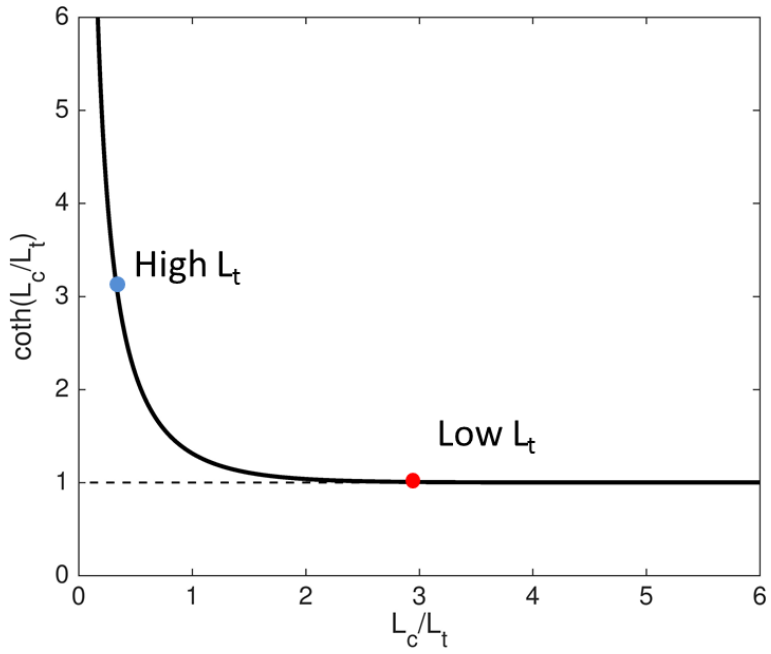

***Figure 13 A schematic of the value of correction factor* coth(L_C/L_t)**

This correction factor is the simplification of the method proposed by G. K. Reeves and H. B. Harrison. They considered both the sheet resistance of semiconductor bulk R_{SH} and the sheet resistance under contacts R_{SK}. The details of method are presented in [34]. When R_{SH} has great difference with R_{SK}, Eq (2-19) cannot describe the $R_t - L_d$ relation perfectly. The contact resistivity ρ_c is hard to achieve precisely. In simulation approach, this problem can be alleviated by increasing the length of contact L_C (i.e. the width of metal finger for practical device) and deploying contacts with wider distance L_d (i.e. the pad spacing for practical device).

The TLM measurements will be simulated by TCAD Sentaurus to study the resistivity of specific contact stacks.

2.4 Research questions

In this thesis, the following questions will addressed,

a) What factors determine the resistivity of carrier selective contacts stack and how they affect the such value?

   i. Poly-Silicon based CSC

   ii. Silicon Heterojunction CSC

b) What is the contribution of each layer and interface to the equivalent resistivity of contact stacks?

c) Which transport mechanism dominates the resistivity of contact stacks?

d) How can we reduce or manipulate the resistivity of contact stacks?

3 Simulation Approach

The accurate solution of the drift-diffusion model is not an analytical equation, in which it is considered all the spacial domain to investigate. Such an assumption, include boundary conditions and symmetry assumptions. This is possible thanks to Technology Computer-Aided Design (TCAD) simulation tools.

In this thesis, TCAD Sentaurus simulation tool is used to model the semiconductor device. TCAD Sentaurus is a simulation tool that include state-of-the-art models and parameters.[36] Moreover, it include ad-hoc drift diffusion model that allows numerical stability for solutions using self-consistent models.

In the following, the simulation process to model TLM structures is described.

3.1 Numerical tools

Numerical modeling has been applied to Si solar cells since the early days of computer modeling and has recently become widely used in the photovoltaics (PV) industry. Simulations are used to analyze fabricated cells and to predict effects due to device changes. Hence, they may accelerate cell optimization and provide quantitative data e.g. of potentially possible improvements, which may form a base for the decision making on development strategies.[22]

TCAD Sentaurus simulation tool is used to simulate the process of TLM measurement. The input parameter sets in this thesis refer to [37], in which A. Fell, K. R. McIntosh, P. P. Altermatt et al provided complete and representative input parameter sets to simulate crystalline silicon solar cells.

The simulation of TLM measurement includes following parts: model building, numerical solution, data processing, as shown in Figure 14.

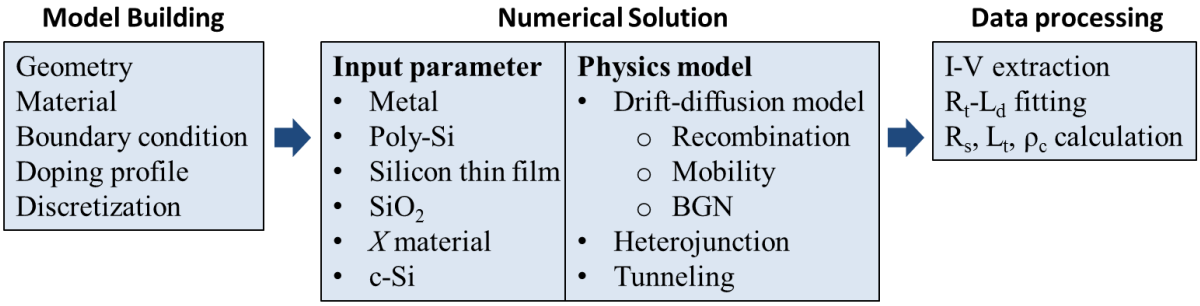

Figure 14 A flow chart of the simulation process

3.1.1 Model building

Sentaurus Structure Editor (SDE) can be used as a two-dimensional (2D) or three-dimensional (3D) structure editor, and a 3D process emulator to create TCAD devices. In Sentaurus Structure Editor, structures are generated or edited interactively using the graphical user interface (GUI). Alternatively, devices can be generated in batch mode using scripts. Scripting is based on the Scheme scripting language.[38]

The device is firstly built as a two-dimensional model using scripts in Sentaurus structure editor. 2D objects are created according to the required dimension of each layer. The geometry of model structure can be flexibly defined as variables, such as the distance between two contacts L_d, which makes the related tests easier to run in simulation sequences.

The materials of each layer can be conveniently defined if they are included in the database of default materials. New materials need be added in database by the custom external file, such as the amorphous silicon involved in **Chapter 5**.

The boundary conditions define the known states of the semiconductor device in which the numerical solver calculate the parameters to investigate. In case of TLM, the boundary is defined as the contacts the semiconductor device. The applied voltage of contacts is varying in order to obtain the current-voltage (IV) characteristic of contact stacks.

Doping profile can be defined with different dopants, which are phosphorus atoms as donors and boron atoms as acceptors in this case. Accordingly, the dopant species can be declared in SDE. The doping profile can be described as dopants distribution following different functions, which are commonly constant function for uniform doping and Gauss function for buried doping as simplification of actual distribution. If the measurements of experimental doping profile are available, the measured doping concentration as function with varying doping depth can be defined as an external file according to the measurements. In many cases, the doping concentration is defined as variable in order to the related tests, presented in **Chapter 4** and **Chapter 5**, run in simulation sequences.

In applied mathematics, discretization is the process of transferring continuous functions, models, variables, and equations into discrete counterparts. This process is usually carried out as a first step toward making them suitable for numerical evaluation and implementation on digital computers.[39] The 2D model is discretized by meshing with appropriate grids. The mesh grids define the minimal computation cell of the simulation. A proper meshing scheme can make the simulation results accurate with acceptable computing time. The dense mesh grids should be defined at the region where massive carrier transport happen to obtain accurate results. The mesh grids at other regions should be loose to save computing time. For the tests

involved in **Chapter 4** and **Chapter 5**, the mesh girds are refined at interface between every two layers and around the contacts, as shown in Figure 15.

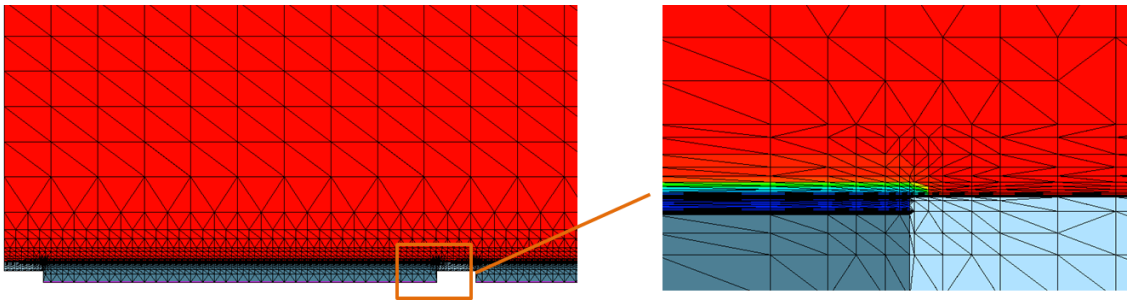

Figure 15 A schematic of the mesh grids of the model, in which a part of the entire mesh and its partial enlarged detail are indicated

After building the virtual device, the numerical solution can be implemented in Sentaurus Device.

3.1.2 Numerical solution

Sentaurus Device (SDEVICE) simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms. A real semiconductor device, such as a transistor, is represented in the simulator as a “virtual” device whose physical properties are discretized onto a non-uniform “grid” (or “mesh”) of nodes.[40]

The files generated by SDE provide the part of input parameters for numerical solution. Some parameters of material need be defined in parameter files for SDEVICE, such as the tunneling mass and band energy state. The initial potential and resistance of metal contacts are provided as input parameters for the solver. The metal contacts have a resistance of 1 mΩ as default value. The initial potential of two contacts is set as zero. One will keep constant, and the other will be raised to 1 V iteratively, so that the current function with varying contact voltage can be obtained.

The semiconductor physics and carrier transport mechanism are defined as physics models for numerical solver. The software integrates commonly-used physics models, which are described in user guide[40] in detail. The required physics models can be easily announced and activated for solver. Some physics models need define specific parameters, which should be written in parameters file. If the tests involve unusual physics models, they should be defined in the external files. The involved physics models will be described in following section.

In this case, the quasistationary solver is selected to compute the current generated between two contacts. The final voltage of contacts and the voltage variation in each iterated step are defined. The results are obtained when simulation sequences is

finally finished or halt due to convergence problems.

3.1.3 Data processing

Sentaurus Visual can be used to create plots that display fields, geometries, and regions, including results such as p-n junctions and depletion layers. It also allows you to view I–V curves and doping profiles, and provides tools to zoom, pan, and rotate images. You also can extract data using measure and probe tools.[41]

MATLAB (matrix laboratory) is a multi-paradigm numerical computing environment and proprietary programming language developed by MathWorks.[42]

Sentaurus Visual extracts the I-V data of contacts and band diagram of semiconductor obtained from numerical solution into the coordinate file (CSV file). MATLAB provides one-dimensional polynomial function curve fitting tool to fit the I-V curves linearly. The total resistance R_t between two contacts can be obtained from the slope of fitting curves. Through increasing the contact distance L_d, a set of R_t as function with varying L_d can be obtained. After fitting the Rt-Ld curve by Eq (2-19), the sheet resistance R_s, transfer length L_t, contact resistance R_C, and contact resistivity ρ_c can be calculated.

3.2 Physics model

The TCAD Sentaurus integrates a lot of physics models to simulate the carrier behavior in semiconductor device. As shwn in Figure 14, the main physics models used in this project include drift-diffusion model, hetero-interfaces, and nonlocal tunneling model. The drift-diffusion model and hetero-interfaces have been introduced in **Chapter 2, Section 2.1**. The remaining physics model for recombination, mobility, and tunneling will be introduced in following sections.

3.2.1 Recombination model

The drift-diffusion model is taken into account for the semiconductor device, in which the Shockley-Read-Hall (SRH) model is used for main generation-recombination model. In Sentaurus Device, the following form is implemented.[43]

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{3-1}$$

With,

$$n_1 = n_{i,eff}\exp\left(\frac{E_{trap}}{kT}\right) \tag{3-2}$$

And,

$$p_1 = n_{i,eff}\exp\left(\frac{-E_{trap}}{kT}\right) \tag{3-3}$$

Where n, p, and $n_{i,eff}$ describe the electron, hole, and effective intrinsic density, respectively; τ_p and τ_n indicate the electron and hole lifetimes; E_{trap} is the difference between the defect level and intrinsic level. The variable E_{trap} is accessible in the parameter file. The silicon default value is $E_{trap} = 0$.

The surface SRH recombination model can be activated at semiconductor-semiconductor and semiconductor-insulator interfaces. At interfaces, an additional formula is used. The detailed expression refers to [43].

3.2.2 Mobility model

Sentaurus Device uses a modular approach for the description of the carrier mobilities. In the simplest case, the mobility is a function of the lattice temperature. This so-called constant mobility model.[44]

The Philips unified mobility model, proposed by Klaassen[45], unifies the description of majority and minority carrier bulk mobilities. In addition to describing the temperature dependence of the mobility, the model takes into account electron-hole scattering, screening of ionized impurities by charge carriers, and clustering of impurities. The description for the model refers to [44].

In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to a finite speed. The high-field saturation models[44] describe mobility degradation in high electric fields

3.2.3 Tunneling model

Quantum-mechanical tunneling of charge carriers through classically forbidden regions is one of the most interesting quantum-mechanical effects. It is therefore necessary to account for tunneling effects in the design of semiconductor devices.[46]

The tunneling current depends on the band edge profile along the entire path between the points connected by tunneling. This makes tunneling a nonlocal process. The nonlocal tunneling model[47] is activated at interfaces, contacts, and junctions.[48] As shown in Figure 16, nonlocal mesh indicates the region and tunneling path for the carriers that cross the barrier. For the material containing trap state in forbidden band, the trap-assisted tunneling will happen. Traps can be coupled to nearby interfaces and contacts by tunneling. Sentaurus Device models nonlocal tunneling to traps as the sum of an inelastic, phonon-assisted process and an elastic process.[49-50]

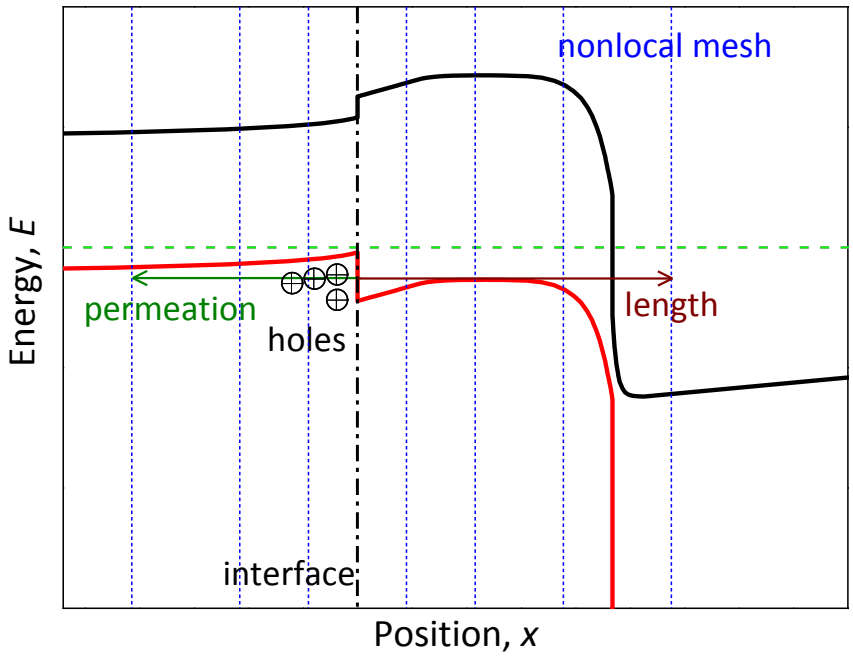

Figure 16 A schematic of nonlocal tunneling for hole carrier, in which the interface, nonlocal mesh, holes, and traps are indicate

3.2.4 Schottky barrier model

At the metal/semiconductor interface, the Schottky contacts are defined. The details refer to [51-52]. The barrier lowering model is used to describe the carrier behavior that electron being emitted from metal into the conduction band or hole being emitted into valence band. The most important one is the image force[25], but it can also model tunneling and dipole effects. The details of barrier lowering model refer to [53].

3.3 Materials

The semiconductor materials involved in this study includes layers used on CSCs as crystalline silicon (c-Si), polycrystalline silicon (poly-Si), silicon oxide (SiO_2), transparent conductive oxide (TCO), and metals (Al or Cu).

3.3.1 Crystalline silicon

Crystalline silicon (c-Si) is commonly used in semiconductor industry. It is the dominant material to fabricate semiconductor device. The typical form of c-Si used for semiconductor is monocrystalline silicon (mono-Si), which has the homogeneous crystal structure inside material and high purity as shown in Figure 17.[24] Due to this nature, the constant atomic structure and electrical properties can be achieved. The typical band gap energy of c-Si is 1.12 eV at 273 K.

3.3.2 Amorphous silicon

Amorphous silicon (a-Si) is the typical material used in thin film solar cell and silicon heterojunction solar cell. The main usage of a-Si is for passivating. During fabricating SHJ solar, the a-Si layer is deposited on both front and back sides of c-Si wafer. The whole process can work under 250 ℃. The low temperature budget requirement reduces the cost of fabrication, which makes a-Si a preferable material in PV technologies.[54]

As shown in Figure 17, differing with c-Si, the atomic structure of a-Si is not homogeneous, which leads a considerable number of defects in a-Si. These defects are due to the unpaired electron of Si atoms, which are dangling bonds and often present on the surfaces of c-Si wafer. Hydrogen is often used for passivating the dangling bond in a-Si to reduce the defect density. This is so-called hydrogenated amorphous silicon (a-Si:H).[55]

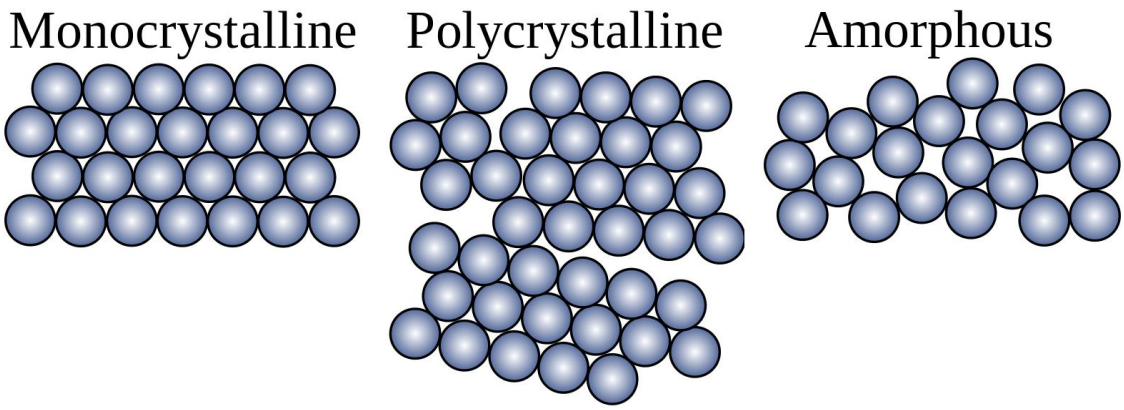

Figure 17 A schematic of different forms of silicon[24]

Due to the heterogeneous atomic structure, the distribution of energy state for a-Si is more complicated than that for c-Si as shown in Figure 18. The band gap of a-Si is 1.5 - 1.7 eV, wider than c-Si. The band edges are extended with tail states. The dangling Si bonds lead the midway energy states between conduction band and valence band. The carriers are frequently trapped in these band tails, which presents the trap density of a-Si layer.[56]

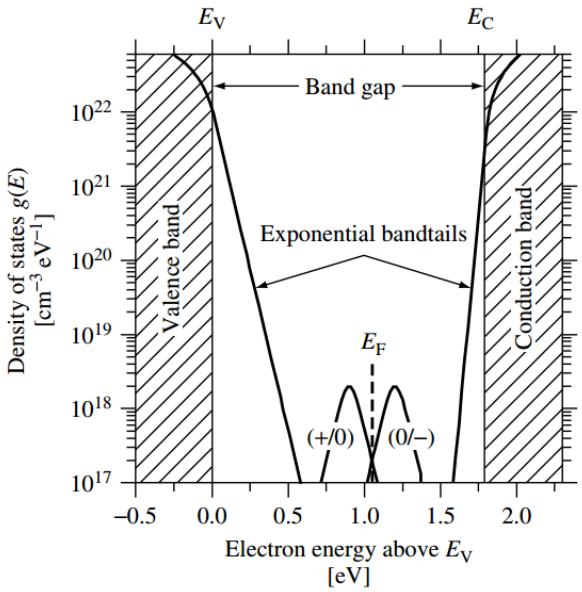

Figure 18 A schematic of Density of electronic states g(E) in hydrogenated amorphous silicon. The shaded areas indicate delocalized states in the bands; these bands themselves have tails of localized states with an exponential distribution. Midway between the bands are levels belonging to gross defects such as dangling Si bonds indicated by the two peaked bands around E_F [56]

3.3.3 Polycrystalline silicon

Polycrystalline silicon (poly-Si) is the common material used in PV technology and electronic production. As shown in Figure 17, the homogeneity of atomic structure for poly-Si is between c-Si and a-Si. There are many crystal planes, also called grains, inside poly-Si with different lattice orientations, which leads some broken covalent bonds at the grain boundary.[57]

The most common fabrication methods are: partial CW-laser annealing, zone melting recrystallization, molecular beam epitaxy, and chemical vapor deposition.[58]

The first method uses a CW (continuous wave) laser equipment to anneal partial implantation damage within an amorphous silicon layer. Due to the heavy ion bombardment, the regularity of the silicon matrix was destroyed. The energy of the light beam melts the silicon crystal and, hence, recrystallization occurs. The grain size of the recrystallized silicon can be controlled by the laser power. CW-laser annealing is applied on a limited area, while the zone melting recrystallization is used to fabricate large-area polysilicon layers. An IR (infrared) or UV (ultra violet) source is scanned across the wafer and, thus, a narrow but large polysilicon recrystallization zone is created. [58]

The molecular beam epitaxy (MBE) is the most expensive method. It operates at lower temperatures than the other methods, so the annoying dopant redistribution is suppressed. An evaporated molecular beam is directed towards the substrate surface. The low vapor pressure of silicon ensures the condensation of the material on the surface. [58]

The most common method for fabrication of polysilicon layers for VLSI circuits is pyrolizing silane SiH_4 between 575 °C and 650 °C in a low pressure ambient, which is referred to as low pressure chemical vapor deposition (LPCVD). [58]

3.3.4 Silicon dioxide

Silicon dioxide (SiO_2) is an oxide of silicon. The common form of SiO_2 is quartz in nature and amorphous thin film in semiconductor device. It is frequently used as electrical insulator in PV technology. In fabrication of semiconductor device, high quality films can be obtained by thermal oxidation of Si, which leads a smooth and low-defect SiO_2 interface in Si wafer. SiO_2 can also be deposited through chemical vapor deposition (CVD).[60] The typical band gap energy is 9 eV.[61]

3.3.5 Transparent conductive oxide

Transparent conductive oxide (TCO) is frequently used as the optically transparent electrode at the front side of solar cell. TCO materials are required high optical transparence and electrical conductance. Among such various TCO materials, indium tin oxide (ITO) is the most commonly used. TCO can act as the electrode with low resistance and without blocking light. It should have wide band gap so that the photons with energy lower than band gap energy will not be absorbed in this material. The typical carrier concentration for TCO used in solar cell is on magnitude of 10^{20} cm^{-3} in order to obtain low resistivity on magnitude of 10^{-4} Ωcm for ITO and the band gap energy higher than 3.1 eV.[62] In particular, TCO is modelled as wide bandgap degenerate semiconductor, using carrier concentration as active doping.

Contact stack is considered as the formation with multiple layers of different materials. It may contain heterojunctions, Schottky interfaces, insulator and so on.

3.4 Contact stack evaluation

As shown in Figure 19, the contact stack is a formation with multiple layers. Each layer has its own resistance due to material property. The interface between any two layers also has the resistance, which is the barrier for carrier to cross. The equivalent resistance of contact stack can be measured by TLM method, discussed in **Chapter 2, Section 2.3**.

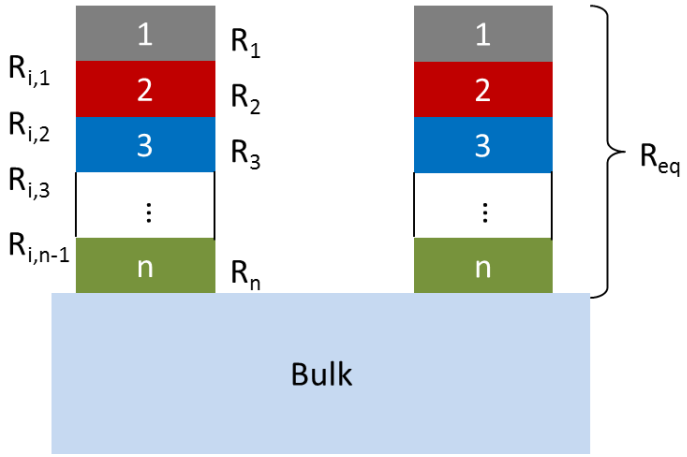

Figure 19 A schematic of contact stack with multiple layers, in which the resistance of each layer are indicated with R_1, R_2, R_3,…, R_n; the resistance of interface are indicated with $R_{i,1}$, $R_{i,2}$, …, $R_{i,n-1}$

The equivalent resistance of contact stack is the sum of layer resistance and interface resistance, which can be expressed with Eq (3-5),

$$R_{eq} = (R_1 + R_2 + \cdots + R_n) + \left(R_{i,1} + R_{i,2} + \cdots + R_{i,n-1}\right) \qquad (3\text{-}4)$$

The results obtained from TLM measurement are the equivalent resistance and resistivity of contact stack. In order to obtain the specific interface resistance, the other layers should be conducted to make the current flow through the layer under that interface, as shown in Figure 20. The equivalent resistance is measured for the stack including different layers. The subtraction of the measured results is the interface resistance.

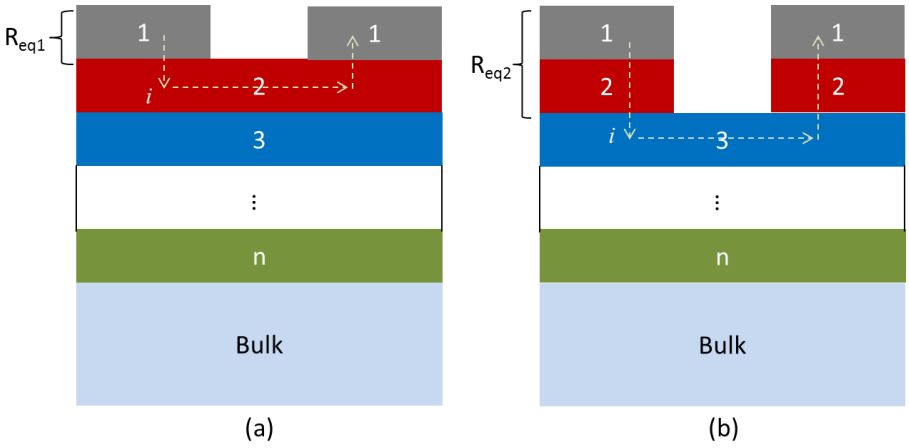

Figure 20 A schematic of contact stack with (a) layer 2, 3, …, n connected and (b) layer 3 , …, n connected, in which the flow path for current i is indicated by dashed arrow.

For example, the interface resistance $R_{i,2}$ can be expressed as the subtraction between two equivalent resistance,

$$R_{i,2} = R_{eq2} - R_{eq1} \qquad (3\text{-}5)$$

3.5 Model description

The models of poly-Si based passivated wafer and SHJ based passivated wafer for TLM measurements are created.

3.5.1 Model 1: poly-Si based passivated wafer

The structure of poly-Si based passivated wafer is shown in Figure 21.

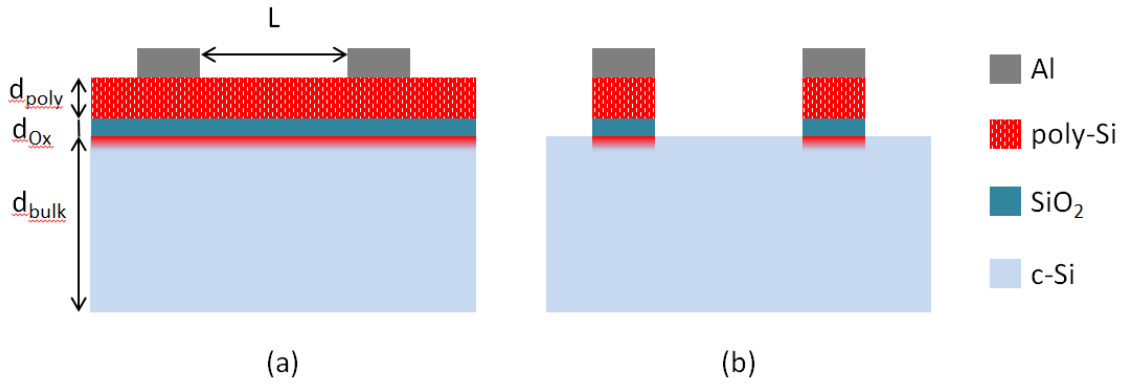

Figure 21 A schematic of the model structure for poly-Si based passivated wafer, in which (a) indicates the wafer with conducted poly-Si layer and (b) indicates the wafer with complete contact stack

Where L indicates the distance between two contacts; d_{poly}, d_{Ox}, d_{bulk} indicate the thickness of each layer. In the 2D deployment, the width of the wafer W is considered as 1 μm by default. The thickness of c-Si bulk d_{bulk} is 280 μm. The thickness of poly-Si layer d_{poly} is 100 nm. The doping concentration of c-Si bulk N_{bulk} is 1×10^{15} cm^{-3}. The doping concentration of poly-Si N_{poly}, the thickness of SiO_2 layer d_{Ox}, and the peak doping concentration of buried region N_{peak} are varying variables. In Figure 21 (a), the poly-Si layer is conducted. Since the poly-Si layer is highly-doped, it is much conductive. The tunnelling barrier of SiO_2 layer is so high that most carriers will transfer through poly-Si layer. The current between two contacts will flow through poly-Si layer under low resistance. In Figure 21 (b), since the doped poly-Si layer is discontinuous between two contacts, the carriers will be forced to transport across SiO_2 layer. The current will flow into c-Si bulk by overcoming the resistance of interfaces and c-Si bulk resistance.

In order to obtain accurate simulation results, the model should be finely meshed. The bulk region is generally meshed with grids of 50 μm × 10 μm. The poly-Si and metal region are generally meshed with grids of 2.5 μm × 10 μm. The mesh around material interface is refined vertically with increasing distance.

Since the poly-Si layer and c-Si bulk can be n-type or p-type doped, there are four kinds of models: n-Contact n-Bulk, n-Contact p-Bulk, p-Contact n-Bulk, and p-Contact p-Bulk. For n-Contact p-Bulk model and p-Contact n-Bulk model, two opposite equivalent diodes will be formed at contact/bulk interface due to the p-n

junction effect. The current cannot flow through two contacts when poly-Si layer is not continuous like the situation in Figure 22, which should be avoided in complete stack model.

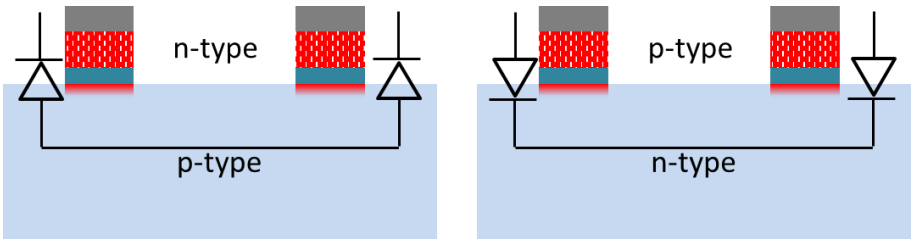

Figure 22 A schematic of equivalent diode formed in n-Contact p-Bulk and p-Contact n-Bulk complete contact stack model.

The band diagrams of n-Contact n-Bulk model and p-Contact p-Bulk model are shown in Figure 23 (a) and (b) respectively.

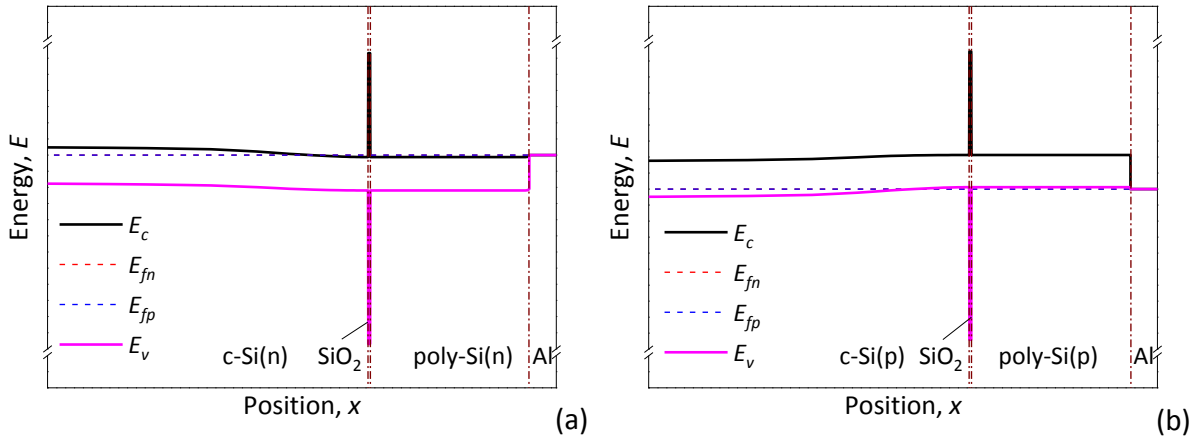

Figure 23 A schematic of the band diagrams for poly-Si based passivated wafer, in which the band diagram of n-Contact n-Bulk model is indicated in (a) and the band diagram of p-Contact p-Bulk model is indicated in (b)

The parameters and physics models used are shown in Table 1.

Table 1 Physics models and parameters for poly-Si based passivated wafer

Model	Parameter
c-Si bulk	Thickness: 280 μm Electron affinity: 4.05 eV Band gap energy: 1.12 eV Doping concentration: 1×10^{15} cm^{-3} Buried doping region: Gaussian profile Tunneling mass m_t: Conduction-band tunneling mass: 0.19 m_0 Valence-band tunneling mass: 0.16 m_0

SiO_2 insulator	Thickness: default: 1.5 nm, varying range: 0.5 ~ 2.5 nm Band gap energy: 9 eV Tunneling mass m_t: Conduction-band tunneling mass: 0.4 m_0 Valence-band tunneling mass: 0.3 m_0
poly-Si passivation	Thickness: 100 nm Electron affinity: 4.05 eV Band gap energy: 1.12 eV Doping concentration: default: 1×10^{15} cm^{-3}, varying range: 5×10^{17} ~ 2×10^{20} cm^{-3} Tunneling mass m_t: Conduction-band tunneling mass: 0.36 m_0 Valence-band tunneling mass: 0.38 m_0
Metal contact	Aluminum
Band gap narrowing	Schenk model[63] in c-Si bulk
Recombination	SRH and surface SRH model
Mobility	Philips unified mobility model and high-field saturation models
Tunneling	Dynamic nonlocal path band-to-band model Nonlocal mesh: c-Si/SiO_2 interface
Schottky barrier	Schottky contact at poly-Si/Al interface

3.5.2 Model 2: SHJ based passivated wafer

The structure of SHJ based passivated wafer is shown in Figure 24.

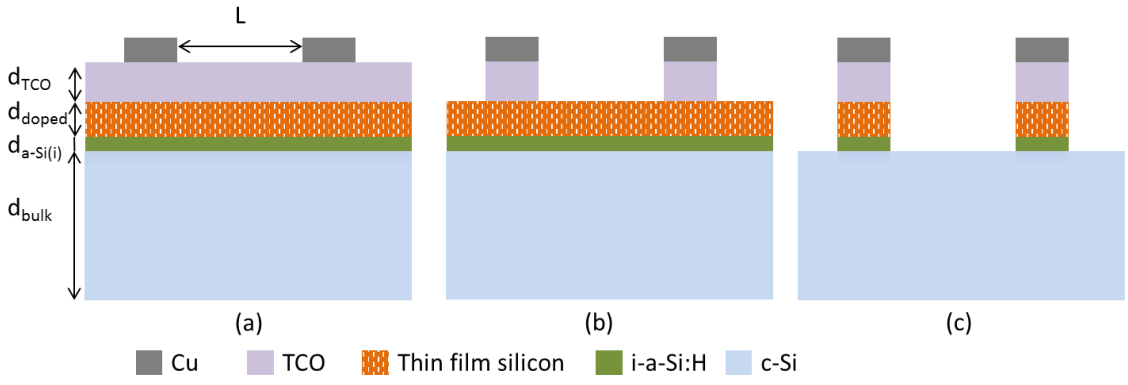

Figure 24 A schematic of the model structure for SHJ based passivated wafer, in which (a) indicates the wafer with connected TCO and doped layers, (b) indicates the wafer with connected doped layer and (c) indicates the wafer with complete stack

Where thin film silicon is the doped layer; *L* indicates the distance between two

contacts; d_{doped}, $d_{a\text{-}Si(i)}$, d_{bulk}, d_{TCO} indicate the thickness of each layer. In the 2D deployment, the width of the wafer W is considered as 1 μm by default. The thickness of c-Si bulk d_{bulk} is 260 μm. The thickness of doped layer d_{doped} is 20 nm. The doping concentration of c-Si bulk N_{bulk} is 1×10^{15} cm^{-3}. The doping concentration of thin film silicon N_{doped}, the TCO carrier concentration N_{TCO}, the thickness of i-a-Si:H layer $d_{a\text{-}Si(i)}$, and the band gap energy of thin film silicon E_g are varying variables. In Figure 24 (a), the doped layer and TCO layer are connected between contacts. Since the TCO layer is very conductive. The current between two contacts will flow through TCO layer under low resistance. In Figure 24 (b), the doped layer is connected but TCO layer is discontinuous between contacts. The current flow through either doped layer or c-Si bulk depending on the doping type. In Figure 24 (c), since the doped layer is discontinuous between two contacts, the carriers will be forced to transport across doped layer. The current will flow into c-Si bulk by overcoming the tunneling barrier, the resistance of interfaces and c-Si bulk resistance.

The meshing strategy is similar to poly-Si based passivated wafer, which has been introduced in **Chapter 3, Section 3.5.1**.

According to the doping type of doped layer and c-Si, four kinds of model are considered: n-Contact n-Bulk, n-Contact p-Bulk, p-Contact n-Bulk, and p-Contact p-Bulk. For the same reason explained in **Chapter 3, Section 3.5.1**, the model with complete contact stack should avoid using different doping type in contact and bulk.

The band diagrams of n-Contact n-Bulk model and p-Contact p-Bulk model are shown in Figure 25 (a) and (b) respectively.

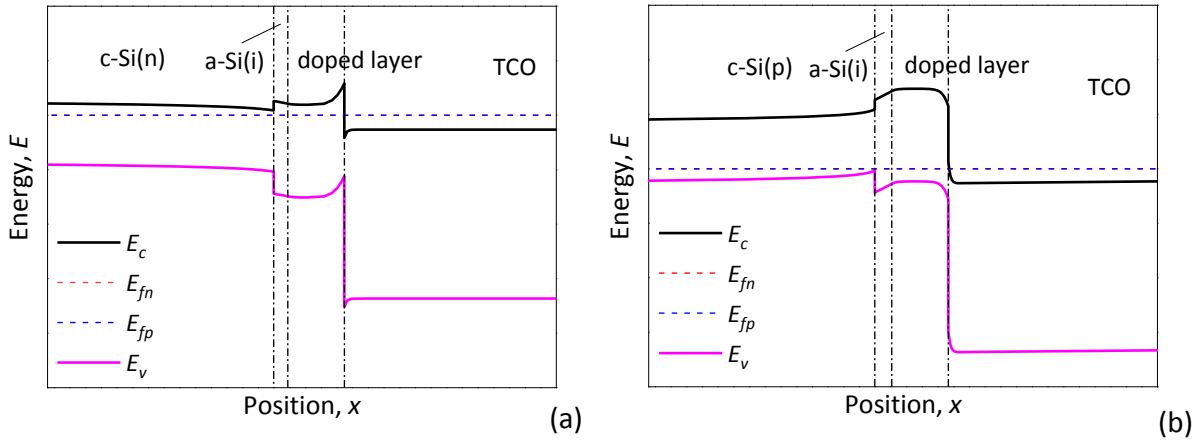

Figure 25 A schematic of the band diagrams for SHJ based passivated wafer, in which the band diagram of n-Contact n-Bulk model is indicated in (a) and the band diagram of p-Contact p-Bulk model is indicated in (b)

The parameters and physics models used are shown in Table 2.

Table 2 Physics models and parameters for SHJ based passivated wafer

Model	Parameter
c-Si bulk	Thickness: 260 μm Electron affinity: 4.05 eV Band gap energy: 1.12 eV Doping concentration: 1.559×10^{15} cm^{-3} Tunneling mass m_t: Conduction-band tunneling mass: 0.19 m_0 Valence-band tunneling mass: 0.16 m_0
Intrinsic a-Si layer	Thickness: default: 5 nm, varying range: 1 ~ 20 nm Electron affinity: 4 eV Band gap energy: 1.7 eV Tunneling mass m_t: Conduction-band tunneling mass: 0.1 m_0 Valence-band tunneling mass: 0.1 m_0
Thin film silicon	Thickness: 20 nm Electron affinity: 4 eV Band gap energy: default: 1.7 eV, varying range: 1.5 ~ 1.8 eV Doping concentration: default: 1×10^{20} cm^{-3}, varying range: n-type: 7×10^{19} ~ 2.5×10^{20} cm^{-3} (activation energy E_a: 350 ~ 18 meV) p-type: 5×10^{19} ~ 2×10^{20} cm^{-3} (activation energy E_a: 400 ~ 53 meV) Tunneling mass m_t: Conduction-band tunneling mass: 0.1 m_0 Valence-band tunneling mass: 0.1 m_0
TCO	Material: ITO Thickness: 140 nm Work function: 4.9 eV Band gap energy: 3.1 eV Carrier concentration: default: 1×10^{20} cm^{-3}, varying range: 1×10^{19} ~ 1×10^{21} cm^{-3} Tunneling mass m_t: Conduction-band tunneling mass: 0.19 m_0 Valence-band tunneling mass: 0.16 m_0
Metal contact	Copper
Band gap narrowing	Schenk model [19] in c-Si bulk
Recombination	SRH and surface SRH model
Mobility	Philips unified mobility model and high-field saturation models
Tunneling	Dynamic nonlocal path band-to-band model Trap-assisted tunneling model Nonlocal mesh: c-Si/i-a-Si:H interface and thin film silicon/TCO interface

4 Polycrystalline Silicon Based Carrier Selective Contacts

As transport mechanisms at hetero-interfaces is described by tunneling and thermionic emission, parameters analized a related to those that affect the band alignment and energy barrier size[64]. Accordingly, In this chapter, the resistivity of poly-Si based contact stack is studied with varying doping concentration of poly-Si N_{poly}, the thickness of SiO_2 layer d_{Ox}, and the peak doping concentration of buried region N_{peak}.

4.1 Validation

In this case, the validating simulation is run to compare with the results of a mimic TLM experiment. The model structure for simulation and measurement is shown in Figure 21 (a). The TLM experiment deploys 8 aluminum metal fingers with dimension of 50 μm × 1 cm × 3 μm as contacts. The contact distance L_d between every two adjacent contacts are set as 25, 500, 1000, 1700, 2500, 3000, and 3500 μm. The simulation uses the model with same dimension as experiment. The doping profile is defined by measured profile from experiment. The metal resistance of contact is not set as default value of 1 mΩ, but calculated according to resistivity of aluminum and dimension of metal finger instead.

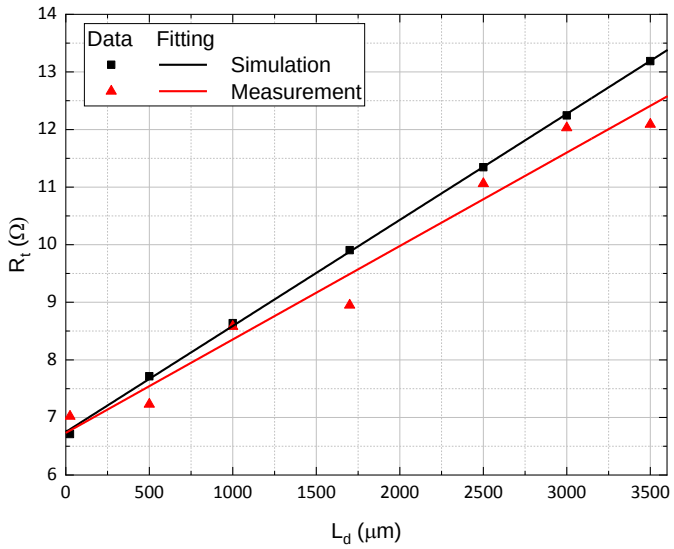

Figure 26 A schematic of R_t – L_d curves for simulation and measurement data, in which the scatters indicate the data points of R_t and solid lines indicate the linear fitting curves R_t - L_d

The simulated results an measured results are shown in Figure 26.

As shown in Figure 26, the red color scatters and lines indicate the measurement data. Through TLM method discussed in **Chapter 2, Section 2.3**, the measured R_t data can be fitted with Eq (2-19) by one-dimensional polynomial function. The goodness of fitting is not completely accurate. The normalized mean squared error (NMSE) for measurement fitting is 0.9681. The contact resistivity ρ_c for measurement is 16.6939 mΩcm^2. The black color scatters and lines indicate the measurement data. On the contrary, the R_t data from simulation show fine linear trend with increasing L_d. The NMSE for simulation fitting is 0.9996, approaching to perfect fitting. The contact resistivity ρ_c for simulation is 16.7158 mΩcm^2.

It turns out from the validation that the simulation can effectively reconstruct the results of TLM experiment. The carrier activities in the poly-Si based passivated wafer can be accurately simulated through simulation approach.

4.2 Doping inside poly-Si layer

The sketch of the structure used within this chapter is shown in Figure 21 (a). The poly-Si and SiO_2 layers are connected within the two contacts. Therefore, the current can flow through the poly-Si layer. Four kinds of model are involved:

i. To calculate the equivalent contact resistance avoiding reverse diode behavior: n-Contact n-Bulk and p-Contact p-Bulk.

ii. To calculate contact resistance at poly-Si/Metal interface: n-Contact p-Bulk and p-Contact n-Bulk. The p-n diode effect from poly-Si/c-Si junction impedes the current flow in c-Si bulk.

The parameters and physics models are defined in Table 1. Except the doping concentration of poly-Si N_{poly} is valued as 1×10^{18}, 5×10^{18}, 2×10^{19}, 1×10^{20}, and 2×10^{20} cm^{-3}, the other parameters are defined as default value. Contact distance L_d is valued as 10, 20, 40, 80, and 160 μm. 25 sequences for each model should be run in total.

4.2.1 Results

The calculation process for n-Contact n-Bulk is taken as example. The I-V data for N_{poly} equal to 1×10^{20} cm^{-3} are shown in Figure 27.

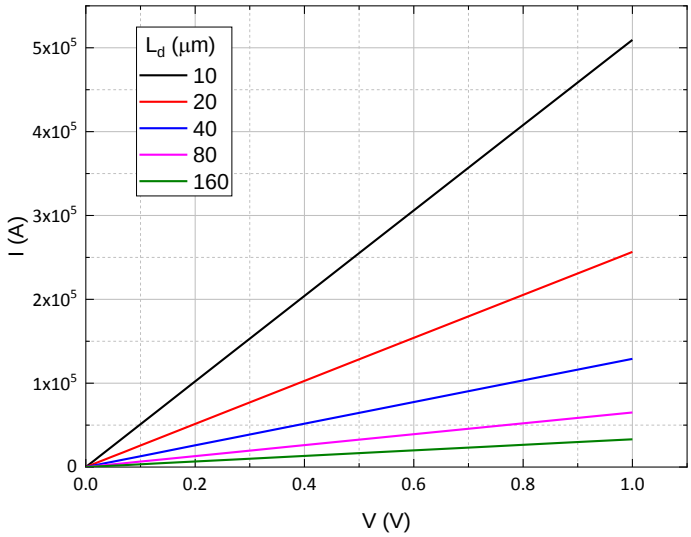

Figure 27 A schematic of I-V curves for N_{poly} = 1×10^{20} cm^{-3} of n-Contact n-Bulk model, in which the curves for contact distance ranged from 10 to 160 μm are indicated

As shown in Figure 27, the I-V data show good linear characteristic. The total resistance R_t can be obtained from the fitting curve as the inverse slope of I-V plot. It is obvious that smaller L_d leads lower R_t. The R_t data and fitting curves are shown in Figure 28. It can be seen that linear trends of R_t with increasing L_d, which is in agreement with TLM method. Through fitting the data with Eq (2-19), the contact resistance R_c, transfer length L_t, sheet resistance R_s can be obtained. The resistivity is calculated then. The results are shown in Figure 29.

For n-Contact n-Bulk and n-Contact p-Bulk models, it can be seen in Figure 29 that the resistivity ρ_c of Metal/poly-Si contact stack is reduced when increasing the poly-Si doping concentration N_{poly}. This is because potential barrier size of poly-Si layer is reduced, so that the potential barrier for carrier transport decreases. The p-Bulk model has higher ρ_c is due to the different barrier height: 4.65 eV and 3.1 eV for holes and electrons respectively.

There are some numerical issues for p-Contact n-Bulk and p-Contact p-Bulk models. They will be discussed in next section **4.2.2**.

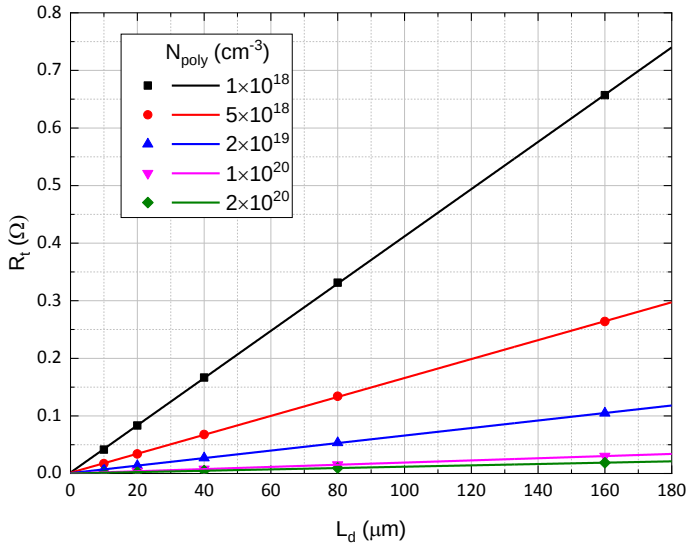

Figure 28 A schematic of R_t – L_d curves for n-Contact n-Bulk model, in which the curves for N_{poly} ranged from 1×10^{19} to $1\times10^{21}cm^{-3}$are indicated, where scatters indicate the data points of R_t and solid lines indicate the linear fitting curves R_t - L_d

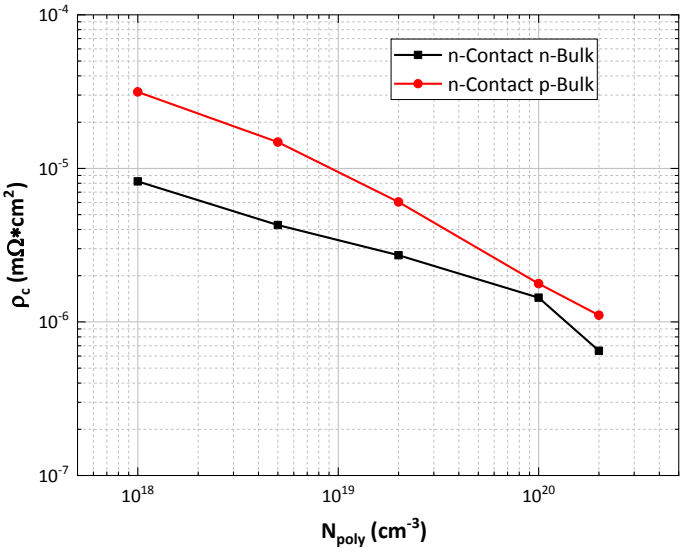

Figure 29 A schematic of the resistivity ρ_c for Metal/poly-Si contact stack as function with varying N_{poly}, in which the ρ_C – N_{poly} curves for n-Contact n-Bulk and n-Contact p-Bulk model are indicated

4.2.2 Numerical issues

For p-Contact n-Bulk and p-Contact p-Bulk models, the I-V plots show nonlinear characteristic. This is due to the Schottky barrier formed at metal-semiconductor interface.

As shown in Figure 30, the Schottky contact is activated at Metal/poly-Si interface. The conduction band of poly-Si layer is bent downwards and makes electrons become beneficial carrier to transport over the interface. The holes transport is influenced by diode effect and leading nonlinear I-V plots. The precise resistance between two contacts cannot be obtained.

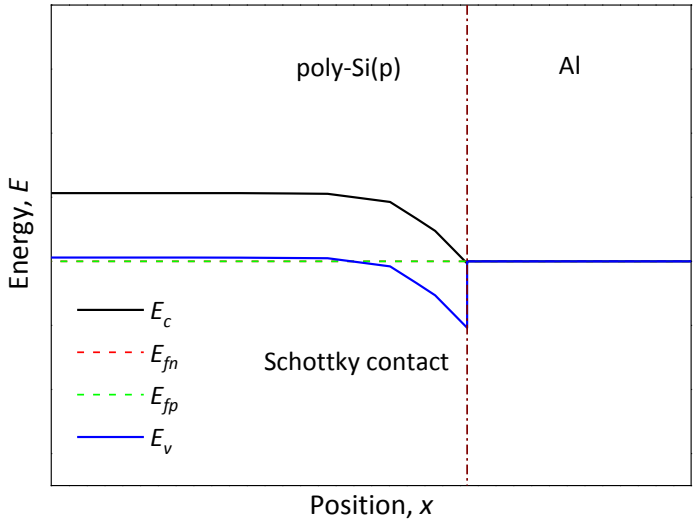

Figure 30 A schematic of band diagram at Metal/poly-Si interface for p-Contact n-Bulk model

4.3 Potential barrier size and band alignment: d_{Ox} and N_{peak}

The complete contact stack of Metal/poly-Si/SiO_2/c-Si is modeled in this case. The model structure is shown in Figure 21 (b). The peak doping concentration of buried region N_{peak} is valued as 1×10^{17}, 1×10^{18}, 1×10^{19}, 1×10^{20}, and 1×10^{21} cm^{-3}. The thickness of SiO_2 d_{Ox} is valued as 0.5, 0.7, 1, 1.2, 1.5 and 1.7 nm. The other parameters are defined as default value. Contact distance L_d is valued as 10, 20, 40, 80, and 160 μm. 150 sequences for each model should be run in total.

4.3.1 Results

Through same calculation process presented in **Chapter 4, Section 4.2.1**. The resistivity ρ_c as function with varying d_{Ox} and N_{peak} are shown in Figure 31.

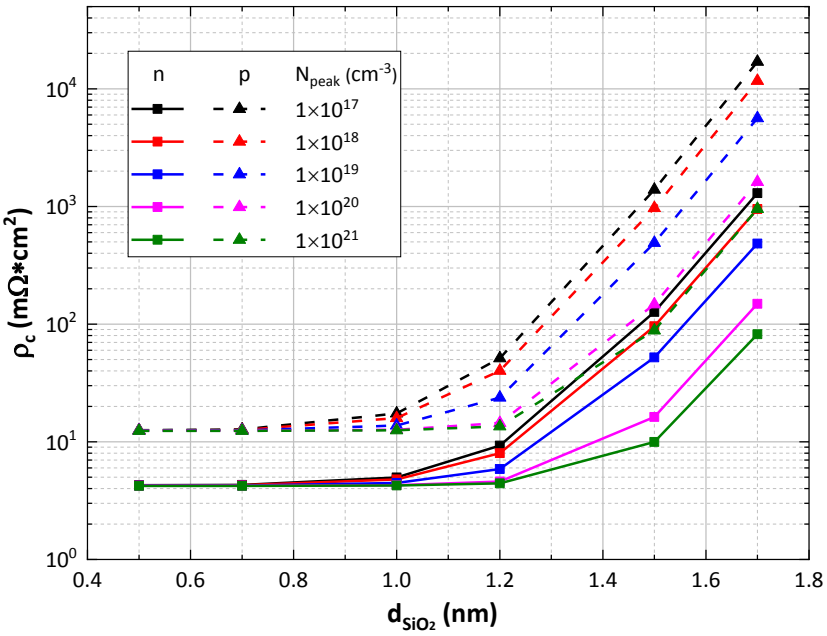

Figure 31 A schematic of the resistivity ρ_c for Metal/poly-Si/SiO_2/c-Si contact stack as function with varying d_{Ox} and N_{peak}, in which the solid lines indicate the n-Contact n-Bulk model and dashed lines indicate p-Contact p-Bulk model

As shown in Figure 31, the resistivity ρ_c increases dramatically when d_{Ox} becomes larger. This is because the carrier need tunnel the interface between poly-Si layer and c-Si bulk. The thicker the SiO_2 layer leads the larger tunneling barrier. The d_{Ox} should keep close to 1 nm to minimize the resistivity. The thinner SiO_2 layer cannot improve the contact dramatically. The N_{peak} should be increased to achieve good band alignment between poly-Si and c-Si so that the low contact resistivity can be obtained.

In addition, the state of band alignment between conduction (valence) band of poly-Si and c-Si in n-type (p-type) model also decide the efficiency of tunneling. In order to observe the band alignment, the band diagram near the poly-Si/c-Si interface is shown in Figure 32. It can be seen that larger N_{peak} can improve the band alignment between c-Si and poly-Si layer, so that the tunneling becomes more efficient and contact resistivity ρ_c can be reduced. It is always preferable to apply higher doping concentration in buried doping region to obtain efficient tunneling.

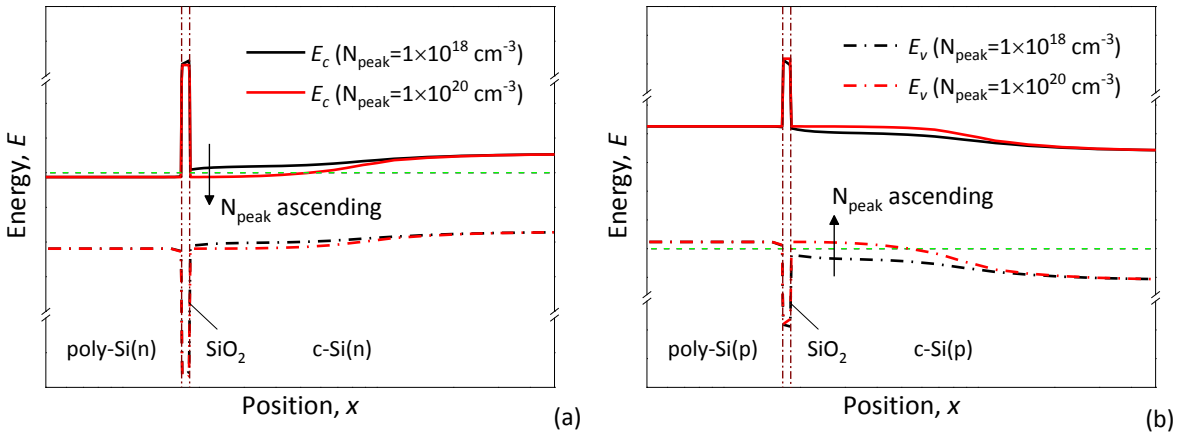

Figure 32 A schematic of the band diagrams for (a) n-Contact n-Bulk model and (b) p-Contact p-Bulk model under condition of d_{Ox}=1.5 nm, N_{poly}=1×10^{20} cm^{-3}, in which black lines indicate the bands for N_{peak}=1×10^{18} cm^{-3} and red lines indicate the bands for N_{peak}=1×10^{20} cm^{-3}

4.3.2 Numerical issues

The I-V plots show linear characteristic in this case. However if the d_{Ox} is larger than 2 nm, potential barrier becomes very thick for carrier to tunnel the SiO_2 layer. Only tiny current can be measured between two contacts through the simulation. This obstruction caused by thick oxide insulator should be avoided in solar cell.

4.4 Band Alignment: N_{peak} and N_{poly}

Except N_{peak} can influence the band alignment as discussed in **Chapter 4, Section 4.3**. The impacts of another factor N_{poly} is studied in this case.

The complete contact stack of Metal/poly-Si/SiO_2/c-Si is modeled in this case. The model structure is shown in Figure 21 (b). The peak doping concentration of buried region N_{peak} is valued as 0, 1×10^{18}, 1×10^{19}, and 1×10^{20} cm^{-3}. The poly-Si doping concentration N_{poly} is valued as 1×10^{18}, 1×10^{19}, 1×10^{20}, and 2×10^{20} cm^{-3}. The other parameters are defined as default value. Contact distance L_d is valued as 10, 20, 40, 80, and 160 μm. 80 sequences for each model should be run in total.

4.4.1 Results

Through same calculation process presented in **Chapter 4, Section 4.2.1**. The resistivity ρ_c as function with varying N_{poly} and N_{peak} are shown in Figure 33.

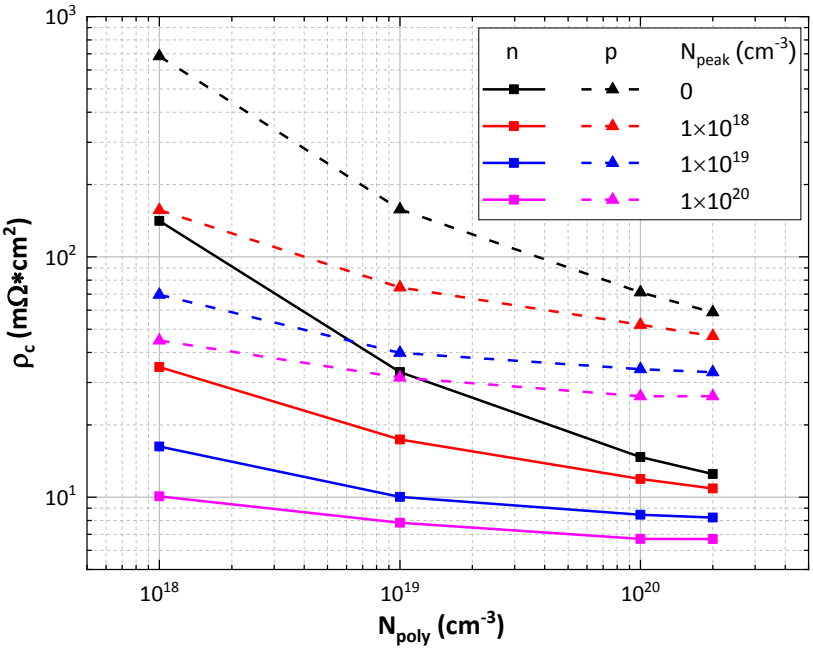

Figure 33 A schematic of the resistivity ρ_c for Metal/poly-Si/SiO_2/c-Si contact stack as function with varying N_{poly} and N_{peak}, in which the solid lines indicate the n-Contact n-Bulk model and dashed lines indicate p-Contact p-Bulk model

As shown in Figure 33, within whole range of N_{poly}, increasing N_{peak} can effectively reduce the contact resistivity ρ_c, and make ρ_c less dependent on N_{poly}. When N_{poly} equals to 1×10^{18} cm^{-3}, the model with N_{peak} of 1×10^{20} cm^{-3} has only one-tenth of ρ_c for the model without buried doping. The reason has been presented in previous chapter.

Increasing N_{poly} can also reduce the contact resistivity ρ_c. This is because the potential barrier for carrier transport is reduced, so that the poly-Si layer becomes more conductive. In addition, high N_{poly} accompanied with appropriate buried doping can improve the band alignment at the interface, which leads the highly efficient tunneling, so that the low resistivity ρ_c can be obtained.

4.4.2 Numerical issues

All simulation sequences converged well in this case. This is due to the proper doping in poly-Si layer and thickness of SiO_2 layer (d_{Ox} = 1.5 nm). The lack of buried doping cannot totally change the contact characteristic, so that I-V data can be linearly fitted in good quality.

4.5 Potential barrier size and doping inside poly-Si: d_{Ox} and N_{poly}

The complete contact stack of Metal/poly-Si/SiO_2/c-Si is modeled in this case. The model structure is shown in Figure 21 (b). The poly-Si doping concentration N_{poly} is valued as 5×10^{17}, 1×10^{18}, 5×10^{18}, 2×10^{19}, 5×10^{19}, 1×10^{20}, and 2×10^{20} cm^{-3}. The buried doping region is applied and the peak doping concentration N_{peak} is set same with N_{poly}. The thickness of SiO_2 d_{Ox} is valued as 0.5, 0.7, 1, 1.2, 1.5 and 1.7 nm. The other parameters are defined as default value. Contact distance L_d is valued as 10, 20, 40, 80, and 160 μm. 210 sequences for each model should be run in total.

4.5.1 Calculation and results

In previous chapters, it is proved that the buried doping supports low values for contact resistivity. In this case, the resistivity ρ_c is studied as the function with varying d_{Ox} and N_{poly}.

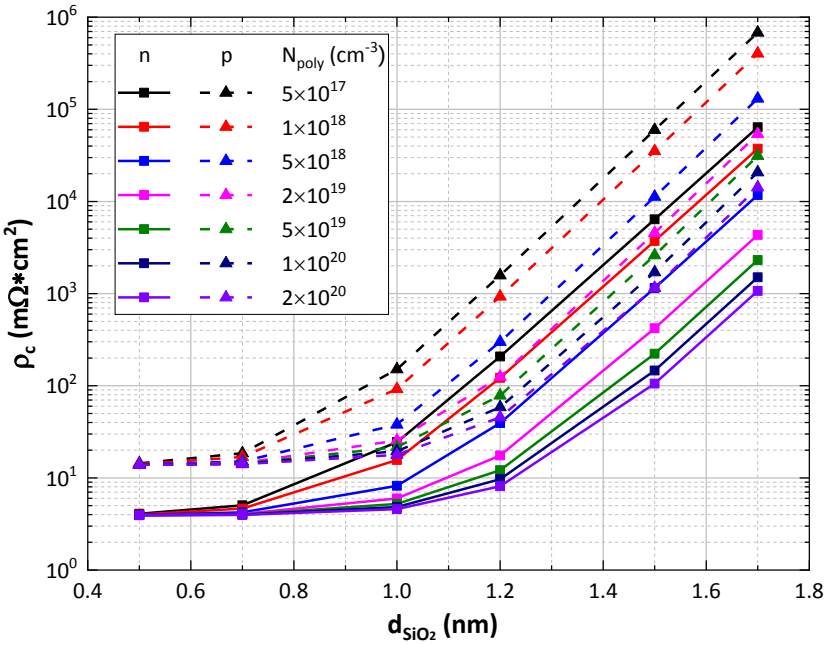

Figure 34 A schematic of the resistivity ρ_c for Metal/poly-Si/SiO_2/c-Si contact stack as function with varying N_{poly} and d_{Ox}, in which the solid lines indicate the n-Contact n-Bulk model and dashed lines indicate p-Contact p-Bulk model

As shown in Figure 34, ρ_c trends larger with increasing d_{Ox} and decreasing N_{poly}. It is presented that d_{Ox} has more impact on ρ_c. When d_{Ox} is increased by 1 nm from 0.7 nm, the contact resistivity ρ_c is increased by nearly 5 orders of magnitude. On the contrary, the impact of varying N_{poly} is relatively gentle.

In summary, thickness of SiO_2 layer d_{Ox} is the dominant parameter to determine the resistivity ρ_c of Metal/poly-Si/SiO_2/c-Si contact stack. However, the contact is more resilient to SiO_2 thickness degradation in the presence of a diffused doping profile

inside c-Si side as Figure 34 illustrates.

4.5.2 Numerical issues

The worst numerical issue is due to the maximal d_{Ox} of 1.7 nm. The high tunneling barrier of SiO_2 makes the contact show nonlinear I-V characteristic. The total resistance R_t cannot be accurately calculated through one-dimensional polynomial function curve fitting. And the R_t - L_d data also cannot be fitted by TLM method well. Although the precise resistivity ρ_c is not obtained under this condition, the general ρ_c trends keep accordance with the condition of low d_{Ox} ranged from 0.7 to 1.5 nm.

5 Silicon Heterojunction Based Carrier Selective Contacts

In case of SHJ based CSCs, the effect of band alignment and energy barrier on contact resistance is investigated. Therefore, as suggested in [64], the resistivity of SHJ based contact stack is studied with varying TCO carrier concentration N_{TCO}, band gap energy of doped layer E_g, activation energy of doped layer E_a, thickness of intrinsic a-Si layer $d_{a\text{-}Si(i)}$.

5.1 TCO/Metal interface

The model used for this case is shown in Figure 24 (a). The TCO and doped layers are connected between contacts. The current can flow through the TCO layer. The parameters and physics models are defined in Table 2. Except the TCO carrier concentration N_{TCO} is valued as 1×10^{19}, 5×10^{19}, 1×10^{20}, 5×10^{20}, and 1×10^{21} cm^{-3}, the other parameters are defined as default value. Contact distance L_d is valued as 10, 50, 100, 200, and 400 μm. The simulation process has 25 sequences in total. Four kinds of model are involved: n-Contact n-Bulk, n-Contact p-Bulk, p-Contact n-Bulk, and p-Contact p-Bulk.

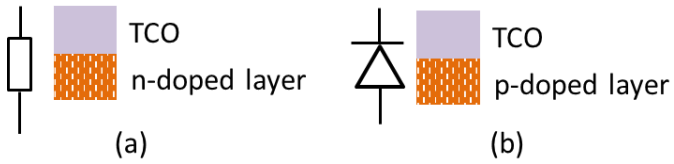

Figure 35 A schematic of the feature of TCO/doped-layer interface

As shown in Figure 35 (a), for n-Contact n-Bulk and n-Contact p-Bulk models, the TCO/doped-layer interface show the feature as resistor. The current can cross the TCO/doped-layer interface and transfer through both TCO and doped layer. The contact resistance obtained by TLM method is from both TCO/Metal interface and TCO/doped-layer interface.

As shown in Figure 35 (b), for n-Contact n-Bulk and n-Contact p-Bulk models, the TCO/doped-layer interface show the feature as diodes that are in opposite directions at two contacts. The current can hardly cross the TCO/doped-layer interface and mainly flow through TCO layer. The contact resistance obtained by TLM method is mainly from bTCO/Metal interface.

5.1.1 Results

The calculation process of n-Contact n-Bulk model is taken for example. In order to show the clear current-voltage plot, only the I-V curves for N_{TCO} = 1×10^{20} cm^{-3} are sketched in Figure 36.

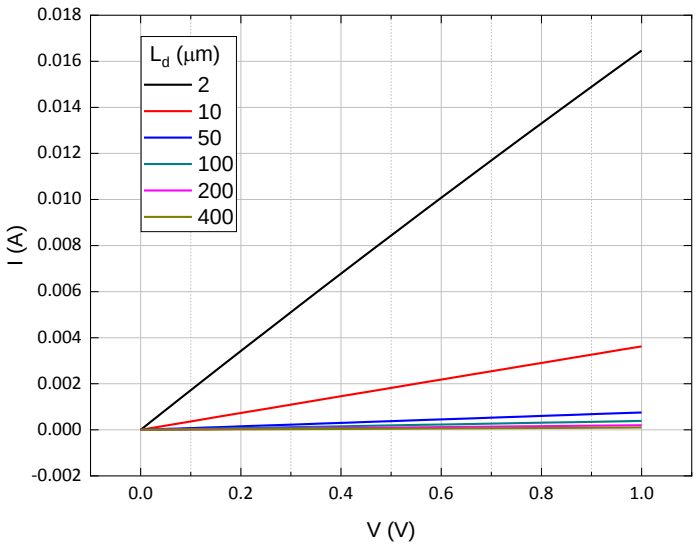

Figure 36 A schematic of I-V curves for N_{TCO} = 1×10^{20} cm^{-3} of n-Contact n-Bulk model, in which the curves for contact distance ranged from 2 to 400 μm are indicated

As shown in Figure 36, the larger contact distance leads the larger resistance between two contacts, which make the slope of I-V curve smaller. Through fitting the I-V data with one-dimensional polynomial function, the value of slope can be obtained. The total resistance R_t between two contacts with different contact distance L_d can be calculated then.

$$WR_t = 1/slope \qquad (5\text{-}1)$$

The R_t – L_d curves can be plotted in Figure 37.

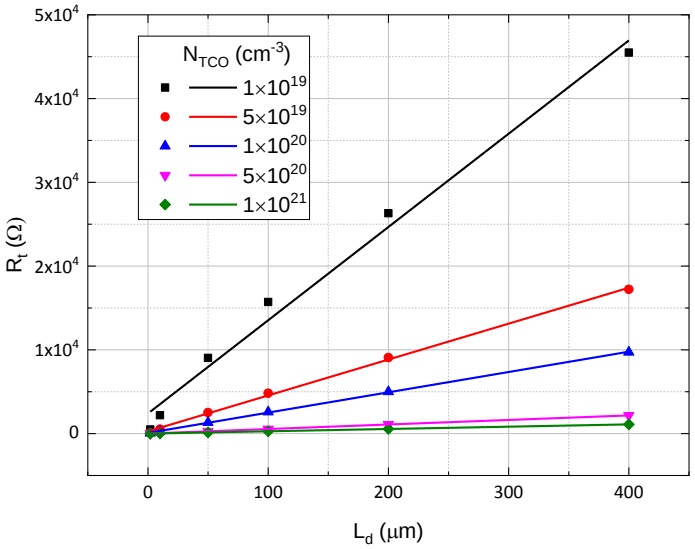

Figure 37 A schematic of R_t – L_d curves for n-Contact n-Bulk model, in which the curves for TCO carrier concentration N_{TCO} ranged from 1×10^{19} to $1\times10^{21}cm^{-3}$are indicated, where scatters indicate the total resistance R_t and solid lines indicate the linear fitting curves R_t - L_d

As shown in Figure 37, the scattering R_t data are fitted with one-dimensional polynomial function. Through the TLM method presented in **Chapter 2, Section 2.3**, the resistivity for Metal/TCO contact stack can be obtained from the fitting curves. The calculation process for n-Contact p-Bulk, p-Contact n-Bulk, and p-Contact p-Bulk models is same. The final results are presented in Figure 38.

It can be seen in Figure 38 that the general trend of contact resistivity ρ_c is decreasing when increasing the TCO carrier concentration N_{TCO}. When N_{TCO} is increased, the work function of TCO will increase, which makes TCO layer more conductive and leads lower resistivity. Since the TCO layer is connected and has much lower resistivity than other layers, most current will transfer through TCO layer, which makes the contact resistivity for different doped model is quite close. The contact resistivity is mainly decided by N_{TCO}. In order to obtain high efficiency of solar cell, TCO with large carrier concentration should be selected.

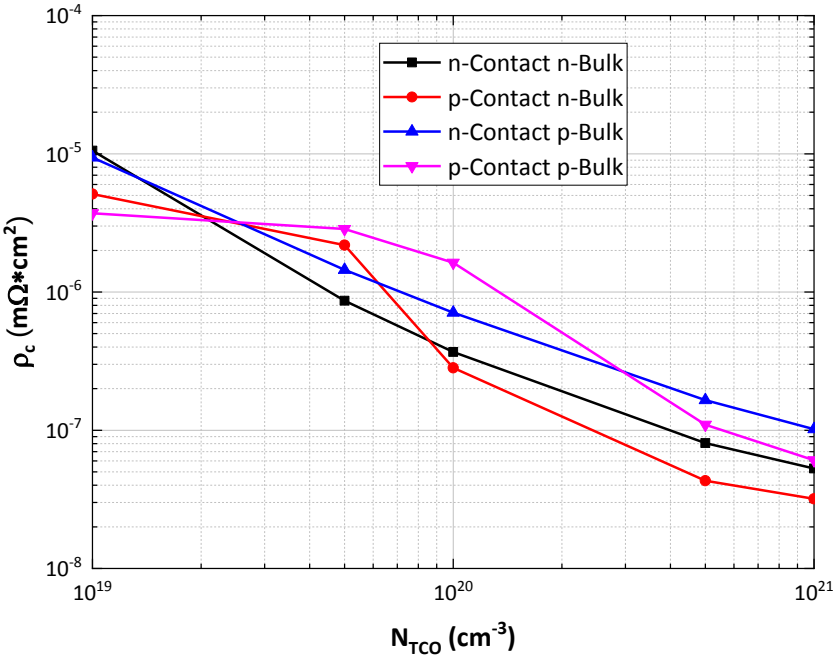

Figure 38 A schematic of the resistivity ρ_c for Metal/TCO contact stack function with varying N_{TCO}, in which the ρ_C - N_{TCO} curves for model with different doping types are indicated

5.1.2 Numerical issues

For common TLM method, the contact distance L_d is valued from 10 to 400 µm. Since the resistance of Metal/TCO contact stack is very small in condition with high N_{TCO}, the fitted R_t – L_d curve may intersect with Y axis very close to zero. In order to obtain the tiny intercept accurately, the smaller contact distance of 2 µm is considered additionally in modeling. It can be seen in Figure 37 that the range of L_d is from 2 to 400 µm.

5.2 Band Alignment and potential barrier: E_a and N_{TCO}

In this case, both activation energy E_a of doped layer and TCO carrier concentration N_{TCO} are varied to study their impact on contact stack resistivity. The activation energy E_a of doped layer depends on doping concentration $N_{a\text{-}Si}$ differently by n-type and p-type. The parameters and physics models are defined in Table 2.The relation between E_a and $N_{a\text{-}Si}$ is shown in Table 3.

The complete contact stack of Metal/TCO/doped-layer/ i-a-Si:H/c-Si is simulated by n-Contact n-Bulk and p-Contact p-Bulk models to avoid reversed diodes effect at contact/bulk interface.

The partial contact stack of Metal/TCO/doped-layer will be simulated respectively is simulated by n-Contact p-Bulk and p-Contact n-Bulk models to impede current across the doped-layer/c-Si interface.

Table 3 The relation between activation E_a and doping concentration $N_{a\text{-}Si}$

n-type		p-type	
$N_{a\text{-}Si}$ (cm^{-3})	E_a (meV)	$N_{a\text{-}Si}$ (cm^{-3})	E_a (meV)
7×10^{19}	350	5×10^{19}	400
7.2×10^{19}	300	6×10^{19}	320
7.5×10^{19}	220	7×10^{19}	270
8×10^{19}	180	8×10^{19}	230
1×10^{20}	110	1×10^{20}	170
2×10^{20}	53	1.5×10^{20}	90
2.5×10^{20}	18	2×10^{20}	53

5.2.1 Complete contact stack of Metal/TCO/doped-a-Si/i-a-Si:H/c-Si

The model structure is shown in Figure 24 (c). N_{TCO} is valued as 1×10^{19}, 2×10^{19}, 5×10^{19}, 1×10^{20}, 5×10^{20}, and 1×10^{21} cm^{-3}. E_a is valued as 350, 300, 220, 180, 110, 18 meV for n-type doped layer and 400, 320, 270, 230, 170, 90, 53 meV for p-type doped layer. L_d is valued as 10, 50, 100, 200, 400 μm. In total, 180 simulation sequences should be run for n-type model, and 210 simulation sequences for p-type.

The calculation process includes *I-V* curve fitting, R_t - L_d curve fitting, ρ_c calculation, which are discussed in **Chapter 2, Section 2.3**. After the calculation, the resistivity of contact stack can be obtained. The final results are shown in Figure 39.

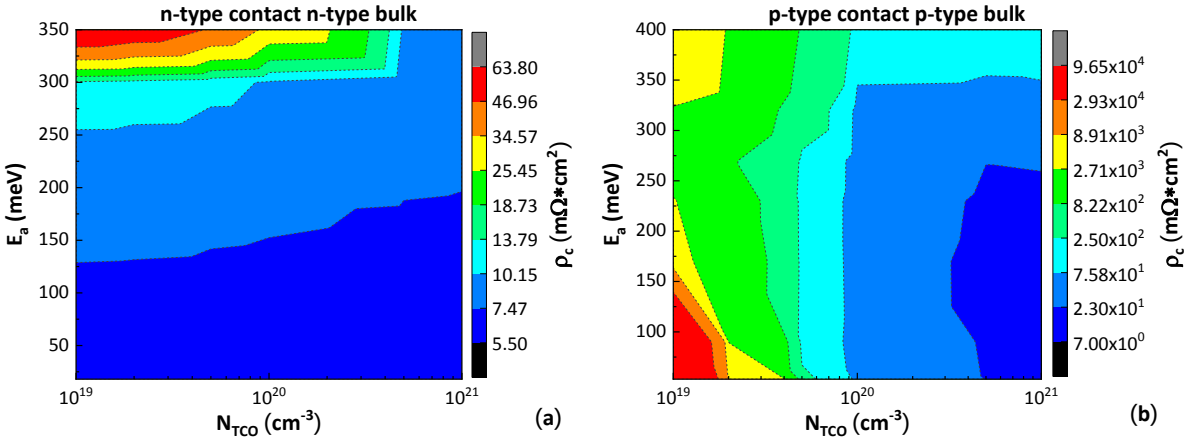

Figure 39 The contour plots of ρ_c as function with varying E_a and N_{TCO} for (a) n-Contact n-Bulk and (b) p-Contact p-Bulk model with complete contact stack

As shown in Figure 39 (a), for n-type model, the contact resistivity ρ_c becomes larger with lower N_{TCO} and higher E_a. When E_a is larger than 300 meV, ρ_c is clearly dependent on N_{TCO}. It can be seen in Figure 40 (a) that increasing N_{TCO} can make the conduction band of TCO layer have better alignment with conduction band of doped layer, which improves the band-to-band tunnelling at TCO/a-Si interface. When E_a is smaller than 300 meV, the potential barrier for carrier transport is

minimized and no longer dependent on N_{TCO}.

As shown in Figure 39 (b), for p-type model, the carrier transport dependency on N_{TCO} is same with n-type model. The large N_{TCO} make the conduction band of TCO layer have better alignment with valence band of doped layer. It can be seen in Figure 40 (b) that when N_{TCO} is larger than 1×10^{20} cm^{-3}, the band alignment is sufficient for band-to-band tunnelling to take effect. The carrier can efficiently tunnel the TCO/a-Si interface. When N_{TCO} is smaller than 1×10^{20} cm^{-3}, the band alignment is insufficient for band-to-band tunnelling. The trap-assisted tunnelling (TAT) is dominant in this condition. The carrier transport depends on the trap state density in doped layer. The I-V characteristic is no longer linear in this N_{TCO} range. The trap state is hard to measure during practical experiment. Although high trap density can improve TAT, it will also lead high recombination rate, which should be avoided in solar cell device.

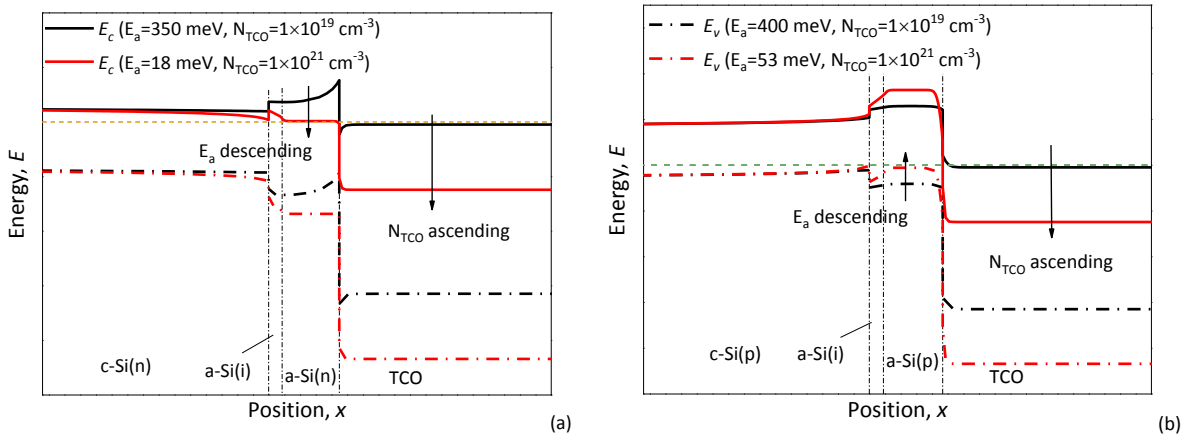

Figure 40 A schematic of the band diagrams for (a) n-Contact n-Bulk model and (b) p-Contact p-Bulk model, in which the models with maximal and minimal E_a and N_{TCO} are indicated

The ρ_c data within N_{TCO} ranged from 1×10^{19} to 1×10^{21} cm^{-3} are shown in Figure 41. It can be seen that ρ_c is more dependent on N_{TCO}. When E_a is smaller than 200 meV, the contact resistivity achieves its minimum for both n-type and p-type model. For n-type model, it is preferable to make N_{TCO} reach 5×10^{20} cm^{-3}, but further increase cannot reduce contact resistivity efficiently. For p-type model, N_{TCO} should keep larger than 1×10^{20} cm^{-3} to avoid TAT dominating.

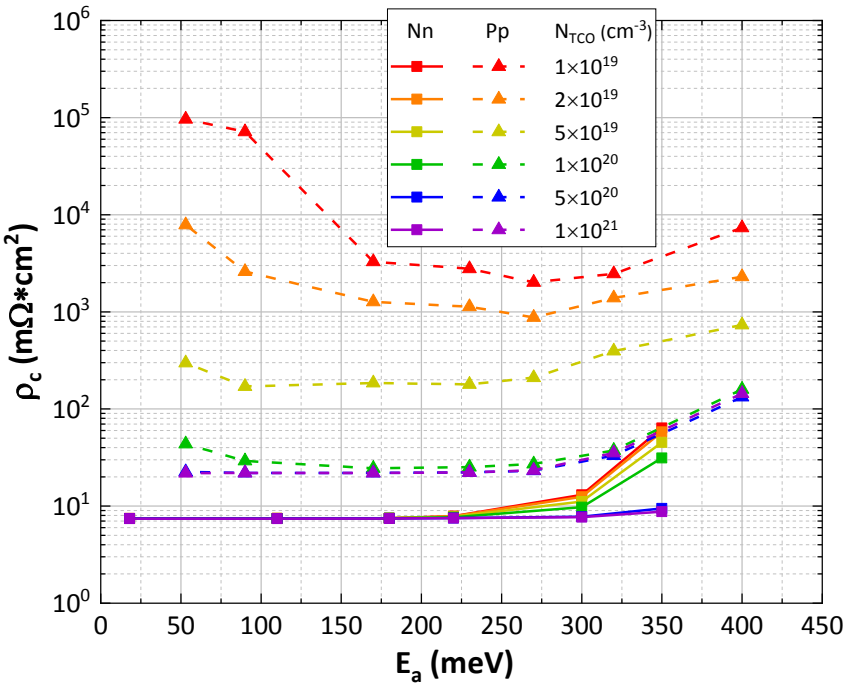

Figure 41 A schematic of the contact resistivity ρ_c as function with vary N_{TCO} and E_a for n-Contact n-Bulk and p-Contact p-Bulk model

5.2.2 Partial contact stack of Metal/TCO/doped-layer

The model structure is shown in Figure 24 (b). N_{TCO} is valued as 1×10^{19}, 2×10^{19}, 5×10^{19}, 1×10^{20}, 5×10^{20}, and 1×10^{21} cm^{-3}. E_a is valued as 350, 300, 220, 180, 110, 35, 18 meV for n-type doped layer and 400, 320, 270, 230, 170, 90, 53 meV for p-type doped layer. L_d is valued as 10, 50, 100, 200, 400 μm. In total, 210 simulation sequences should be run for each model respectively.

The similar contour plots Figure 42 decribes the contact resistivity ρ_c as function with varying E_a and N_{TCO}. E_a and N_{TCO} cause same impacts on ρ_c as discussed before.

The ρ_c data within N_{TCO} ranged from 1×10^{19} to 1×10^{21} cm^{-3} are shown in Figure 43. It can be seen that for n-Contact, the TCO and doped-layer with their interface contribution to the resistivity of complete contact stacks increases with the increasing E_a. This is because the potential barrier in doped layer becomes larger with higher E_a, and the tunneling barrier becomes larger at TCO/doped layer interface due to the inefficient band alignment. For p-Contact, apart from TAT dominated region due to low N_{TCO}, the TCO and doped-layer with their interface contributes most resistivity of complete stack. This is due to the potential barrier for holes transport in doped layer is larger than electrons.

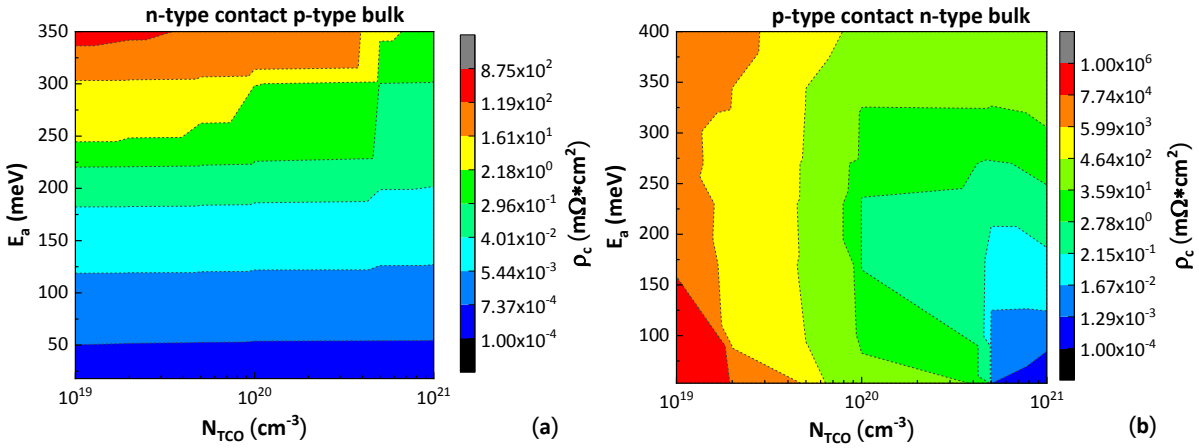

Figure 42 The contour plots of ρ_c as function with varying E_a and N_{TCO} for (a) n-Contact p-Bulk and (b) p-Contact n-Bulk model with partial contact stack

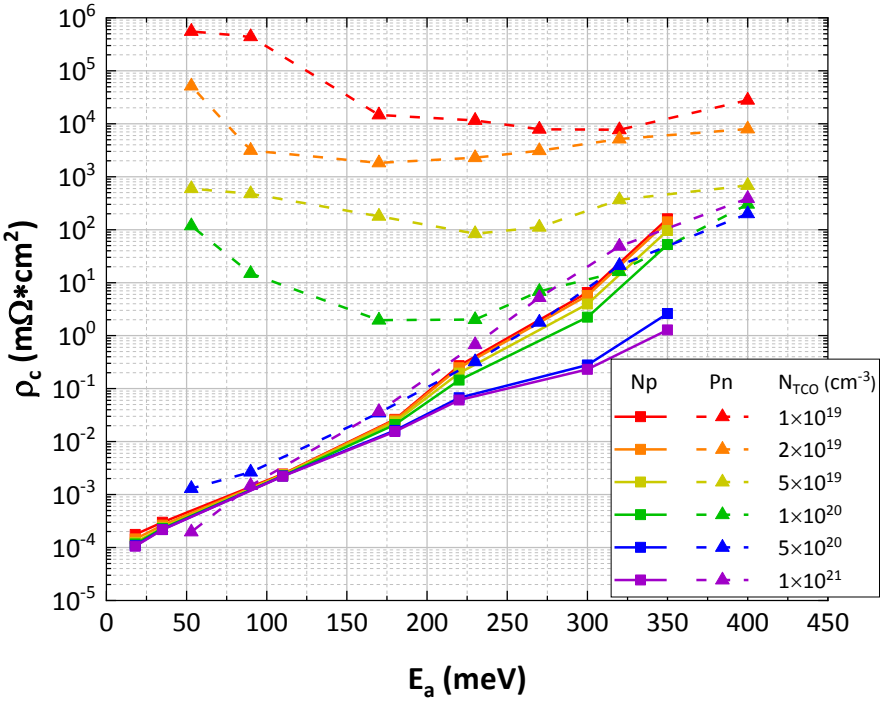

Figure 43 A schematic of the contact resistivity ρ_c as function with vary N_{TCO} and E_a for n-Contact p-Bulk and p-Contact n-Bulk model

Through comparing the resistivity ρ_c from partial contact stack Metal/TCO/doped-layer and complete contact stack Metal/TCO/doped-layer/ i-a-Si:H/c-Si, the resistivity contribution of doped layer, TCO and their interface can be obtained. The Metal/TCO interface resistivity is very small, shown in Figure 38, so that the contribution in total resistivity is negligible. The partial resistivity and complete resistivity for n-Contact are shown in Figure 44.

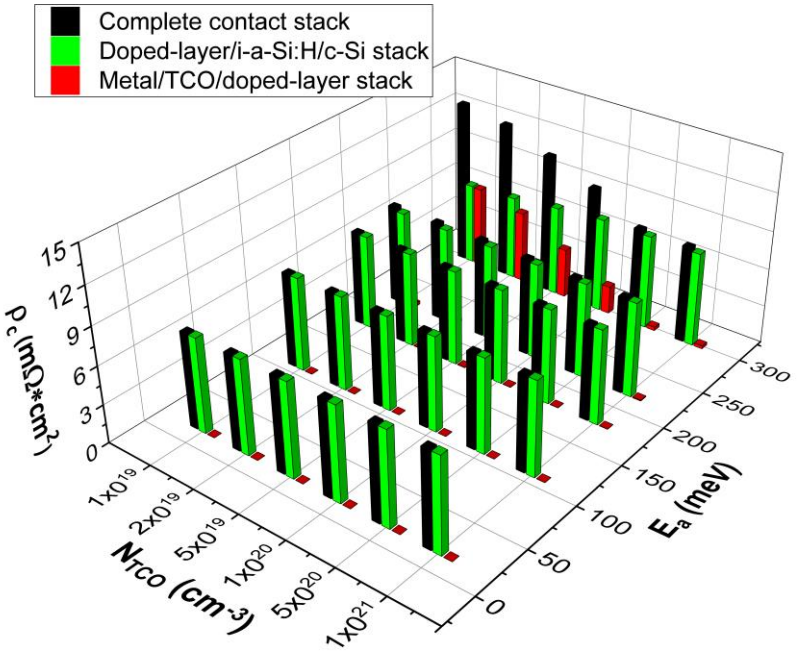

Figure 44 A schematic of the complete and partial contact resistivity ρ_c as function with vary N_{TCO} and E_a for n-Contact model, in which the resistivity of complete contact stack, doped-layer/i-a-Si:H/c-Si stack, and metal/TCO/doped-layer stack are indicated in different colors.

It can be seen in Figure 44 that when E_a is smaller than 180 meV, the partial resistivity for metal/TCO/doped-layer stack is nearly zero, which means the contact resistivity in condition of low activation is mainly from i-a-Si:H layer and the interface between c-Si bulk and doped layer. This is because the potential barrier for carrier transport is very small, and the low band offset between conduction band in doped layer and TCO is beneficial to tunneling. When E_a is larger than 180 meV, the partial resistivity for metal/TCO/doped-layer stack increases with growing E_a, and raises more dramatically in condition of lower N_{TCO}. This is because the band alignment between doped layer and TCO affects the tunneling efficiency. When N_{TCO} is smaller than 1×10^{20} cm^{-3}, the band alignment is not so efficient that a small increment in E_a can results in a large raise of tunneling barrier. The situation of p-Contact model will be discussed in next section.

5.2.3 Numerical issues

In this case, a lot of simulation sequences under the conditions with high E_a and low N_{TCO} encounter convergence problem. The bad band alignment and larger potential barrier for carrier transport lead complex numerical problems. Some sequences cannot finish the whole iteration to reach the contact voltage of 1 V. Some sequences obtain nonlinear I-V data due to the TAT dominated condition. In order to show the ρ_c trends when N_{TCO} is under 1×10^{20} cm^{-3}, or E_a is over 300 meV. The I-V curve fitting only use the most linear part, as shown in Figure 45, of all data points to calculate the total resistance R_t.

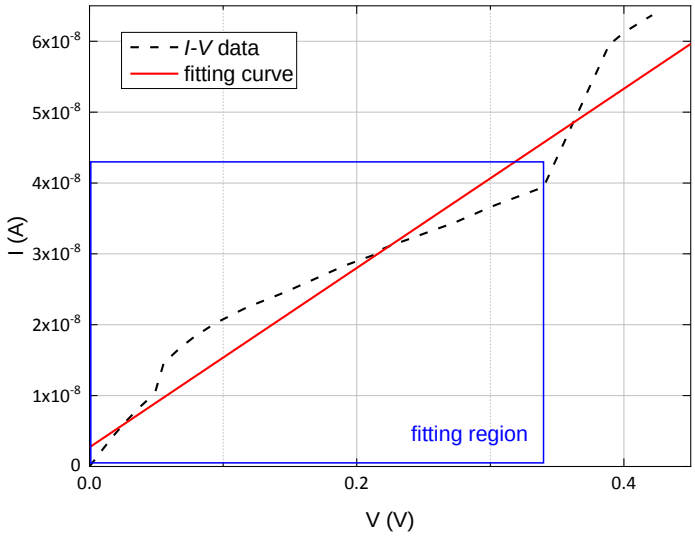

Figure 45 A schematic of I-V curve for unfinished sequence, in which the fitting region is indicated by blue rectangle

Especially in p-Contact model, the domination of TAT under the conditions with high E_a and low N_{TCO} not only causes convergence problem, but also leads exaggerated partial resistivity for Metal/TCO/doped-layer stack shown in Figure 46. The partial resistivity can exceed complete stack resistivity in conditions of $N_{TCO} < 1\times10^{20}$ cm^{-3} or $E_a > 320$ meV. TLM cannot obtain accurate contact resistivity in this condition. The reason has been discussed in **Chapter 2 Section 2.3**.

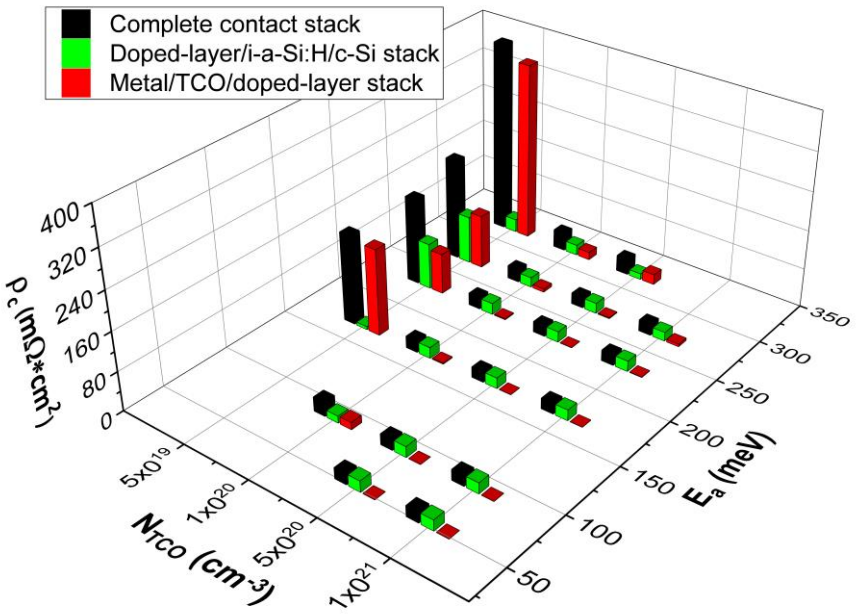

Figure 46 A schematic of the complete and partial contact resistivity ρ_c as function with vary N_{TCO} and E_a for p-Contact model, in which the resistivity of complete contact stack, doped-layer/i-a-Si:H/c-Si stack, and metal/TCO/doped-layer stack are indicated in different colors.

5.3 Band alignment: E_g of doped layer

The model used in this case is shown in Figure 24 (b). Since doped layer contains huge amount of traps, the thickness of doped layer is set as 100 nm to promote the carrier transport. In this case, only the band gap energy E_g of doped layer is changed and the electron affinity keeps constant. The position of conduction band of doped layer keeps same and only the position of valance band changes. For n-type doped layer the carrier transport is mainly determined by conduction band, so the varying E_g will not affect the potential barrier. Therefore only p-Contact n-Bulk and p-Contact p-Bulk models are considered in this case. The range of E_g is from 1.5 to 1.8 eV. 20 sequences for each model should be run.

5.3.1 Calculation and results

As shown in Figure 47, the varying E_g changes the position of valence band in doped layer. The holes transport is affected by band offset.

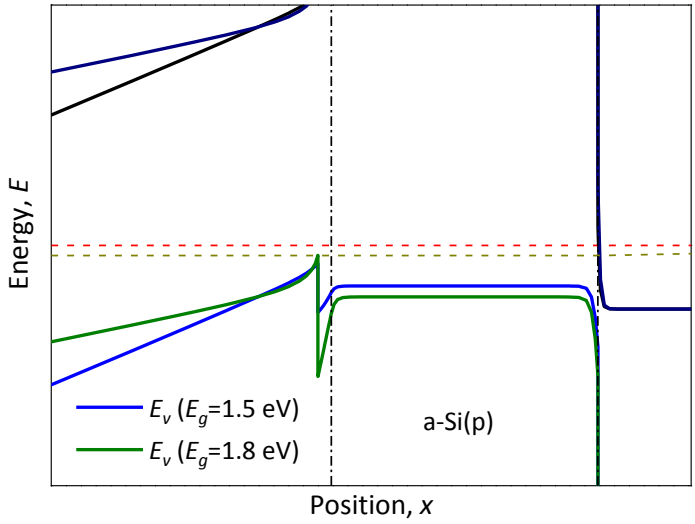

Figure 47 A schematic of valence band of p-Contact n-Bulk model with E_g equal to 1.5 and 1.8 eV respectively

Through I-V data obtained from TLM simulation. The R_t – L_d curves can be obtained, which of p-Contact n-Bulk model are shown in Figure 48.

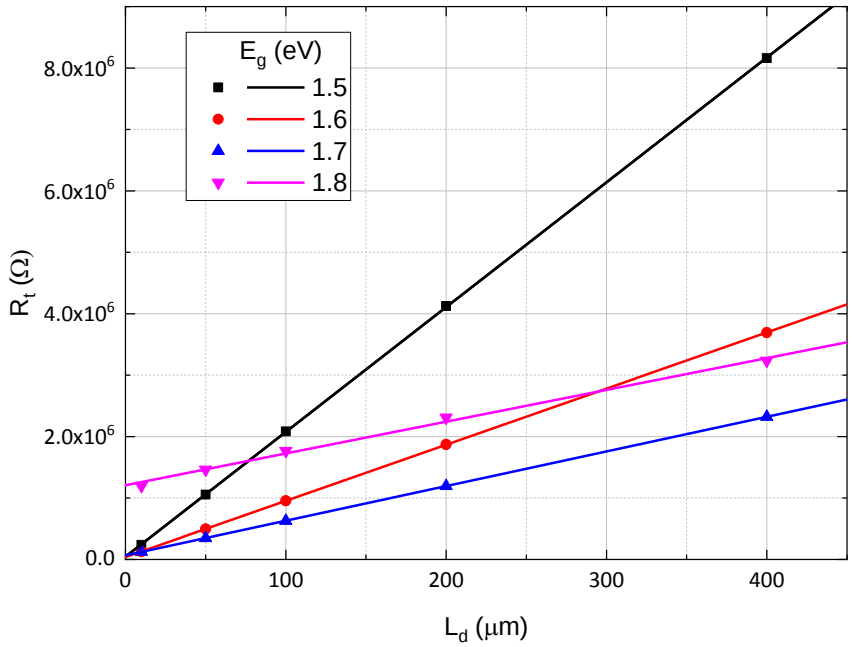

Figure 48 A schematic of R_t – L_d curves for n-Contact p-Bulk model, in which the curves for E_g ranged from 1.5 to 1.8 eV are indicated, where scatters indicate the total resistance R_t and solid lines indicate the linear fitting curves R_t - L_d

As shown in Figure 48, when E_g increases, the slope of curve decreases and the intercept of curve increases. This is because the potential barrier of doped layer becomes higher, which increases the contact resistance R_c and makes the contribution of semiconductor sheet resistance R_s lower.

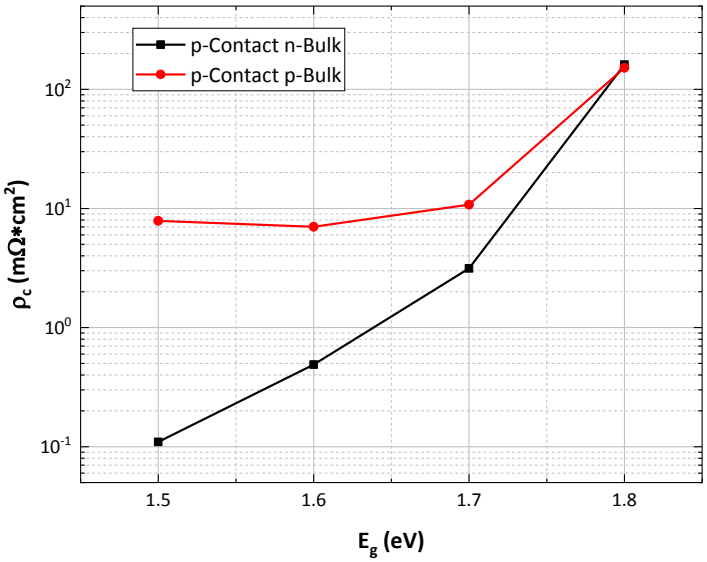

Figure 49 A schematic of the resistivity ρ_c as function with vary E_g for p-Contact n-Bulk and p-Contact p-Bulk model

Through the curve fitting, the resistivity can be obtained. The results are shown in Figure 49. When E_g increases and electron affinity keeps constant, the valence band

become lower, so that the potential barrier for holes transport becomes larger. The contact resistivity will increase with larger band gap energy.

5.3.2 Multiple doped layers

As suggested in [65], larger band gap energy E_g is recommended to improve the band alignment between doped layer and c-Si bulk like Figure 50 illustrates. However large E_g also leads high contact resistivity as shown in Figure 49.

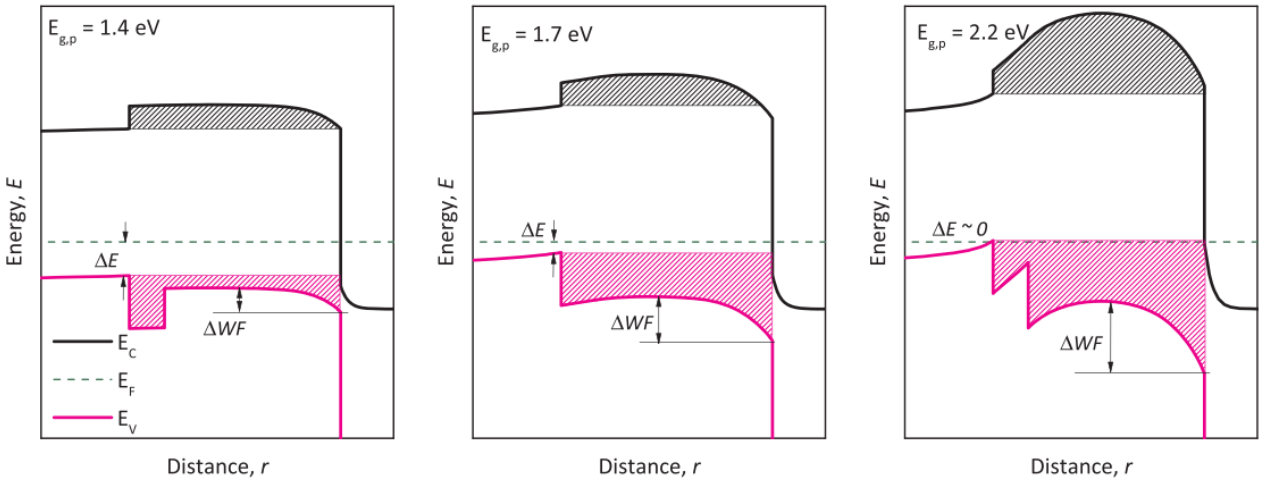

Figure 50 Band diagrams at equilibrium of p-type contact stack for different bandgap of p-type layer. In these cases, $E_{a,p}$ = 400 meV, WF_{TCO} = 4.7 eV and $d_{i/p}$ = 25 nm. Patterned areas indicate energy barriers for electrons (conduction band) and holes (valence band). ΔE is related to the band bending at the c-Si interface. ΔWF indicates work-function mismatch at the p-type layer/TCO interface. Increasing $E_{g,p}$ increases band bending at c-Si interface but also ΔWF.[65]

In order to reduce the high contact resistivity due to large band gap of doped layer, an alternative contact stack is considered. The structure is shown in Figure 51. In this model, the doped layer I is p-type doped with low concentration of 5×10^{19} cm^{-3}. The activation energy is around 400 meV. The doped layer II is p-type doped with high concentration of 2×10^{20} cm^{-3}. The activation energy is around 50 meV. Their band gap energy are indicated by $E_{g,I}$ and $E_{g,II}$.

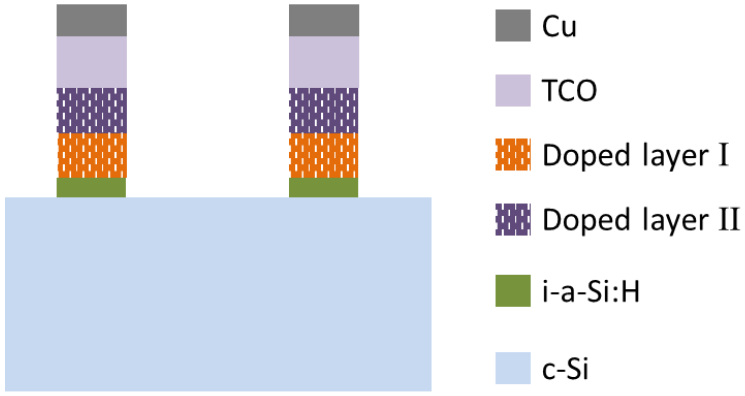

Figure 51 A schematic of the model structure containing multiple doped layers

In first test, the band gap energy of two layers is set as same. They both vary from 1.5 to 2.3 eV. In second test, the band gap energy of layer II $E_{g,II}$ is set as constant. Only $E_{g,I}$ varies from 1.5 to 2.3 eV. When it achieves low band gap, the material is close to nano-crystalline Si. The trends of contact resistivity can be obtained through TLM simulation.

The results are shown in Figure 52. It can be seen that the contact resistivity for Test II is lower than Test I. It means that if a high band gap layer is required in contact stack, the resistivity can be reduced by replace this layer with one high band gap layer and one low band gap layer to make the trade-off.

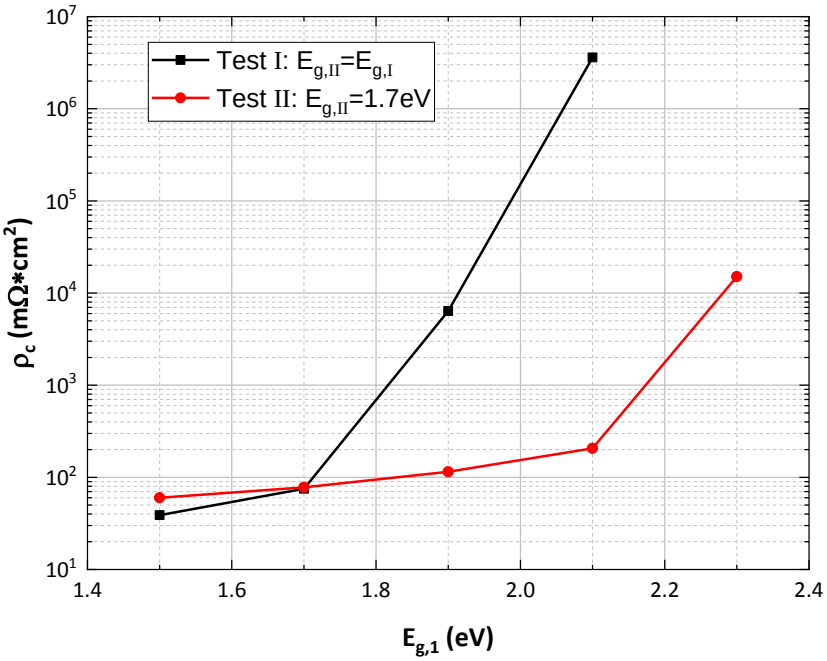

Figure 52 A schematic of the resistivity ρ_c as function with vary E_g for multiple doped layer model

5.3.3 Numerical issues

Convergence problems often happen when running the simulation. If the iteration process cannot converge, the sequence will abort at the last computing point. For the sequences not converged, the varying range of contact voltage cannot reach 1 V. The simulation results for p-Contact n-Bulk model with E_g of 1.8 eV are taken as example, shown in Figure 53. Although the whole process is not finished, I-V data points are still enough for linear curve fitting. It can be seen that the total resistance trends larger when contact distance increases.

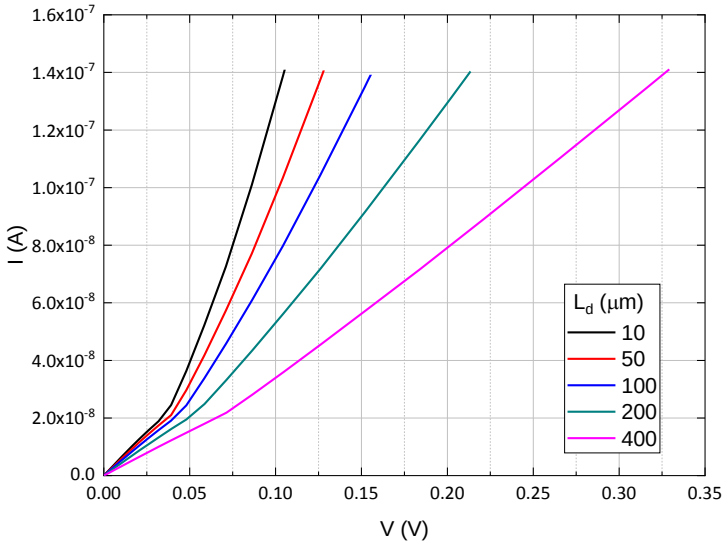

Figure 53 A schematic of I-V curves for aborted simulation sequence with E_g=1.8 eV

5.4 Passivating layer thickness: $d_{a\text{-}Si(i)}$

The model used for this case is shown in Figure 24 (c). The contact stack has complete structure Metal/TCO/doped-layer/i-a-Si:H/c-Si. Two kinds of doping model are considered in this case: n-Contact n-Bulk and p-Contact p-Bulk. The parameters and physics models are defined in Table 2. Except the thickness of i-a-Si:H layer $d_{a\text{-}Si(i)}$ is valued as 1, 5, 10, 15, and 20 nm. Contact distance L_d is valued as 50, 100, 200, and 400 μm. The simulation process has 20 sequences for each model in total.

5.4.1 Results

Through the I-V data obtained from simulation, the total resistance R_t can be calculated by liner curve fitting. The fitting curves for 1 and 20 nm are shown in Figure 54. It can be seen that the varying $d_{a\text{-}Si(i)}$ cause little impact on R_t for n-Contact n-Bulk model. On the contrary, the larger $d_{a\text{-}Si(i)}$ can lead very high resistance.

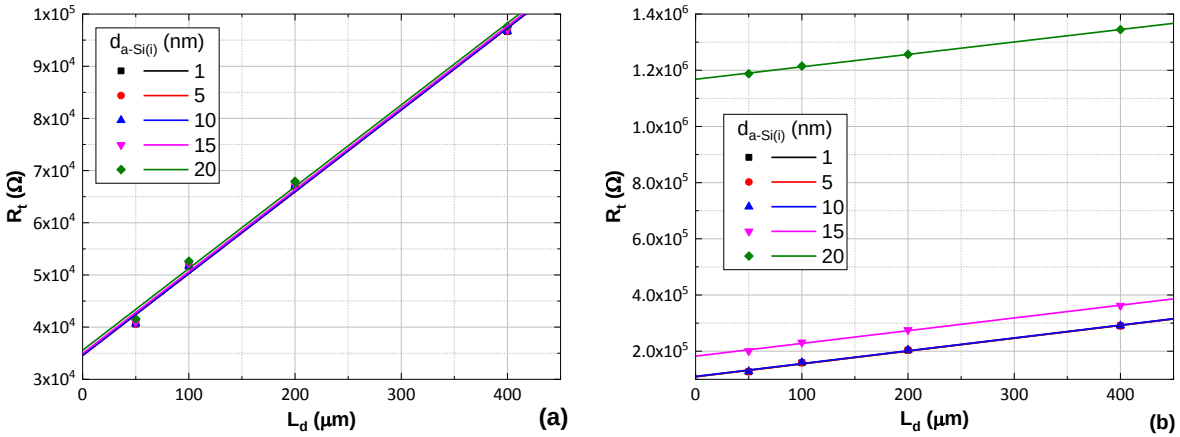

Figure 54 A schematic of R_t – L_d curves for (a) n-Contact n-Bulk and (b) p-Contact p-Bulk model, in which the curves for $d_{a\text{-}Si(i)}$ ranged from 1 to 20 nm are indicated, where scatters indicate the total

resistance R_t and solid lines indicate the linear fitting curves R_t - L_d

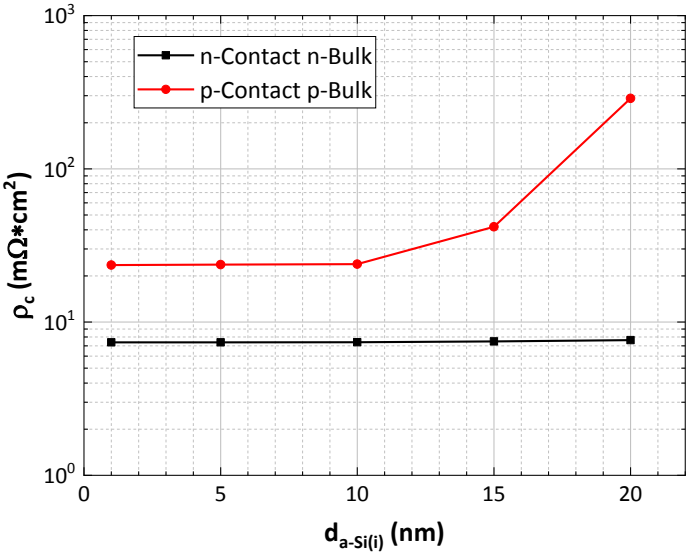

Figure 55 A schematic of the resistivity ρ_c as function with vary $d_{a\text{-}Si(i)}$ for n-Contact n-Bulk and p-Contact p-Bulk model

The resistivity of contact stack can be obtained through fitted R_t – L_d curves. The results are shown in Figure 55. It can be seen that the contact resistivity is more sensitive to $d_{a\text{-}Si(i)}$ in p-Contact p-Bulk model. The preferable decision is to keep the thickness of intrinsic a-Si layer $d_{a\text{-}Si(i)}$ under 10 nm for p-type wafer.

5.4.2 Numerical issues

For p-Contact p-Bulk model, if $d_{a\text{-}Si(i)}$ is over 15 nm, the tunneling barrier for carrier across the layer will be very large. The contact built in this condition cannot work efficiently due to the high resistivity. The I-V data will show nonlinear characteristic like Figure 56 illustrates. In this case, only the I-V data ranged from 0 to 0.3 V are used for linear curve fitting to obtain the resistance between two contact stacks. Although this resistance cannot show the electrical performance for whole voltage range, it is still meaningful to study the resistivity trends within high $d_{a\text{-}Si(i)}$ range.

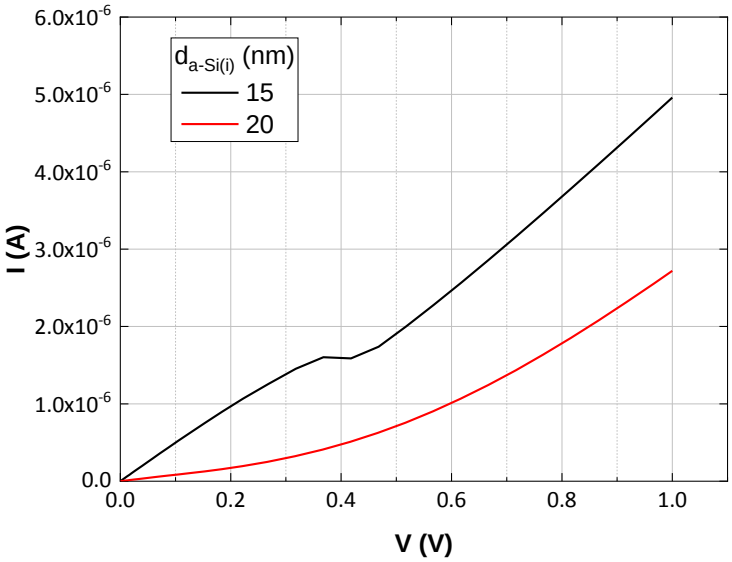

Figure 56 A schematic of I-V curves for $d_{a\text{-}Si(i)}$ equals to 15 and 20 nm

6 Conclusion

In this thesis, the contact resistivity in high efficiency solar cell featuring carrier-selective contacts (CSCs) is investigated on the basis of TCAD Sentaurus. To do so, the transmission line measurement (TLM) process is modelled. Then, a validation process is successfully carried out based on comparison of measured and simulated data from a reference poly-Si CSC. Accordingly, the simulation platform is used to address the research questions proposed in **Chapter 2, Section 2.4**.

a) *What factors determine the resistivity of carrier selective contacts stack and how they affect the such value?*

The resistivity of CSCs is mainly determined by potential barrier size and band alignment. Therefore, it depends on the nature of individual materials forming the contact stack. Then, poly-Si and SHJ CSC are investigated individually.

i. Poly-Silicon based CSC

For poly-Si based CSCs, the resistivity of complete contact stack is clearly dependent on the thickness of SiO_2 layer. The decrease of SiO_2 thickness reduces the potential barrier size for tunneling. In addition, increasing doping in poly-Si layer and doping in buried region inside c-Si bulk can reduce the resistivity dependence on SiO_2 thickness as shown in Figure 31 and Figure 34. This is because the band alignment at poly-Si/c-Si interface is improved. The efficient band alignment can reduce the barrier for band-to-band tunneling.

ii. Silicon Heterojunction CSC

For SHJ based CSCs, in complete contact stack of metal/TCO/doped-layer/i-a-Si:H/c-Si, the resistivity exhibits different patterns for n-Contact and p-Contact as shown in Figure 39.

In n-Contact, increasing activation energy in doped thin film silicon layer reduces the resistivity as shown in Figure 41. Contact resistivity is minimized when activation energy is under 300 meV because of the low potential barrier for band-to-band tunneling. Additionally, increasing carrier concentration in TCO leads highly-efficient band alignment at TCO/doped-layer interface, which can improve the band-to-band tunneling and reduce contact resistivity.

In p-Contact, different pattern are exhibited when TCO carrier concentration lower than 1×10^{20} cm^{-3}. Due to the inefficient band alignment at TCO/doped-layer interface, trap-assisted tunneling (TAT) dominates the transport mechanism. The efficiency of TAT mainly depends on trap state in forbidden band as shown in Figure 41. The domination of TAT leads nonlinear I-V characteristic as shown in Figure 45, which

results in high recombination that should be avoided in solar cell. Apart from activation energy in doped layer and TCO carrier concentration, the thickness of i-a-Si:H passivating layer is also a parameter to affect contact resistivity for p-Contact. The decrease of thickness of i-a-Si:H passivating layer can reduce the potential barrier size for tunneling so as to reduce contact resistivity. Additionally, increasing the band gap of p-doped layer leads higher contact resistivity due to the larger potential barrier for hole carrier transport.

b) What is the contribution of each layer and interface to the equivalent resistivity of contact stacks?

In order to investigate the contribution of each layer and interface to the equivalent resistivity of contact stacks, the partial resistivity of contact stacks is evaluated.

For poly-Si based CSCs, the resistivity of metal/poly-Si interface is around 10^{-5} ~ 10^{-6} $m\Omega cm^2$, decreasing with increasing doping in poly-Si as shown in Figure 29. The resistivity for complete contact stack ranges within 10 ~ 10^6 $m\Omega cm^2$ as shown in Figure 31 and Figure 34. It is indicated that the most contribution to resistivity of poly-Si based CSCs is from tunneling barrier at poly-Si/c-Si interface.

For SHJ based CSCs, the resistivity of metal/TCO interface is around 10^{-5} ~ 10^{-7} $m\Omega cm^2$, decreasing with increasing carrier concentration in TCO as shown in Figure 38. The metal/TCO interface contributes little to resistivity of complete contact stack. The resistivity for partial contact stack of metal/TCO/doped-layer is shown in Figure 43. For n-Contact, it can be seen that the contribution of TCO/doped-layer junction to the resistivity of complete contact stacks increases with the increasing activation energy in doped layer. This is because the potential barrier in doped layer becomes larger with higher activation energy, and the tunneling barrier becomes larger at TCO/doped layer interface due to the inefficient band alignment. For p-Contact, apart from TAT dominated region due to low N_{TCO}, the TCO/doped-layer junction contributes most resistivity of complete stack independent of activation energy in doped layer. This difference pattern with n-Contact is due to the potential barrier for holes transport in doped layer is larger than electrons.

c) Which transport mechanism dominates the resistivity of contact stacks?

In general, at metal/semiconductor interfaces, tunneling and thermionic emission describe the transport across interfaces. In particular, for poly-Si based CSCs, direct tunneling is the core of the transport of carriers as transport performs towards only conduction or valence band for n- or p-contact stack respectively. In case of SHJ CSCs, transport through n-contact stack layers is also described by direct tunneling and/or thermionic emission. However, for p-contact SHJ stack, transport mechanisms exhibit more complexity. At c-Si/a-Si:H interface until p-layer the transport is through the valence band by means of direct tunneling/ thermionic emission. From p-layer to TCO, the transport is described by band-to-band tunneling, if the proper band alignment is achieved (see Figure 40). On the contrary, in the

absence of band alignment, the transport through p contact is band-to-band combined by TAT.

d) How can we reduce or manipulate the resistivity of contact stacks?

In order to reduce resistivity of poly-Si based contact stack, the thickness of SiO_2 layer should not exceed 1.2 nm. The resistivity is minimized when achieving very thin SiO_2 layer of 1 nm thickness. Additionally, high doping in poly-Si layer and doping in buried region inside c-Si bulk over 1×10^{20} cm^{-3} can also reduce the resistivity.

In order to reduce resistivity of SHJ based contact stack, the TCO carrier concentration should keep larger than 1×10^{20} cm^{-3} for n-Contact and 5×10^{20} cm^{-3} for p-Contact. The activation energy in doped thin film silicon layer should be lower than 300 meV, the lower the better. The thickness of i-a-Si:H passivating layer should not exceed 10 nm for p-Contact. For p-Contact, if the wide band gap is required to obtain good band alignment between doped layer and c-Si bulk, the doped layer can be replaced by one wide band gap layer together with one narrow band gap layer to reduce the potential barrier.

In addition to the answers to research questions, it is noteworthy to discuss the following aspects that were observed during the simulation process.

As discussed in **Chapter 2, Section 2.3**, the correction factor used in Eq (2-19) cannot solve the effect of inconsistent sheet resistance of semiconductor and contacts. In simulation approach, this problem can be alleviated by increasing the length of contact (i.e. the width of metal finger for practical device) and deploying contacts with wider distance (i.e. the pad spacing for practical device). Then, the contribution of sheet resistance prevails over the sheet resistance beneath metal contacts.

It provides that the presented simulation platform has the potential and flexibility of predicting the contact resistance for any type of CSC stack in terms of materials and number of layers.

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