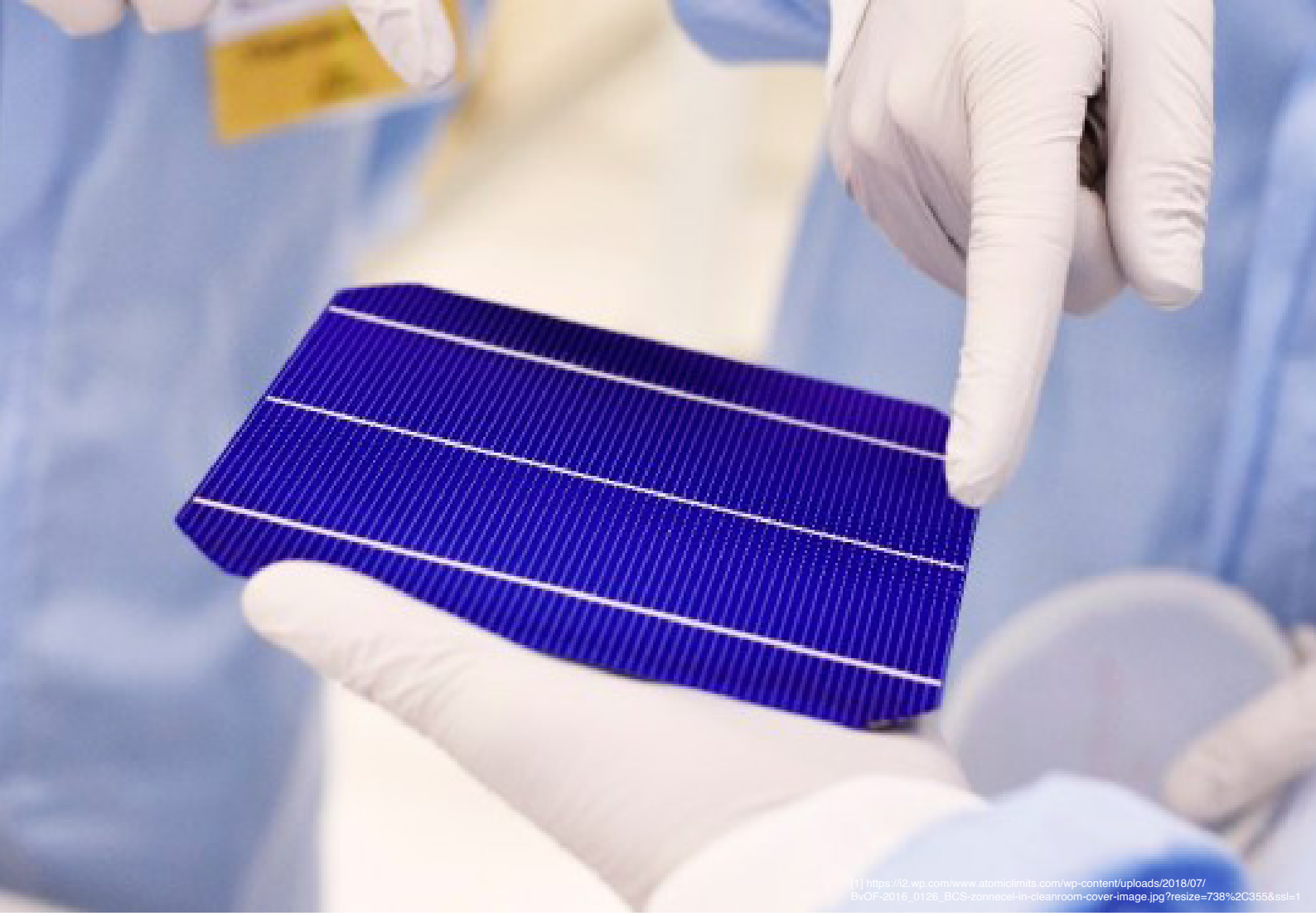

MASTER THESIS

Development of poly-Si(C_x) passivating contacts for high efficient c-Si based solar cells

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Development of poly-Si(C_x) passivating contacts for high efficient c-Si based solar cells

Master of Science

Sustainable Energy Technology

PVMD group

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"There are not problems, only solutions."

John Lennon

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Abstract

Carrier-selective passivating contacts (CSPC) are very promising contact structures for highly efficient silicon solar cell. They provide passivation of silicon surface and high carrier selectivity. So far, superior results have been achieved through the use of a stack of poly-Si with SiO_2. The objective of this project is the optimization of an alternative passivation stack based on carbon alloyed poly-Si (poly-SiC_x). The alloy is selected since carbon provides improved material resilience against blistering and wet-chemical stability in commonly used chemicals in the silicon industry. The optimized poly-SiC_x contacts are implemented in fornt back contacted (FBC) solar cell.

We improve the passivation quality of SiO_x/poly-SiC_x contacts optimizing several parameters. Our main focus is on the buffer layer optimization and its deposition methods comparing LPCVD and PECVD technique. We also turn our attention to identify the optimum annealing temperature and thickness of doped layers. Finally, we focus on the influence of the different capping layer composition on hydrogeneation process. With the optimization of the annealing temperature, and thickness of (i)a-Si layer deposited by LPCVD, we obtain high passivation quality on cell precursor structure: i-Voc of 713 mV, τ_{eff} of 2.14 ms and J_o of 9.5 fA/cm^2. On the contrary, during the optimization of buffer layer deposited by PECVD, we firstly focus on the material properties and the bonds present in the deposited layers to minimize the hydrogen contact. After the optimization of the (i)a-Si:H layer thickness, deposition parameters and annealing temperature on (p)poly-SiC_x symmetrical sample, we obtain the remarking results: i-Voc of 681 mV, τ_{eff} of 1.15 ms and J_o of 31.3 fA/cm^2.

The potential of SiO_x/poly-SiC_x passivation contacts is checked on the device level of FBC solar cells. On FBC solar cells with buffer layer deposited by the PECVD, after an effective post annealing of the cell performed at a temperature of 350°C, we achieve the remarking parameters; Voc of 659 mV, J_{sc} of 34.36 mA/cm^2, FF of 77.58 % and η_{act} of 17.56 %. We check also the the influence of different SiN_x capping layers on the hydrogenation process. We obtain the best results on the FBC solar cell on which the capping layer is stoichiometric. These results, after the high-temperature port annealing, are Voc of 690 mV, J_{sc} of 36.18 mA/cm^2, FF of 80.38 %, and η_{act} of 20.06 %. These are also the best FBC poly-SiC_x results which we have obtained in this project.

The application of SiO_x/poly-SiC_x passivation contacts is investigated also in terms of the IBC solar cell concept. We proposed two alternative fabrication methods based on photolithography, which is crucial for contact formation of IBC solar cells. One of the fabrication methods focuses on a buffer layer deposited by LPCVD as this layer is of higher quality and homogeneity than the interlayer deposited by PECVD. The second developed method focuses on the buffer layer deposited by LPCVD and PECVD. Despite the lower passivation quality achieved on contact with the buffer layer deposited by PECVD, this method has a significant advantage because it requires fewer photolithography steps when compared to the fabrication method, which makes use only of buffer layers deposited by LPCVD. In the view of the photolithography processes, we have performed etching tests on (i)a-Si, (i)a-Si: H, and amorphous doped layers. Thanks to these tests, we have identified etching rates of these layers in various prepared poly-Si etching solutions.

Contents

Nomenclature

τ_{eff}	Effective lifetime
σ_L	Conductance
ALD	Atomic Layer Deposition
CSPC	Carrier-Selective Passivating Contact
DSP	Double Side Polished
E_c	Conduction Band
E_v	Valence Band
EQE	External Quantum Effciency
FBC	Front and Back Contacted
FF	Fill Factor
FGA	Forming Gas Annealing
FST	Front Side Textured
FTIR	Fourier-Transform Infrared Spectroscopy
FZ	Float Zone
HF	Hydroflouric Acid
HNO_3	Nitric Acid
ITO	Indium Tin Oxide
i-V_{oc}	Implied Open Circuit Voltage
IBC	Interdigitated Back Contact
J_o	Saturation Current density
J_{sc}	Short-Circuit Current density
LPCVD	Low Pressure Chemical Vapour Deposition
NAOS	Nitric Acid Oxidation of Silicon
PECVD	Plasma Enhanced Chemical Vapour Deposition
poly-SiC_x	Polycrystalline Silicon-Carbide
poly-Si	Polycrystalline Silicon
PV	Photovoltaic
SiO_x	Silicon Oxide
SP	Screen-Printing

TCO	Transparent Conductive Oxide
TMA	Terimethylaluminium
V_{oc}	Open Circuit Voltage

1

Fundamentals

This chapter is an introduction to the presented project, it contains basic background information which is crucial for a correct understanding of this master thesis topic. Firstly, an introduction to solar energy is given. Subsequently, the analysis of photovoltaic technology development is being performed. The basic working concept of a PV cell is also presented as well as the main loss mechanisms that suppress the cell output. Following, the most efficient passivating contact architectures are introduced with the main focus on poly-silicon passivating contacts, which are also the main objective of this project. Finally, the motivation for the master thesis is being presented followed by the work outline and the research questions.

Introduction

Nowadays one of the most significant issues that society has to face is the growing world population and consequently increasing demand for energy. Electricity is not a luxurious good anymore but rather a necessity. In 2017, global total final electricity consumption was estimated at a level of 21 372 TWh [1]. As stated by IEA, in 2018 the energy demand has grown up by 2.3 % [2]. This rising trend is expected to continue in the next years.

The biggest contribution to the increase in energy demand have developing countries, the reason for this is the significant population growth and economic progress, which results in a higher need for energy. Most of the growth in global electricity consumption (80 %) is recorded in Asia, where China contributes 60 % of it [3]. The explanation of this trend can be the demand acceleration against steady economic growth and industrial demand. In other Asian countries like India, Indonesia or South Korea, the analyzed growth is a consequence of the same reasons as in China. Figure 1.1 depicts the global trend for energy demand over the past 30 years. It can be easily recognized that electricity demand in well-developed regions of the world like in Europe or North America is rather constant. This is a consequence of the fact that the electrical revolution; electrification of households and the introduction of the electrical railway in these areas started at the beginning of the 20th century [4].

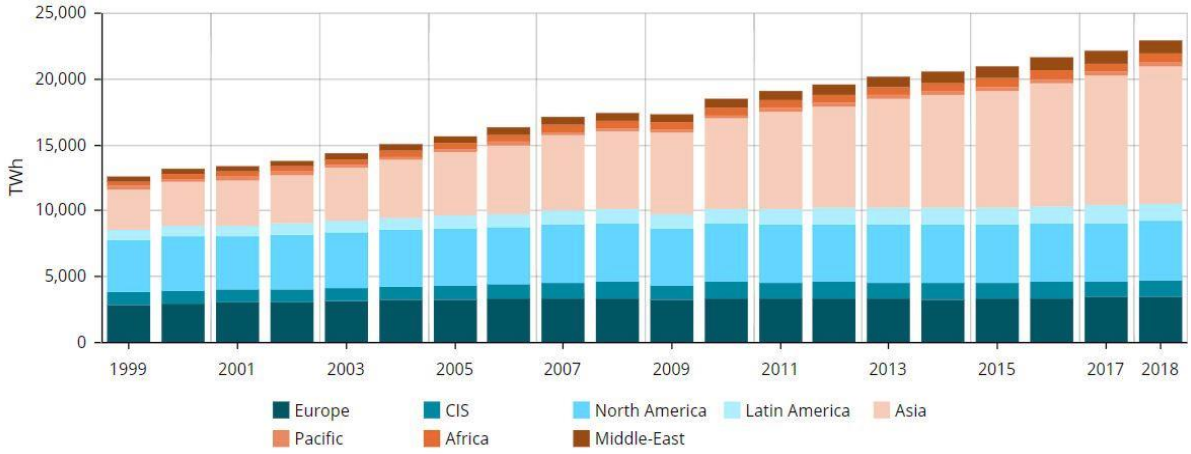


Figure 1.1 Global power consumption trend over past 20 years [3].

Despite the increasing trend in energy and electricity demand many people are still living without access to these goods. As estimated by IEA almost 14 % of the global population (1.1 billion people) is living in unelectrified areas [5]. Besides, IEA states that 2.8 billion of people-38 % of the world population heat their houses and cook by burning wood and coal. In the nearest future, the reliable electricity network will have to be delivered to these communities that will lead to even faster growth in electricity demand.

Up till these days, the great majority of global energy need was delivered by fossil fuels. Extraction and burning of coal, gas, and petrol lead to disastrous changes in Earth's natural environment. One of the biggest issues that global society has to face now is the greenhouse effect and rapid climate changes that are a consequence of it. It is projected that by the end of 2020 the global surface temperature will be at least 0.5 °C warmer than in the past 30 years (1986-2005) [6]. This phenomenon will have a detrimental effect on the global ecosystem. In order to avoid these many global actions should be performed. In December 2015 with the Paris Agreement 197 countries agreed to boost the global reaction to the danger of climate change by keeping the rise of global temperature in this century below 2 °C above the pre-industrial time and to take actions to suppress the temperature increase even till 1.5 °C [7]. Besides, the Agreement aim is to increase the ability of countries to deal with the consequences of climate change. In order to reach these ambitious goals, fast actions have to be performed for instance the introduction of new pilot renewable technologies and appropriate mobilization of countries governments. It can be stated that the main good outcome of climate change is the increased interest in renewable technologies and their significant growth.

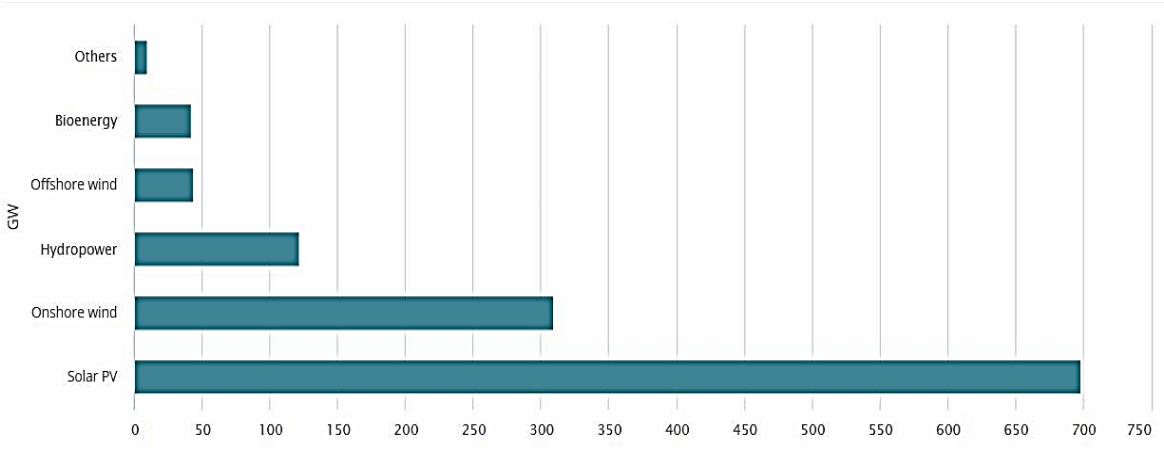


Figure 1.2 Renewable capacity growth between 2019 and 2024 by technology [8].

In 2018, renewable energy generation increased by 4 %, which accounts for approximately one-quarter of global energy demand growth [8]. Solar PV, wind and hydropower accounted for about a third of the growth, with bioenergy accounting for most of the rest. According to the estimations renewable power capacity is forecasted to expand by 50 % between 2019 and 2024, where this growth will be mainly driven by solar PV (Figure 1.2), that alone contributes to almost 60 % of the forecasted growth, with onshore wind representing one-quarter of it [8].

1.1 PV Technology

PV systems technology can directly process solar energy into electricity. Solar PV has two important advantages. Firstly, PV module manufacturing can be performed in big factories, which allows for economies of scale. On the contrary, PV is a very modular, compact technology, that can be mounted in very small quantities at a time. This feature allows for a broad range of applications. Developed systems can be small, like in off-grid applications, up to utility-scale power generation modules.

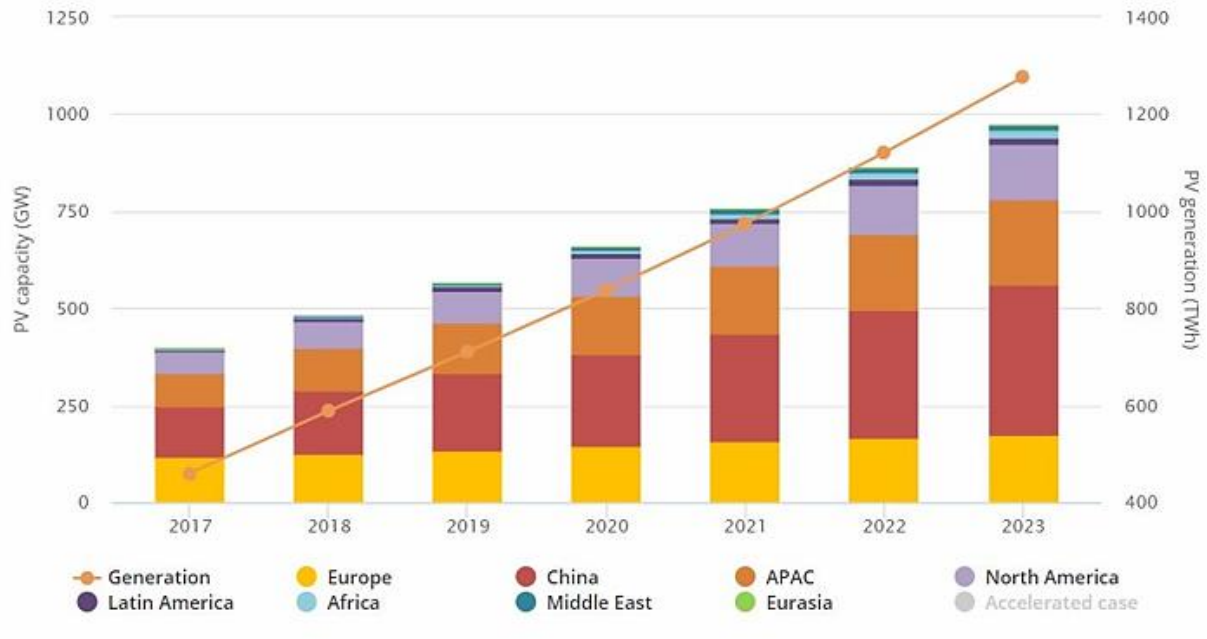


Figure 1.3 Solar PV generation and cumulative capacity by region 2017-2023 [9].

As stated by IEA, in 2017 the cumulative installed PV capacity reached approximately 398 GW and produced over 460 TWh of energy [9]. These values represent nearly 2 % of global power output. Figure 1.3 depicts the solar PV production and cumulative capacity by region. As it can be easily recognized PV technology is following an increasing trend what is a very positive tendency since PV development can be the main entity in reducing fossil fuels share in global energy production. Besides, it is worth mentioning that the most significant increase in PV capacity is recorded in China, which contributes to 60 % of the energy demand growth in Asia, as mentioned in the introduction. Consequently, accordingly to this forecast, China will be in the future the country with the biggest share of PV in total energy production.

Solar PV is classified in 3 generations. The 1st generation consists of materials with a bandgap of 1.1 eV that vary by crystallization level; there can be distinguished mono- and poly-crystals. Although the efficiency of monocrystalline silicon is higher than polycrystalline, polycrystalline technology is dominating the market, sharing about 95 % of total PV production [10]. The first-generation solar cells are based on a single p-n junction concept and high purity crystalline silicon (c-Si). The theoretical efficiency limit for 1st generation solar cells is known as the Shockley Queiser limit which corresponds to the efficiency value of 29.4% for materials with an aforementioned bandgap of 1.1 eV and considers only Auger recombination [11]. The record efficiencies for 1st generation c-Si solar cells are reaching a level of 26.7 % for n-type Interdigitated Back Contact (IBC) solar cells by Kaneka [12].

The 2nd generation of solar PV consists of a-Si: H, CIGS, CdTe, and c-Si solar cells. All of these devices belong to the so-called thin-film technology. A great advantage of this technology is the fact that the device can be fabricated on flexible substrates, hence can be installed on rough surfaces e.g on a spherical shape. Besides their cost of production is also lower than 1st generation technology due to the fact that less material is needed for the production and fewer steps are performed during the fabrication [13]. Regardless of the advantages listed above 2nd technology

solar cells reach lower efficiencies than c-Si. The record efficiency for CdTe (First Solar) is 21%, for CIGS (Solar Frontier) is 21.7 % and for a-Si 10.2 % (AIST) [12].

Third-generation technology includes the devices that are produced from very cheap abundant materials or that are potentially able to overcome the Shockley–Queisser limit [14]. The third-generation concept focuses on tandem approach-many solar cells with different bandgaps stacked on each other (one on top of the other). These concepts achieved efficiencies of up to 27.3 % (perovskites/monolithic Si) manufactured by Oxford PV [12]. On the contrary, 3rd generation concepts that are basing on abundant materials reach significantly lower efficiencies e.g. organic cell manufactured by Toshiba has a record efficiency of 11.2 % [12].

1.2 Crystalline Silicon

Photovoltaic (PV) cells based on crystalline silicon (c-Si) have governed the PV market with a share of 95 % of total energy production [10]. It is expected that c-Si will have an essential role in future PV market development.

Silicon is an abundant material commonly available on the earth's crust and is nontoxic what is a great advantage over CdTe technology [15]. Furthermore, silicon has a bandgap energy of 1.12 eV what corresponds to a light absorption cut-off at a wavelength of 1107 nm [16]. This bandgap is effectively correlated with the solar spectrum, very close to the optimum for solar energy conversion to electric using a single semiconductor optical absorber.

Silicon is an indirect bandgap material [17]. This means that the conduction band minimum and valence band maximum are not at the same position in the momentum space. This fact has a significant advantage. It makes the radiative recombination inefficient, which consequently causes a longer lifetime of photogenerated electrons and holes [18]. Unfortunately, due to previously mentioned indirect bandgap silicon has a low light absorption coefficient near the bandgap area. Nevertheless, taking into account simple wafer texturing that can be combined with antireflection coatings and rear surface reflectors an efficient light absorption can still be obtained (including infrared region) [16]. Surface texturing is commonly used concept as the surface "roughening" lowers the reflection by improving the chances of the reflected light to come back into the surface, rather than out to the air.

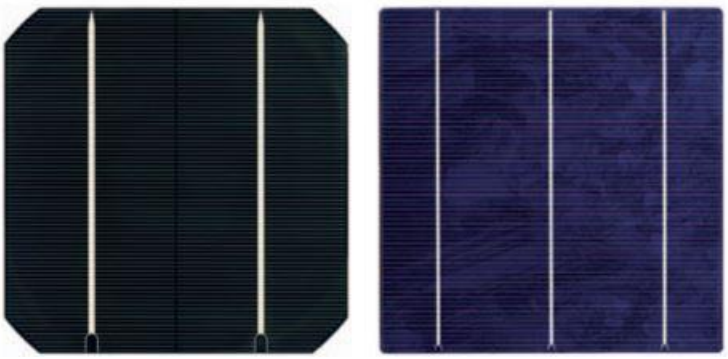


Figure 1.4 Monocrystalline and multi-crystalline wafer [19].

Figure 1.4 depicts the comparison between monocrystalline silicon and mulit-crystalline silicon solar cells. Monocrystalline silicon reaches higher efficiencies than multicrystalline Si (mono-Si 26.7 % and multicrystalline 22.3% [12]). The explanation of this can be the structure of the materials. Poly-Si is a material that contains many small grains of crystal that have a random orientation. On the other hand, a monocrystalline silicon wafer has continuous and unbroken crystal lattice without any visible grain boundaries in the bulk [17]. Consequently, the effective charge carrier lifetime for poly-Si is shorter than for mono-Si. This is a direct result of the Shockley-Read-Hall (SRH) recombination mechanism since the more grain boundaries present in the material the more defects in the bulk, and the lower the lifetime of minority charge carriers. Nonetheless, despite the higher efficiencies reached by mono-Si, polycrystalline silicon is more often used than monocrystalline in commercial modules due to its lower production cost. Besides, the process of poly-Si production is more simple than monocrystalline silicon and the amount of waste that comes from polysilicon production is lower than from production of mono-Si [19].

1.3 The working principle of a solar cell

The photovoltaic solar cell (Figure 1.5) is a semiconductor device that is able to directly convert the sunlight energy into electrical energy without any transitional process. The fundamental principle of the PV cell operation is the photovoltaic effect. The photovoltaic effect creates a potential difference (voltage) between the junction of two different materials as responding to the incident radiation. If two of the aforementioned materials are connected with an external circuit power will be delivered to an external device; the current will flow from the generator (PV cell) to the load e.g lamp. In order to fully describe the basic principle of PV cell operation, it is worth mentioning that in the photovoltaic effect three different processes can be distinguished: generation, separation, and collection of charge carriers at the terminals of the junction [20]. Each process will be shortly described below.

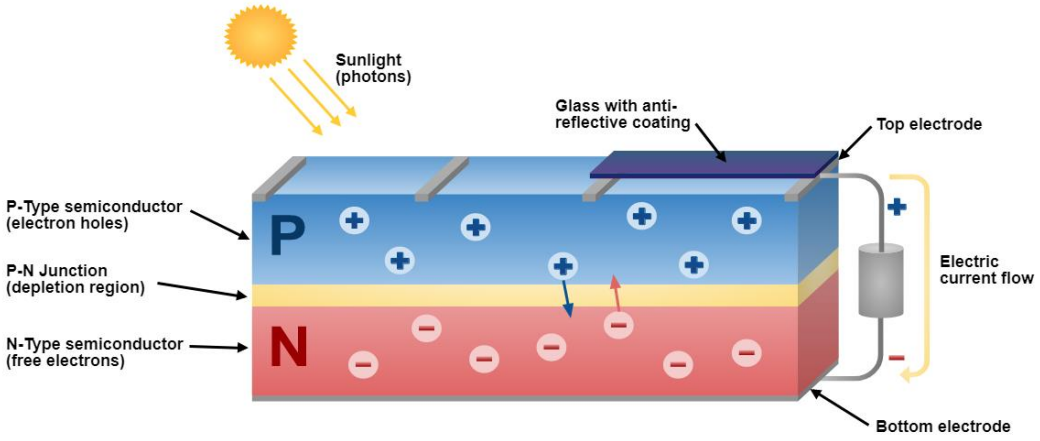


Figure 1.5 PV cell under the operation [21].

While explaining the working principle of the PV cell it is crucial to refer to the bandgap of the analyzed material. Consequently, Figure 1.6 depicts the bandgap of typical semiconductor material as c-Si. This figure presents also the three possible conditions which may occur during the generation process of the charge carriers in semiconductor material. Besides, analyzing Figure 1.6, three different levels can be distinguished: E_V- valence band, E_C-conduction band, and E_G- bandgap.

Electrons and holes are the two charge carriers that are initiating the current flow in semiconductor materials. A hole in the band theory of electrical conductivity is the lack of an electron in the valence band [22]. Even though the hole is not a physical particle in the sense as an electron, the hole can move between atoms in a semiconductor material. On the other hand, electrons rotate around the nucleons at defined energy levels called bands. The hole is formed in an atom when an electron moves from the valence into the conduction band.

Electrons in the E_V are strongly bonded with the atom. Ev has a lower energy state, hence, due to the application of external potential, the electrons in Ev move out of it and relocate towards the higher state-conduction band. This mechanism allows the conduction through the material. On the contrary in the E_C electrons are not attached to the atoms, consequently, they can freely move and conduct the current. E_G is defined as the energy difference between the E_C bottom and E_V top. Energy levels between E_C and E_V are forbidden energy states for electrons and this energy is defined as bandgap (E_G). These energy levels are the origin of one of the recombination mechanisms - Shockley Read Hall Recombination (SRH) that will be described in detail in the next subsection.

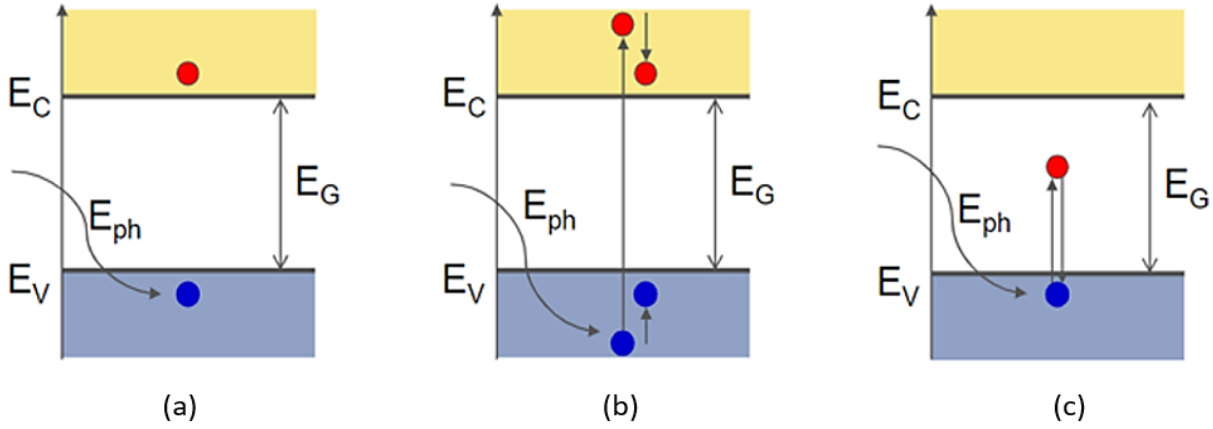


Figure 1.6 Generation of charge carriers (a),(b),(c) [23].

Charge carrier's generation

Generation of charge carriers can occur in the semiconductor if a list of requirements will be met since different photon energies cause different mechanisms. Figure 1.6(a) presents an ideal condition when the photon energy has an energy equal to E_G. In this situation, photon will be absorbed by the semiconductor and an electron will be excited from the E_V to E_C. Subsequently, in E_V a positive charge carrier-hole will be left. This photon energy forms the ideal condition for charge carrier's generation. Nonetheless, two other-different mechanisms can also occur. First, the incident photon may have energy higher than E_G (Figure 1.6(b)), consequently, heat dissipation will occur. This process is caused by the excited electron that will „jump" into a higher energy state in E_C and later will return into the conduction band edge and dissipate excess of energy in form of

the heat. This phenomenon is known as thermalization loss. The third condition occurs when the photon energy is lower than the bandgap energy (Figure 1.6(c)). In this case, the photon will be not absorbed but will flow through the semiconductor without excitation of the electron.

Nevertheless, the set of processes described above is valid for a direct bandgap, and silicon is indirect bandgap material (section 1.2). A comparison between direct and indirect bandgap material is depicted on Figure 1.7. In indirect bandgap material electron requires not only the energy but also a momentum in order to be excited from the conduction band. The needed momentum can be delivered by the crystal lattice vibrations or by the photons.

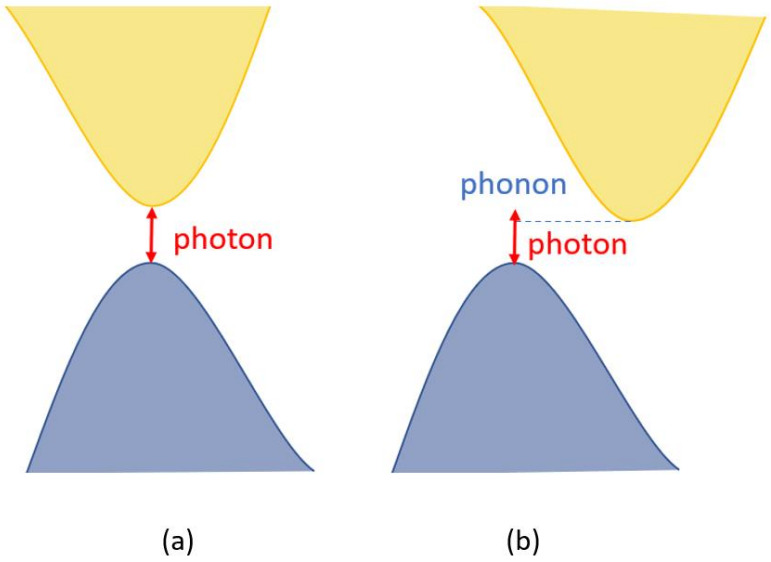


Figure 1.7 Direct (a) and indirect (b) bandgap material [24].

Charge carrier's separation

The subsequent stage after the charge carrier's generation is their separation. Charge carrier separation can be compared with the membrane that allows only one charge carrier to pass through. In reality, this membrane is called a p-n junction (Figure 1.8). A solar cell design, depletion region width must be optimized in such a way that it will allow electrons and holes to reach the membrane before they will recombine with each other. Electrons are negative charge carriers while holes are the positive ones. Their opposite charge provokes the recombination process that leads to a lower electric current. Details of the recombination process will be described in the following subsection.

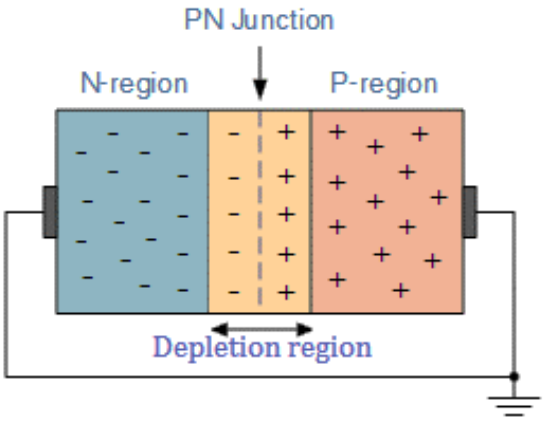


Figure 1.8 P-N junction [25].

Collection of charge carriers

Finally, the charge carriers are extracted from the PV cell with the electrical contacts and they can execute work in an external circuit. Electrons are passing through the external circuit and recombine at an absorber metal interface with holes. In this step electron chemical energy is converted into electrical energy.

1.4 Recombination mechanisms

Recombination is a loss mechanism in the solar cell. The recombination results in a reduction of the available charge carriers what consequently causes the suppression of the current. There are four different recombination mechanisms: Surface, Radiative, Shockley Read Hall (SRH), and Auger recombination (Figure 1.9). In order to define the recombination rate in solar cells, it is worth referring to the minority carrier lifetime that is given by the equation (1.1). This expression defines the average time that excess minority charge carrier needs to recombine. In modern photovoltaic, the biggest challenge is to decrease surface recombination [26], since the bulk of the wafer is produced of great quality and recombination mechanisms that occurred in the bulk are not the major source of the losses. The detailed mechanisms that suppress the surface recombination are described in section 1.5. The equation for the effective lifetime (equation (1.1)) of the minority charge carriers consists of two components. One that represents the surface recombination and the second one that refers to the recombination that occurs in the cell bulk, while to the bulk recombination component contribute all listed recombination mechanisms apart from the surface one.

$$\frac{1}{t_{eff}} = \frac{1}{t_{bulk}} + \frac{1}{t_{surface}} \qquad (1.1)$$

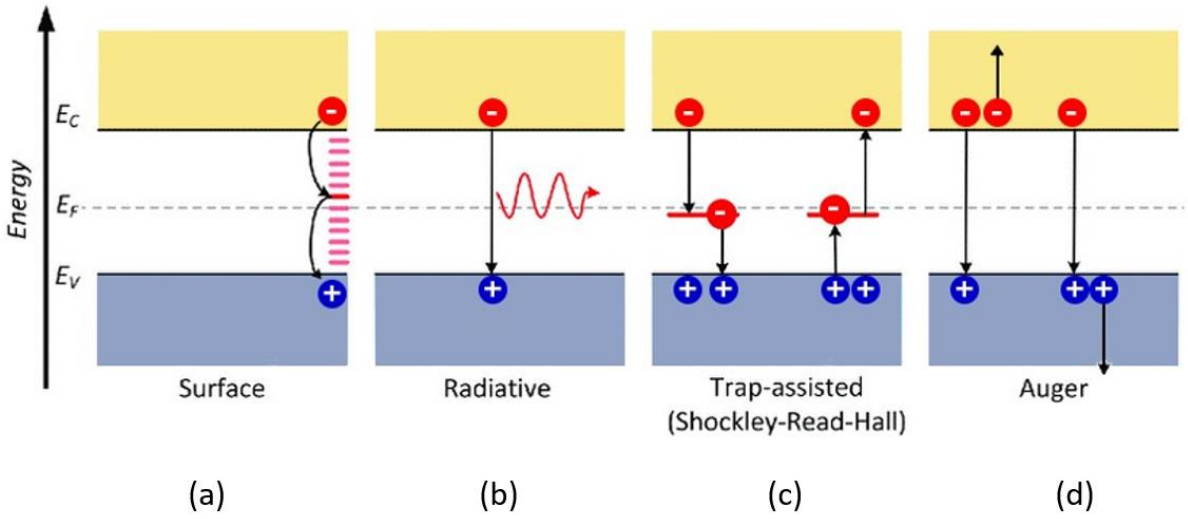


Figure 1.9 Recombination mechanisms[24].

Surface Recombination

Surface recombination (Figure 1.9(a)) is the only mechanism that does not occur in the wafer bulk but, as the name suggests, at the semiconductor surface. This is the loss that the most significantly suppresses the efficiency of the cell. Therefore, in order to enhance cell performance, passivation techniques are introduced whose main aim is to reduce the surface recombination process. More details of analyzed passivation solutions can be found in section 1.5.

The origin of surface recombination is the presence of dangling bonds on the semiconductor surface. These defects are a result of the fact that many valence electrons at the semiconductor surface cannot find a partner that they can form a covalent bond with. Consequently, because of these dangling bonds, many trap states are formed within the E_G. Subsequently, these defects may boost SRH recombination which bases on trap states within the bandgap of the material. The surface recombination rate for an n-type semiconductor can be defined by the equation (1.2) :

$$R_s = \upsilon_{th}\sigma_p N_{sT}(p_s - p_0) \qquad (1.2)$$

Where υ_{th} is the thermal velocity, N_{ST} is the surface trap density and σ_p is the capture cross section for holes.

Equation 1.2 illustrates that surface recombination can be reduced in two ways. Firstly, due to the reduction of the trap density N_{sT}, as the higher the trap density the higher the possibility of electron and hole recombination and the enhanced probability of occurrence of trap states in the bulk. Secondly, surface recombination can be suppressed by the reduction of minority carrier concentration on the surface, as the more minority charge carriers the higher the recombination

possibility. This issue can be mitigated due to the introduction of the back surface field or front selective emitter [16].

Radiative Recombination

Radiative recombination is the reverse process of photon absorption, where an electron comes back to its equilibrium energy and emits a photon [27]. This photon can have the energy equal to E_G or lower. Radiative recombination is the major recombination process in direct bandgap semiconductors (Figure 1.7(a)), hence it does not play a significant role in the silicon PV cells.

Shockley Read Hall Recombination

SRH recombination (Figure 1.9(c)) takes place when an electron falls into a "trap state"; an energy level within the E_G. This trap state can be induced for example by the presence of a structural defect or foreign atom. Once the trap is filled it cannot accept another electron. Subsequently, the electron that fills the trapped energy can in a next step fall into an empty state in the valence band, hence completing the recombination process. This process can be described either as a two-step conversion of an electron from the conduction band to the valence band or as the annihilation of the electron and hole which recombine in the trap.

Auger Recombination

Auger recombination (Figure 1.9(d)) is a non-radiative process in which the excess energy from the electron-hole recombination is transferred to the third particle (electron or hole). If the energy and momentum are transferred to electrons as the third particle the recombination rate is given by equation 1.3. On the other hand, if the third involved particle is a hole the recombination rate is characterized by an equation 1.4.

$$R_{eeh} = C_n n^2 p \tag{1.3}$$

$$R_{ehh} = C_n p^2 n \tag{1.4}$$

Where C_n and C_p are the proportionality constants, n electron charge carrier density and p hole charge carrier density.

Within the Auger recombination process remaining steps can be distinguished. Firstly, the particle is excited into higher energy levels and afterward relaxes again, its energy is transferred into vibrational energy of the lattice and lastly, this energy is converted into heat. As Auger recombination is the process that involves three particles this is the major recombination mechanism that occurs in the bulk of heavily doped semiconductors[28].

1.5 Passivation techniques

Currently, the solar cell efficiency can be improved mainly due to suppression of the surface recombination. This is a direct consequence of the fact that the recombination process at a silicon

solar cell is governed by the existence of lattice defects-dangling bonds, which reduce the voltage and consequently lowers the efficiency of the solar cell [29].

Further, recombination at the c-Si surface can be lowered by one of the subsequent two solutions, or a mix of both. Firstly, by chemical passivation which can be treated as the surface passivation "par excellence"[26]. Secondly, by changing the relative concentrations of electrons and holes-field effect passivation.

Chemical passivation; refers, to the joint of molecular or atomic species to the unfulfilled "dangling" bonds of surface Si atoms. Typically, a certain amount of interface defects persists after thin film deposition or an oxidation process. The density of these "defects" can be significantly reduced through a hydrogenation treatment. The existence of hydrogen, in atomic form, is a simple common ground for all the approaches that led to the high quality of surface passivation, in conjunction with semiconductors like amorphous silicon (a-Si:H) and dielectrics like silicon oxide ($Si0_2$)[26].

Field effect passivation; consists in reducing the recombination at the c-Si interfaces by introducing a layer that can repels either electron or holes [30]. This means that the field-effect passivation technique is using the conduction phenomena as the main driving force. Consequently, it can be stated that there exist "electron contact" or "hole contact" which refer to a multilayer structure or region, which contain an outer metal layer and which has high conductivity for one of the two carriers (contact condition) and builds an asymmetry in the carrier conductivities (selectivity condition) [26]. The easiest way to achieve field-effect passivation is by heavy doping. The additional doping significantly suppresses the minority carrier conductivity by lowering the equilibrium concentration of minority carriers as a result of the difference in chemical potential in favor of the c-Si bulk; and reducing the minority carrier mobility. Simultaneously, the majority carrier conductivity is increased due to the large concentration of these carriers, leading to a low contact resistivity. This allows a relatively low J_o-recombination current (representing recombination losses) to be accomplished even if the defect concentration at the c-Si/metal interface is very high [30].

1.5.1 Silicon heterojunction solar cells

The silicon heterojunction (SHJ) was invented in the 1990s and has been commercialized under the name of HIT (heterojunction with intrinsic thin layer). The heterojunction between two materials is formed when they are connected to each other. By the use of this concept, Kaneka Corp. has manufactured SHJ cells with an outstanding record parameters with fill factor (FF) 84.9 % and conversion efficiency of 26.7 % [31].

The silicon heterojunction concept is formed basing on two passivation approaches mentioned in previously. Firstly, it uses a thin hydrogenated amorphous silicon a-Si: H layer in order to achieve high surface passivation (chemical passivation) [32]. Secondly, the passivating thin film is embedded below the electron selective and hole selective contact layer to provide field-effect passivation. These solutions outputs to virtually recombination-free areas, even for surfaces contacted with the metal electrodes. Consequently, SHJ cells have very high V_{oc}, which can reach a value of 750 mV [33].

The manufacturing process of SHJ cells starts with the texturing of the surface and subsequent cleaning. Afterward passivation of the surface with aSi:H is performed. In order to form the carrier selective contacts, doping layers are deposited. Phosphorus (P) is used as an n-type layer for the conduction of electrons and Boron (B) as a p-type layer for the transport of holes. This means that minority carriers are being repelled and do not accumulate at the surface, which ensures a low surface recombination rate. The full-contact area is created when the transparent conductive oxide (TCO) is being deposited in order to boost the lateral conductivity of charge carriers. This is because doped layers are not highly conductive. Besides, TCO acts as an antireflection coating which results in enhanced optical performance [34].

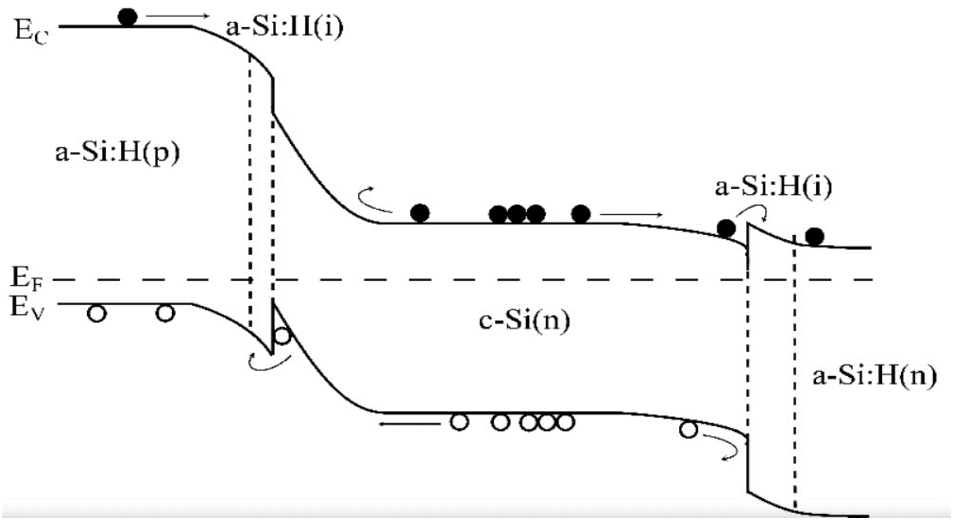


Figure 1.10 SHJ cell band diagram [35].

Band diagram of HIT heterojunction is depicted in Figure 1.10. It can be easily recognized that the a-Si:H has a wider bandgap than the c-Si. The bandgap of a-Si:H depends on hydrogen content (increases with hydrogen content) and most typically has a range of 1.7-1.8 eV [36], while c-Si has a bandgap of 1.12 eV. Furthermore, in Figure 1.10 are visible some band offsets which provide field effect passivation; ΔEv (valence band offset) and ΔEc (conduction band offset).

ΔEc creates the electron accumulation at the interface between c-Si and (i)a-Si:H. Subsequently, electrons can overcome the energy barrier, move to n-type a-Si:H and finally can be collected at the electrode. In contrary holes are being repelled due to energy generated by the n-type layers. Using the same rule, in the hole contact as in the electron contact, in hole contact electrons are pushed away as a result of energy barrier inferred by the p-type and (i)a-Si:H and at the same time holes are passing through the junction and finally are collected in the electrode.

1.5.2 Poly-silicon passivating contact

Poly-silicon passivating contacts are known since the mid-1980 [16]. The concept of implementation of an ultra-thin layer of SiO_x between semiconductor and metal was used in metal-insulator-semiconductor and later was used in devices with a p-n junction.

This passivation contact has been implemented in a hybrid device named TOPCon with a diffused front emitter and a poly-Si passivating rear contact (Figure 1.11). The TOPCon structure

incorporates a thin tunnel oxide and a phosphorous (P) doped poly-Si layer contact. The P-doped polycrystalline-silicon (poly-Si) layer can be manufactured by either crystallization of (i)a-Si:H or by direct deposition of poly-Si using LPCVD (Low-Pressure Chemical Vapour Deposition).

One of the carrier selectivity approaches present in TOPCon structure is the direct tunneling of carriers via a very thin SiO_x. As the oxide layer is present, it is roughly impossible for the minority carriers, holes for the n-type wafer base, to reach the back contact of the cell since they cannot pass the potential barrier introduced by the oxide layer. On the contrary, since this layer is kept very thin, electrons can tunnel through the barrier and be collected at the back contact with virtually zero loss. This combination was proposed by Fraunhofer ISE. This institute is also the holder of the highest efficiency developed for this concept, 25.7 % (Voc=725 mV, Jsc=42.5 mA/cm2, FF=83.3% [37]. The main advantages of TOPCon technology are an efficient charge carrier transport, full-area surface passivation, and the compatibility with the high-temperature industrial process [38]. Especially the compatibility with the high temperature industrial process is very significant, as it has a big influence on the manufacturing process of a-Si:H that deteriorates at temperatures above 250 °C [30] .

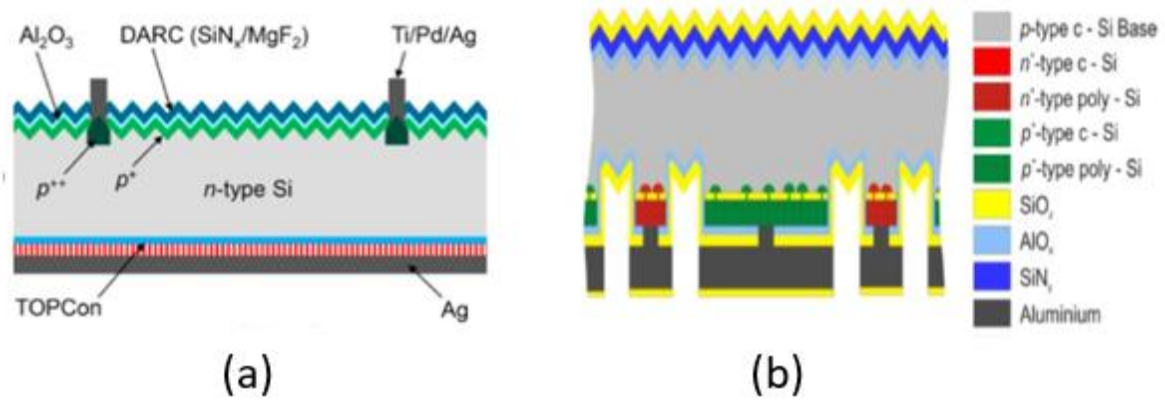


Figure 1.11 TOPCon [39] (a) and POLO [37] (b) solar cell structures.

The other polysilicon passivated contact is the so-called POLysilicon on Oxide (POLO). This concept was developed by the end of the 1970s and the beginning of the 1980s. Implementation of the POLO structure allowed for great results. The highest efficiency obtained by this concept is 25 % (Voc=723 mV, Jsc=41.9 mA/cm^2) [40].

Figure 1.12 depicts the band diagram of the poly-Si passivating contact consisting of a SiO_x layer and a highly doped poly-Si layer. The band bending visible on the Figure 1.12 is the result of the work function difference between heavily doped n-type Si and n-Si base. This means that the electrons will concentrate against the poly-Si layer and tunnel through oxide (indicated by the thick arrow) simultaneously holes will be repelled from the oxide layer. The tunnel oxide provides the energy barrier for electrons (3.1 eV) and holes (4.2 eV) [41]. Nonetheless, tunnelling can arise only if the oxide layer is thin enough typically around 1.1 nm [42].

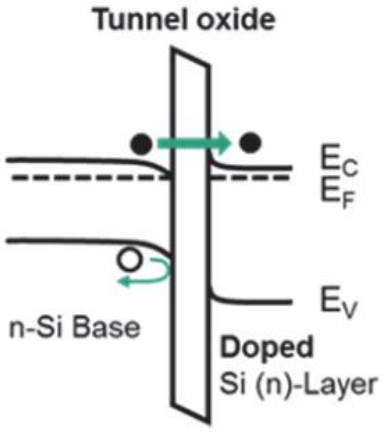


Figure 1.12 Electron selective poly-silicon passivating contact [43].

Tunnel oxide is a basic component of contact since it cannot inhibit majority carriers flow and at the same time has to diminish the minority carrier recombination. Besides, SiO_x provides chemical passivation of the surface (saturates the present dangling bonds).

Furthermore, due to silicon oxide implementation epitaxial growth of silicon crystals in poly-SiC_x material can be avoided [34], which has a crucial meaning for this project. Finally, as it was described above SiO_x maximizes the band bending what enhances the passivation and during the high temperature, annealing works as a barrier to the diffusion dopants to the bulk [44]. While the diffusion is the move of atoms from regions of high concentration of mobile carriers to regions of low concentration. Diffusion occurs at all temperatures, but the diffusivity has an exponential reliance on temperature [42].

As it was listed above silicon oxide has a great list of advantages, nonetheless, inappropriate implementation of this layer can also have a detrimental effect on the cell. A too thick silicon oxide layer will suppress the charge carriers tunnelling what will result in a low FF. The thinner SiO_x layer has better carrier tunnelling and easier creates conduction-enabling pinholes [45]. Consequently, the optimum oxide thickness is found to be between 1.2-1.5 nm [46].

This section focuses mainly on the advantages of implemented poly-Si passivation contacts. Nonetheless, there are still constraints that reduce the application of the mentioned materials in solar cells. Firstly, poly-Si CSPCs are not transparent, exclusively when heavily doped, due to the significant free-carrier absorption (FCA). Consequently, this results in significant parasitic absorption of the high energy photons, as poly-Si layers have higher E_G. Besides, significant losses occur also in the infrared region, where the low energy photons are also not being absorbed. This limitation makes the application of these layers more complicated at the front side of the solar cells. Moreover, poly-Si has a higher resistance than Si, this leads to reduced carrier mobility and affects the FF.

1.5.3 Alternative passivating contacts

In the previous section were listed advantages as well as the drawbacks of the well-known passivation techniques; poly-Si/SiO_x CSPC. One of the most substantial problems of these concepts is the presence of the highly doped layers, where more charge carriers are present, consequently leading to higher Auger recombination losses (section 1.4). The increased doping has also a detrimental effect on the V_{oc} and J_{sc} of the device [16]. Besides, the (i)a-Si:H layer in SHJ concepts and poly-Si layer in poly-Si/SiO_x CSPC have higher bandgap compared to the Si. This consequently encourages the absorption of high energy photons, again reducing the J_{sc} of the cell. Therefore, in order to mitigate this other alternative passivation techniques are being developed.

One of the alternative solutions of passivating contacts can be the implementation of transition metal oxides that have a high working function. For example as hole selective materials for c-Si solar cells, can be mentioned MoO_x and WO_x that have a high work function (>6 eV) and are highly transparent material as compared to silicon-based films which makes them very interesting for application at the front surface. Using such an extreme work function for selective contact formation results in a considerable band bending that consequently improves carrier collection and lowers surface recombination. Currently, the record efficiency for the solar cell that is using MoO_x as hole selective contact is 23.5 %[47]. The other transition metal VO_x is used as an electron selective contact. The record efficiency for this concept is 19.7 %[48].

Despite the good response of the MoO_x and WO_x to the high energy photons (high work function) these materials have another significant advantage; they have a low thermal budget used during their manufacturing. Both materials (MoO_x and WO_x) require fabrication temperatures less than 200 °C [49]. This can be a great advantage when it comes to the cost of production and efficient energy use during the fabrication process, as more energy can be saved and used for other processes. Nonetheless, despite their advantages, more research and development of these concepts is needed in order to achieve higher efficiencies that can compete with other concepts.

1.6 Different approach for high efficiency solar cells

Rapid progress of PV technology has lead to the investigation of new alternatives for the currently existing Front Back Contacted so]lar cells (FBC) solar cells Figure 1.11(a). A new concept is developed with both collecting diffused regions; back surface field (BSF) and emitter. and electrodes placed on the rear side of the silicon substrate. This design of solar cells is commonly called interdigitated back contact solar cells (IBC). The schematic of this concept is presented on Figure 1.13.

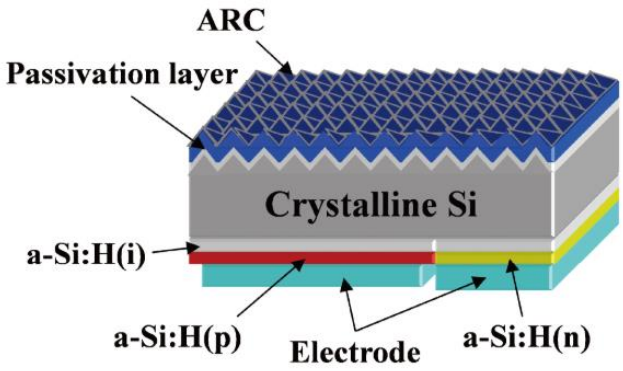


Figure 1.13 Schematic of IBC solar cell [50].

The IBC solar cell design has many advantages over conventional FBC solar cell concept:

- In IBC solar cell concept shadow losses are suppressed due to the lack of front electrode. which corresponds to the gain of 5-7 % of photogenerated current with comparison to the conventional PV cells [51].
- In IBC solar cell the electrical optimization of the backside and optical optimization of the front side of the solar cell are separated. In contrary to the conventional FBC cell design. IBC is not constrained by the trade-off between the sheet resistance of front emitter (in order to keep the series resistance on the satisfactory level) and the recombination J_o of the same front emitter to keep profitable quantum efficiency and high Voc [52].
- IBC solar cell has relatively low series resistance because every electrode can cover almost 50 % of the back surface of the solar cell.
- The front side of IBC where largest concentrations of minority charge carriers are placed. may be optimized to reach low surface recombination and as a result low J_o [52].

Nonetheless, despite many advantages, the design of IBC solar cells is more complicated and difficult with comparison to FBC solar cells. In the FBC solar cells most of the charge carriers are generated in the vicinity of the junction. In the rear junction cell (IBC solar cells). photogenerated charge carriers are generated near the front surface. As a result, they have to travel through the thickness of silicon wafer with the majority charge carriers towards the BSF or bulk contact and minority charge carriers towards the emitter. Consequently, the efficiency of IBC cells is very susceptible to front surface recombination. Accordingly, IBC requires long minority charge carrier's lifetime and low surface recombination in order to achieve decent efficiency.

Therefore, IBC solar cell design should provide:

- Diffusion length of minority charge carriers of about 5-10 times greater than solar cell thickness [51].
- Equivalent to a charge carrier lifetime greater than 1 ms.
- Front surface recombination parameter J_o smaller than 10 fA/cm^2.

Consequently, the IBC solar cell fabrication process is more complex and requires:

- Two of three doping steps; emitter, BSF and possibly front surface field (FSF).
- Alignment and pattering of the p-type and n-type region on the same side of the wafer with their correlating contacts windows and metal contacts (photolithography).

- Sophisticated cleaning procedures and high-quality contamination control as well as high accuracy lithography processes.

1.7 Motivation

In section 1.1 was pointed out that the demand for energy and electricity is following an increasing trend. The positive outcome of this phenomenon is the fact that the generation of energy from renewable energy sources is also increasing, only in 2018, the generation increased by 4 %, and this increasing trend will rather remain. According to the estimations 60 % of the total renewable energy generation will be represented PV technology [9]. Nonetheless, renewable energy sources still have to compete with fossil fuels. Consequently, it is crucial to focus on the competitive price of renewable technologies; decrease their LCOE (Levelized Cost of Electricity). In modern PV systems, the lowest efficiency of all components is represented by PV panels. Crystalline silicon PV panel e.g manufactured by Sharp reaches an efficiency of 17% [53], which is still lower than the efficiency of the other PV systems components, like charge controllers, inverters, that are a part of Balance of the System (BOS) elements. Therefore, the boost in PV panels efficiency may have significant influence on PV Technology position on future energy markets. The higher the efficiency of energy generators, in the case of PV technology that are the PV panels, the more interest in these solutions and consequently the better development of renewable energy technologies.

Currently, the PV cells are produced form the materials of outstanding bulk quality. Consequently, the recombination, loss mechanism in the bulk does not have a significant effect on PV cell performance. Hence, the open-circuit voltage of such cells is high. On the other hand, the presence of the dangling bonds considerably lowers the PV cell performance. Therefore, many passivation mechanisms are in a point of interest in order to increase the PV cell efficiency.

The objective of this project is a study of poly-Si passivation contact (poly-SiC_x) that is alloyed with carbon. Thanks to the carbon incorporation this structure is more resilient to blistering that may occur as the result of hydrogen effusion from the a-Si:H structure during the annealing process. The ruptured blisters can provide a diffusion path for the metals during the metallization step, which will further deteriorate the passivation quality[49]. Moreover, Si-C alloys provide advantages of the high stability to wet chemistry that is commonly used for cell fabrication [45]. It is also crucial to mention that hydrogen-carbon bonds are more stable than hydrogen-silicon bonds [54]. Besides, poly-Si can provide a strong doping area that will further enhance carrier selectivity.

Ingenito et. al investigated that that for Si-rich SiC_x (n) layers minority carriers are better shielded by the in-diffused region from the electronic defects at SiO_x /c-Si interface. This results in a very high value of i-Voc-almost 700 mV that is achieved without hydrogenation. Besides the addition of carbon to the silicon results in the fact that the material is more resilient to blistering after the deposition on the silicon oxide. Blistering is a direct result of hydrogen effusion that provides additional areas for the metals incorporation during the metallization process what consequently deteriorates the passivation process.

Concluding, enhancing the PV cell efficiency with alloyed materials like SiC_x can be very meaningful for the development of high-efficiency poly-SiC_x PV panels. This is because carbon incorporations hinder the blistering of the material and allows for tuned bandgap bending that depends on the carbon content. Besides, SiC_x provides also wet-chemical stability during the

manufacturing process which makes the production process of PV cells less complicated and leaves the open window for further improvement.

1.8 Thesis objective

The objective of the presented master thesis is the fabrication of high-efficiency solar cells through the implementation of poly-SiC_x passivating contacts. In order to successfully fabricate the high-efficiency solar cell many experiments must be performed which main aim is the analysis of the effect of the material properties, and applied passivation contact on the cell performance. Consequently, in order to obtain satisfactory results various fabrication parameters must be checked; deposition processes, annealing time and temperature, material etching tests. Moreover, crucial importance on the cell parameters has the applied hydrogenation process, whose influence was also tested. Through finding a balance between many variables and constraints of the fabrication process FBC solar cells with poly-SiC_x passivating contacts have been manufactured. Besides, first attempts of fabrication of IBC solar cells also have been taken out, the fabrication flow chart for IBC solar cells with poly-SiC_x passivating contacts have been developed as well as first fabrication attempts-etching tests have been performed.

The fundamental research questions of this thesis are:

- What are the possibilities for improvement of SiO_x/poly-SiC_x passivating contacts?
- How does the thickness of the deposited buffer layer affect the passivation quality of poly-SiC_x passivation contacts?
- What is the influence of PECVD deposition parameters on (i)a-Si:H layer applied on poly-SiC_x passivating contacts?
- What is the difference between the passivation results obtained via the deposition of the buffer layer through LPCVD and PECVD method, and what is the origin of this difference?
- What is the effect of the post-annealing process of solar cells on the final cell performance?
- What is the optimum ratio of SiH_4/NH_3 gases used for the deposition of SiN_x layer?
- What is the optimal etching time for wet etching of poly-SiC_x contacts in terms of the fabrication of the IBC solar cells?

1.9 Thesis outline

Presented thesis work consists of 6 chapters, whose aim is the optimization of poly-SiC_x passivating contacts and consequently successful fabrication of FBC and IBC solar cells with the implemented beforementioned contacts.

Chapter 2 provides details of the followed experimental method. Firstly, the detailed processing techniques are provided as well as the information about the equipment-tolls which were used. Moreover, the characterization techniques are presented, where the equipment applied for the determination of material properties and electrical, and optical properties is briefly introduced.

In chapter 3 the poly-SiC_x passivation contacts are tested on symmetrical structures as well as on cell precursors. Consequently, in this chapter, various deposition parameters are checked in order to further optimize the passivation properties of the studied structure. Moreover, in chapter 3 the optimization of hydrogenation gas content and its influence on the studied passivation contacts is

presented. In chapter 4, studied poly-SiC_x passivation contacts are implemented on a device-level-FBC solar cell. In this chapter solar cells with different configurations are checked.

The objective of chapter 5 is an intensive study of other concept-IBC solar cells. Firstly, in chapter 5 a photolithography is introduced - a method which is crucial for the fabrication of IBC solar cells. Afterward, the fabrication method for IBC with poly-SiC_x passivation contacts is presented. Finally, etching tests, on studied material- doped a-SiC_x:H and (i)a-Si, are performed.

In the last 6 chapter, the conclusions of the thesis work are presented, the most important aspects are briefly summarized in order to provide better understanding of the presented topic and the progress made through this work. Moreover, the outlook of the possible ways for further improvement of fabricated poly-SiC_x solar cells is given which can be consequently an entry point for a further research.

2

Experimental methods

This chapter focuses on the fabrication and characterization methods of the assembled samples. Every step of wafer processing is briefly introduced and described. The working principles of the used equipment and process parameters are also discussed. The solar cell fabrication order follows the list provided in this chapter. Finally, all of the characterization techniques used for the analysis of the manufactured samples are also introduced.

2.1 Fabrication process

In order to provide high quality of the manufactured samples experiments were performed in a clean working environment. Consequently, the fabrication processes were carried out at EKL and Kavli clean rooms located at the TU Delft campus. Most of the fabrication processes were performed in CR100 and CR10k, where the number 100 and 10k refers to the clean room classification. Class 100 area is defined as space where the maximum number of 0.5-µs-sized particles per cubic meter do not exceed 100 molecules. Consequently for class 10k maximum allowed amount of particles is 10 000 [55].

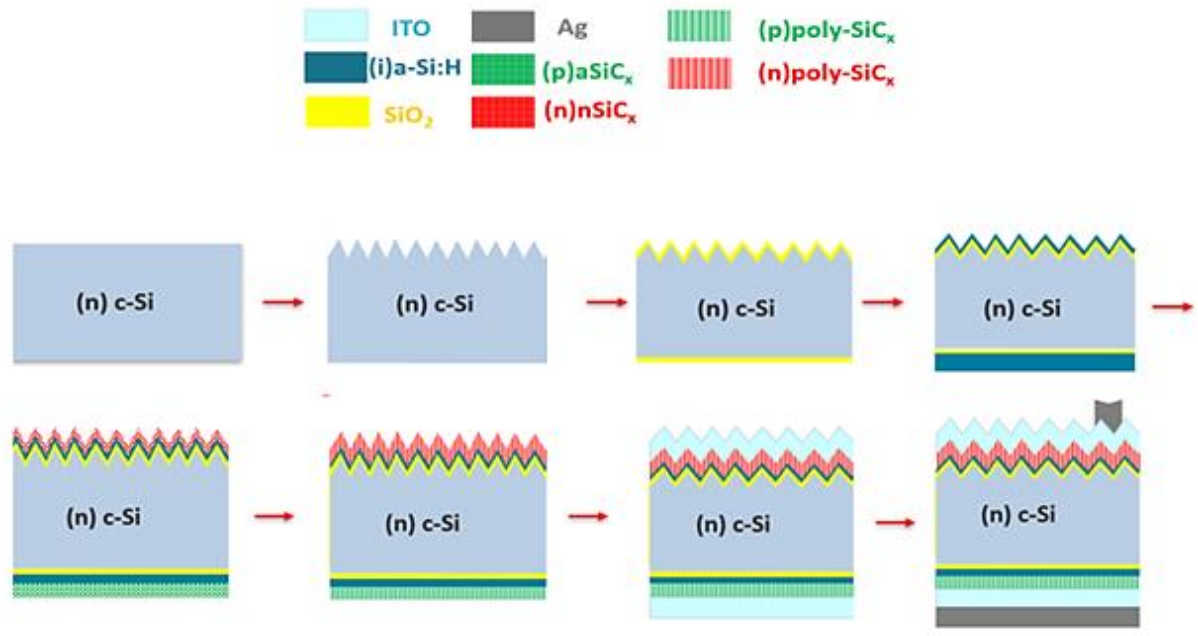


Figure 2.1 Schematic sketch of the fabrication process of the FBC solar cell with poly-SiCx passivating contacts.

In Figure 2.1 is presented the fabrication process of front-back contacted (FBC) solar cells and a schematic of the deposited layers. Besides, Table 2.1 is a brief summary of all deposited layers and equipment that was used for the deposition.

Table 2.1 Specification of the layers deposited during the fabrication process.

Material deposited	Tool	Used material	Pressure	Temperature
a-SiC_x	LPCVD furnace *TEMPRESS SYSTEMS*	SiH_4 45 sccm	0.2 mbar	580 °C
a-SiC_x:H	PECVD *Elettrorava Amor*	SiH_4 45 sccm	0.7-1.2 mbar	180-220 °C
(p)a-SiC_x:H	PECVD *Elettrorava Amor*	SiH_4 20 sccm CH_4 45 sccm B_2H_6 5 sscm	0.7 mbar	180 °C
(n)a-SiC_x:H	PECVD *Elettrorava Amor*	SiH_4 20 sccm CH_4 45 sccm PH_3 5 sccm	0.7 mbar	180°C
SiN_x	PECVD *Plasmalab80Plus*	NH_3 10-30 sccm SiH_4 10-30 sccm	0.87 mbar	400 °C
ITO	Sputtering *Zorro*	In_2O_3 90% SnO_2 10 %	0.022 mbar	196 °C
Metallization	SP	Ag		

2.1.1 Silicon wafer material

We use for this project phosphorus doped crystalline silicon (c-Si) wafers produced by *TOP - SIL*. As the wafer bulk is used the n-type material. Material properties of processed wafers are summarized in Table 2.2 The choice of n-type semiconductor is motivated by two important differences between p-type and n-type semiconductors. Firstly, considering wafers with the proportionate defect and dopant concentration, the carrier lifetime of n-type silicon is higher than that of p-type Si [16]. These properties can be related to the transition metals impurities within the Si lattice [56] that have increased the capture cross-section for electrons over holes [57]. Secondly, oxygen impurities caused by the wafer fabrication specifically affect the minority carrier lifetime of p-type Si. The oxygen presence leads to the formation of boron-oxygen complex under the light exposure or excess carrier injection [58],[59].

Table 2.2 c-Si material properties as given by the producer.

Parameter	Value
Diameter [mm]	100 +/- 2
Thickness [µm]	260≃300
Doping	n-type
Specific resistivity	1-5 Ω·cm
Orientation	<100>
Resistivity [ohm·cm]	1-5
Finish	Polished

We have used c-Si wafers with <100> surface orientation which means that its surface is normal in the <100> direction. In this type of silicon surface, every Si atom has two valence electrons pointing to the front and two back bonds. On the other hand, another type of Si material, the <111> surface has three back bonds and one valence electron that is pointing towards the normal of the plane. The two structures are presented on Figure 2.2. The reason behind selection <100> orientation is the fact that for the fabrication of FBC solar cells one of the surfaces (front side of the solar cell) must be textured and have <111> orientation. Consequently, after the texturing process the obtained wafer structure has one side with <100> orientation and the second, textured side with <111> orientation. Moreover, some of the experiments like passivation tests are performed on double side flat wafers as a result for these experiments wafers with <100> orientation are used.

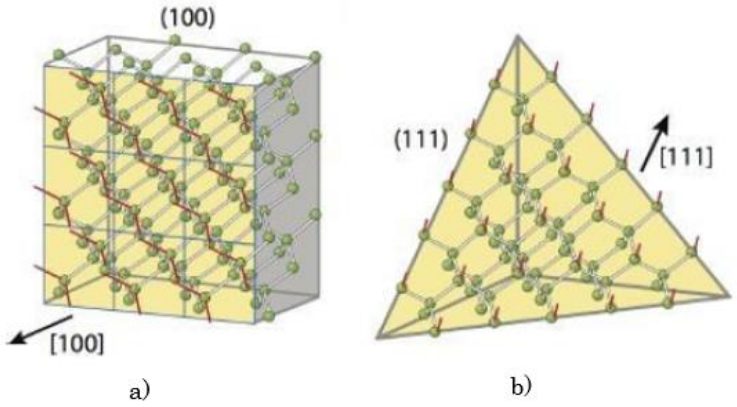


Figure 2.2 Schematic representation of (a) <100>, and (b) <111> silicon surfaces orientation [24].

2.1.2 Wafer cleaning

Before any process, the wafer must be properly cleaned in order to remove inorganic and organic contamination from the surface. Wafer cleaning consists of many standardized sub-processes [60]. Firstly, the wafer must be immersed in a 99% HNO_3 solution and later has to be washed for 10 minutes in a deionized (DI) water. Subsequently, the wafer is dipped for 10 minutes in 69.5% HNO_3 solution at the temperature of 110 °C and once more washed off in DI water for 10 minutes. The listed steps complete one cleaning sequence, that ensures the removal of inorganic and organic contamination [61]. In order to provide excellent cleaning of the wafer surfaces, the aforementioned sequence is repeated three times.

Unfortunately, during the cleaning, the native oxide layer is formed on the wafer surfaces. This native oxide is not a desirable layer since later on the silicon surface will be grown the silicon oxide of excellent quality, which should not be disturbed by any other deposited layers. Consequently, in order to remove the native oxide formed during the cleaning process, the wafer is dipped in 0.55% hydrofluoric acid (HF) until the surfaces become completely hydrophobic[1]. Subsequently, the wafer is washed out for 4 minutes in DI water and finally, isopropyl alcohol is added for approximately 1 minute to dry the wafers. The last three steps are known as a Marangoni process and have to be

[1] An hydrophobic surface has the property of repelling water, i.e. it cannot easily become wetted in contact with water. This phenomenon is the result of the unbalanced molecular forces at the water/solids interface that causes surface tension [120].

done just before the further processing of the wafer. As mentioned earlier, Marangoni guarantees a bare surface for the subsequent silicon oxide growth that will be performed in the next step.

2.1.3 Chemical oxide growth

The subsequent step of the manufacturing process is the growth of the thin silicon oxide (SiO_x) layer. The objective of this step is to achieve the ultra-thin SiO_x layer with a thickness of ~1.5 nm. In this project, we grow SiO_x via wet-chemical method using the so-called Nitric Acid Oxidation of Silicon (NAOS). Consequently, in order to obtain this ultra-thin layer, the wafer is immersed in a 69.5% HNO_3 solution for 60 minutes. This step is performed immediately after the native oxide removal via Marangoni. Finally, after the oxidation in NAOS the wafer is immersed in DI water for 4 minutes.

It is important to note that during the process the formed thin oxide layer has a thickness in a range of 1.2-1.5 nm [62]. For this thickness it is assumed, that SiO_2 is homogenous in thickness, and hence has a very low leakage current density. The one disadvantage of the analyzed method is the fact that silicon oxide grown by the use of NAOS has lower thermal stability with comparison to the other grown methods, which may result in SiO_2 breaking during the high temperature annealing processes [63]. Despite this one loss wet chemical oxidation has also significant advantages. The NAOS is very simple in application and is characterized by a very low thermal budget [64]. This a big pros over the other oxidation methods that require temperatures range of 600-700 °C [65].

2.1.4 Deposition methods

Low pressure chemical vapor deposition

Silicon-based layers can be deposited through many methods. One of them is Low Pressure Chemical Vapor Deposition (LPCVD) (Figure 2.3). This technique enables the deposition of layers with a thickness varying from a few nanometers up to few micrometers.

In LPCVD the wafers are processed in low-pressure regime (10-1000 Pa) and relatively high temperature up to 600°C [66]. The significant advantage of this process is the fact that layers deposited by LPCVD are of high homogeneity and purity which is crucial for the performed experiments. Besides, layers that are deposited through LPCVD are free of pin-holes [67]. This guarantees the tunnel oxide layer protection in the following chemical treatments and deposition steps.

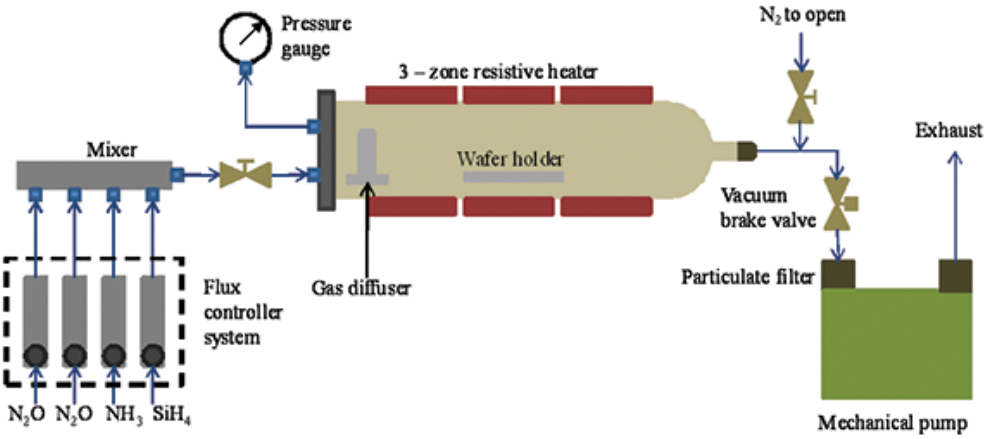


Figure 2.3 Schematic view of a LPCVD system [68].

The LPCVD used in the presented project is the tube furnace manufactured by *TEMPRESS SYSTEMS*. This device was used in order to deposit intrinsic amorphous silicon films [(i)a-Si]. The (i)a-Si layer was deposited according to the optimized recipe, which parameters are: deposition rate 2.16 nm/min, temperature 580 °C and pressure of 20 Pa. The used gas is silane-SiH_4 with a flow ratio of 45 standard cubic centimeters per minute (sccm). The recipe includes a post-deposition annealing step at 600 °C to release the stress of the layer.

Plasma enhanced chemical vapor deposition (PECVD)

Plasma-enhanced chemical vapor deposition (PECVD) is the second deposition technique used in the project. PECVD is a widely used process for silicon thin films deposition, where dissociation energy of the gas species is not only temperature driven but it is obtained via a gas discharged that created a so called plasma. This deposition technology is preferred in situations when it is crucial to keep the low temperatures of the wafers while achieving desired film properties. Figure 2.4 depicts the PECVD reactor scheme.

In PECVD processes, deposition is possible due to the introduction of reactant gases between parallel electrodes a grounded electrode (lower one) and an RF-energized electrode (upper one). The capacitive coupling between the electrodes energizes the reactant gases into a plasma, which consequently induces a chemical reaction and finally the reaction product is deposited on the substrate. The substrate, which is placed on the lower, grounded electrode, is typically heated to 250°C -350°C. The heating temperature depends on the specific film requirements.

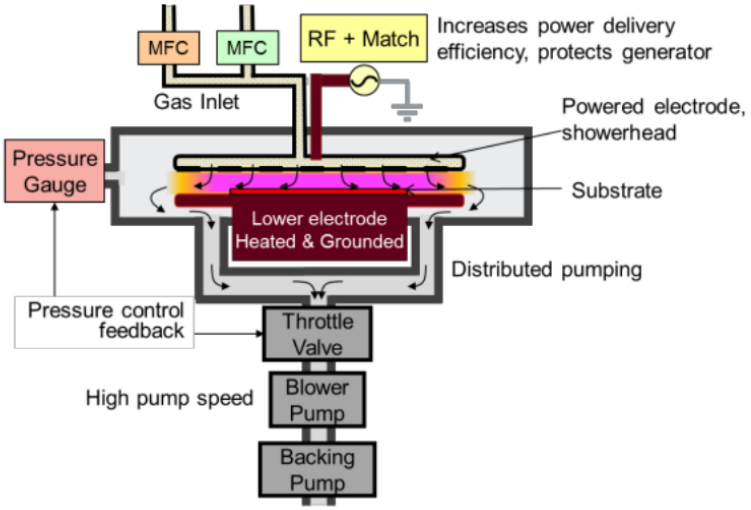


Figure 2.4 PECVD chamber [66].

PECVD process consists of the subsequent four fundamental steps:

1. Creation of plasma generating of active gas species
2. The reaction at the target substrate surface
3. Pump down of the reaction by-products

In this project, the PECVD device *AMOR* assembled by *Elettrorava* is used. This equipment consists of four deposition chambers dedicated to specific materials in order to prevent cross-contamination of deposited layers. An additional chamber is used to `flip` the processed wafer and allows deposition on both sides of the substrate without breaking the vacuum. Table 2.3 provides the details about the deposited layers and the conditions of the deposition.

Table 2.3 Specification of the layers deposited through PECVD.

Layer	Gas used	Gas flow ratio	Pressure	Temperature
a-SiC_x:H	SiH_4	45 sscm	0.7-1.2 mbar	180-220 °C
(p)SiC_x:H	SiH_4 CH_4 B_2H_6	20 sscm 45 sscm 5 sscm	0.7 mbar	180 °C
(n)SiC_x:H	SiH_4 CH_4 PH_3	20 sscm 45 sscm 5 sscm	0.7 mbar	180°C

2.1.5 High Temperature Annealing

High-temperature annealing is the following step of the wafer processing. The objective of this process is to activate the dopants which has been deposited in the earlier steps [54] and to crystallize the (i)a-Si:H/doped-a-SiC_x:H layer in order to obtain poly-SiC_x layers. Poly-SiC_x layers characterize outstanding electrical and optical properties with comparison to the amorphous layers. Additionally, the crystallized layers show lower series resistance than the amorphous ones, which is a result of the high doping efficiency [69]. In fact, in polysilicon structure, it is easier for dopants

to move than in a disordered crystalline lattice of the amorphous silicon. Nonetheless, it is important to note that the annealing process is very sensitive with respect to the p-type layer. There is a high possibility, that some boron atoms will diffuse too far into the c-Si bulk. This unprofitable phenomenon may lead to the suppression of the passivation effect, which is the critical objective of this project. Consequently, it is crucial to focus on an optimum annealing process that will provide favorable conditions for the dopant profile between c-Si and poly-SiC_x layers.

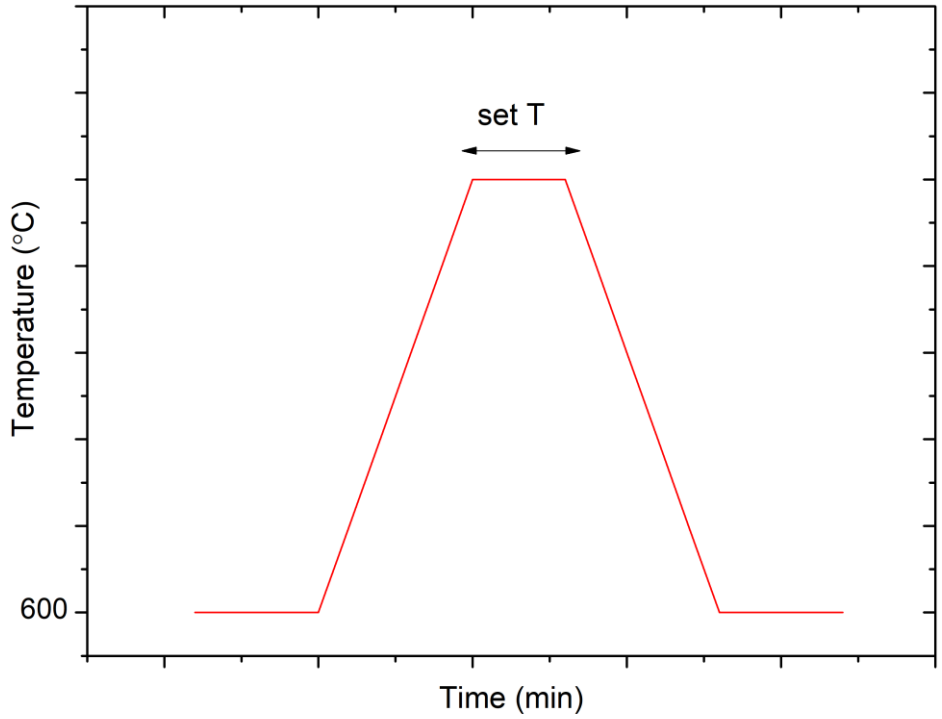


Figure 2.5 Temperature ramping during the thermal annealing.

The equipment that was used in this project is a furnace manufactured by *TEMPRESS SYSTEMS* with a similar structure as discussed in section 2.1.4. The annealing process was performed under N_2 atmosphere at temperatures between 775°C-900°C and durations between 0-5 minutes. On Figure 2.5 is depicted the relation between the time of the process and the setup annealing temperature and time.

2.1.6 Hydrogenation

The hydrogenation step is one of the passivation techniques that are applied in this project. Hydrogenation is considered as a chemical passivation method (section 1.5), since it saturates the unsatisfied dangling bonds or surface silicon atoms with hydrogen atoms. The hydrogenation consists of two steps: deposition of a H-rich capping layer (SiN_x) and a subsequent forming gas annealing (FGA).

The SiN_x layer was deposited through the PECVD technique. *Plasmalab80Plus* device provided by *Oxford Instruments* was used. It is important to note, that for this process both radio frequency (RF) and LF generators were applied. Used gases were ammonia (NH_3) and silane (SiH_4). The

selected conditions were; temperature of 400 °C and pressure of 87 Pa. The hydrogen that passivates the material comes from the aforementioned gases which have a high hydrogen content.

The FGA annealing treatment was performed in order to release H atoms incorporated in the H-rich SiN_x layer and provide extra hydrogen[70]. The machine used for FGA is a furnace manufactured by *TEMPRESS SYSTEMS*. FGA was carried out in the mixture of H_2 and N_2 environment at a temperature of 400 °C for 30 min. The hydrogen gas flow ratio was kept at a level of 400 standard cubic centimeters per minute (sccm).

2.1.7 Transparent conductive oxide layer

Transparent Conductive Oxides (TCO) are used at the front side and back side of the solar cells. In this project, the Indium Tin Oxide (ITO) layer previously developed by the other members of the PVMD group was used. This layer consists of 90% of In_2O_3-Indium Oxide and 10 % of Tin Oxide.

Before the ITO deposition metal masks were used on both sides of the wafer, whose main role is to define the structure of the cells on the wafer. ITO was deposited in the places defined by the mask through the sputtering method. The chamber conditions for this process were set as: sample temperature 110 °C, pressure 2.2 10^{-5} bar. These conditions have been tested in the past by the other members of PVMD group. The thickness of applied ITO is changing with regard to the back and front side. The front side of ITO layer is thinner-75 nm and the rear is 150 nm. These thickness parameters guarantee satisfactory light trapping and carrier transport.

2.1.8 Metallization

The last step of the cell production is the metallization. Metallization plays both electrical and optical roles in solar cell performance. Optically, the gridline width impacts cell shading, which consequently influences the short circuit current. Electrically metallization affects the series resistance through the contact and gridline resistances, which influences the fill factor [71].

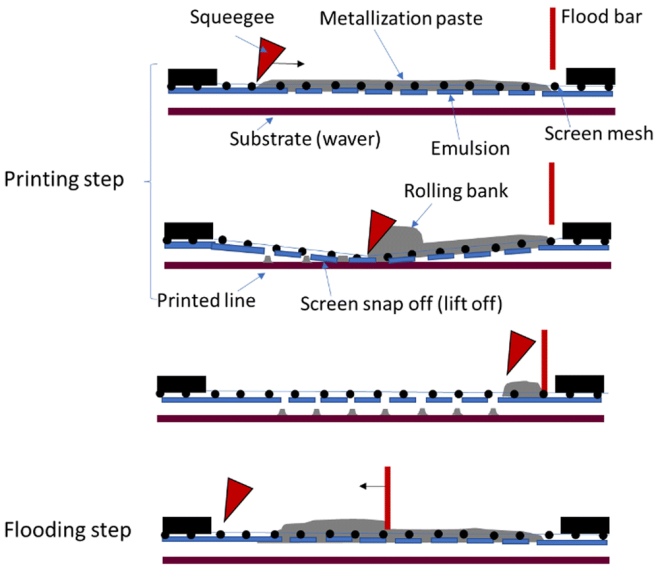


Figure 2.6 Screen Printing [72]

In this project, the back of the cell has a full area contact and the front metallization has a front metal grid. As it was mentioned before, the metallization step must be correctly designed, since the wider finger spacing causes higher FF due to the lower resistance for the lateral transport. On the contrary, a smaller finger spacing means that more fingers must be placed on the front side of the cell which causes significant shading losses [73]. Consequently, the metal coverage selection is a trade-off between optical shadowing and electrical resistance. Higher metal coverage might be beneficial for the fill factor but will penalize the current.

Solar cell metal contacts are created using screen printing (SP) (Figure 2.6). The SP method used in this project applies a low temperature silver paste. Thanks to this paste the collector gridlines; fingers and bus bars are created. Silver (Ag) is firstly heated till the room temperature. Subsequently is applied on the screens which define the final structure of the cells. The screen that is selected for the cell metallization is depicted in Figure 2.7 Different cells have various metallization coverage that varies from 3.2% to 4.4 %. After the screen-printing cells are annealed in the oven at the temperature of 200 °C in order to dry the paste and harden the structure.

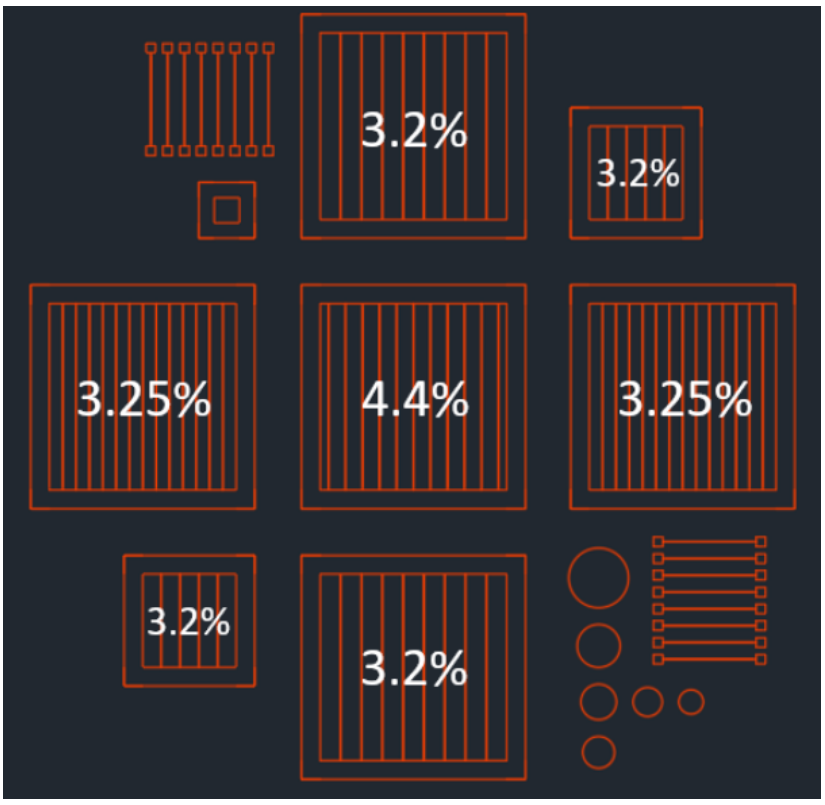


Figure 2.7 Metallization mask scheme.

After the first measurements and analysis of the cells the post-annealing process is performed. Every cell is annealed at heating-plate at temperature of 350°C for a duration of 5 minutes on each side.

2.2 Characterization methods

In this section, we describe the characterization tool and techniques used to evaluate the material quality for the optimization of the fabrication process and the performance of the manufactured devices. The correct identification and optimization of the material are crucial for the efficient performance of the manufactured solar cells, consequently, firstly the tools that characterize the used material are presented. Subsequently, device characterization equipment is introduced that enables extraction from the device its parameters.

2.2.1 Material Characterization

This subsection focuses on the material characterizations that were performed. The objective of these methods is to inspect the material composition and bonds present in the deposited layers.

Fourier-transform infrared spectroscopy

Fourier Transform-Infrared Spectroscopy (FTIR) is an analytical method that is used to determine the absorption of infrared radiation (IR) by the sample material as function of wavelength. The IR absorption bands classify molecular structures and components [74].

Once the material under investigation is irradiated with IR radiation, absorbed infrared radiation usually excites molecules into a higher vibrational state. The wavelength of light absorbed by a specified molecule is the function of the energy difference between the at-rest and the excited vibrational states. Wavelengths that are absorbed by the sample are typical of its molecular structure [74].

FTIR spectrometer uses an interferometer to adjust the wavelength from a broadband IR source. The detector measures the intensity of transmitted or reflected light as a relation of its wavelength. The signal obtained from the detector is the interferogram, which must be examined with software using Fourier transforms to get a single-beam infrared spectrum. The FTIR spectra are usually depicted as plots of intensity against wavenumber (cm^{-1}). The intensity can be depicted as the percentage of light absorbance or transmittance at each wavenumber.

To classify the material investigated, the unknown IR absorption spectrum is compared with the standard spectra of software databases or with a spectrum acquired from a known material. The equipment used during this project is *Nicolet 5700* manufactured by *Thermo Fisher*.

Spectroscopic Ellipsometry

In this section are presented the electrical and optical characterizations that were carried out. Some of the characterization techniques were performed on the wafer while others on quartz glass substrates. Nonetheless, most of the measurements were accomplished on silicon wafer substrates which enable electro-optical and material characterization of deposited layers.

Ellipsometry measures the change in the polarization of the incident light compared to the light detected after being reflected by the sample (Figure 2.8). Hence, ellipsometry is mainly used to

obtain the thickness of the analyzed film and its optical constants. Ellipsometry basically focuses on the relation between coefficients of reflection; r_p and r_s . Where p-polarized light coincides with the electric field parallel to the plane of incidence and s-polarized to the plane perpendicular to the plane of incidence. The change in polarization; ρ-reflectance ratio is described by the use of equation (2.1) where Ψ is the amplitude ratio and Δ is a phase difference.

$$\rho = \frac{r_p}{r_s} = tan\Psi e^{\Delta} \qquad (2.1)$$

Once the measurement is performed the data must be fitted to the already existing model on a base of which we can build the model that is relevant with measured samples and allow us to its analysis for example layer thickness and the optical properties.

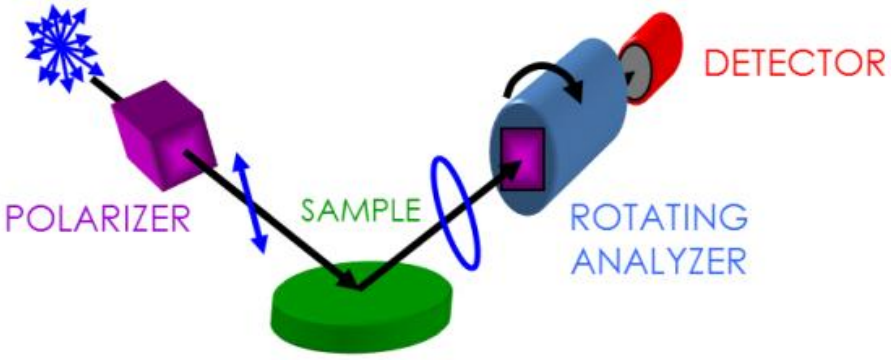


Figure 2.8 Spectral Ellipsometry setup [75] .

The tool used in this project is *EC-400* manufactured by *J.A Woolam Co. Inc*. Measurements were mainly performed on layers which were deposited on a wafer substrate. This allowed finding the thickness of the deposited layers that were further optimized for the best possible cell results. All of the measurements were carried out at the angles that are close to the Brewster Angle[2]. At this angle the difference between p-polarized and s-polarize light is the biggest. In all performed measurements the Brewster Angle was set a value between 65° and 75°.

2.2.2 Device characterization

This section focuses on characterizations carried out on different types of samples: symmetrical samples used for passivation tests and completed solar cells. Characterization techniques performed on symmetrical samples provide beneficial information about the optimization of the deposited layers that can be adopted on the device level. Besides, characterization techniques

[2] Brewster Angle- angle of polarization at which the light with specific polarization is perfectly transmitted through a transparent surface. Additionally, no reflection occurs at this angle. If an unpolarized light is incident at this angle light is subsequently reflected from the surface and perfectly polarized [121].

mentioned in this section were also used to estimate the performance of the analyzed samples during the crucial steps of the fabrication process.

Photoconductance lifetime measurement

Wafer passivation quality can be defined thanks to the effective minority carrier lifetime (τ_{eff}). The minority carrier lifetime is represented by the average time than an excess minority carrier needs to recombine. Effective carrier lifetime strongly depends on the recombination mechanisms that occur on the wafer surface and its bulk (section 1.4). As was mentioned before in section 1.4 c-Si substrate is of great quality and the recombination takes place mainly on the surface of the wafer.

*Sinton WCT-120 Lifetime Tester (*Figure 2.9) was used to extract effective minority carrier lifetime (τ_{eff}) and implied open circuit voltage (i-Voc). This device is equipped with the filtered xenon flash lamp which provides a light within a range of red color. The light flash entails the generation of excess carriers in the wafer bulk. Subsequently, these carriers recombine until the equilibrium is reached. Other equipment that is used in *Sinton WCT-120* is an eddy-current conductance sensor. This sensor measures the light intensity that is provided by the aforementioned lamp and the wafer photoconductance.

Figure 2.9 Sinton WCT-120 lifetime Tool [76]

Basing on the assumption that the carrier generation of electrons and holes is uniform and equal, the increase of conductance can be calculated by the equation (2.2).

$$\sigma L = q(\Delta p \mu_p + \Delta n \mu_n) W \qquad (2.2)$$

Where q is the elementary charge, Δp and Δn are the excess charge carriers (holes and electrons) and μ_n and μ_p are the charge carriers mobility, that are the function of injection level and doping. Finally, W is the wafer thickness [77].

In order to find the equation for charge carrier generation it is crucial to start from the continuity equation for n-type semiconductor, that is given by the relation (2.3)

$$Dp\frac{d^2(\Delta p)}{dx^2} - \mu_p E\frac{d(\Delta p)}{dx} + G - \frac{d\Delta p}{\tau_e ff} = \frac{d\Delta p}{dt} \tag{2.3}$$

Assuming no external electric field and a uniform distribution in the excess carrier the continuity equation for the n-type semiconductor has the following form (2.4)

$$G - \frac{d\Delta p}{\tau_{eff}} = \frac{d\Delta p}{dt} \tag{2.4}$$

From this equation it is possible to find an effective minority carrier lifetime (2.5)

$$\tau_{eff} = \frac{\Delta p}{G - \frac{d\Delta p}{dt}} \tag{2.5}$$

The equipment used in these tests *(Sinton WTC-120)* provides different modes for the calculation of the minority carrier lifetime. The quasi-steady-state mode (QSS) is used for the minority carrier lifetime below 100 µs. Quasi-Steady-State lifetime measurements depend on the number of carriers available when a steady light is flashing on the analyzed sample. It is estimated that the intensity of the flash differs slowly so that the number of carriers in the wafer is always at a steady state. Therefore, in the QSS mode it is assumed that $\frac{d\Delta p}{dt} = 0$. Consequently, the lifetime equation is given by the relation (2.6)

$$\tau_{eff} = \frac{\Delta p}{G} \tag{2.6}$$

The second available mode is a transient mode. It is valid for the lifetimes above 100 µs. In transient lifetime measurements, the carries will decompose overt their lifetime. Carriers are generated by a very short pulse of light and later the decomposition of the carrier density is measured with time. In a transient mode, it is assumed that G=0. This leads to the following equation for the lifetime of minority charge carriers (2.7).

$$\tau_{eff} = -\frac{\Delta p}{\frac{d\Delta p}{dt}} \tag{2.7}$$

Apart from the minority carrier lifetime, form the measured lifetime curve, it is also possible to extract the i-Voc and the dark saturation current density (J_o). i-Voc is measured at an injection level of (10^{15} cm^{-23}). The relation for the i-Voc is given by the equation (2.8).

$$i - Voc = \frac{k_b T}{q}\ln\frac{(N_d + \Delta n)\Delta n}{n_i^2} \tag{2.8}$$

Where k_B is Boltzmann constant, T is temperature N_D donor concentration and n_i intrinsic carrier concentration. It is important to note that i-Voc analysis does not take into account the metal-silicon recombination losses, consequently they provide the value of the upper limit of the solar cell voltage.

Illuminated J-V curve

The example (J-V) curve of the PV cell is depicted in Figure 2.10. Illuminated J-V curve characterizes the cell under Standard Test Conditions (STC); at illumination of 1000 W/m² and temperature of 25°C. From the J-V curve PV cell parameters can be extracted: open-circuit voltage (V_{oc}), short circuit current density (J_{sc}) and fill factor (FF). Our laboratory is equipped with is AAA Wacom WXS-156S solar simulator.

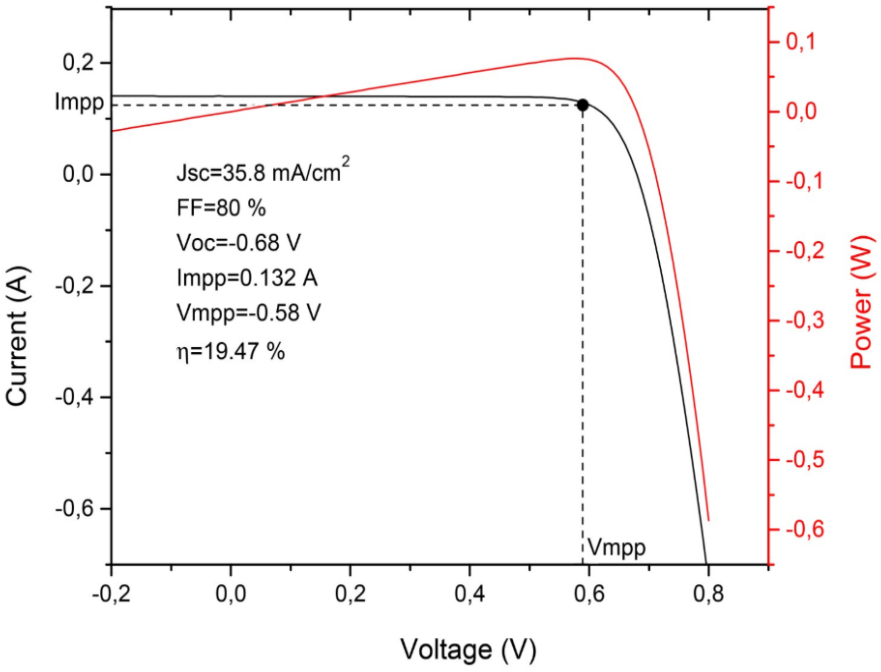


Figure 2.10 J-V curve of illuminated solar cell.

V_{oc} is the maximum voltage that the solar cell can deliver and is the voltage at which no current is flowing through the external circuit and is described by equation (2.9).

$$V_{oc} = \frac{k_{bT}}{q} \ln\left(\frac{J_{ph}}{J_0} + 1\right) \tag{2.9}$$

Where J_{ph} is the photogenerated current density, J_0 saturation current density and q is the elementary charge.

The short circuit current density (J_{sc}) it the maximum current delivered by a solar cell. J_{sc} is obtained from the equation (2.10).

$$J_{sc} = \frac{I_{sc}}{A} \tag{2.10}$$

Where I_{sc} is short circuit current and A is area of the measured solar cell.

The FF is the ratio between the maximum power (P_{max}) obtained by the solar cell and the product of the J_{sc} with the V_{oc} equation (2.11).

$$FF = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{oc}} \tag{2.11}$$

Where J_{mpp} is the current density measured at maximum power point (MPP) and V_{mpp} it the maximum power point voltage.

Having obtained all the parameters mentioned above it is possible to find the efficiency of the analyzed cell. The cell efficiency is given by the equation (2.12).

$$\eta = \frac{V_{oc}\, J_{sc}\, FF}{P_{in}} \tag{2.12}$$

External Quantum Efficiency (EQE)

The External Quantum Efficiency (EQE) measurement is carried out in order to acquire the response of the analyzed solar cell for photons with a specific wavelength or energy. EQE is determined as the ratio of charge carriers that were successfully collected by the solar cell to the number of incident photons on this cell.

EQE can be given as a function of energy or wavelength. EQE is commonly measured by illuminating the cell with the monochromatic (single wavelength) light and measuring the photocurrent (I_{ph}) through the cell. The wavelength dependent EQE is described through the equation (2.13).

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \tag{2.13}$$

Where $\Psi_{ph,\lambda}$ is the spectral photon flow incident and q is the elementary charge.

In this project, the EQE measurements were carried out with an in-house set-up. This equipment consists of a light source-xenon gas discharge lamp which has a broad spectrum that covers all the wavelengths that are relevant for Si solar cell performance (300-1200 nm). Other devices that build

this equipment are filter monochromator which allows selection of light with the very narrow wavelength, lock-in amplifiers, chopper and metallic probes.

From the EQE measurements, it is possible to extract short circuit current density of the cell. J_{sc} is calculated from the integration of EQE over the entire light spectrum as presented in equation (2.14).

$$Jsc = q\int_{300nm}^{1200nm} EQE(\lambda)\Psi(\lambda)d\lambda \tag{2.14}$$

3

Passivation optimization of the SiO_x/poly-SiC_x passivating contacts

The objective of this chapter is the optimization of the passivation quality of SiO_x/poly-SiC_x passivating contacts. In order to study different variable parameters of the fabrication step, each process is optimized and characterized separately. The first focus is on the effect of annealing temperature on the i-layer deposited by LPCVD or PECVD method. Subsequently, after the selection of the best annealing temperature, the i-layer thickness deposited by the LPCVD or PECVD method is optimized. For the PECVD deposition method, not only the optimization of (i)a-Si:H layer thickness is presented but also the optimization of deposition parameters such as pressure and temperature. Finally, in order to further enhance the studied passivation quality, the hydrogenation process is optimized applying variable stoichiometry of SiN_x layers. In particular, the gas mixture of SiN_x is varied to identify the optimal material composition and its influence on passivation quality.

3.1 Experimental details

This section briefly explains the different fabrication methods that were followed in order to obtain satisfactory passivation quality. Two different deposition methods were applied for the i-layer deposition: LPCVD and PECVD process (section 2.1.4). The passivation tests were performed on different passivation structures: double-side polished, double side textured and cell precursor structure. In order to clarify the fabrication, process a schematic of all analyzed structures and deposited layers is depicted in Figure 3.1. Each step of the fabrication process is described below for three different type of samples: symmetrical (a and b) and cell precursors (c).

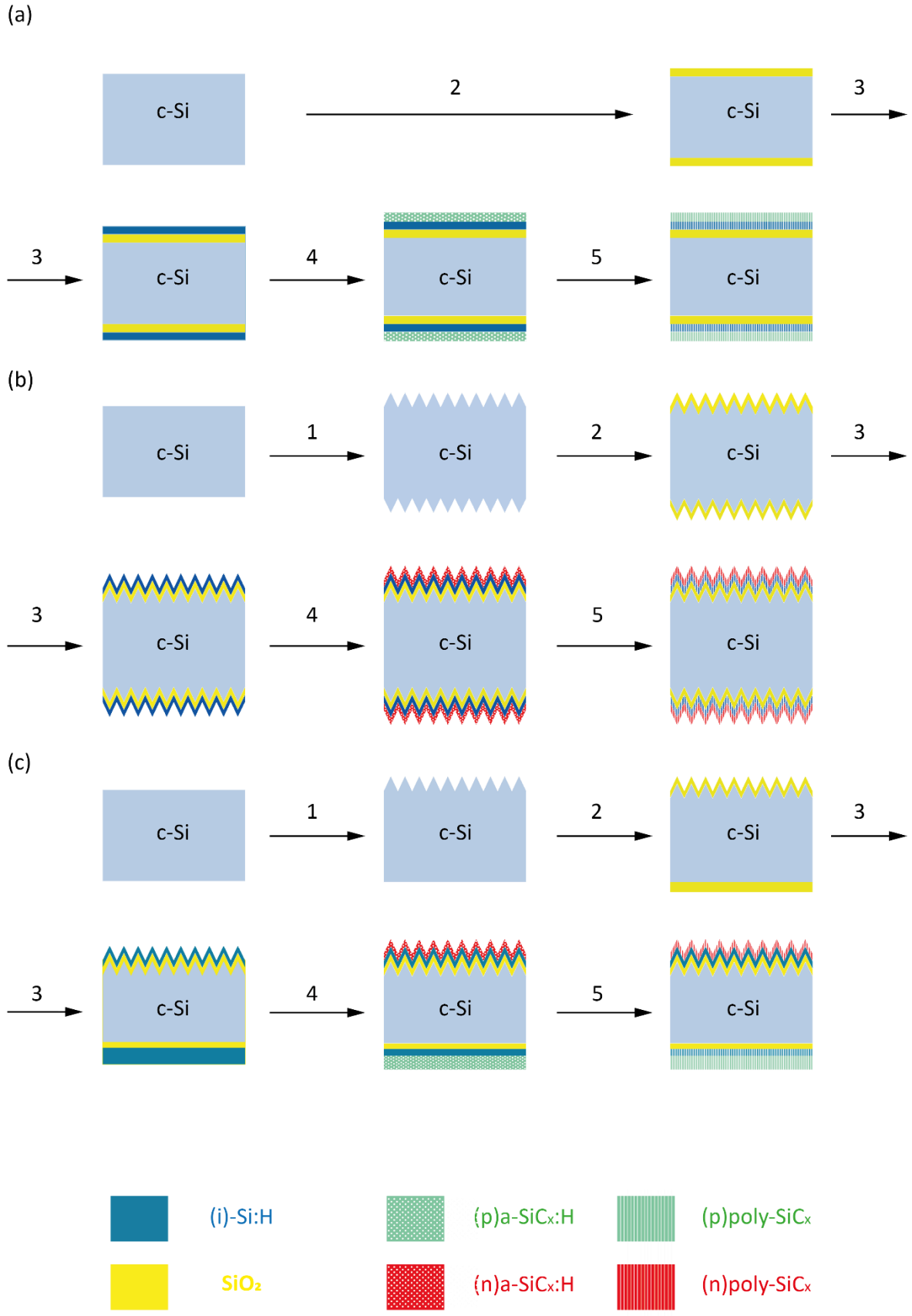


Figure 3.1 Schematic sketch of the passivation tests performed.

As it was mentioned in Chapter 2, the n-type Float Zone Si wafers are used for our study. Originally the wafers are double side polished and have initial thickness of 280 µm with <100> surfaces orientation. Starting from this material, only the most relevant fabrication steps are described below. Some necessary steps, like wafer cleaning are not included here in order to provide clarity of the presented process, for more details see section 2.1. Moreover, layers that have a protective function like SiN_x are not presented on Figure 3.1 as they are removed just after the texturing step.

1. The first fabrication step can differ regarding the wafer surface morphology. Some samples are polished, Figure 3.1(a), some are chemically textured on both sides Figure 3.1(b), other are one-side textured Figure 3.1(c).To obtain one-side textured wafers, SiN_x protective layer is deposited on one side of the wafer. The purpose of application of SiN_x is the protection of one side of the wafer from being textured. For double side textured samples, this step is not performed. Subsequently, the before mentioned texturing is carried out in a solution composed by Alka-Tex mixture and Tetramethylammonium in water and heated at 80°C. The wafers are then immersed in the BHF solution until the textured side will become hydrophobic and afterward, in poly-etch solution for approximately 2 minutes in order to achieve slight rounding of the pyramids. Finally, in case of one-side textured samples a final etching step in BHF solution is required to completely remove the SiN_x protective layer. All processes presented in step 1 one are not performed on double side polished samples Figure 3.1(a).
2. The tunneling oxide is formed chemically by dipping the wafer in 69.5 % HNO_3 solution for 1 hour. The resulting SiO_x layer has a thickness of approximately of 1.2-1.5 nm (section 2.1.3).
3. (i)a-Si film is deposited by the LPCVD or PECVD method. The difference between these two methods is described in section 2.1.4.
4. Doped a-SiC_x:H layers are deposited by PECVD from SiH_4 and CH_4 mixture. Doping gasses are B_2H_6 and PH_3 to obtain p-and n-doped layers, respectively.
5. High-temperature annealing is performed at different temperatures and times in order to crystallize the amorphous layers and activate the dopants. Annealing temperature and time are varied to find the optimum parameters for the passivation. After the annealing, the hydrogenation step with different gas contents is performed in order to deposit the SiN_x layer with different hydrogen concentration. Subsequently, the FGA treatment is carried out at a fixed temperature of 400 °C for 30 min in a tube furnace. Finally, the SiN_x capping layer is etched away completely by dipping the wafers in BHF solution for approximatively 20 min.

3.2 Effect of annealing temperature and duration

As it was already mentioned in Chapter 2, the annealing process has a great influence on passivation results. This step consists in the crystallization of the deposited (i)a-Si, (p)a-SiC_x and (n)a-SiC_x layers which result in the poly-SiC_x structure. Besides, the annealing process is responsible for the activation of dopants and their diffusion into the c-Si absorber [78]. Finding the correct annealing temperature and time is crucial for the passivation of the solar cell since too high annealing temperature and too long annealing time may be a reason for an excessive diffusion of dopants in c-Si [54]. This can be the origin of the band bending, which has a deteriorated influence on solar cell performance, as the high diffusion of dopants moves away the band from the Fermi level and consequently the material conductivity is reduced. Moreover, harsh annealing conditions might be responsible for local break-ups of the deposited SiO_x resulting in a negative effect of the

chemical passivation [54]. The objective of this section is an intensive optimization study of the optimal annealing process for poly-SiC_x passivation contacts. Considering the importance of the annealing process, different durations and temperatures are tested.

3.2.1 Annealing temperature influence on (i)a-Si deposited through LPCVD

The first series of experiments are focused on the influence of the annealing temperature and duration on 12-nm thick (i)a-Si layer deposited by LPCVD, as this thickness was identified as the most suitable for passivation based on previous results [79]. Studied samples were one side polished one-side textured wafers prepared according to the method described in section 3.1. The p-type and n-type layers have a constant thickness of 30 nm and 10 nm, respectively. The measured i-Voc results are presented in Figure 3.2.

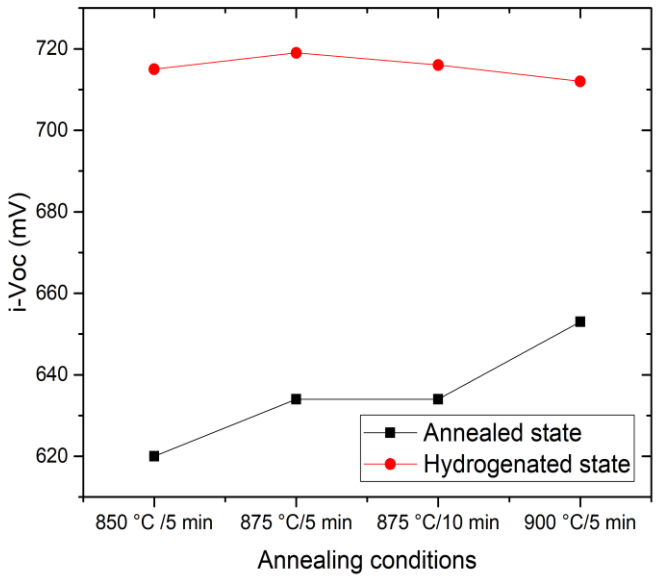


Figure 3.2 i-Voc as a function of various annealing temperature/time after annealing and after hydrogenation for cell precursors with 12 nm thick (i)a-Si deposited via LPCVD and 30-nm thick (p)poly-SiC_x and 10 nm thick (n)poly-SiC_x layer.

From Figure 3.2, it is clearly visible that the i-Voc measured after annealing progressively increases for higher temperature and longer time of annealing. The highest i-Voc is obtained for annealing at 900°C for 5 minutes. The sample annealed at these conditions achieves i-Voc of 653 mV, τ_{eff} of 320 µs and recombination current density (J_0) of 92.5 fA/cm^2. Annealing condition of 900°C is visibly outperforming the lower temperatures of 875°C, where the achieved i-Voc is in a range of 631 - 634 mV ($\tau_{eff} = 153 - 156$ µs.) . Focusing on the hydrogenated state at annealing temperature of 875°C the i-Voc changes according to the annealing time; the longer is the annealing time the lower is the i-Voc (5 minutes annealing i-Voc of 718 mV and 10 min annealing time i- Voc of 715 mV).

The result obtained for high annealing temperature is quite surprising since for annealing conditions at a temperature of 900 °C a drastic drop in i-Voc was expected as a result of temperature-induced local disruptions of the chemical SiO_x leading to the local thickness changes

or pinhole formation [80]. This may consequently be the main cause of a localized current path for the charge carriers. With increased annealing temperature pinhole size and density increase what deteriorates the passivation contacts even more [81]. Nonetheless, as it is visible in Figure 3.2 after the hydrogenation the passivation improves strongly with values above 710 mV. The highest i-Voc is measured at 875 °C/5 minutes. Consequently, this annealing temperature is considered as optimal for the cell precursors with the intrinsic amorphous silicon layer deposited through LPCVD.

3.2.2 (i)a-Si:H material structure deposited through PECVD

Before the study of annealing temperature influence on the passivation structures with the intrinsic layer deposited through the PECVD deposition method, the impact of different deposition parameters was studied. The reason behind this study is the fact that cell precursors with (i)a-Si:H layer deposited through PECVD method [79] are giving considerably worse results than cell precursors with intrinsic layer deposited through LPCVD (Table 3.1). The explanation of this might be related to the fact that the layers deposited through PECVD deposition method are of lower homogeneity and density with comparison to buffer layer deposited through the LPCVD method [63]. The possible reason for the lower homogeneity of layers deposited through PECVD can be the hydrogen content in the buffer layer, therefore we try to minimize the hydrogen concentration in the buffer layer [82]. Consequently, at the beginning of this series of experiments, the analysis of the deposited material was performed, and possible ways of improvement were considered. Depositing buffer layer through the PECVD method it is possible to manipulate 3 main parameters: gas flow ratio, deposition pressure, and temperature. As the (i)a-Si: H layer was deposited with the maximum possible gas flow ratio the influence of temperature and pressure variation was studied.

Table 3.1 Results obtained on cell precursors with intrinsic layer deposited through PECVD and LPCVD deposition method.

Deposition method	**Interlayer thickness (nm)**	**i-Voc (mV)**	**τ_{eff} (ms)**
PECVD	8	684	1.24
LPCVD	8	711	1.40

FTIR analysis of buffer layer deposited through PECVD

FTIR analysis allows the investigation of material properties and the bonds present in the deposited layers. In order to correctly characterize the material n-type CZ silicon wafers were used with a thickness of 525 µm, <100> orientation and a resistivity of 15 Ω-cm. Before the measurements, the wafers were immersed in NAOS which objective is a chemical growth of SiO_2. The details of this process are described in section 2.1.3. Subsequently on top of the silicon oxide 100 nm thick (i)a-Si:H layer was deposited through the PECVD method. During the deposition process, the SiH_4 flow ratio was kept constant at 45 sscm, but the deposition pressure and temperature were varied in the widest range possible for our PECVD tool. From the initial values of 0.7 bar, the pressure is increased up to 1.2 mbar, which is the highest pressure at which the plasma ignites. Then, the temperature is increased from 180 °C up to 220 °C.

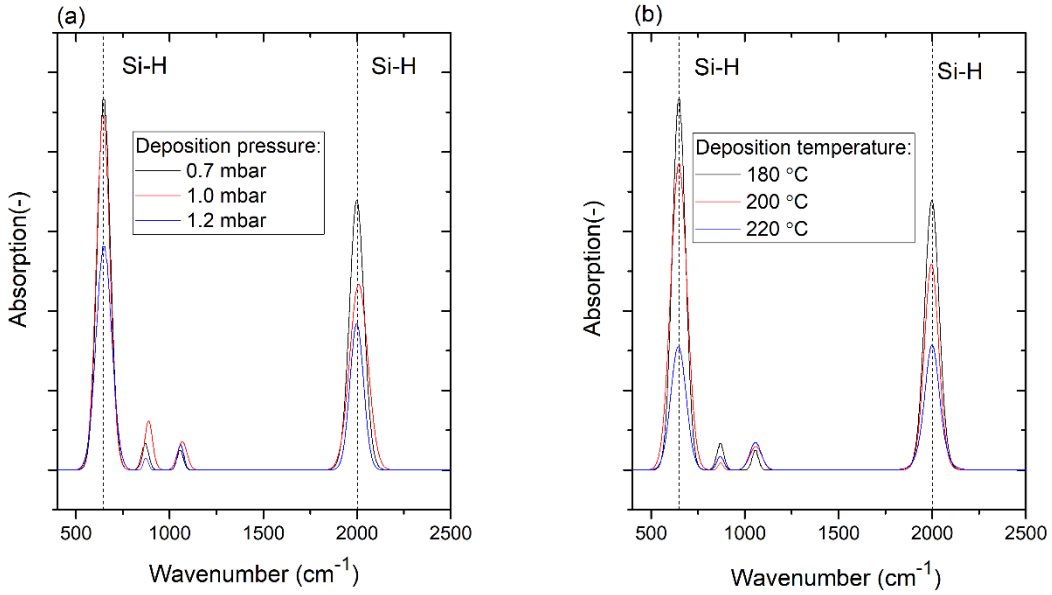


Figure 3.3 FTIR spectra of samples with intrinsic layer deposited at different pressures (a) and different temperatures (b). Layers have a thickness of 100 nm.

Figure 3.3(a) and Figure 3.3(b) show the FTIR spectra of (i)a-Si:H layers deposited at different pressures (0.7-1.2 mbar) and temperatures (180°C-220°C). For every deposition, the most intensive peak is occurring at the 640-650 cm^{-1}. This wavenumber corresponds with the Si-H wagging vibration mode [83]. The second most intensive peak that has been recorded is appearing for 2080-2200 cm^{-1} which is correlating with Si-H stretching vibration mode. This absorption peak is typical observed in PECVD layers as reported by Wieder et al.[84].

Analyzing Figure 3.3(a) it is straightforward that peaks intensity is decreasing with increasing deposition pressure. The sharpest peaks are recorded at 680 cm^{-1} (Si-H wagging vibration mode) at a deposition pressure of 0.7 mbar. This is an indication of the fact that more hydrogen is incorporated in the structure of samples deposited at lower pressure. A similar trend is observed for Si-H stretching vibration mode (2080 cm^{-1}). Therefore, from Figure 3.3(a) can be concluded that the higher the deposition pressure the lower the hydrogen content in the structure. For this project (i)a-Si:H layers deposited with the lowest hydrogen content are the most desirable. This is due to the fact that during the annealing process the hydrogen effusion leads to the destruction of the dopant structure (blistering).

FTIR analysis of (i)a-Si:H deposited at different temperatures (Figure 3.3 (b)) is representing similar trends like the one investigated for pressure variation. The significant difference between the spectra of various deposition temperatures is the fact that the higher the deposition temperature the more significant are the changes in the peaks which are representing Si-H wagging vibration mode (680 cm^{-1}) and Si-H stretching vibration mode (2080 cm^{-1}). This result is correlating with the trend that was followed by the deposition pressure increase that indicates that for this project the most suitable are (i)a-Si:H layers with the lowest hydrogen content in the as-deposited state, since the dangling bonds present at the wafer surface will be later saturated during the hydrogenation process.

Influence of deposition parameters on annealing temperature

Optimization of annealing temperature for the samples with an intrinsic layer deposited by the PECVD method is a sensitive process. Many aspects influence the optimal annealing temperature, which differs with regard to annealed and hydrogenated state. In this series of experiments, a variation of deposition temperature and pressure of the (i)a-Si:H layer is performed, as in the previous section was proved that deposition pressure and temperature variation results in a change of material composition. The (i)a-Si:H layer thickness is fixed at 10 nm. All of the studied samples are symmetrical (p)poly-SiC_x samples with a constant p-layer thickness of 30 nm fabricated on polished c-Si wafers. In order to better visualize analyzed samples Figure 3.4 depicts a sketch of the investigated structure.

Figure 3.4 Schematic sketch of (p)poly-SiC_x symmetrical sample.

The (p)a-SiC_x:H symmetrical samples have been annealed at different temperatures for a constant annealing time equal to 5 minutes.

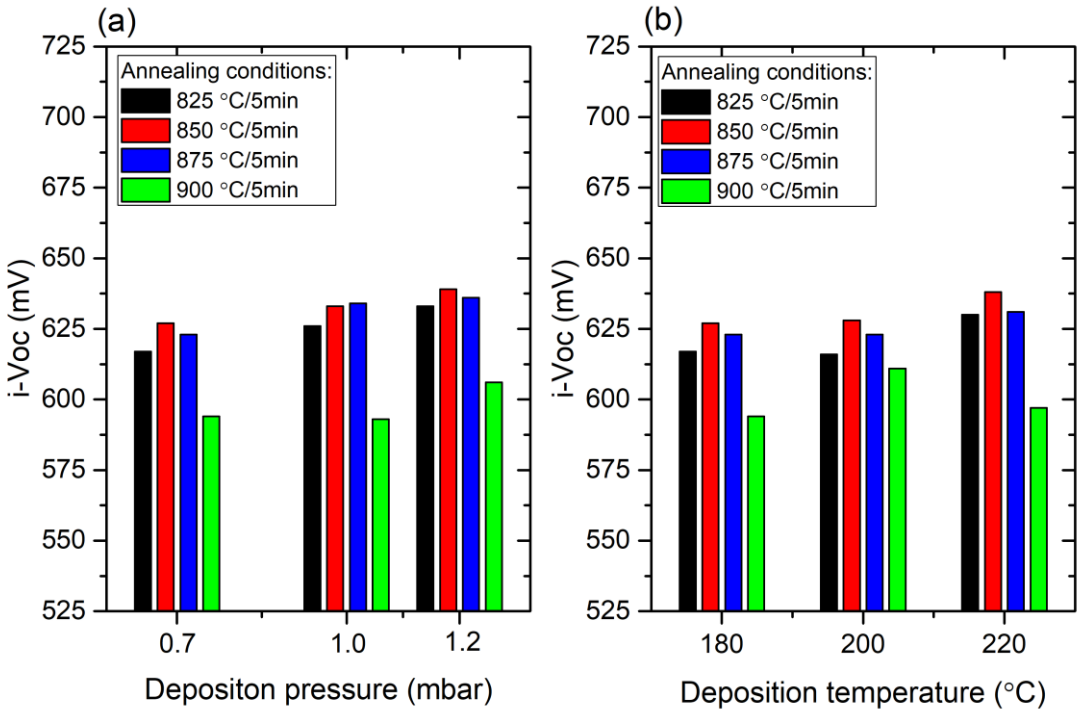


Figure 3.5 i-Voc values of (p)poly-SiC_x symmetrical samples after annealing at various temperatures for (a) different deposition pressure of (i)a-Si:H and constant deposition temperature of 180 °C and (b) different deposition temperature and constant deposition pressure of 0.7 mbar.

Analyzing Figure 3.5, it is visible that at the annealed state the best results are obtained for annealing condition of 850 °C/5 min for every deposition pressures and temperatures tested. Moreover, higher i-Voc values are also reached for samples deposited at higher pressures and higher temperatures (1.2 mbar and 220 °C). Champion i-Voc for this set of experiments (Figure 3.5(a)) is obtained for the sample annealed at 850 °C/5 min with an intrinsic layer deposited at 1.2 mbar with i-Voc of 639 mV, τ_{eff} of 290 µs and J_o of 153.5 fA/cm^2. The i-Voc variation, with regard to the change of annealing temperature, is more visible for samples deposited at higher temperature and pressure (Figure 3.5). The most significant i-Voc drop of 32 mV between the annealing temperature of 825°C and 900°C occurred for samples deposited at a pressure of 1.2 mbar. This can be linked to the fact that the deposition process of (i)a-Si:H at higher pressures and temperatures is less stable than for lower pressures and temperatures and also less stable than the LPCVD process. Consequently, (i)a-Si:H deposited at higher pressures has a lower homogeneity and locally lower thickness. Moreover, the significant drop in i-Voc at annealing conditions of 900°C/5 min can be a result of the destroyed structure of SiO_x which is one of the elements responsible for passivation contacts. Nogay et. al [63] have proved in their research, that the thin chemically grown oxide layer disappears during thermal annealing at 900 °C, which consequently leads to degraded surface passivation. In most of the cases, the disappearance of chemically grown SiO_x is happening when no buffer layer is incorporated in the structure. Nonetheless, the hydrogen incorporated in the intrinsic layer deposited through PECVD is effusing during the annealing process and consequently can form the diffusion paths for the SiO_x molecules. Subsequently, this can lead to the chemical reaction between carbon atoms present in (p)SiC_x layer and the chemical oxide layer and finally i-Voc drop.

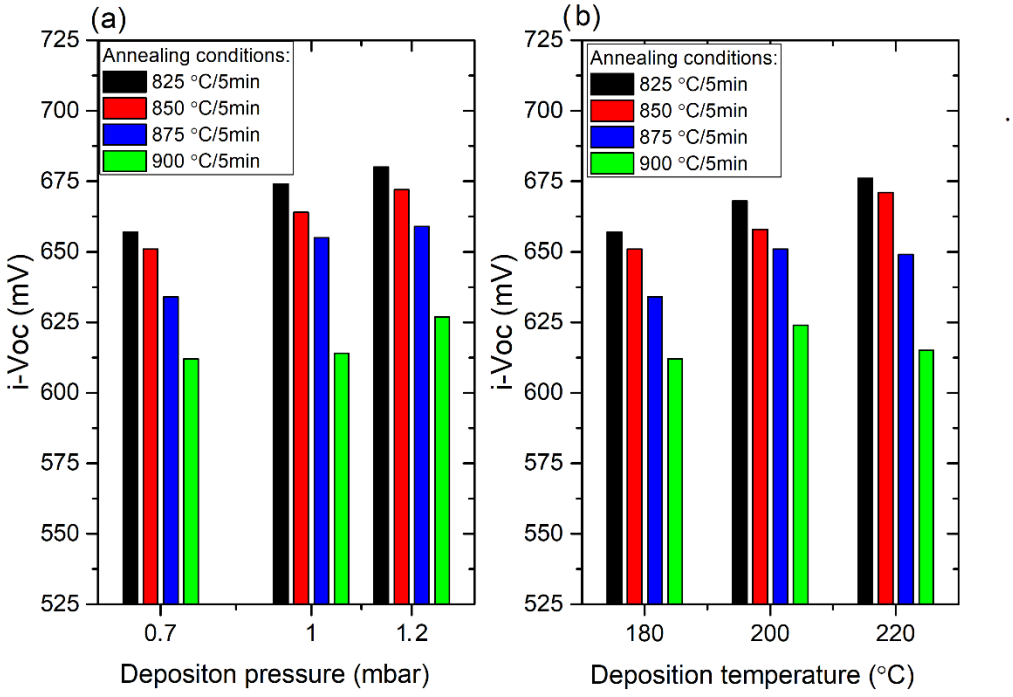


Figure 3.6 i-Voc values of (p)poly-SiC_x symmetrical samples after hydrogenation at various temperatures for (a) different deposition pressure of (i)a-Si:H and constant deposition temperature of 180 °C and (b) different deposition temperature and constant deposition pressure of 0.7 mbar.

Looking at Figure 3.6(a) and Figure 3.6(b) it is visible that after the hydrogenation process the optimum annealing temperature of samples with (i)a-Si:H deposited through PECVD has changed. Moreover, analyzing Figure 3.6(a) and Figure 3.6(b) we observe a clearly decreasing trend of i-Voc with regard to the annealing temperature. For each deposition pressure, as well as, for each deposition temperature, the best annealing condition in the hydrogenated state is 825 °C for 5 min. Furthermore, the best performing sample is the one with (i)a-Si:H layer deposited at 1.2 mbar: i-Voc=680 mV, τ_{eff} =1.04 ms and Jo= 31.3 fA/cm^2. The possible explanation of this is the fact that the intrinsic layer of these samples has the lowest hydrogen content (FTIR analysis). Consequently, on these samples, the least possibility of damage through hydrogen effusion occurs (blistering). Moreover, in the hydrogenated state, the i-Voc variation is more visible. The most significant i-Voc drops with regard to the annealing temperature is recorded for the highest deposition pressure of 1.2 mbar (-53 mV) and the deposition temperature of 220 °C (-56 mV). Where the drop refers to the annealing temperatures of 825 °C and 900°C.

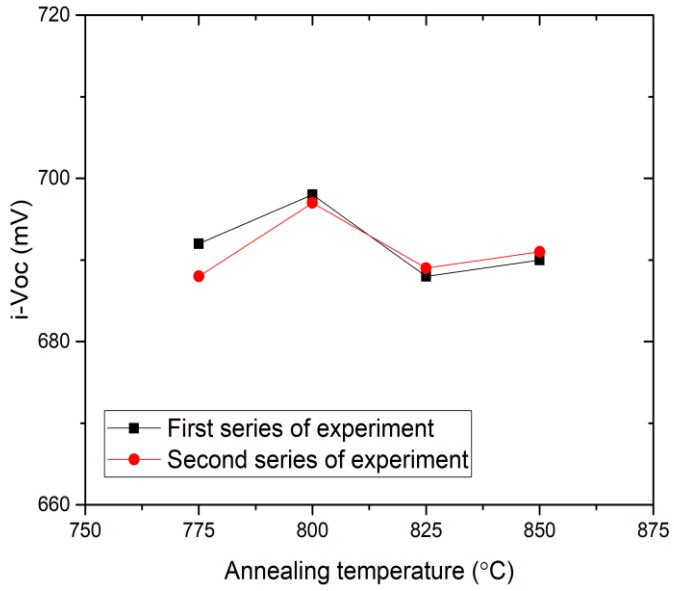


Figure 3.7 i-Voc values of polySi-C$_x$ cell precursors after hydrogenation with intrinsic layer deposited at 1.2 mbar and 180 °C and annealed at different temperatures.

The increasing i-Voc trend for lower annealing temperature observed in Figure 3.6(a) and Figure 3.6(b), motivated further tests with annealing temperature below 800 °C. Two series of experiments have been carried out, as we wanted to check in the results are reproducible and follow the same trend. During the two series of experiments for samples with a fixed n-type layer thickness equal to 10 nm and p-type layer equal to 30 nm and (i)a-Si:H thickness of 10 nm deposited at pressure of 1.2 mbar and temperature of 180°C, the best results at the hydrogenated state are found. These tests have been performed on cell precursors, as the study of lower annealing temperatures was performed during the doped layer thickness optimization.

As presented in Figure 3.7, the highest i-Voc value for poly-SiC$_x$ sample is obtained for annealing conditions of 800 °C/ 5 min (i-Voc 698 mV and τ_{eff} of 1.3 ms and Jo of 20.9 fA/cm^2). Finally, the annealing conditions of 800 °C/ 5 min is found to be the best for further solar cell fabrication with

(i)a-Si:H layer deposited by the PECVD method. Consequently, this annealing condition will be applied for FBC solar cells fabrication with (i)aSi:H deposited through PECVD in the next chapter.

3.3 Interlayer optimization

As we have shown in section 3.2, the (i)a-Si layer is needed to reach a decent passivation quality in the view of fabricating poly-SiC_x solar cells. So far, we have compared two deposition methods for a fixed (i)a-Si:H layer thickness LPCVD and PECVD (section 2.1.4). The presence of this layer was proven by Nogay et.al. [63] to be fundamental to preserve passivation. In fact, they have indicated that C atoms can react with SiO_x therefore, decreasing passivation quality. The origin of this phenomenon is the fact that carbon atoms are deposited in the form of CH_3 groups, which indicates that they are poorly connected within the a-Si structure (only one bond is present between carbon and silicon) [78]. Moreover, during the annealing process hydrogen effuse, leaving dehydrogenated C atoms to be bonded only with one Si atom. Therefore, carbon atoms can likely react with the SiO_x layer. This may cause an oxygen effusion in the form of CO_2 or CO [81]. Consequently, in order to avoid this behavior-direct contact of the carbon with SiO_x and reduce their chemical reaction the (i)a-Si interlayer is deposited between SiC_x and SiO_x layers. This section objective is an intensive study of the (i)a-Si deposited by the PECVD and LPCVD method.

3.3.1 Thickness optimization for LPCVD (i)a-Si

In the first part of experiment three different thicknesses of (i)a-Si layer deposited by the LPCVD method are investigated 8 nm, 12 nm, and 14 nm. Nonetheless, it is worth mentioning that the presented thicknesses are the values obtained on the flat side. Considering the pyramids of the textured structure, the thickness of the deposited layer will be thinner by the ratio of 1.7 or 1.5 which is a result of geometrical calculations that take into account the geometry of the pyramids [85]. The performed analysis is referring to the intrinsic layer thickness on the flat side. On Figure 3.8 is presented the analyzed passivation structure.

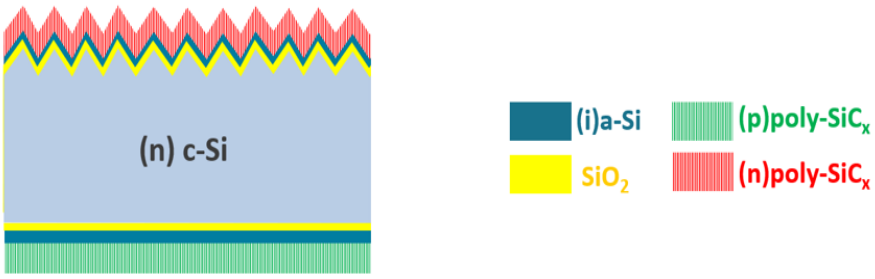


Figure 3.8 Schematic sketch of tested poly-SiC_x sample.

Figure 3.9(a) depicts the i-Voc as a function of annealing temperature change and buffer layer thickness. As presented in Figure 3.9(a) the i-Voc for different thicknesses follows the same trend- the best annealing condition is 875°C/ 5 minutes. Considering the studied thicknesses the thickest layer of 14 nm behaves the worst, the best results obtained for this film in the annealing process (875 °C/ 5 min) are i-Voc of 616 mV, τ_{eff} of 87 µs and J_o of 395 fA/cm^2. The explanation of this trend can be the fact that the deposited i-layer is too thick and reduced dopant diffusion from doped layers

to the c-Si still can occur. The best results are obtained for (i)a-Si thickness of 12 nm. This layer thickness in the annealed state is visibly outperforming other thicknesses values (i-Voc of 634 mV, τ_{eff} of 156 µs and J_o of 160 fA/cm^2). Moreover, 12 nm (i)a-Si is behaving better in the annealed state for every annealing temperature. This is proof that this layer thickness deposited by the LPCVD is an optimum for this process. On the other hand, a thinner layer of 8 nm is slightly outperforming 14 nm layer for higher annealing temperatures. The best results obtained for the 8 nm layer are (i-Voc of 622 mV, τ_{eff} of 111 µs and J_o of 319.5 fA/cm^2). Nonetheless, for this thickness the achieved results are still worse than for the optimum thickness of 12 nm. Possible explanation of these results can be the diffusivity of carbon in silicon [86]. It can be assumed that for a very thin (i)a-Si carbon atoms can still approach the chemical SiO_x, which can explain the lower performance of the sample.

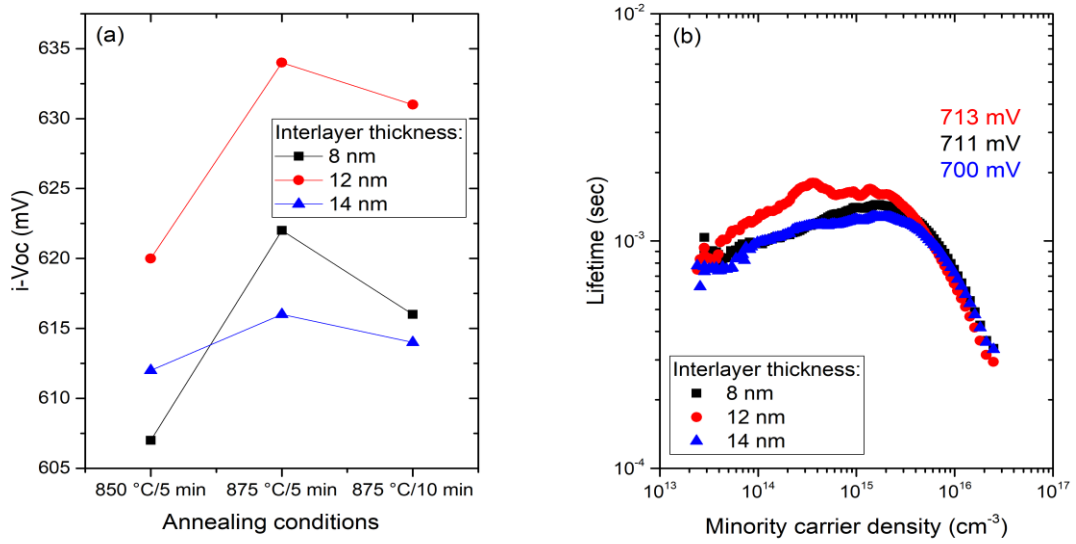


Figure 3.9 i-Voc as a function of various annealing temperature/time and interlayer thickness after annealing for polySi-C_x (a) and lifetime of poly-Si-C_x samples with variable (i)a-Si:H thickness after hydrogenation (b)

Figure 3.9(b) depicts the lifetime curves of minority charge carriers for the samples annealed at 850°C/5 min after hydrogenation. The 12 nm interlayer is still outperforming other thickness values (i-Voc 713 mV τ_{eff} 2.14 ms and J_o of 9.5 fA/cm^2) even if the differences are less pronounced. For the thinner intrinsic layer (8 nm), the i-Voc value is similar to the champion value of 713 mV, but for the thicker layer (12 nm) we observe a reduction in i-Voc of 13mV. However, the τ_{eff} of 1.24 ms for 8 nm interlayer thickness is considerably lower than for the optimum thickness (12 nm).

3.3.2 Thickness optimization for PECVD (i)a-Si:H

The tested thickness of (i)a-Si:H layers deposited by PECVD changed in a range of 5-20 nm. The deposition parameters are: SiH_4 flow of 45 sscm, the temperature of 180 °C and the deposition pressure of 1.2 mbar as this condition was giving the best results during the annealing temperature optimization as it was presented in Figure 3.5 and Figure 3.6. The previous section (3.2.2) explains that the layer deposited at 1.2 mbar pressure has the lowest hydrogen content what is giving desirable passivation results. In order to better visualize the fabricated samples in the experiments

reported here, Figure 3.10 presents the sketches of the investigated structures. The doped layers of these samples have a fixed thickness of 30 nm for (p)poly-SiC_x layer and 10 nm for (n)poly-SiC_x layer.

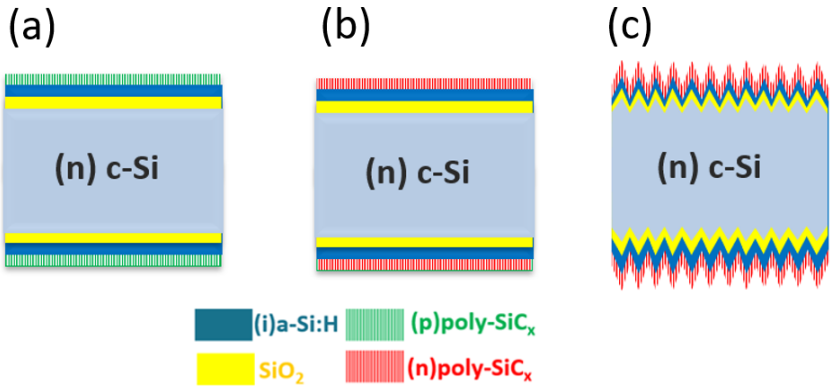


Figure 3.10 Sketches of tested structures: (p)poly-SiC_x symmetrical polished (a), (n)poly-SiC_x symmetrical polished (b) and (n)poly-SiC_x symmetrical textured (c).

The intrinsic layer thickness variation tests were initially performed on symmetrical (p)poly-Si-C_x samples (Figure 3.11(a)), as the results obtained for polished (p)poly-SiC_x are valid for FBC as well as for IBC solar cells. Figure 3.11(a) presents the i-Voc as a function of different annealing temperature and intrinsic layer thickness. Every studied buffer layer thickness follows the same trend, the best annealing temperature for every sample is 850 °C. Studying the different thicknesses in the annealed state the best results have been obtained for the (i)a-Si:H layer with a thickness of 10 nm annealed at 850°C/5min, what coincides with the results presented on Figure 3.5(a). The champion i-Voc value for these parameters in the annealed state is i-Voc of 638 mV, τ_{eff} of 290 µs and J_o of 160 fA/cm^2. Moreover, on Figure 3.11(a) is easy to recognize that the use of thicker i-layers results in deteriorated performance on cell passivation, with clearly decreasing trend. This can be associated with the fact that too thick layers do not allow the efficient diffusion of dopants consequently leading to the deteriorated field-effect passivation. On the other hand, the 5 nm (i)a-Si:H also behaves worse than the optimal 10-nm thick i-layer. The best i-Voc achieved for 5 nm interlayer is 634 mV and τ_{eff} of 230 µs and J_o of 187 fA/cm^2 (850°C/5min). The origin of this weaken passivation results is the fact that dopants are deposited too close to the c-Si bulk and higher dopants in-diffusion into c-Si but may occur [78]. Moreover, every interlayer thickness is behaving the worst in the lowest annealing temperature, this can indicate that the temperature might be not high enough to provide a complete (i)a-Si:H crystallization. As it was mentioned in section 1.2 c-Si has superior electrical properties over a-Si, hence the explanation of this trend is straightforward. On the contrary, the highest annealing temperature of 875 °C is also behaving worse than the most optimal one at 850 °C. This can be explained by the fact that dopants diffuse too far into c-Si bulk, consequently, again deteriorate field-effect passivation [87] .

Figure 3.11(b) depicts the effective lifetime of minority charge carriers in the hydrogenated state. The lifetime of samples with different interlayer thickness is presented only for the temperature of 800 °C, as this value was giving the best results after the hydrogenation process during the previous experiments(Figure 3.6(a)). Considering the data presented in this graph, it is easy to notice that again the best performance is representing the interlayer with a thickness of 10 nm-the highest i-Voc of 681 mV, τ_{eff} of 1150 µs and J_o of 31.3 fA/cm^2. The worst results were obtained for interlayer of 5 nm i-Voc 676 mV, τ_{eff} of 913 µs and Jo of 39.65 fA/cm^2. This result proves that even the

hydrogenation process cannot improve the passivation quality of the sample with too thin (i)a-Si:H layer and that the diffusion of dopants into the c-Si cannot be suppressed by the hydrogenation process.

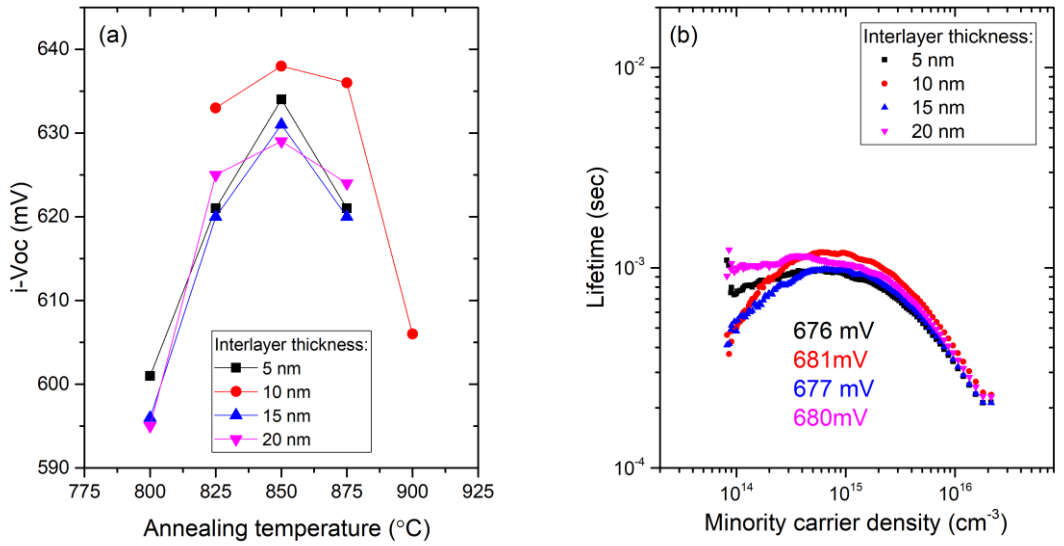


Figure 3.11 i-Voc as a function of various annealing temperature and interlayer thicknesses after annealing for symmetrical polished (p)poly-Si-C_x samples (a) and lifetime curves of (p)poly-Si-C_x symmetrical samples annealed at 800 °C with variable (i)a-Si:H thickness after hydrogenation (b).

The effect of (i)a-Si:H layer thickness was tested not only for (p)poly-SiC_x symmetrical polished samples, but also for (n)poly-SiC_x symmetrical samples. The tests were performed on double side polished and double side textured wafers as depicted in Figure 3.12 and Figure 3.13, respectively. The objective of performance of (n)poly-SiC_x on polished surface was the investigation of (i)a-Si:H layer results on polished surface in terms of IBC solar cells.

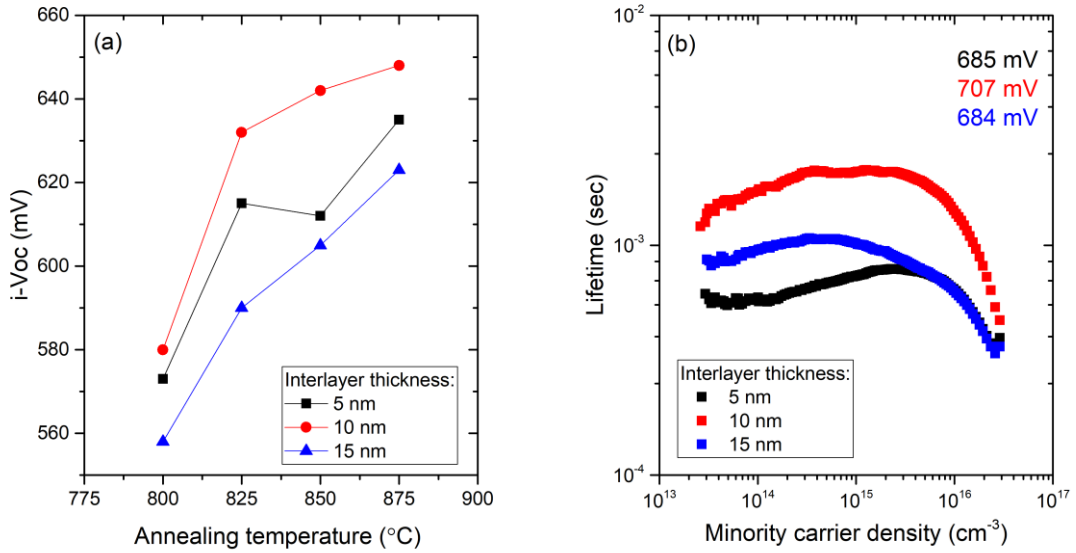


Figure 3.12 i-Voc as a function of various annealing temperature and interlayer thickness after annealing for (n)poly-SiC_x symmetrical polished samples (a) and lifetime curves of (n)poly-SiC_x symmetrical polished samples annealed at 800°C with variable (i)a-Si:H thickness after hydrogenation (b).

Figure 3.12(a) presents i-Voc as a function of different annealing temperatures and thicknesses of the buffer layer deposited on (n)poly-SiC_x symmetrical polished samples. Looking at this figure, a clearly increasing trend with regard to the annealing temperature is presented. For every analyzed thickness, the highest i-Voc is achieved for annealing temperature of 875°C. Besides, looking at Figure 3.12(a) it is straightforward that the best results achieve the sample with an interlayer thickness of 10 nm. The champion parameters for this thickness are; i-Voc of 648 mV, τ_{eff} of 331 µs and J_o of 198 fA/cm^2 which indicates that the optimal interlayer thickness is the same for p-type as well as for n-type dopants. Besides, looking on Figure 3.12(b) and comparing it with Figure 3.11(b) the champion i-Voc with (i)a-Si:H thickness of 10 nm after hydrogenation is higher for n-type semiconductors than for p-type (n-type 709 mV p-type 681 mV), and the minority carrier lifetime for n-type semiconductors is also higher than for the p-type (2.1 ms and 1.15 ms). The possible reason of this is the fact that typical lifetime killers in silicon are transition metals [88]. These metals have bigger carrier capture cross-section for electrons than for holes [89], which therefore means that holes are more effectively captured than electrons, what finally deteriorates the passivation quality.

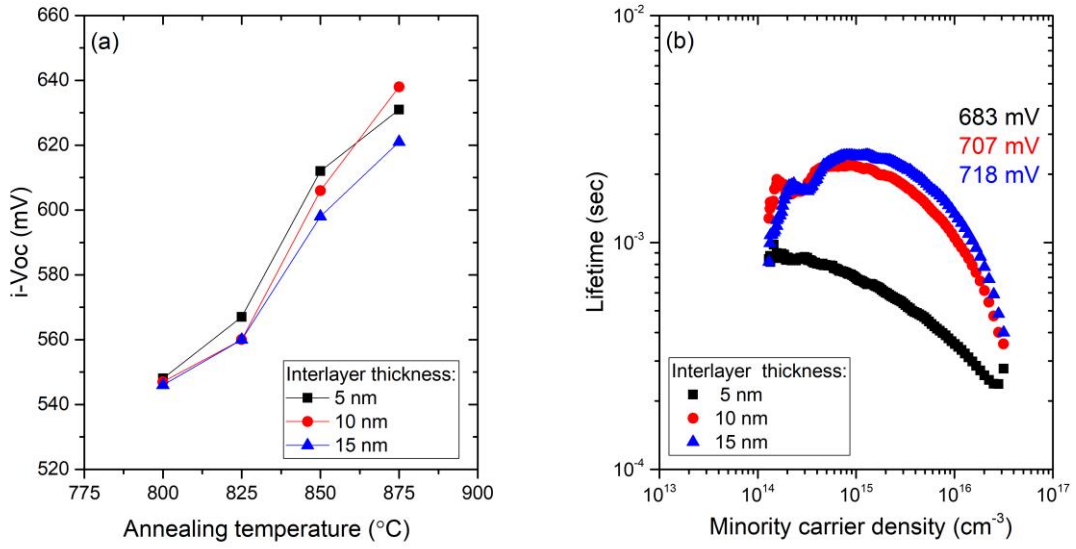


Figure 3.13 i-Voc as a function of various annealing temperature and interlayer thickness after annealing for symmetrical textured (n)poly-SiC_x samples (a) and Lifetime of (n)poly-SiC_x on symmetrical textured samples annealed at 800°C with variable (i)a-Si:H thickness after hydrogenation (b).

Finally, the last interlayer tests were performed on (n)polySi-C_x double-side textured samples (Figure 3.13). The (i)a-Si:H thickness variation was carried out on textured wafers in order to obtain the best results for FBC solar cells for which intrinsic layers and dopants will be deposited by the PECVD.

Looking at Figure 3.13(a) an increasing trend, similar to the one presented on Figure 3.12(a) is visible-the higher the annealing temperature the higher the obtained i-Voc value for every thickness. Moreover, as presented on Figure 3.13(a) in the annealed state, the best performance is obtained for 10-nm thick (i)a-Si:H (i-Voc 638 mV, τ_{eff} of 193 µs and Jo of 298.5 fA/cm^2). In the annealed state the worst behavior is represented by the (i)a-Si:H thickness of 15 nm (621 mV). i-Voc drop of 17 mV with regard to the 10 nm thickness. Nonetheless, as shown in Figure 3.13(b) this

trend is reversed in the hydrogenated state. The champion samples is the one with 15 nm interlayer thickness. The obtained parameters for this cell are i-Voc of 718 mV, τ_{eff} of 2.45 ms and J_0 of 7.8 fA/cm^2. Furthermore, 15 nm i-layer thickness in the hydrogenated state is also very stable with regard to different annealing temperatures (Figure 3.14). The possible explanation of this fact can be the lower sensitivity of a thicker layer on the hydrogen effusion and possible material blistering.

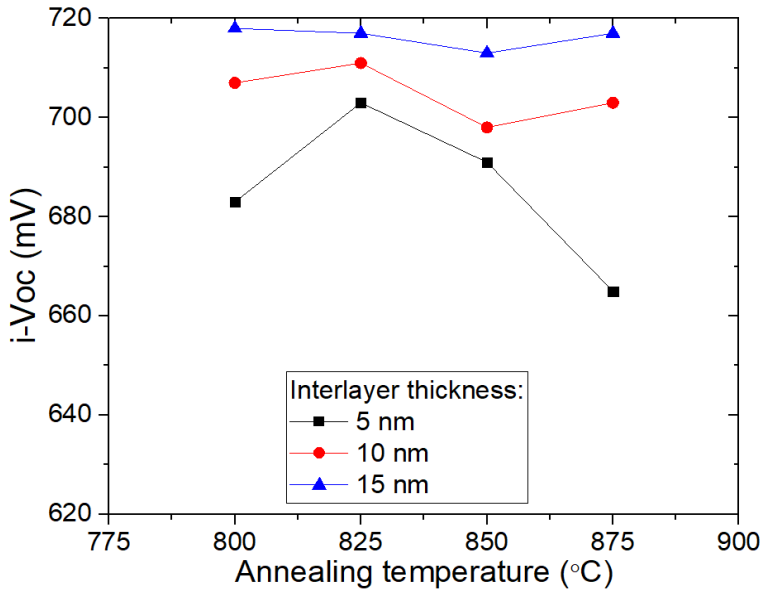


Figure 3.14 i-Voc as a function of various annealing temperature and interlayer thickness after hydrogenation for symmetrical textured (n)poly-SiC$_x$ samples.

3.4 Comparison of LPCVD and PECVD interlayer

In order to better present the difference between the LPCVD and PECVD deposition methods, the results discussed in the previous subchapter are presented in Figure 3.15. Each graph in Figure 3.15 presents the champion i-Voc achieved for different interlayer thickness and wafer structure. It is important to note that all the LPCVD layers were deposited on cell precursor structure with one side polished and one side textured while the PECVD deposition method was tested on symmetrical polished and symmetrical textured samples.

Looking at Figure 3.15(a) the comparison between LPCVD and PECVD deposition method is present. The champion i-Voc obtained for (i)a-Si:H deposited through the LPCVD method is 713 mV and was achieved for a thickness of 12 nm. This value represents the optimal interlayer thickness, since as it is presented on Figure 3.15(b) thicker and thinner layers demonstrate lower passivation quality. Nonetheless, it is important to note that 12 nm thickness was measured with regard to polished surface structure not textured one. The (i)a-Si: H thickness on the textured surface is thinner by the ratio of 1.7 [67], which comes from the geometry of the pyramids which are present on the textured side. Consequently, the best buffer layer thickness deposited through LPCVD method for the textured side is 7 nm.

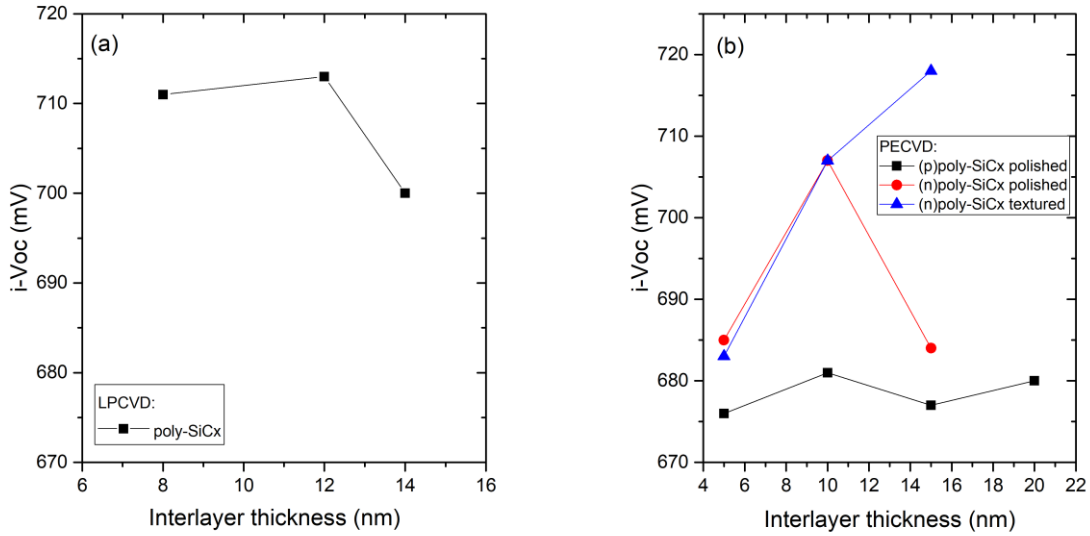


Figure 3.15 i-Voc change as function of the (i)a-Si:H thickness deposited through (a) LPCVD (b) PECVD.

The i-Voc values obtained for the interlayer deposited by the PECVD are varying more significantly than for the LPCVD method. Firstly, it is important to note that the PECVD method allows obtaining different interlayer thickness on the textured and polished side, which is a significant advantage because more accurate optimization of the analyzed layer is possible. As presented on Figure 3.15(b) the optimal thickness of (i)a-Si:H deposited by PECVD is different for polished and a textured side. The champion i-Voc for (n)poly-SiC_x double side textured sample is 718 mV and was achieved for the interlayer thickness of 15 nm. On the other hand, the best i-Voc result for (p)poly-SiC_x polished sample was obtained for the interlayer thickness of 10 nm and reached a value of 681 mV. Finally, it is important to note that tests were also performed for (n)poly-SiC_x polished sample. The best interlayer thickness of this layer was found to be 10 nm.

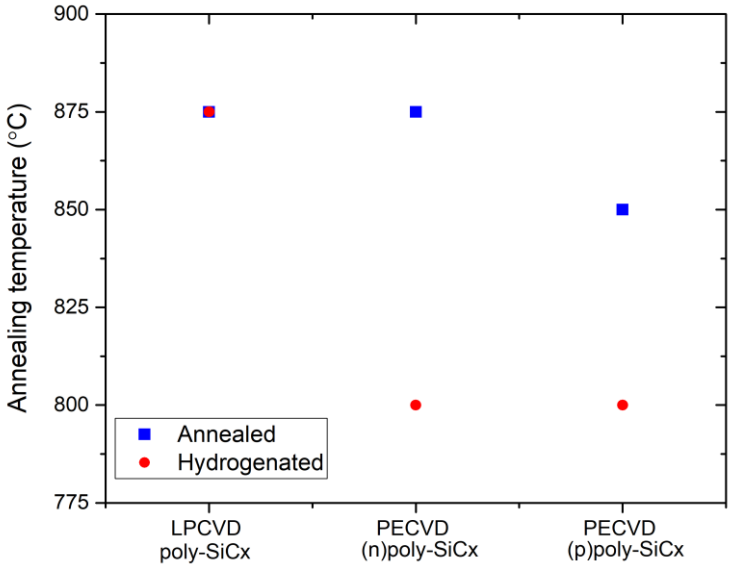


Figure 3.16 Comparison of annealing conditions for LPCVD and PECVD deposition methods.

Moreover, in order to compare LPCVD and PECVD deposition method, it is also crucial to point out that the optimal annealing temperature for the interlayers deposited through these methods are different (Figure 3.16) For every sample with (i)a-Si thickness deposited through LPCVD the best annealing temperature is 875 °C. This parameter is constant through the fabrication process, which means that samples processed in this annealing condition are giving also the best results after the hydrogenation process. On the other hand, as presented on (Figure 3.16) the value of the best annealing temperature for samples with (i)a-Si:H deposited through PECVD is varying with regard to annealed and hydrogenated state. Furthermore, the best annealing temperature for (i)a:Si:H deposited through PECVD is also lower than for the LPCVD method. The possible explanation of this phenomenon can be the fact that films deposited through LPCVD are of higher density and homogeneity, and therefore higher temperatures are needed in order to efficiently activate the dopants present in doped layers and crystallize the structure. The champion result in the annealed state for interlayers deposited through PECVD was recorded at a temperature of 850 °C and have changed after the hydrogenation process when the best results have been obtained for 800 °C annealing temperature

3.5 Doped a-SiC$_x$:H layers optimization

In this project, doped layers are deposited through the PECVD method (section 2.1.4). The dopant gas flow was kept at a constant level of 5 sscm and its mix with other gases (CH_4 with flow ratio of 45 sscm and SiH_4 with flow ratio of 20 sscm) was optimized by other members of the PVMD group [79]. The optimization of doped layers was focused on the change of their thickness. The intrinsic layer in studied samples was deposited through PECVD method. The deposition conditions of the intrinsic layer are pressure 1.2 bar, temperature 180°C, and SiH_4 gas flow ratio 45 sscm. The

thickness of the buffer layer is 10 nm for the polished side and 15 nm for the textured side as optimized in the previous section.

3.5.1 Optimization of the (p)poly-SiC$_x$ thickness

Careful optimization of (p)poly-SiC$_x$ has crucial importance for the correct performance of the solar cell. In this series of experiments firstly the thickness variation of (p)poly-SiC$_x$ layer was carried out, while the thickness of (n)poly-SiC$_x$ layer was kept at a constant level of 10 nm.

As presented in Figure 3.17(a), (p)poly-SiC$_x$ layer thickness was varied in the range of 30-100 nm. At this point, it is important to note that p-type doping layers are manufactured to be thicker than n-type layers. The reason for this is the fact that the minority charge carriers in the p-type semiconductors are electrons while in n-type holes [90]. Electron mobility in c-Si is 1350 cm^2/(Vs) while holes mobility is almost three times lower- 450 cm^2/(Vs) [91]. Considering the fact that electrons have higher mobility than holes their diffusion length is also higher, consequently, the optimum thickness of p-type semiconductor is larger than n-type. Besides, on the rear side we are less constrained by the optical losses than on the front side, thus the front side doped layer must be thinner. In fact on this project the optimization of the (n)poly-SiC$_x$ thickness started from 30 nm, but later it was reduced in order to limit parasitic abrosption losses I started wiuth 30 nm for both n and p-layers and then I reduced the fornt one to reduce parasitic absorption

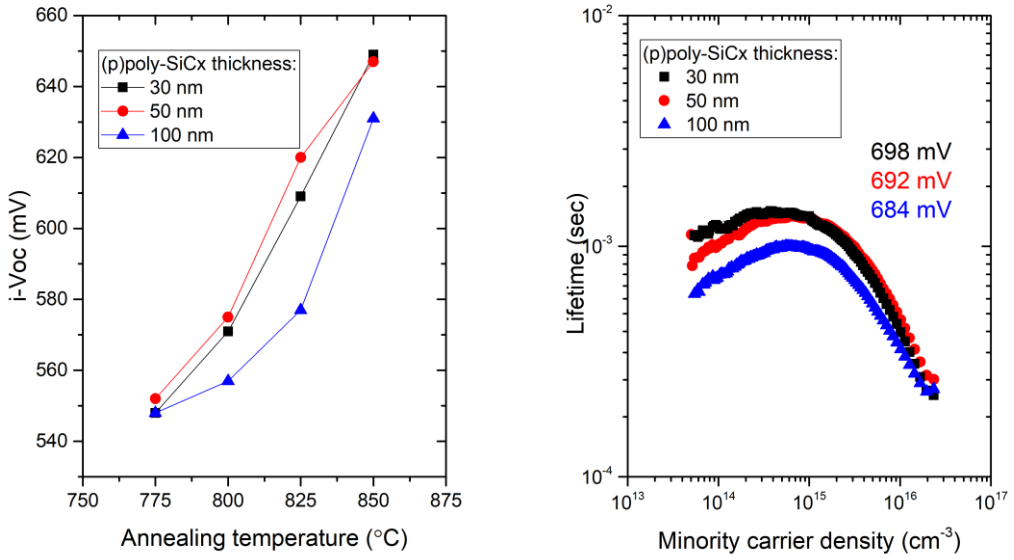


Figure 3.17 i-Voc as a function of various annealing temperature and (p)poly-SiC$_x$ thickness after annealing for cell precursor structure (a) and lifetime of poly-SiC$_x$ samples annealed at 800°C with various (p)poly-SiC$_x$ thickness after hydrogenation (b).

Firstly, looking at Figure 3.17(a) an increasing trend is observed for higher annealing temperature for all the layer thickness tested. The most significant i-Voc improvement is recorded for (p)poly-SiC$_x$ layers with a thickness of 30 nm (Δi-Voc=101 mV). The possible explanation of this trend is the fact that higher temperatures are needed to activate dopants which in the as-deposited state were saturated by the hydrogen atoms. Moreover, the higher the annealing temperature also the higher the dopant concentration and the in-diffused region is also formed deeper [54]. Secondly, in Figure 3.17(a) it is clearly visible that the (p)poly-SiC$_x$ thickness of 100 nm is performing

considerably worse than other investigated thicknesses. The best results of 100 nm (p)poly SiC_x at annealed state are: i-Voc of 631 mV τ_{eff} of 71 µs us and J_o of 285 fA/cm^2. The explanation of the deteriorated performance of this layer can be the fact that the electron diffusion length is lower than the introduced (p)poly-SiC_x thickness what consequently leads to the more effective recombination which has a demanding effect on passivation quality [24]. Analyzing lower thicknesses, it is visible that at annealing temperatures 775°C-825°C the 50 nm (p)poly-SiC_x is behaving better than 30 nm. Nonetheless, at the annealing temperature of 850 °C the 30 nm (p)poly-SiC_x is slightly outperforming other investigated thickness parameters (i-Voc 649 mV τ_{eff} of 262 µs and J_o of 158 fA/cm^2).

Considering Figure 3.17(b) which depicts the minority carrier lifetime at the hydrogenated state for samples which were annealed at 800 °C, again the best results were obtained for the sample with (p)poly-SiC_x thickness of 30 nm. This champion cell at hydrogenated state achieved the i-Voc of 698 mV and τ_{eff} of 1312 us and J_o of 29.3 fA/cm^2. This thickness of the p-layer was also giving the best results for other research groups like Bashiri et al. [92]. Consequently, for further investigation of the best n-type layer thickness (p)poly SiC_x layer is kept at a constant thickness of 30 nm, as this value gives the best result in the performed study. Besides, when applied in FCB solar cell, a thin p-type layer gives higher currents since in the high wavelength range poly-Si materials suffer from free carrier absorption leading to the parasitic absorption losses, and finally lower efficiency of the device.

3.5.2 Optimization of the (n)poly-SiC_x thickness

As it was mentioned before, (n)poly-SiC_x layer thickness optimization (5-15 nm) is performed for lower thickness parameters in comparison to (p)poly-SiC_x thickness optimization (30-100 nm). The reason for this is the fact that minority charge carriers in the n-type semiconductor are holes that have lower mobility than electrons and consequently lower diffusion length. Moreover considering the fact that (n)poly-SiC_x layer will be applied at the front of the FBC solar cells it is crucial to keep this layer as thin as possible in order to avoid the parasitic absorption losses in the short wavelength region [93].

In Figure 3.18(a), the results of different (n)poly-SiC_x thicknesses (5-15 nm) and various annealing temperatures are presented. Firstly, looking at Figure 3.18(a) a clearly increasing trend of i-Voc with regard to the annealing temperature is present. The best results are obtained for the highest annealing temperatures of 875 °C. For this temperature in the annealed state, the worst result is obtained for the (n)poly-SiC_x layer with a thickness of 5 nm. The champion parameters for this thickness are: i-Voc 630 mV τ_{eff} of 140 µs and J_o equal to 277 fA/cm^2. 15-nm thick (n)poly-SiC_x is outperforming 10 nm one in all annealing temperatures except f 875 °C where the points overlap. At this annealing condition, the best passivation is measured from a (n)poly-SiC_x layer of 10 nm. Nonetheless, the results difference between the 10 nm and 15 nm thicknesses are not very significant (Δi-Voc=5 mV). Finally, the champion parameters of 10 nm (n)poly-SiC_x layer are; i-Voc 649 mV, τ_{eff} of 262 us and J_o of 158 fA/cm^2.

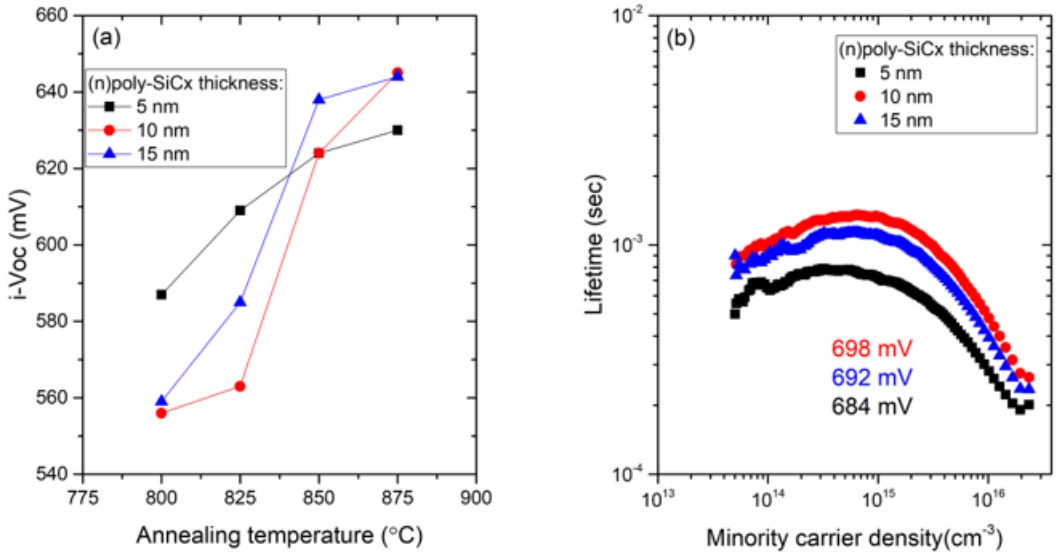


Figure 3.18 i-Voc as a function of various annealing temperature and (n)poly-SiC_x thickness after annealing for cell precursor structure (a) and lifetime of (n)poly-SiC_x samples annealed at 800°C with various (n)poly-SiC_x thickness after hydrogenation (b).

Figure 3.18(b) represents the minority carrier lifetime of different (n)poly-SiC_x thickness after the hydrogenation. Prior to hydrogenation all cell precursors were annealed at a temperature of 800 °C, as this annealing temperature was giving the best passivation results (Figure 3.7). The best results were obtained for the 10 nm (n)poly-SiC_x thickness, the same value that was behaving the best also in the annealed state. The champion sample achieved remaining parameters; i-Voc =698 mV τ_{eff} of 1.32 ms and J_o 29.3 fA/cm^2. Consequently, for further analysis of the cell (chapter 4) 10 nm thick (n)poly-SiC_x is applied.

3.6 Hydrogenation

One objective of this project is to minimize the surface recombination that has deteriorated performance on solar cell efficiency. In section 1.5 different passivation techniques have been described. This section will focus on the hydrogenation process which can provide chemical passivation. Hydrogenation is of high importance as during this process the electronic defects present in the material are passivated with hydrogen atoms. Consequently, the chemical passivation enhances cell performance providing higher minority carrier lifetime and higher implied open circuit voltage.

As presented in section 2.1.6 hydrogenation is performed through the PECVD deposition method. During this process, different SiN_x layers are deposited on top of the poly-SiC_x stacks as capping layer and reservoir of H. We intend to identify the best SiN_x material in term of composition for passivation propose. The main aim of this study is to check which composition of gases is the most suitable for the passivation purposes. Therefore, the gas mixture was varied during deposition to obtain SiN_x films with variables x.

The gas mixture and the corresponding SiH_4/ NH_3 ratios used in this experiment are presented in Table 3.2. The deposition time was adjusted to obtain a thickness of 100 nm for all layers.

Table 3.2 Gas mixture and gas ration used for deposition of SiN_x layers.

SiH_4 (sccm)	NH_3 (sccm)	SiH_4/NH_3 ratio
10	30	0.33
20	20	1.00
25	15	1.66
30	10	3.0

The four different SiN_x layers were investigated via FTIR and ellipsometry to check the different composition and H content and then applied on passivation samples as capping layer followed by the FGA performed at a temperature of 400 °C for a duration of 30 minutes. The passivation tests have been carried out on (p)poly-SiC_x and (n)poly-SiC_x symmetrical polished samples, (n)poly-SiC_x symmetrical textured samples and cell precursors structures.

3.6.1 FTIR analysis

The composition of gases used for the deposition of SiN_x capping layer defines which passivation mechanism is dominating in the structure. In order to investigate the material properties, the bonds present in the deposited layers and check whenever the studied films are nitrogen or hydrogen rich the FTIR measurements were carried out. For this characterization n-type CZ silicon wafers were used with <100> orientation resistivity of 15 Ω-cm and thickness of 525 µm. The analyzed layers are 100 nm thick SiN_x that vary according to the gas compositions reported in Table 3.2.Measurements are performed on the samples in the as deposited state consequently, no thermal treatment was performed on the samples (FGA) in order to identify the H content in the layer.

In Figure 3.19 the FTIR spectra are plotted for four different gas compositions. The sharpest peak can be observed at 970 cm^{-1}, which corresponds to the Si-N stretching vibration mode [94]. Moreover, a peak is also recorded at 2100 cm^{-1} which correlates typically to the Si-H stretching vibration mode [95]. Finally, the last observed peak corresponds to N-H stretching mode recorded at 3340 cm^{-1} , but this peak is present only for one of the gas compositions [95]. Moreover, at 1200 cm^{-1} wavenumber also is observed a peak, which is visible only for two of the investigated gas mixtures. This peak is equivalent to Si-O vibration mode [94].

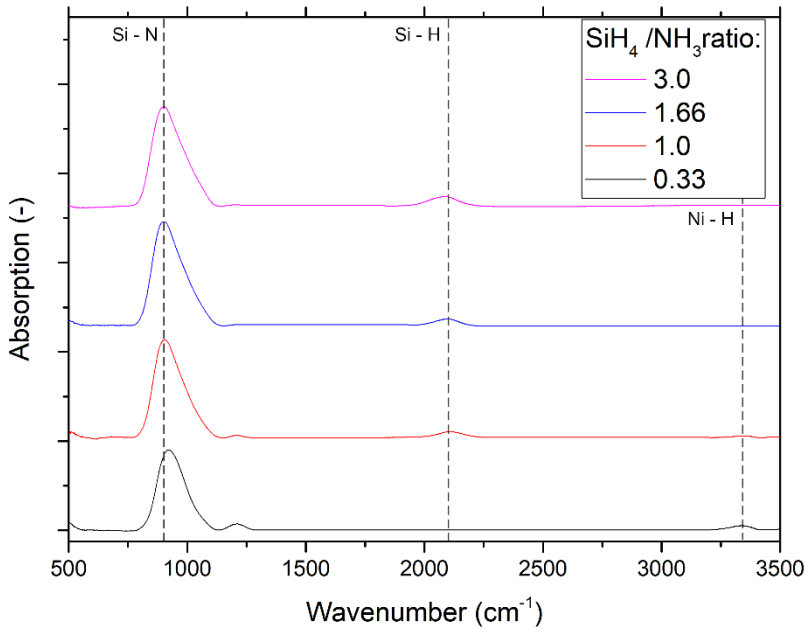


Figure 3.19 FTIR spectra for SiNx layers deposited with different gas compositons of SiN_4 and NH_3. Th layers are 100-nm thick and are in the as-deposited state.

Looking at the absorption peak at 970 cm^{-1} for different gas mixture, it is visible that the higher is the SiH_4 flow, sharper and higher is the absorption peak, which indicates that more silicon is incorporated in the deposited layer. On the other hand, the subsequent peak recorded at 1200 cm^{-1} is present only for the 0.33 and 1.0 SiH_4/NH_3 ratio. This peak corresponds to the Si-O stretching mode. This is an indication of the fact that this layer has some concentration of oxygen that most probably comes from surface oxidation since the deposited layers do not contain oxygen. Subsequently, looking at Si-H stretching mode (2100 cm^{-1}) the sharpest peak was recorded for the SiH_4/NH_3 ratio of 3.0. This is proof that this layer is hydrogen reach, consequently highly saturated with hydrogen. Finally, the last analyzed peak N-H stretching mode (3340 cm^{-1}) was observed only for the highest NH_3 flow. This peak indicates that this layer has a high nitrogen content which comes from a high concentration of ammonia.

As it was studied by other groups like Xiao et al. [96], by changing the ratio of SiH_4 to the NH_3 it is possible to achieve structures with dominating field-effect passivation mechanism or chemical passivation. In their study, they have proved whether the field-effect passivation or chemical passivation is dominant strongly depends on nitrogen content. Films rich in silane perform amorphous Si-like properties. In this case, the high level of passivation is mainly driven by chemical passivation. On the contrary, for high nitrogen content, the N-rich films induce a significant amount of filed-effect passivation [97].

3.6.2 Optical properties of SiN_x layers

The further analysis of deposited layers focused on their optical characterization. The refractive index (n) and extinction coefficient (k) were established through angle-dependent spectral

ellipsometry (SE). The silicon nitride layer was modeled using the Tauc-Lorentz dispersion model. The n spectra gives an indication of the SiN_x composition.

Looking at Figure 3.20(a) and Figure 3.20(b), we observe that both n and k reduce for lower $SiH4/NH_3$ ratio. The n value extracted at 630 nm goes from 2.36 to the 1.88 for SiH_4 NH_3 decreasing from 3.0 to 0.33. We can conclude that particularly for the higher refractive index films are silane reach layers while for lower n the layers are N-rich. The SiH_4/NH_3 of 1.00 corresponds to the stoichiometric SiN_x. Observing the k in Figure 3.20(b), we can also observe that Si-rich material are more absorptive in the low wavelength range then the N-rich ones. These results are consistent with other studies reported in the literature [98], [96]. Moreover, analyzing Figure 3.20(a), it is clearly visible that the refractive index curves for SiH_4/NH_3 ratio of 0.33 and 1.0 have a similar shape to the silicon nitride Si_3N_4 refractive index curve in Ref. [99], which proves that the analyzed layers are N-rich what was also investigated in the previous section. On the other hand, silane rich deposited layers with SiH_4/NH_3 ratio of 1.66 and 3.0 have a refractive index curve that coincides with the silicon refractive index curves what indicates that these layers are silicon rich [99].

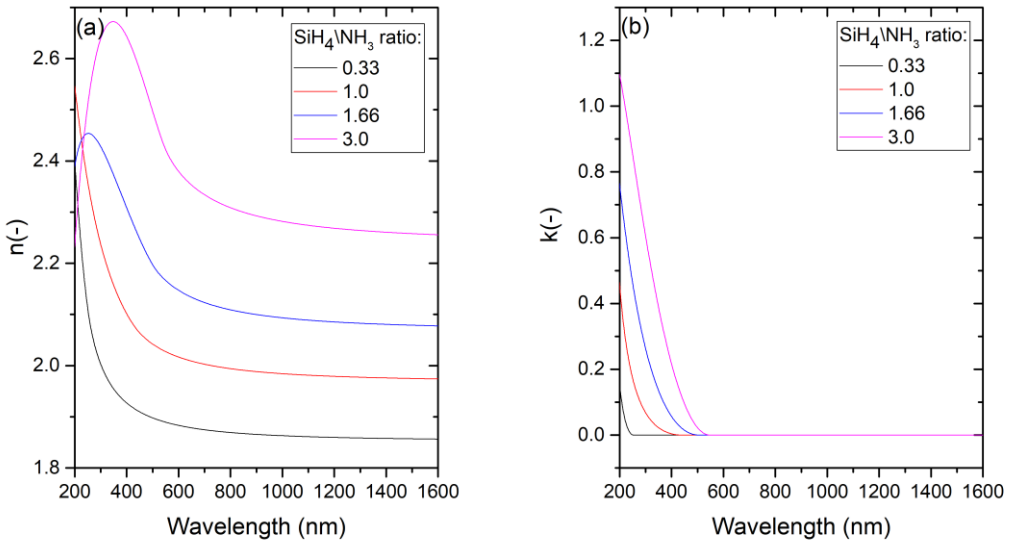


Figure 3.20 Refractive index of samples with different $SiH_4\backslash NH_3$ ratio in the as deposited state (a) and extinction coefficient of samples with different $SiH_4\backslash NH_3$ ratio in the as deposited state (b).

Considering the optical properties of the samples the best choice would be to select for the hydrogenation process the layer with gas compositions of 10 sscm of silane and 30 sscm of ammonia as this layer has the lowest absorption in the short wavelength region. Nonetheless, other groups like Dominguez et al. [99] have proved that nitrogen rich SiN_x films are more prone to develop a porous structure which consequently may have deteriorated performance on passivation structure. Dominguez et al. demonstrated that the non-homogeneity of the SiN_x density which is an origin of the porous structure disappears when the compositions of the film move towards stoichiometry. Consequently, leading to more smooth, dense and homogenous films. This improved microstructure which is achieved at stoichiometric SiH_4 and NH_3 composition is desirable to achieve the light propagation with low losses, as the SiN_x capping layer should have the lowest parasitic absorption losses. Nonetheless, optical aspect is not important for the studied project since the deposited SiN_x layer before the deposition of ITO will be etched away. This is a consequence of the fact that SiN_x

is used to saturate the dangling bonds present on the surface with hydrogen atoms-chemical passivation and in this project, the applied SiN_x layer does not work as an antireflective coating [100].

3.6.3 Passivation results

Finally, in order to investigate the effect of SiN_x composition on passivation quality, implied open-circuit voltage and lifetime of minority charge carriers have been measured. The studied samples were prepared according to the experimental methods presented in section 2.1. The samples consist of symmetrical samples or cell precursors fabricated with 12 nm (i)a-Si layer deposited through the LPCVD process. Afterwards, the doped layers were deposited through PECVD with the doping layer thicknesses of 30 nm (p-type) and 10 nm (n-type). Finally, before the hydrogenation process the samples were annealed at the optimized temperature of 875°C for 5 minutes.

Figure 3.21(a) depicts the i-Voc variation with regard to different gasses composition used for deposition of SiN_x capping layer and different sample structures. The highest value of i-Voc obtained for the N-rich film is 720 mV and was achieved for double side textured sample. On the contrary Si-rich samples (ratio of 3.0) give the lowest i-Voc. The explanation of this can be the phenomenon mentioned earlier that was investigated by other groups like Dominguez et al. [99] who proved that the non-homogeneity of the SiN_x density which is an origin of the porous structure disappears when the compositions of the film move towards stoichiometry. This consequently leads to more homogenous structure that has lower number of defects which could be the origin of surface recombination.

Analyzing the results obtained for p-type and n-type semiconductors it is visible that for the same composition of gases passivation is better achieved for n-type semiconductors. The superior surface passivation achieved for n-type c-Si could be explained by a large capture cross-section ratio of majority to minority charge carriers [97]. Consequently, this may lead to worse surface passivation for p-type silicon. Considering different gasses composition, the best i-Voc values are obtained for the stoichiometric ratio of SiH_4 and NH_3. The champion i-Voc of 728 mV at this gas composition is achieved for double side textured (n)poly-SiC_x sample. Double side textured (n)poly-SiC_x sample also has reached a very high minority carrier lifetime equal to 4.13 ms and J_o of 4.7 fA/cm^2. On the other hand, for the cell precursor, the champion parameters are i-Voc of 718 mV, τ_{eff} of 3.66 ms and J_o equal to 11 fA/cm^2. As expected, the (p)poly-SiC_x samples have poorer passivation quality as compared to the (n)poly-SiC_x (section 3.5). The champion i-Voc for (p)poly-SiC_x samples is achieved at 1.0 ratio of SiH_4/NH_3 and the results are: i-Voc of 702 mV τ_{eff} of 2.80 us and J_o of 15.2 fA/cm^2. Overall, it can be also concluded that for the same composition of gases surface passivation is better achieved for n-type semiconductors than for p-type.

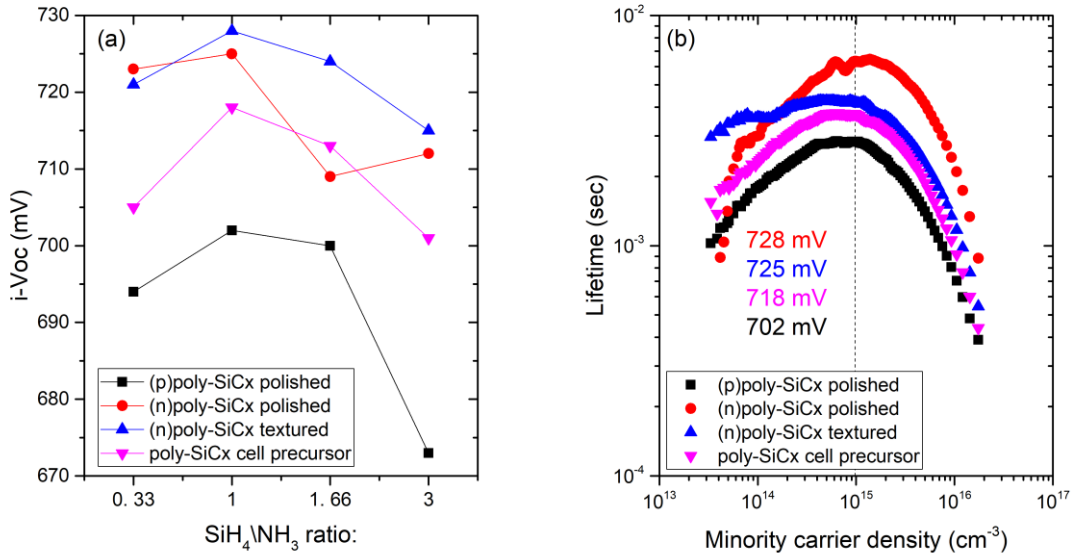


Figure 3.21 i-Voc as a function of different $SiH_4\backslash NH_3$ ratio for different passivation structures (a) and lifetime curves of samples with capping layer with $SiH_4\backslash NH_3$ ratio of 1.0 (b)

Looking at Figure 3.21(b) a significant increase in minority carrier lifetime for (n)poly-SiC_x samples with a double side polished surface is visible. The highest recorded minority carrier lifetime for (n)poly-SiC_x polished sample is equal to 6.15 ms. Besides, looking at the lifetime curves depicted on Figure 3.21(b) information about the mechanism responsible for the passivation of the sample can be obtained. Regions with low density of minority carriers (below 10^{15} cm^{-3}) are associated with field effect passivation while higher injection levels can be linked to chemical passivation (hydrogenation process) [63]. Finally, almost all samples depicted in Figure 3.21(b) apart from (n)poly-SiC_x textured one shows a decreasing of lifetime at low injection levels, signifying that field effect passivation is not optimal to surpass the surface recombination [96]. Besides once the SiN_x film will be removed it is expected that field effect passivation will disappear leading to poor passivation quality. More details regarding this aspect will be presented in section 4.5.

.

3.7 Conclusions

In this chapter, the optimization of the passivation contacts was carried out. In order to achieve the best possible passivation results, several fabrication steps have been optimized.

Firstly, annealing temperature optimization was performed for samples manufactured with an interlayer deposited by LPCVD and PECVD. Through this analysis, it was found that the best annealing temperature for samples with interlayer deposited through LPCVD is 875 °C/ 5 min while for cell precursours with films entirely deposited through PECVD the best annealing temperature is 850°C/ 5 min. Moreover, for samples with (i)a-Si:H deposited through PECVD optimum annealing conditions changed after the hydrogenation process. Finally, the best annealing temperature for these samples (cell precursors) in hydrogenated state is 800 °C/5 min.

Following, the optimum interlayer thickness for samples with (i)a-Si deposited through LPCVD and PECVD was found. The optimum (i)a-Si thickness for LPCVD process is 12 nm. The champion passivation results for this thickness are i-Voc of 713 mV, τ_{eff} of 2.14 ms and J_o of 9.5 fA/cm². The

optimization of interlayer deposited through PECVD was more complex process. Firstly, in order to optimize the PECVD deposition parameters, different deposition pressures and temperatures were tested in order to minimize the hydrogen content. The best results are obtained for the highest deposition pressure of 1.2 mbar. Afterward, for this pressure, different interlayer thicknesses were tested. It is worth to point out that the PECVD deposition process allows deposition of films independently on both sides, therefore we identify the optimal interlayer thickness values for each wafer side. For (n)poly-SiC_x samples deposited on textured surfaces, the optimum intrinsic layer thickness is found to be 15 nm and demonstrates the results i-Voc of 718 mV τ_{eff} of 2.4 ms and J_o of 7.8 fA/cm^2. On the contrary, the best optimized interlayer thickness for polished (p)poly-SiC_x symmetrical samples is set to be 10 nm. The champion passivation results for this thickness are i-Voc of 681 mV, τ_{eff} of 1.15 ms and J_o of 31.3 fA/cm^2.

The subsequent step of the passivation optimization concentrated on finding the best thickness of (p) and (n) type doped layers. Consequently, it was found that the highest i-Voc results are obtained for 30-nm thick (p)poly-SiC_x and 10-nm thick (n)poly-SiC_x layer. The champion results for these parameters with the interlayer deposited according to the previous optimization for the PECVD deposition process are i-Voc 698 mV τ_{eff} of 1.31 ms and J_o 29.3 fA/cm^2.

Lastly, in order to further increase the passivation quality, the hydrogenation process was studied. Four different gas compositions for the deposition of SiN_x capping layer were investigated. The best results is giving the stoichiometric gas composition of SiH_4 and NH_3. As a result, the parameters of the champion (n)poly-SiC_x symmetrical polished sample are i-Voc of 728 mV, τ_{eff} of 4.2ms, and J_o of 4.7 fA/cm^2.

Finally, it is important to note that despite the fact that passivation results obtained for interlayer deposited through PECVD are worse with comparison to LPCVD, the PECVD deposition method has one significant advantage. Considering industrial processes, it is more economically viable to use as little devices as possible. PECVD method allows deposition of interlayer and dopants in the same tool without the need for integration of new equipment what as a result makes the industrial process cheaper and more efficient.

4

Front Back Contacted Solar Cells

In this chapter, the poly-SiC$_x$ passivating contacts optimized in chapter 3 are implemented at device level in front back contacted solar cell. Firstly, solar cells with variable intrinsic layer thickness deposited through the LPCVD method are fabricated. For these cells also the influence of different annealing temperatures and the postannealing process is investigated. Subsequently, the influence of (p)poly-SiC$_x$ and (n)poly-SiC$_x$ thickness for cells with interlayer deposited through PECVD is examined. Finally, solar cells with different stoichiometry of deposited SiN$_x$ layer are inspected in order to identify the optimum SiN$_x$ stoichiometry that maximizes passivation quality and improve the performance of the solar cell.

4.1 Experimental details

This section presents the experimental details of fabrication of FBC solar cells. The the followed process is presented in the sketches of Figure 4.1.

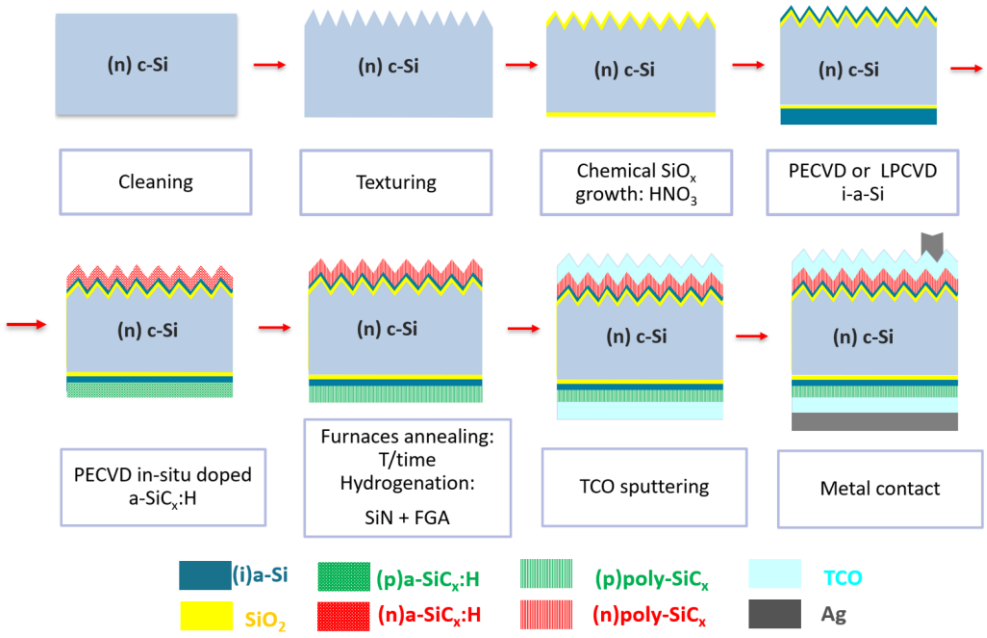


Figure 4.1 Schematic sketch of the fabrication process of FBC solar cell with poly-SiC$_x$ passivating contacts.

The bulk material is n-type c-Si FZ wafer with <100> orientation and initial thickness of 280 µm. The detailed specification of used material can be found in section 2.1.1.

1. In the first step, a 150 nm thick SiN_x layer is deposited on one side of the wafer substrate. The main role of the SiN_x layer is the protection of one surface of wafer from texturing. Subsequently, the wafer is immersed in the texturing solution of Alka-Tex and Tetramethylammonium Hydroxide (TMAH) with a temperature of 80 °C for approximately 15 minutes in order to uniformly texture the unprotected surface of the c-Si wafer. Afterward, the wafer is immersed in BHF solution until the textured surface will become hydrophobic. Finally, wafer is immersed in a poly-etch solution for approximately 2 minutes in order to round the pyramids tips and valleys present on the textured side. Lastly, wafer is again immersed in BHF solution for approximately 30 minutes until the SiN_x protective layer will be completely etched away.
2. The wafer is cleaned according to the cleaning process described in section 2.1.2 in order to remove organic and inorganic contaminations.
3. Tunneling oxide is grown through immersion of wafer in 69.5 % HNO_3 solution at room temperature for 60 minutes.
4. Subsequently, (i)a-Si layer is deposited by PECVD or LPCVD deposition method (section 2.1.4).
5. Doped a-SiC_x: H layers are deposited by PECVD.
6. High-temperature annealing is performed at temperatures of 850 °C/5 min or 875°C for cells with (i)a-Si deposited through LPCVD and at a temperature of 800 °C/5 min for (i)a-Si:H deposited through PECVD.
7. Subsequently, the hydrogenation step is performed using a 100-nm thick SiN_x capping layer deposited through PECVD on both sides of the wafer. Afterward, FGA is carried out at 400 °C for 30 minutes. After the hydrogenation step the wafer is immersed in BHF batch for 5-30 minutes to etch the SiN_x capping layer.
8. Following ITO is sputtered through a metal mask to define the cell area of 3.92 cm^2. On the front, ITO with a thickness of 75 nm is deposited while a thickness of 150 nm is deposited on the rear side.
9. Lastly, the metallization process is performed through Screen printing (SP) using a low temperature silver paste. The rear side of each cell is fully metallized while for the front grid a screen with different metal coverage is used (Figure 2.7). After SP, the wafer is annealed in an oven for 30 minutes at 200°C for each side. Finally, post-annealing treatment is performed using the hot plate for 5 min at 350°C.

4.2 Effect of (i)a-Si interlayer thickness (LPCVD)

The objective of the first set of experiments carried out on a device-level, is the investigation of the influence of various (i)a-Si layer thicknesses and different annealing temperatures on solar cell performance. For the analyzed cells, (i)a-Si interlayer was deposited through the LPCVD method in the same deposition run on both sides of the wafer. Three different thicknesses 8 nm, 12 nm, and 14 nm are studied. Similarly, as it was explained in section 3.3.1, the interlayer thickness refers to the flat surface, while on the textured surface the layer is thinner with a corrective factor of 1.7. After the deposition of doped layers, the cell precursor is annealed in temperatures of 875 °C or 850 °C for a duration of 5 minutes.

After each individual fabrication step, the cell precursors are checked in terms of passivation quality. The values of i-Voc measured after each fabrication steps are depicted on Figure 4.2(a). Firstly, looking at Figure 4.2(a) it is visible that (i)a-Si thickness of 12 nm is outperforming other studied thicknesses after each fabrication step. Moreover, it is important to note that the most significant i-Voc difference occurs between the as-deposited and annealed state (Δi-Voc of 109 mV). The i-Voc increase is a direct result of the change of layer structure: crystallization of (i)a-Si layer and doped layer stack. As it was described in section 1.2, doped poly-Si have superior electrical properties over a-Si. Following, the best measured values for i-Voc are achieved after the hydrogenation step when the dangling bonds are saturated by the hydrogen atoms. The champion i-Voc during this process is obtained for (i)a-Si thickness of 12 nm (i-Voc of 713 mV). After the deposition of TCO, a significant decrease in i-Voc is present especially for (i)a-Si thickness of 8 nm. This degradation can be linked to the sputtering damage that occurs during the ITO deposition [101]. The highest i-Voc decrease of 20 mV is recorded for the thinnest buffer layer (8 nm) and n-layer 10 nm, which indicates that this layer is not thick enough to protect the structure from sputtering damage . On the other hand, the lowest sputtering damage is recorded for the thickest buffer layer of 14 nm (Δi-Voc of 9 mV), which confirms that in terms of sputtering damage thicker layers are more restive and better protect the junction. Nevertheless, as it was presented above after the hydrogenation the worst results are obtained for this-thickest layer. The final Voc of the cells is in a range of 678-642 mV. The lower values of the final Voc of the cells can be correlated to metal deposition technique, the blisters formation and the series resistance which can suppress the passivation quality [101].

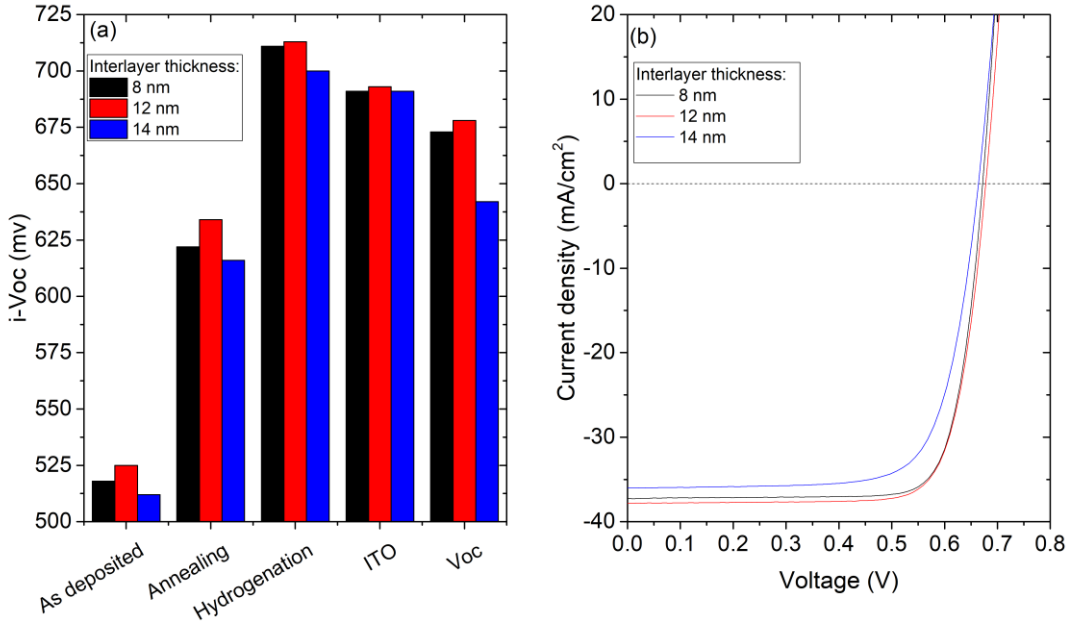


Figure 4.2 i-Voc as function of fabrication step of cell precursors with variable (i)a-Si thickness annealed at 875 °C for a duration of 5 minutes (a) and J-V curves of final cells annealed at 875 °C for a duration of 5 minutes with different thickness of (i)a-Si measured byt the solar simulator (b).

On Figure 4.2(b) are depicted J-V curves under standard illumination conditions. It is clearly visible that (i)a-Si thickness of 14 nm is giving considerably worse results than other investigates

thicknesses (8 nm and 12 nm). The contacts of sample with 14 nm (i)a-Si thickness are suffering from a lower FF with comparison to other studied thicknesses.

Figure 4.3 presents the parameters of solar cells fabricated with variable thicknesses and annealed at different annealing temperatures. Voc and FF have been measured by solar simulator (section 2.2.2) and J_{sc} was calculatedf from EQE (section 2.2.2). Firstly, looking at each graph of Figure 4.3, it is visible that better results are obtained for the annealing temperature of 875 °C. A similar trend was investigated during the analysis of the passivation tests (section 3.2.1). Moreover, looking at Figure 4.3(a)-(c) it is visible that the results achieved for the interlayer thickness of 12 nm are the most stable when it comes to the annealing temperature with comparison to cells with other buffer layer thickness. On the contrary, the biggest deviation of parameters is recorded for (i)a-Si thickness of 14 nm. Nonetheless, this can be correlated with the experimental error since TCO deposited on sample with 14 nm buffer layer annealed at 850 °C had, unintentionally, a lower thickness with comparison to other samples. This is most probably the result of the disturbtion, which occurred during the TCO deposition. Consequently, it can be the possible reason of the deteriorated performance as the lateral conductivity of ITO can be to low to ensure collection of charges. Figure 4.3(a) depicts the same trend as Figure 4.2(a). The highest Voc values are obtained for a thickness of 12 nm- champion Voc 678 mV. Considering the annealing temperature, as it was mentioned before in the study of passivation contacts (section 3.2.1), the temperature of 875 °C gives the best results. Following, looking at Figure 4.3(b) that depicts the J_{sc} variation the champion value is achieved for (i)a-Si thickness of 12 nm annealed at 875 °C (36.47 mA/cm^2). Afterward, looking at Figure 4.3(c), significant difference in the FF of the sample with (i)a-Si of 14 nm annealed at 850 °C is visible (FF of 52.22 %). The explanation of this trend is the fact, that this is the cell on which ITO with lower thickness was deposited (experimental error). Finally, looking at the efficiencies of studied cells, the highest efficiency of (19.83 %) is recorded for cell annealed at 875°C with (i)a-Si of 12 nm. Nonetheless, significantly high efficiency was also obtained for a cell with a buffer layer thickness of 8 nm (19.48%). The worst efficiency is achieved for the cell with a buffer layer of 14 nm, this cell is behaving worse than other cells in every annealing temperature and thickness investigated. The champion efficiency of the cell with (i)a-Si thickness of 14 nm is 15.85 % and is lower than the efficiencies obtained for other thicknesses at an annealing temperature of 850 °C (12 nm η of 19.28 % and 8 nm η of 17.77 %). These results indicate that the buffer layer of 14 nm might not allow the efficient diffusion of dopants leading to the deteriorated field-effect passivation and consequently lower efficiency.

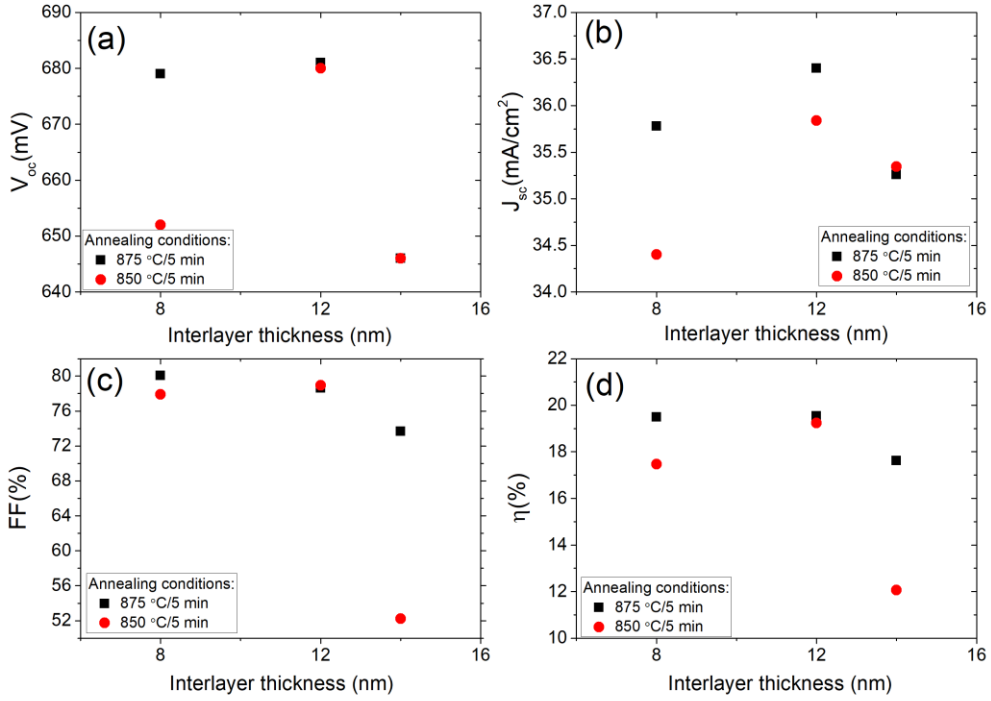


Figure 4.3 Voc of cells with variable (i)a-Si thickness at different annealing temperatures (a) J_{sc} of cells with variable (i)a-Si thickness at different annealing temperatures measured by EQE (c) FF of cells with variable (i)a-Si thickness at different annealing temperatures and (d) Efficiency of cells with variable (i)a-Si thickness at different annealing temperatures.

Lastly, the optical characterization of the cells was performed. For this characterization, the EQE and reflection measurements have been carried out. The EQE and (1-R) curves of the cells are depicted in Figure 4.4. The EQE curves are very similar with a common trend. Nonetheless, looking at the thicker layer (14 nm) a small loss in EQE can be observed in the low wavelength range which is better visible in Figure 4.4(b). This deteriorated performance of thicker (i)a-Si layer, especially in short wavelength region can be attributed to the higher absorption of high energy photons for thicker buffer layer at the front of the device what results in higher parasitic absorption losses and consequently lower J_{sc} values. On the other hand, in the longer wavelength region of the EQE measurements, high optical losses can be observed, which can be correlated with the low energy photons not being absorbed by the cell, thus they are propagating through the material without any contribution to the J_{scEQE}, Finally, it is worth to point out that 1-R curves are almost identical for all fabricated cells.

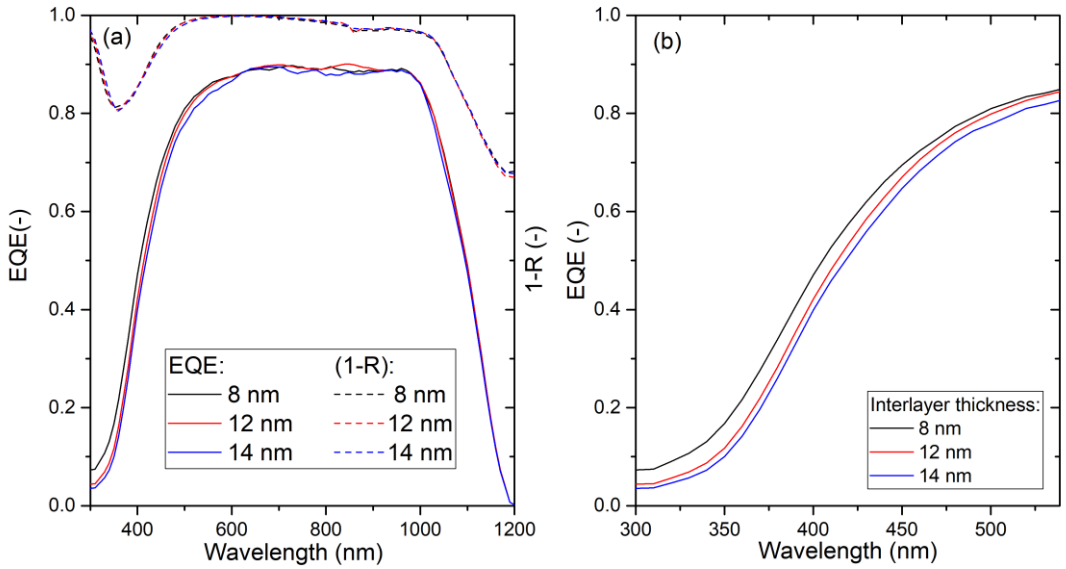


Figure 4.4 EQE and (1-R) curves of fabricated solar cells with variable interlayer thickness in the whole range of wavelength (a) EQE curves of fabricated solar cells in the short wavelength region (b).

Post annealing effect

The last step of the fabrication process is post-annealing of the finished solar cells. As it was presented by Feldmann et al. [102] for poly-Si cells, an effective curing of the solar cell can be achieved at ~350 °C. In order to perform this step cells were placed on a hot plate for a duration of 5 minutes at the temperature of 350°C. The obtained results are presented in Figure 4.5 and Table 4.1 where they are compared to the initial performance values. The effect of the post-annealing process was studied on cells annealed at a temperature of 875°C as this annealing temperature was giving better cell results than 850 °C.

Looking at Figure 4.5, it is clearly visible that the curing process has a positive effect on solar cell electrical performance. Each of the investigated parameter is affected by the curing process with an increase of values. Similar results have been recorded by the other groups [102], they have proved that curing temperature till 400 °C can effectively restore the surface passivation. The most important impact of the post-annealing process is recorded for FF values. It is known that the FF is influenced by the series resistance that comes from the contact resistance between the junction and electrodes, and the resistance of the electrodes themselves [103]. Consequently, the higher the FF, which is recorded after the curing process the lower the contact resistance between the electrodes and junction and lower the resistance of the electrode. The champion FF after 350°C curing has a value of 80.02 % and is obtained for a cell with (i)a-Si thickness of 8 nm. It is an increase of 0.88 $\%_{abs}$ with regard to the initial value of 79.14 %. On the other hand, the most significant variation of FF is recorded for the buffer layer thickness of 12 nm with +2.37 $\%_{abs}$ improvement.

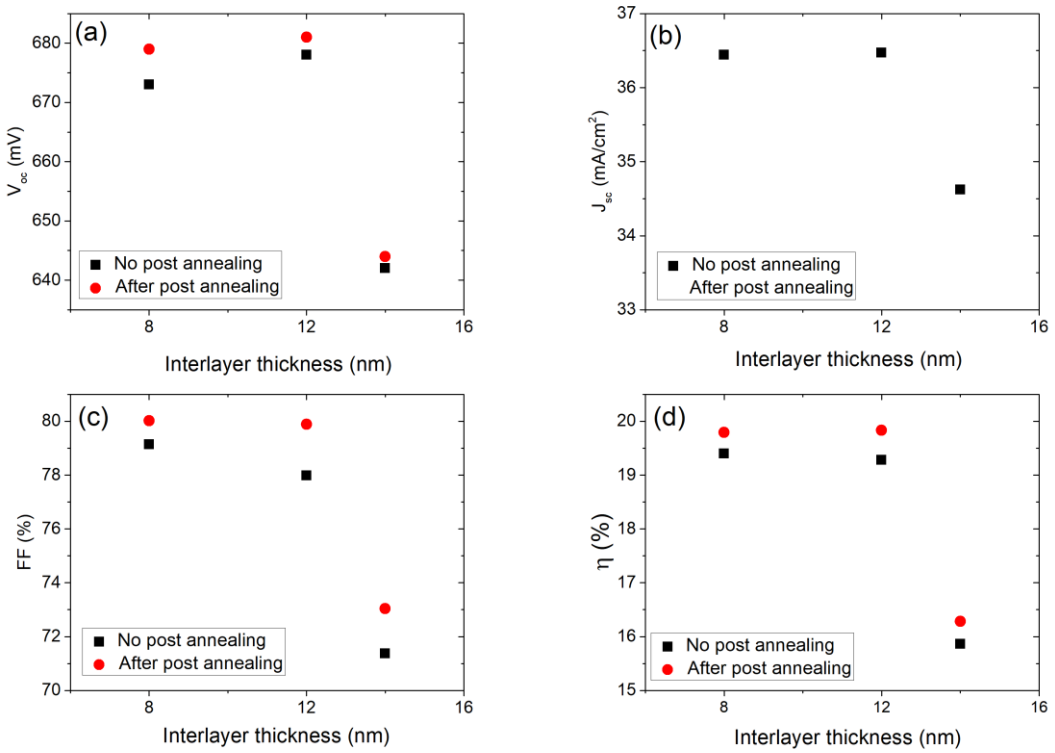


Figure 4.5 Voc of cells with variable (i)a-Si thickness before and after post annealing treatment at 350°C for 5 min (a) J_{sc} of cells with variable (i)a-Si thickness before and after post annealing treatment (b) FF of cells with variable (i)a-Si thickness at before and after post annealing treatment (c) Efficiency of cells with variable (i)a-Si thickness before and after post annealing treatment (d).

Table 4.1 presents the detailed values of the solar cell parameters before and after the curing process. Looking at Figure 4.5 and Table 4.1 it is worth to point that the J_{sc} measured through EQE did not change after the post-annealing process. The obtained value of 36.47 mA/cm^2 (12 nm thickness) measured before the high temperature curing coincide with the result obtained after this process (not shown here), consequently it can be agreed that curing does not affect the EQE output. Considering the cell that performs the worst, (i)a-Si thickness of 14 nm, a significant variation of FF values after the post-annealing process is recorded (ΔFF of 2.33 %). This improvement has a significant effect on studied actual solar cell efficiency that increased by 2.58 %. Nonetheless, even after curing the cell with (i)a-Si thickness of 14 nm (η_{act} of 16.28%) is still the worst-performing one between different analyzed thicknesses of 8 nm and 14 nm (η_{act} of 19.79 % and 19.83 %). This means that the post-annealing process cannot improve the deteriorated passivation quality of this cell completely. Finally, the record actual efficiency obtained in this experiment is 19.83% and is achieved for (i)a-Si thickness of 12 nm, the cell that achieved the champion values also before the post-annealing process.

Table 4.1 Summary of parameters of solar cells before and after post annealing treatment.

(i)a-Si (nm)	V_{oc} (mV)		FF (%)		J_{scEQE} (mA/cm²)	η_{act} (%)	
8	673	679	79.14	80.02	36.44	19.40	19.79
12	678	681	77.98	79.88	36.47	19.28	19.83
14	642	644	71.37	73.04	34.62	15.86	16.28

Before post annealing | After post annealing

4.3 Influence of (p)poly-SiC$_x$ thickness

In this set of experiments, the influence of different (p)poly-SiC$_x$ thicknesses and (i)a-Si:H layer deposited through the PECVD method is investigated. The thickness of (i)a-Si:H layer deposited through PECVD method vary with regards to flat and textured side. The buffer layer deposited on the flat side has a thickness of 10 nm, on the contrary on the textured side the deposited interlayer has a thickness of 15 nm, as these thickness values were giving the best passivation results (section 3.3.2). Consequently, in this set of experiments the advantage of the PECVD deposition method was used, as thanks to PECVD deposition, it is possible to optimize the thickness of the deposited layer separately on each side. Moreover, deposition of (i)a-Si: through PECVD is making the whole process easier, less complex, so it its profitable to apply it for industrial solutions since it is possible to deposit (i)a-Si and doped layers in one device. The thickness of (p)poly-SiC$_x$ layer was varied between 30-100 nm, while the (n)poly-SiC$_x$ thickness was kept at a constant value of 10 nm. After the deposition of doped layers, the whole structure was annealed at a temperature of 800 °C for 5 minutes, since as it was presented in section 3.2 to be the optimal temperature for buffer layer deposited by PECVD.

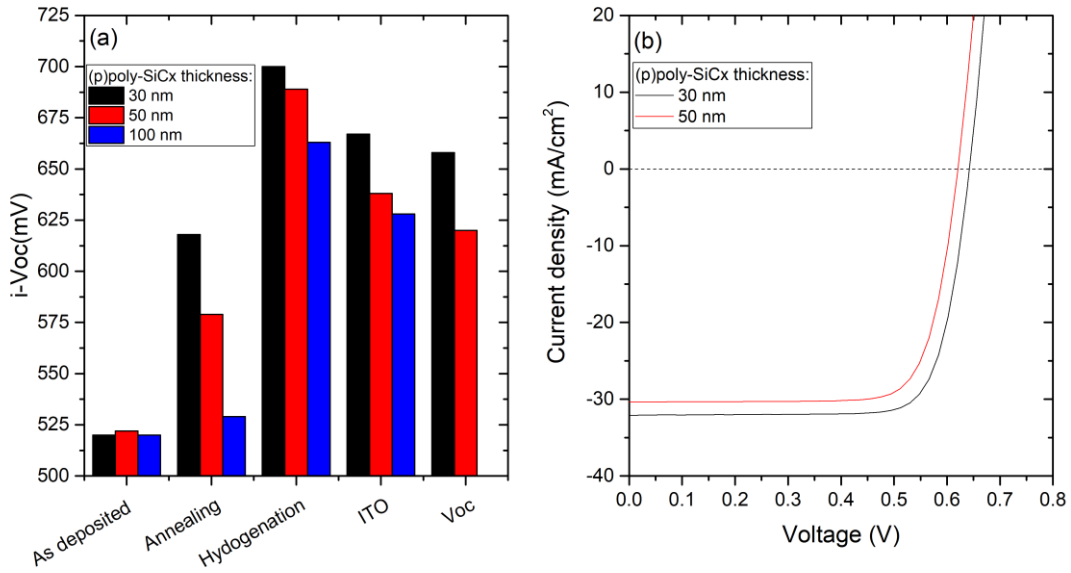


Figure 4.6 i-Voc variation of cell's precursors after each of the fabrication steps (a) and J-V curves of final cell (b).

The i-Voc change of cell precursors is depicted in Figure 4.6(a). In the as-deposited step, cell precursors achieve similar i-Voc between 520 mV and 522 mV. Subsequently, after the annealing process, a significant boost in i-Voc is visible, almost 100 mV change in i-Voc is recorded for (p)poly-SiC_x with a thickness of 30 nm. In contrast to the buffer layer deposited through LPCVD (section 4.2) where the most significant increase in i-Voc occurred between as deposited and annealed state, here the biggest i-Voc growth is present between annealed and hydrogenated state (ΔVoc=110 mV). The possible reason for this can be the fact that buffer layers deposited through the PECVD method are hydrogen-rich (section 3.2.2) During the annealing process hydrogen incorporated in buffer layer effuses leaving unsaturated dangling bonds on the wafer surface. After the hydrogenation the remained dangling bonds are saturated with hydrogen, which is coming from used hydrogen-rich gasses [104], which consequently surpass the surface recombination losses. Consequently, the highest i-Voc of 700 mV is obtained for the cell precursor in the hydrogenated state with (p)poly-SiC_x of 30 nm. After the ITO deposition, a significant decrease in i-Voc is recorded (Δi-Voc of 35 mV) for cell precursor with (p)poly-SiC_x thickness of 50 nm. This drop in i-Voc can be caused by the sputtering damage, which occurs during the ITO deposition [99]. It is important to point that for cells with a buffer layer deposited through PECVD sputtering damage is more significant with comparison to the cells with buffer layer deposited through LPCVD (section 4.2). Besides, high sputtering damage occurs for thicker (p)poly-SiC_x layers (50 nm, 100 nm) which is not expected as a thicker layer should better protect the junction from the sputtering. The highest i-Voc drop for cells with interlayer deposited through PECVD is 35 mV while for cells with interlayer that comes from LPCVD the most significant i-Voc drop is 20 mV. The possible reason of the more significant i-Voc drop for samples with buffer layer deposited through PECVD is the fact that the buffer layer deposited through PECVD method has lower homogeneity than (i)a-Si deposited through LPCVD. Furthermore, possible local damages of the PECVD buffer layer structure, which are a result of the hydrogen effusion during the annealing process can also lead to the higher porosity in this layer. Consequently, the buffer layer deposited through PECVD is not strong enough to protect the junction from sputtering damage.

Finally, as it is presented on Figure 4.6(a), the final Voc of the cell extracted from J-V curves, after the screen printing process has been obtained only for a cells with (p)poly-SiC_x thickness of 30 nm and 50 nm. The cell with (p)poly-SiC_x thickness of 100 nm gives the Voc curve which is not a diode, therefore no Voc was measured. The possible hypothesis for the deteriorated performance of the solar cell with (p)poly-SiC_x thickness of 100 nm is the fact that thick doped layer needs more doping optimization. The J-V curve of these cells is presented on Figure 4.6(b). Looking at this figure it is clear that better performance has a cell with (p)poly-SiC_x thickness of 30 nm. Moreover, no S-shape is recorded for the measured cells.

Post annealing effect

Similar to the cells with buffer layer deposited through LPCVD (section 4.2), also the cells presented in this section undergo to post-annealing. Figure 4.7 depicts the results obtained on cells with variable (p)poly-SiC_x thickness before and after the curing process at 350°C for a duration of 5 minutes.

Looking at Figure 4.7 it is visible that the curing process has a positive influence on each parameter of the solar cell apart from the J_{sc} measured through EQE, as J_{sc} was not affected after the curing at 350°C for 5 minutes. Firstly, looking at Figure 4.7(a), small changes in Voc are visible. For the

cell with (p)poly-SiC_x thickness of 30 nm, the increase in Voc is only 2 mV, consequently it can be said that no clear effect on Voc is present after the post-annealing. On the contrary, the FF variation is more significant, the increase of 1.8 % occurred for a cell with (p)poly-SiC_x layer of 30 nm. Slightly lower FF increase is recorded for the cell with 50-nm thick (p)poly-SiC_x with a ΔFF of 1.62%. Finally, looking at Figure 4.8(d), the highest efficiency is achieved after the high-temperature curing for the cell with (p)poly-SiC_x thickness of 30 nm and is equal to 17.58 %. The detailed values of each measured parameter of the cell are given in Table 4.2.

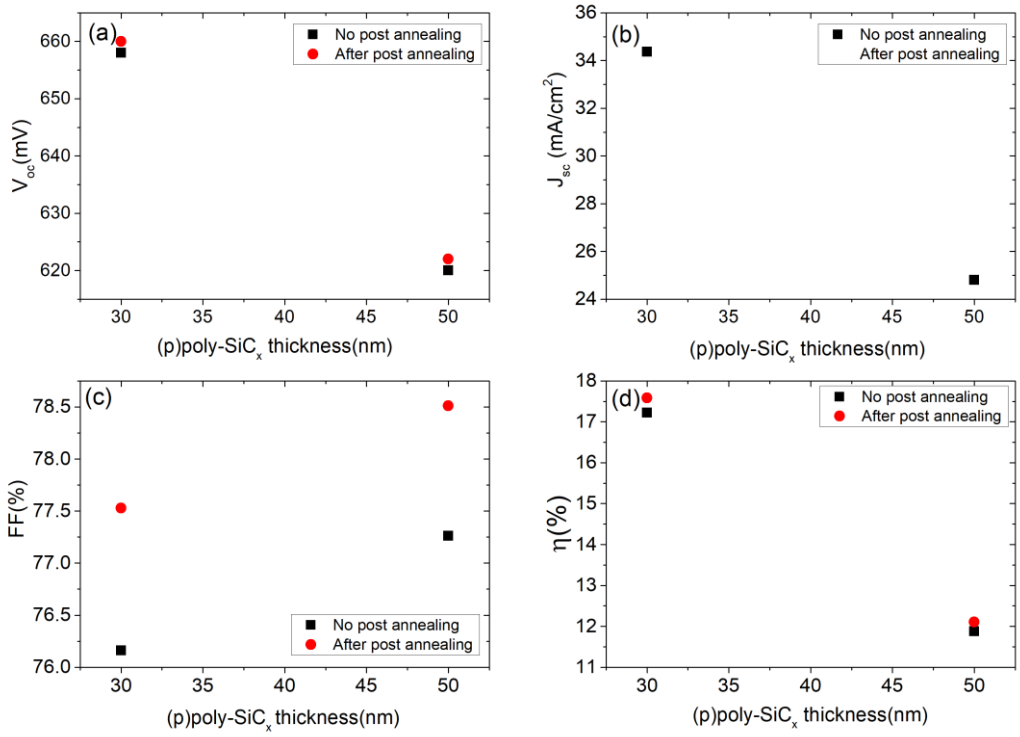


Figure 4.7 Voc of cells with variable (p)poly-SiC_x thickness before and after post annealing treatment (a) Jsc of cells with variable (p)poly-SiC_x thickness before and after post annealing treatment (b) FF of cells with variable (p)poly-SiC_x thickness at before and after post annealing treatment (c) Efficiency of cells with variable (p)poly-SiC_x thickness before and after post annealing treatment (d).

Table 4.2 Summary of parameters of solar cells before and after post annealing step.

(p)poly-SiC_x (nm)	**V_{oc} (mV)**		**FF (%)**		**J_{scEQE} (mA/cm²)**	**η_{act} (%)**	
30	658	660	76.16	77.53	34.36	17.22	17.58
50	620	622	77.26	78.51	24.8	11.88	12.11

Before post annealing	After post annealing

4.4 Influence of (n)poly-SiC_x thickness

Following the investigation of (p)poly-SiC_x thickness variation, the influence of different (n)poly-SiC_x thicknesses is also studied. The thickness of (n)poly-SiC_x layer was varying in a range of 5-15 nm. Moreover, in this set of experiments the buffer layer was deposited through the PECVD deposition method. The reason for the deposition of the buffer layer through PECVD is the investigation of the possible application of this deposition method in the industry, since the PECVD allows us to optimize the layer thickness on both sides; textured and flat one. Furthermore, deposition of (i)a-Si: through PECVD is making the whole process easier, less complex, so it its profitable to apply it for industrial solutions since it is possible to deposit (i)a-Si and doped layers in one device. As a consequence of the optimization performed in section 3.3.2, on the flat side the deposited (i)a-Si:H has a thickness of 10 nm, on the contrary on the textured side the interlayer has a thickness of 15 nm. After the deposition in PECVD the whole structure was annealed at 800 °C for a duration of 5 minutes.

The i-Voc of cell precursors after each fabrication step is depicted on Figure 4.8(a). Similarly, as it was observed for the previous set of experiments (section 4.3) the hydrogenation step significantly increases the i-Voc of the cells. The record i-Voc after the hydrogenation step has been obtained for the cell precursor structure with (n)poly-SiC_x thickness of 10 nm (i-Voc of 700 mV). Moreover, it is clearly visible that during the whole fabrication process (n)poly-SiC_x thickness of 5 nm is behaving the worst. The possible reason for this can be the fact that 5 nm layer is too thin to create a strong enough electric field which is responsible for one of the transport mechanisms-drift of the charge carriers [105]. Therefore, the resulting electric field from a very thin layer does not create enough drift force, thus a portion of the photogenerated charge carriers will recombine. Other possible hypothesis is the fact that doped layers deposited by PECVD are of low homogeneity, hence the layer can be locally thinner than the nominal 5 nm thickness. As it can be seen, a thicker (n)poly-SiC_x layer of 15 nm also has deteriorated performance with comparison to the best thickness of 10 nm. Besides that, after the deposition of ITO a significant sputtering damage occurred for every (n)poly-SiC_x thickness. Nevertheless, the most significant decrease is recorded for 5 nm thickness of (n)poly-SiC_x layer. This can be linked to the fact that doped layer is too thin, and consequently suffers from the sputtering damage the most- the i-Voc drop of 36 mV with regard to the previous process. On the other hand, the thickest (n)poly-SiC_x layer of 15 nm suffers from the sputtering damage the least, which means that thicker doped layer provides better protection against sputtering damage, what it was not true in case of thickest (p)poly-SiC_x layer.

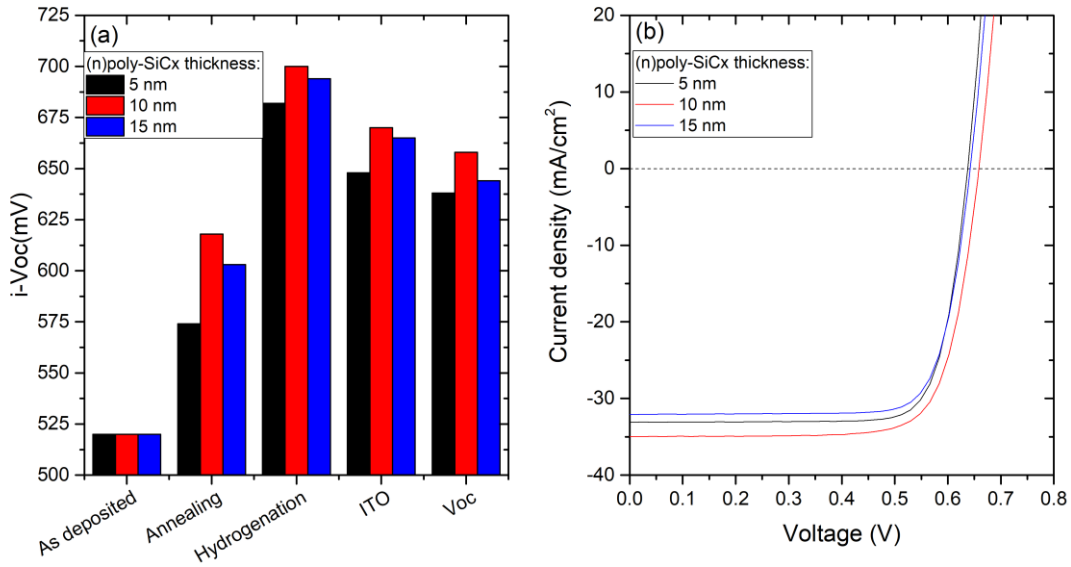


Figure 4.8 i-Voc change of cell's precursors after each of the fabrication steps (a) and J-V curves of final cell (b)

Figure 4.8(b) presents J-V curves obtained from the measurements performed under the solar simulator. It is visible that cell with (n)poly-SiC_x thickness of 15 nm is giving considerably worse results, but similar to the (n)poly-SiC_x thickness of 5 nm. Nevertheless, among the measured cells no S-shape is observed at the illuminated J-V curve.

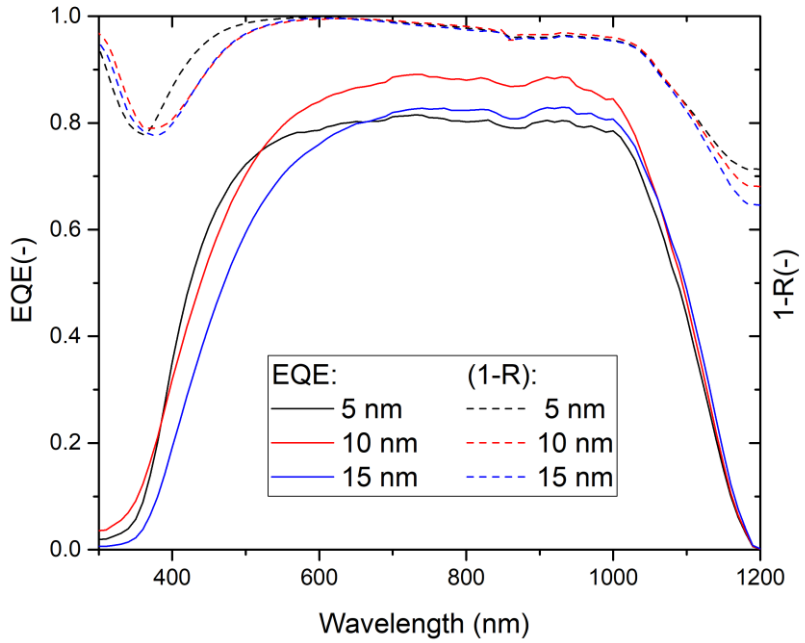


Figure 4.9 EQE and (1-R) curves of fabricated solar cells with variable (n)poly-SiC_x thickness in the whole range of wavelength.

The EQE and (1-R) curves of the manufactured cells are presented on Figure 4.9. Looking at EQE curves it is clearly visible that in the low wavelength region higher parasitic absorption losses of

high energy photons are present for the cell with thicker (n)poly-SiC_x layer. Significant difference is present between the (n)poly-SiC_x thickness of 5 and 15 nm. Furthermore, in the long wavelength region, high optical losses are observed (EQE drop), which can be correlated with the non absorption of low energy photons, thus these photons are propagating through the material without any contribution to the J_{scEQE} and also higher recombination losses. Finally, it is worth to point that that 1-R curves of all fabricated cells are following the same trend. Nevertheless, the cell with 5 nm thick (n)poly-SiC_x layer show lower absorption in the lower wavelength region of the spectrum. This observation can be related to too thin (n)poly-SiC_x layer thickness (5 nm).

Post annealing effect

Similar to the previous section, on cells analyzed in this section also the high temperature post treatment was studied. Figure 4.10 depicts the results obtained on cells with variable (n)poly-SiC_x thickness before and after the post-annealing process. Looking at Figure 4.10, it is visible that the post-treatment process has a positive influence on each of the measured parameters apart from J_{sc} measured through EQE. The highest Voc increase after the curing process is present for the cell with (n)poly-SiC_x thickness of 15 nm (ΔVoc= 4 mV). On the contrary, for this cell FF changes are the smallest (ΔFF= 0.54 %). Overall, the best results before and after the curing process was obtained for a cell with 10-nm thick (n)poly-SiC_x layer, the record efficiency for this cell is equal to 17.56 % with 0.34 % improvement with regard to the result obtained before the post-annealing process. This efficiency increase is mainly FF driven as presented in Figure 4.11(c), the biggest increase in FF values is present for (n)poly-SiC_x thickness of 10 nm and is equal to 0.43%. The detaile values of the parameters obtained before and after the curing process are present in Table 4.3.

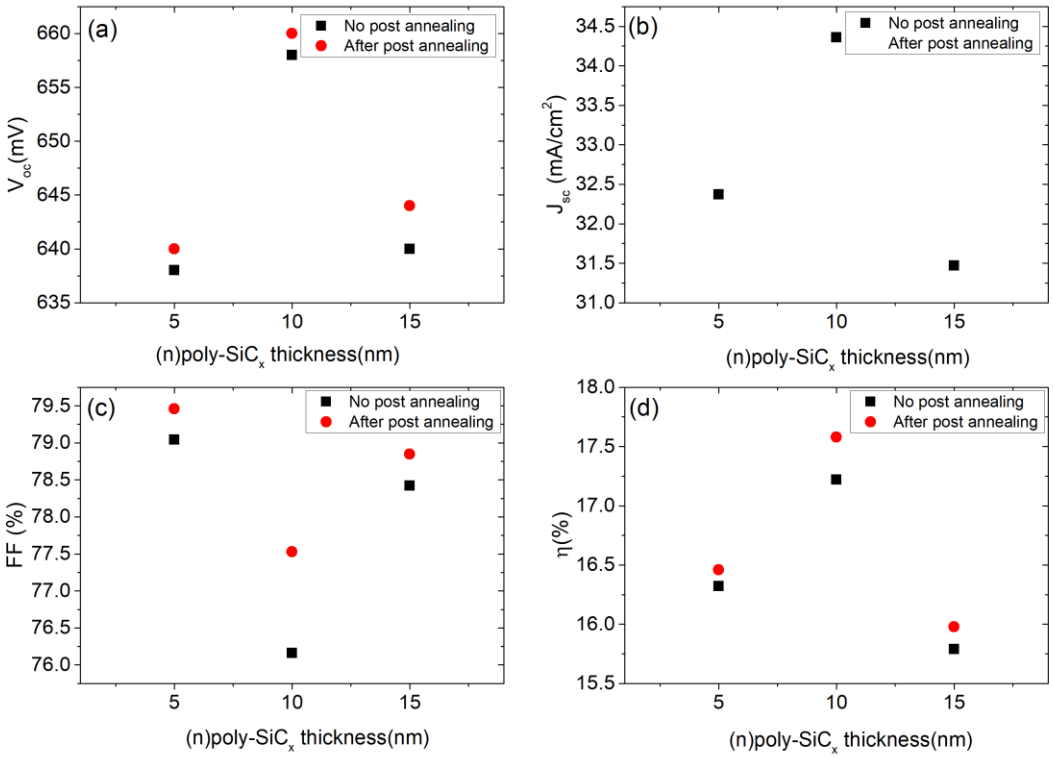


Figure 4.10 Voc of cells with variable (n)poly-SiC_x thickness before and after post annealing treatment (a) Jsc of cells with variable (n)poly-SiC_x thickness before and after post annealing treatment (b) FF of cells with variable (n)poly-SiC_x thickness at before and after post annealing treatment (c) Efficiency of cells with variable (n)poly-SiC_x thickness before and after post annealing treatment (d).

Table 4.3 Summary of the parameters measured before and after the post annealing step.

(n)poly-SiC_x	**V_{oc} (mV)**		**FF (%)**		**J_{scEQE} (mA/cm²)**	**η_{act} (%)**	
5	638	640	79.04	79.46	32.37	16.32	16.46
10	658	660	76.16	77.53	34.36	17.22	17.56
15	640	644	78.42	78.85	31.47	15.79	15.98

Before post annealing	After post annealing

4.5 Influence of SiN_x stiochiomoetry

Finally, in the last set of experiments we aim to investigate the influence of different hydrogenation gas composition on passivation quality. The cell precursors had a buffer layer of 12 nm deposited by LPCVD method. After the deposition of doped layers (30 nm (p)poly-SiC_x and 10 nm (n)poly-SiC_x), the whole structure was annealed in temperatures of 875 °C for 5 minutes. Subsequently, during the hydrogenation process, different gas compositions during SiN_x deposition were tested (Table 4.4). After the hydrogenation process, cell precursors with variable SiN_x layer were immersed in BHF solution in order to etch away the SiN_x layer. The deposited SiN_x film is removed

in BHF solution as the main purpose of the applied capping layer is to provide high passivation quality not antireflection coating [96].

Table 4.4 Gas mixture and gas ratios used for deposition of SiN_x layers.

SiH_4 (sccm)	NH_3 (sccm)	SiH_4/NH_3 ratio
10	30	0.33
20	20	1.00
25	15	1.66
30	10	3.0

After each fabrication step, cells were checked in terms of passivation quality (Figure 4.11 (a)). Looking at Figure 4.11(a), it is clearly visible that the biggest i-Voc difference occurs between the as-deposited and annealed state (Δi-Voc of 126 mV). The i-Voc increase is a direct result of the change of layer structure: crystallization of (i)a-Si layer and doped layer stack. Subsequently, the highest values of i-Voc are achieved after the hydrogenation step in which different composition of gases was used to obtain SiN_x films with variables x (section 3.6.1). Looking at the i-Voc measured after the hydrogenation process the best i-Voc value is achieved for the film deposited at SiH_4/NH_3 ratio of 1.0 (i-Voc of 708 mV). On the contrary, the lowest i-Voc has been obtained on cell precursors on which the ammonia-rich layer (ratio of 0.33) and silane-rich layer (ratio of 3.0) were deposited. The obtained i-Voc for both cell precursors reached a value of 700 mV. The achieved results follow the trend presented in section 3.6.3, where the hydrogenation gas composition influence on passivation quality was studied. Furthermore, looking at Figure 4.11(a) it can be seen that the i-Voc variation after the hydrogenation process is not significant, the difference between the obtained i-Voc values does not exceed 8 mV. Similarly to the previous experiments (section 4.2 and section 4.3), we observe an i-Voc drop after the ITO deposition which is a consequence of sputtering damage. Nonetheless, the i-Voc drop after the ITO deposition in this set of experiments is less significant that the one presented in section 4.3. The main reason for this is the fact that for currently analyzed samples buffer layer was deposited through LPCVD, which is of higher density and homogeneity with comparison to the intrinsic layer deposited through the PECVD method. Finally, looking at the Voc values obtained after the metallization, it is clearly visible that the cell in which the nitrogen rich capping layer (SiH_4/NH_3 ratio of 0.33) was deposited is performing the worst. On the contrary, cells on which the SiN_x layer with high silane content was deposited are giving better results. This can be the direct consequence of the fact that this layer is hydrogen-rich (Figure 3.19), consequently provides high passivation quality. The best Voc of 677 mV is achieved for the cell which was hydrogenated with silane rich gas (3.0 ratio). In order to explain the deteriorated performance of the sample which was hydrogenated in nitrogen-rich gas, it is important to analyze the minority carrier lifetime curves.

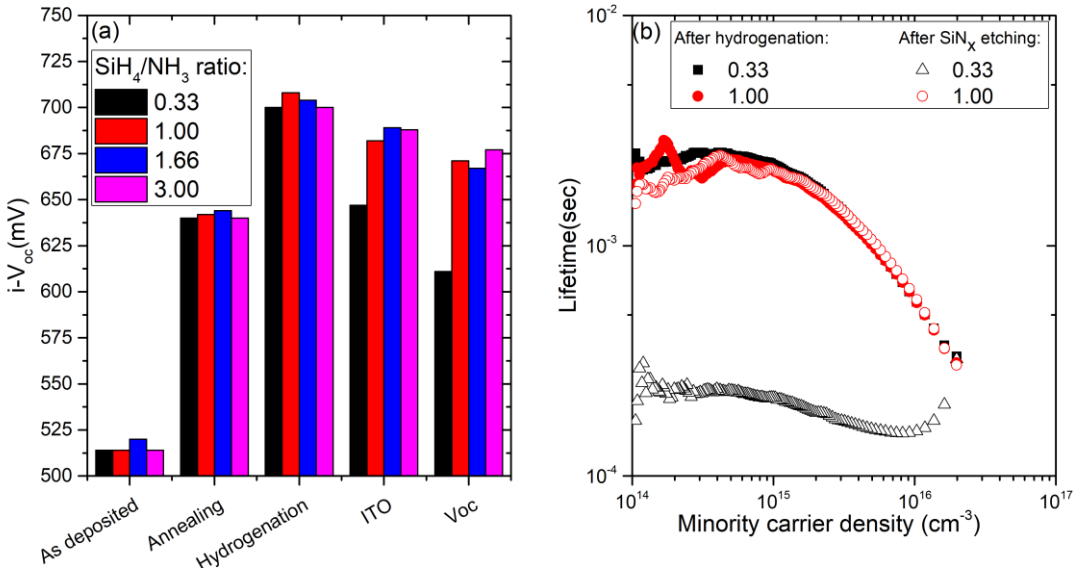


Figure 4.11 i-Voc change of cell's precursors after each of the fabrication steps (a) and lifetime for two different SiH_4\NH_3 ratios for cell precursors before and after etching of the SiN_x layer (b).

Figure 4.11(b) depicts the lifetime of minority charge carries as a function of two different SiH_4/NH_3 ratio before and after the etching of the SiN_x film. Looking at Figure 4.12(b) it is visible that cell precursor on which the stoichiometric capping layer was deposited is achieving better τ_{eff} and are not influenced by the SiN_x etching process. The highest τ_{eff} after the etching of the SiN_x capping layer is recorded for cell precursor with 1.0 composition of gases and is equal to 2.2 ms. Nonetheless, it is important to note, that after etching of SiN_x layer with high nitrogen content(0.33 gas ratio) very low τ_{eff} equal to 0.22 ms is measured as well as significant i-Voc drop (Δi-Voc=54 mV). The possible explanation of this can be the fact that for nitrogen rich films the mechanism that is driving the passivation is field effect passivation not chemical passivation [96]. If the nitrogen content is relatively high the N-rich films induce a significant amount of field-effect passivation with fixed positive charge densities in the magnitude of 10^{12} cm^{-2}. Consequently once the nitrogen-rich SiN_x films are etched away the main passivation mechanism disappears, which as a result leads to low minority carrier lifetime and deteriorated solar cell output [96]. On the contrary, the Si-rich films represent amorphous like properties [97]. For Si-rich films, a high level of passivation is maintained by chemical passivation, when the dangling bonds are saturated with hydrogen atoms that are coming from hydrogen-rich gases (SiH_4 and NH_3). Therefore, for Si-reach films after the etching of the capping layer (Figure 4.11(b)) no significant drop in τ_{eff} is recorded.

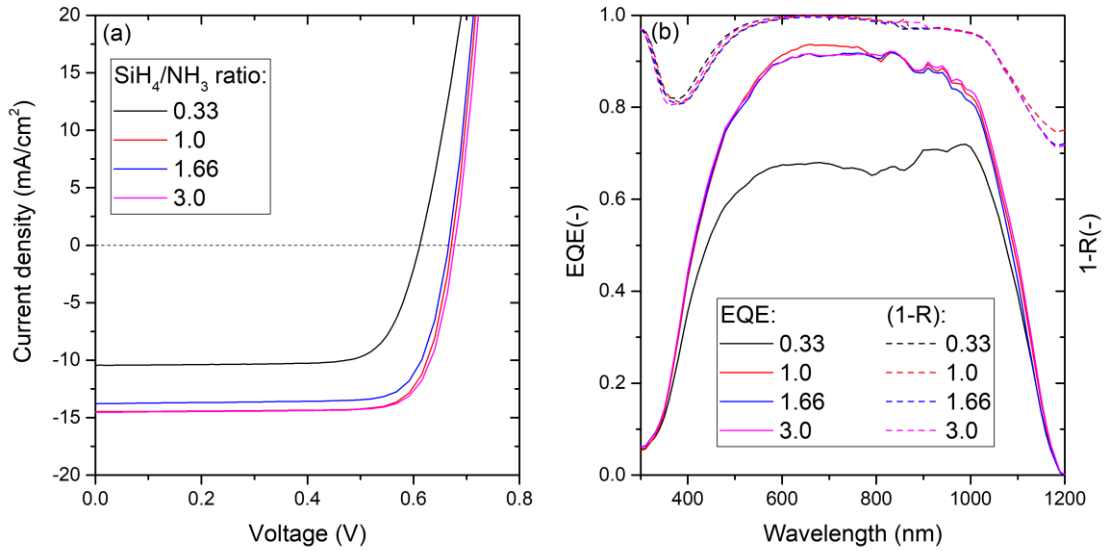


Figure 4.12 J-V curve of fabricated cells as a function of different SiH_4\NH_3 ratio of gases used for hydrogenation process (a) and EQE curves of fabricated solar cells with variable SiH_4/NH_3 ratio used for hydrogenation process in the whole range of wavelength (b).

Figure 4.12(a) depicts the J-V curves of manufactured cells. As it can be observed no S-shape is recorded. Nonetheless, it is visible that cell which was hydrogenated at nitrogen rich gas is performing worse that other studied cells. This can be attributed to the deteriorated collection of charge carriers, which is a result of poor passivation quality of the studied cell.

Lastly, EQE and (1-R) analysis of the solar cells have been performed. In Figure 4.12(b) the EQE curves and (1-R) curves of manufactured cells are illustrated. Firstly, looking at this figure a deteriorated performance of cell which was hydrogenated in nitrogen-rich gas (0.33 ratio) is visible. This cell with comparison to the other cells reached a relatively low EQE in the wavelength range of 500-1000 nm. The low EQE value is a result of poor charge carrier's collection, which is a consistent with the poor passivation quality since as it was mentioned before the passivation in nitrogen-rich films is field-effect passivation driven, which later disappears after the etching of SiN_x film. On the contrary, the EQE curves of the remaining cells are following the same trend as expected. Low EQE values are present in short and long-wavelength regions. In the long-wavelength region, the observed high optical losses can be linked to the low energy photons not being absorbed, hence they are propagating through the material without any contribution to the J_{scEQE}, On the other hand, the high optical losses in low wavelength region are a result of parasitic absorption of high energy photons and reflection losses. Finally, looking at (1-R) characteristic of manufactured cells similar trend is visible for each fabricated cell.

Post annealing effect

The final step of the fabrication process is the post-treatment of the finished solar cells. In literature are presented results which prove that a short post annealing at temperature 350 °C of the solar cells can be beneficial for electrical performances [102]. Consequently, in this set of experiments in order to cure the solar cells they were placed on a heating plate warmed up to the temperature of 350 °C for a duration of 5 minutes. The achieved results are given on Figure 4.13 and On Figure 4.13 it is proved that the curing process improves solar cell performance, as electrical measured

parameters are positively affected by the post annealing process. Similar to results presented in section 4.2, Jsc measured through EQE did not change after the curing of solar cells. Moreover, looking at Figure 4.13, it is important to note, that the lowest Voc and FF have been measured for the cell which was hydrogenated at nitrogen-rich gas. After the post treatment process, this cell achieved the worst results eventhogh they exhibit a great improvement. The biggest influence of the post-annealing is registered for Voc values (Figure 4.14(a)) of the cell which was hydrogenated in gas with a 0.33 ratio of SiH_4/NH_3. The recorded difference of Voc is 29 mV and is a 4.74 % increase with regard to the Voc measured before the curing process. Moreover, a significant increase in Voc value was also recorded for cell hydrogenated in the stoichiometric ratio of gases (1.0 ratio). For this cell the Voc measured after the curing process is 19 mV higher, which is a 2.83 % increase with regard to the previously measured values. It can be observed that, higher is the SiH_4/NH_3 ratio, lower is the improvement after the post-treatment. In fact, for the cell which was hydrogenated at 3.0 ratio of gasses we detect an almost constant Voc with only 1mV variation.

Considering other solar cell parameters visible changes are present also for FF values (Figure 4.13(b)). Similar to Voc, the highest FF variation is measured for cell hydrogenated at 0.33 ratio of gasses with a 2.07 % increase. Furthermore, the record measured FF is equal to 80.38 % and increased by 0.83 % with regard to the previous value of 79.71 %. This record parameter has been measured for cells hydrogenated at a stoichiometric ratio of gasses. Looking at Figure 4.13(c) only one series of measurements is present since as was mentioned before the curing process does not have an influence on Jsc measured through EQE. Finally, in Table 4.5 as well as in Figure 4.13(d) the changes in ηact after the curing process are present. After the post annealing process, the record efficiency was achieved for cell on which the stoichiometric SiNx layer was deposited (1.0 ratio). The record achieved efficiency is 20.06 % and increased by 0.71 % with regard to the previously measured value-before the post treatment. Furthermore, as presented in Table 4.5 a significantly high efficiency has been achieved also for a cell hydrogenated at 3.0 ratio of SiH_4/NH_3. Nonetheless, for his cells, the increase in efficiency is the smallest ($\Delta\eta$=0.05 %).

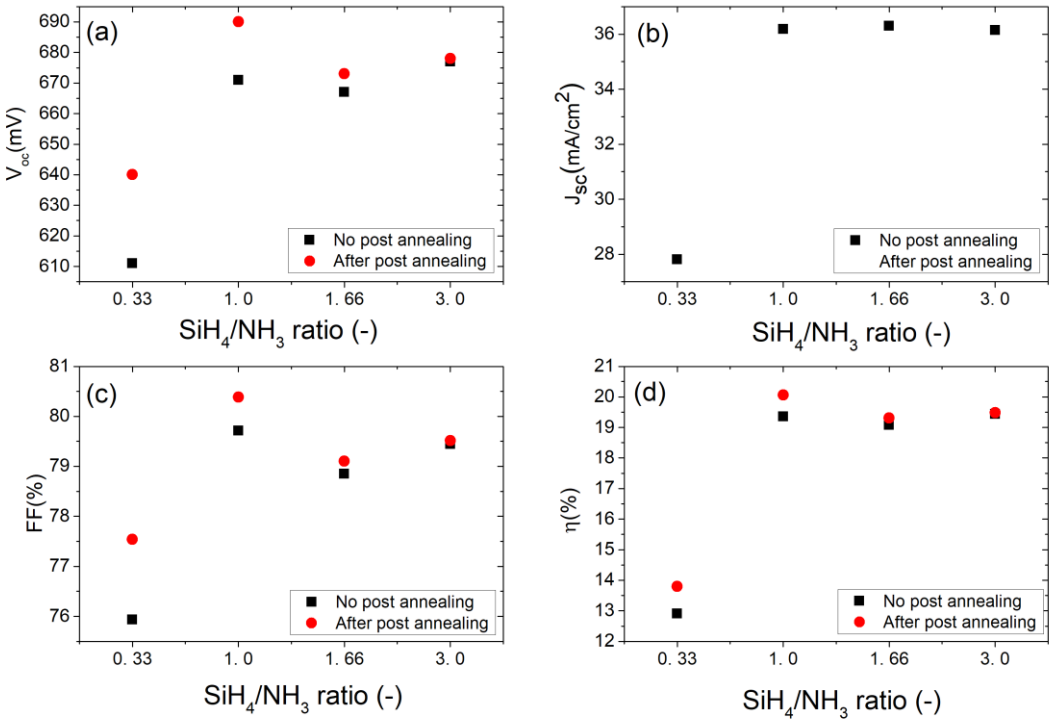


Figure 4.13 Voc of cells hydrogenated at different SiH_4/NH_3 ratio before and after post annealing treatment (a) Jsc of cells hydrogenated at different SiH_4/NH_3 ratio before and after post annealing treatment (b) FF of cells hydrogenated at different SiH_4/NH_3 ratio before and after post annealing treatment (c) Efficiency of cells with variable (i)a-Si thickness before and after post annealing treatment (d)

On Figure 4.13 it is proved that the curing process improves solar cell performance, as electrical measured parameters are positively affected by the post annealing process. Similar to results presented in section 4.2, J_{sc} measured through EQE did not change after the curing of solar cells. Moreover, looking at Figure 4.13, it is important to note, that the lowest Voc and FF have been measured for the cell which was hydrogenated at nitrogen-rich gas. After the post treatment process, this cell achieved the worst results eventhogh they exhibit a great improvement. The biggest influence of the post-annealing is registered for Voc values (Figure 4.14(a)) of the cell which was hydrogenated in gas with a 0.33 ratio of SiH_4/NH_3. The recorded difference of Voc is 29 mV and is a 4.74 % increase with regard to the Voc measured before the curing process. Moreover, a significant increase in Voc value was also recorded for cell hydrogenated in the stoichiometric ratio of gases (1.0 ratio). For this cell the Voc measured after the curing process is 19 mV higher, which is a 2.83 % increase with regard to the previously measured values. It can be observed that, higher is the SiH_4/NH_3 ratio, lower is the improvement after the post-treatment. In fact, for the cell which was hydrogenated at 3.0 ratio of gasses we detect an almost constant Voc with only 1mV variation.

Considering other solar cell parameters visible changes are present also for FF values (Figure 4.13(b)). Similar to Voc, the highest FF variation is measured for cell hydrogenated at 0.33 ratio of gasses with a 2.07 % increase. Furthermore, the record measured FF is equal to 80.38 % and increased by 0.83 % with regard to the previous value of 79.71 %. This record parameter has been measured for cells hydrogenated at a stoichiometric ratio of gasses. Looking at Figure 4.13(c) only one series of measurements is present since as was mentioned before the curing process does not have an influence on J_{sc} measured through EQE. Finally, in Table 4.5 as well as in Figure 4.13(d)

the changes in η_{act} after the curing process are present. After the post annealing process, the record efficiency was achieved for cell on which the stoichiometric SiN_x layer was deposited (1.0 ratio). The record achieved efficiency is 20.06 % and increased by 0.71 % with regard to the previously measured value-before the post treatment. Furthermore, as presented in Table 4.5 a significantly high efficiency has been achieved also for a cell hydrogenated at 3.0 ratio of SiH_4/NH_3. Nonetheless, for his cells, the increase in efficiency is the smallest ($\Delta\eta$=0.05 %).

Table 4.5 Summary of parameters of solar cells before and after post annealing step.

SiH_4/NH_3 ratio	**V_{oc} (mV)**		**FF (%)**		**J_{sEQE} (mA/cm²)**	**η_{act} (%)**	
0.33	611	640	75.93	77.54	27.81	12.90	13.80
1.0	671	690	79.71	80.38	36.18	19.35	20.06
1.66	667	673	78.85	79.10	36.29	19.08	19.31
3.0	677	678	79.44	79.51	36.14	19.43	19.48

Before post annealing	After post annealing

4.6 Conclusions

In this chapter, the poly-SiC_x passivating contact stacks optimized in chapter 3 are implemented on a device level in front-back contacted solar cells. In order to achieve the best possible FBC cell results various thicknesses of buffer layer deposited through LPCVD and PEVD has been checked, as well as, various doped layers thicknesses. Finally, solar cells with variable SiN_x capping layer are inspected in order to check if the hydrogenation gas content variation may be beneficial for the performance of the solar cell.

Firstly, annealing temperature optimization was performed on FBC cells manufactured with an interlayer deposited by LPCVD. Due to this analysis, it was found that the best annealing temperature for FBC cells with interlayer deposited through LPCVD is 875 °C. In this set of experiments also the influence of variable a-Si layer was checked. The best results have been obtained for i-a-Si thickness of 12 nm (V_{oc} of 678 mV J_{sc} of 36.47 mA/cm² FF of 77.98 % of and η_{act} of 19.28%). Subsequently, the effect of the post-annealing at 350°C for duration of 5 minutes was investigated. It was proved that the post annealing has a positive effect on solar cell performance as an increase of each of the electrical parameters except for J_{sc}. After the post-annealing, the champion cell results are: Voc of 681 mV, J_{sc} of 36.47 mA/cm², FF of 79.88 % and η_{act} of 19.83 %.

Following, cells with variable doped layers thickness and buffer layer deposited through PECVD deposition method were checked. In terms of doped layers thicknesses, it was found that the best results have been obtained for cells with (n)poly-SiC_x thickness of 10 nm and (p)poly-SiC_x thickness of 30 nm. The champion parameters of this cell are Voc of 658 mV J_{sc} of 34.36 mA/cm² FF of 76.16 % and η_{act} of 17.22 %. After the post-annealing process the parameters of this cell increased (Voc of 659 mV, Jsc of 34.36 mA/cm², FF of 77.58 % and η_{act} of 17.56 %), but still are considerably lower than results obtained from cells with buffer layer deposited by LPCVD deposition method, where the record efficiency with a doped layer thickness of 10 nm for (n)poly-SiC_x and 30 nm for (p)poly-

SiC_x is 19.83 %. This indicates that more optimization on the a-Si:H layer deposited through PECVD method should be done.

Lastly, the hydrogenation gas content influence on FBC solar cells was studied. The SiN_x layers which variable gas content (SiN_x capping layer stoichiometry variation) were deposited via PECVD and tested on cells having LPCVD buffer layer. We observe that passivation critically depends on the SiN_x stoichiometry. The worst performing was the cell in which the nitrogen-rich capping layer was deposited. As it was studied by Xiao et.al [96] the passivation mechanism in nitrogen-rich structures is field-effect passivation driven which after the etching of the hydrogenated layer disappears, leading to deteriorated performance of the cell. The results obtained on this cell before the post annealing process are: Voc of 611 mV J_{sc} of 27.81 mA/cm^2 FF of 75.93 % and η_{act} of 12.90 % and after the post annealing process: Voc of 640 mV J_{sc} of 27.81 mA/cm^2 FF of 77.54 % and η_{act} of 13.80 %. On the contrary, the best results have been obtained on FBC solar cell on which the capping layer with stoichiometric composition. The best results achieved for FBC solar cells before the post-annealing process are: Voc of 671 mV, J_{sc} of 36.18 mA/cm^2, FF of 79.71 % and η_{act} of 19.35 %). After the annealing at 350°C for a duration of 5 minutes, the cell parameters increased similarly as it was in previous experiments and the champion values are Voc of 690 mV, J_{sc} of 36.18 mA/cm^2, FF of 80.38 % and η_{act} of 20.06 % which are also the best FBC poly-SiC_x results obtained in this project so far.

5

Interdigitated back contact solar cells

This chapter focuses on the -IBC solar cell architecture. Firstly, the IBC solar cell approach is briefly introduced, as well as, advantages that it brings with comparison to FBC device architecture. Later, the photolithography process, which is crucial for IBC fabrication, is described. Afterward, two different IBC fabrication processes based on photolithography are introduced and discussed. Finally, the results of the etching tests are given.

5.1 SiO_x/poly-SiC_x passivating contacts in IBC solar cells

The optical characterization performed by members of PVMD group has proved that the optoelectronic properties of poly-SiC_x depend on the carbon content and that optical properties are not as profitable as it was expected. M. Singh et.al. [106] demonstrated that the layer featuring higher carbon content is more absorptive, especially in the short wavelength region (Figure 5.1). Consequently, in order to avoid parasitic absorption losses, it is more beneficial to apply the poly-SiC_x contacts at the rear side of the device in an IBC configuration. As it was already mentioned in section 1.6, in IBC solar cell architecture both contacts are located at the back of the device. Consequently, lower parasitic absorption and reflection losses are present at the front of the solar cell, which leads to higher values of J_{sc}. Despite the unprofitable optical properties, poly-SiC_x has other advantages that make it desirable material in semiconductor processing. By the incorporation of carbon in the silicon structure the material is more resilient to blistering which can occur due to the hydrogen effusion in the annealing process [106]. The reason for this is the fact that carbon-hydrogen bonds are more stable with comparison to the hydrogen-silicon bonds [54]. Besides, SiC materials are common for their chemical resistance in many etching solutions like BHF [45], consequently, SiC_x layer can be used as a chemically stable layer in the fabrication process which can offer great flexibility. Lastly, poly-Si has higher thermal stability than other passivating contacts like SHJ, thus poly-Si contacts offer a great adaptability of the process allowing for a different combinations of fabrication steps in broad range of temperatures.

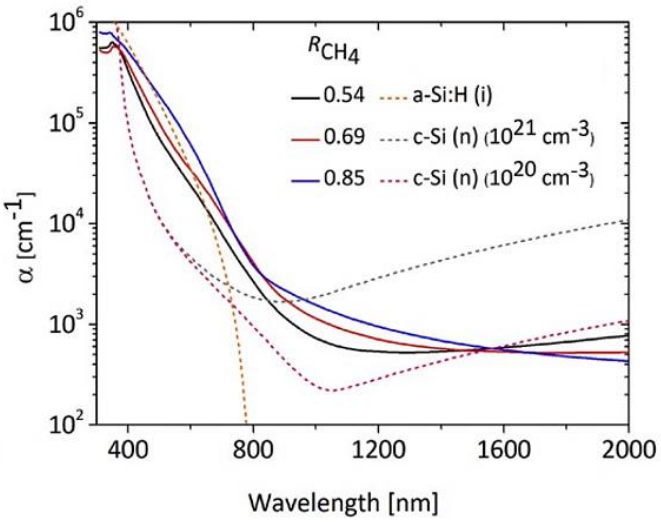


Figure 5.1 Absorption coefficients from PDS measurements of n-type doped poly-SiC_x layers with varying R_{CH4}. Intrinsic amorphous silicon and c-Si (characterized by two different doping concentrations) were used as reference[106].

Before the fabrication for IBC solar cells, which is more complex than FBC solar cell manufacturing (section 1.6), tests on FBC solar cells have been performed in order to find the best poly-SiC_x passivation contacts properties (chapter 4). After achieving promising efficiency of 20.06 % for FBC solar cells with a buffer layer deposited through LPCVD and 17.58 % for a device with a buffer layer deposited by PECVD, our focus turns to IBC solar cells.

In the following sections, the photolithography process which is essential for IBC solar cell fabrication is briefly introduced. Besides, the fabrication process of IBC solar cells and the details of the studied and fabricated concept are also presented. Moreover, results of the performed fabrication tests i.e a-SiC_x etching tests will be presented as well.

5.2 Photolithography

As it was mentioned in section 1.6, IBC solar cells require pattering of the n- and p-type contacts on the same side of the silicon wafer. The most common way of layer patterning is photolithography, nevertherless another possible method cosists in deposition of doped layers through a hard mask [107]. Consequently, the design of IBC solar cells that we discuss in this theiss involes the implementation of photolithography processes in addition to the methodology described in chapter 2.

Photolithography is a process which adopts light in order to transfer geometric shape from an optical mask to the light-sensitive chemical photoresist which is placed onto the substrate [108]. Photolithography consists of many sub-processes as depicted in Figure 5.2: wafer cleaning, photoresist application, pre-bake, light exposure, photoresist development, hard-baking and photoresist removal. Each sub-process of photolithography is briefly introduced below.

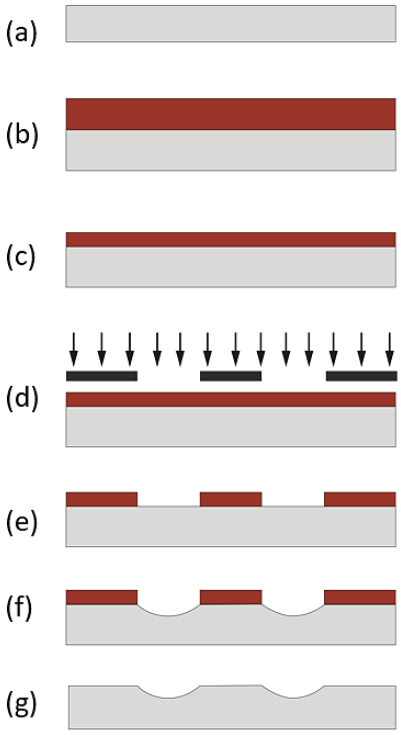


Figure 5.2 Schematic sketch of photolithography process (a) wafer cleaning, (b) photoresist application, (c) photoresist pre-bake, (d) exposure, (e) development, (f) hard bake, (g) etching).

Wafer cleaning (wafer preparation)

Photolithography processing requires substrates of an excellent clearness and quality. Accordingly, the samples must be cleaned (Figure 5.2(a)) from dust/particles which may come from atmosphere. Besides, processed samples must be free from photoresist residue which may come from previous photolithography steps and other organic and inorganic contamination. The wafer cleaning process in detail is described in section 2.1.2.

Photoresist application

The first step in the photolithography process is the photoresist layer formation (Figure 5.2(b)) which is an organic polymer layer that is sensitive to ultraviolet radiation [109]. Substrates are covered with photoresist through spin-coating: the method used to uniformly deposit a film on substrate[110]. During spin-coating, the coating material with an appropriate viscosity (photoresist) is applied to the center of the substrate. Afterward, in order to spread the photoresist, the substrate is rotated at high speed. Rotating movement lasts till the photoresist reaches the substrate edges and the rotation time is optimized to reach the desired thickness. This phase lasts from few seconds till few minutes [108]. The final thickness of the photoresist depends on the spin-rotating speed, the time of the rotation and the viscosity of the applied photoresist. The higher the rotational speed is, the thinner is the deposited film which is a direct result of centrifugal force which is acting on the fluid [108].

Photoresist pre-bake

Once the photoresist is applied uniformly onto the substrate, wafer is pre-baked (Figure 5.2(c)) in order to solidfy the layer which is sticky and still very viscous. With pre-baking, the substrate is prepared for the subsequent step in which we have to handle, transport the wafer and put it in close touch with the mask for the exposure. Besides, this step relaxes the build-in stresses that are present on the surface since the spreaded resist still may contain up to 15 % of solvent (depending on the used solvent and film thickness) [111]. Consequently, in order to remove solvents and stress, and to improve the adhesion of the photoresist layer to the wafer the photoresist is pre-baked. Standard pre-baking temperatures are usually in range of 90-100 °C. Typically pre-baking lasts 30-60 seconds and it is performed on a hotplate. During pre-baking the photoresist thickness is usually lowered by 10-25% due to the solvent release [112].

Exposure

Following the prebaking process, the photoresist is exposed to intense light (Figure 5.2(d)) through a mask with a pattern. In photolithography during the exposure step the light sources illuminate the resist coated wafers with very short wavelengths of light below 570 nm. Exposure of photoresist to light provokes a chemical change which subsequently allows the removal of the photoresist.

Development

After the exposure step, the selected resist mask is present as a latent image in the photoresist: The exposed areas vary chemically from the non-exposed one. The photoresist can be removed by dipping the wafer in a so-called developer solution. The behavior of the photoresist in contact with the developer depends on the type of used photoresist. There are two different kinds of photoresist: negative and positive (Figure 5.3).

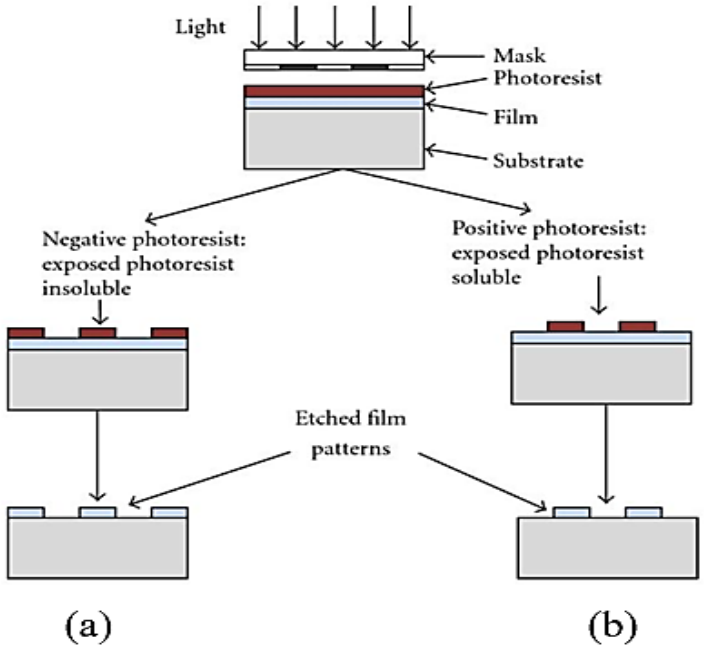


Figure 5.3 Negative photoresist after the exposure (a) and positive photoresist after the exposure (b). The figure is taken from Ref. [113].

Negative photoresist becomes insoluble after the exposure to light. Only the unexposed regions of negative photoresists are soluble in the developer (Figure 5.3(a)). On the controrary for a positive photoresist the exposed photoresist becomes soluble (Figure 5.3(b)) in the developer solution and it is therefore removed exposing the layer underneath. The develop chemistry takes place on a spinner, similar to photoresist deposition or through immersion of wafer in a bath with developer. As a developer typically are used metal-ion-free materials like tetramethylammonium hydroxide (TMAH) [82].

Hard bake

Finally, after the photoresist development, the hard bake step is applied. The hard bake stabilizes the patterned areas in order to provide the best performance during etching, as hard bake guarantees the entire removal of the solvent. The hard bake leads to a more stable patterned layer in subsequent processes like wet chemical etching, plasma etching or ion implantation.

Etching

During the etching step (Figure 5.2(f)), the layer not covered by the photoresist can be etched away. There can be distinguished two etching methods: dry and wet etching. Wet etching is the process (Figure 5.4 a)) in which etching is performed in a liquid solution. Chemicals used for the etching process are called etchants. During the wet etching, the material that should be removed is dissolved by immersing it in a chemical bath.

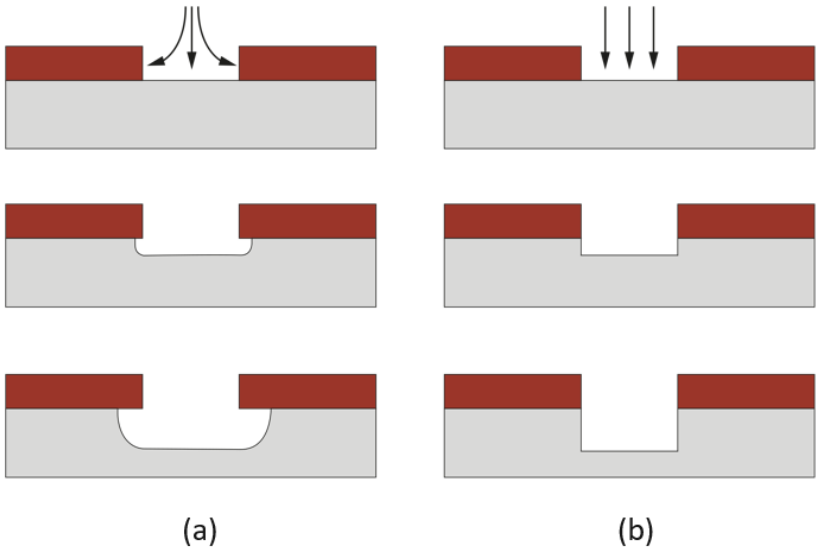


Figure 5.4 Schematic sketch of wet etching (a) and dry etching process (b).

On the contrary, the dry etching process (Figure 5.4(b)) is performed in plasma phase. Consequently, the reactions that lead to material removal take place in the gas phase. An important advantage of the dry etching process is the fact that this process is anisotropic, avoiding significant under etching of the photoresist pattern possible via wet etching [82].

Photoresist removal

Generally, photoresists are applied only as a temporary mask for patterning the layer untherneath. Consequently, the last lithography step is the removal of the resist mask (Figure 5.2(g)). The resist removal usually involves "resist stripper", which chemically modifies the resist so that it does not adhere to the surface anymore. Besides, the photoresist may be removed by acetone or a plasma containing oxygen [113].

5.3 IBC solar cells experimental details

Having introduced the experimental details of the FBC solar cell fabrication (chapter 2) and photolithography process (section 5.2), it is possible to develop the flowchart for IBC solar cell processing. In this section we use the knowledge gained in the previous chapter to propose methods for the fabrication of poly-SiC_x IBC solar cells. Two different concepts are presented here, which vary with regard to use of the deposited material i.e. the buffer layer. Details of each presented solution are discussed below.

5.3.1 IBC fabrication process introduction

In the following sections, two alternative methods of IBC solar cell fabrication which vary with regard to the deposited buffer layer will be presented. Each concept has significant advantages as

well as some drawbacks. In the first approach, the buffer layer for both contacts, emitter and BSF, is deposited through the LPCVD deposition method. This choice is based on the superior passivation quality of the contacts with buffer layer deposited through LPCVD with comparison to the one reached by PECVD (section 3.4).

Table 5.1 Summary of parameters of solar the best FBC solar cells.

Buffer layer	i-V_{oc} (mV)	V_{oc} (mV)	J_{scEQE} (mA/cm^2)	FF (%)	η (%)
LPCVD	689	690	36.18	80.38	20.06
PECVD	674	660	34.36	77.53	17.58

As presented in section 3.4, the record i-Voc obtained on a cell precursor after the hydrogenation process with a buffer layer thickness of 12 nm deposited by LPCVD is equal to 718 mV. On the contrary record i-Voc obtained on cell precursor with buffer layer deposited by PECVD is equal to 700 mV (section 4.4) .Later, it was studied in chapter 4 that the results of FBC solar cells with buffer layer deposited through LPCVD are significantly better than the results of FBC solar cells with buffer layer deposited through PECVD. Record cell results are presented in Table 5.1. The possible explanation of the deteriorated performance of FBC solar cell with buffer layer deposited by the PECVD method is the fact that (i)a-Si:H layer deposited by PECVD is of lower homogeneity with comparison to the buffer layer deposited through LPCVD (section 3.4). Consequently, on solar cells with buffer layer deposited by PECVD higher sputtering damage was recorded with comparison to solar cells with LPCVD buffer layer. Therefore, for IBC solar cells it is better to apply buffer layer deposited by LPCVD as higher quality and homogeneity of passivation contacts is guaranteed. Nonetheless, the developed fabrication method of IBC solar cell which makes use of buffer layer deposited by LPCVD has one significant disadvantage. In this method one additional photolithography step must applied during the emitter formation. The main role of the additional photolithography step is to protect the buffer layer form etching during the (p)a-SiC_x etching. Consequently, to decrease the need for photolithography processes, the second alternative IBC solar cell fabrication method is proposed.

In the second suggested fabrication method the buffer layer is deposited through PECVD and LPCVD deposition methods for p- and n-contact, respectively, in order to decrease the number of needed photolithography processes. The explanation of this is the fact that, when the buffer layer deposited by LPCVD will be used only for emitter contact then there is no need for separate protection of (i)a-Si layer and (p)a-SiC_x layers from etching (Appendix A). Consequently, it may be profitable to use for BSF surface contact the buffer layer deposited by PECVD, despite its lower homogeneity, as higher quality of the finished cell can be achieved by limiting the photolithography steps (misalignment issue and over etching issues). Besides, the second developed fabrication method leaves a window for improvement of homogeneity and quality of (i)a-Si:H layer. Moreover, it is worth to point that the buffer layer deposited by PECVD will be used for (n)poly-SiC_x contact not (p)poly-SiC_x. The reason for this choice is the fact that p-type semiconductors are very sensitive for changes of passivation quality with comparison to n-type semiconductors. The explanation of this fact is the difference in barrier tunneling heights. 4.7 eV for valence band and 3.2 eV for conduction band implying more significant barrier for electrons than holes as minority charge carriers [114]. It was also proved in results obtained before. The passivation results obtained on

double side polished (p)poly-SiC$_x$ samples (i-Voc of 707 mV) are worse than results achieved on symmetrical polished (n)poly-SiC$_x$ samples (i-Voc of 717 mV). Hence, this is also a proof that it is possible to apply buffer layer deposited by PECVD for the BSF contact but not for the emitter.

Finally, it is worth to point that the etching of the doped layers will be performed before the annealing process which results in a change of the a-Si structure into poly-Si. The reason for this is the fact that it is very difficultto etch poly-SiC$_x$ layers in standard chemical solutions.

5.3.2 Flowchart A: LPCVD buffer layer approach

Figure 5.5 shows the schematic sketch of the first flowchart developed. The thicknesses of the deposited layers presented on Figure 5.5 are not in scale in order to clearly illustrate the introduced process-draw every deposited layer. Figure 5.5 reports only the most important steps of contact formation. A detailed description of each photolithography step applied and connected with it sub-processes can be found in Appendix A.

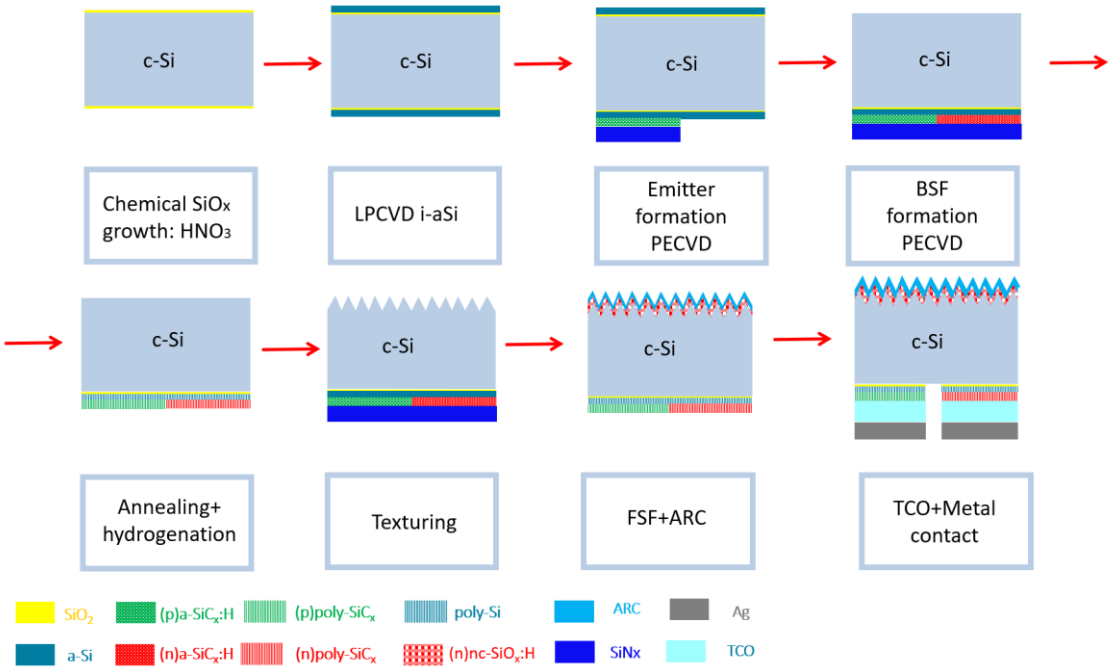


Figure 5.5 Schematic sketch of our self-aligned process for fabrication of poly-SiC$_x$ IBC solar cells.

The used substrate material is phosphorus doped float zone 4- inch shiny c-Si wafer with <100> orientation, thickness of 260≃300 µm and a resistivity of 1-5 Ω·cm. More details regarding the used substrate material can be found in section 2.1.1.

1. Firstly, the n-type substrate wafer is cleaned using the standard cleaning method described in section 2.1.2. During this step a thin SiO_2 layer is formed, which will be subsequently removed by dipping the wafer is HF solution for few minutes (Marangoni process), which is one of the sub steps of the cleaning method.

2. Tunneling oxide is formed through immersion of the wafer in HNO_3 solution (69.5 %) at room temperature for approximately 60 minutes.
3. Subsequently, the wafer is loaded into the LPCVD furnace for a-Si layer deposition.
4. Afterwards, SiN_x layer is deposited through PECVD in order to protect part of (i)a-Si from etching. Later, the first photolithography step is applied to pattern the SiN_x layer, which is followed by BHF etching in order to remove SiN_x in the openings. Afterwards, doped (p)a-SiC_x:H layer is deposited through PECVD onto the patterned SiN_x. Then again, the SiN_x layer is deposited to protect the part of (p)a-SiC_x layer from etching. Subsequently, the second photolithography step is applied to pattern the SiN_x layer, which is followed by a BHF etching and the wet-chemical etch-back step is applied to remove the (p)a-SiC_x layer.
5. Subsequently, the (n)a-SiC_x layer is deposited by PECVD method. Later, the SiN_x protective layer is deposited and the third patterning step by photolithography is applied to pattern the (n)a-SiC_x layer. Afterward, the wet-chemical etch-back step is applied to remove the (n)a-SiC_x layer and BHF etching in order to remove SiN_x which is remaining after the previous photolithography steps.
6. The whole structure is annealed at high temperature to activate and drive in the dopants for emitter and BSF as optimized in section 3.2.1.
7. Following the SiN_x layers deposited through PECVD followed by FGA are used to passivate the patterned rear wafer surface.
8. Following, the previously deposited SiN_x is used as protective layer for the texturing process. Subsequently, the wafers are immersed in the texturing solution of Alka-Tex and Tetramethylammonium Hydroxide (TMAH). Afterward, wafers are again immersed in BHF solution for approximately 30 minutes until the SiN_x protective layer will be completely etched.
9. Afterwards, the front side is completed with a FSF stack deposited via PECVD. It consists of a thin (i)a-Si:H as passivation and a (n)-doped silicon film of (n)nc-SiO_x:H. More details of layer stacks can be found in Ref. [115].
10. Subsequently the ARC coating is deposited on the front of the wafer. Afterwards, the fourth patterning step by photolithography is used to pattern the back side of the wafer and prepare the structure for the pattering of deposited TCO. Finally, after the TCO deposition the fifth pattering step by photolithography is applied and IBC cell is finished creating interdigitated patterned fingers on the rear side.

5.3.3 Flowchart B: LPCVD and PECVD buffer layer approach

The objective of this section is the presentation of the second fabrication method for poly-SiC_x IBC solar cells. In this approach, the buffer layer is deposited through different methods (PECVD and LPCVD), consequently, the material properties are also different. In particular, for the emitter the buffer layer is deposited through the LPCVD deposition method (section 5.3.1). On the contrary, for BSF the interlayer is deposited through the PECVD deposition method. Figure 5.6 depicts the most important steps of the fabrication process. The detailed method is presented in Appendix B, where each fabrication step has been clearly described.

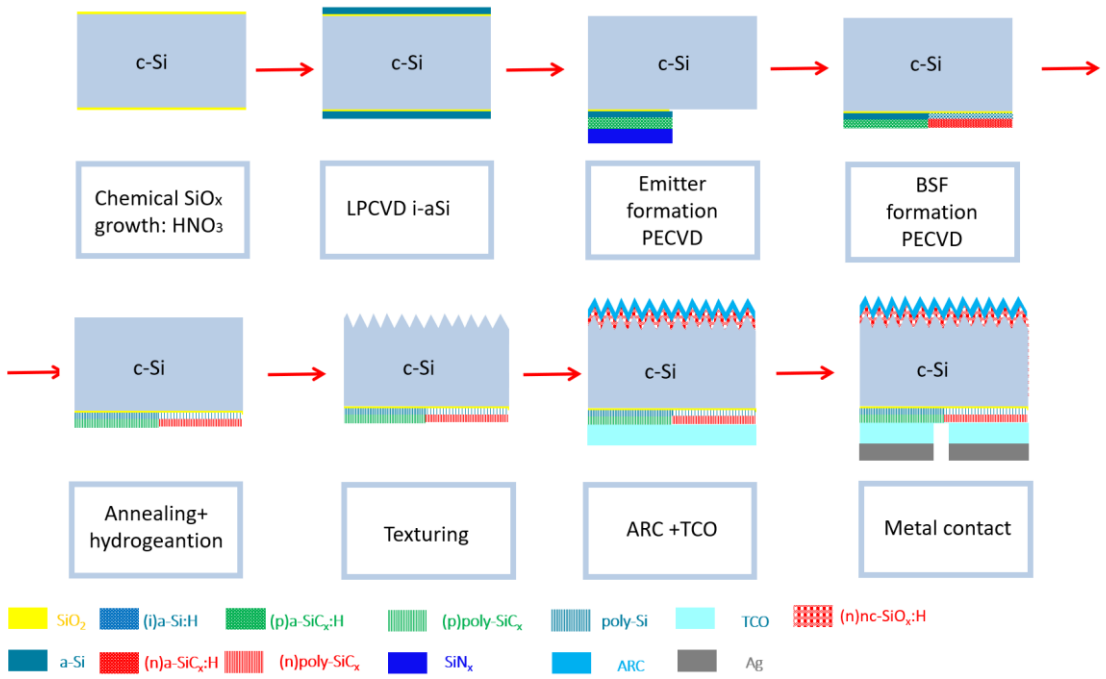


Figure 5.6 Schematic sketch of proposed self-aligned process for fabrication of poly-SiC_x IBC solar cells.

The used substrate material is phosphorus doped float zone 4- inch shiny etched c-Si wafer with <100> orientation, thickness of 260≃300 µm and a resistivity of 1-5 Ω·cm. More details regarding the used substrate material can be found in section 2.1.1.

1. In the first step, the c-Si substrate wafer is cleaned using the standard cleaning method described in section 2.1.2. During this step the thin surface is oxidizing and SiO_2 is formed. The grown SiO_2 will be later removed during the Marangoni process, which is one of the sub-steps of the cleaning method (section 2.1.2).
2. Tunneling oxide is formed through immersion of the wafer in (69.5 %) solution of HNO_3 at room temperature for approximately 60 minutes.
3. Later, the (i)a-Si buffer layer is deposited through LPCVD. Subsequently, (p)a-SiC_x is deposited through PECVD deposition method. Following the SiN_x is deposited to protect (p)a-SiC_x and (i)a-Si from etching. Afterward, the first photolithography step is applied which will allow the wet-chemical etch-back of SiN_x and the wet-chemical etch back of excess of (p)a-SiC_x:H and (i)a-Si.
4. In next step, firstly the SiO_2 is formed through the wet chemical method. Later the (i)a-Si:H and (n)a-SiC_x:H are deposited through the PECVD deposition method. After, again SiN_x protective layer is deposited through PECVD. Subsequently, the second photolithography step is applied to remove the excess of (n)a-SiC_x:H and (i)a-Si:H layer. Later BHF etching is performed in order to remove SiN_x which is remaining after previous photolithography steps.
5. The whole structure is annealed at high temperature to activate and drive in the dopants for emitter and BSF as optimized in section 3.2.1.
6. Following the SiN_x layers deposited through PECVD followed by FGA are used to passivate the patterned rear wafer surface.
7. Following, the previously deposited SiN_x is used as protective layer for the texturing process. Subsequently, the wafers are immersed in the texturing solution of Alka-Tex and Tetramethylammonium Hydroxide (TMAH). Afterward, wafers are again immersed in BHF

solution for approximately 30 minutes until the SiN_x protective layer will be completely etched.

8. Afterwards, the front side is completed with an FSF stack deposited via PECVD. It consists of a thin (i)a-Si:H as passivation and a (n)-doped silicon film of (n)nc-SiO_x:H [115].
9. Subsequently the ARC coating is deposited on the front of the wafer. Afterwards the patterning step by photolithography is used to pattern the back side of the wafer and prepare the structure for the pattering of deposited TCO. Finally, after the TCO deposition the fourth pattering step by photolithography is applied and IBC cell is finished creating interdigitated patterned fingers on the rear side.

5.4 Etching optimization of the contact stacks

As it was already described in section 5.2 one of the photolithography steps is the etching process. In experimental details of the flowcharts developed for the fabrication of IBC solar cells many etching steps are present. Every etching step performed in the studied project is a wet etching method (Figure 5.4(a)). Some of the wet etching steps do not need the additional etching tests, for example the SiN_x can be easily etched in BHF solution and the etching will stop at the Si surface [116]. Furthermore, SiN_x removal is a standard procedure performed many times during the fabrication of FBC solar cells (chapter 4). On the other hand, considering other layers like doped silicon carbide layers like (p)a-SiC_x, (n)a-SiC_x or (i)a-Si, etching tests must be performed to avoid a too deep etching into the c-Si (see Flowchart B). Since these layers cannot be etched in commonly used etching solutions like BHF or HF a special solution must be prepared.

Careful optimization of etching of the (n)a-SiC_x, (p)a-SiC_x and (i)a-Si layers is very important for the passivation quality and the performance of the manufactured IBC solar cell. Too long wet etching-isotropic etching of the layers can lead to the over-etching of the material and consequently poor adhesion of photoresist to the protected layer (Figure 5.4(a)). Consequently, different etching tests were performed in order to determine the etching rate of the studied materials in the pol-Si etch solution. The chemicals which were used for the preparation of studied etching solution are listed in Table 5.2.

Table 5.2 Chemicals and volumes used for the preparation of poly-Si etch solution with three concentrations.

Solution	**HF 40 % (ml)**	**HNO_3 69.5 % (ml)**	**H_2O (ml)**
A (initial)	15	525	210
B	7.5	263	420
C	7.5	263	210

The etching rate of poly-Si material in the solution A at room temperature is 0.35 µm/minute. This is the etching rate measured by the staff of EKL laboratory. Nonetheless, due to the fact that the layers for which the etching tests will be performed contain carbon (n)a-SiC_x and (p)a-SiC_x or are amorphous silicon layers ((i)a-Si) different etching rate is expected. The thickness of each studied layer was measured before and after the etching process. The thickness was established through angle-dependent spectral ellipsometry (SE). All the silicon-based layers were modeled using the Tauc-Lorentz dispersion model.

Intrinsic layer etching tests

The first etching tests have been performed on the intrinsic layer deposited through LPCVD. The initial layer thickness is 15 nm deposited on a polished wafer. Figure 5.7(a) depicts the results of the performed etching tests on this layer. Three different etching times have been tested (5, 10, and 15 s) for three different chemical solutions. As it can be seen in Figure 5.6(a), the longer is the etching time, the thinner is the obtained layer for the three solutions tested. The fastest etching of the material occurred using solution A, which means that this solution is aggressive with regard to the (i)a-Si layer. The obtained etching rate of (i)a-Si in solution A is equal to 40 nm/minute, and its slower with comparison to results obtained by members of EKL laboratory. In order to avoid over etching (Figure 5.4(a)), less aggressive solutions are tested. The second checked solution is solution B for which etching rate is equal to 16 nm/minute. Later one more solution has been checked, solution C with the etching rate of 24 nm/minute. The summary of all calculated etching rates is presented in Table 5.3. Analyzing the etching tests results, the best would be to select the solution C, since the etching process occurs slower and can be better controlled. Consequently, in order to etch 12 nm of buffer layer using solution B, the etching time should be limited to 30 seconds to guarantee no over-etching. The nominal thickness is 12 nm, as this buffer layer thickness gave the best result in the passivation tests (section 3.3.1) hence this is the best choice for IBC solar cell as well.

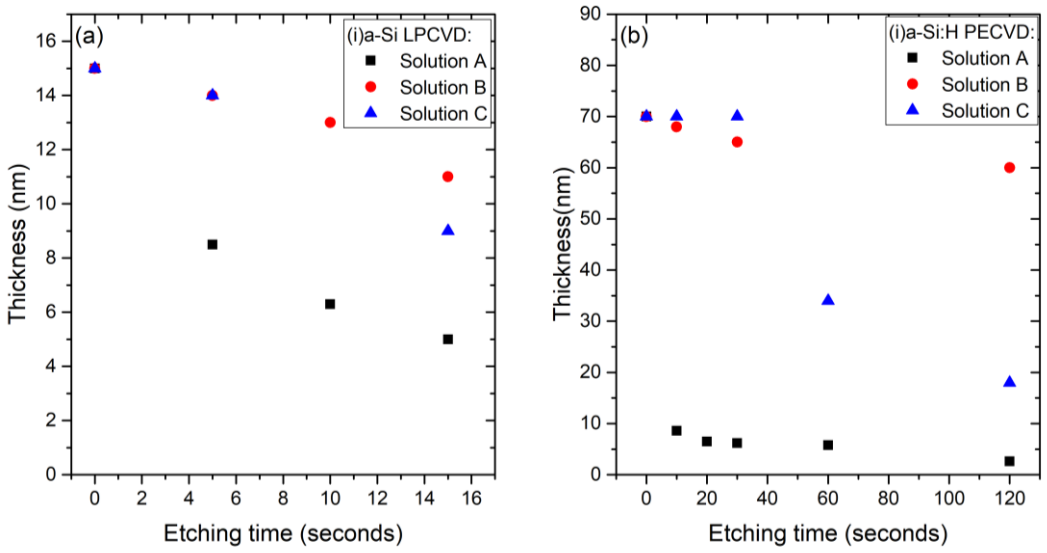


Figure 5.7 Etching tests performed on (i)a-Si layer deposited through LPCVD (a) and on (i)a-Si:H layer deposited through PECVD (b).

As is presented in section 5.3, (i)a-Si:H buffer layer will be used for (n)a-SiC_x-BSF contact (Appendix B). This i-layer is deposited through PECVD tool. The film which is studied during the etching tests is (i)a-Si:H layer with an initial thickness of 70 nm. Considering the fact that the deposited layer is thicker than the film deposited through the LPCVD tool, longer etching times have been applied. Figure 5.7(b) presents the etching tests for different duration of times. As it can be seen in Figure 5.7(b), (i)a-Si:H layer is etched faster with comparison to (i)layer which is coming to form LPCVD (Figure 5.7(a)). Focusing on the solution A, it can be agreed that the analyzed mixture of chemicals

is too aggressive with regard to (i)a-Si:H layer since it can be seen that after the etching time of 5 seconds the majority of the material was etched away and for longer times the etching process was almost saturated. The obtained etching rate during the first 10 seconds of the process is equal to 360 nm/minute (Solution A). The possible reason for this can be the fact that the buffer layer deposited through PECVD has lower homogeneity and is also more porous and H rich than the buffer layer deposited via LPCVD (section 3.4). Consequently, it is possible that if the wafer would be kept in the etching solution too long (even a few seconds) the isotropic etching could have a detrimental effect on formed contacts. Therefore, again the best choice would be to select less aggressive solution B or C. Looking at etching curves it is visible that material is etched the slowest in solution B (etching rate equal to 2.5 nm/minute). On the contrary etching in the solution C is also aggressive with regard to (i)a-Si:H layer. The etching rate of (i)a-Si:H layer in solution C is equal to 26 nm/minute. Hence, the selection of solution B would be the best choice, as it would guarantee no over-etching of the c-Si material. In order to etch away 10 nm of (i)a-Si:H layer, the applied etching time should be 60 seconds. This process duration will guarantee that no over etching will occur [114] and consequently the adhesion of the protective layer (photoresist and SiN_x) will be not disturbed.

Table 5.3 Etching rates of solutions used for etching of buffer layer deposited by LPCVD and PECVD.

	Etching rate (nm/minute)	
Solution	**(i)a-Si LPCVD**	**(i)a-Si:H PECVD**
A (base)	40	360
B	16	2.5
C	24	26

Doped layers etching tests

According to the flow charts presented in section 5.3, not only the intrinsic silicon buffer layers have to be etched but (n)a-SiC_x and (p)a-SiC_x:H layers as well. The studied films are deposited through PECVD deposition method. Figure 5.8 depicts the etching tests results on (n)a-SiC_x and (p)a-SiC_x:H layers with the initial thickness of 125 nm and 70 nm, respectively. Comparing Figure 5.8(a) and Figure 5.8(b) it can be seen that (n)a-SiC_x:H is etched faster in the used solutions than the (p)a-SiC_x:H layer. As presented in Figure 5.8(a), in solution A the change in thickness is not significant during the first 20 seconds of etching with only 3 nm of material etched away. Nonetheless, after 60 seconds of etching a significant drop in the material thickness was measured. After 60 seconds, 44 nm of the material was etched. After the duration of 120 seconds, only 37 nm of the material remained, which gave the etching rate 44 nm/minute. The etching rate of (p)a-SiC_x:H layer in solution A is equal to 42 nm/minute. On the contrary, looking at the results obtained after etching in solution B, it can be seen that this solution is not a good choice, as after 120 seconds of the process only 4 nm of the layer was etched away which proves that the (p)a-SiC_x:H layer is highly resistive against this solution, as the etching rate is equal to 2 nm/minute respectively. The detailed values of etching rates are presented in Table 5.4.

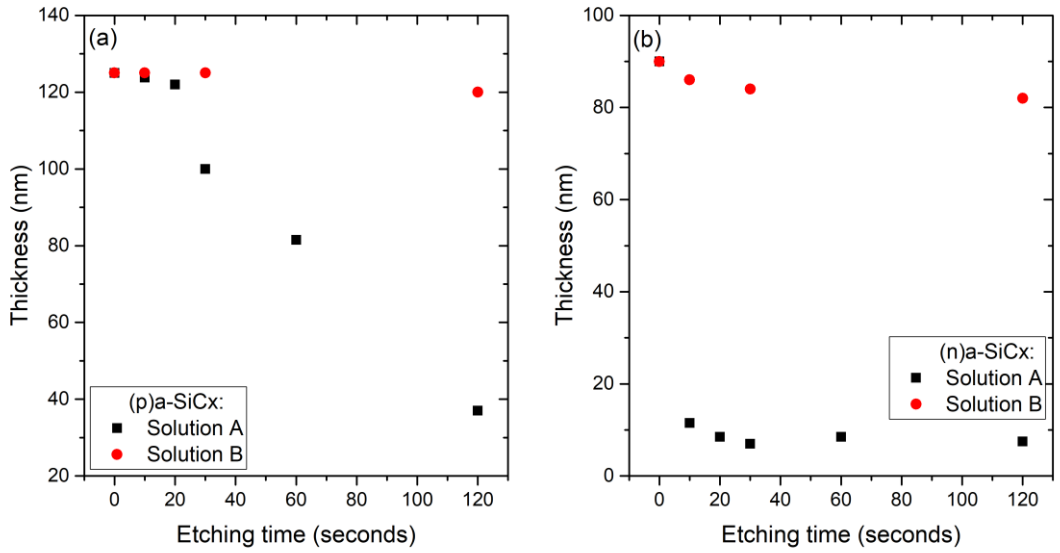


Figure 5.8 Etching tests performed on (p)a-SiC_x layer deposited through PECVD (a) and on (n)a-SiC_x layer deposited through PECVD (b).

As it was mentioned earlier, (n)a-SiC_x:H layer is etched faster than (p)a-SiC_x:H. Looking at Figure 5.8(b) it can be seen that in the first 10 seconds of etching performed in solution A 80 nm of material has been removed. This means that the prepared solution is very aggressive with regard to the (n)a-SiC_x:H material-etching rate 48nm/minute. On the contrary, thickness measured after etching in solution B did not vary significantly what again proves that this film is also resistive with regard to the prepared solution (etching rate 4 nm/minute).

Table 5.4 Etching rates of solutions used for etching of (p)a-SiC_x:H and (n)a-SiC_x:H layers.

	Etching rate (nm/minute)	
Solution	**(p)a-SiC_x**	**(n)a-SiC_x**
A (base)	42	48
B	2	4

Stack of layers

Finally, the last etching tests have been performed on stack of deposited layers. The analyzed structures are presented in Figure 5.9. Three different combinations of layers are presented. Combination (a) correlates with deposited films which will have to etched during the BSF formation in the flowchart B (section 5.3.3). Other combinations of layers (b) and (c) were checked in terms of future development of IBC solar cells fabrication within PVMD group with buffer layer deposited for both contacts via PECVD will be intensively studied.

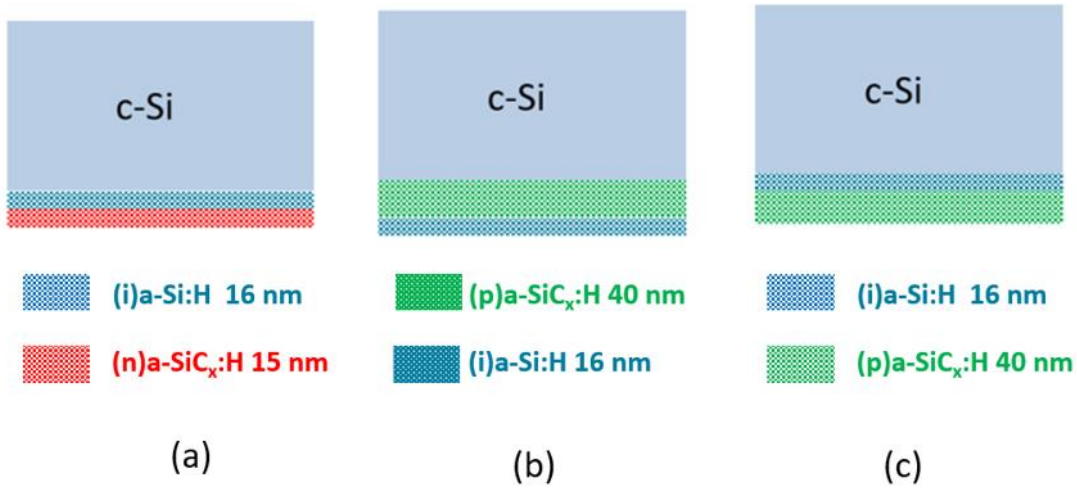


Figure 5.9 Three different configurations of layer stacks with buffer layer deposited through PECVD on which the etching tests have been performed.

Figure 5.10 depicts the results of the etching tests performed on different stacks of deposited layers with thicknesses compatible with solar cell application. Firstly, it is important to point that each test has been performed with the use of solution C listed in Table 5.2. Secondly, it is important to note that during the applied etching times only the outer layer was etched away. As it is presented in Figure 5.10(a),(b),(c), none of the inner layer thickness has changed. This means that none of the inner layers have been etched during the process. Focusing on Figure 5.10(a) it is visible that after the etching time of 120 seconds only 3 nm of (i) layer remained. Nonetheless, this measured value can be also a result of measurement fitting to the Tauc-Lorentz model.

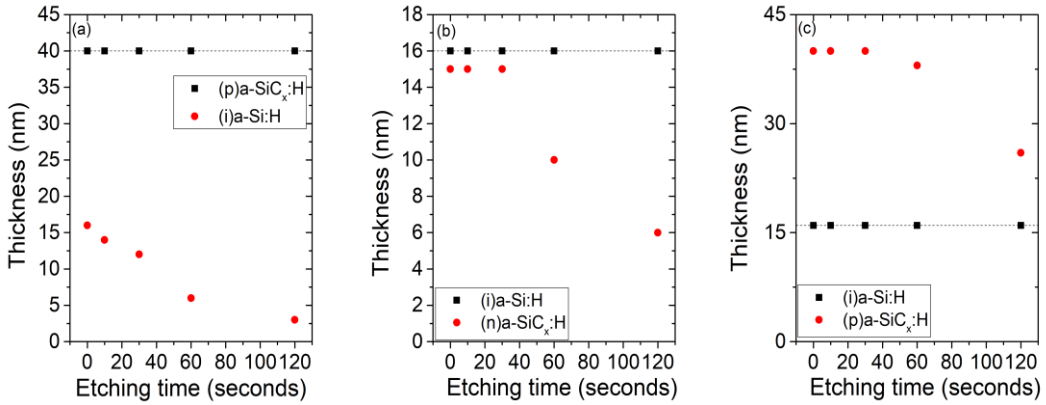


Figure 5.10 Etching results performed on (p)/(i) stack (a) (i)/n stack (b) and (i)/(p) stack (c).

Secondly looking at Figure 5.10(b) representative of a layer stack used for BSF field formation, it is visible that even after 120 seconds of etching 6 nm of (n)a-SiC_x layer still remains. Consequently, more aggressive solution should be used for etching of these layers or longer etching times should be tested, as it is crucial to etch away completely (n)a-SiC_x and a-Si:H layer.

Finally, looking at Figure 5.10(c),it is visible that only the outer layer has been etched. The thickness of (p)a-SiC_x layer changes in a range of 40-26 nm. Again (p)a-SiC_x layer is the one which is the most stable in the poly-Si etching solution. Consequently, in order to etch away this stack longer etching tests should be performed or more aggressive solution should be used, nevertheless,

here we have to be careful with the etching time as the etching process may not stop on the interface and will probably etch (i)a-Si:H layer underneath.

5.5 Conclusions

In this chapter, the process to fabricate IBC solar cells was briefly summarized. Later it was explained why it is advantageous to apply poly-SiC_x passivation contacts in IBC solar cells despite its unprofitable optical properties. Following the photolithography process was introduced which is crucial for the successful fabrication of IBC solar cells. Afterward, two flowcharts for IBC solar cell fabrication were presented, and finally, the results of the performed etching tests have been discussed.

Focusing on the developed fabrication methods of IBC solar cells, two alternative flowcharts have been introduced. In the first approach, the buffer layer is deposited through LPCVD for both contacts, while in the second concept the buffer layer is deposited through PECVD and LPCVD. Each flowchart has significant advantages as well as drawbacks. Considering the first introduced method with a buffer layer deposited by LPCVD, it is expected to achieve higher passivation quality and consequently higher i-Voc similarly as it was shown in chapter 4 for FBC solar cells. Nonetheless, this concept requires five photolithographic steps. In particular, during the emitter formation, two photolithography steps have to be applied one in order to protect LPCVD (i)a-Si layer from etching and the second one in order to protect (p)a-SiC_x layer from etching. On the contrary in the second proposed flowchart, there is no need to apply the additional photolithography step during the emitter formation, as it is not needed to protect (i)a-Si layer from etching. The reason for this is the fact that for BSF will be applied (i)a-Si:H layer deposited by PECVD and buffer layer deposited by LPCVD will be applied only for emitter. Nevertheless, this concept has also one drawback. The (i)a-Si:H buffer layer deposited by PECVD is of lower quality and homogeneity, consequently leading to lower passivation quality and lower i-Voc values.

Lastly, the influence of the wet etching process has been investigated. Firstly, the tests have been performed with the use of the solution-A which consist of 210 ml of H_20, 525 ml of HNO_3 (69.5 %) and 15 ml of HF (40%). This mixture of chemicals was too aggressive regarding the buffer layers; for (i)a-Si the etching rate is 40 nm/minute, for (i)a-Si:H the etching rate is 360 nm/minute and for (n)a-SiC_x:H layer (etching rate 48 nm/minute). Consequently, the quantity of acids was reduced by 50 % and the amount of water was doubled, and with the use of this solution-B, etching tests have been performed. On the contrary, solution B was not strong enough to etch (p)a-SiC_x layer (etching rate 2 nm/minute) and (n)a-SiC_x layer (etching rate 4 nm/minute). Therefore, a third solution has been developed in which the amount of chemicals used was reduced by half with regard to the base solution and the quantity of water remained the same. The etching tests performed with this solution gave the best results (i)a-Si etching rate of 24 nm/minute and (i)a-Si:H etching rate of 26 nm/minute. In order to successfully etch 16 nm of deposited (i)a-Si:H layer at least 36 seconds of etching in solution C should be performed. Finally, the tests on the stack of the layers have been performed with the solution C, as it is not as aggressive as a base mixture and a smaller chance of the overcutting issue may occur. Unfortunately, the etching attempts were not successful and only the outer layer have been etched. In the presented stack of the layers none of the inner layer was etched away which means that too short etching times have been applied.

6

Conclusions and Outlook

The objective of this master thesis work is the optimization of the poly-SiC_x passivating contacts in order to successfully fabricate FBC and IBC solar cells. Many sets of experiments have been carried out fabricating various sample structures. The main conclusions of the performed work are summarized in this chapter. Finally, in this chapter are given also the recommendations for further improvement of studied topic.

6.1 Conclusions

In the first set of experiments the annealing temperature optimization was performed on samples manufactured with an interlayer deposited by LPCVD and PECVD. Due to these tests, it was found that the optimized annealing temperature for cell precursors with interlayer deposited through LPCVD is 875 °C/ 5 min, while for contact stacks entirely deposited by PECVD the best annealing temperature is 850 °C/5 min. Furthermore, for cell precursors with (i)a-Si:H deposited by PECVD most favorable annealing conditions changed after the hydrogenation process. The best annealing temperature for these samples (cell precoursor) in hydrogenated state is 800 °C/5 min.The change in the annealing temperature for samples with buffer layer deposited by PECVD indicates that LPCVD material is more stable against temperature than PECVD.

Subsequently, the optimum interlayer thickness for samples with an intrinsic buffer layer deposited through LPCVD and PECVD was found. The best (i)a-Si thickness for the LPCVD process is 12 nm. Nevertheless, it is important to note that this thickness is measured with regard to the flat surface not textured. The best passivation results obtained on cell precursor with 12 nm buffer layer thickness (n)poly-SiC_x thickness of 10 nm and (p)poly-SiC_x thcnkess of 30 nm are i-Voc of 713 mV, τ_{eff} of 2.14 ms and J_o of 9.5 fA/cm^2. The optimization process of buffer layer deposited through PECVD brings more challenges. Firstly, in order to optimizate the PECVD (i)a-Si layer we tested different deposition temperatures and pressures aming in minimizing the hydrogen content incorporated within the layer. The best results are achieved for the highest deposition pressure of 1.2 mbar. Following, for this pressure, various interlayer thicknesses were tested. It is important to point that the PECVD deposition method has the advantage of de-coupling the film thickness on both sides of the wafer, polished and textured. Hence, we have identified the best interlayer thickness values for each wafer side. For (n)poly-SiC_x samples deposited on double side textured surfaces, the best intrinsic layer thickness is found to be 15 nm and exhibits the remaining results i-Voc of 718 mV τ_{eff} of 2.4 ms and J_o of 7.8 fA/cm^2. On the contrary, the best optimized buffer thickness for polished (p)poly-SiC_x symmetrical samples is found to be 10 nm. The best passivation results on symmetrical (p)poly-SiC_x samples for this thickness are i-Voc of 681 mV, τ_{eff} of 1.15 ms and J_o of 31.3 fA/cm^2.

Following, we have focused on the optimization of the thickness of the doped layers. It was found that the best i-Voc results are achieved for a cell precursor with 30-nm thick (p)poly-SiC_x and 10-nm thick (n)poly-SiC_x layer. The best results for these parameters with the (i)a-Si:H layer deposited according to the previous optimization for the PECVD deposition process are i-Voc 698 mV τ_{eff} of 1.31 ms and J_o of 29.3 fA/cm^2 and are obtained on cell precursor structure.

Later, in order to further improve the passivation quality, the influence of the hydrogenation process was studied. Four different gas compositions for the SiN_x capping layer were investigated. The best results have been achieved for the stoichiometric SiN_x film. As a result, the parameters of the champion (n)poly-SiC_x symmetrical sample on polished wafer are i-Voc of 728 mV, τ_{eff} of 4.2ms, and J_o of 4.7 fA/cm^2.

In the following part of this master thesis, the poly-SiC_x passivating contacts optimized in chapter 3 were implemented at solar cell level in front back contacted configuration. Firstly, the annealing temperature optimization have been done on FBC cells manufactured with a (i)a-Si buffer layer deposited by LPCVD. Thanks to this optimization, the best annealing temperature for FBC cells with buffer deposited through LPCVD is 875 °C/5 min. In this set of tests also the effect of various (i)a-Si layer was checked. The best results have been obtained for buffer thickness of 12 nm (V_{oc} of 678 mV J_{sc} of 36.47 mA/cm^2 FF of 77.98 % of and η_{act} of 19.28%). Later, the effect of the post-annealing at 350°C for duration of 5 minutes was investigated. It was demonstrated and proved that the post annealing has a positive effect on solar cell performance as an improvement of electrical parameters while J_{sc} stays constant. After the post annealing, the champion cell results are: Voc of 681 mV J_{sc} of 36.47 mA/cm^2 FF of 79.88 % and η_{act} of 19.83 %.

Following, cells with variable doped layer thicknesses and buffer layer deposited through PECVD deposition method were checked. In terms of doped layer thicknesses, it was proved that again the best results have been obtained for cells with (n)poly-SiC_x thickness of 10 nm and (p)poly-SiC_x thickness of 30 nm, the same which were giving the best results during the passivation quality optimization. The parameters of this champion cell are Voc of 658 mV J_{sc} of 34.36 mA/cm^2 FF of 76.16 % and η_{act} of 17.22 %. After the post-annealing process the parameters of this cell increased (Voc of 659 mV, J_{sc} of 34.36 mA/cm^2, FF of 77.58 % and η_{act} of 17.56 %), although still are considerably worse than results obtained from cells with buffer layer deposited by LPCVD deposition method, where the record efficiency with a doped layer thickness of 10 nm for (n)poly-SiC_x and 30 nm for (p)poly-SiC_x is 19.83 %. This means that more optimization on the a-Si:H layer deposited through PECVD method should be done.

Lastly, the influence of the stochiometry of SiN_x deposited caspping layer on FBC solar cells with LPCVD buffer layer was studied. The worst performing was the cell where nitrogen-rich capping layer was deposited. The results obtained on this cell before the post annealing process are: Voc of 611 mV J_{sc} of 27.81 mA/cm^2 FF of 75.93 % and η_{act} of 12.90 % and after the post annealing process: Voc of 640 mV J_{sc} of 27.81 mA/cm2 FF of 77.54 % and η_{act} of 13.80 %. On the other hand, the best results have been obtained on FBC solar cell on which the capping layer with stoichiometric SiN_x was deposited. The best results achieved for FBC solar cells before the post-annealing process are: Voc of 671 mV, J_{sc} of 36.18 mA/cm^2, FF of 79.71 % and η_{act} of 19.35 %). After the annealing at 350°C for a duration of 5 minutes, the cell parameters increased similarly as it was previously observed and the champion values are Voc of 690 mV, J_{sc} of 36.18 mA/cm^2, FF of 80.38 % and η_{act} of 20.06 % which are also the best FBC poly-SiC_x results achieved in this project so far.

Finally, in the last part we have focused on the IBC solar cell concept. Turning our attention into the development of fabrication methods of IBC solar cells two different concepts have been introduced. First of them focuses on a buffer layer deposited through LPCVD in the second concept the layer was deposited through PECVD and LPCVD. Each concept has significant pros as well as cons. Focusing on the first proporsed flowchart with an interlayer deposited by LPCVD, it is expected to achieve better passivation quality and therefore higher i-Voc similarly as it was obtained in chapter 4 for FBC solar cells. Nonetheless, this concept has one significant drawback. During the emitter formation, two photolithography steps have to be applied one in order to protect (i)a-Si layer from etching and the second one in order to protect (p)a-SiC_x layer from etching.

On the contrary in the second proposed fabrication process, there is no need to apply the additional photolithography step during the emitter formation, as it is not needed to protect (i)a-Si layer from etching. The explanation of this is the fact that for BSF we chose to apply a (i)a-Si:H buffer layer deposited by PECVD that give decent passivation results in combination with (n)polySiC_x films. Nonetheless, this concept has also a one drawback. The (i)a-Si:H buffer layer deposited by PECVD is of lower quality and homogeneity, consequently leading to lower passivation quality and lower i-Voc values.

6.2 Outlook

The progress that has been done in this master thesis project still leaves the room for further improvements. The research activity on poly-SiC_x contact layers can lead to higher efficiency FBC and IBC solar cells. Possible solutions for further enhancement of the parameters of the cells with poly-SiC_x passivating contacts are briefly discussed in this section.

To further improvement of PECVD (i)a-Si:H layer

In this master thesis it was proved that the hydrogen content of the (i)a-Si:H layers deposited by PECVD has a significant influence on the passivation quality. In this project, hydrogen content was limited by the increase of deposition pressure (section 3.2.2). Nonetheless, there are also other methods that can limit the amount of hydrogen incorporated in the amorphous structure.

Osborne et al. [117] in their research have proved that the use of PECVD with a triode electrode configuration consisting in a wire mesh placed between the cathode and anode can lead to the deposition of high quality Si films with lower hydrogen content incorporated in the (i)a-Si:H layer. In their research, they have performed a set of experiments in which the substrate was grounded to the mesh bias scanned over a range of -150 V till +50 V. Thanks to these tests they have proved that within this voltage range the hydrogen content is changing rapidly and reaches a minimum of 8 %. Consequently, this idea could be proposed within further research among the members of the PVMD group, as this solution allows a limitation of hydrogen content incorporated in the structure through the change of bias applied to the mesh during the deposition.

Another alternative solution of controlling the hydrogen content of the (i)a-Si:H films deposited by PECVD at fixed temperatures without changing other properties of the film can be to change the gas mixture. For example S.Mashima et al. [118] use helium as carrier gas. This research group has proved that Si films deposited through helium dilution show low hydrogen content without

deterioration of the photoelectric properties. They have demonstrated that hydrogen content decreases as the flow rate of helium increases. This solution could be applied in the tests performed within PVMD group since it would be needed only to connect helium to the used PECVD tool (section 2.1.4).

Finally, the other option of the deposition of the (i)a-Si:H film with low hydrogen content would be reactive sputtering of the a-Si:H, as this method has one significant advantage. The hydrogen content can be inherently controlled through the hydrogen partial pressure in the discharge leaving other deposition parameters as substrate temperature fixed. This idea was demonstrated by Pinarbasi et al. [119].

To improve the J_{sc}

In order to improve the J_{sc} it is crucial to successfully fabricate the IBC solar cells, as it is commonly known that the J_{sc} of the IBC solar cells is significantly higher than J_{sc} of FBC solar cells. This is the direct result of decreased shadow losses which are a consequence of placement of the front electrode on the back of the device. Consequently, in order to further improve the J_{sc} within PVMD group more work should be done in the field of IBC solar cell fabrication. The starting point has been already performed in this master thesis work and two flow charts have been developed. Therefore, the next step is to fabricate the first IBC solar cells according to the proposed fabrication methods. Further room for improvement has been left in terms of photolithography step. It may be very profitable to design a new mask for patterning the emitter, BSF and TCO.

To simplify the fabrication process

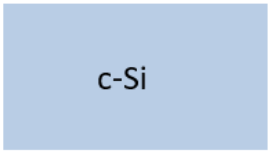
In this thesis, it was presented that the buffer layer deposited through PECVD was significantly improved with comparison to the results with were obtained in the past in our laboratories. Our attention took the possibility of deposition of the buffer layer through PECVD since it may make the whole process easier. Considering industrial processes, it is more economically viable to limit the number of used tools. PECVD method allows the deposition of interlayer and dopants in the same tool without the need for integration of new equipment what as a result makes the industrial process cheaper and more efficient. Consequently, as it was presented in the previous section more work must be done in order to optimize be the quality of (i)a-Si:H layer deposited through PECVD.

Appendix A

Detailed flow chart for fabrication of IBC solar cell with (i)a-Si buffer layer form LPCVD.

1. Interdigitated emitter formation

Standard cleaning



Equipment:

Cleaning bench - HNO_3 99% Si (RT) and HNO_3 69.5% Si (110 °C)

Before the cleaning, check if heating of HNO_3 69.5% is on.

Cleaning 10 minutes in fuming nitric acid (99%) at ambient temperature.

Use wet bench "HNO_3 (99%)" and the carrier with the white dot.

Rinsing in the DI water with the standard program.

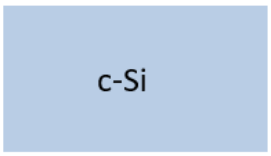
Cleaning 10 minutes in concentrated nitric acid (69.5%) at 110 °C.

Use wet bench “HNO3 (69.5%)” and the carrier with the white dot.

Rinsing in the DI water with the standard program.

Drying Use the Spin Rinse Dryer (SRD) with the standard program, and the carrier with a red dot.

Marangoni



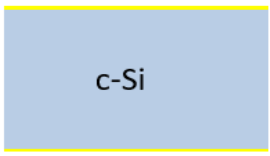
Equipment:

Cleaning bench
Dip the wafer for ~5 minutes in HF until hydrophobic

Dip the wafer for 4 minutes in DI Water

Add IPA for 1 minute

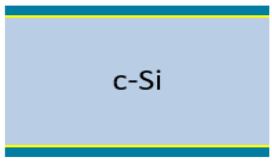
NAOS oxidation



Equipment:

SAL lab
Immerse the wafer in HNO_3 69.5% at room temperature for 30 minutes
Rinse the wafer in water for 4 minutes
Dry after

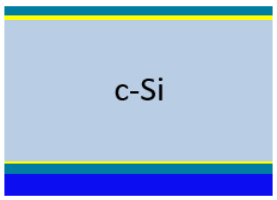
LPCVD (i)a-Si deposition



Equipment:

Furnace E3
Recipe LPOLYBIN

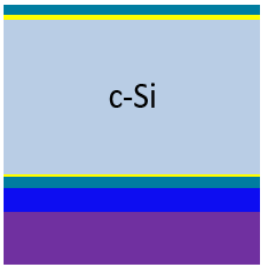
SiN_x PECVD



Equipment:

Novellus EKL lab CR100
Deposit the protective layer with a thickness of at least 50 nm at the back side of the wafer

First layer alignment mask



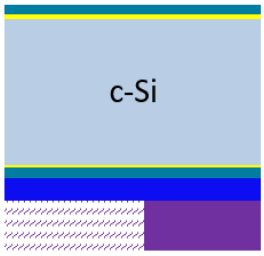
Equipment:

Coater station EVG120
Before the use of coater station EVG120, always align the primary flat to correction direction (bottom, horizontal)
Always check the relative humidity **(48 ± 2 %)** in the room before coating, and follow the instructions for this equipment.
Use the coater station of the EVG120 system to coat the wafers with photoresist.
The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 **negative resist thickness: 1.40 µm**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds

an automatic edge bead removal with a solvent

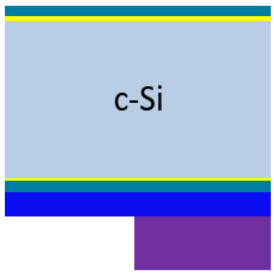
Alignment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-MO contaminated sets
Follow the instruction attached to the tool.

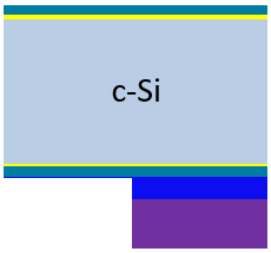
Developing



Equipment :

Developer station, use your own becker

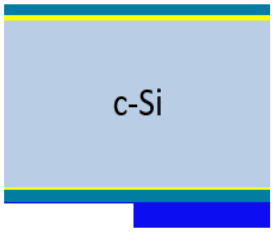
BHF etching



Equipment:

SAL lab
Dip the wafer in BHF solution at room temperature till exposed SiN_x will be etched away.
Rinse in water for 4 minutes
Dry after

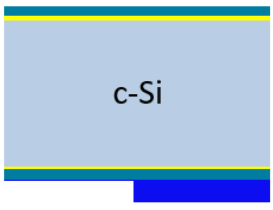
Acetone



Equipment:

SAL lab
Immerse the wafer in acetone at room temperature till photoresist will be etched away.
Dip in water for 4 minutes
Dry after

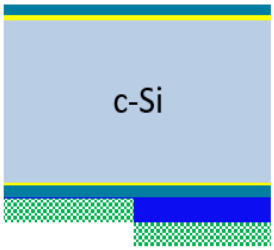
Remove native SiO_x



Equipment:

SAL lab
Immerse the wafer in HF at room temperature surface till will be hydrophobic.
Dip in water for 4 minutes
Dry after

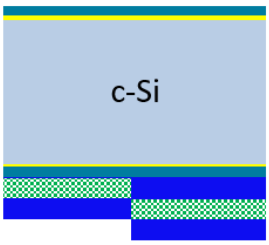
PECVD (p)aSi-C_x



Equipment:

AMOR PECVD
Place the wafer for 40 minutes in the chamber to heat it up.
Deposit (p)a-SiC_x according to the latest recipe.
After this step, the wafer is assumed as `contaminated` therefore no deposition tools in CR100 can be used.

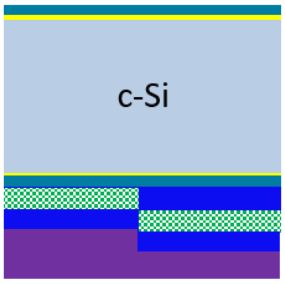
SiN_x PECVD



Equipment:

Plasmalab80Plus Kavli Nanolab that allows `contaminated` samples
Deposit the protective layer with a thickness of at least 50 nm at the back side of the wafer

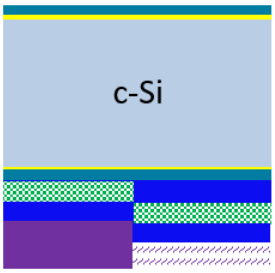
Second layer alignment mask



Equipment:

Coat manually
positive resist thickness: 1.40 µm,

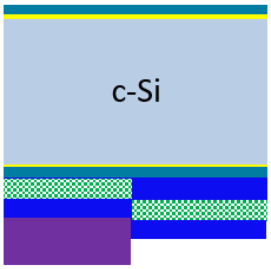
Alignment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-MO contaminated sets
Follow the instruction attached to the tool.

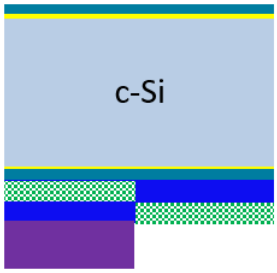
Developing



Equipment :

Developer station you own becker

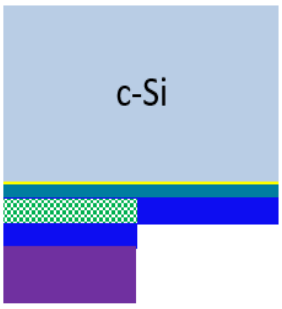
BHF etching



Equipment:

SAL lab
Immerse the wafer in BHF at room temperature till exposed SiN_x will be etched away.
Rinse in water for 4 minutes
Dry after

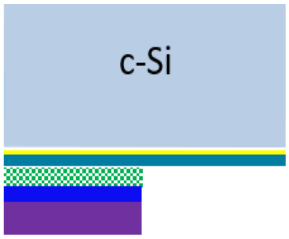
poly-Si etch



Equipment:

SAL lab
Immerse the wafer in poly-Si etch at room temperature for 3 minutes
Dip in water for 4 minutes
Dry after

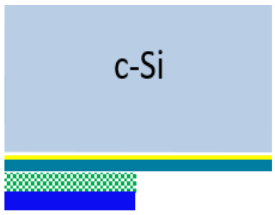
BHF etching



Equipment:

SAL lab
Immerse the wafer in BHF (1:7) solution at room temperature till SiN_x will be removed.
Dip in water for 4 minutes
Dry after

Acetone

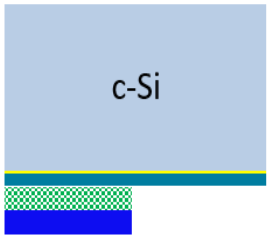


Equipment:

SAL lab
Immerse the wafer in acetone at room temperature until photoresist will be removed.
Dip in water for 4 minutes
Dry after

2. Interdigitated BSF formation

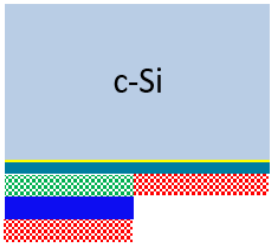
Remove native SiO_x



Equipment:

SAL lab
Immerse the wafer in HF at room temperature surface will be hydrophobic.
Dip in water for 4 minutes
Dry after

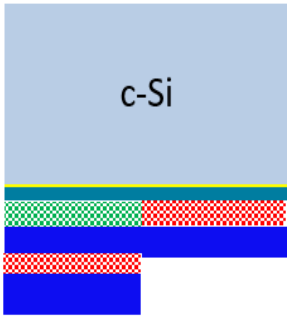
PECVD (n)a-SiC_x



Equipment:

AMOR PECVD
Place the wafer for 40 minutes in a chamber to heat it up.
Deposit (n)a-SiC_x according to the latest recipe.

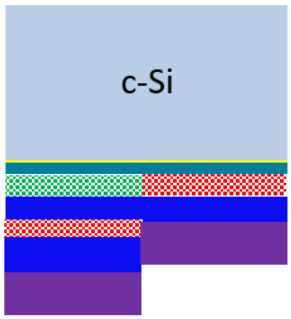
SiN_x PECVD



Equipment:

Plasmalab80Plus Kavli Nanolab
Deposit the protective layer with a thickness of at least 50 nm at the back side of the wafer

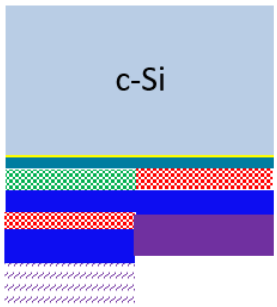
Third layer alignment mask



Equipment:

Coat manually
Negative resist thickness: 1.40 µm,

Alignment and exposure

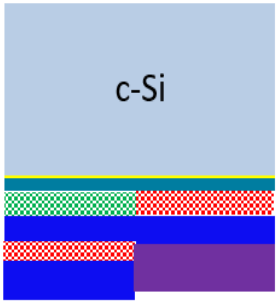


Equipment:

Use contact aligner
Exposure mas IBC-G2-MO contaminated sets

- Follow the instruction attached to the tool.

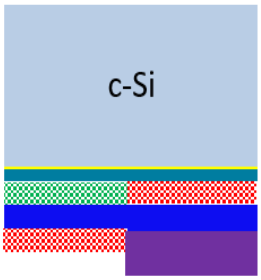
Developing



Equipment :

Developer station your own becker

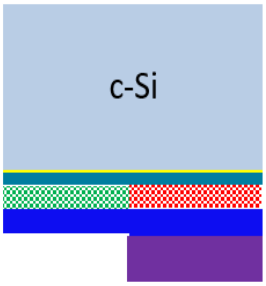
BHF etching



Equipment :

SAL lab
Immerse the wafer in BHF at room temperature till SiN_x will be etched away.
Dip in water for 4 minutes
Dry after

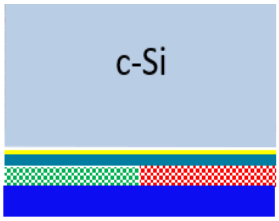
Poly-Si etch



Equipment:

SAL lab
Immerse the wafer in poly-Si etch at room temperature for few minutes (etching tests)
Dip in water for 4 minutes
Dry after

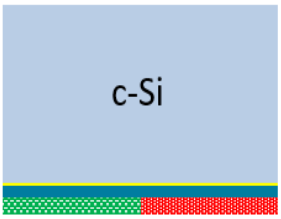
Acetone



Equipment:

SAL lab
Immerse the wafer in Acetone at room temperature till photoresist is completely removed
Dip in water for 4 minutes
Dry after

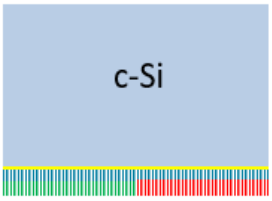
BHF etching



Equipment :

SAL lab
Immerse the wafer in BHF at room temperature till SiN_x will be etched away.
Dip in water for 4 minutes
Dry after

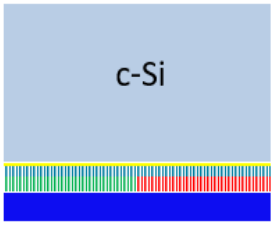
3. Annealing



Equipment:

Furnace A2 MEMS lab variable temperature and time

4. Hydrogenation



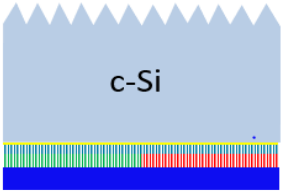
Equipment:
Plasmalab80Plus Kavli Nanolab:

SiN_x layer thickness 100 nm temperature 400°C.

FGA FURNANCE A3 recipe FGA YANG

5. Texturing

Texturing

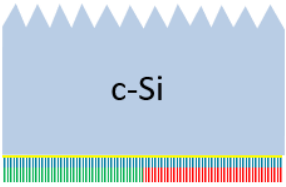


Equipment:

Mems lab PVMD group bench

Switch on the heater at 80°C for ~30-45 min
(Texturing time depends on how fresh is the solution)
Check the etching time on a dummy wafer (it should be 12-15min)
Dip in water for 5 minutes

BHF etching



Equipment:

SAL lab

Dip wafer in BHF until SiNx layer will be removed

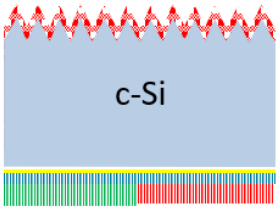
Dip in Di water for 5 minutes

Dry after

6. FSF

Equipment:

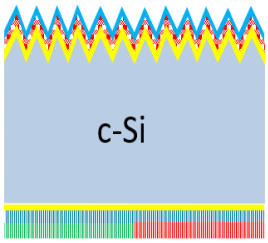
PECVD device Amigo CR10k



(i)a-Si:H + (n)nc-SiOx:H from SHJ solar cells

7. Front anti reflection coating and metallization

ARC coating deposition

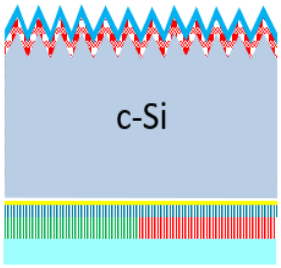


Equipment:

Plasmalab80Plus Kavli Nanolab:

Thickness: adjust thickness according to the refractive index.
SiN_x composition SiH_4 20 sscm NH_3 20 sscm
Adjust time low temperature below 200°C

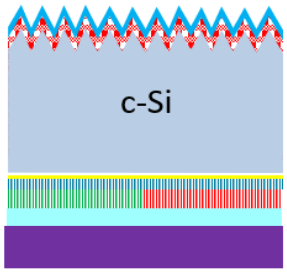
TCO deposition



Equipment :

Zorro Sputtering
ITO thickness 150 nm on the rear side

Fourth layer alingment mask



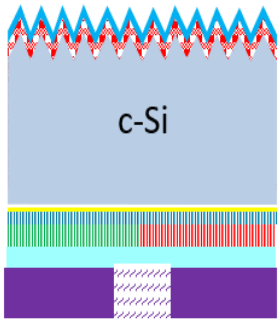
Equipment:

Coat manually
Negative resist thickness: 1.40 µm,

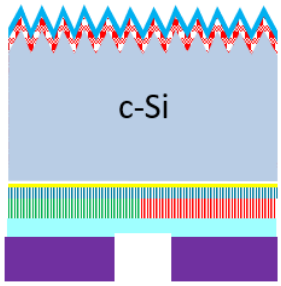
Alingment and exposure

Equipment:

Use contact aligner
Exposure mask IBC-G2-ME contaminated sets
Follow the instruction attached to the tool.



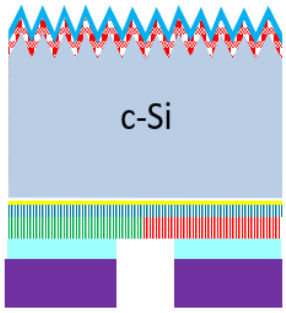
Developing



Equipment :

Developer station you own batch

ITO etching



Equipment:

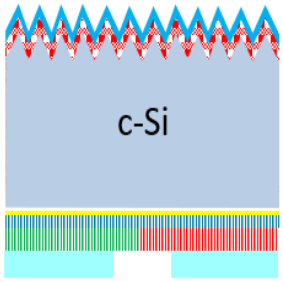
SAL lab

Dip wafer in HCl until TCO in the opening will be removed (approximately 20 minutes)

Dip in Di water for 5 minutes

Dry after

Acetone



Equipment:

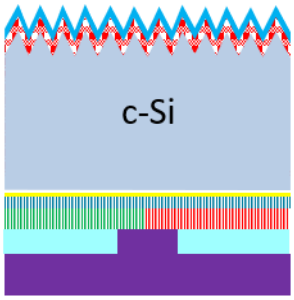
SAL lab

Dip wafer in Acetone until photoresist will be removed.

Dip in Di water for 5 minutes

Dry after

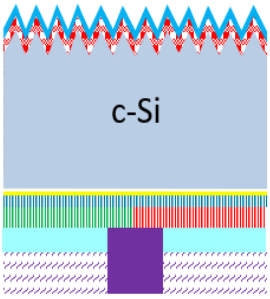
Fifth layer alignment mask



Equipment:

Coat manually
Positive resist thickness: 1.40 µm,

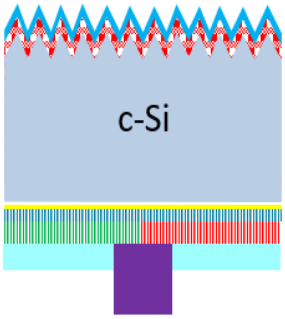
Alignment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-ME contaminated sets
Follow the instruction attached to the tool.

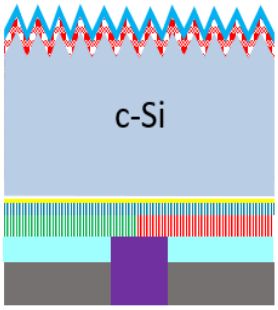
Development



Equipment :

Developer station you own batch

Metallization



Equipment:

Provac
Metal contact 2 um Ag layer

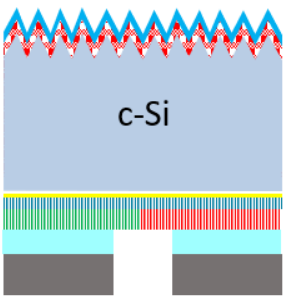
Acetone

Equipment:

SAL lab

Dip wafer in acetone until photoresist will be removed.

Dip in Di water for 5 minutes

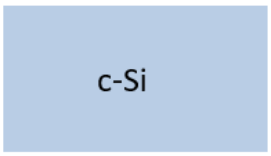


Dry after

Appendix B

1. Interdigitated emitter formation

Standard cleaning



Equipment:

Cleaning bench - HNO_3 99% Si (RT) and HNO_3 69.5% Si (110 °C)

Before the cleaning, check if heating of HNO_3 69.5% is on.

Cleaning 10 minutes in fuming nitric acid (99%) at ambient temperature.

Use wet bench "HNO_3 (99%)" and the carrier with the white dot.

Rinsing in the DI water with the standard program.

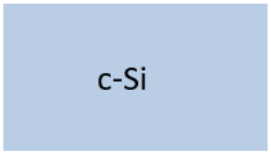
Cleaning 10 minutes in concentrated nitric acid (69.5%) at 110 °C.

Use wet bench “HNO3 (69.5%)” and the carrier with the white dot.

Rinsing in the DI water with the standard program.

Drying Use the Spin Rinse Dryer (SRD) with the standard program, and the carrier with a red dot.

Marangoni



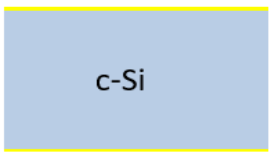
Equipment:

Cleaning bench
Immerse wafers for 5 minutes in HF (check if hydrophobic)

Immerse wafers for 4 minutes in DI Water

Add IPA for 1 minute

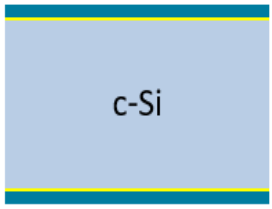
NAOS oxidation



Equipment:

SAL lab
Immerse the wafer in HNO_3 69.5% at room temperature
Dip in water for 4 minutes
Dry after

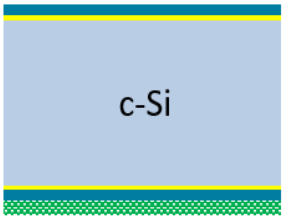
LPCVD (i)a-Si deposition



Equipment:

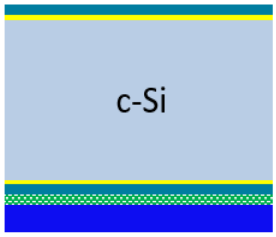
Furnace E3
Recipe LPOLYBIN

PECVD (p)a-SiC$_x$



Equipment:
AMOR PECVD
Place the wafer for 40 minutes in a chamber to heat it up.
Deposit (p)a-SiC$_x$ according to the latest recipe.
After this step, the wafer is assumed as `contaminated` therefore no deposition tools in CR100 can be used.

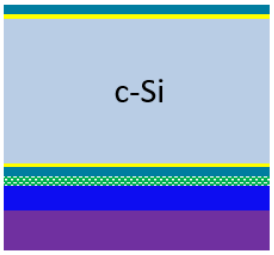
SiN$_x$ deposition



Equipment:

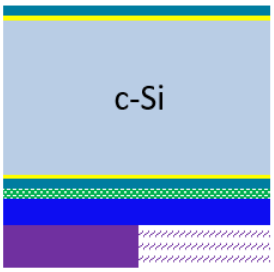
Plasmalab80Plus Kavli Nanolab
Deposit the protective layer with a thickness of at least 50 nm at the back side of the wafer

First layer alignment mask



Coat manually
Positive resist thickness: 1.40 µm,

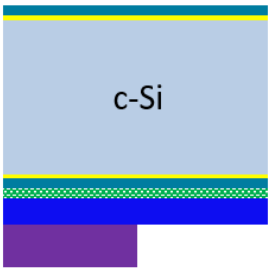
Alignment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-MO contaminated sets
Follow the instruction attached to the tool.

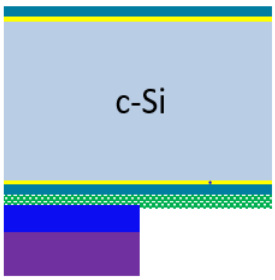
Development



Equipment :

Developer station your own becker

BHF etching



Equipment:

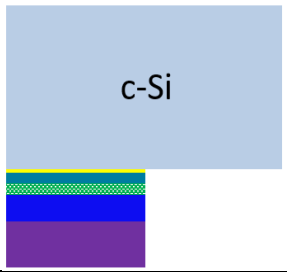
SAL lab PVMD

Dip wafer in BHF solution until SiN_x in the opening will be removed

Dip in Di water for 5 minutes

Dry after

poly-Si etch



Equipment:

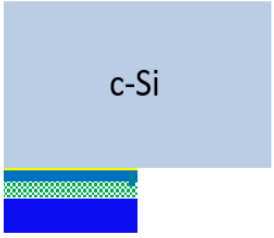
SAL lab PVMD group bench acetone

Dip wafer in prepared poly-Si solution until (p)a-SiCx and (i)a-Si in the opening will be removed

Dip in Di water for 5 minutes

Dry after

Acetone



Equipment:

SAL lab PVMD

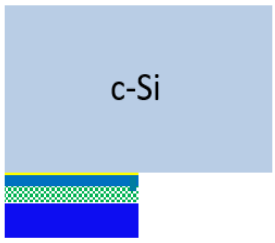
Dip wafer in acetone until photoresist will be removed

Dip in Di water for 5 minutes

Dry after

2. Interdigitated BSF formation

Remove native oxide



Equipment:

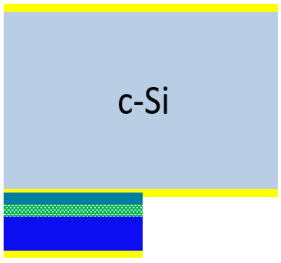
SAL lab PVMD

Dip wafer in HF solution until surface will be hydrophobic

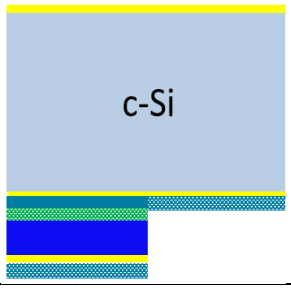
Dip in Di water for 5 minutes

Dry after

NAOS oxidation (as given)



PECVD (i)a-Si:H

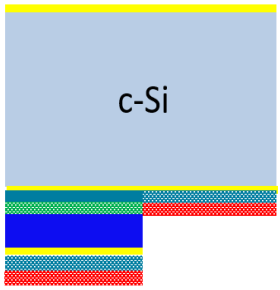


Equipment:

AMOR PECVD

Place the wafer for 40 minutes in a chamber to heat it up.
Deposit (i)a-Si:H according to the latest recipe.

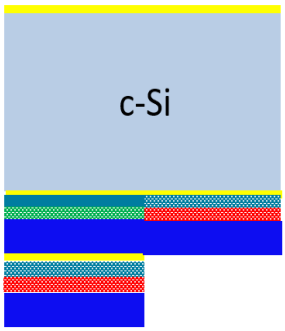
PECVD (n)a-SiC$_x$



Equipment:

AMOR PECVD
Place the wafer for 40 minutes in a chamber to heat it up.
Deposit (n)a-SiC_x according to the latest recipe.

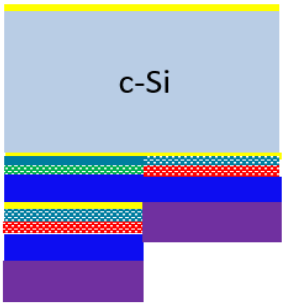
SiN_x deposition



Equipment:

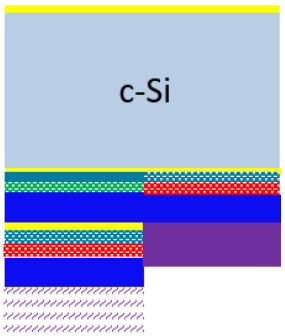
Plasmalab80Plus Kavli Nanolab
Deposit the protective layer with a thickness of at least 50 nm at the back side of the wafer

Second layer alignment mask



Coat manually
negative resist thickness: 1.40 µm,

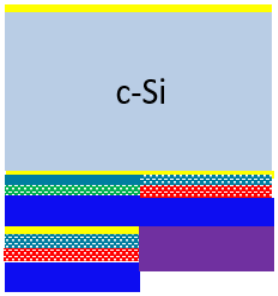
Alingment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-MO contaminated sets
Follow the instruction attached to the tool.

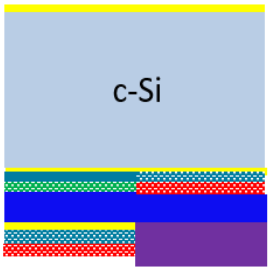
Development



Equipment:

Developer station your own becker

BHF etching



Equipment:

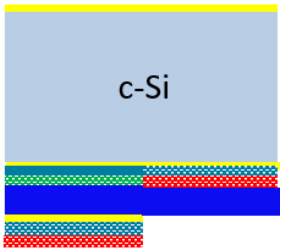
SAL lab PVMD

Dip wafer in BHF solution until SiN_x surface will be etched away.

Dip in Di water for 5 minutes

Dry after

Acetone



Equipment:

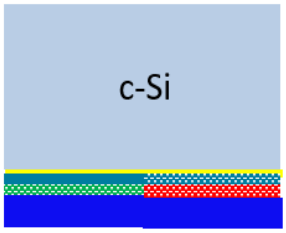
SAL lab PVMD

Dip wafer in acetone until photoresist will be removed.

Dip in Di water for 5 minutes

Dry after

Poly-Si etch



Equipment:

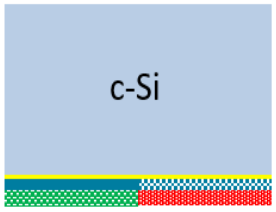
SAL lab PVMD

Dip wafer in prepared poly-Si solution until (n)a-SiCx and a-Si:H will be etched away.

Dip in Di water for 5 minutes

Dry after

BHF etching



Equipment:

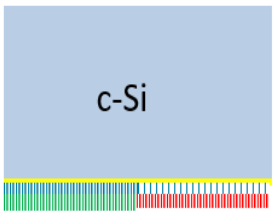
SAL lab PVMD

Dip wafer in BHF solution until SiN_x surface will be etched away.

Dip in Di water for 5 minutes

Dry after

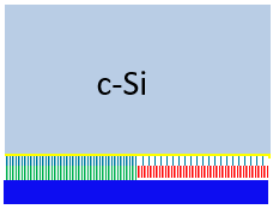
3. Annealing



Equipment:

Furnace A2 MEMS lab variable temperature and time

4. Hydrogenation

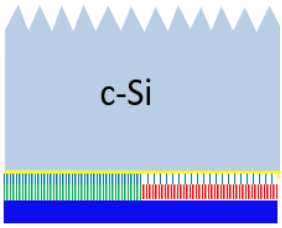


Equipment:
Plasmalab80Plus Kavli Nanolab:

SiN_x layer thickness 100 nm temperature 400°C.

FGA FURNANCE A3 recipe FGA YANG

5. Texturing

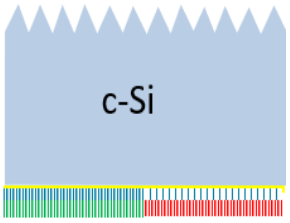


Equipment:

Mems lab PVMD group bench

Switch on the heater at 80°C for ~30-45 min
(Texturing time depends on how fresh is the solution)
Check the etching time on a dummy wafer (it should be 12-15min)
Dip in water for 5 minutes

BHF etching



Equipment:

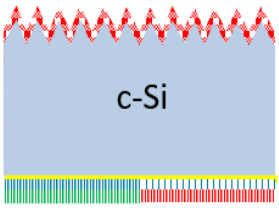
SAL lab

Dip wafer in BHF until SiNx layer will be removed

Dip in Di water for 5 minutes

Dry after

6. FSF



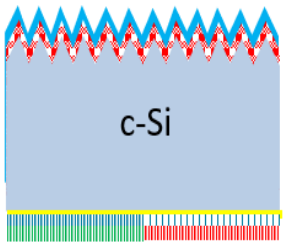
Equipment:

PECVD device Amigo CR10k

(i)a-Si:H + (n)nc-SiOx:H from SHJ solar cells

7. Front anti reflection coating and metallization

ARC coating deposition



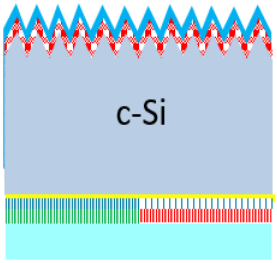
Equipment:

Plasmalab80Plus Kavli Nanolab:

Thickness: 60 nm
SiN_x composition SiH_4 20 sscm NH_3 20 sscm
Adjust time

Low temperature below 200 degrees

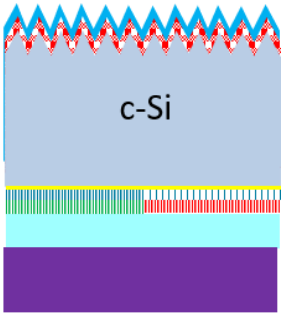
TCO deposition



Equipment :

Zorro Sputtering
ITO thickness 150 nm

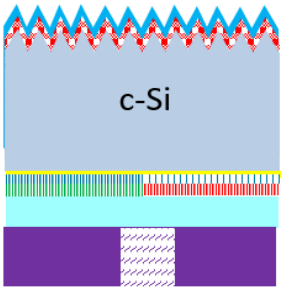
Third layer alingment mask



Equipment:

Coat manually
Negative resist thickness: 1.40 µm,

Alingment and exposure



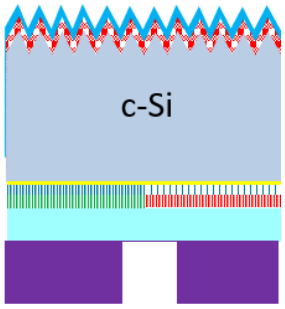
Equipment:

Use contact aligner
Exposure mask IBC-G2-ME contaminated sets
Follow the instruction attached to the tool.

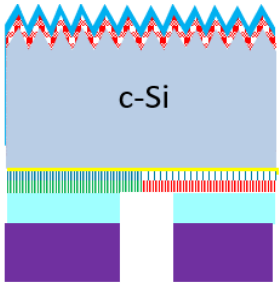
Developing

Equipment :

Developer station you own batch



ITO etching



Equipment:

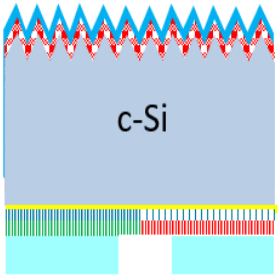
SAL lab

Dip wafer in HCl until TCO in the opening will be removed

Dip in Di water for 5 minutes

Dry after

Acetone



Equipment:

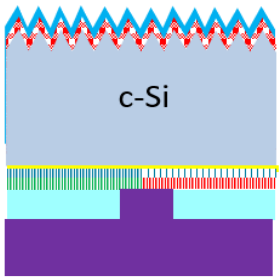
SAL lab

Dip wafer in Acetone until photoresist will be removed.

Dip in Di water for 5 minutes

Dry after

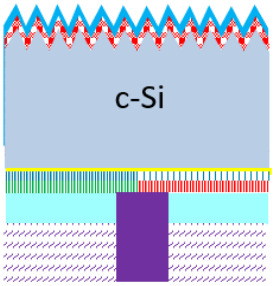
Fourth layer alignment mask



Equipment:

Coat manually
Positive resist thickness: 1.40 µm,

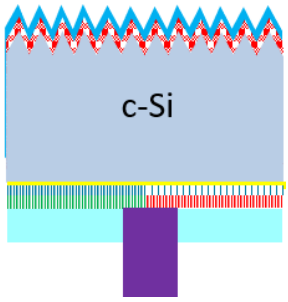
Alignment and exposure



Equipment:

Use contact aligner
Exposure mask IBC-G2-ME contaminated sets
Follow the instruction attached to the tool.

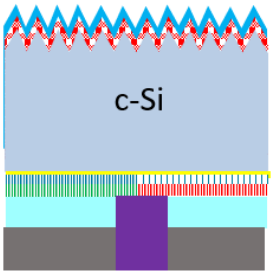
Development



Equipment :

Developer station you own batch

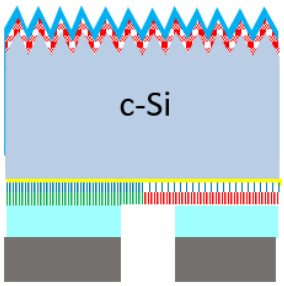
Metallization



Equipment:

Provac
Metal contact 2 um Ag layer

Acetone



Equipment:

SAL lab

Dip wafer in acetone until photoresist will be removed

Dip in Di water for 5 minutes

Dry after

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