MMC PERFORMANCE EVALUATION CONCERNING DIFFERENT DC BREAKERS AND CONVERTERS

Pragati Kidambi Murali

TU Delft

MMC performance evaluation concerning different DC breakers and converters

By

Pragati Kidambi Murali

to obtain the degree of Master of Science
in Electrical Engineering
at the Delft University of Technology
to be defended publicly on Friday, August 28, 2020 at 02:00 PM.

Student number	4823656		
Thesis committee	Dr.ir. M. Popov	Associate Professor, Academic Supervisor, Chair	TU Delft
	Dr. A. Lekic	Assistant Professor, Committee	TU Delft
	Dr. B. Gholizad	Assistant Professor, Committee	TU Delft
	Ir. K. Koreman	Industrial Supervisor, Committee	TENNET TSO

Summary

Renewable energy resources are the most successful, promising, and economical mode of energy generation. Moreover, wind energy is also one of the victorious candidates in generating renewable energy. Currently, High Voltage Direct Current (HVDC) systems are designed to integrate the energy harvested in the Offshore Wind Farm (OWF) to the grid system. The HVDC system uses AC-DC converters, and then with the help of DC cables the power is transmitted from the offshore to the onshore area, where it again gets converted back to AC. The converters used here are called high voltage converters, where these power electronic components have the ability to sustain high voltages and current. Further, in this thesis Modular Multilevel Converter (MMC) is used for the conversion of AC to DC and vice versa.

The MMC is built using stacked Insulated Gate Bipolar Transistor (IGBT)s, where these power electronic components are current sensitive in nature. Thereby, if there is a fault, and if this fault current flows through them, then these components get damaged permanently. Moreover, if the offshore MMC goes down, the OWF system has to undergo a restart. Therefore, the DC Circuit Breaker (DCCB) is used in order to clear the DC fault in an HVDC system and thereby protecting the grid side.

Meanwhile, designing a DCCB for HVDC system is not easy, one major reason is that there are no natural zero crossings in a DC Fault. Also, the fault must be cleared very quickly because DC faults have a very high rate of rising in fault currents. Currently, the MMC protects itself by using the blocking algorithm. Here, the switching devices turn off temporarily until the fault is cleared. When they are turned off, the fault current flows through the freewheeling diodes, as diodes have the capability to withstand high currents.

Indeed, if the MMC is blocked, the purpose of DCCB is not completely justified. Therefore, in this thesis, the performance of the MMC is examined with the presence of DCCBs for a $525KV$ system. Besides, there are two DCCBs used, in order to evaluate the more suitable breaker for the system. Further, with the initial performance, the fault behavior of MMC is analysed and illustrated. Consequently, the DC inductance, converter inductance, and arm inductance were modified in order to improve the performance of the system.

On the other hand, there are two types of MMC, namely Half Bridge MMC (HB MMC) and Full Bridge MMC (FB MMC). Generally, this HB MMC are called as fault feeding converters, whereas the FB MMC are called as fault blocking converters. This is due to the topology of the FB MMC, where it completely blocks the fault current by itself. Therefore, the performance of the HB MMC with a DCCB is compared with the FB MMC with blocking protection for a 320 KV network.

Acknowledgement

With immense gratitude, I am going to thank my building blocks of this thesis. First and foremost, I would like to whole-heartedly thank *Dr. Marjan Popov* from Delft University of Technology and *Ir. Kees Koreman* from TenneT TSO B.v for supervising and supporting me throughout the Master thesis. Their experience and expertise have provided me a strong technical background, apart from that, I also learned some presentation tactics. I also extend my immense thanks to the thesis committee members, *Dr. Babak Gholizad* and *Dr. Aleksandra Lekic*. Further, I also want to extend my profound and sincere thanks to *Ir. Sertkan* and *Dr. Yanny* from TenneT for providing me valuable suggestions, techniques, and improvements during the weekly meetings. I would also like to thank *Prof.ir. M.A.M.M. van der Meijden* for providing me this opportunity in the first place. Further, I would like to thank Ir. Seyed Mirhosseini, and Ir. Ajay Shetgaonkar for sharing the models, clearing my doubts concerning the models, and also Dr. Siyuan Liu for giving me a headstart for the thesis. Moreover, I would like to thank Dr. Thiago for clearing my doubts concerning power electronics during the literature phase. I would like to thank the secretaries of the IEPG research group, Ellen and Carla, for providing the Master students all the facilities before the corona pandemic and also with respect to communication to the Board of Examiners. Also, I thank Manager, Patrick and student HR, Janine for helping me with the document work during the initial phase at TENNET. I also thank the TENNET TSO for the opportunity and financial support. Finally, I would like to thank Anil Kumar and Ajay for proofreading my whole thesis.

This thesis won't be possible without *Family and Friends*. I would like to thank my mom Chithra, my dad Murali and my brother Aadhi for bearing with all my tantrums throughout the year. They are my biggest and strongest support untill now. I would also like to thank my friends who are in oversea, Srivarshini, Vaishnave, Rajalakshmi, Vaidhegi, and Shachin by providing me a constant encouragement and stress relief calls often. I also would like to immensely thank my support system of the Netherlands, Anil Kumar, Subhitcha, Saravana, Kanya, Raj, and Madhumitha.

Pragati Kidambi Murali
Delft, 28th August 2020

Dedicated to my
Wonder women and Iron man - Chithra and Murali
Little groot - Aadhi Kesav
My evergreen stars in my heart - Vasantha and Chakravarthy.

Contents

List of Figures

List of Tables

1

Introduction

1.1. Introduction to HVDC systems

"Electric power is everywhere present in unlimited quantities and can drive the world's machinery without the need for coal, oil or gas" - Nikola Tesla (1856-1943).

According to the Paris agreement, the United Nations Framework Convention on Climate Change (UNFCCC) with 197 countries decided to reduce the global warming by $1.5^{\circ}C$ while trying for 2.0°C [1]. Climate change is global concern, given that one of the major contributions to increase in CO_2 is from fossil fuel power plants. The shift towards renewable energy is inevitable, and wind energy is one of the predominant sources of renewable resources. The wind energy can be harvested either onshore or offshore. The offshore wind energy is a faster and steady source of energy, thus more promising. The concept of High Voltage Direct Current (HVDC) transmission is the key technology which enables Offshore Wind Farm (OWF) to be a promising wind energy supply. The HVDC transmission is more advantageous than HVAC transmission system, owing to the efficiency, grid support, stability, and controllability.

- **Efficiency**: The efficiency of the AC system is lower owing to the presence of reactive power, which is due to the phase difference between voltage and current that occupies the transmission capacity. In addition, the losses are high due to the skin effect which increases the transmission capacity only through the surface of the conductor, thereby increasing the total equivalent impedance and power losses in the cable. Even though the latest AC cables are having improved efficiency by reducing the skin effect losses; it increases the overall cost and complexities of the cables.

- **Grid support**: The HVDC grid can support the weak grids by modifying the impedance. Introducing the Phase Locked Loop (PLL) for synchronization

1

[2] can further provide synchronization and grid support. Further, two asynchronous systems (different frequency) can be connected together using back to back HVDC system, thus forming more robust systems.

- **Controllability**: The ability to control the active and reactive power independently on an HVDC system has given higher degree of freedom in power control. The flexibility is also due to the four quadrant operation possibility in Voltage Source Converter (VSC) mode [3].
- **Stability**: By Equal Area Criterion (EAC), the generators go out of stability if the fault is not cleared within the critical clearing time; which is due to the excess kinetic energy stored in the rotor [4]. However, VSC HVDC has the capacity of reversing the power flow (by changing the current direction), so that it can quickly release energy to the healthy part of the system thus preventing the healthy system from going into instability. The quick power reversal ability increases its capability to change up to two times the rated power [3].
- **Cost**: HVDC cables are more cost-effective after $50Km$ (the break-even distance), this is explained in the Figure 1.1

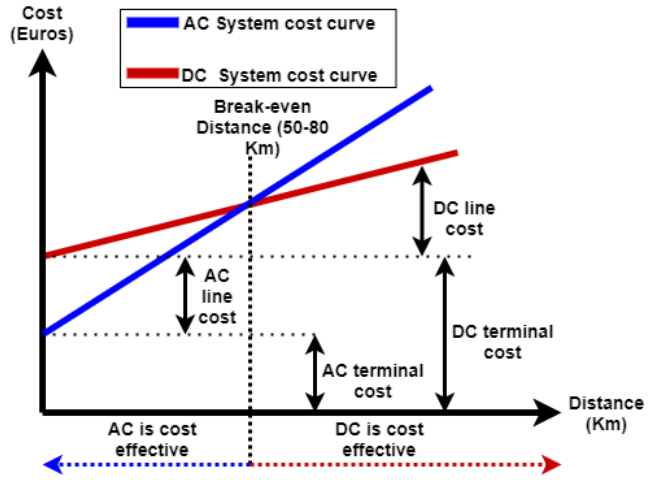

Figure 1.1: Cost comparison for HVAC submarine cable vs HVDC submarine cable [5]

Thus, Offshore Wind Farm (OWF) connected to HVDC is more advantageous than the HVAC systems. The number of HVDC projects in Europe is rising yearly, to make the grid the current and upcoming HVDC networks are shown in Figure 1.2 as per the year 2020.

But, there are also bottlenecks involved in the HVDC systems, such as converter losses, switching losses, commutation failures (in case of Line Commutated Converter (LCC)), interoperability, protection for DC cables and black start capability.

Therefore, there is an ongoing evolution in system level as well as component level in the HVDC technology. This includes DC converters, HVDC cables, DC Circuit Breaker (DCCB), Gas Insulated Substation (GIS), etc, as there are a lot of complexities involved, which has to be solved and analysed to make HVDC as a reliable, robust and secured transmission system for the future power systems.

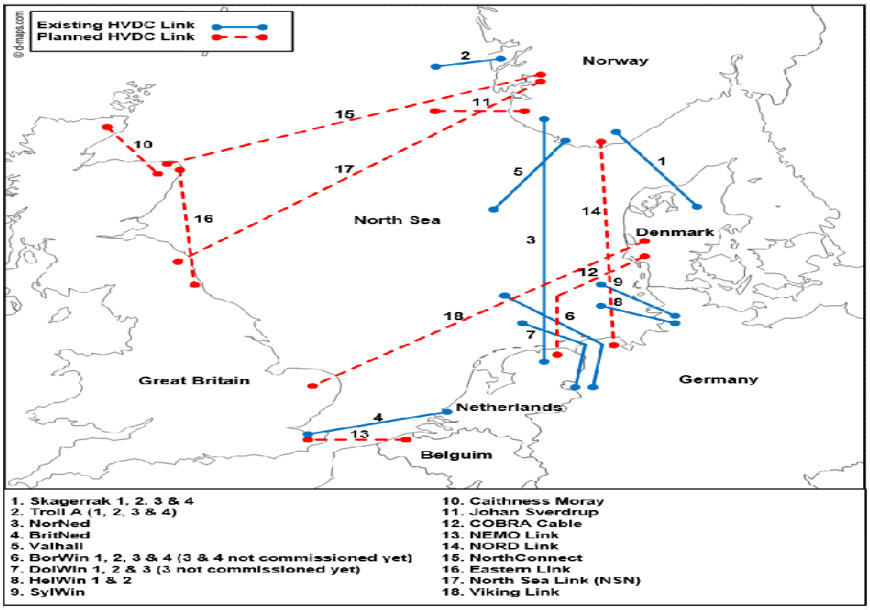

Figure 1.2: HVDC Network in Europe [6]

1.2. Motivation

The most famous HVDC systems in the Netherlands are BritNed, NorNed, and Cobra cable, whose details are given in the Table 1.1. Currently, the VSC based HVDC is operating with the maximum voltage of $450\ KV$ in the Netherlands. However, one main advantage of DC networks is that it can be transmitted at higher voltage levels. Eventually, the only power electronic component used for high voltage - high current is thyristors. But, the main disadvantage of thyristors is, it can be operated in two quadrants i.e unidirectional power flow is only possible. Even though Insulated Gate Bipolar Transistor (IGBT)'s have high voltage withstanding capacity, it is very sensitive to high currents. In addition, special care must be taken while handling DC faults, since they are more severe in nature. On the other hand, the upcoming HVDC bipole system planned by TENNET TSO is operating at $\pm 525\ KV$ DC. Thus, the fault behavior of the system has to be carefully analysed component and system-wise for various scenarios. Therefore, the thesis deals with OWF connected to MMC HVDC system with DC voltage $525\ KV$.

1

HVDC System	Countries	DC Voltage (KV)	AC Voltage 1 (KV)	AC Voltage 2 (KV)	Cable Length (Km)
BritNed	Netherlands-Britain	450	380	400	260
NorNed	Netherlands-Norway	450	400	300	580
Cobra Cable	Netherlands-Denmark	320	400	400	325

Table 1.1: The basic details of few HVDC connections in the Netherlands

1.3. Research background and Research questions

This thesis will focus on OWF connected Multi-Terminal HVDC (MTHVDC) network and the system characteristics are given in Table 1.2

The configuration of the system can always determine the re-routing power possibility. The bipolar configuration is used in order to improve the reliability and Security of Supply (SoS). With the help of two converters at each terminal, one connected to positive and ground, and the other connected to negative and ground as shown in the Figure 1.3, the reliability can be increased. If one of the conductor is out of service, the healthy pole can transfer the power at reduced capacity, and a relatively lower voltage conductor will act as the metallic return [7]. The Modular Multilevel Converter (MMC) have lower switching frequency and better power quality compared to VSC, this is because MMC follows the Step Pulse Modulation (SPM) strategy instead of Pulse Width Modulation (PWM). SPM provides low switching losses and high waveform quality [8]. Thus, the MMC is preferred in the upcoming HVDC projects.

DC Voltage	$\pm 525KV$
AC Voltage	$400KV$ L-L RMS
Frequency (AC)	50 Hz
Configuration	Bipole with Metallic Return
Converter Model	MMC
Number of Terminals	4

Table 1.2: The system details of the MTHVDC network

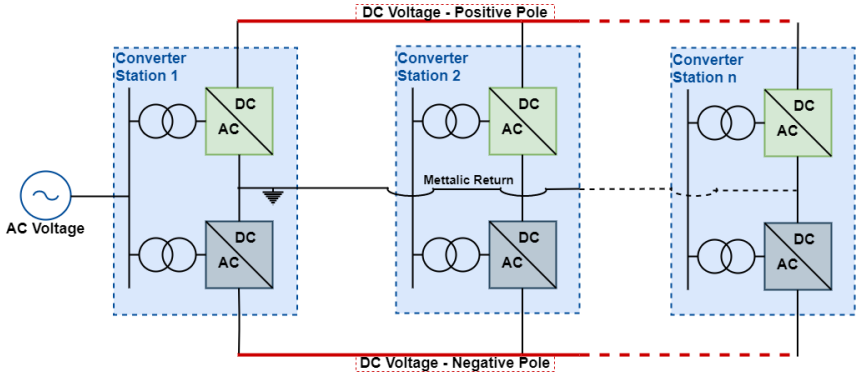

Figure 1.3: Bipole with Metallic return configuration connected back to back

As we shift to higher DC voltage levels, the protection of system must be taken special care, especially to the converter system. Since the IGBTs are current sensitive, they have their own protection system by blocking the switching devices. Afterwards, the fault current flows through the anti-parallel diodes and enters rectification mode if the converter is in standalone operation. On the other hand, fault currents generated during DC faults are higher than AC faults for the rated voltage levels, this is demonstrated in Figure 1.4 for the model shown in Figure 3.1.

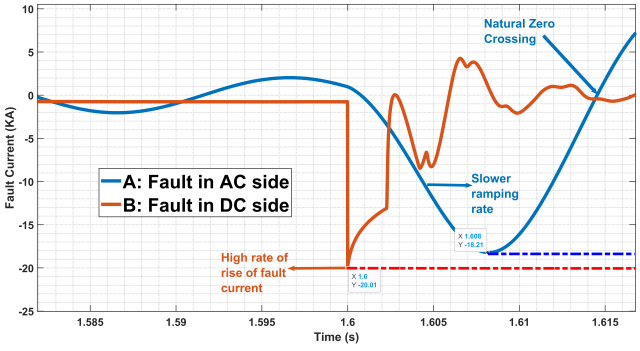

Figure 1.4: Fault current for two different cases, A - When fault is in the AC side of the converter (Single phase to to Ground Fault), B - Fault is in the DC side of the converter (Pole to Ground Fault) for the model shown in Figure 3.1

In this example, a single phase to ground fault (phase A) is applied in the AC side of the converter, and a pole to ground fault is applied in the DC side of the converter. For, both of the cases, the fault is applied at $1.6s$. Further, there is a zero crossing observed in the DC side due to the presence of the breaker. Since the DC faults are severe in nature, the faulty system has to be separated quickly, thus the development of DC Circuit Breaker (DCCB) has been initiated. Unlike AC faults,

there is *no natural zero crossings in DC Fault current*, thus artificial zero crossings are created. The main challenges in DCCB are creation of artificial current zero, energy dissipation across the system inductance, and the capacity to sustain the voltage response of the system after the interruption of the fault current [9].

As mentioned before, it is also important to have MMC's own protection because there is a chance that the DCCB might fail in certain circumstances or there might be an operation delay. But, the converter must be protected in any of the cases, as its a very sensitive component in an HVDC system. Thus, this thesis revolves around the protection of MMC and its performance.

1.3.1. Research questions

This thesis focuses on three main research objectives, they are

- The validation of performance and protection for the MMC during different faults, using DCCB has to be evaluated. Here, we use two different types of DCCB namely *Mechanical CB* and *VSC assisted Resonant Current CB*.
- The coordination between the MMC protection and the DCCB protection.
- Analysis of protection and performance for Half Bridge MMC (HB MMC) with DCCB and Full Bridge MMC (FB MMC) with blocking algorithm.

The detailed explanation and literature of the different DCCBs, HB MMC and FB MMC are discussed in the chapter 2.

1.4. Outline of Thesis

The whole thesis report is split into 6 chapters. **chapter 2** explains the severity of DC faults, Overview of MMC, current interruption by a simple DCCB, and the MMC protection techniques. Further, **chapter 3 and chapter 4** elucidates the HB MMC responses with respect to different DCCBs and the coordination techniques. Consequently, **chapter 5**, compares the performance of HB MMC and FB MMC protection system. Finally, the chapter 6 concludes the results of the complete master thesis and suggested future works.

References

[1] S. Teske, T. Pregger, S. Simon, T. Naegler, S. Schmid, and M. Meinshausen, *Achieving the Paris Climate Agreement Goals* (2019).

[2] J. A. Suul, S. D'Arco, P. Rodriguez, and M. Molinas, *Extended stability range of weak grids with voltage source converters through impedance-conditioned grid synchronization,* in *11th IET International Conference on AC and DC Power Transmission* (2015) pp. 1–10.

[3] L. Zhang, L. Harnefors, and P. Rey, *Power system reliability and transfer capability improvement by vsc-hvdc (hvdc light ©),* (2007).

[4] J. Grainger and W. Stevenson, *Power system analysis*, McGraw-Hill series in electrical and computer engineering: Power and energy (McGraw-Hill, 1994).

[5] Siemens, *Siemens hvdc transmission,* (Accessed 28 July 2020).

[6] A. Elahidoost and E. Tedeschi, *Expansion of offshore hvdc grids: An overview of contributions, status, challenges and perspectives,* in *2017 IEEE 58th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)* (2017) pp. 1–7.

[7] CIGRE-B4-52, *Hvdc grid feasibility study,* (2013).

[8] M. Hagiwara and H. Akagi, *Control and experiment of pulsewidth-modulated modular multilevel converters,* IEEE Transactions on Power Electronics **24**, 1737 (2009).

[9] C. M. Franck, *Hvdc circuit breakers: A review identifying future research needs,* IEEE Transactions on Power Delivery **26**, 998 (2011).

2

Overview of DCCB and MMC

This chapter gives the overview of the technologies used and their details. Initially, the basic components of an HVDC system in explained (section 2.1), followed by an introduction to MMC (section 2.2). Subsequently, the transient behaviour of DC faults is explained (section 2.3). Further, the aspects of a DCCB are discussed. Finally, it is summarized on conclusion.

2.1. HVDC systems

The Figure 2.1 shows the basic components in an HVDC system. Here the VSC HVDC system is explained without the addition of DCCB. The main purpose of this section is to give an idea about general components in an HVDC network.

- **Point of Common Coupling (PCC)**: The interconnection of the AC system and VSC or LCC unit takes place via PCC. Here VSC is operated as controllable voltage source, thereby it has the ability to generate required voltage (magnitude and phase). This ensures that predetermined amount of reactive and active power are exchanged through the PCC [1].
- **AC filters**: The AC filters are used to eliminate the harmonics created due to switching of valves. However, the harmonics filter are required only for 2 level and 3 level VSC and LCC systems and not an essential element for MMC unit. These AC filter can either be 2^{nd} order filter, 3^{rd} order filter, notch filter or LCL filter [2].
- **Converter transformer**: The converter transformer is used in order to connect different voltage level of AC side and the VSC unit. The ripple current is also removed by the converter transformer.
- **Phase reactor**: The phase reactor has two purposes, first is to facilitate the active and reactive power transfer and control. Secondly, to filter the higher order harmonics.

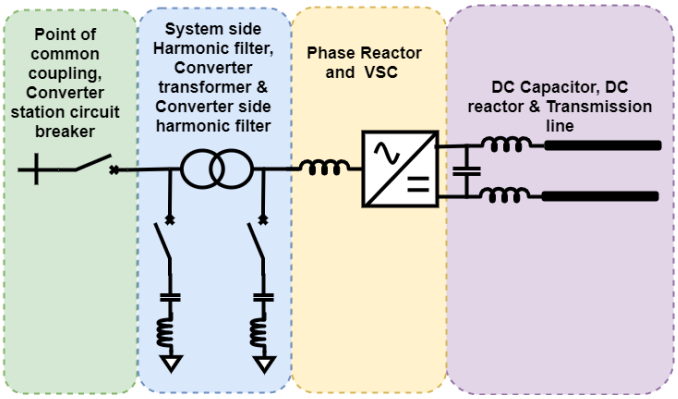

Figure 2.1: HVDC system components [3]

- **DC capacitors**: The DC capacitor have dual benefit, it acts as a storage element as well as to minimize the ripple content in the DC side. The DC capacitor is not predominantly essential for MMC because, it contains cell capacitors in each of the sub modules, which already acts as the storage element. The capacitor's energy storing capacity is characterized by its time constant (τ) as shown in the Equation 2.1 [1]. In the model shown in Figure 3.1 an optional DC capacitor of $25\mu F$ is used. However, it is not enabled in maximum of the simulation results.

$$\tau = \frac{C_{\mathrm{dc}} v_{\mathrm{dc}}^2}{2 \cdot P_{\mathrm{N}}} \tag{2.1}$$

$$\tau = 6.8\ ms$$

  Here, the τ is the time constant for the capacitor, C_{dc} is the extra DC capacitance value, V_{dc} is the DC voltage of the system and P_N is the rated power transfer.

- **DC reactor**: The DC reactor is used to slowdown the rate of rise of fault current. This is used together with the DCCB so that the fault current does not rise quickly thereby blocking the converter. The sizing of the inductor with respect to the DCCB can be found in [4].

- **Transmission line**: It can be either cable or Over Head Lines (OHL). The basic difference is the inductance and capacitance values, where the inductance is higher for OHL, whereas capacitance is higher for cables. Anyways, submarine HVDC cables are used in the upcoming chapters.

2.2. Overview of MMC

The converters used for HVDC went through a lot of evolution. The basic classification of the high power converters can be found in [5]. The main types of

converters used for HVDC systems are either LCC or VSC. The predominant disadvantages of LCC systems are unidirectional power flow, commutation failure and lack of controllability [6]. However, bidirectional power flow is possible in the LCC system by reversing the voltage using polarity changing switches or by modifying the converter topologies and this has been used in [7]. However, this comes with the cost of constructing the poles and the neutral at the fully rated DC voltage, thereby increasing the insulation complexities. Moreover, VSC converters are more advantageous in order to have multi terminal grid operation. The main reason are due to the quick current reversal, controllability, lesser area compared to a LCC system, no commutation failure, rigid support in case of AC faults and enhanced grid support. Further, after extensive research, it is been proven that VSC is more suitable for HVDC systems [8–12]. However, VSC also have its own disadvantages, especially higher power losses compared to LCC [13]. The list of VSC based HVDC systems worldwide are found in [12].

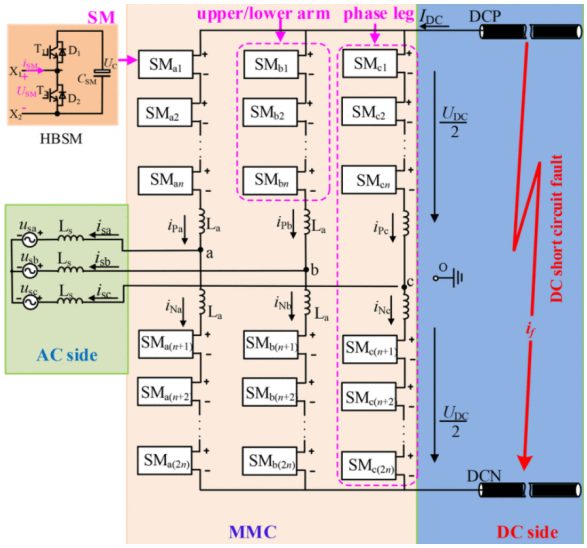

Figure 2.2: MMC circuit configuration [14]

MMC is a type of VSC with a higher number of sub-modules connected in series, the basic structure of MMC is shown in Figure 2.2. MMC is better than two level VSC owing to reduced harmonics, reduced slope of arm currents and lower surge currents from the stored DC capacitor compared to other VSC converters [16]. The arrangements of the IGBT's form different topologies of the sub-modules in an MMC, the mathematical model of the different topologies can be found in [17]. The HB MMC is more vulnerable to DC faults since they feed in the fault current. Thereby, many solutions came up to block the fault current by modifying the sub-module configuration topologies such as semi full-bridge, thyristors inserted sub-modules, five- level crossed sub-modules, etc. However, HB MMC and FB MMC are more popular for practical cases.

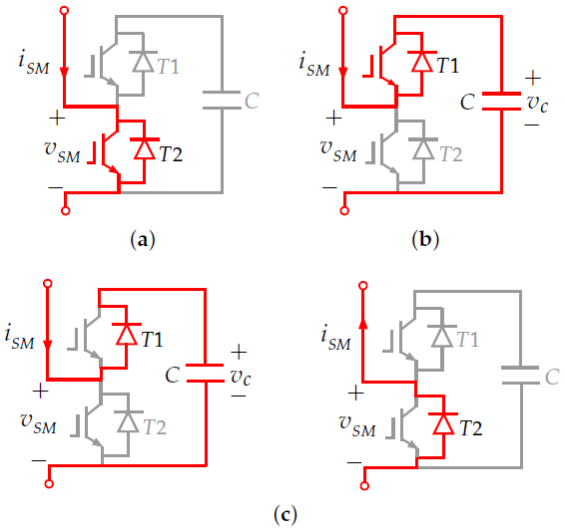

Figure 2.3: HB MMC states during a) Bypassed, b) Inserted and c) Blocked state [15]

Half bridge has three states, inserted, bypassed, and blocked states as shown in Figure 2.3. During the insertion state, the output voltage of the sub-module is equal to the capacitor voltage V_c, while during the bypassed state, the output voltage of the sub module is equal to 0.

2.3. DC faults in an MMC HVDC systems

The behavior of DC faults is different from AC faults. In this section, the stages of DC faults from the converter point of view is explained.

The maximum instantaneous fault current generated initially is given by the Equation 2.2 [18]

$$I_{sc} = 2\sqrt{2}\frac{V_a}{Z_{sc} + Z_{ac}} \tag{2.2}$$

where, V_a is the rated voltage, Z_{sc} is the short circuit impedance, and Z_{ac} is the grid side impedance.

In general, after the inception of fault, the fault current rises steeply, meanwhile the IGBTs turn off if their threshold limits are violated. The converter responses can be characterized as three steps.

- **Capacitor discharge**: The inserted sub-module's capacitance discharge current leads to a steep rise in fault current. At this stage, the upper and lower arm currents will be identical. The inserted capacitors tend to discharge until or unless they are blocked or given bypassing signal by the lower level con-

trols. Moreover, if the sub-modules are not blocked, and if the controls are not in the freeze mode, the insertion of sub-modules continues, thereby the capacitors also continues to discharge.

- **Transient stage**: The DC and AC current together contribute to the fault current. Here, the DC component is decaying current owing to the dissipation of energy stored across the arm inductors (L_{arm}). The time constant (τ_{dc}) for this stage is given by the Equation 2.3, where L_{arm} is the arm inductance and R_{arm} is the equivalent sub module resistance [19]. The AC transients represents the current flowing through the series RL circuit. The recharging of the sub-modules takes place if the AC transient component is higher than the DC transient component.

$$\tau_{\mathrm{dc}} = \frac{L_{\mathrm{arm}}}{R_{\mathrm{arm}}} \tag{2.3}$$

- **AC infeed**: During this phase, where the arm currents are zero, the fault current is injected from the AC side through the anti parallel diodes. Thereby, the converter acts as an uncontrollable rectifier. The three phase short circuit current of an AC grid system without connecting to the converter system (I_{SC}) is always less than the DC short circuit current (I_{SCDC}) by connecting the converter system. The relative difference (ΔI_{max}) is given by the Equation 2.4 [20]. Further, the relation between ΔI_{max} and the Short Circuit Ratio (SCR) is shown in Figure 2.4, as it is observed that it is inversely proportional. In addition, the load level of the system also determines the ΔI_{max}, so that when the converter is operating as a Static Synchronous Compensator (STATCOM), the short circuit current generated is very high [20].

$$\Delta I_{\mathrm{max}} = \frac{I_{SCDC} - I_{SC}}{I_{SC}} \tag{2.4}$$

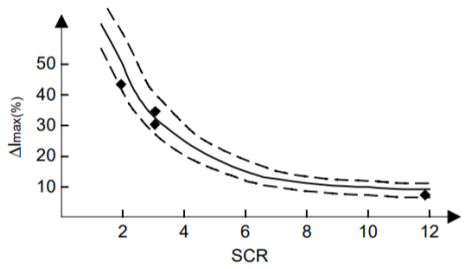

Figure 2.4: The relation between ΔI_{max} and SCR [20]

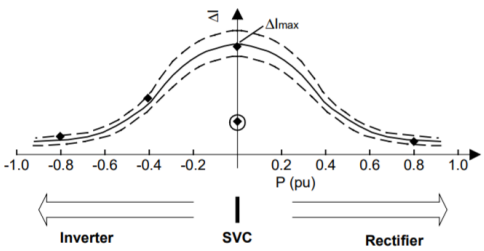

Figure 2.5: The relation between load levels and ΔI_{max} [20]

Moreover, apart from the aforementioned fault current contribution, the transmission cable also contributes to the fault current at the initial stage. However, the capacitor sub-module discharge is higher than the cable discharge.

2.4. Overview of DCCB

The requirement of DCCB is elaborated in [21–23]. A basic DCCB has a main branch, energy absorption branch, and commutation branch. The DC faults have a steep rise and high steady-state current, thus fast isolation is needed. The fast fault current identification and interruption is one main criterion while developing a DCCB. With higher fault clearing time (in the range of ms), the traveling wave also contributes towards the DC fault current transients. The wave velocity of a traveling wave is determined by the submarine cable's capacitance and inductance (Equation 2.5).

$$\mu = \frac{1}{\sqrt{LC}} \tag{2.5}$$

Here, μ is the wave velocity, L is the equivalent cable inductance, C is the equivalent cable capacitance.

The major parameters for a DCCB are the creation of counter voltage, current interruption capability, fault clearing time, and energy absorption.

The above-mentioned criteria are explained using a simple DC circuit[1] as shown in Figure 2.6 [24].

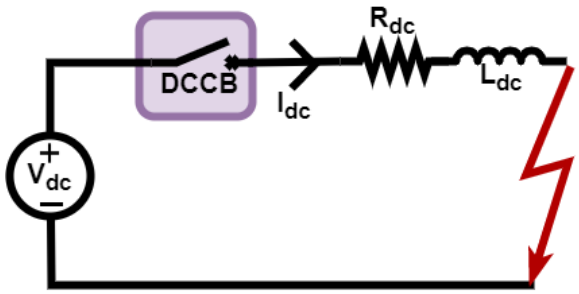

Figure 2.6: An example DC circuit [24]

- **Counter voltage**: The voltage required to demagnetize the grid and drive short circuit current zero. The counter voltage required here is given by Equation 2.6. Generally, the counter voltage is created by the Surge Arrester (SA) [24].

$$V_C = V_{dc} - V_{DCCB} = L_{dc} \cdot \frac{di_{dc}}{dt} + I_{dc} \cdot R_{dc} \tag{2.6}$$

Here, R_{dc} and L_{dc} are equivalent resistance and inductance respectively. V_c is the counter voltage, V_{dc} is the DC system voltage, V_{dccb} is the voltage generated across a breaker, and i_{dc} is the DC current flowing through the circuit.

[1] Here the R_{dc} and L_{dc} are the whole system's resistance and inductance

- **Current interruption**: The commutation branch determines the current interruption ability. The voltage to withstand across the breaker is given by the Equation 2.7, where I_{sc} is the short circuit current, which is calculated in Equation 2.8 [24].

$$V_{\text{DCCB}} = R_{dc} \cdot I_{sc} + L_{dc} \cdot \frac{dI_{sc}}{dt} \tag{2.7}$$

$$I_{sc} = \frac{V_{sc}}{R_{dc}} \cdot \left(1 - e^{\frac{t \cdot R_{dc}}{L_{dc}}}\right) \tag{2.8}$$

- **Clearance time**: The time taken to clear the fault, i.e time from the inception of fault to its interruption. Higher the switching time, higher the short circuit current. Thus quick switching is required.
- **Energy absorption**: The energy absorbed by the inductors is dissipated through the SA. The energy is dissipated is given by Equation 2.9.

$$E = \frac{1}{2} L I_{sc}^2 \tag{2.9}$$

In this thesis, there are two types of DCCB used, namely VARC DCCB and mechanical DCCB. One important point to note is that in this thesis only the simplified models are used and not the detailed model, as the thesis focuses on the MMC performance.

- **VARC breaker**: The main motive of the VARC breaker is to use the VSC for generating artificial current zero. The VARC CB uses a series resonant circuit and a VSC for the purpose of commutation. A gradually increasing high frequency current is generated till the zero crossing in the current is achieved. The detailed working, modelling, and the results are discussed in [25, 26]
- **Mechanical breaker**: The mechanical breaker used here consists of 3 branches, namely the main branch, current injection, and energy absorption. The main branch consists of high-speed switch and a residual breaker. Besides, the current injection branch consists of a switchable series LC circuit, with a precharge resistance parallel to the capacitor. Further, the SA connected in parallel to the capacitor becomes the energy absorption branch. The detailed working, modelling and technical performance of the breaker is found in [27].

2.5. Conclusion

In this chapter, the working of MMC is understood and also their fault stages. The fault response of MMC is an important part of studies, because, an section 2.2 contains both passive and active components, thereby a single equation cannot be used to determine the fault equation. Finally, the working of DCCB is elucidated and a short description of the breakers used in the thesis are discussed.

References

[1] G. Stamatiou, *Analysis of VSC-based HVDC systems*, Ph.D. thesis (2016).

[2] L. Liu, M. Popov, M. Meijden, and V. Terzija, *Optimized control of lcl-vsc converter with refined s-parameter,* IEEE Transactions on Power Delivery **PP**, 1 (2016).

[3] M. Krishnan, *Hvdc vsc technology for offshore wind farms application,* (Accessed 28 July 2020).

[4] M. Abedrabbo, W. Leterme, and D. Van Hertem, *Systematic approach to hvdc circuit breaker sizing,* IEEE Transactions on Power Delivery **35**, 288 (2020).

[5] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, *Recent advances and industrial applications of multilevel converters,* IEEE Transactions on Industrial Electronics **57**, 2553 (2010).

[6] CIGRE-B4-52, *Hvdc grid feasibility study,* (2013).

[7] wikipedia, *Hvdc cross channel,* (Accessed 26 August 2020).

[8] G. Ding, G. Tang, Z. He, and M. Ding, *New technologies of voltage source converter (vsc) for hvdc transmission system based on vsc,* in *2008 IEEE Power and Energy Society General Meeting-Conversion and Delivery of Electrical Energy in the 21st Century* (IEEE, 2008) pp. 1–8.

[9] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, *Prospects of multilevel vsc technologies for power transmission,* in *2008 IEEE/PES Transmission and Distribution Conference and Exposition* (IEEE, 2008) pp. 1–16.

[10] R. Marquardt, *Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications,* in *The 2010 International Power Electronics Conference-ECCE ASIA-* (IEEE, 2010) pp. 502–507.

[11] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, *Detailed and averaged models for a 401-level mmc–hvdc system,* IEEE Transactions on Power Delivery **27**, 1501 (2012).

[12] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, *Vsc-based hvdc power transmission systems: An overview,* IEEE Transactions on Power Electronics **24**, 592 (2009).

[13] P. S. Jones and C. C. Davidson, *Calculation of power losses for mmc-based vsc hvdc stations,* in *2013 15th European Conference on Power Electronics and Applications (EPE)* (2013) pp. 1–10.

[14] X. Yang, Y. Xue, P. Wen, and Z. Li, *Comprehensive understanding of dc pole-to-pole fault and its protection for modular multilevel converters,* High Voltage **3**, 246 (2018).

[15] R. Vidal-Albalate and J. Forner, *Modeling and enhanced control of hybrid full bridge–half bridge mmcs for hvdc grid studies,* Energies **13**, 180 (2020).

[16] R. Marquardt and A. Lesnicar, *New concept for high voltage-modular multilevel converter,* in *IEEE PESC* (2004) pp. 1–5.

[17] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, *Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters,* IEEE Journal of Emerging and Selected Topics in Power Electronics **5**, 1631 (2017).

[18] H. N. S. N. K. Sharifabadi, L. Harnefors and R. Teodorescu, *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems* (Newark: Wiley, 2016).

[19] W. Leterme, J. Beerten, and D. Van Hertem, *Equivalent circuit for half-bridge mmc dc fault current contribution,* in *2016 IEEE International Energy Conference (ENERGYCON)* (2016) pp. 1–6.

[20] Y. Jiang-Hafner, M. Hyttinen, and B. Paajarvi, *On the short circuit current contribution of hvdc light,* in *IEEE/PES Transmission and Distribution Conference and Exhibition*, Vol. 3 (2002) pp. 1926–1932 vol.3.

[21] C. D. Barker and R. S. Whitehouse, *An alternative approach to hvdc grid protection,* in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)* (2012) pp. 1–6.

[22] C. M. Franck, *Hvdc circuit breakers: A review identifying future research needs,* IEEE Transactions on Power Delivery **26**, 998 (2011).

[23] C. Meyer, M. Kowal, and R. De Doncker, *Circuit breaker concepts for future high-power dc-applications,* (2005) pp. 860 – 866 Vol. 2.

[24] B. Geebelen, W. Leterme, and D. V. Hertem, *Analysis of dc breaker requirements for different hvdc grid protection schemes,* in *11th IET International Conference on AC and DC Power Transmission* (2015) pp. 1–7.

[25] S. Liu, M. Popov, S. S. Mirhosseini, S. Nee, T. Modeer, L. Ängquist, N. Belda, K. Koreman, and M. A. M. M. van der Meijden, *Modeling, experimental validation, and application of varc hvdc circuit breakers,* IEEE Transactions on Power Delivery **35**, 1515 (2020).

[26] L. Ängquist, A. Baudoin, T. Modeer, S. Nee, and S. Norrga, *Varc – a cost-effective ultrafast dc circuit breaker concept,* in *2018 IEEE Power Energy Society General Meeting (PESGM)* (2018) pp. 1–5.

[27] S. Liu, Z. Liu, J. D. J. Chavez, and M. Popov, *Mechanical dc circuit breaker model for real time simulations,* International Journal of Electrical Power & Energy Systems **107**, 110–119 (2019).

3

General Analysis of Faults concerning different DCCB

This chapter discusses the performance of MMC together with the VSC assisted Resonant Current (VARC) DCCB and the mechanical DCCB. Initially, the model is described, followed by the fault responses of the converter with respect to the VARC breaker and mechanical breaker are illustrated. Finally, both of the model are compared and concluded.

3.1. Network Description

The simulation model's block diagram is shown in the Figure 3.1. Initially, the onshore converters were not connected together through the 4^{th} line[1]. However, in order to improve the stability of the system, the 4^{th} cable is connected between the onshore converters. It is important to note that, the network is interconnected only in DC side of the system. In chapter 2, the basic components of an HVDC structure and their necessity are explained, thus only a short system description is given here.

From the Figure 3.1, it is seen that there are two AC grids ($3Phase$, $400\ KV$, $50\ Hz$), 2 onshore converter station , 2 offshore converter station, 2 separate wind farms ($66\ KV$, $1\ GW$) and the DCCB set up. It is important to note that, the Figure 3.1 is only single line representation. Further, both of the AC grids are strong grids, owing to the fact that power grids in Netherlands are strong and they have the short circuit power of $12\text{-}26\ GVA$. The converter transformer used here is a star delta ($\gamma - \Delta$) transformer. Further, the HB MMC are connected in bipole configuration as shown and explained in the Figure 1.3 and section 1.3 respectively. Subsequently, there are DCCB in the ends of positive and negative pole of the converter station. The measurements are made at the points after and before the

[1]The results of the 3 cable model can be seen in the Appendix A

DCCB, however, the former one is used extensively for calculation and graphs. Also, the offshore converter's metallic return pole is grounded using 0.5 Ω resistor. The fault clearance are mainly cleared by the DCCB and the isolation time varies for each breaker. The clearance time for VARC is 3 ms, whereas for mechanical breaker is 5 ms. The converter blocks the switching devices once the arm current crosses the threshold of 2.7 KA. The positive and negative pole MMC are controlled by separate controllers and moreover, the protection is based on over current, low DC voltage and low AC voltage. The positive and negative pole converters in the bipole configuration have separate but identical controls systems. The control system consist of 2 main layers, namely upper level and lower level controls. The upper level controls consist of voltage, frequency, active and reactive power controls. Whereas, the lower control system manages the circulating current, capacitor voltage and fault current control [2].

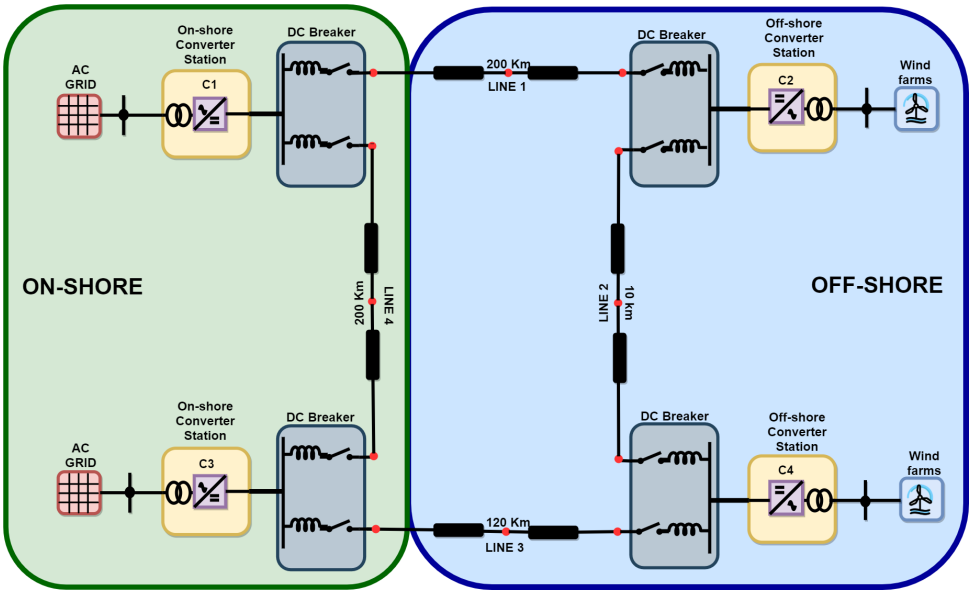

Figure 3.1: Modified Block Diagram of the network model used for the upcoming simulation

Henceforth, the onshore and offshore converter stations will be addressed as *C1 & C3 (Onshore) and C2 & C4 (Offshore)* respectively as marked in the Figure 3.1. Further, the cable connecting different converter stations are also marked in the diagram. The detailed rating and specifications of the whole network is given in the Appendix B. The faults are applied at 3 different location for each of the cable (marked in red in the Figure 3.1). For example, in the line 1, the fault near the onshore converter is at 0%, the middle of the cable is at 50%, and the other side of the cable is 100%. The similar representation will be used in the following sections.

[2]Only in case of Full bridge system

3.2. The 4th cable

Since the 4^{th} line is inserted for the stability purpose, different cable lengths are tested initially to choose a suitable submarine cable of particular length from the available options. The simulations are performed and results are tabulated in Table 3.1.

Maximum fault current values - Different cable lengths				
Type	**Cable length** (Km)	I_P (KA)	I_N (KA)	I_M (KA)
Pole to Pole Fault	200	3.7691	3.7267	0.1249
	120	4.5169	4.4593	0.1421
	100	4.5441	4.4802	0.1863
	60	4.6236	4.5532	0.205
	10	4.8825	4.7931	0.2285
	5	4.8846	4.7911	0.229

Table 3.1: The maximum fault current flowing through the cable for different cable lengths

Here, I_P is the maximum current flowing through the positive poles, I_N is the maximum current flowing through the negative and I_M is the maximum metallic return current flowing through the metallic return when a pole to pole fault is applied. From, the above table, it is evident that with reduction in cable length, there is an increase in fault current. It is because of reduction on over all impedance. Further, $200\ Km$ cable is used for further simulation results.

3.3. DC Fault analysis concerning VARC DCCB

The main objective of this section is to validate the model shown in the Figure 3.1 with a DCCB with an active MMC protection. Generally, in order to test the performance of the DCCB, the MMC protection is switched off. But, since this thesis validates the MMC performance, all the controls and protections are active. The main objective of a DCCB is to clear the DC fault before blocking. But, the MMC has an instantaneous protection based on the arm currents. If the arm currents violates the threshold value, the blocking signal is enabled to the IGBTs. Consequently, here three types of faults are applied at three different cable positions. The fault applied are pole to ground fault, pole to pole fault and double to pole to ground fault. Note

that, all the faults applied here are on the DC side only. Further, only one example is explained in each case and the other cases are shown in the Appendix C.

Before the fault application, the general equations of an MMC system during a steady state are given in Equation 3.1 for the Figure 2.2. Here, I_{Pa} is the current flowing through upper arm and phase A, I_{dc} is the DC current, and I_{Za} is the circulating current component. From the below equations, it is seen that there is a DC component always present in the arm currents. Furthermore, circulation current controller is used in order to keep the circulation current minimal.

$$\begin{aligned} i_{Pa} &= \tfrac{1}{3} I_{\mathrm{dc}} + \tfrac{1}{2} i_{sa} + i_{Za} \\ i_{Na} &= \tfrac{1}{3} I_{\mathrm{dc}} - \tfrac{1}{2} i_{sa} + i_{Za} \\ i_{sa} &= i_{Na} - i_{Pa} \end{aligned} \tag{3.1}$$

Similarly, the AC and DC voltages are given by Equation 3.2.

$$\begin{aligned} V_{Pa} &= \tfrac{V_{\mathrm{dc}}}{2} - V_a - L_{\mathrm{arm}} \tfrac{\mathrm{d}i_{Pa}}{\mathrm{d}t} - R_{\mathrm{arm}} i_{Pa} \\ V_{Na} &= \tfrac{V_{\mathrm{dc}}}{2} + V_a - L_{\mathrm{arm}} \tfrac{\mathrm{d}i_{Na}}{\mathrm{d}t} - R_{\mathrm{arm}} i_{Na} \\ V_a &= \tfrac{V_{Na} - V_{Pa}}{2} - \tfrac{L_{\mathrm{arm}}}{2} \tfrac{\mathrm{d}V_{sa}}{\mathrm{d}t} - \tfrac{R_{\mathrm{arm}}}{2} i_{sa} \\ V_{\mathrm{dc}} &= V_{Pa} + V_{Na} + 2L_{\mathrm{arm}} \tfrac{\mathrm{d}i_{Ca}}{\mathrm{d}t} + 2R_{\mathrm{arm}} i_{Ca} \end{aligned} \tag{3.2}$$

Here, V_{Pa} and V_{Na} are the upper and lower arm's phase A voltages. Further, V_{dc} is the rated DC voltage of the system. V_a is the phase voltage. Also, L_{arm} and R_{arm} are the arm inductance and resistance respectively.

3.3.1. Pole to ground Fault

Fault Description : Here, the fault is applied at cable 1 (cable connecting the converter station C1 and C2) at $1.6s$ and the fault is applied at the beginning of the cable ($0KM$). The DC inductance is kept as $30mH$.

This is the most common type of fault, and since it is a bi-pole system, it can have both positive pole to ground fault and negative pole to ground fault. However, here only the positive pole to ground fault is shown owing to the reason that both of them have a similar kind of behavior. Moreover, always the positive fault have higher fault current magnitude than the negative fault.

The pole to ground fault response is shown in the Figure 3.2, 3.3, C.1, C.2, C.3 and C.4. It is seen that the voltage drops immediately after the short at the affected pole, however healthy pole remains unaffected from the major disturbances.

When the fault is near the onshore converter as shown in Figure 3.2 and 3.3, the line 1 converters see a high current flowing through the system *(C1 & C2)*. After the inception of the fault, the DCCB detects and clears the fault by permanently disconnecting the faulty cable. Afterwards, the voltage of the converters stabilize

for a new voltage of *550 KV*. Since, the system is interconnected, after the disconnection of cable 1, the generated power immediately goes through cable 4 and cable 2 to converter 3 and 4 respectively. Thus, there is an increase in current up to $1.5\ KA$ after the fault clearance at cable 1 and later the new nominal currents are regulated by the upper level controllers.

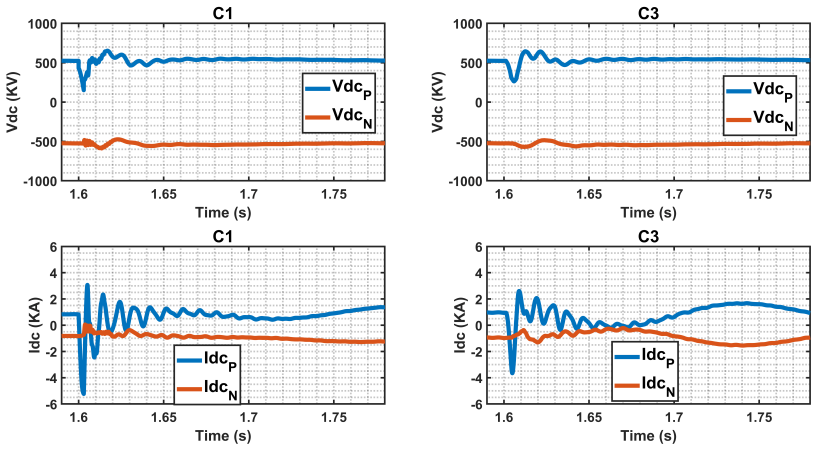

Figure 3.2: Voltage and current plots for onshore converters (C1 & C3) for pole to ground fault 0%

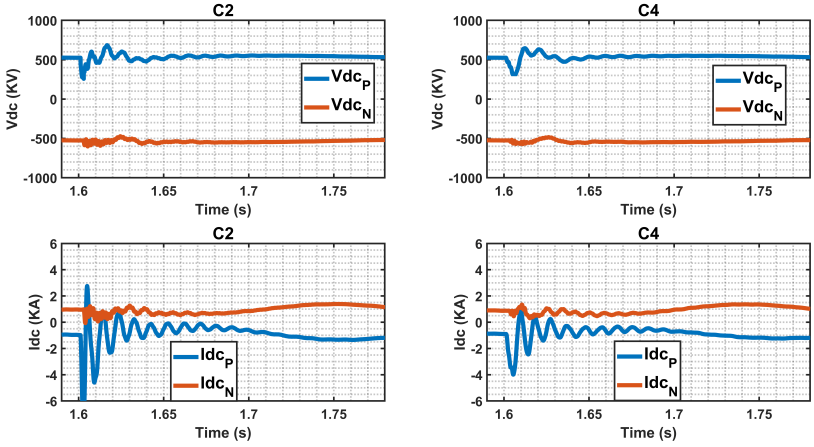

Figure 3.3: Voltage and current plots for Offshore converters (C2 & C4) for Pole to ground fault 0%

3.3.2. Pole to Pole Fault

Pole to Pole fault is more severe than pole to ground fault. The dynamics of pole to pole fault in an HVDC system are explained in the [1].

Fault Description : Here, the fault is applied at cable 1 (cable connecting the converter station C1 and C2) at $1.6s$ and the fault is applied at the start of the cable ($0KM$, near the converter station C1). The DC inductance is kept as $30mH$.

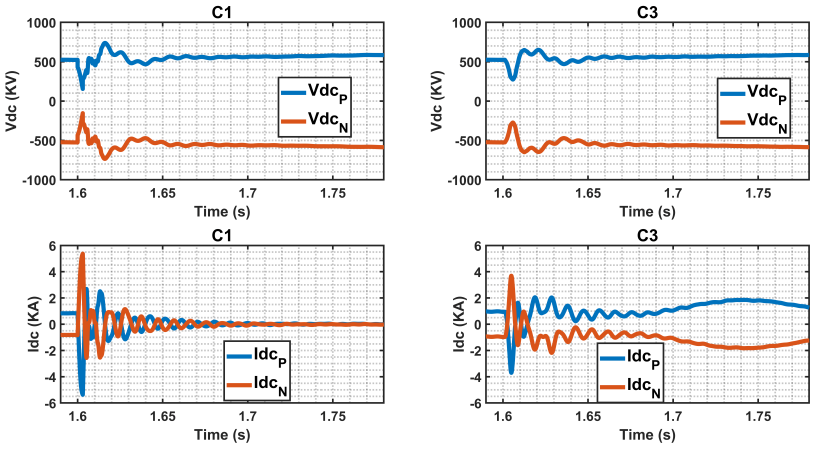

Figure 3.4: Voltage and current plots for Onshore converters (C1 & C3) for pole to pole fault 0%

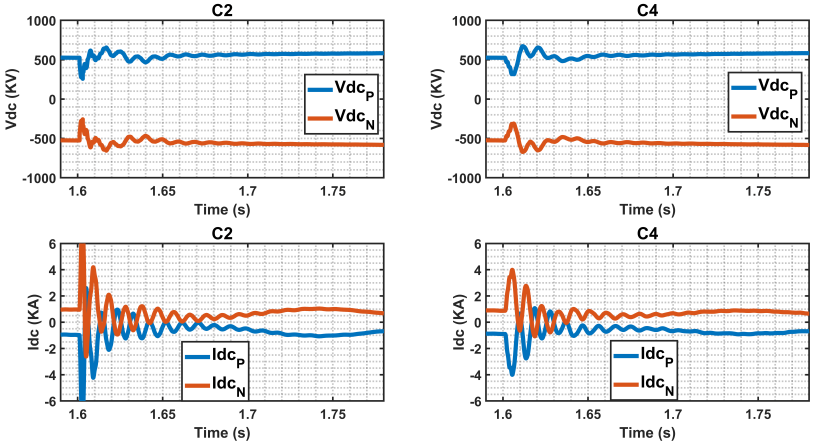

Figure 3.5: Voltage and current plots for Offshore converters (C2 & C4) for pole to pole fault 0%

The converter voltages and current plots are shown in Figure 3.4, 3.5, C.5, C.6, C.7 and C.8. In the case of pole to pole fault 0%, it is seen that the converter 1 is blocked in the Figure 3.4. It can be seen that the converter current reaching zero during the process of fault clearance. Thereby, here the MMC is blocked even before the fault is cleared due to the violation in arm current limits. The detailed explanation of violation in arm current limits is explained in subsection 4.1.2. Therefore, here the purpose of DCCB is not realized. Also, when the cable 1 is disconnected and the converter 1 is blocked, the AC grid 1 and the converter 3 see a lower impedance system. This is because the diode's equivalent resistance is lower than that of IGBT's.

3.3.3. Double pole to ground Fault

Double pole to ground fault is similar to pole to pole fault, but have higher magnitude of fault current flowing through the system. It is one of the rarest, as well as worst case scenario. Moreover, the blocking of the converters are similar to pole to pole fault.

Fault Description : Here, the fault is applied at cable 1 (cable connecting the converter station C1 and C2) and the fault is applied at the end of the cable ($200KM$, near the converter station C2). The DC inductance is kept as $30mH$.

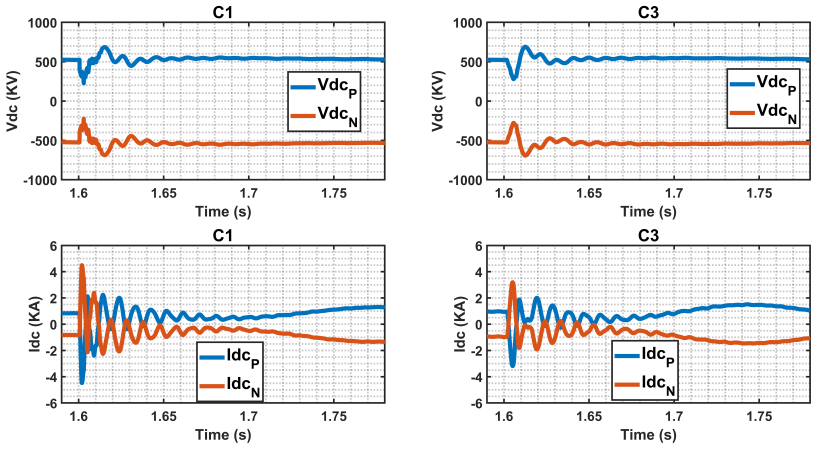

Figure 3.6: Voltage and current plots for Onshore converters (C1 & C3) for double pole to ground fault 100%

The results of above mentioned fault description is shown in Figure 3.6 and 3.7. The other results are shown in Appendix C. It is seen that, when a fault is applied, the voltage drops and simultaneously, the current rises. Later, the breaker open to clear the fault. Also, when a double pole to ground fault is applied near the offshore side of the cable 1 (100%), there is no blocking observed. Similarly, even when a pole to pole fault is applied at the same position, there is no blocking observed. On the other hand, it is interesting to note that, when pole to pole fault or double pole

to ground fault is applied at the onshore side of the cable 1 (0%), the converter 1 is blocked. This is because of the different Short Circuit Ratio (SCR)s of the grid side and the wind farm side. This is further explained in chapter 4.

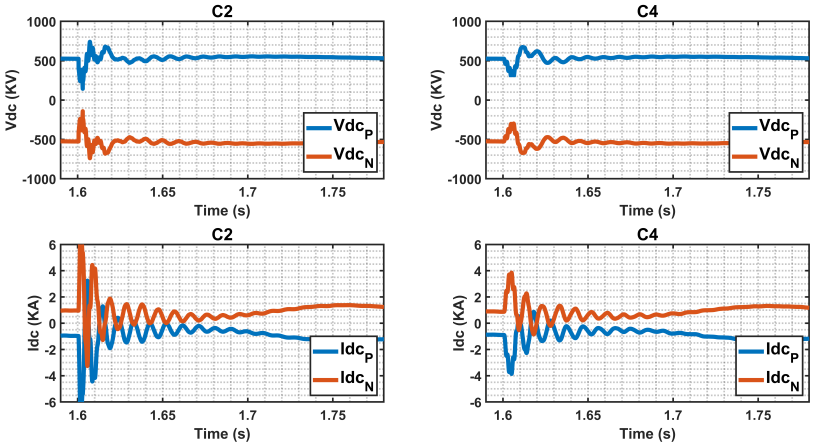

Figure 3.7: Voltage and current plots for Offshore converters (C2 & C4) for double pole to ground fault 100%

The maximum current generated in each of the pole for different cases are shown in Table 3.2. It is important to note that, the L_{dc} has been changed to $40mH$, in order to control the fault current flowing through the converter system. Further, I_p means positive pole current, I_n is negative pole current and I_m is metallic return current. Moreover, in the table, only the maximum current flowing, including all the four converters are shown.

3.4. DC faults w.r.t mechanical DCCB

Mechanical breaker uses LC path as an injection circuit in order to create the current zero. The major advantages of mechanical breakers are, simple in construction, less number of components, and less complexity. However, one main disadvantage of the mechanical breaker system is, time of operation is high. As mentioned earlier, the mechanical breaker takes $5ms$ in order to clear the fault. During this time, the fault current rises, there by allowing a higher amount of fault current to flow in the power system.

3.4.1. Pole to pole fault

Since, the fault analysis is similar to VARC breaker fault analysis. An example plot of pole to pole fault at middle of the cable 1 is represented here.

Fault Description: Here, the fault is applied at cable 1 (cable connecting the converter station C1 and C2) and the fault is applied at the middle of the cable ($100KM$, near the converter station C2). The DC inductance is kept as $80mH$.

It is seen that, while using a mechanical breaker, both the onshore converters gets disconnected from the system (Figure 3.9). Meanwhile, the offshore converters starts operating in the stand alone rectification mode, as shown in the Figure 3.8. The remaining voltage and current plots for pole to pole fault in the mechanical breaker operations are shown in the Appendix C.

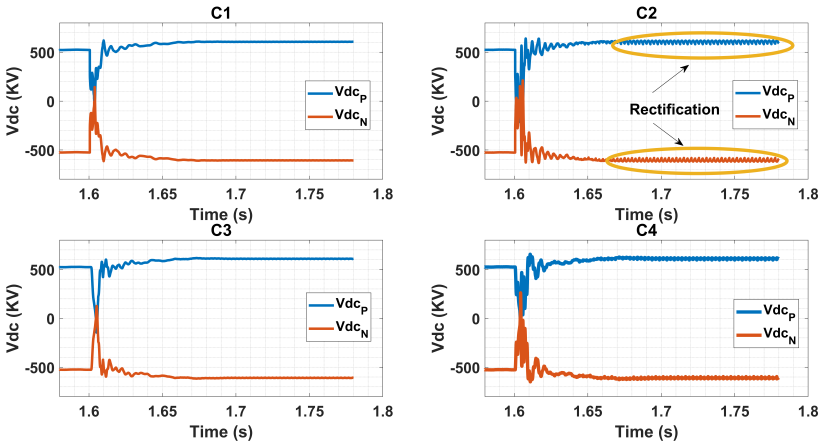

Figure 3.8: Voltage plots for all converters pole to pole fault 50%

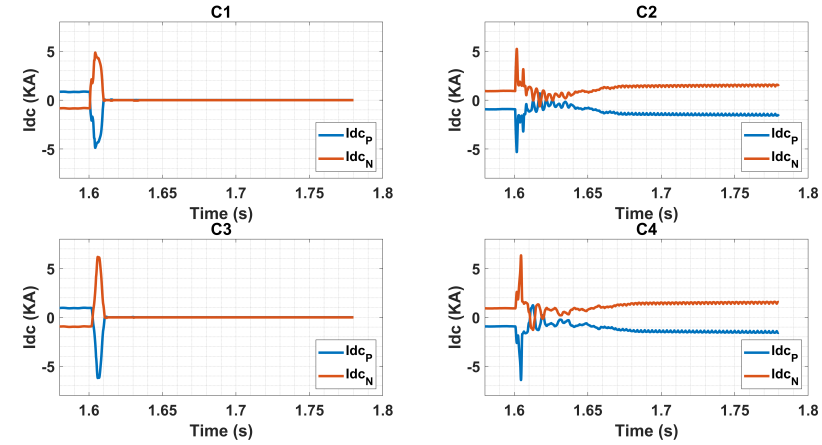

Figure 3.9: Current plots for all converters pole to pole fault fault 50%

Here, the line inductance used is $80\ mH$, it is seen that the MMC gets blocked. Thus, the inductance of the inductor is restricted to further increase in order to make the DCCB reasonable.

3.5. Comparison of MMC's performance w.r.t Mechanical and VARC Breaker

On the whole, the performance of VARC DCCB and the mechanical DCCB are discussed here. The rise in converter current (I_{dc}) while using a mechanical breaker is higher than the VARC breaker. It is seen that, with the mechanical breaker, MMC blocks the converter in all the cases, whereas with the VARC breaker, MMC blocks only in certain cases. The current flowing through the VARC and mechanical breaker is compared in the Figure 3.10. Here, the L_{dc} for both the mechanical and VARC breaker are $40mH$. From the figure, it is seen that, the fault current in mechanical breaker is always higher than the VARC breaker.

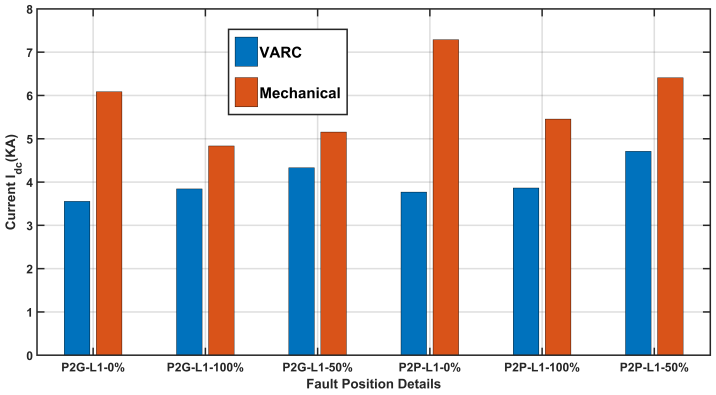

Figure 3.10: Maximum current comparison for different types of fault between the VARC and mechanical breaker

To compare the performance of VARC and mechanical breaker, a pole to pole fault at the middle of the cable is applied. Beside, here the L_{dc} for VARC breaker is changed to $30\ mH$, whereas for mechanical breaker $L_{dc} = 80\ mH$. In the Figure 3.11, it is seen that with VARC breaker, the voltage wave comeback to stability, whereas, with the mechanical breaker, V_{dc} experiences lot of oscillation and later goes to rectification mode as shown in the Figure C.14. Moreover, the initial dip in VARC breaker is around $80\ KV$, whereas for mechanical breaker it is $280\ KV$.

Similarly, when the current plots of the converters are compared, as seen in the Figure 3.12,the converter current for the system using VARC breaker comes to stability earlier than the mechanical breaker. The purple line in the figure indicates the opening of the breaker. One important observation to be made is, the magnitude of fault current in the converter produced by using a VARC breaker is higher than the mechanical breaker. This is attributed to the different inductance value chosen as mentioned. The oscillations in the converter current are quickly damped in the case of VARC than the mechanical breaker.

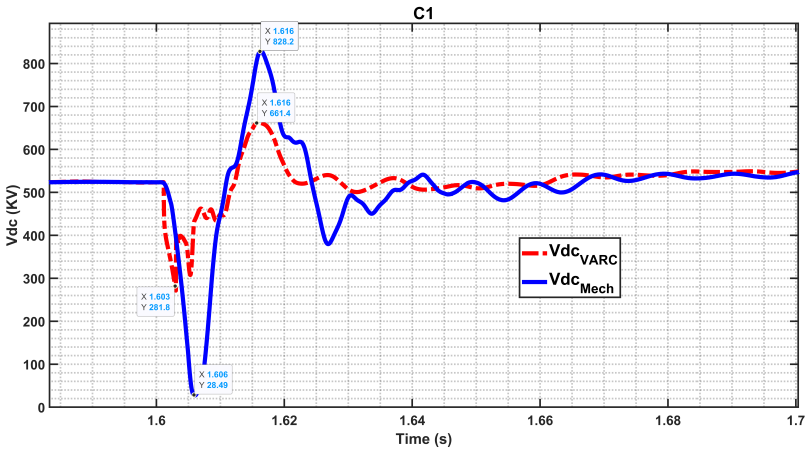

Figure 3.11: Voltage comparison between VARC and mechanical breaker, for a pole to pole fault.

Further, there are different slopes observed in the mechanical breaker current. From a converter point of view, the fault is sustaining in the system more than the expected time, thus the blocking action takes place. During the blocking of the converter, the diodes switches after particular time, there by the total impedance of the circuit keeps on changing. Once the converter gets blocked, there are different stages of circuit formation. That is why, in an HVDC system, the fault current cannot be given by a single equation. If the converter is blocked, the immediate stage is freewheeling, this stage continues till one of the arm currents reaches zero. The equation of this state is explained by Equation 3.3 [2].

$$I_{freewheeling}(t) = I_{02}e^{-\frac{R_{Equ_9}}{L_{Equ}(t-t_B)}} + I_{TW}(V_{cab}, t)$$
$$R_{Equ} = \frac{2R_{arm}}{3} \tag{3.3}$$

Here, $I_{freewheeling}$ is the fault current generated at this phase, and I_{02} is the decaying fault current (stage 2 current) and I_{TW} is the travelling wave component and R_{arm} is the arm resistance.

Further, after this three diode switching circuit formation takes place, where three conductor arm starts conducting and the fault current defined at this stage and, ends only at the next switching event. The DC fault current at this stage is given by Equation 3.4.

$$I_{DC3stage}(t) = \frac{\sqrt{3}\left|\hat{V}_{LL}\right|}{L_T\omega_{ac}}\left[1 - \cos\left(\omega_{ac}t + \theta_C\right)\right] + I_{0C} \tag{3.4}$$

$$L_T = 2L_{dc} + \frac{3}{2}\left(L_a + L'_g\right) \tag{3.5}$$

Here, the V_{LL} is the line to line voltage of the converter, θ_C is the conduction angle, L_g is the equivalent inductance of the star transformation to the AC side [3].

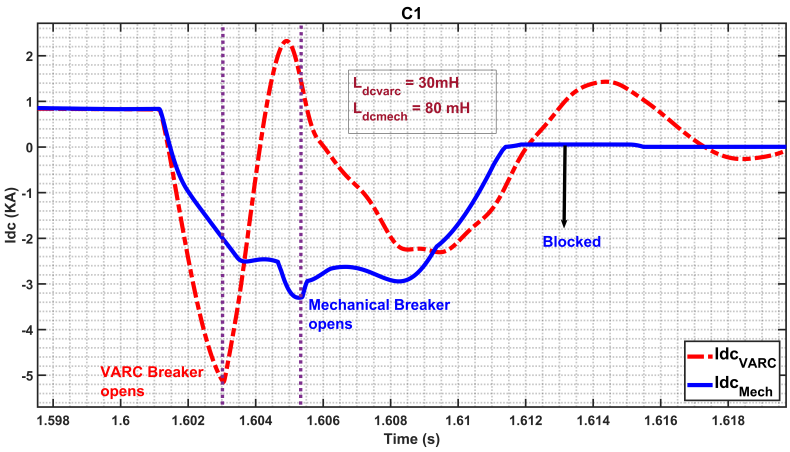

Figure 3.12: Converter current comparison between the VARC and mechanical breaker for a pole to pole fault

3.6. Conclusion

To conclude, this chapter discussed the response of MMC and the DCCB. Further, the performance of VARC breaker and mechanical DCCB is discussed with respect to MMC. Finally, the comparison between the breakers are illustrated, it is seen that VARC breaker performs better with respect to MMC's aspect of protection of MMC. Eventhough, the VARC breaker does not protect the MMC at all the times with $L_{dc} = 30mH$, as seen from Table 3.2, it performs better than the mechanical breaker. Therefore, it requires slight modification in order to coordinate it with the MMC protection. The analysis and coordination are seen in the chapter 4.

Fault Current Max values - VARC Breaker						
Type	**Line**	**Location**	**I_P**	**I_N**	**I_M**	**Blocking STATUS**
Pole to Pole Fault	L1	0%	3.7691	3.7267	0.1249	C1
Pole to Pole Fault	L1	50%	4.7097	4.6698	0.1739	No blocking
Pole to Pole Fault	L1	100%	3.8636	3.8108	0.1731	No blocking
Positve Pole to Ground Fault	L1	0%	3.5541	1.3061	3.1824	No blocking
Positve Pole to Ground Fault	L1	50%	4.3311	2.9513	2.8301	C2 Positive Pole MMC
Positve Pole to Ground Fault	L1	100%	3.8415	1.2631	3.051	No Blocking
Negative Pole to Ground Fault	L1	0%	1.3461	3.5355	3.122	No blocking
Negative Pole to Ground Fault	L1	50%	2.9417	4.3216	2.6912	C2 Negative Pole MMC
Negative Pole to Ground Fault	L1	100%	1.2883	3.8069	2.9105	No Blocking
Pole to Pole to ground Fault	L1	0%	4.754	4.703	0.1658	C1
Pole to pole to ground Fault	L1	50%	4.6825	4.6739	0.1475	No blocking
Pole to pole to ground Fault	L1	100%	3.8429	3.8211	0.1572	No blocking
Pole to Pole Fault	L2	0%	3.9967	3.9529	0.1165	No blocking
Pole to Pole Fault	L2	50%	4.0369	3.9926	0.1175	No blocking
Pole to Pole Fault	L2	100%	4.0882	4.042	0.1182	No blocking
Positve Pole to Ground Fault	L2	0%	3.8451	1.0763	1.6907	No blocking
Positve Pole to Ground Fault	L2	50%	3.8887	1.0703	1.6996	No blocking
Positve Pole to Ground Fault	L2	100%	3.9345	1.0687	1.7148	No blocking
Negative Pole to Ground Fault	L2	0%	1.0928	3.8117	1.5565	No blocking
Negative Pole to Ground Fault	L2	50%	1.087	3.851	1.5647	No blocking
Negative Pole to Ground Fault	L2	100%	1.0855	3.9011	1.5819	No blocking
Pole to pole to ground Fault	L2	0%	3.9842	3.959	0.112	No blocking
Pole to pole to ground Fault	L2	50%	4.0253	3.9994	0.1136	No blocking
Pole to pole to ground Fault	L2	100%	4.075	4.0491	0.1142	No blocking

Table 3.2: The maximum fault values for different cases using VARC breaker

Fault Current Max values - Mechanical Breaker						
Type	**Line**	**Location**	I_P	I_N	I_M	**Blocking**
Pole to Pole Fault	L1	0%	7.2876	7.2611	2.4486	C1 C3, C2 one pole
Pole to Pole Fault	L1	50%	6.4081	6.3342	0.2813	C1 C3
Pole to Pole Fault	L1	100%	5.4537	5.3866	0.4267	C1 C3
Positve Pole to Ground Fault	L1	0%	6.0854	3.1789	12.1116	C2 Positive Pole, C1
Positve Pole to Ground Fault	L1	50%	5.1541	3.6796	12.1271	C2 Positive Pole
Positve Pole to Ground Fault	L1	100%	4.8341	3.7792	12.621	C2 Positive Pole, C1
Negative Pole to Ground Fault	L1	0%	3.0084	5.5861	12.3731	C2 Negative Pole, C1
Negative Pole to Ground Fault	L1	50%	3.8157	4.9494	12.4431	C2 Negative Pole
Negative Pole to Ground Fault	L1	100%	3.4495	4.6704	12.134	C2 Negative Pole, C1
Pole to pole to ground Fault	L1	0%	8.74512	7.98721	3.1456	C1 C3, C2 one pole
Pole to pole to ground Fault	L1	50%	7.04891	7.60104	0.3751	C1 C3
Pole to pole to ground Fault	L1	100%	6.4771	5.92526	0.4896	C1 C3

Table 3.3: Maximum currents generated in MMC using a mechanical breaker

References

[1] X. Yang, Y. Xue, P. Wen, and Z. Li, *Comprehensive understanding of dc pole-to-pole fault and its protection for modular multilevel converters,* High Voltage **3**, 246 (2018).

[2] O. Cwikowski, H. R. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, *Modular multilevel converter dc fault protection,* IEEE Transactions on Power Delivery **33**, 291 (2018).

[3] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, *Operating dc circuit breakers with mmc,* IEEE Transactions on Power Delivery **33**, 260 (2018).

4

Analysis and Coordination of MMC and DCCB

Initially, the MMC's response is analysed, subsequently, the effect of capacitor discharge and arm currents are elaborated. In addition, the effect of the converter inductance, DC inductance, and inductance position are illustrated. Finally the chapter briefs on the coordination concepts and ends with a summary of the results.

4.1. Analysis of MMC's response

The stages of converter faults were explained in the section 2.3. The stages of fault as explained in the section 2.3 is shown here in the Figure 4.2.

4.1.1. Analysis of capacitor discharge

As mentioned earlier, the capacitor discharge is the major contribution to the steep rise in fault current. The capacitor discharge is given by the Equation 4.1 using a simple thevenin circuit [1]. Using the below equation, the initial fault current for $3ms$ is calculated as $10.33\ KA$ which is similar to the DCCB current.

$$I_{dc}(t) = (1 + k_{TW})\frac{V_{DC}}{L_{Equ}}t + I_{0A}$$
$$L_{Equ} = 2L_{dc} + \frac{2}{3}L_{arm} = 0.118H \tag{4.1}$$
$$I_{dc} = 10.33KA$$

From the Figure 4.2, it is seen that, at the initial phase there is peak discharge from the capacitors. Also, as mentioned in the Equation 3.1, there are both AC components and DC component in the arm currents of a MMC. At this stage, the AC current increases, meanwhile the DC component decreases, so at a particular point, the converter current touches zero. Since, the converter is blocked, the equivalent

resistance is reduced, as diodes have lower resistance than the IGBT. Thereby, the AC system starts to feed in the fault current. However, since the entire process is interrupted by the DC breaker in between, the significance of AC in-feed is not very high. The comparison of fault interruption in a DCCB and the converter arm is shown in the Figure 4.1.

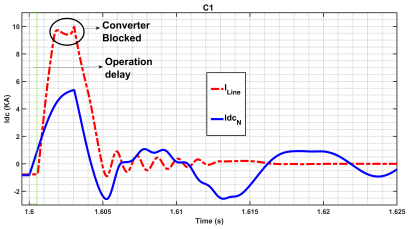

Figure 4.1: I_{Line} and Idc for pole to pole fault

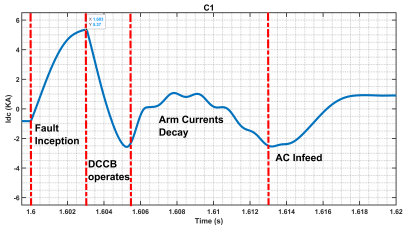

Figure 4.2: The Converter current representing the stages of the fault

4.1.2. Analysis of Arm Currents

The blocking of the converter is based on the instantaneous arm current protection. Thus, the analysis of arm current is one main criteria. The general representation of arm currents is shown in Figure 4.3. The detailed analysis of arm currents is shown in the Figure 4.4. There are six arm currents flowing in a single MMC (3 phases and two arms). If one of the arm current violates the threshold as highlighted in the figure, blocking signal is enabled. Moreover, when the arm current is positive at the moment when the converter is blocked, the inserted capacitors will continue to discharge until the arm current has reached zero, this is also highlighted in the figure.

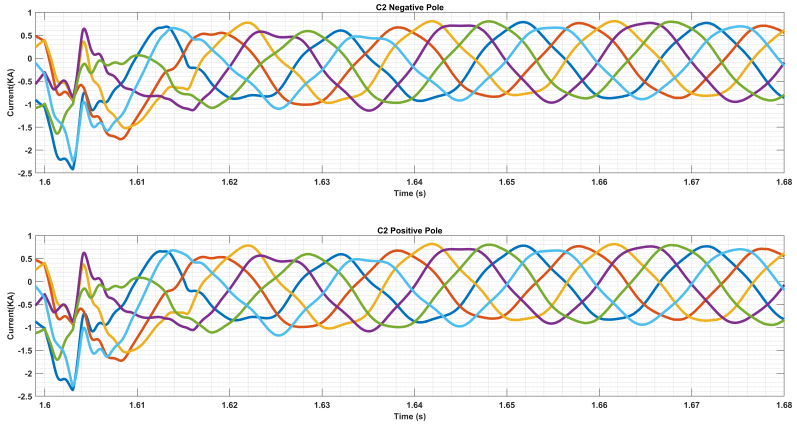

Figure 4.3: The arm currents of the converter 2(Offshore)

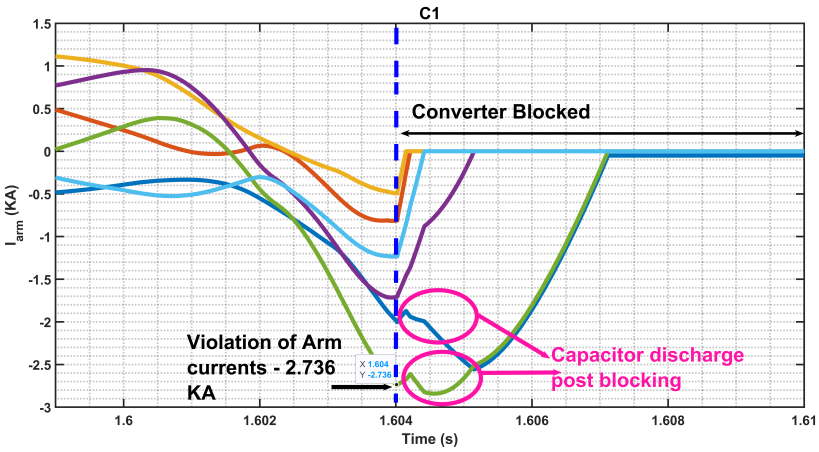

Figure 4.4: The arm currents of the converter 1 (Onshore)

4.1.3. Interval at which the Fault occurs

The MMC system have 3 types of inner protection, that enables blocking signal even if one of the protection limits are violated. The three protection are over current, under voltage and low AC voltage protection. In case of over current protection, the instantaneous arm currents are measured and continuously compared with the threshold limit. Arm current limit is set as $2.7\ KA$, this is slightly higher than twice the rated nominal DC current $2\ KA$. But by Equation 3.1, it is observed that the arm currents have AC, DC and circulating current components. Thus, the threshold set is higher than the 2 times the rated nominal current.

Since, the protection is instantaneous, there is a possibility of converter blocking at one instant and not at the other. This can be seen from the Figure 4.5. When, the fault occurs at 1.6s, both the MMCs in a bipolar system gets blocked. However, when fault is applied 1ms later, only the positive pole is blocked, meanwhile, the negative pole is not blocked. Similarly, at 1.603 and 1.604s, there is no blocking observed. Thus the blocking of the converters are purely instantaneous. On contrast, there is not a much of difference in the breaker currents and energy observed by this effect. This can be seen from Figure 4.6 and C.16. This is because, the arm currents only influence the protection of the converter by a margin, but not the rate of rise in fault current.

Further, since the arm currents are periodic in nature, there should be a periodicity in this pattern also. The periodicity repeats after every $3.3333ms$ ($1/6^{th}$ of the power frequency). This is proven from the Figure 4.7 and 4.8. There is a minute difference observed in the currents, which is due to the irrational nature of the periodicity number. Also, here the fault is applied at 1.6034s not at 1.6033333s.

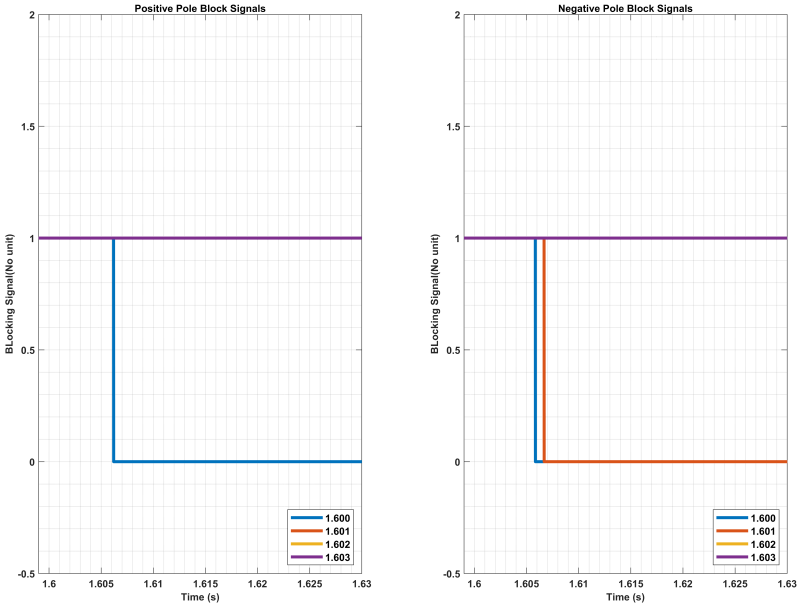

Figure 4.5: Blocking signals for different time of fault inception

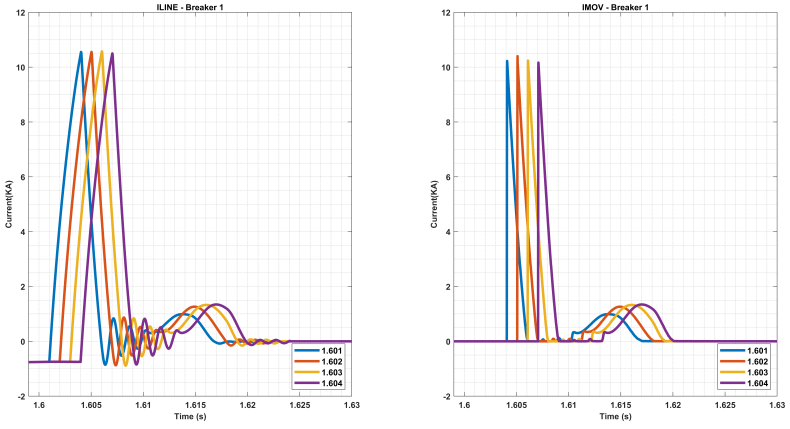

Figure 4.6: Comparison of breaker currents, when the fault occurs at different time

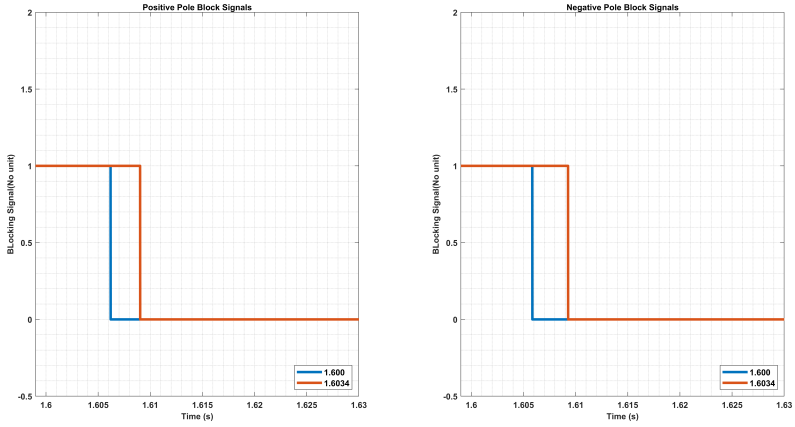

Figure 4.7: The blocking signals when the fault is applied at 1.6s and 1.6034a at the positive (left) and negative pole (right) MMC

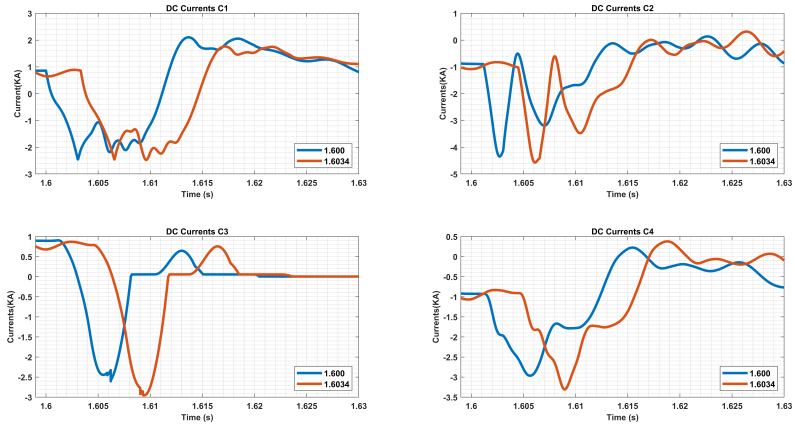

Figure 4.8: The converter currents when the fault is applied at 1.6s and 1.6034s

4.2. Effect of Inductance

The blocking of converter while there is a VARC DCCB is undesirable. One possible way to prevent this kind of situation is by increasing the DC inductance value. Basically, inductor opposes the change in current, thereby reducing the rate of rise of fault current . Therefore, there is a sufficient time given to the breaker to operate and clear the fault current.

There are two DC side inductance in the system, namely breaker inductance (L_{dc}) and converter inductance (L_{conv}). The breaker inductance is adjacent to the

breaker, however, the converter inductance is placed in the DC side of converter and it is common to the branches from a converter station. For example, in the Figure 3.1, there are two branches coming from converter station C1. This can be understood from the Figure 4.9.

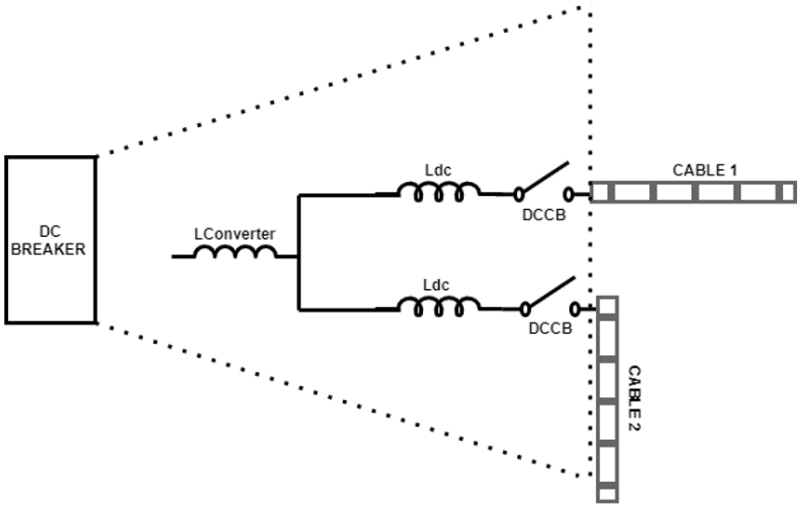

Figure 4.9: The placement of L_{conv} and L_{dc}

4.2.1. Effect of converter inductance

Here the L_{conv} is increased from 30mH - 100 mH. This range is chosen based on the literature and the stability is also taken into account. I_{Line} is the current flowing through the main switch in a DCCB, I_{mov} is the current across the SA, and E_{SA} is the energy dissipated across the SA. From the Figure 4.10, 4.11 and C.17, it is seen that, there is a minute difference in the peak current values, however, there is no much changes in the slope of the I_{Line} and I_{mov} for different L_{conv} values. Thus, the increase in L_{conv} value is not much helpful in order to avoid the blocking of the converter.

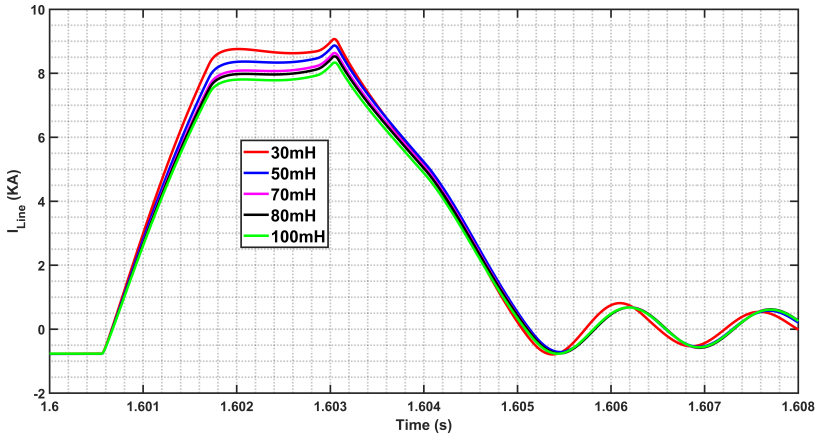

Figure 4.10: I_{Line} for different L_{conv} values

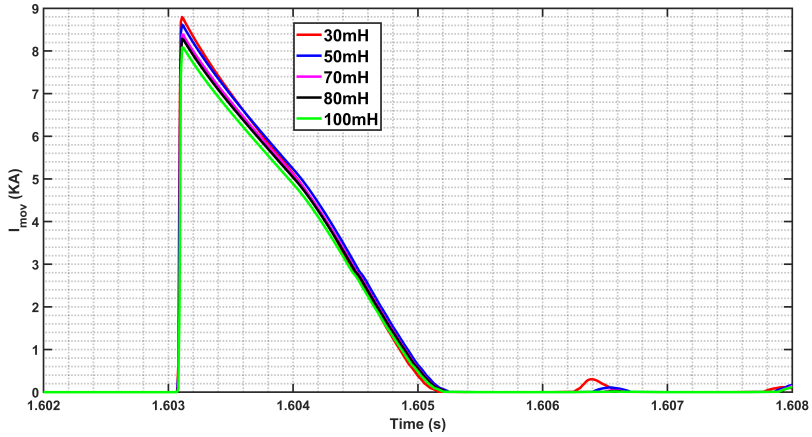

Figure 4.11: I_{mov} for different L_{conv} values

4.2.2. Effect of Breaker Inductance

As mentioned earlier, the inductance limits the rate of rise of fault current. Here, the L_{dc} is increased from $20mH$ to $200mH$. In Figure 4.12, it is evident that with increase in inductance, there is a reduction in the slope of the current. Further with increase in inductance, the oscillations present in the I_{dc} is also damped. However, from Figure C.18, it is seen that, even though the ramping of fault current is low, the time taken to dissipate the energy across the SA is larger for higher L_{dc} value. Also, the energy absorbed by the SA is higher for lower inductance. By Equation 2.9, the SA energy increases with higher value of inductance. Yet, E_{sa} decreases because,

the overall fault current is reduced and this becomes the contributing factor here. Thus, there is an reduction in energy across the SA with higher inductance. One more observation to be made is, with higher inductance values, the leakage current flowing in the circuit after the opening of the auxillary circuit breaker (also known as residual circuit breaker) is reduced or not seen. This can be seen for the L_{dc} values ranging from $120mH$ - $200mH$. The leakage current flowing after the opening of residual breaker is the hump seen after I_{line} touches zero.

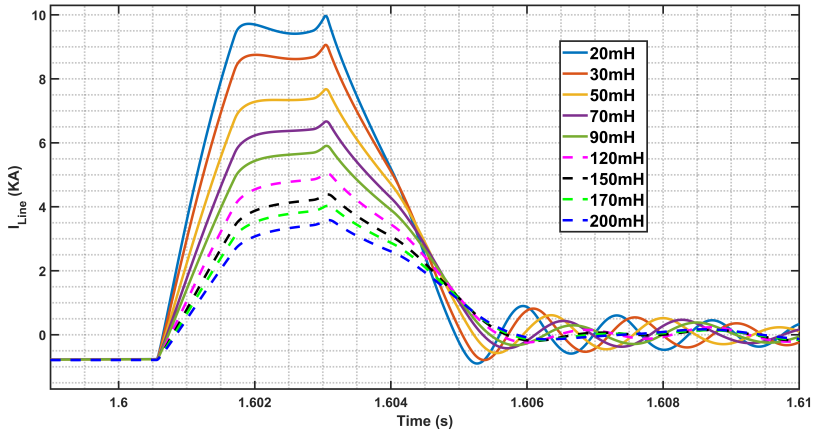

Figure 4.12: I_{Line} for different L_{dc} values

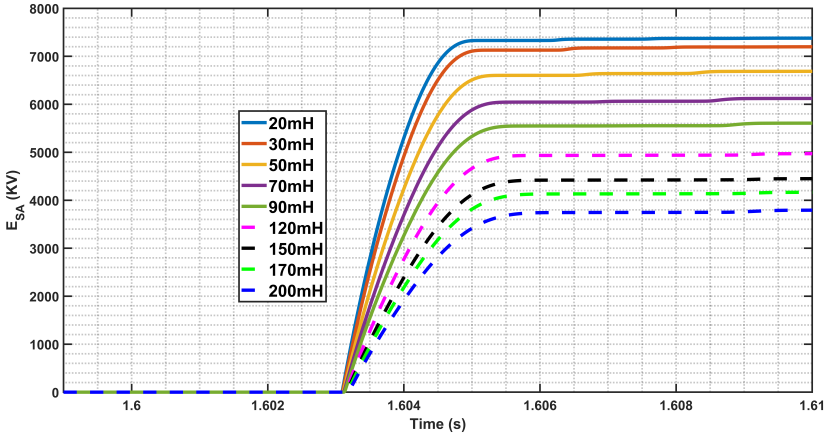

Figure 4.13: E_{SA} for different L_{dc} values

However, increasing the inductance also have its own merits and demerits. Ac-

cording to the literature, the inductance values can go upto $300\ mH$, but in practical cases, 300mH makes the DCCB size large and there is a possibility of converter interactions. Moreover, the system becomes unstable, this is illustrated in Figure C.13.

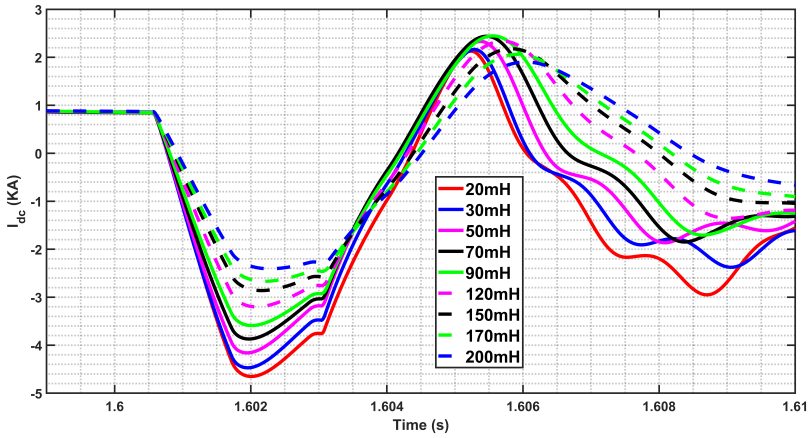

Figure 4.14: I_{dc} for different L_{dc} values

4.2.3. Effect of Breaker inductance position

In this section, the breaker and inductance positions are interchanged, in order to investigate the fault current responses. The positions of the breakers and inductors are shown in the Figure 4.15. In the first case, there is an asymmetrical arrangement of breaker and the inductor, followed by the position 2 with DCCB at the ends of the cable, and finally the inductors are place in the ends of the cable. The type 2 and type 3 have a symmetrical structure unlike type 1.

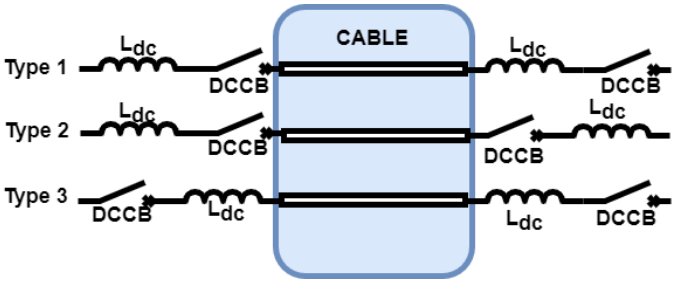

Figure 4.15: Different arrangements of L_{dc} and the breaker

The results are plotted in the Figure 4.16 and Figure 4.17. Since, the inductor play a major role in travelling waves, the cable voltages are also observed as shown in the Figure 4.16. It is seen that, there no much of difference observed in the cable voltages, as well as in the generation of fault currents. This is because, the breaker

and inductance are series connected and doesn't make a much of difference. There is a minute difference observed in breaker current after the opening of residual breaker (Figure 4.17, this can be accounted as type 1 is asymmetrical in nature of arrangements of component, whereas, type 2 and type 3 are symmetrical in nature. However, in the future cases, the simulations are performed with type 2 arrangements, in order to maintain symmetrical structure.

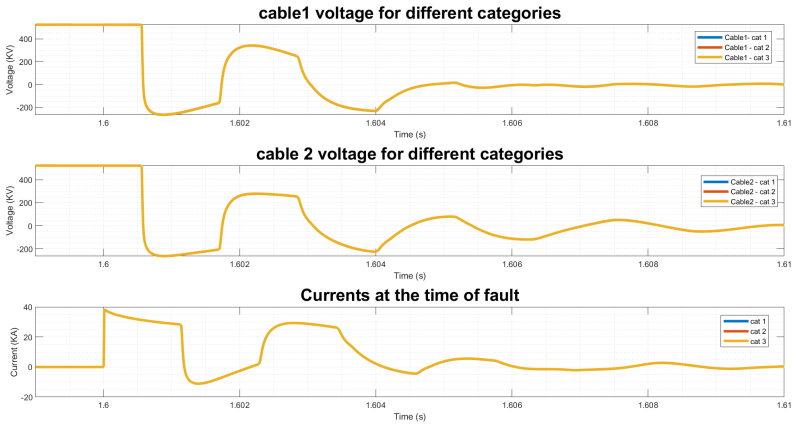

Figure 4.16: The cable voltages and total fault current for different L_{dc} positions

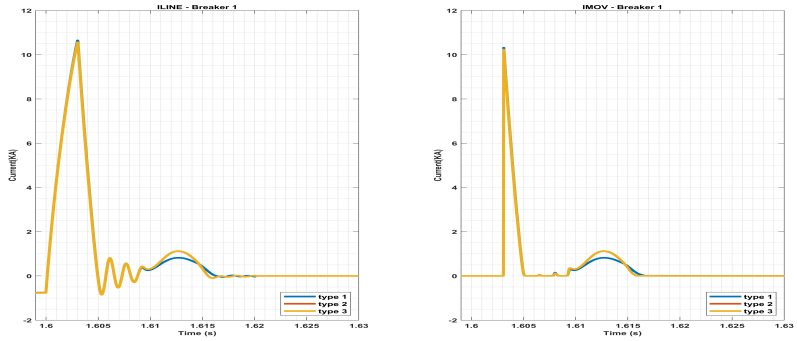

Figure 4.17: The current through the main switch for different L_{dc} positions

4.3. Coordination of MMC and Breaker

Coordination between the MMC and the DCCB is one of the most important aspect of a protection. This might be easier, if there is a proper communication between both of them. But, it can also achieved by playing with the passive devices. One

of the famous method is to increase the inductance or reduce the fault detection time. The effect of increasing the inductance is explained in the previous sections. However, the increase in inductance also increases the breaker sizing. In the below section, two ideas are implemented in order to incorporate the coordination of the system.

4.3.1. Coordination between onshore and offshore inductance

One main problem in increasing the inductance is that the sizing of the breaker also increases. Moreover, the space becomes a main constraint, when it comes to the offshore converter station. On observing the Table 3.2, it is seen that, the contribution from AC side is higher than the wind farm side. Thus, separate inductance values are chosen with respect to the short circuit capacity of the grid side and wind farm side. The relation between the SCR and the fault current are discussed in section 2.3. Also, the steady state short circuit current is given by Equation 4.2, from which it is evident that the short circuit current generated is affected by the inductance value [2].

$$I_{sc} = \frac{3}{\pi} \frac{V_{dc}}{\sqrt{\left(R_{equ}\right)^2 + \left(\omega L_{equ}\right)^2}} \qquad \begin{matrix} R_{equ} = R_{ac} + \frac{2}{3} R_{arm} \\ L_{equ} = L_{ac} + \frac{L_{arm}}{2} \end{matrix} \tag{4.2}$$

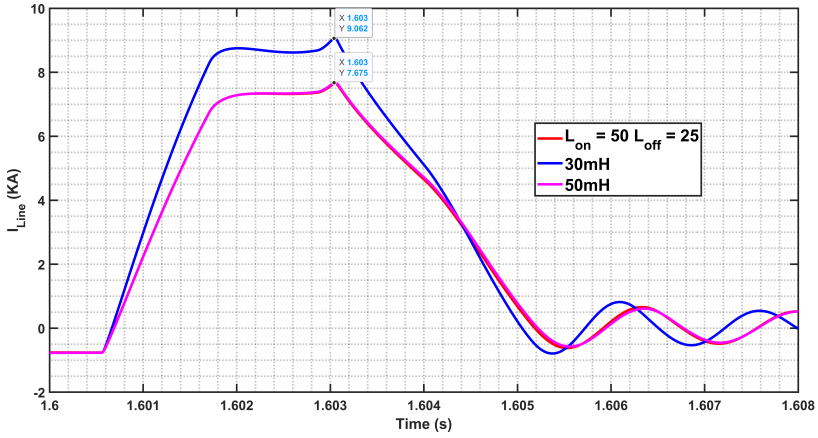

Figure 4.18: I_{line} for proposed method, $L_{dc} = 30mH$ and $L_{dc} = 50mH$

The AC inductance also plays a significant role, as seen in the equation. Further, in the simulation model, the wind farm is modelled as a controlled voltage source and also the wind farm system has its own controlling algorithm and also separate inductance and resistance. Therefore, the L_{dc} required for offshore is not same as onshore.

So, here the $L_{dconshore}$ is modified to $50mH$ and the $L_{dcoffshore}$ is kept as $25mH$. For comparison, three cases are demonstrated, first case is that both the L_{dc} are kept as $30mH$, secondly is the proposed method, third case is where both the L_{dc} are changed to $50mH$. From the Figure 4.18 and Figure 4.19, it is seen that, there is not a much of difference in the breaker current for case 2 and case 3. This is also because, the I_{line} is plotted from the onshore side, thereby only the over all impedance seen is reduced, but the onshore impedances are the same. Further, the converter currents and voltage are plotted for checking any instability issues caused due to the asymmetrical inductance values. But, no such instabilities are observed as shown in Figure 4.20 and Figure C.19. It is also seen that, with L_{on} = 50 mH, and L_{off} = 25 mH, the converter is not blocked as shown in Figure 4.19. Further, the behavior of case 2 is almost similar to case 3, without increasing the offshore inductance.

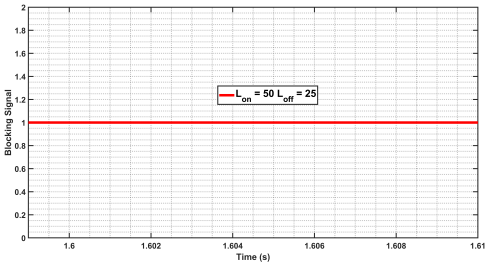

Figure 4.19: Blocking signal for L_{on} = 50mH and L_{off} = 25mH

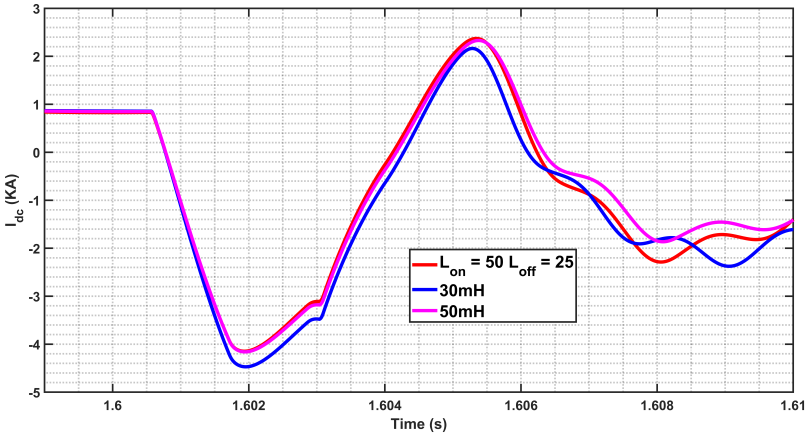

Figure 4.20: I_{dc} comparison for the different cases

4.3.2. Coordination using the arm inductance

The converter can help the DC breaker in many ways in order to reduce the fault current, since the AC infeed is in the converter side control, it can help in reducing the AC infeed during the fault. This can be done by various means, such as slowing down the voltage control, regulating the AC infeed, controlled switching of diodes, changing the sub module's topology, etc.

Here, the arm inductance value is increased in order to prevent blocking and at the same time maintain the stability of the system. Initial value of arm inductance is $42mH$. The L_{arm} can't be increased to a very higher value, since the stability of the system will be affected. Moreover, it is also an AC inductance, therefore it will have higher interactions if it is not decided properly. The main purpose of arm inductance is to eliminate the high frequency currents, that induces a difference between the lower arm and an upper arm parameters.

Before calculating arm inductance, the arm capacitance must be calculated. Since in the simulation, DC link capacitor is not enabled, it is not included in the equation [3]. Here, EP is energy power ratio, S_n is the rated power in KVA, n is the number of submodules = 175.

$$C_{\text{arm}} = \frac{E_{\text{Cmax}}}{3V_{\text{dc}}^2} = EP\frac{S_{\text{n}}}{3V_{\text{dc}}^2}C_{arm} = 14.28\mu F \tag{4.3}$$

Then L_{arm} value is calculated using Equation 4.4 [3]. Here, $h = 2.n$, m is the modulation index which is taken as 0.5 and $\omega = 2.\pi.f$.

$$L_{\text{arm}}|_{C_{\text{arm}}=C_{\text{arm}}} = \frac{1}{C_{\text{arm}}\omega^2}\frac{2\left(h^2-1\right)+m_{\text{a}}^2h^2}{8h^2\left(h^2-1\right)} \tag{4.4}$$

By the equation, it is calculated that L_{arm} = 48mH. Moreover, small percentage of increase in L_{arm} is not much significant with respect to stability, thus L_{arm} is increased from 42 mH to 60 mH and the results are observed. This variation is only verified experimentally and not through the literature. The results are plotted in the Figure 4.21, 4.23 and 4.24.

As a result, there is no blocking observed when $L_{arm} = 50mH$ as shown in the Figure 4.22. From the comparison results it is seen that, the fault current reduces with L_{arm} = 47 mH - $60\ mH$. Further, there is a overlap in the graph for the figure from $47mH$ - $60\ mH$. Thus, choosing the modified L_{arm} = 50 mH is more justifiable than preferring higher arm inductance values. Further, since the arm inductance is common to both the AC and DC side, it is important to check on the AC side performance also. Subsequently, from the graphs 4.23 (DC current of the converter) and 4.24 (ACrms current of the converter), it is concluded that, the chosen arm inductance doesn't affect the performance, rather, it only improves.

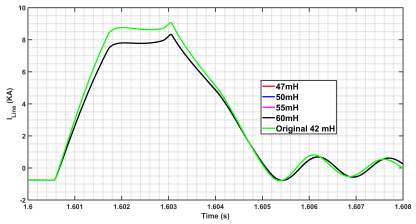

Figure 4.21: I_{line} for different L_{arm} values

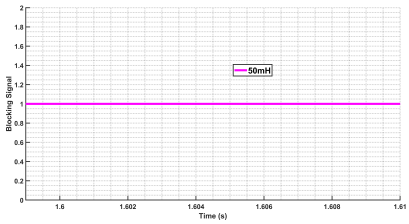

Figure 4.22: Blocking signal for L_{arm} = 50mH

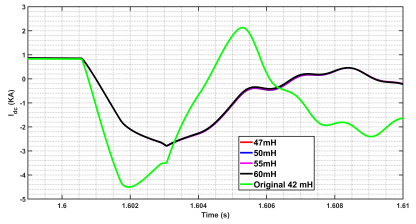

Figure 4.23: I_{dc} for different L_{arm} values

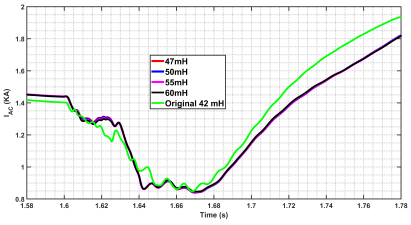

Figure 4.24: I_{ac} for different L_{arm}

4.4. Conclusion

In this chapter, the detailed analysis of the MMC stage by stage during a fault is demonstrated. Further, in order to reduce the rate of rise of fault current, the different inductance values were changed and discussed. Moreover, in order to coordinate the protection, inductance value is chosen based on the short circuit capacity of the system and the performance is evaluated. Later, the AC in feed is controlled by modifying the arm inductance, thereby coordination is achieved by modifying the passive elements.

References

[1] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, *Operating dc circuit breakers with mmc,* IEEE Transactions on Power Delivery **33**, 260 (2018).

[2] A. Wasserrab and G. Balzer, *Determination of dc short-circuit currents of mmc-hvdc converters for dc circuit breaker dimensioning,* in *11th IET International Conference on AC and DC Power Transmission* (2015) pp. 1–7.

[3] B. R. M.Zygmanowski1, *Capacitance and inductance selection of the modular multilevel converter,* (Accessed 28 July 2020).

5

Full Bridge MMC

The chapter focuses on the Full Bridge MMC (FB MMC) topology for $320\ KV$ network. Unfortunately, the $525\ KV$ full bridge network results were inconsistent with FB MMC, therefore the analysis is shifted to $320\ KV$ system. Initially, the response of FB MMC is explained, followed by the validation of the steady state performance of the FB MMC. Since, the model was initially a half bridge model, it is later converted to full bridge circuit, the evaluation of steady state becomes a necessity. Later, the response of FB MMC during a pole to pole fault is discussed. Finally, the chapter concludes with a comparison between both of them.

5.1. DC response to Full Bridge MMC

The FB MMC have two current paths, thus it is more flexible. However, it increases the cost, size and losses. But, the full bridge converter is also known as fault blocking converters, thereby doesn't require a separate DCCB. Using a DCCB and a full bridge will make the system more redundant for protection. The current path in a FB MMC is shown in the Figure 5.1.

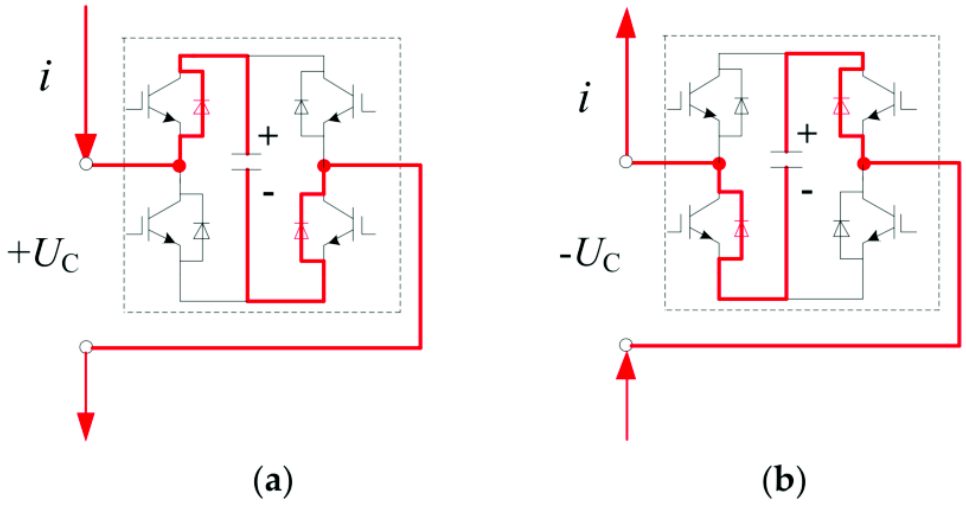

Figure 5.1: Current paths in FB MMC [1]

There are 3 stages while blocking the FB MMC during a DC fault. Initially, there is an increase in DC current. At this stage, there is no response from the controls, thereby arm currents see an increase in fault current. Consequently, the arm voltage starts to react to the DC fault, thereby it reaches to zero. Thus, there is a sudden reduction in the phase voltages, as a result the phase current also reduce to zero. Finally, since the dc-side current has reached zero, the phase currents alternate around zero instead of the $V_{dc}/2$ [2]. Moreover, the fault can be handled either by blocking or by using the controllers in a full bridge system. Further, the voltage generated at the output of a full bridge circuit is higher than the rated voltage. Due to this reason, the average cell capacitor voltage is greater than the peak line voltage. Thereby, the cell capacitors opposes the arm current. Thus, unlike HB MMC, there is no straight path for the current to flow through the switched resistances. The comparison of different fault clearance methods are explained in [3].

5.2. Steady State Analysis

The network was initially a $320\ KV$ half bridge network, which was later converted in to $320\ KV$ full bridge network for simulation purpose. Thereby, steady state analysis is important to ensure that system is without any inconsistency. Therefore, the steady state analysis is shown from *1.58s - 1.78s (0.2s)*, and it is seen from Figure 5.2, 5.3, 5.4 and 5.5 that, there is no surge or instability observed. Further, the DC voltage and current values is different from the previous chapters, $V_{dc} = 320KV$, $I_{dc} = 2KA$. Therefore, the system is said to be stable and the fault analysis is done in the next section.

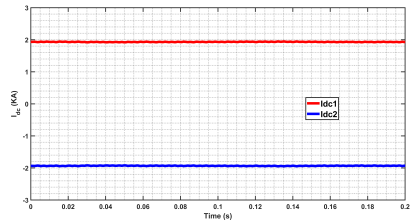

Figure 5.2: I_{dc} steady state for the FB MMC circuit

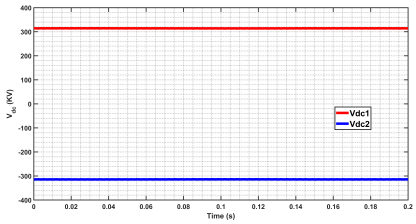

Figure 5.3: V_{dc} steady state for the FB MMC circuit

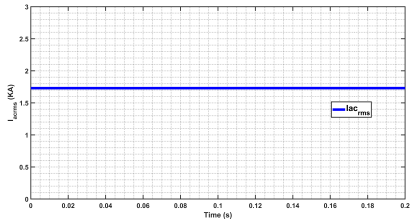

Figure 5.4: I_{acrms} steady state for the FB FB MMC circuit

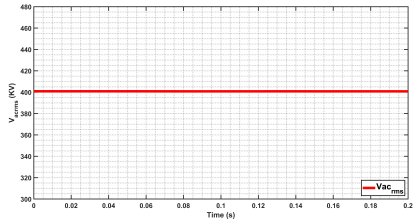

Figure 5.5: V_{acrms} steady for the FB MMC circuit

5.3. Fault Analysis

As explained in the section 5.1, the fault current increases, later owing to the reduction in arm currents and phase voltages, the current reaches zero. This is the main reason, why the FB MMC are called the fault blocking converters. The converter voltage and current plot for a FB MMC, when applied a pole to pole fault at the middle of the cable is given in Figure 5.6 and Figure 5.7. Here, the converter inductance used is $10mH$, whereas the converter inductance used in HB MMC are 30mH, apart from that, there is a breaker inductance also which is $30mH$ or above. Therefore, in a FB MMC system, there is no need of high inductance value and can be kept minimal.

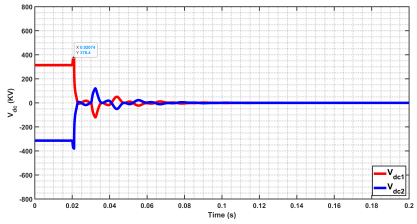

Figure 5.6: Vdc for a pole to pole fault 50%

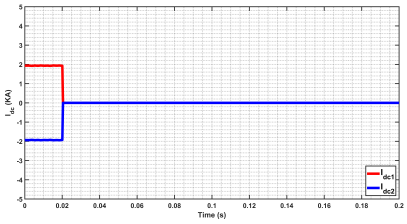

Figure 5.7: Idc for a pole to pole fault 50%

5.4. Comparison between Half bridge and full bridge MMC

The response of a HB MMC and FB MMC are discussed here. Firstly, both the systems were given a pole to pole fault at 50% and the DC side inductance were kept $10\ mH$ in order to evaluate the performance for the same parameters.

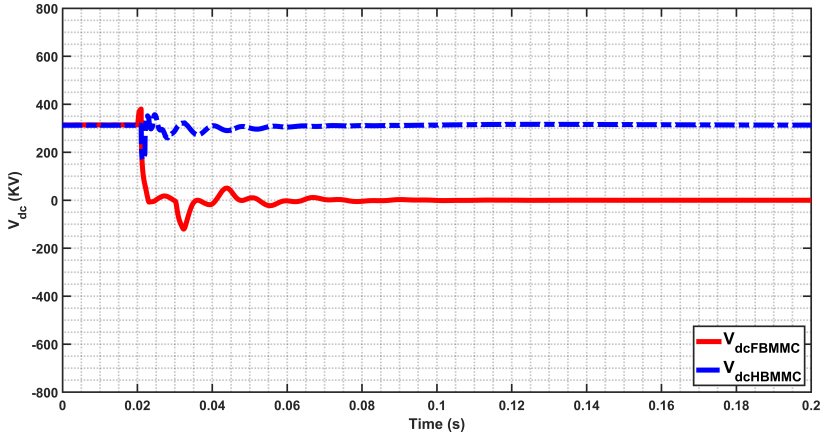

Figure 5.8: Comparison of V_{dc} between full bridge and Half bridge, when applied a pole to pole fault at middle of the cable

The voltage response is shown in Figure 5.8, and the response for first $0.06s$ is shown in 5.9. Similarly, the current responses where shown in 5.10. Here, it is important to note that the DCCB used is a simplified model of a mechanical circuit breaker. From the results it is evident that, FB MMC takes less time to block the fault than the HB MMC. Further, it is also noticed that,there is a small positive peak observed in the voltage after the inception of fault in the FB MMC, also an initial di in voltage after the blocking is enabled. Whereas, in HB MMC the converter voltage drops during the inception of the fault, later the DCCB opens and the system comes back to stability. Similarly, there is an influence of breaker operation in the HB MMC converter current (current swings), where as the FB MMC blocks and the current reaches zero.

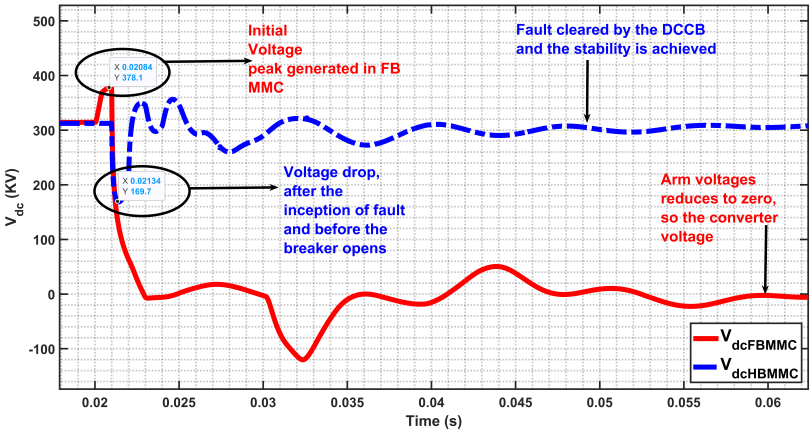

Figure 5.9: Magnified image of Figure 5.8

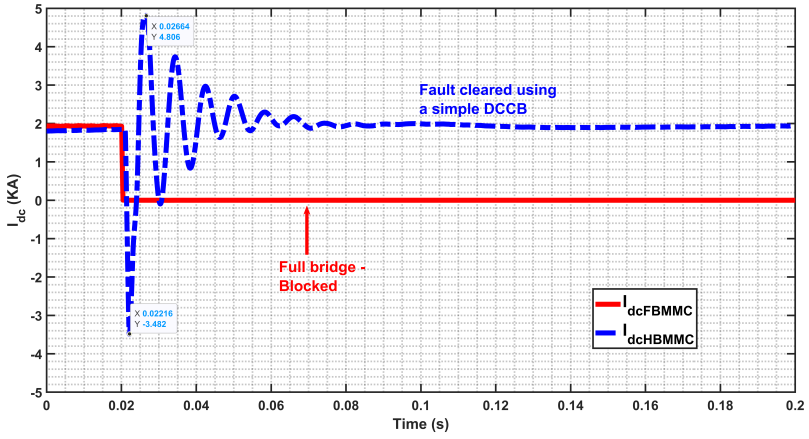

Figure 5.10: Comparison of I_{dc} between Full bridge and Half bridge for 320 KV system, when applied a pole to pole fault at middle of the cable.

5.5. Conclusion

Finally, the performance of FB MMC is first validated, consequently, fault is applied and it is compared with the HB MMC system. In the comparison, it is proven that the FB MMC blocks the fault current quickly and even before the opening of the DCCB in a HB MMC.

References

[1] Z. Xu, H. Xiao, L. Xiao, and Z. Zhang, *Dc fault analysis and clearance solutions of mmc-hvdc systems,* Energies **11**, 941 (2018).

[2] W. Leterme, P. D. Judge, J. Wylie, and T. C. Green, *Modeling of mmcs with controlled dc-side fault-blocking capability for dc protection studies,* IEEE Transactions on Power Electronics **35**, 5753 (2020).

[3] S. Wenig, M. Goertz, J. Prieto, M. Suriyah, and T. Leibfried, *Effects of dc fault clearance methods on transients in a full-bridge monopolar mmc-hvdc link,* in *2016 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia)* (2016) pp. 850–855.

6

Conclusion

6.1. Summary

The Modular Multilevel Converter (MMC) is a vital component in a system. Further, they are highly fault current intolerant owing to the current sensitive nature of the Insulated Gate Bipolar Transistor (IGBT)s. Thus the DCCB are used to protect the converters from the fault currents. There are three fault stages for a converter during a fault, during each stage, different fault current flows in the circuit. However, this addition of DCCB should be validated, so that the converter should remain protected without blocking. Also, the fault current can be divided into three stages, capacitor discharge, transient component and AC infeed. The performance of both the breakers are discussed with respect to converter voltage, current and their blocking status. Further, the coordination of DCCB and the MMC by modifying the passive elements are explained. Further, it is seen that, the contribution of fault current is more from the grid side, compared to the wind farm side. Thus, there can be separate inductance's for the DC and AC side with respect to their short circuit capacity. On the other hand, it is also seen that, the converter can help the breaker in reduction of fault current. One way is to find a suitable arm inductance, so that the converter fault feeding current is low. Moreover, a simple comparison between the fault blocking and fault feeding converters is performed.

6.2. Future work

Since, this is a field having very wide scope for more research, there are lot of works which can be continued from this research.

- In this research, only the passive components were modified in order to restrict the fault current. However, there are ways to reduce the fault current by modifying the sub-module topology.
- One more method to reduce the fault current with the help of converter is by reducing the arm currents to zero. Thus, the zero arm current leads to

significant reduction in fault current contribution. This can be done by setting the arm current controller's reference to zero during the time of fault. So, in this case, the first step of converter protection will not be blocking, rather, it would reducing the arm currents to zero.

- One more suggestion of improvement will be connecting the 4^{th} cable on the AC side, rather than the DC side.

A

3 CABLE model results

In this section, the results of 3 cable model is discussed. The model schematics is given in the Figure A.1. This model was discontinued due to the instability caused in the network. This happens when there is a pole to pole fault in the cable 1, and after the isolation of the faulty cable by the DCCB. Now, the converter 1 becomes isolated and enters rectification mode, with voltage of $320KV$. It is also, observed from Figure A.3, that the current starts to ramp up thereby causing an instability in the system.

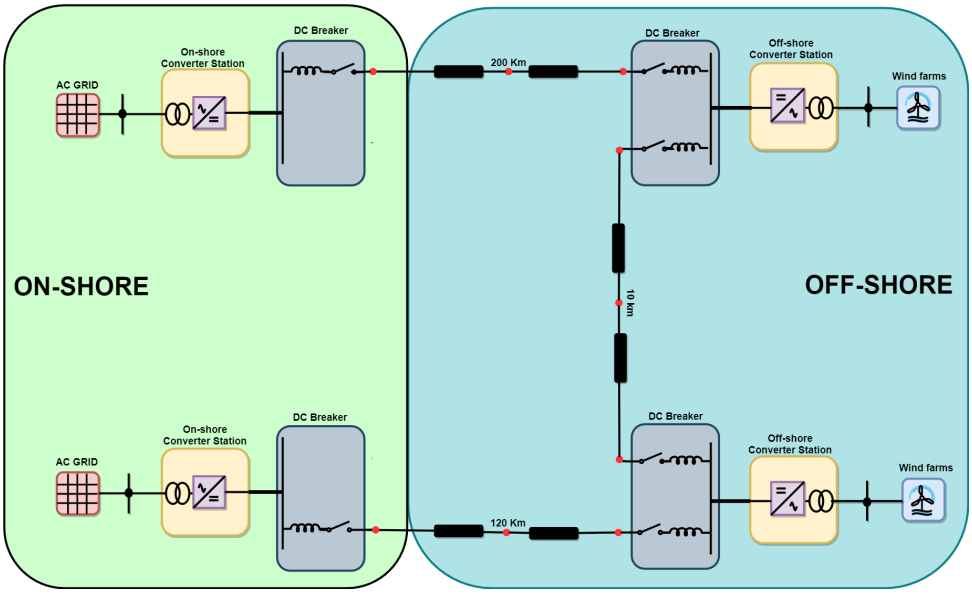

Figure A.1: Initial Block Diagram of the network model

A

A.1. Pole to Pole Fault

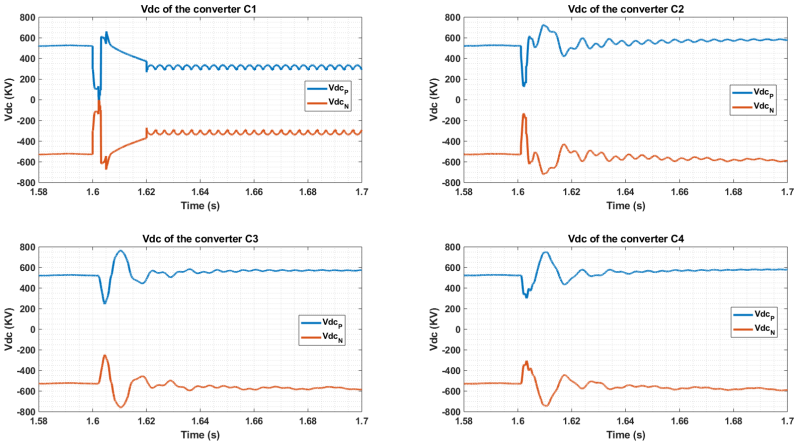

Figure A.2: Voltage plots for pole to pole fault at 0%

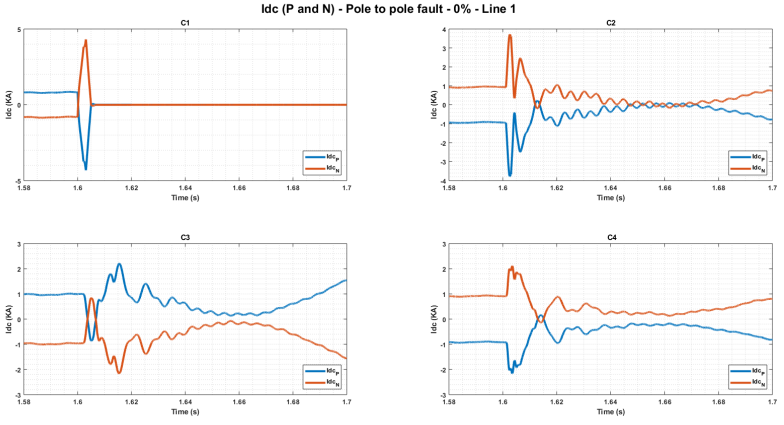

Figure A.3: Current plots for pole to pole fault at 0%

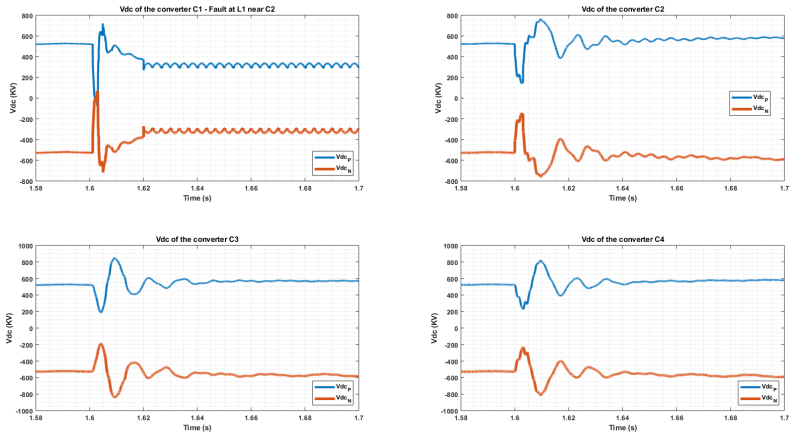

Figure A.4: Voltage plots for pole to pole fault at 100%

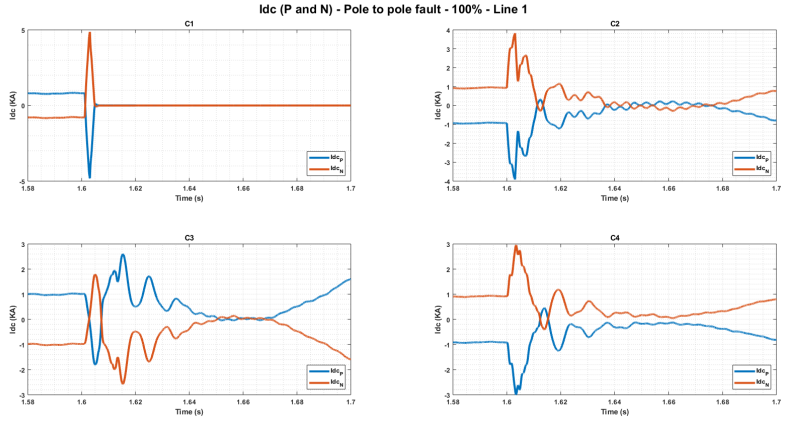

Figure A.5: Current plots for pole to pole fault at 100%

B

Model Details

The detailed characteristics and values of the AC grid, AC transformer, AC and DC breakers are given in the following tables.

AC BREAKER			
Details	**Variable**	**Value**	**Unit**
AC breaker Pre insertion resistor	R_{Prein}	100	Ω
Time to open insertion resistor	-	0.01	s
AC breaker closing time	-	40	ms
AC breaker opening time	-	100	ms

Table B.1: Details of the ACCB

AC GRID				
Details	**Value**	**Unit**		
Base MVA 3 Ph	2500	MVA		
Base Voltage	400	KV		
Frequency	50	Hz		
Voltage input time constant	0.05	s		
GRID DETAILS	**Values**			**Unit**
	Strong grid	**Moderate grid**	**Weak grid**	
Positive Sequence Resistance	0.58	3.5	4.86	Ω
Positive Sequence Reactance	5.28	31.7	44.02	Ω
Zero Sequence Resistance	0.77	4.67	6.48	Ω
Zero Sequence Reactance	7.04	42.26	58.69	Ω

Table B.2: Details of the AC grid

AC SWITCH YARD - Transformer			
Detail	**VariableName**	**Value**	**SI unit**
Rated transformer Power	S_{base}	632.5	MVA
AC grid Frequency	$freq$	50	Hz
Primary winding voltage On-shore	$Vtr_{Onshore}$	400	KV
Primary winding voltage Off-shore	$Vtr_{Offshore}$	66	KV
Secondary winding voltage	Vtr_2	250	KV
Positive sequence leakage reactance	Xt	0.18	pu
Copper losses	CuL	0.002	pu
Eddy current losses	NLL	0.0003	pu
Magnetizing current	Im	0.06	%
Air core reactance	X_{Air}	0.36	pu
Knee Voltage	V_{Knee}	1.2	pu
Star Point Inductance	$LStar$	5000	H
Start Point Resistance	$RStar$	5000	Ω
Rated voltage Surge arrester Primary	$U500A_V$	2497	KV
Rated voltage surge arrester Secondary	$U500A_T$	2225	KV

Table B.3: Details of the converter transformers

B

Half Bridge				
Details	**Variable**	**Value**	**Unit**	
Sum of Cap voltage per arm at t = 0	$SumVc0$	0	KV	**MMC Switchyard**
Cell DC capacitor	C_{dc}	15000	uF	
Switch off resistance	R_{SOff}	100000000	$M\Omega$	
Switch on resistance	R_{SOn}	0.001361	$m\Omega$	
Capacitor leakage resistance	R_{leak}	10000000	$M\Omega$	
DC Bus capacitor (Enable-1/Disable -0)	$DCCapEn$	0	Signal	
Total DC bus capacitance	$DCCap$	25	uF	
Reference Average Cap Voltage	-	1.9	KV	
Arm Inductance	L_{arm}	0.042	H	
Arm Resistance	R_{arm}	0.08	Ω	
Ground Resistance (MR grounded if closed)	R_{gnd}	0.5	Ω	
Rated Voltage of SA DC pole P and N	$U500A_{DC}$	920	KV	
Rated Voltage of SA DC pole MR	$U500A_{DCM}$	160	KV	
Rated Voltage of SA AC	$U500A_{V}$	2497	KV	
Reference Average capacitor voltage	$Vcap_{ref}$	1.9	KV	
Active Power set point	$P_{set(C1/C3)}$	-1000	MW	**Set Points**
	$P_{set(C2/C4)}$	1000	MW	
Active Power increase/decrease rates	$P_{set-rate-pu}$	1	pu/sec	
Reactive Power set point	$Q_{set(C1/C2/C3/C4)}$	0	MVAR	
Reactive Power increase/decrease rates	$Q_{set-rate-pu}$	4	pu/sec	
Rated DC voltage	Vdc_{base}	525	KV	
AC Voltage set point (L-L)	$Vac_{setOnshore}$	400	KV	
	$Vac_{setOffshore}$	66	KV	
DC voltage set point (Pole -pole)	$Vdc_{set(C1/C2/C3/C4)}$	1050	KV	
Nominal DC voltage	Vdc_{base}	1050	KV	
Nominal Active Power	P_{base}	1000	MW	
Third harmonic coefficient	$h3Mag$	0.15	-	**Regulation Parameters**
Maximum Current	$Imax$	1.1	pu	
DC Voltage Droop	Drp_{DC}	2	-	
AC Voltage droop	Drp_{AC}	0.01	-	
Frequency droop (Island mode)	$DrpF$	0	-	

Table B.4: Details of the HB MMC

C

Fault Currents

The voltage and current wave forms for different fault currents and locations are shown here. The plots for pole to ground fault an using VARC breaker at 50% and 100% are given.

C.1. Pole to Ground Fault using VARC

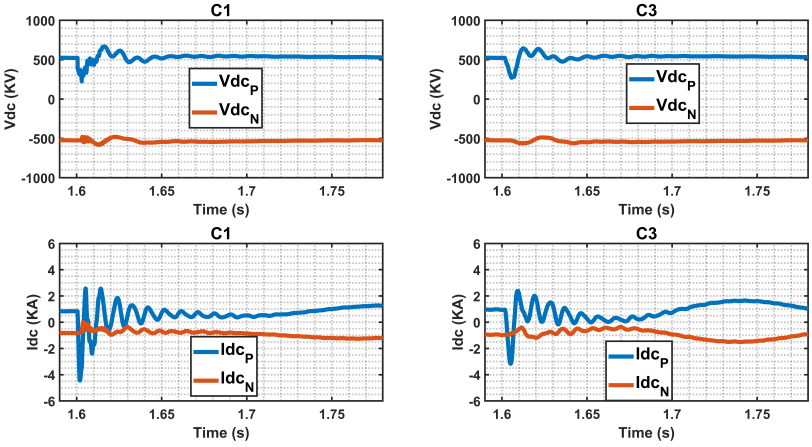

Figure C.1: Voltage and Current plots for Onshore converters (C1 & C3) for Pole to ground fault 50%

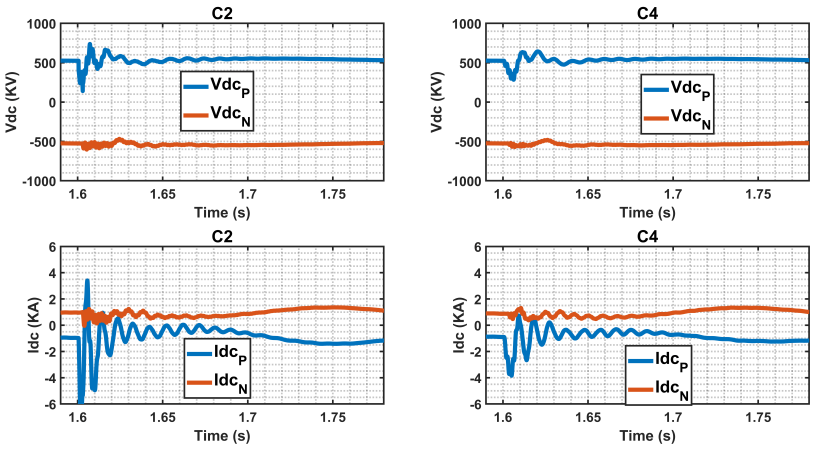

Figure C.2: Voltage and Current plots for Offshore converters (C2 & C4) for Pole to ground fault 50%

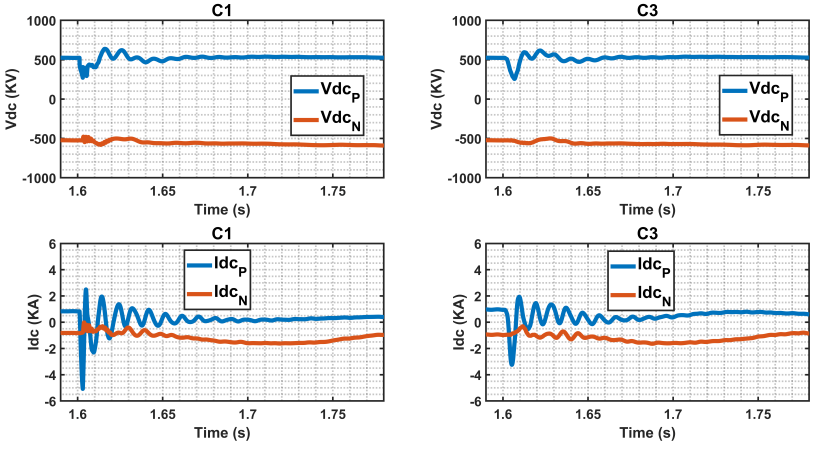

Figure C.3: Voltage and Current plots for Onshore converters (C1 & C3) for Pole to ground fault 100%

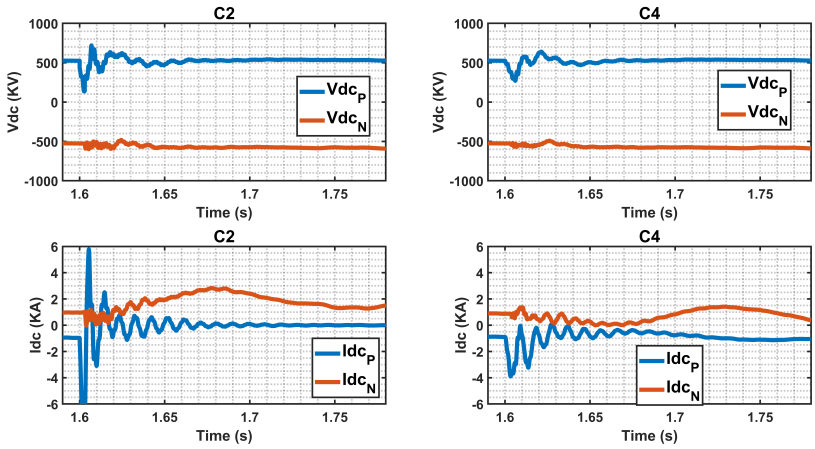

Figure C.4: Voltage and Current plots for Offshore converters (C2 & C4) for Pole to ground fault 100%

C.2. Pole to Pole Faults using VARC

The voltage and current wave forms for different fault currents and locations are shown here. The plots for pole to pole fault an using VARC breaker at 50% and 100% are given.

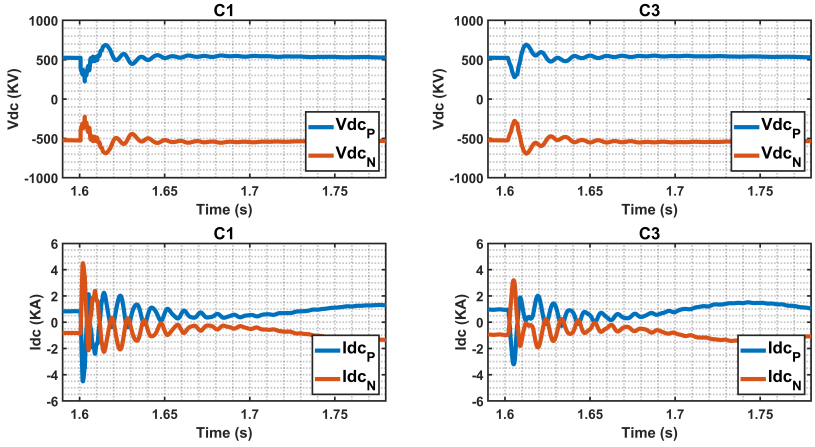

Figure C.5: Voltage and Current plots for Onshore converters (C1 & C3) for Pole to pole fault 50%

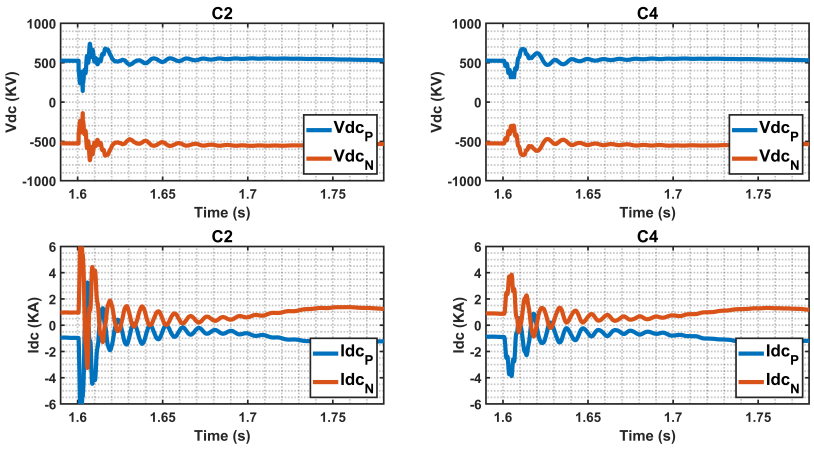

Figure C.6: Voltage and Current plots for Offshore converters (C2 & C4) for Pole to pole fault 50%

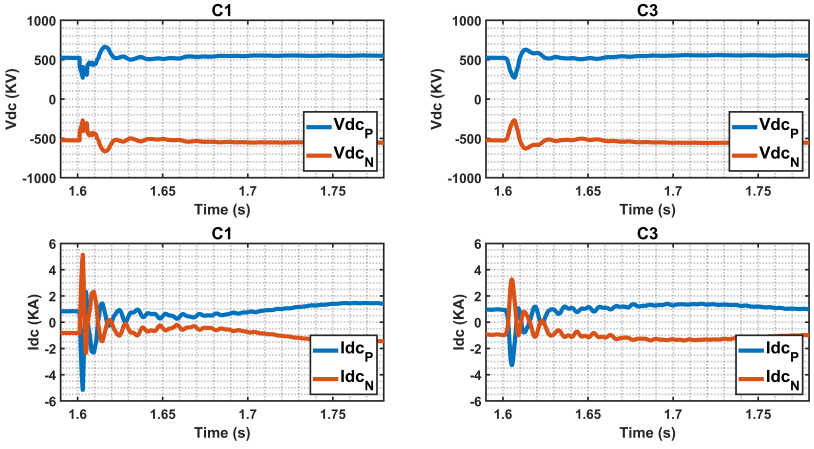

Figure C.7: Voltage and Current plots for Onshore converters (C1 & C3) for Pole to pole fault 100%

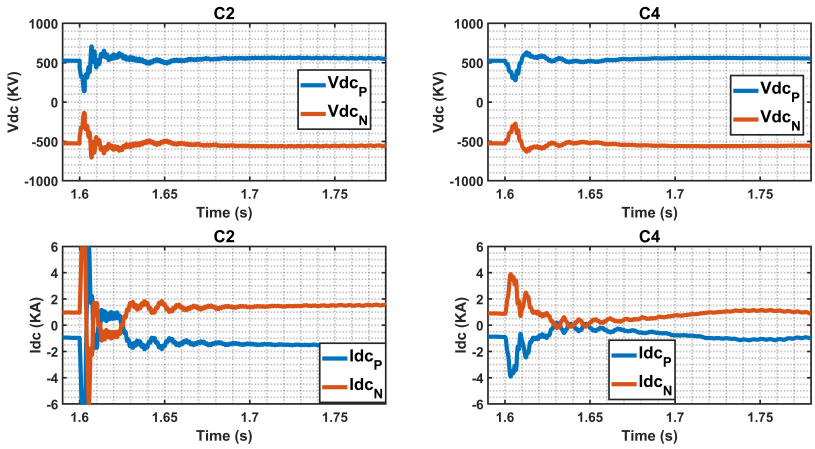

Figure C.8: Voltage and Current plots for Offshore converters (C2 & C4) for Pole to pole fault 100%

C.3. Double Pole to Ground Fault using VARC

The voltage and current wave forms for different fault currents and locations are shown here. The plots for double pole to ground fault an using VARC breaker at 0% and 50% are given.

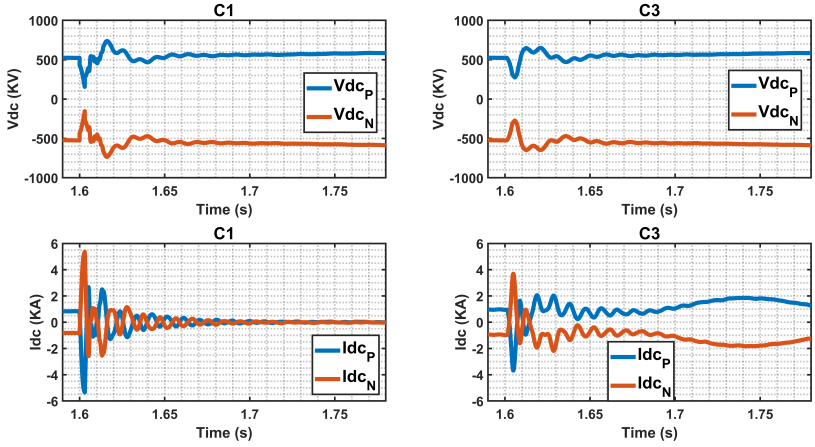

Figure C.9: Voltage and Current plots for Onshore converters (C1 & C3) for double pole to ground fault 0%

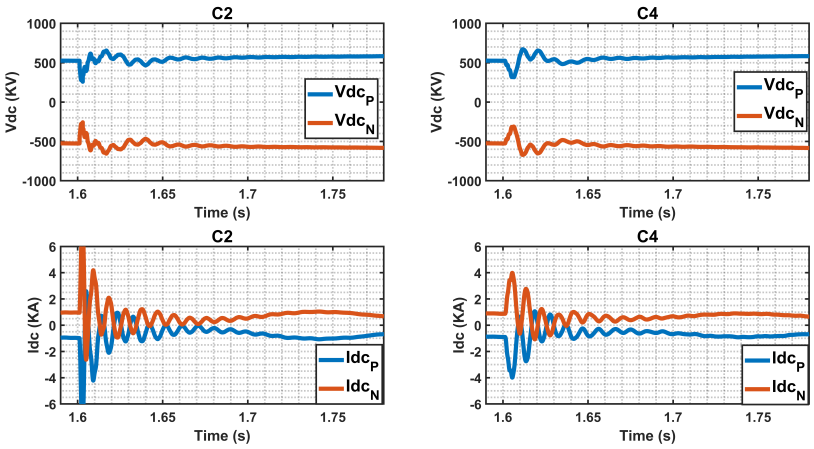

Figure C.10: Voltage and Current plots for Offshore converters (C2 & C4) for double pole to ground fault 0%

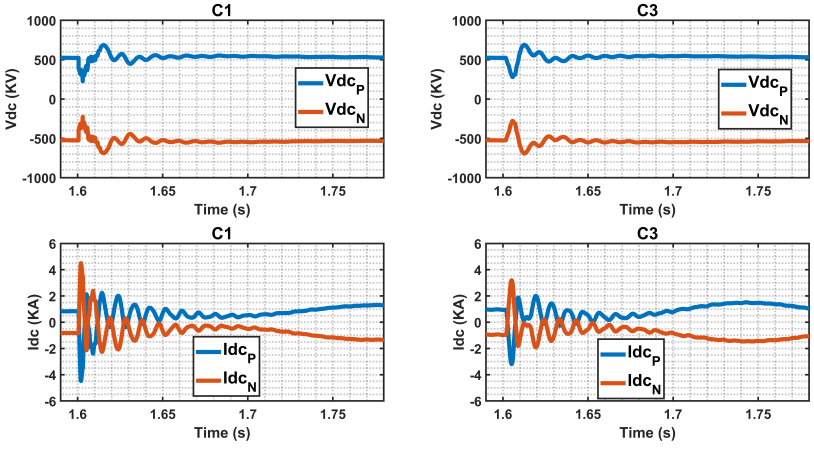

Figure C.11: Voltage and Current plots for Onshore converters (C1 & C3) for double pole to ground fault 50%

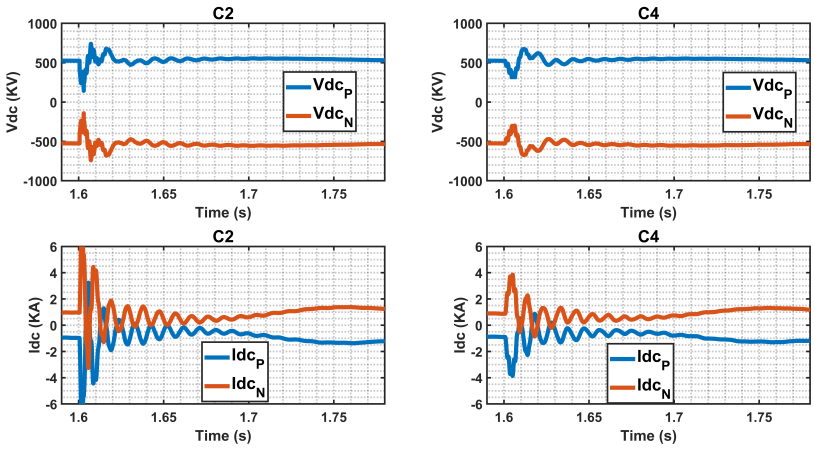

Figure C.12: Voltage and Current plots for Offshore converters (C2 & C4) for double pole to ground fault 50%

C.4. Effect of very high Inductance

Increasing the inductance will introduce high converter interactions and reduce the stability. This is demonstrated with L_{dc} = 300 mH and it is clearly seen that, there are significant oscillations observed.

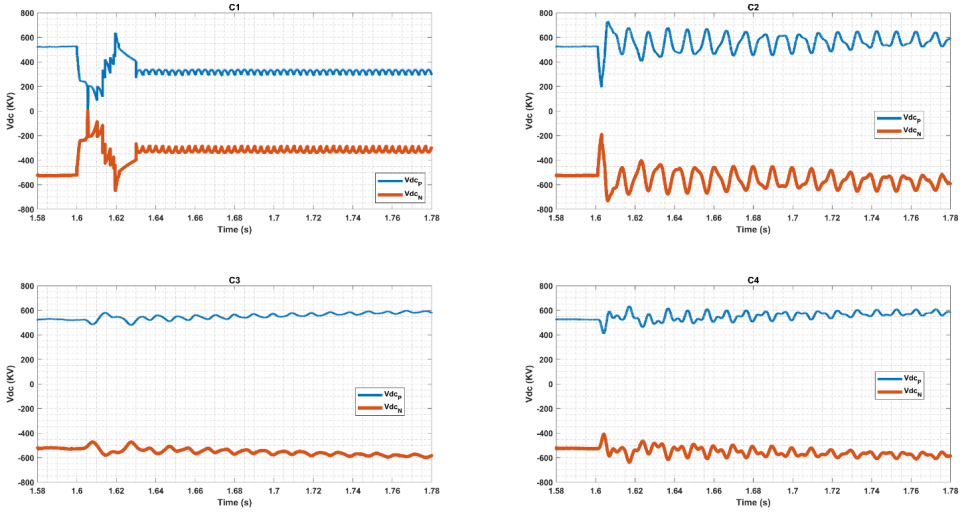

Figure C.13: Voltage Plots for all the converters (C1, C2, C3 & C4)) with L_{dc} = 300mH after a pole to pole fault

C.5. Pole to Pole fault using Mechanical breaker

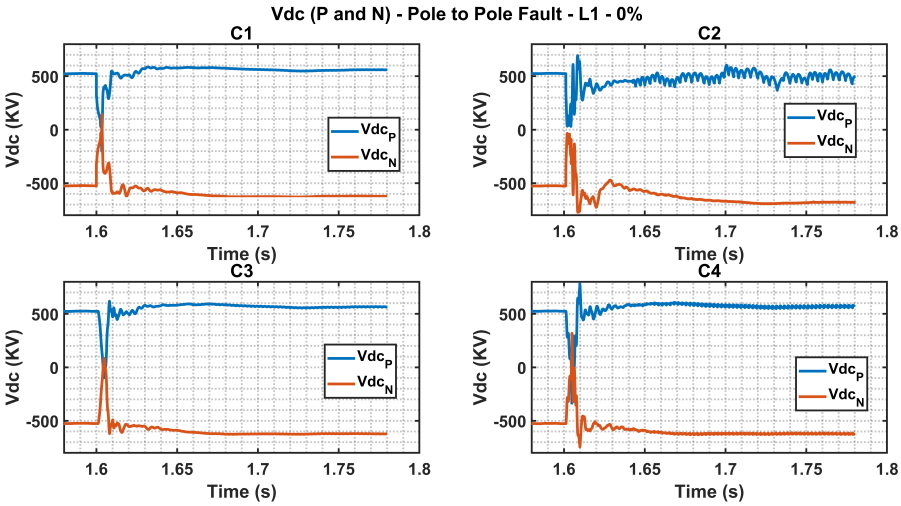

Figure C.14: Voltage Plots for all the converters (C1, C2, C3 & C4)) pole to pole fault 0%

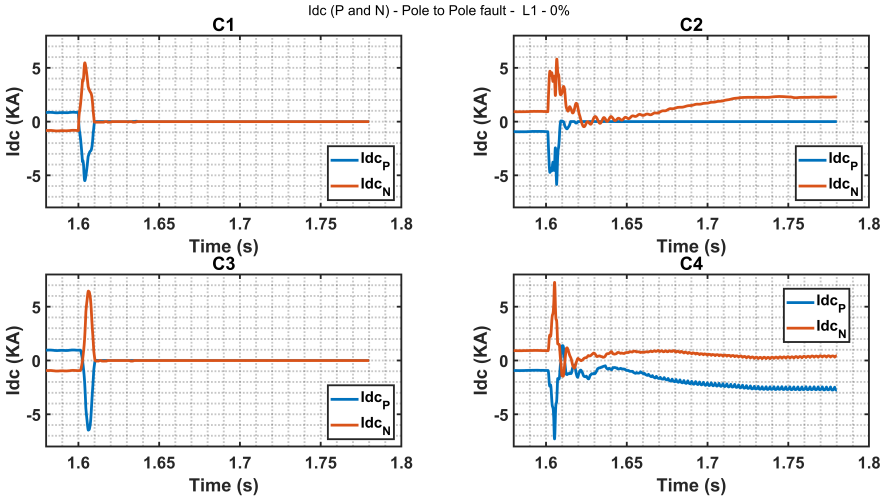

Figure C.15: Current Plots for all the converters (C1, C2, C3 & C4)) with after a pole to pole fault 0%

C.6. Energy absorbed by the Surge arrester for Figure 4.6

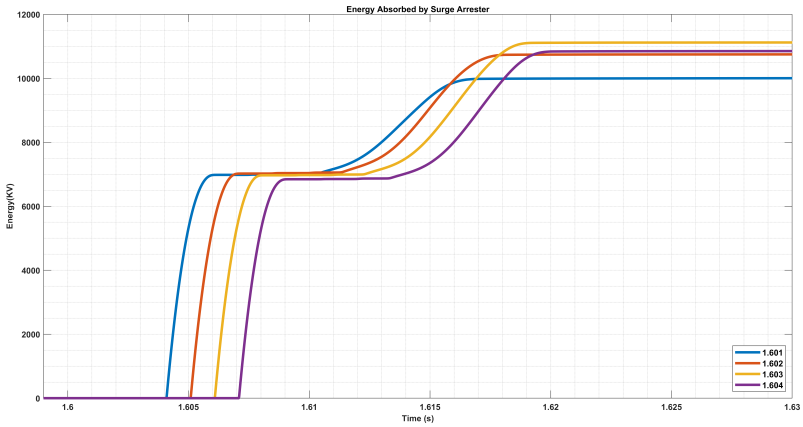

Figure C.16: Comparison of Energy dissipated across the SA when fault occurs at different time

C.7. Energy absorbed by the Surge arrester for Figure 4.10

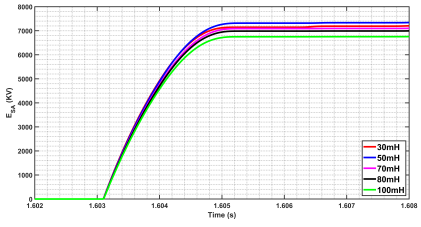

Figure C.17: E_{SA} for different L_{conv} values

C

C.8. Current through the Surge arrester for Figure 4.12

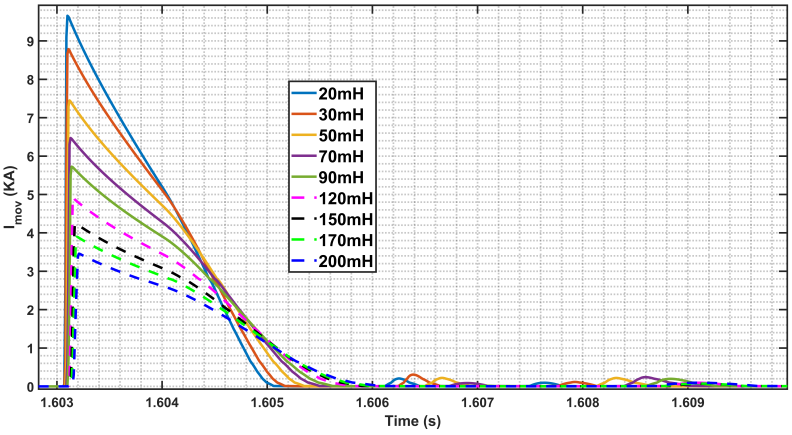

Figure C.18: I_{mov} for different L_{dc} values

C.9. DC Voltage comparison for cases proposed in subsection 4.3.1

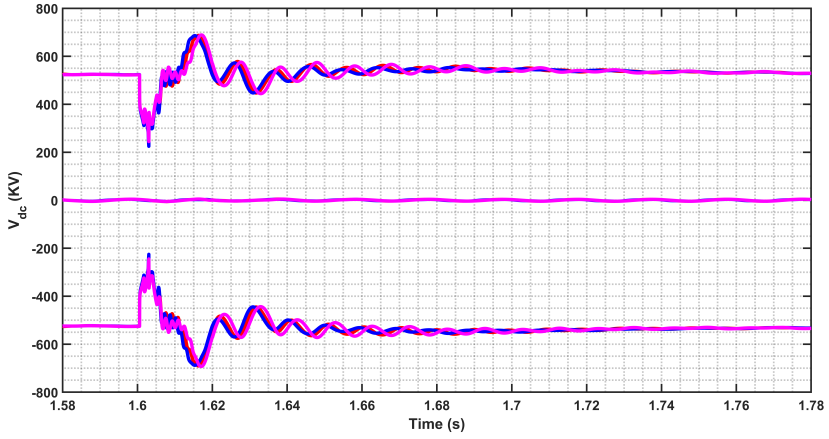

Figure C.19: Comparison of voltage stability for the proposed method

Abbreviations & Acronyms

AC Alternating Current. xiii, 9, 19, 59, 60, 73

ACCB AC Circuit Breaker. xiii, 59

CB Circuit Breaker. 6

DC Direct current. i, 3, 5, 59, 73

DCCB DC Circuit Breaker. i, 3, 5, 6, 9, 10, 14, 15, 19–22, 25, 27, 28, 30, 34, 37, 38, 41, 42, 47, 50, 51, 53, 55

EAC Equal Area Criterion. 2

FB MMC Full Bridge MMC. i, x, 6, 11, 47–51

GIS Gas Insulated Substation. 3

HB MMC Half Bridge MMC. i, ix, xiii, 6, 11, 12, 19, 48–51, 62

HVAC High Voltage Alternating Current. ix, 1, 2

HVDC High Voltage Direct Current. i, ix, 1–4, 6, 9–11, 19, 24, 29, 73

IGBT Insulated Gate Bipolar Transistor. i, 3, 5, 11, 12, 21, 25, 34, 53

LCC Line Commutated Converter. 2, 9, 11

MMC Modular Multilevel Converter. i, ix, x, xiii, 3, 4, 6, 9–11, 15, 19–22, 25, 27, 28, 30, 32–35, 37, 42, 46, 47, 53, 73

MTHVDC Multi-Terminal HVDC. xiii, 4

OHL Over Head Lines. 10

OWF Offshore Wind Farm. i, 1–4

PCC Point of Common Coupling. 9

PLL Phase Locked Loop. 1

PWM Pulse Width Modulation. 4

SA Surge Arrester. xi, 14, 15, 38–40, 71

SCR Short Circuit Ratio. ix, 13, 26, 43

SoS Security of Supply. 4

SPM Step Pulse Modulation. 4

STATCOM Static Synchronous Compensator. 13

UNFCCC United Nations Framework Convention on Climate Change. 1

VARC VSC assisted Resonant Current. ix, x, xiii, 6, 15, 19, 20, 26, 28–31, 37

VSC Voltage Source Converter. 2–4, 6, 9, 11, 15, 19, 74