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RESEARCH ARTICLE

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Advanced textured monocrystalline silicon substrates with high optical scattering yields and low electrical recombination losses for supporting crack-free nano- to poly-crystalline film growth

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Abstract
Crystalline silicon tandem devices with perovskites, CIGS, and nanocrystalline silicon, as well as the TOPCon design, are incompatible with the conventional pyramidal surface texture of silicon. This is a result of crack formation in nano to polycrystalline growth on large sharp surface features. In this work, three texturing approaches are investigated, using alkaline and/or acidic wet chemical etches, that can lead to the crack-free growth of nano to polycrystalline materials on textured surfaces. In this work, we show that without acidic smoothening, the fraction of <111> pyramidal surface coverage has to remain relatively small to prevent crack formation during crystalline growth on these surfaces. Applying an acidic etch as a function of time continuously smoothens surface features. This shifts the reflection to wider scattering angles and results in higher total reflected intensity with respect to the conventional texture, making it an interesting option for a wide variety of tandem pv applications. Finally, we demonstrate crater-like features on a <100> monocrystalline silicon surface using an etching process including a sacrificial layer. These craters increase light scattering into wider angles, but to a lesser extent than the former approach. In terms of passivation, we demonstrate the positive effect of a post deposition hydrogen treatment. Initial dilution of the silane plasma improves passivation on a <111> surface, but is detrimental to passivation on a <100> surface, likely because the hydrogen dilution results in epitaxial growth at the c-Si/a-Si:H hetero-interface. A minority carrier lifetime of over 3 ms has been achieved for all texturing approaches, after deposition of a 15 nm a-Si:H layer on both sides of the wafer, for different a-Si:H deposition and annealing schemes.

KEYWORDS
amorphous growth, crystalline silicon, epitaxial growth, novel texture, passivation, surface features, wet chemical etch

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1 | INTRODUCTION

With the relative price of crystalline silicon modules dropping faster than the balance of systems costs for a PV system, increasing the efficiency of PV devices at low production costs is crucial. As such, much attention is devoted to the TOPCon design. TOPCOn devices can be upgraded from PERC and PERT devices with relative ease through addition of an ultrathin SiO_2 layer and a doped poly-Si layer. Moreover, TOPCon is easily adapted for IBC[1] and bifacial use.[2] Alternatively, tandem PV devices are receiving increased attention, where a crystalline silicon (c-Si) bottom cell is to be combined with a perovskite,[3-5] C(I)GS[6] or nano-c-Si top cell.[7,8] These approaches all have a major challenge in common. The <111> crystal orientation, the pyramidal surface texture that is the standard for industry, and the scientific community is crucial for light management but incompatible with the crystalline phase in the nano/poly-si, perovskite, and C(I)GS materials.[9-11] Not only is conformal growth challenging on the sharp pyramidal features, the crystalline phase tends to form cracks,[12] or low-density defective regions.[13,14] These cracks are located in the valley between sharp features, or in other words, the focal point of perpendicular growth on steep features. Developing surface features on monocrystalline silicon through a wet chemical treatment requires anisotropic etching behavior. One approach, widely used industry, is the use of an KOH-, NaOH-, or TMAH-alkaline etch.[15,16] Alkaline etches preferentially etches crystal orientations with lower activation energies for the etching reactions. The bonds of the <111> crystal orientation for instance are much stronger, and therefore harder to break, than the <100> orientation. Consequently, the preferential etching of the <100> plane results in a square based pyramidal <111> plane. Alternatively, the <110> orientation is also preferentially etched, but results in perpendicular trenches with <111> side walls that are less attractive for pv applications.[17] Applying an acidic etch, such as a combination of hydrofluoric acid (HF) and nitric acid (HNO3), on a polished monocrystalline silicon results in isotropic etching. Some nonuniformity is required to develop features on a mono c-Si surface. Saw damaged wafers exhibit such nonuniformity, but the optical effectiveness of features resulting from the chemical polish of the saw damaged is limited, due to a lack of tunability.[16,18] Alternatively, with the use of photolithography, some parts of the surface can be masked, resulting in anisotropic etching of the surface. This has proven successful,[19,20] but such an expensive approach would limit the wide scale application.

In this work, we explore 3 alternative wet chemical etching approaches on polished n-type monocrystalline silicon wafers with <100> crystal orientation. The aim is to develop a texture that does not negatively affect the quality of the crystalline phase processed on top of the wafer surface and provide efficient light scattering. Moreover, for use in photovoltaic devices, it is important that the developed surface can be passivated with relative ease to ensure sufficiently high charge carrier lifetimes. Passivation can be complicated if multiple crystal orientations are exposed on the wafer surface. In texturing approach 1 (T1) and texturing approach 2 (T2), anisotropic etching is achieved through an alkaline TMAH etch. In T1, however, the process is interrupted before the surface is fully covered. In T2, the alkaline etch is followed by an acidic HF/HNO_3 poly etch step, which etches isotropically, resulting in the smoothening of the sharp pyramidal features. In texturing approach 3 (T3), a sacrificial boron implanted poly-Si layer is first processed to create anisotropic etching behavior, as the grain boundaries in the poly-Si layer are favorably etched with respect to the crystalline phase. This sacrificial layer is then fully etched away using poly etch. Simplified flowcharts of the three approaches are shown in Figure 1. For all 3 approaches, the influence of the etching time on the surface features and optical behavior was characterized, and the passivation quality of a range of amorphous silicon layers was investigated.

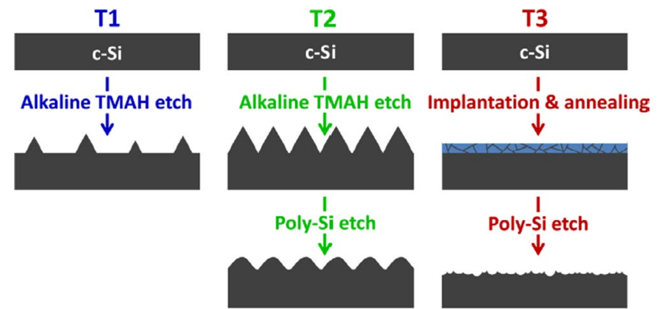

FIGURE 1 Simplified flowchart of texturing approaches T1-T3

2 | EXPERIMENTAL DETAILS

2.1 | Texturing approaches

In this work, Topsil Floatzone n-type <100> monocrystalline silicon wafers were used with a thickness of 300 µm, unless mentioned otherwise. These wafers were used for three texturing approaches. For T1, an alkaline Tetramethylammonium hydroxide (TMAH) (25% wt. in H_2O) etch solution is used at a temperature of 80°C, followed by a 3 minute rinse in deionized (DI) water. For T2, a 10 minute TMAH etch and rinse was followed by an acidic poly etch, consisting of 1 part HF (405% wt. in H_2O), 6 parts HNO3 (69.5% wt. in H_2O), and 3 parts H_2O. For T3, a 2 nm SiO_2 layer is first grown on the wafer through a nitric acid oxidation cycle (NAOC), which is described elsewhere.[21] On top of this, an amorphous silicon layer of 250 nm is processed, using a Tempress low pressure chemical vapor deposition (LPCVD) tube furnance. This layer is then implanted with boron ions

and annealed at high temperature to active the dopants and crystallize the amorphous layer. For the boron implantation, a Varian Implanter E500HP is used with an energy of 5 keV and a dose of 1016 cm^{-2}. Next, a Tempress tube furnace is used for annealing in an N_2 atmosphere at 950°C. The ramping rate for heating or cooling is 10°C/min. The poly-si sacrificial layer is then fully etched away using a different acidic poly etch solution with respect to T2, consisting of 1 part HF (40% wt. in H_2O), 35 parts HNO3 (69.5% wt. in H_2O), and 14 parts H_2O.

2.2 | Roughness and optical measurements

The SEM analysis was performed on a FEI Nova NanoSEM 450, using an immersion detector at an acceleration voltage of 10 kV. The AFM analysis was performed on an Bruker AFM FastScan. Using a Fastscan closed loop scanner head, a 20 µm by 20 µm area was measured. The RMS roughness (Sq), maximum peak height (Sz), and mean slope (Sdq) were extracted using the NanoScope Analysis software from Bruker. The reflectance measurements were performed using a LAMBDA 1050+ UV/Vis/NIR Spectrophotometer with 150 mm InGaAs integrating sphere from PerkinElmer. For the angular distribution of the reflectance, the 180 mm automated reflectance/transmittance analyzer (ARTA[22]) accessory is used on a similar LAMBDA 950 PerkinElmer base unit.

2.3 | Wafer passivation

Between the texturization process and the amorphous silicon deposition, the wafers were cleaned through 3 consecutive NAOC cycles. The amorphous silicon layers used for passivation were grown using a radiofrequency plasma-enhanced chemical vapor deposition cluster tool, operating at a frequency of 13.56 MHz. The deposition conditions are indicated in Table 1. The nc-Si:H film was grown in a separate reactor in the same cluster tool, at very high frequency (40 MHz), a substrate temperature of 180°C, a pressure of 4 mbar, and forward power of 278 mW cm^{-2}. The H_2 flow is set at 120 standard cubic centimeters per minute (sccm), while the initial SiH_4 flow of 1.2 sccm is increased to 3.5 sccm after about 50 nm of deposition for the remainder of the growth. The lifetime measurements were performed on a Sinton WCT-120 under Transient photoconductance decay (Transient PCD) mode. The reported lifetimes are at a minority carrier density of 1e15 cm^{-3}. The wafers were annealed in a Thermo Scientific Heratherm in an ambient atmosphere.

TABLE 1 Conditions used for processing the different a-Si:H passivation layers and hydrogen plasma treatment

	a-Si:H-1	a-Si:H-2	a-Si:H-3	HPT
SiH_4 (sccm)	40	10	2	0
H_2 (sccm)	0	30	200	200
T_{sub} (°C)	180	180	130	180
P_{rf} (mW cm^{-2})	19.4	20.8	62.5	20.8
p (mbar)	0.7	1.4	10	2.2

3 | RESULTS AND DISCUSSION

3.1 | Influence of texturing approaches on surfaces and optical behavior

The three texturing approaches result in different textures, as shown in Figure 2. For T1, the surface is transformed from the flat <100> to a pyramidal <111> surface with increasing etching time. The RMS roughness (Sq), maximum peak height (Sz), and mean slope (Sdq), resulting from the AFM analysis, are plotted in Figure 3. For T1, increasing the etching time from 30 seconds to 4 minutes leads to an increase of the RMS roughness from about 9 nm to 360 nm while the maximum peak height increases from about 210 nm to 1.9 µm. After about 5 minutes, the surface is fully covered with pyramids. At this point, the mean slope of about 45 degrees no longer increases. The RMS roughness and max peak height keep steadily increasing to about 480 nm and 2.8 µm at 9 minutes, our last measured data point. This has a large impact on the spectral reflected intensity, as shown in Figure 4. While the shape of the reflectance does not change, the reflectance at a wavelength of 600 nm is decreased from about 35% to 12% when the etch time is increased from 30 seconds to 9 minutes. For T2, the pyramidal <111> features are smoothened using an acidic etch. The etching time was varied from 30 seconds to 30 minutes. The SEM images in Figure 2 show how the pyramidal features are smoothened with increasing etch time. The RMS roughness is decreased from about 630 nm after 30 seconds to about 530 nm after 3 minutes and down to 290 nm after 10 minutes. The maximum peak height is decreased from 3.8 µm to 2.1 µm in that same period of time, while the mean slope is decreased from about 45 degrees to 22 degrees. As shown in Figure 4, as a result of the decreasing roughness and peak height, the reflected intensity is increased from 22% to 34% when the etch time is increased from 30 seconds to 10 minutes. For T2, a 250 nm sacrificial poly-si layer is etched using a poly etch. As Figure 2 shows, getting the timing of the etching process right is important to obtain the desired crater-like features. At 3 minutes, the poly-si layer is removed, but some of the SiO2, which has a much lower etching rate than Si, remains. At 5 minutes, the crater-like features are apparent. The features are rather small with a RMS roughness of about 25 nm, a maximum peak height of about 210 nm, and a mean slope of

about 17 degrees, as reported in Figure 3. Since the features are relatively small, the reflectance is about 32% at 600 nm, almost similar to that of a flat surface. When the etching time is further increased, the roughness, peak height, and reflectance do not change much for the observed etching times. The features are eventually smoothened again, as the poly etch has an isotropic etching behavior on mono c-Si.

For single junction solar cells, the features on the silicon wafer surface will be positioned at the front of the device. In this case, minimal reflectance, so maximal light in-coupling is desirable. However, for tandem PV applications in which c-Si operates as the bottom cell, the surface features will be located at the interface between two junctions. In this case, wide angle light scattering is potentially more critical than light in-coupling. To investigate the light-scattering efficiency of the surfaces, the angular distribution of the reflected intensity at a wavelength of 600 nm is shown in Figure 5. For T1, the shape of the angular reflection changes as the surface is transformed from predominantly flat to pyramidal. For a polished surface (0 m), the reflection is in the direction normal to the surface. Since the incident light has a certain spot size, a very small angular distribution is observed. A fully pyramidal surface also reflects mainly in the normal direction. The pyramids have a mean slope of 45 degrees. A fraction of the light, under normal incidence, is reflected off this slope parallel to the surface. When it encounters a second slope, a fraction is reflected back perpendicular to the surface, as schematically shown in Figure 6. Since there is a distribution in the slope and size of the pyramids, we observe an increased reflection in the 30-80 and −30 to −80 degree angle range with increasing pyramidal coverage. For T2, we observe a shift of the angle of maximum intensity with increasing etching time. This is because the average slope of the pyramids decreases from about 45 degrees to about 30 degrees, as shown in Figure 3. As the average slope is decreased, the earlier mentioned double reflection events become increasingly rare. This leads to an increase of the total reflected intensity with etching time, as observed in Figure 4, and a shift to scattering angles equal to twice the angle of the slope of the pyramids. This is demonstrated by the observation that for T2 the angle of maximum reflected intensity is about 0 degrees for a mean slope of 42 degrees at 30 seconds. At 60 seconds, the means slope is about 30-35 degrees and maximum reflected intensity is about 70 degrees, and it is further shifted to about 50 degrees at 5 minutes etch time and a mean slope of 25 degrees. For T3, the etching time does not significantly affect the angular reflection distribution. Light is scattered in wider angles than for flat surfaces, but due to the relatively small features, light is still mainly reflected in the perpendicular direction.

3.2 | Passivation of textured surfaces

An important criteria for wafers with texture resulting from T1-T3 is that they should be relatively easy to passivate. In

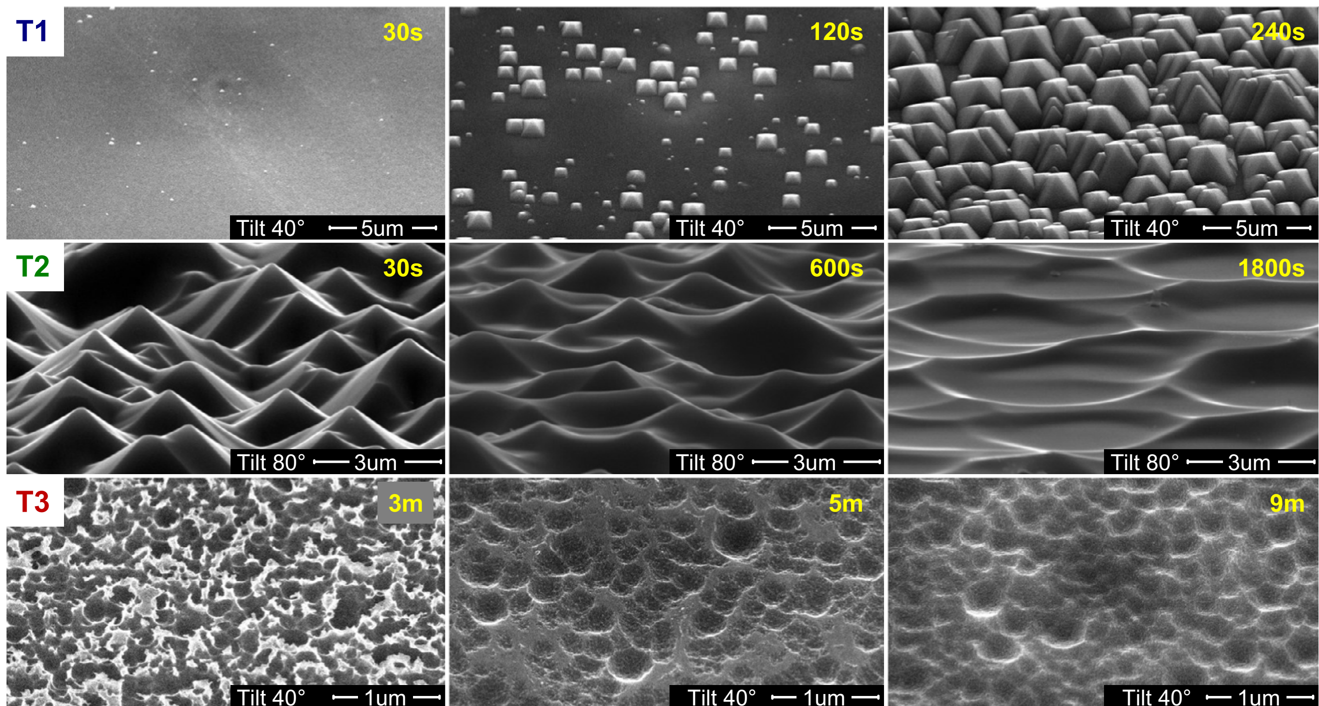

FIGURE 2 Scanning Electron Microscopy images of the T1 (top), T2 (middle), and T3 (bottom) textures as a function of etching time of the final step in the texturing process. Sample tilt and scale are indicated in the images

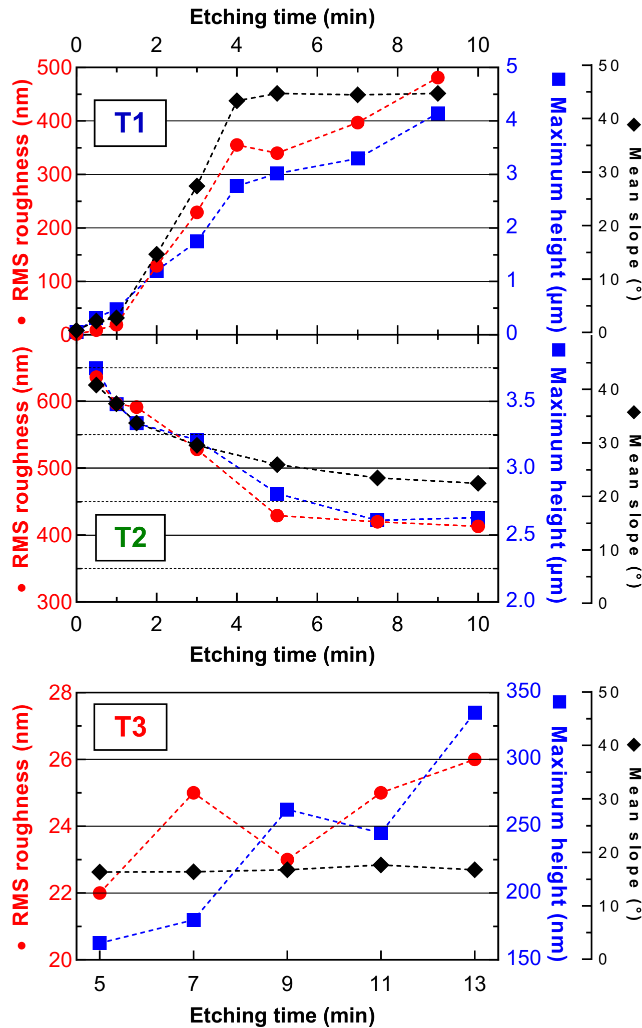

FIGURE 3 RMS roughness (red circles), Mean slope (black diamonds), and maximum feature height (blue squares) as a function of etching time of the T1 (top), T2 (middle), and T3 (bottom) texturing approaches. T1 0 min represents a polished wafer

order to test the passivation quality, we processed a 15 nm amorphous silicon layer on both sides of the textured wafers and measured the minority carrier lifetime. For good passivation, in the order of several milliseconds, a thin uniform amorphous silicon layer is desirable. Initial experiments showed that the growth of such a layer is not only a function of the deposition conditions. A recipe optimized for the passivation of a c-Si surface with pyramidal <111> features, referred to as a-Si:H-2 in Table 1, resulted in very low lifetimes of several tens of microseconds on a polished <100> surface. The lifetime decreased even further upon low temperature annealing, at 180°C, potentially indicating epitaxial growth.[23] Epitaxial crystalline growth through the amorphous silicon passivation layer is detrimental to the passivation quality.[23-26]

To distinguish between the effect of the surface roughness and the crystal orientation on the amorphous silicon growth, the experiment was repeated on a flat, polished <111> <100> surface. The results are shown in Figure 7, indicated by the black curves with open symbols. This time, the a-Si:H-2 deposition was followed by a hydrogen plasma treatment (HPT). The results show that a <100> surface is more challenging to passivate than an <111> surface, which is in line with earlier reports.[25,27,28] This is likely because at the surface, a <111> crystal orientation only has a single dangling bond per surface atom that requires passivation, while the <100> surface has two dangling bonds per surface atom. This is illustrated in Figure 8, where the red lines indicate dangling bonds at the surface of the silicon crystal in case of a flat <111> and <100> crystal orientation. Apart from the overall higher lifetimes of the <111> wafers, the results show that if the silane precursor is diluted in hydrogen, poor minority carrier lifetimes are very likely to occur on a <100> surface. The lifetimes further decrease upon annealing, potentially indicating epitaxial growth. On the other hand, hydrogen diluted silane plasmas lead to decent passivation on a <111> surface in this work and in others.[27,29] Introducing hydrogen in the plasma has two effects on etching and growth of the amorphous and crystalline phase. Firstly, introducing hydrogen causes competition between the silicon growth flux and atomic hydrogen etching.[30,31] The atomic hydrogen more efficiently etches weaker bonds. Consequently, it selectively etches the amorphous over the crystalline phase.[32,33] Secondly, the initial growth is determined by the availability of SiHX precursors at the surface. For dense material growth, or indeed for crystalline growth, sufficient mobility of SiHX precursors on the surface is required. The atomic hydrogen flux to the substrate surface in a hydrogen diluted plasma is believed to enhance the mobility and increase the diffusion of SiHX precursor on the surface.[34,35] The main difference between the two crystal orientations is the additional terminated silicon bond per surface atom available on the <100> surface.

In addition, the crystalline orientation plays a crucial role in etching and growth as well. A c-Si surface with <100> orientation etches faster than a <111> orientation. A <100> surface atom has only two back bonds that needs to be simultaneously broken by hydrogen atoms or other etchants; whereas, the <111> surface has alternately a full monolayer that requires three back bonds to be simultaneously broken. This relative stable monolayer acts as a barrier for fast etching in the <111> direction. It requires more effort and consequently more energy to etch the <111> surface. The opposite is also true: since it costs less energy to remove <100> surface atoms it also requires less energy to form crystalline layers on top in the <100> direction. In addition, a <100> surface atom has no rotational freedom, a condition which benefits crystalline growth. The <111> surface has alternately a monolayer of single back bonded atoms with rotational freedom. This will hinder crystalline growth, and it becomes more likely to facilitate the growth of amorphous tissue on

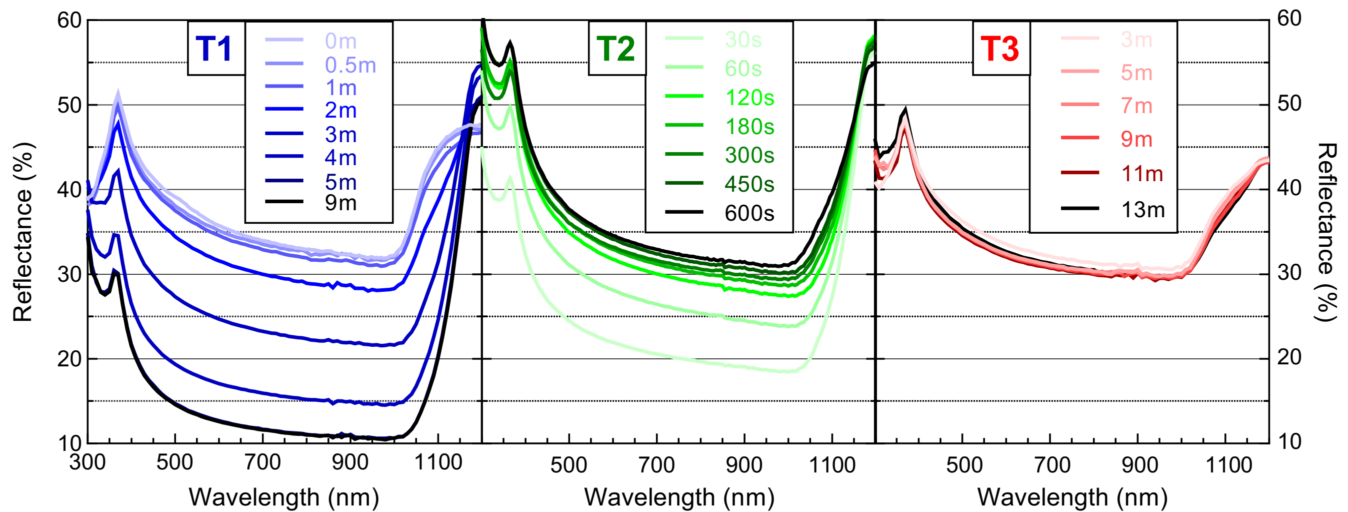

FIGURE 4 Spectral reflectance measurements as a function of etching time for T1 (left, blue), T2 (middle, green), and T3 (right, red). T1 0 min represents a polished wafer

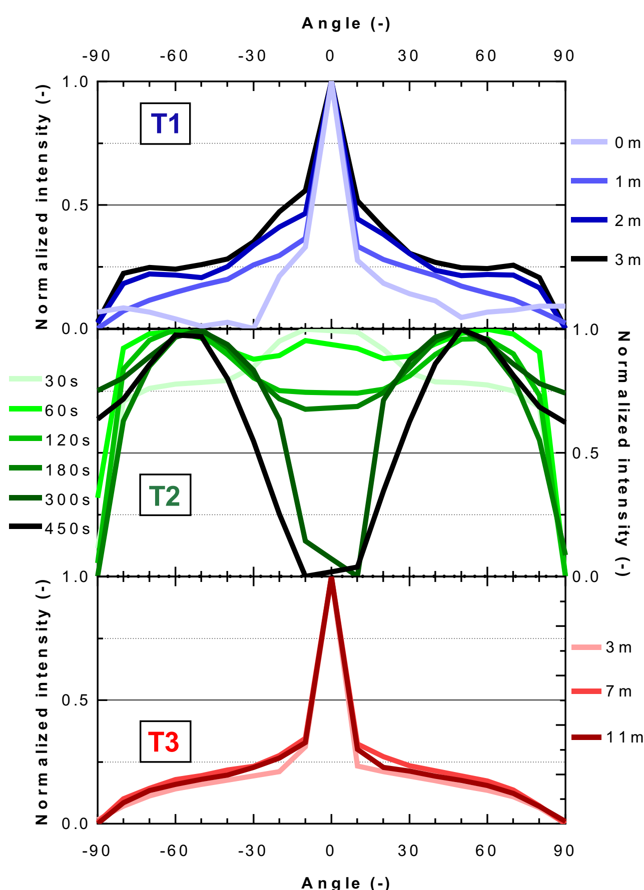

FIGURE 5 Normalized intensity of T1 (top, blue), T2 (middle, green), and T3 (bottom, red) as a function scattering angle, for different etching times. Normalization is performed with respect to the maximum intensity. T1 0 min represents a polished wafer

top. Consequently, a hydrogen-diluted silane plasma results easily in epitaxial growth on top of the <100> oriented silicon surface in reference to a <100> oriented silicon surface.

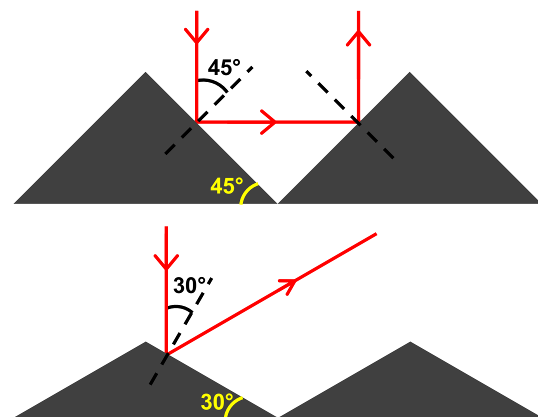

FIGURE 6 Simplified visual of light (red) reflected of a surface with a 45 degree slope (top) and 30 degree slope (bottom), respectively

To prevent epitaxial growth, an amorphous silicon layer was grown on a polished <100> surface using only SiH_4 as a precursor, indicated by a-Si:H-1. As Figure 7 shows, this leads to a minority carrier lifetime of about 1.2 ms in the as deposited, or preanneal (PA) state. The lifetime is further increased to a maximum of over 5 ms when annealed for 30 minutes at 240°C. When hydrogen is introduced post a-Si:H deposition, the lifetime can be further increased. Hydrogen was introduced through a hydrogen plasma treatment, or by growing amorphous bilayers, where the a-Si:H-1 deposition was followed by a hydrogen-diluted silane plasma (a-Si:H-2 or a-Si:H-3) deposition. For the latter, the combined thickness was kept constant at about 15 nm and both layers were of roughly equal thickness. The deposition conditions used for these layers are shown in Table 1. The lifetimes of these passivated wafers are shown in Figure 7, as a function of annealing temperature. Preanneal, for all samples, the lifetime is increased when hydrogen is introduced in some form.

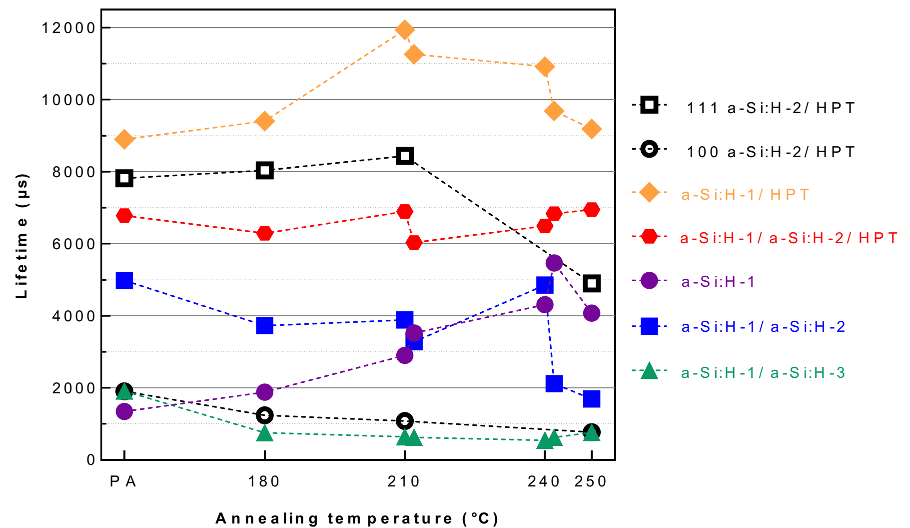

FIGURE 7 Lifetimes of passivated wafers as a function of annealing temperature. The legend indicates the various amorphous silicon conditions used for passivation. These conditions can be found in table. PA indicates wafer passivation preannealing. Multiple datapoints at the same temperature indicates the lifetime of wafers annealed at 10 min followed by an additional 20 min

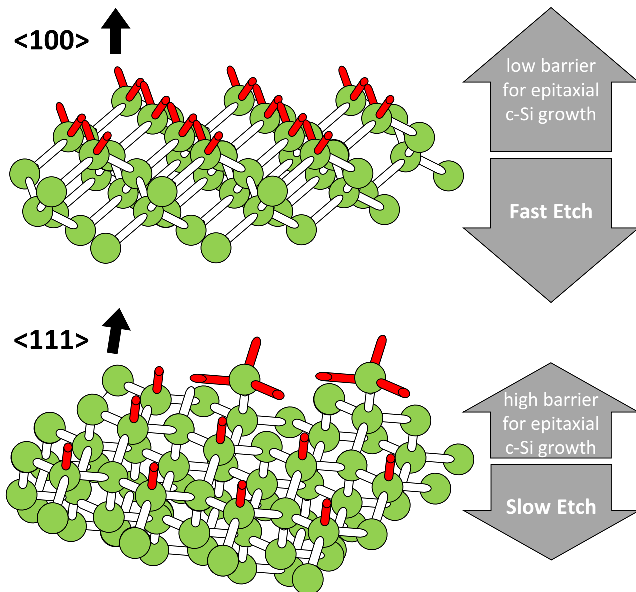

FIGURE 8 <100> (top) and <111> (bottom) orientations at the surface of a silicon crystal. Green circles represent silicon atoms, white lines represent covalent silicon bonds, red lines represent the dangling bonds at the surface

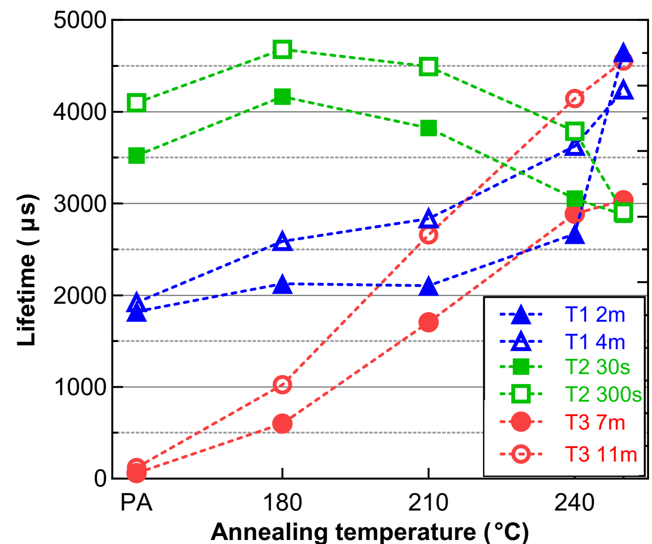

FIGURE 9 Lifetimes of textured wafers passivated by a 15 nm a-Si:H-1 + HPT layer, as a function of annealing temperature. Lifetimes are reported at a minority carrier density of 1e15 cm^{-3}. Lifetimes are reported for two different etching times for T1 (blue), T2 (green), and T3 (red), respectively

The combination with a-Si:H-3 seems to lead to epitaxial growth, since the lifetime drops significantly when annealed. The highest lifetimes are obtained when an a-Si:H-1 layer or a-Si:H-1/a-Si:H-2 bilayer is followed by a HPT. Lifetimes between 7-9 ms are obtained preanneal, and for the best sample, this is increased to 12 ms when annealed for 10 minutes at 210°C. This is on par with > 8 ms lifetimes reported by Mews et al[36] for a similar a-Si:H layer and HPT on <100> polished wafers. For higher annealing temperatures, the lifetime drops. During regular processing of a SHJ device, however, substrate temperatures are generally kept below 200°C, so this should be no obstacle.

This demonstrates that integration of hydrogen in the amorphous silicon is crucial for high quality passivation, but dilution of silane in hydrogen during initial growth can lead to undesired epitaxial growth on <100> surfaces. This means that passivating the T1-T3 surface can be challenging since different crystal orientations are exposed and different roughness's are obtained as a function of etching time. To get an indication of the passivation effectiveness, 15 nm of a-Si:H-1 followed by HPT was processed on each texturing approach. The lifetimes are shown in Figure 9. The figure shows that decent lifetimes of 3 ms and up can be achieved for all texturing approaches. However, T1 and T3 require annealing at relatively high temperatures, 240-250°C, for

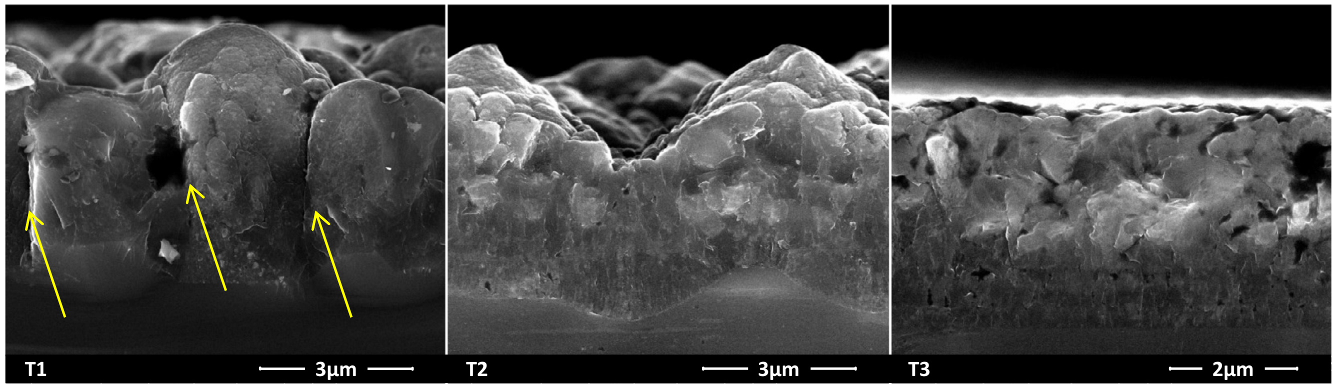

FIGURE 10 Cross-sectional SEM images of a 3 µm nc-Si:H layer grown on top of a textured c-Si wafers. T1 is shown left, T2 in the center, and T3 on the right. Yellow arrows indicate cracks in the grown material

30 minutes to achieve these lifetimes. A strong increase of the lifetime from the µs to ms range has been reported earlier, especially when hydrogen diluted amorphous silicon is used.[29] It is understood that the increase of the passivation quality upon annealing is mainly a result of hydrogen moving to the c-Si/a-Si:H interface, reducing the interface defect density.[37,38] For longer annealing times, the passivation quality can be further increased as a results of hydrogen induced reorganization of the amorphous silicon bulk.[36,37,39] For T2, lifetimes of 4-7 ms are achieved already preanneal. The passivation remains stable up to 180°C, after which the quality slightly deteriorates at higher annealing temperatures. The reason why the observed lifetime decrease as a function annealing temperature occurs exclusively for T2 is unclear. It is most likely a result of the relatively large geometry of the T2 pyramidal features, which can potentially cause some nonuniformity in thin films in terms of thickness and porosity, in combination with the relative large fraction of <100> surface orientations.

3.3 | Growth of device quality nanocrystalline silicon absorber

Finally, we consider the quality of the nc-Si:H processed on the 3 textures. Cross-sectional SEM images of these films are shown in Figure 10. Feature sharpness determines whether cracks appear. Where along the growth position the cracks appear depends on the focal point of the features, which is a function of the feature size and depth. In Figure 10, about 3 µm of nc-Si:H was grown on the different textures, which is representative for a nc-Si:H absorber in a multijunction device,[40,41] and much thicker than the poly-Si layer in a TOPcon device[42,43] and the required absorber thickness of a perovskites[44] or C(I)GS top cell.[45] The images show crack-free, device quality nc-Si:H growth on T2 that was smoothened for 300 seconds and T3 that was etched for 5 minutes. Only T1, etched for 3 minutes, clearly shows cracks through the nc-Si:H film, meaning that yet shorter etching times are required for the growth of a device quality film.

4 | CONCLUSION

We have performed a study on the surface of monocrystalline silicon wafers, following the application of three novel wet chemical texturing approaches that are designed to support the processing of device quality nano to polycrystalline materials. Specifically, we characterized the influence of etching time, of the final processing step, on the surface features, optical behavior, and passivation quality of the three texturing approaches. The development of small and dispersed pyramids (T1) does not seem very promising for pv applications. The fraction of pyramidal surface coverage has to remain small for crack-free nanocrystalline material growth, at which point the optical behavior is close to that of a flat surface. The surface features, and resulting optical behavior, of the smoothening of a surface fully covered by square based pyramidal <111> features (T2) show a strong etch-time dependence. The roughness, peak height, and the average slope of pyramids decrease with etch time. These changes lead to a shift to wider scattering angles and higher total reflected intensity, which makes for an interesting texture for tandem pv applications. The processing of a crack-free device quality 3 µm nc-Si:H layers has been demonstrated at an etch time of 300 seconds. The etch time could potentially be further reduced, especially for thinner films, without damaging the integrity of the nano or polycrystalline film. The use of a sacrificial layer to create anisotropic etching behavior with an acidic etch is potentially very promising. We have demonstrated that crater-like features can be produced on a <100> monocrystalline silicon surface. These features decrease the reflected intensity by 3%-5% with respect to flat wafers and increase the reflection into wider angles, albeit not as efficiently as T2. This texturing approach could benefit from further optimization of the sacrificial layer.

The passivation quality showed a strong dependence on the crystal orientation at the wafer surface, in combination with the amorphous silicon deposition conditions. Postdeposition treatment of the a-Si:H passivation layer with hydrogen, either through a hydrogen plasma or a bilayer configuration with hydrogen diluted a-Si, strongly improves passivation quality. Dilution of the plasma with hydrogen during initial growth increases passivation quality on a <111> surface, likely as a results of densification of amorphous phase. On a <100> surface, however, hydrogen dilution leads to very poor lifetimes, as it increases the probability of epitaxial growth at the at the c-Si/a-Si:H hetero-interface, which is detrimental to the passivation quality. Different a-Si:H deposition conditions were used on the 3 texturing approaches, which have multiple crystal orientation at the c-Si/a-Si:H interface. A minority carrier lifetime of over 3 ms has been achieved for all texturing approaches after deposition of a 15 nm a-Si:H layer on both sides of the wafer.

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