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A 210 nW NPN-Based Temperature Sensor With an Inaccuracy of ±0.15 °C (3σ) From −15 °C to 85 °C Utilizing Dual-Mode Frontend

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***Abstract*—This letter describes an NPN-based temperature sensor that achieves a 1-point trimmed inaccuracy of ±0.15 °C (3σ) from −15 to 85 °C while dissipating only 210 nW. It uses a dual-mode frontend to roughly halve the power consumption of conventional frontends. First, two NPNs are used to generate a well-defined PTAT bias current, then this current is sampled and applied to the same NPNs to generate well-defined PTAT and CTAT voltages. These voltages are then applied to a low-power tracking ΔΣ modulator-based ADC, which employs a digital filter to efficiently generate a multibit representation of temperature. A prototype fabricated in a 180-nm BCD process achieves 15-mK resolution in a 50 ms conversion time, which translates into a state-of-the-art resolution FoM of 2.3 pJK^2.**

***Index Terms*—BJT, low leakage, low power, temperature sensor, temperature-to-digital converter.**

I. Introduction

Accurate temperature sensors are essential for many Internet of Things (IoT) applications. Since such applications are usually highly power and energy constrained, low-power sensors with high energy efficiency are required. In addition, to minimize calibration effort and cost, they should only require a 1-point trim.

Recently, sub-1μW MOSFET and resistor-based temperature sensors have been presented [1], [2], [3]. However, due to process spread, such sensors are relatively inaccurate after a 1-point trim or require a 2-point trim to achieve decent accuracy. BJT-based sensors can achieve higher accuracy after a 1-point trim, but they typically consume more power (>1 μW), which restricts their use in low-power temperature sensing applications. A current-to-frequency converter (CFC)-based temperature sensor using MOSFET subthreshold current [4] consumes only 860 nW while achieving ±0.4 °C inaccuracy after 1-point trim. But it requires an external 1-MHz reference clock, which results in additional power in a fully integrated design. By applying a zoom ADC, [5] presented a 600 nW, ±0.4 °C 1-point trimmed inaccuracy temperature sensor using dynamic threshold-voltage MOSFET (DTMOS) instead of BJTs. However, the complicated and power consuming digital controller for the zoom ADC was implemented externally.

This work, an extension of [6], describes a low-power, energy efficient, and high-accuracy NPN-based temperature sensor. It achieves an inaccuracy of ±0.15 °C (3σ) from −15 to 85 °C after a 1-point trim, and consumes only 210 nW thanks to the use of a power-efficient dual-mode frontend (DMFE) and a tracking ΔΣ modulator-based ADC.

II. Dual-Mode Frontend

A. Conventional Frontend

As shown in Fig. 1, the frontend (FE) of a BJT-based temperature sensor typically consists of two BJT-based circuits, a bias circuit, which generates a PTAT current I_{BIAS}, and a BJT core, which uses

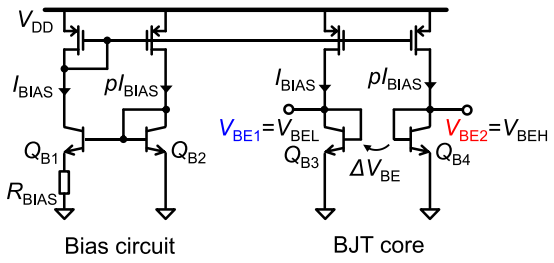

Fig. 1. Typical frontend of the BJT-based temperature sensor.

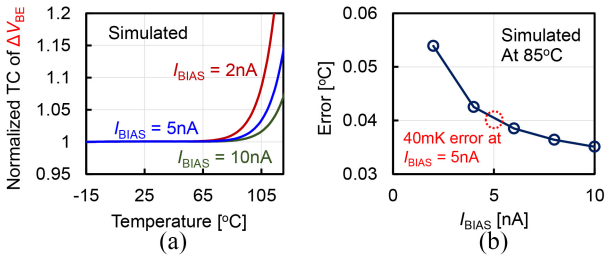

Fig. 2. (a) Simulated temperature coefficient of ΔV_{BE}. (b) Inaccuracy of analog FE at 85°C in a simulation.

copies of the bias current I_{BIAS} and $p \times I_{\mathrm{BIAS}}$ to generate well-defined CTAT (V_{BEL} and V_{BEH}) and PTAT ($\Delta V_{\mathrm{BE}} = V_{\mathrm{BEH}} - V_{\mathrm{BEL}} > 0$) voltages. This concept can be applied to both NPN-based and PNP-based FEs. The bias circuit and the BJT core will thus consume similar amounts of power. Although I_{BIAS} should be minimized for low-power operation, at low collector current densities and/or high temperatures, ΔV_{BE} will no longer be a linear function of temperature, leading to temperature errors. This is due to the BJT's finite current gain, n-well leakage, and finite saturation current I_{S} which all are nonlinear functions of temperature. With minimum-size (2 μm × 2 μm) NPNs in the intended 180-nm BCD CMOS process, reducing I_{BIAS} to nA-levels will result in significant ΔV_{BE} nonlinearity [Fig. 2(a)] and temperature errors [Fig. 2(b)]. Simulations show that I_{BIAS} must be greater than 5 nA at room temperature (RT) to ensure that the resulting nonlinearity is less than 0.04 °C at 85 °C. In this letter, V_{BE1} and V_{BE2} simply denote the name of the two outputs of the FE, and V_{BEL} and V_{BEH} denote the absolute voltage of the two CTAT outputs, respectively.

B. Proposed Dual-Mode Frontend

In this work, a single, reconfigurable circuit is used to generate I_{BIAS}, V_{BE} (V_{BEL} and V_{BEH}), and ΔV_{BE}, thus roughly halving the power of the FE. The simplified schematic of the proposed DMFE is shown in Fig. 3. During the initial precharge phase ($\Phi_{\mathrm{AFE}} = 1$), the circuit is configured as a bias circuit that uses two NPNs to generate PTAT currents I_{BIAS} and $p \times I_{\mathrm{BIAS}}$. These currents are then sampled by storing the gate voltage of $M_{\mathrm{A,B}}$ on a capacitor C_{S}. During the conversion phase ($\Phi_{\mathrm{AFE}} = 0$), the FE is configured as a BJT core in which the sampled currents are used to generate V_{BEL}, V_{BEH}, and ΔV_{BE}. Base-current errors are mitigated by the NPN's relatively high current gain ($\beta > 60$ over −15 °C to 85 °C) without

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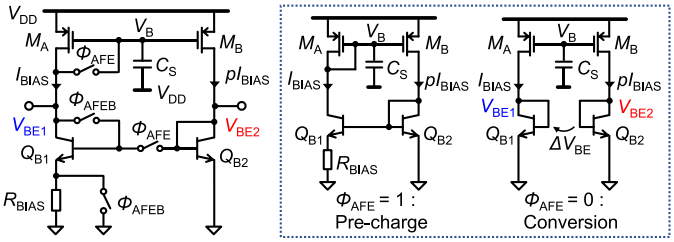

Fig. 3. Simplified schematic and concept of DMFE.

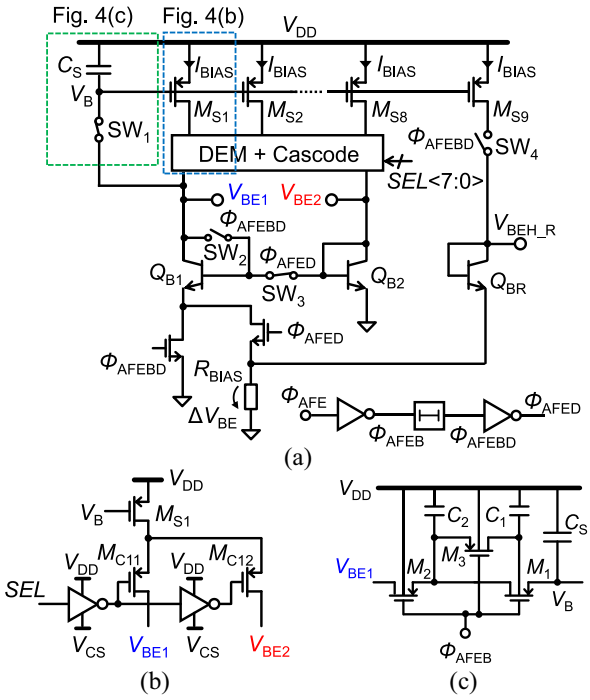

Fig. 4. (a) Schematic of DEFE, (b) cascode combined with DEM switch, and (c) sample and hold circuit based on a passive bootstrap switch.

applying a β compensation. Since the precharge phase is much shorter (2 ms) than the total conversion time (50 ms), the average power consumption of the DMFE is roughly half of a conventional FE.

Fig. 4(a) shows the detailed schematic of the DMFE. A current mirror ratio $p = 7$ is chosen as a compromise between DMFE power, resolution, and accuracy. Furthermore, all the NPNs are minimum-size (2μm $\times$ 2μm) to minimize I_S and, thus, maximize the linearity of V_{BE1} and V_{BE2} at high temperatures. An accurate 1:7 current ratio is achieved by applying dynamic element matching (DEM) to current sources M_{S1-8}. A resistor $R_{BIAS} = 10$ MΩ sets $I_{BIAS} = 5$ nA at RT. As shown in Fig. 4(b), the cascodes of the current sources are reused as DEM switches, thus halving the number of MOSFETs, and thus the number of leakage current sources in the bias current paths.

As shown in Fig. 4(c), a bootstrapped sampling switch SW_1, consisting of M_{1-3} and two sampling capacitors $C_{1,2}$ (1pF) is used to limit the leakage of the sampled gate voltage due to the off-resistance and bulk of the main switch M_1. C_S is then set to 5 pF, which reduces temperature errors due to the residual leakage to less than 10 mK. During the conversion phase ($\Phi_{AFE} = 0$), a dummy BJT Q_{BR} is biased at I_{BIAS} to generate a replica of V_{BEH} ($= V_{BEL} + \Delta V_{BE}$). This is used to bias the drain/source and bodies of the pMOSFETs sampling switches used in the ADC, as will be discussed later.

III. Tracking ΔΣ Modulator Topology

A. Conventional ΔΣADC-Based Temperature Sensor

To realize BJT-based temperature sensors with high energy efficiency, zoom ADCs, which digitize $X = V_{BE}/\Delta V_{BE}$, have been

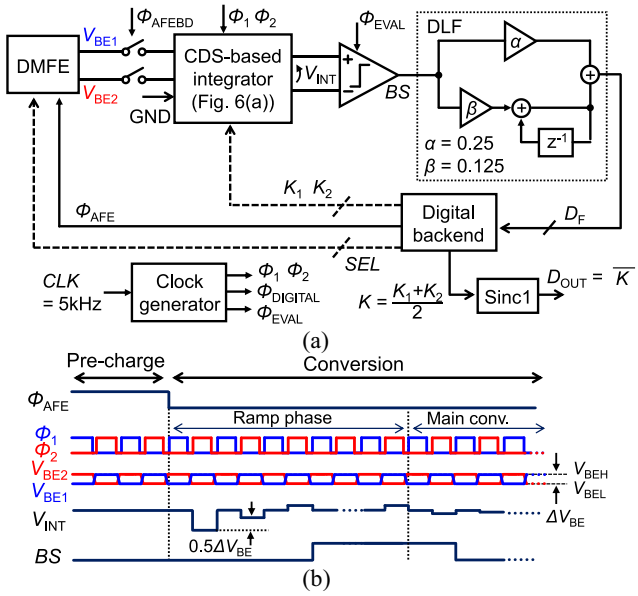

Fig. 5. (a) Block diagram of entire temperature sensor. (b) Timing diagram.

proposed [7]. By combining a coarse SAR ADC and a fine ΔΣ modulator, the modulator's reference voltage can be reduced to ΔV_{BE}, thus reducing the number of ΔΣ cycles required to achieve a certain resolution. In addition, the required swing and linearity of the loop filter is greatly relaxed, leading to lower power consumption. However, to suppress SAR ADC errors, zoom ADCs often employ over-ranging, which increases the reference voltage to $2\Delta V_{BE}$ [5] or $3\Delta V_{BE}$ [7]. As a result, the required cycles per conversion and the loop filter power increase accordingly. Furthermore, the two-step approach requires a complicated and power-consuming digital controller.

B. Proposed Tracking ΔΣ Modulator

In this work, we propose the use of a low-power tracking ΔΣ modulator [8]. Like a zoom ADC, it digitizes $X = V_{BEL}/\Delta V_{BE}$ but does not require over-ranging. Also, its digital controller is much simpler, as it only requires the implementation of a digital filter.

Fig. 5(a) and (b) shows a simplified block diagram of the proposed tracking ΔΣ modulator and its timing diagram, respectively. It employs a correlated double sampling (CDS)-based 1st integrator followed by a comparator and a digital loop filter (DLF) [9], whose multibit output drives the DAC. The output of the DMFE is then efficiently digitized by a charge-balancing scheme that adjusts the gain $K = (K_1 + K_2)/2$ of a switched-capacitor (SC) DAC so that $K \times \Delta V_{BE} = V_{BEL}$ on average, where K_1 and K_2 are the gains of the two DAC halves, respectively. After decimation, the output of the ADC is obtained as $D_{OUT} = V_{BEL}/\Delta V_{BE}$. The CDS-based integrator drives a latched comparator via a preamplifier, which consists of a pMOS differential pair with a latch load. After an initial reset at $\Phi_{AFE} = 1$, the DLF output will ramp to the average value of K and then start toggling. The ramp phase takes 25 cycles, which is much less than the 250 cycles required for a full conversion. Compared to a zoom ADC, the single-mode operation of the tracking modulator results in a simpler and lower power controller. However, since its quantization noise is only 1st-order shaped, this comes at the expense of resolution. This problem is mitigated by independently controlling the gains of the two halves of the SC DAC, thus effectively doubling its resolution.

As in [5], the OTA's offset is mitigated by CDS as shown in Fig. 6(a). During each ΔΣ cycle, the DAC injects $2C_{DAC}V_{BEL}$ and a differential charge $-(K_1+K_2) \times C_{DAC}\Delta V_{BE}$ into the integrator. The variation in the integrator is expressed as

$$\Delta V_{INT} = 2\frac{C_{DAC}}{C_{INT}}\left(V_{BEL} - \frac{K_1 + K_2}{2}\Delta V_{BE}\right). \quad (1)$$

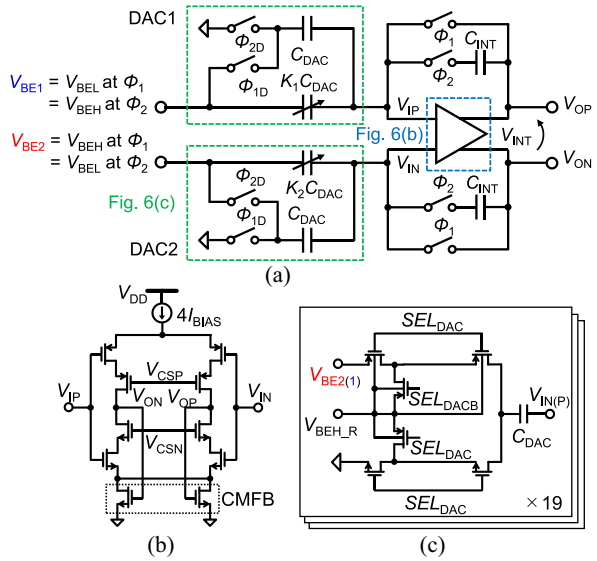

Fig. 6. Schematics of (a) CDS-based integrator, (b) OTA, and (c) unit cell of DAC.

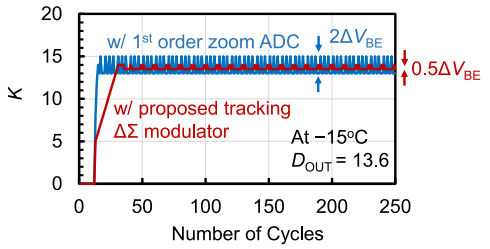

Fig. 7. K versus number of cycles in simulation.

In this work, the two halves of the DAC may have two different gains, a gain of $N = K_1 = K_2$, or a gain of $N + 0.5$, which is obtained by alternating between $K_1 = N$ and $K_2 = N + 1$, and $K_1 = N + 1$ and $K_2 = N$. Thus, the LSB step of the DAC is reduced to $0.5\Delta V_{BE}$ and its resolution is doubled. Although this results in an alternating $\pm 0.5\Delta V_{BE}$ common-mode (CM) variation, the resulting CM swing at the integrator output will be rejected by the differential comparator.

Fig. 7 compares the simulated output K of the proposed tracking $\Delta\Sigma$ modulator with that of a 1st-order zoom ADC with $2\Delta V_{BE}$ over-ranging. Compared to the zoom ADC, the proposed tracking $\Delta\Sigma$ modulator has 4 × less DAC swing. As shown in Fig. 6(b), this allows the 1st integrator to be realized as an energy-efficient current-reuse OTA operating from a 1.2-V supply. With $C_{INT} = 2C_{DAC} \approx 120$ fF, the worst case output swing (at 85 °C) is ±90 mV. The OTA has two operating phases. During Φ_1, its input and output are shorted and its operating point and offset are stored on C_{DAC}. During Φ_2, it is configured as an integrator and charge is transferred into C_{INT}. Its gain (>82 dB) is high enough to ensure that temperature-sensing errors due to gain variation and nonlinearity are well below 100 mK over the intended temperature range.

Each half of the SC DAC is implemented by 19-unit cells shown in Fig. 6(c), which consist of sampling switches and a sampling capacitor C_{DAC}. Switch leakage then becomes a major challenge because it alters the bias currents of the NPN diodes and causes temperature sensing errors. In contrast to [5], the number of switches per capacitor is halved by swapping the bias currents of the NPN diodes in the DMFE to create a ΔV_{BE} step that is transferred to the integrator at each cycle as shown in Fig. 5(b). In addition, pMOS/nMOS T-switches [10] are used to minimize switch leakage. Body and drain/source leakage is minimized by connecting them to the replica bias voltage V_{BEH_R}, which is generated in the DMFE [Fig. 4(a)]. When the switches are "off," their mid-points are also connected to V_{BEH_R}, thus minimizing leakage via their off resistances. Compared to using $V_{DD}/2$ as the bias voltage [10], using V_{BEH_R} minimizes the voltages across the reverse-biased drain and source diodes, thus reducing switch leakage. These measures ensure that the total leakage current drawn from the DMFE is less than 3 pA in simulation, which corresponds to a temperature error of only 20 mK. Monte Carlo simulations show that the sensor achieves an inaccuracy of ±0.2°C (3σ) from −40 to 85°C.

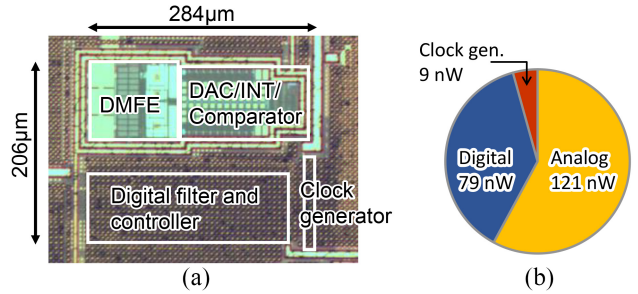

Fig. 8. (a) Chip photograph of the proposed temperature sensor. (b) Breakdown of the power consumption.

Fig. 9. (a) Capture of conversion time versus I_{BIAS} and (b) its enlarged picture.

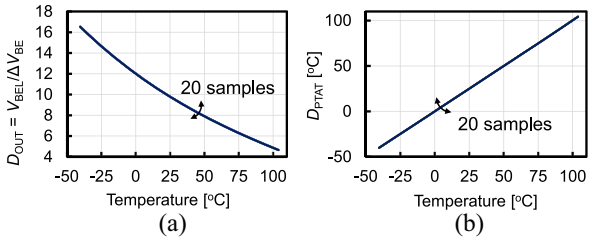

Fig. 10. (a) Measured output and (b) replicated temperature among 20 dies.

IV. Measurement Results

As shown in Fig. 8(a), the proposed temperature sensor occupies a core area 0.058 mm^2 in a 180-nm BCD process, The digital controller and the DLF are synthesized with cells from a standard digital library. $R_{BIAS} = 10$ MΩ is a high resistance poly resistor, which occupies 1.5% of the total area. For flexibility, the 1st-order sinc decimation filter is implemented off-chip. With a 1.25-V supply and a 5-kHz system clock, the sensor consumes 210 nW at RT, with 121/79/9 nW consumed in the analog core, the digital controller, and the clock generator, respectively, as shown in Fig. 8(b). The line sensitivity is 0.07 °C/V for supply voltages ranging from 1.2 to 1.8 V. The variation of I_{BIAS} during a conversion is shown in Fig. 9. The charge injection of SW_1 in Fig. 4(a) causes an equivalent error of 30 mK during the transition from the precharging phase ($\Phi_{AFE} = 1$) to the conversion phase ($\Phi_{AFE} = 0$). At 85 °C, the leakage-induced droop of V_B causes less than 10-mK error in a 100-ms conversion time.

Twenty samples in ceramic DIL packages from one batch were tested in an oven. A Pt-100 is used as a reference sensor. The decimated bitstream output and the linearized result [5,7] are shown in Fig. 10. The sensor achieves an untrimmed inaccuracy of ±0.4 °C (3σ) from −15°C to 85°C [Fig. 11(a)]. After applying a 1-point

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED LOW POWER TEMPERATURE SENSORS

	This work		Zhang [11]	Xin [2]	Souri [5]		Tang [4]	Park [12]
Sensor type	**BJT**		BJT	Resistor	DTMOS		MOS	MOS + BJT
Process [nm]	**180**		180	65	160		55	180
Area [mm²]	**0.058**		0.18	0.06	0.085		0.0024	0.12
Fully integrated	**Yes**		Yes	Yes	Ext. digital-backend		Yes	Ext. 20nF cap.
Power [nW] (Supply V_{DD})	**210 (1.25V)**		720 (1.0V)	488 (1.0V)	600 (0.85V)		860 (0.8V)	0.49 (1V)
Temp. [°C]	**−15–85**		0–100	0–100	−40–125		−40–85	−10–100
Error [°C]	**±0.4*¹**	**±0.15*¹**	±0.2*¹	−1.1/1.5*²	±1.0*¹	±0.4*¹	±0.4*¹*³	±2.4*¹
Trim Point	**0**	**1**	1	1	0	1	1	1
# of samples	**20**		15	12	16		32	15
R-IA [%]	**0.8**	**0.3**	0.4	2.6	1.3	0.5	0.5	4.3
Resolution [mK]	**15**		40	610	63		17	590
Conv. time [ms]	**50**		40	0.01	6		1	200
FoM [pJ·K²]	**2.3**		46	1.8	14		0.26	34
PSS [°C/V] (V_{DD} range)	**0.07 (1.2–1.8V)**		N/A	N/A	0.45 (0.85–1.2V)		5.8 (0.8–1.3V)	1.1 (1.0–2.1V)

*¹ 3σ inaccuracy *² Peak-to-peak inaccuracy *³ Master curve fitting is applied.

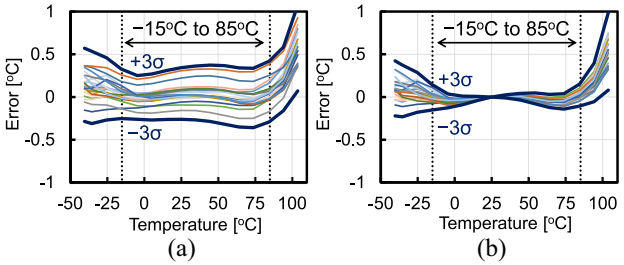

Fig. 11. Measured inaccuracy among 20 dies (a) w/o trim (b) w/ 1-point trim.

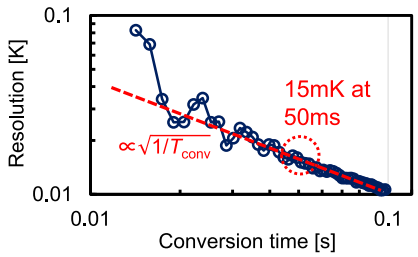

Fig. 12. Measured resolution versus conversion time.

offset trim, this improves to ±0.15 °C (3σ), which corresponds to a relative inaccuracy (R-IA) of 0.3 % [Fig. 11(b)]. As expected from the simulation results in Fig. 2, the sensor's output becomes nonlinear at high temperatures (>85 °C), while at low temperatures, it exhibits more spread as I_{BIAS} and the gain of the OTA decrease. Fig. 12 shows the measured resolution versus conversion time at multiples of the current-mirror DEM period. The sensor achieves a thermal-noise limited resolution of 15 mK (RMS) in a 50-ms conversion time.

Table I summarizes the performance of the proposed sensor and compares them with those of other sub-μW temperature sensors utilizing only 1-point trim. The proposed sensor consumes 2.9 × less power than [5], which does not have an on-chip controller, and 4 × less power than [4], which requires extra power related to generating a relatively high frequency of 1-MHz reference. Also, its R-IA is more than 8 × better than [2] and competitive with that of [4]. Moreover, it achieves a 15-mK resolution in 50 ms, which translates into a state-of-the-art resolution FoM of 2.3 pJK².

V. CONCLUSION

In this work, an NPN-based temperature sensor with a 1-point trimmed inaccuracy of ±0.15 °C (3σ) from −15 to 85°C has been presented. It employs a DMFE that effectively halves its power consumption by using two NPNs to generate a precision PTAT current, which is then sampled and applied to the same NPNs to generate well-defined CTAT and PTAT voltages. A tracking ΔΣ modulator-based temperature-to-digital converter was used to further reduce its power consumption. A test chip fabricated in a 180-nm BCD process dissipates 210 nW at RT. It achieves 15-mK resolution in a 50-ms conversion time, which corresponds to a 2.3-pJK² resolution FoM. These results showed that the proposed temperature sensor combines ultralow power with good accuracy and is thus suitable for use in low-power IoT applications.

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