Electrical Modeling of Perovskite Solar Cells

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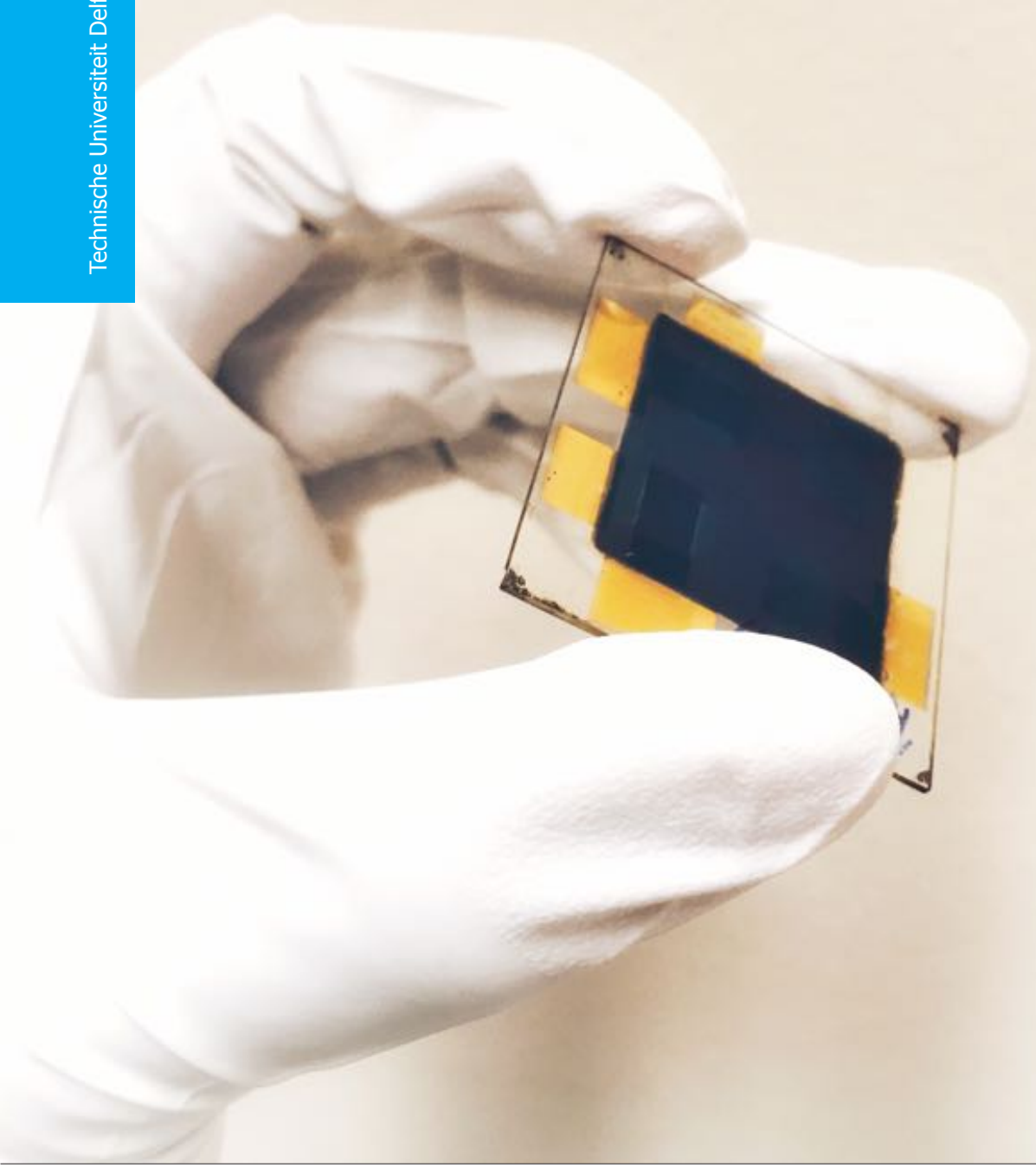

TU Delft Delft University of Technology

Challenge the future

Electrical Modeling of Perovskite Solar Cells

by

E. R. Evasari

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SOLAR RESEARCH SOLLIANCE

Abstract

High-performance perovskite solar cells (PSCs) have attracted great attention from researchers around the world. Rapid researches and developments of PSCs are shown by the increase of its efficiency from 3.8% in 2009 to a new world record of 22.4% in 2017. Hysteresis phenomenon in current density-voltage (J-V) is one of the challenges occurring in some specific PSCs that should be overcome to continue the improvement of PSCs. This phenomenon occurs when a voltage is swept with different scan directions from negative to positive value (forward) and positive to negative value (backward). Hysteresis effect results in a different maximum power point on the J-V characteristic leading to under- or overestimation of PSCs efficiency.

Furthermore, when the applied voltage is abruptly changed, a transient current density response is introduced implying a capacitive behaviour. Due to this behaviour, there is an indication that PSCs cannot be represented by the conventional equivalent circuit. Thus, the purpose of this project is to investigate hysteresis phenomenon in PSC by electrical modelling. In this project, a PSC sample was fabricated by Solliance Solar Research. Time-resolved J-V measurement was done to obtain more insight of J(t) as a function of applied voltage. The hysteresis phenomenon was analyzed in different voltage scan direction and various scan rates. Simulation of band diagram in dark condition was done to understand working principle of PSC device. Two predicted equivalent circuit of the cell were derived from the simulated band diagram. These equivalent circuit models considered the charge accumulation at the bulk of perovskite and at the interface between charge transport layers and perovskite. Furthermore, two additional equivalent circuit models were proposed to represent the hysteresis effect. J(t) curve fitting of measurement results and simulation was employed to verify the equivalent circuit. This insight might help to get a better understanding of hysteresis effect in PSCs.

Preface

I would like to express my gratitude to Olindo Isabella as my main supervisor who gave me an opportunity to take this master thesis under his supervision. I thank him for his help and advice through the process of this thesis project. My profound appreciation goes to my daily supervisors, Rudi Santbergen and Nasim Rezaei, for their supervision and patience to help me during my thesis period. They helped me to understand some new concepts and assisted me when I found bottlenecks. I thank them for all the fruitful discussions when we had a meeting or when I directly passed by their office. Also, for Nasim, thanks for sharing the Iranian snacks and for Rudi, thanks for accompanying me to travel to Solliance, Eindhoven, at the beginning of this thesis project.

My gratitude also goes to Miro Zeman and Tom Savenije for their willingness to be my graduate committee. I would also like to thank Dong Zhang for his attendance at my thesis defence. He also helped me to get the perovskite solar cells. I thank him for all discussions through email or when I went to Solliance, Eindhoven. Furthermore, I would also like to thank Remko Koornneef for his help on Wacom that made the time-resolved I-V measurement possible. My appreciation also goes to Stefaan Heirman and Martijn Tijssen as the technicians of PVMD group who assisted me for the measurements. My sincere gratitude is to Rene van Swaaij, Arthur Weber, Gianluca Limodio, and Paul Procel for the valuable discussions. For all PVMD group members, thank you for your feedback and suggestions to my thesis.

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List of Figures

1.1 Renewable electricity growth [1]. . . . 1
1.2 Efficiency record of various PV Technologies [2]. . . . 2
1.3 The crystal structure of perovskite in 3D. . . . 3
1.4 The sandwiched layers of PSCs for (a) ETL-perovskite-HTL and (b) HTL-perovskite-ETL planar structure. . . . 4
1.5 An illustration of PSC sample from Solliance Solar Research. . . . 5
1.6 The transient slow response of current density in response to staircase voltage sweep as function of time by (a) forward and (b) reverse scan [3]. . . . 7
1.7 The equivalent circuit of a solar cell with (a) a single diode and (b) with double diodes in parallel. . . . 7
1.8 Equivalent circuit model with double diodes in series [4]. . . . 9
1.9 Equivalent circuit model of PSCs with additional capacitor and resistor [5]. . . . 10
1.10 Equivalent circuit model of inverted PSCs with two photodiodes and Schottky diode [6]. 10
1.11 Equivalent circuit model of inverted PSCs with two photodiodes and capacitors [7]. . . . 11
1.12 Flow diagram of methodology in this study. . . . 12

2.1 The illustration of band diagram of PSC (a) in dark condition and (b) under illumination [8]. . . . 14
2.2 The flowchart of basic simulation process with Sentaurus TCAD [9]. . . . 14
2.3 The simulated band diagram of PSC sample using Sentaurus TCAD. . . . 16
2.4 The illustration of charge carriers transport in PSC. . . . 17
2.5 Band diagram of device for CBO calculation[10]. . . . 18
2.6 Band diagram of device for VBO calculation [10]. . . . 19
2.7 Positive and negative CBO [10]. . . . 19
2.8 Positive and negative VBO [10]. . . . 20
2.9 An illustration of charge accumulation [11]. . . . 21
2.10 Equivalent circuit of PSC with one capacitor. . . . 22
2.11 An illustration of a complete equivalent circuit of a capacitor [12]. . . . 22
2.12 Equivalent circuit of PSC with two capacitors. . . . 23

3.1 The schematic illustration of PSC sample and the mask. . . . 25
3.2 An illustration of voltage steps used in the measurement. . . . 26
3.3 The J-V curve of forward and backward scan of PSC sample. . . . 27
3.4 The J-V characteristic with various scan rates of (a) forward and (b) backward scan direction. . . . 28
3.5 Hysteresis constant as a function of scan rates. . . . 29
3.6 The J-V characteristic as a function of time of (a) forward and (b) backward scan direction. 29
3.7 An illustration of a transient current density response *J(t)* of a certain voltage step. . . . 30
3.8 Time constant of each voltage step measured at (a) forward and (b) backward scan direction; distribution of time constant of (c) forward and (d) backward scan. . . . 31
3.9 Distribution of steady-state current density of (a) forward and (b) backward scan. . . . 32
3.10 A transient current density response of a voltage step with various Δt. . . . 32
3.11 C-V characteristic of (a) forward and (b) backward scan. . . . 33
3.12 The schematic diagram of C-V characteristics [13]. . . . 33

4.1 The graphical user interface of QUCS. . . . 36
4.2 An illustration of voltage source creation of forward scan with first approach manual method: (a) voltage pulses and (b) a staircase voltage source. . . . 37

4.3 An illustration of voltage source creation of forward scan with second approach manual method: (a) voltage pulses and (b) a staircase voltage source. 37
4.4 A schematic diagram of simulation process. 39
4.7 The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit with one capacitor. 39
4.5 A schematic overview of equivalent circuit with one capacitor. 40
4.6 J-V curve obtained from simulation. 40
4.8 A schematic overview of equivalent circuit with two capacitors. 41
4.9 The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit with two capacitors. 42
4.10 A schematic overview of equivalent circuit from a literature. 43
4.11 The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit from literature. 43
4.12 A schematic illustration of equivalent circuit of scenario 4. 44
4.13 The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit of scenario 4. 45

List of Tables

4.1 Parameters values of equivalent circuit with one capacitors 40
4.2 Parameters values of equivalent circuit with two capacitors 42
4.3 Parameters values of equivalent circuit of scenario 3 44
4.4 Parameters values of equivalent circuit of scenario 4 45

A.1 Thickness of materials 55
A.2 Doping concentration 55
A.3 Parameter of ITO 55
A.4 Parameter of NiO nanoparticles 56
A.5 Parameter of Perovskite 56
A.6 Parameter of PCBM 56
A.7 Parameter of ZnO nanoparticles 56
A.8 Parameter of Au 56

Glossaries

List of Acronyms

1D	One-dimensional
2D	Two-dimensional
2-T	Two-terminal
3D	Three-dimensional
3-T	Three-terminal
4-T	Four-terminal
AC	Alternating Current
AM	Air Mass
a-Si	Amorphous Silicon
CBO	Conduction Band Offset
CdTe	Cadmium Telluride
CIGS	Copper Indium Gallium Diselenide
c-Si	Crystalline Silicon
DC	Direct current
EQE	External Quantum Efficiency
ETL	Electron Transport Layer
FA	Formamidinium
FF	Fill Factor
FTO	Fluorine-doped Tin Oxide
GaAs	Gallium Arsenide
GBs	grain bourndaries
GUI	Graphical User Interface
GW	Gigawatts
HTL	Hole Transport Layer
IEA	International Energy Agency
ITO	Indium Tin Oxide
LC	Lethal Concentration
LCA	Life Cycle Analysis
MA	Methylammonium
MPP	Maximum Power Point
NiO	Nickel Oxide
PCBM	Phenyl-C61-Butyric acid Methyl ester
PCE	Power Conversion Efficiency
PSC	Perovskite Solar Cell
PV	Photovoltaics
QUCS	Quite Universal Circuit Simulator
RH	Relative Humidity
SBD	Schottky Barrier Diode
SDE	Structure Device Editor
SQ	Shockley-Quisser
TCAD	Technology Computer-Aided Design
TCO	Transparent Conductive Oxide
VBO	Valence Band Offset
ZnO	Zinc Oxide

List of Symbols

C	Capacitance
D_n	Electron diffusion coefficient
D_p	Hole diffusion coefficient
E	Electric field
E_c	Conduction band level
E_{F0}	Fermi level at thermal equilibrium
E_{Fn}	Quasi-Fermi level of electrons
E_{Fp}	Quasi-Fermi level of holes
E_G	Bandgap energy
E_v	Valence band level
E_{vac}	Vacuum level
ε	Permittivity of the materials
G	Generation
J	Current Density
$J(t)$	Current density as a function of time
J_o	Saturation current density
J_{ph}	Photo-generated current density
J_{sc}	Short circuit current density
J_{ss}	Steady-state current density
k_B	Boltzmann's constant
μ_n	Electron mobility
μ_p	Hole mobility
n	Ideality factor
P_{max}	Peak power
ρ	Volume charge density
q	Elementary charge
R	Recombination
R_p	Shunt resistance
R_s	Series resistance
t_0	Starting time
τ	Time constant
V	Voltage
V_{bi}	Built-in voltage
V_{oc}	Open circuit voltage
φ	Work function
χ	Affinities

Contents

Abstract iii

Preface v

List of Figures vii

List of Tables ix

Glossaries xi

1 Introduction 1
- 1.1 Background . . . 1
- 1.2 Perovskite Solar Cell . . . 2
  - 1.2.1 Perovskite material . . . 2
  - 1.2.2 Device Architecture . . . 3
- 1.3 Issues in Perovskite Solar Cells . . . 5
  - 1.3.1 Toxicity issue . . . 5
  - 1.3.2 Stability and scale-up issues . . . 6
  - 1.3.3 Hysteresis phenomenon . . . 6
- 1.4 Existing Researches . . . 8
  - 1.4.1 Optical model . . . 8
  - 1.4.2 Optoelectronic model . . . 8
  - 1.4.3 Equivalent circuit model . . . 9
- 1.5 Research gap . . . 11
- 1.6 Objective and Research questions . . . 11
- 1.7 Methodology . . . 12
- 1.8 Report structure . . . 12

2 Investigation of Band Diagram 13
- 2.1 Theoretical Working Principle of PSC device . . . 13
  - 2.1.1 Dark condition . . . 13
  - 2.1.2 Under illumination . . . 13
- 2.2 Simulation of the Band Diagram . . . 14
  - 2.2.1 Sentaurus Workbench . . . 14
  - 2.2.2 Sentaurus Structure Editor (SDE) . . . 15
  - 2.2.3 SNMESH . . . 15
  - 2.2.4 SDEVICE . . . 15
- 2.3 Analysis of Simulated Band Diagram . . . 15
  - 2.3.1 Band offset . . . 16
  - 2.3.2 Junction between two materials . . . 17
- 2.4 Predicted Equivalent Circuit of PSC . . . 20
  - 2.4.1 Equivalent Circuit with One Capacitor . . . 21
  - 2.4.2 Equivalent Circuit with Two Capacitors in Parallel . . . 21
- 2.5 Conclusion . . . 22

3 Time-resolved I-V measurement 25
- 3.1 Experimental setup . . . 25
- 3.2 Experimental Result . . . 26
  - 3.2.1 J-V characteristic . . . 26
  - 3.2.2 Transient response on J-V curve as a function of time . . . 28
  - 3.2.3 C-V characteristic . . . 32
- 3.3 Conclusion . . . 34

4 Electrical Modeling **35**
4.1 Equivalent Circuit Simulation with QUCS . . . 35
4.1.1 Introduction of QUCS . . . 35
4.1.2 Voltage Source Creation . . . 35
4.1.3 Transient Simulation . . . 38
4.2 Simulation Integration of QUCS and Matlab . . . 38
4.2.1 Exporting Equivalent Circuit parameters from QUCS to Matlab . . . 38
4.2.2 *J(t)* curve fitting method . . . 38
4.3 Scenario 1: Equivalent Circuit with One Capacitor . . . 38
4.3.1 *J(t)* curve Fitting of Forward and Backward scan with Voltage Increment of 50 mV . . . 38
4.4 Scenario 2: Equivalent Circuit with Two Capacitors . . . 41
4.4.1 *J(t)* curve Fitting of Forward scan with Voltage Increment of 50 mV . . . 41
4.5 Additional equivalent circuit design of PSC device . . . 42
4.5.1 Scenario 3: Equivalent Circuit based on a Reference Paper . . . 42
4.5.2 Scenario 4: Simulation of Equivalent Circuit Combination of Scenario 1 and 3 . . . 44
4.6 Analysis of Saturation Current and Ideality Factor . . . 45
4.7 Discussion . . . 46
4.8 Conclusion . . . 46

5 Conclusions and Recommendations **47**
5.1 Conclusions . . . 47
5.1.1 Simulation of Band Diagram of PSC device . . . 47
5.1.2 Hysteresis phenomenon in PSC sample . . . 48
5.1.3 Electrical modelling of equivalent circuit . . . 48
5.2 Recommendations . . . 49
5.2.1 Measurement . . . 49
5.2.2 Simulation . . . 49

Bibliography **51**

A Device Parameters for Simulation of Band Diagram of PSC **55**
A.1 Input of Sentaurus Structure Editor . . . 55
A.2 Input of Sentaurus Structure Device . . . 55

1

Introduction

1.1. Background

Renewable energy becomes an alternative solution for fossil fuels towards the increase of energy consumption, mainly in electricity. As electricity is a fundamental human need, it is important to find sustainable energy sources. These renewable energy sources are derived from wind, solar, biomass, hydro, waves, etc. The growth of renewable electricity by technology is depicted in Figure 1.1 where the growth in 2017-2022 is obtained by forecasting [1]. A study by the International Energy Agency (IEA) has found a remarkable growth of solar energy capacity in 2016 achieving annual growth of over 74 gigawatts (GW) and exceeding the growth of coal. Furthermore, they predicted a more optimistic forecast, expecting 80% of world renewable electricity capacity of 920 GW will come from solar energy by 2022 [1]. In other words, it is expected that for the next five years more researches and developments will deliver innovations and ideas towards photovoltaic technologies and systems. The optimistic forecasting can compensate the global ambition in diminishing CO_2 emission. It can be achieved by generating the renewable energy of 25,000 GW by 2050 [14].

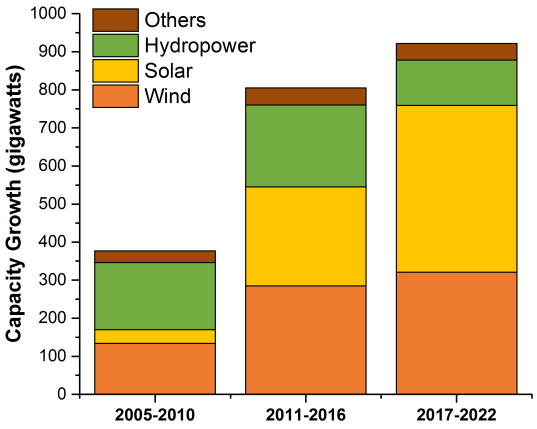


Figure 1.1: Renewable electricity growth [1].

The heart of converting solar energy into electricity lies in a semiconductor-based device called solar cell. When a solar cell is illuminated by sunlight, it directly converts the light into electricity. This process is commonly known as the photovoltaic effect. However, not all the sunlight that illuminates the cell will be converted into electricity. It can also be lost as heat. The efficiency of the converted sunlight is indicated as power conversion efficiency (PCE). The maximum theoretical limit of PCE is described

as Shockley-Quisser (SQ) limit [15]. However, this SQ limit was measured for inorganic solar cell, thus, it is not valid for the organic solar cell [5]. PCE depends on several factors, such as the temperature of the cell, the intensity of the light, and PV technologies. Various PV technologies have been introduced since the first photovoltaic effect was discovered in 1839 by Alexandre-Edmond Becquerel [16]. The wafer-based solar cell has been well-developed in decades. In 2017, silicon-wafer based technology has dominated the PV market for about 95% of the total production. The remaining 5% of the market share was from thin film technologies which consist of amorphous silicon (a-Si), cadmium telluride (CdTe), and copper indium gallium diselenide (CIGS) [17].

The intense research and development have lead researchers to discover novel thin film technologies. One of them is perovskite solar cells (PSCs). In recent years, the emergence of organometal halide PSCs drives a great allure for the researchers to improve the PCE. The PCE of PSCs has increased from its initial value of 3.8% in 2009 to a new world record of 22.4% in 2017, achieved by Korean Research Institute of Chemical Technology [18]. The rapid increase of PCE of 18.6% in 8 years exhibits a steep learning curve of PSCs. This can be seen from Figure 1.2 that shows the rapid development of PSCs comparing to other PV technologies. Additionally, several studies have reported that PSCs suffer from some issues that should be overcome to improve the efficiency of the cells. These issues are the stability towards humid condition and temperature increases, scale-up issue, and hysteresis phenomenon [14]. The latest issue leads to under- or overestimation of yielded PCE when the voltage is applied to the cell but the current response is slow [3]. The physical mechanism for this phenomenon is not fully understood yet. Thus, the focus of this study is to investigate the hysteresis effect in PSC using electrical simulations. Further detailed explanation of hysteresis phenomenon will be discussed in subsection 1.2.1.

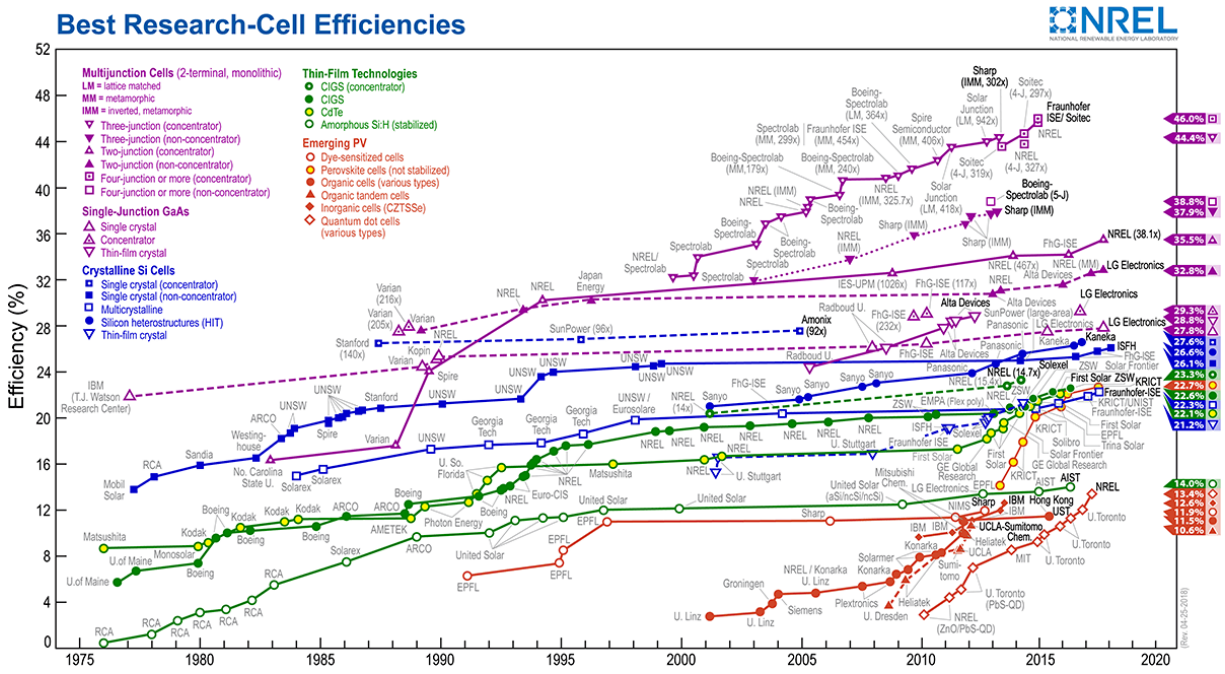


Figure 1.2: Efficiency record of various PV Technologies [2].

1.2. Perovskite Solar Cell

1.2.1. Perovskite material

Perovskites are organic-inorganic hybrid materials that have attracted great attention from researchers around the world. The general chemical formula of perovskite is ABX_3, where A and B are cations and X is an anion, depicted in Figure 1.3. A represents monovalent organic cation, i.e. methylammonium (MA) or formamidinium (FA) whose chemical formula is $CH_3NH_3^+$ and $CH(NH_2)_2^+$, respectively. B expresses metal cation, such as Pb(II) or Sn(II), while X denotes halide (i.e Cl^-, Br^-, or I^-) [19]. The first emergence of organic-inorganic lead halide perovskite as solar cell has been reported by Miyasaka and

co-workers in 2009 in the form of $MAPbI_3$ ($CH_3NH_3PbI_3$) or $MAPbBr_3$ ($CH_3NH_3PbBr_3$) [20]. However, these types of PSCs suffer from stability issue due to the moisture and rise of temperature. The organic cations are hydrophobic which is remarkably sensitive to the humid condition. On the other side, the increase of temperature induces the phase transition. A study by Ye and co-workers found that stable tetragonal phase of $MAPbI_3$ at room temperature experienced phase transition to the cubic phase when temperature increased to above 55°C [21]. This issue might be significant when the solar cell is measured under illumination for a period of time. Furthermore, researchers mixed the ions into material of perovskite to achieve more stable and high efficiency perovskite, for instance, $CH_3NH_3PbI_{(3-x)}Cl_x$, $CH_3NH_3PbI_{(3-x)}Br_x$ [14], and $FA_xMA_{(1-x)}PbBr_yI_{(1-y)}$ [22].

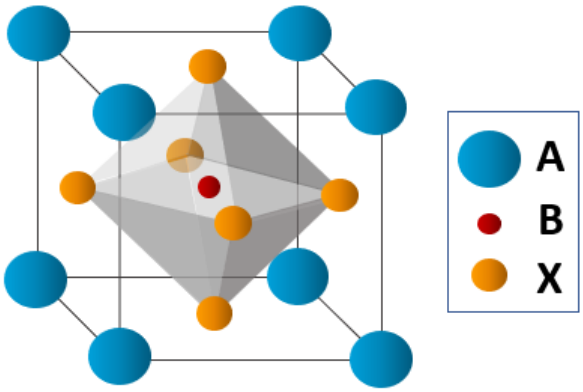


Figure 1.3: The crystal structure of perovskite in 3D.

Researchers in the solar cell society are interested in perovskite due to its several desirable properties, i.e. high carrier mobilities, high absorption coefficient, and long charge carrier diffusion length [14]. Ziang and co-workers reported the comparison of the absorption coefficient between perovskite and three other materials [23]. Perovskite has higher absorption coefficient than the c-Si material in the visible light range (400-700 nm). It is close to the absorption coefficient of GaAs material which has direct band gap. In addition, a study reported that the carrier lifetime of $CH_3NH_3PbI_3$ is approximately hundred nanoseconds up to microseconds. Consequently, it results in long charge carrier diffusion length [24]. Hence, the longer carrier lifetime will result in longer carrier diffusion length. The potential of perovskites to be scaled up to an industrial level is another advantage that gives a promising contribution to the large-scale electricity generation in the future.

1.2.2. Device Architecture

Studies have shown that PSCs architectures can be mesoporous or planar [25]. In this project, we will only focus on the planar configuration. In this configuration, the hole transport layer (HTL), perovskite absorber layer, and the electron transport layer (ETL) are stacked in several layers as shown in Figure 1.4. When the absorber layer absorbs the photon from incident light, the created charge carriers go to HTL and ETL, respectively. Subsequently, HTL will transport holes from the absorber layer to the respective electrode, whereas ETL will transport electrons from the absorber layer to the related electrode [26]. These transport layers could surpress the losses due to recombination [5]. The detailed explanation of charge carrier transport in PSC will be provided in Chapter 2.

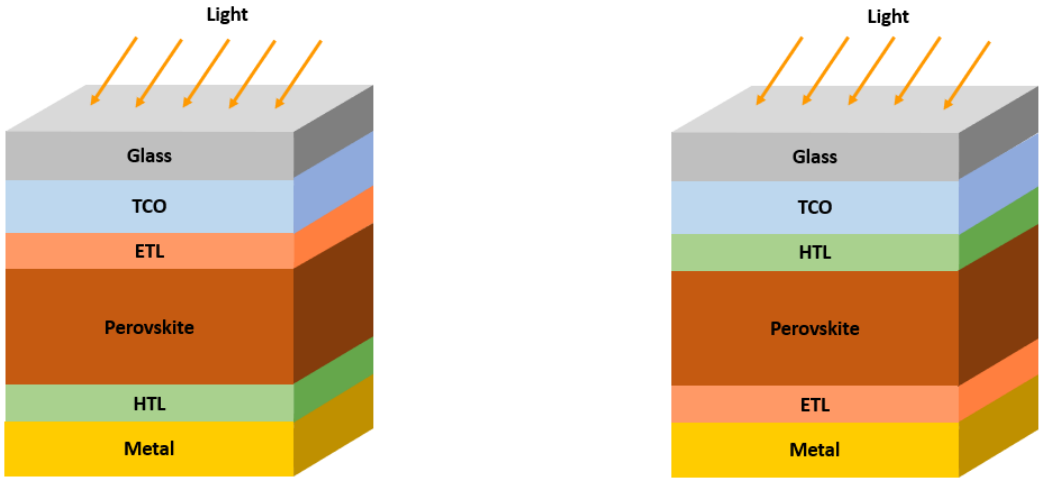


Figure 1.4: The sandwiched layers of PSCs for (a) ETL-perovskite-HTL and (b) HTL-perovskite-ETL planar structure.

The common organic material employed as HTL is poly(3,4-ethylenedioxythio- phene):poly(styrene-sulfonic acid) or abbreviated as PEDOT:PSS [25]. The J-V curve of PSCs showed minor hysteresis effect by using PEDOT:PSS as HTL. However, PEDOT:PSS is a hygroscopic material and has high acidity which might be a challenge towards long-term stability. The use of PEDOT:PSS in the PSCs also resulted in open circuit voltage (V_{oc}) lower than 1 V because of recombination occurred at its interface [27]. Moreover, the ohmic contact formed by this material is imperfect. Thus, there are several good candidates substituting PEDOT:PSS, including 2,2′,7,7′-tetrakis(N,N-di-p-methoxyphenyl-amine)-9,9′-spirobifluorene (Spiro-OMeTAD) [6, 14], NiO [25], poly(N,N-bis(4-butylphenyl)-N,N-bis(phenyl)ben- zidine (polyTPD), N4,N4,N4″,N4″-tetra([1,1′-biphenyl]-4-yl)-[1,1′:4′,1″-terphenyl]]-4,4″-diamine (TaTm) [26], poly[bis(4-phenyl)(2,4,6-trimethylphenyl)-amine] (PTAA) [28].

Furthermore, phenyl-C_{61}-butyric acid methyl ester (PCBM) is the most common material as ETL. PCBM can lower the hysteresis issue induced by the trapped charges at the interface between the absorber layer and ETL. It is because this material forms a good contact with the perovskite [6]. Prior study stated that the use of C_{60} as ETL results in better extraction of the charge carriers due to its high mobility and conductivity. Other prevalent materials for ETL are ZnO and TiO_2. A study reported that the use of TiO_2 as ETL and spiro-OMeTAD as HTL made the device experienced strong hysteresis [6]. The top contact of the PSCs is made of metal, such as gold (Au) and silver (Ag) [11]. When the HTL material is firstly deposited on the substrate, the configuration is commonly called inverted planar. In contrast, when the first material that is deposited on the substrate is ETL, it is called regular planar PSC. The substrate is a glass which is coated with the transparent conductive oxide (TCO), e.g. fluorine-doped tin oxide (FTO) or indium tin oxide (ITO).

In this project, the PSC was fabricated by Solliance Solar Research with the structure of ITO/NiO nanoparticles/$Cs_{0.05}(MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.9}Br_{0.1})_3$/PCBM/ZnO nanoparticles/Au. The solar cell encapsulated with laminated thin film barrier concerning temperature and humidity stability. Figure 1.5 depicts architecture of the device. NiO nanoparticles were used as HTL due to its good chemical stability, conductivity, and low-temperature processing. It was capped by poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) material. Its valence band of -5.4 eV was also well-aligned with valence band of perovskite (-5.4 eV) [27]. On the other side, the conduction band of perovskite of -3.9 eV has a good alignment with the conduction band of PCBM as ETL. PCBM with additional ZnO nanoparticles interlayer formed bilayer-structured ETL which can improve PCE of the cell. ZnO nanoparticles have a wide band gap and thus, it is beneficial to prevent Au migration to the absorber layer. Besides, it can act as a barrier of ion migration to absorber layer which leads to the stability issue of PCE.

The mixed cations and halide anions were used in perovskite compounds. These mixed compounds are significant to address the thermal and structural instability that commonly occurs in pure perovskite

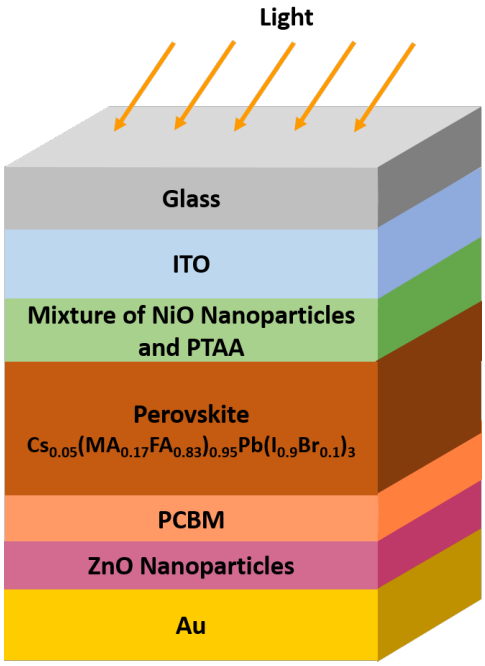


Figure 1.5: An illustration of PSC sample from Solliance Solar Research.

compounds [29]. The absorber layer was made by combining three cations which consist of MA, FA, and Cs. The mixed MA and FA cations were employed to have smaller band gap leading to more photon absorption. The increase of absorbed photons, thus, resulted in the increase of photo-generated current. Nevertheless, these combinations are thermally unstable towards processing condition. In the fabrication of perovskite, it is prominent to prevent impurities as it influences the growth of crystal and morphology of perovskite. These impurities can interrupt the charge collection and thus, lower the performance of the cell. Saliba and co-workers reported that the presence of Cs as inorganic cation showed better thermal stability and more robust device achieving PCE 20%. It is because Cs can suppress impurities resulting in defect-free perovskite [29]. These triple cations of PSCs exhibited higher absorptance in the range 500-800 nm in contrast to $MAPbI_3$ [27].

The use of mixed halide anion of iodine (I) and bromine (Br) gives some benefits to the perovskite. The mixture of these materials can lead to effective bandgap tuning of perovskites. An experimental work which was done by Noh *et al.* has proved that there was a shift in the absorption edge to shorter wavelength or blue light region with increasing Br content [30]. Moreover, Ono and co-workers have reported that the Br content of 0.2 provides better stability toward humidity (RH 55%) [31]. However, there is a limit of Br content in the mixed halide perovskite solar cell. The increase of Br content larger than 0.4 will lead to structural defect and smaller grain size, thus, results in chemical decomposition in perovskite [32]. The Br content in PSC sample is 0.3 which indicates that the perovskite is more stable toward humidity and less probability to suffer from the structural defect. From the electronic standpoint, the rise of Br content leads to lower current density J_{sc} but higher open circuit voltage V_{oc} and fill factor FF [30].

1.3. Issues in Perovskite Solar Cells

1.3.1. Toxicity issue

The rapid development of PSCs shows that there is a possibility of PSCs to be utilized for a solar panel in the future. Structural failure in the solar panel might lead to some issues that can endanger surroundings. The exposure of PSCs to the ambient atmosphere can induce the degradation. Moreover, when exposed to moisture, dissolution of decomposition compound can harm the environment [33]. Hence, it is also worthwhile to understand the impact of perovskite compound to the environment and

health. The heavy metal content (Pb or Sn) of perovskites are classified as a hazardous constituent. It is because of their toxicity to the environment and human health. The Pb compound can be absorbed through dermal contact, respiratory, and gastrointestinal. Blood will transport the Pb compound to the soft tissues in the human body, e.g. kidney and liver. This heavy metal compound can also deposit to the skeleton. Another heavy metal, Sn, has similar toxicity to Pb. Its oxidation reaction releases harmful by-products, e.g. a strong acid and hydroiodic acid [34]. A study has found the effect of high temperature (200°C) on perovskite compounds. The perovskite of $MAPbI_3$ and $MASnI_3$ transformed into PbI_2 and SnI_2, respectively, due to the heat treatment. They have reported that PbI_2 has a higher concentration of Lethal Concentration for 50% of the population (abbreviated as LC50) than SnI_2. It means that SnI_2 has a lower limit of concentration required to cause mortality compared to PbI_2 [33].

Additionally, the solvents used in the fabrication of PSCs (dimethylformamide or DMF and dimethylsulfoxide or DMSO) should be taken into account. These solvents are miscible with water, and thus, it is sensitive to the absorption through dermal contact and ingestion [34]. The further thorough study of the toxicological impact can be done by the cradle-to-grave life cycle assessment (LCA) method. The observation is based on different cycle life stages, such as raw material extraction, synthesis of starting products, fabrication, use, and decommissioning. However, a detailed explanation of LCA of PSCs can be found in [14, 34]. Another aspect that should be considered is the decomposition of perovskites due to humidity. A good encapsulation can be the solution to this issue.

1.3.2. Stability and scale-up issues

Other challenges, such as moisture sensitivity, scalability, and stability, should be overcome to accomplish high performing PSCs. First, the issue that is attributed to the high sensitivity of the cells to moisture. PSCs exposure to the humid environment can give a detrimental effect to the device. A preceding study has reported that the major cause of performance loss on PSCs originated from perovskite decomposition due to the high solubility of $MAPbI_3$ in water. This issue is related to the long-term application. This issue can be overcome by isolating the device by an encapsulation. The production of PSCs on industrial scale is considered because of the advantageous of this devices. One of the issues that should be resolved to scale up PSCs is the deposition technique, spin coating. Thus, other deposition technologies can be used to fabricate the cells, such as slot-die, inkjet printing, spray coating [14]. Another challenge regarding the scalability of PSCs is the increase use of Pb that implies higher environmental impact.

1.3.3. Hysteresis phenomenon

Apart from its attractive efficiency, there is peculiar behaviour of measured current and voltage of PSCs which turns it into a hot topic for PV world. The anomalous implies the slow response of the current through the device as the voltage applied to the device. It is caused by the delay time in the J-V measurement [3] and, thus, results in current lags as can be seen in Figure 1.6. It is an obstacle to accurately measure the efficiency of the cell which is commonly well-known as hysteresis phenomenon. Prior study has reported that hysteresis was strongly caused by the ion migration that dominates via extended defects, for instance, grain boundaries (GBs). On the other side, PSCs without GBs exhibited no ion migration and thus, hysteresis-free on the device [35]. The hysteresis-free cells can be achieved when the device contains a low density of trap and subsequently, low defect states [11]. Moreover, Unger et al. have found that the hysteresis in PSCs can be caused by the trapped/de-trapped charge carriers, ferroelectricity, and changes in contact conductivity or absorber [3].

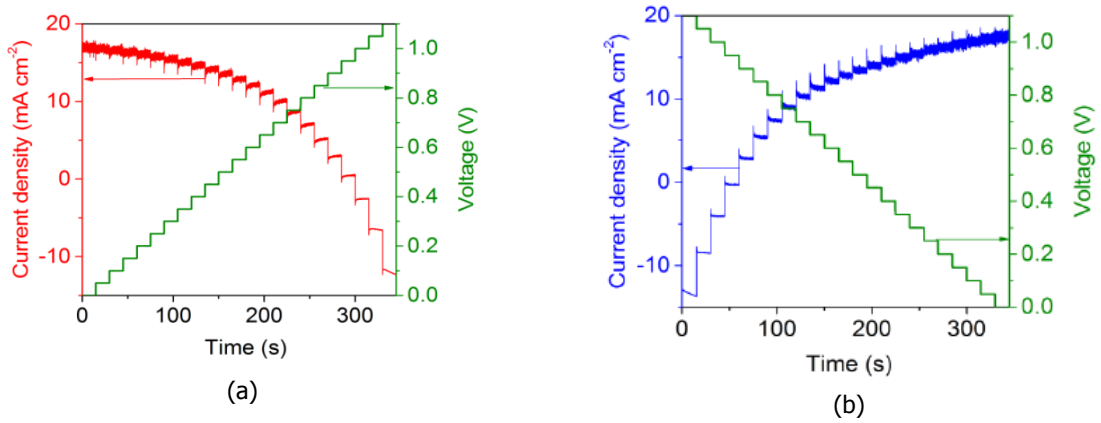


Figure 1.6: The transient slow response of current density in response to staircase voltage sweep as function of time by (a) forward and (b) reverse scan [3].

Hysteresis phenomenon refers to the difference in I-V curve when sweeping the voltage in forward (from negative to positive value) and backward (from positive to negative value) direction. The forward and backward scan of the device result in underestimation and overestimation of the actual PCE, respectively [36]. Hysteresis effect is also influenced by scan rates. A study found that hysteresis increases with slower scan rate [37]. However, another study reported that slow scan rate resulting in less severe hysteresis [5]. The J-V characterization is aimed to understand hysteresis effect on PSC. J-V characteristic under illumination of light has the same behaviour with an ideal diode, which consists of a current source and a diode. As the J-V curve of PSC exhibits a hysteresis effect, the investigation of an equivalent circuit of PSCs is essential and hence, becomes the focus of this project.

An equivalent circuit model is considered as a model to simulate the J-V curve of the cell. The performance depends on fundamental parameters of the solar cell, such as V_{oc}, J_{sc}, peak power (P_{max}), and fill factor (FF) [16]. FF is affected by other parameters as well as series and shunt resistance. Besides these parameters, the study needs to consider the configuration of the circuit. In most cases, the configuration of the solar cell consists of single and double diode configuration, as depicted in Figure 1.7. The latter configuration gives a more accurate result, however, due to its complexity, it is less enticing for the solar cell simulation. Further deeper analysis of the equivalent circuit will be discussed in Chapter 2.

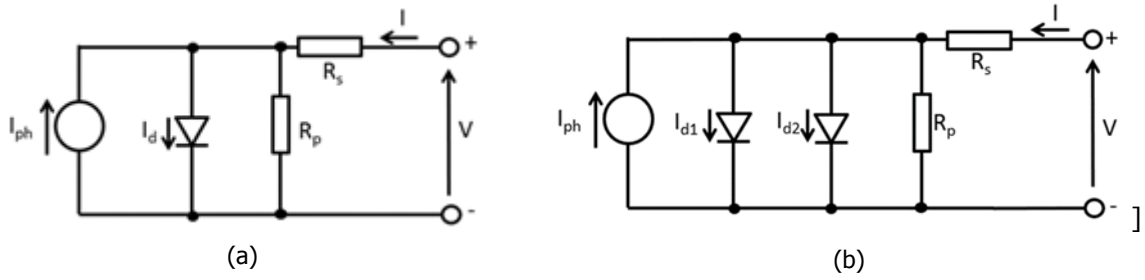


Figure 1.7: The equivalent circuit of a solar cell with (a) a single diode and (b) with double diodes in parallel.

The equivalent circuit of single and double diode configuration can be represented in equation 1.1 and 1.2 [16], respectively.

$$J = J_o \left\{ exp\left[\frac{q(V - AJR_s)}{nk_BT} \right] - 1 \right\} + \frac{V - AJR_s}{R_p} - J_{ph} \tag{1.1}$$

$$J = J_{o1}\left\{exp\left[\frac{q(V - AJR_s)}{n_1 k_B T}\right] - 1\right\} + J_{o2}\left\{exp\left[\frac{q(V - AJR_s)}{n_2 k_B T}\right] - 1\right\} + \frac{V - AJR_s}{R_p} - J_{ph} \quad (1.2)$$

where, J is current density of the solar cell (A/m^2), J_o is saturation current density of the diode (A/m^2), q is elementary charge (C), V is voltage across the device (V), k_B is Boltzmann's constant (m^{2}kg/s^2/K), T is temperature (K), n is the ideality factor of the diode, A is the area of the solar cell (m^2), R_s is series resistance (Ω), R_p is parallel or shunt resistance (Ω), and J_{ph} photo-generated current density (A/m^2). As shown by equation 1.2, in the double diode configuration, there are J_{o1} and J_{o2} that denote the saturation current density of the first and second diode (A/m^2), respectively, while n_1 and n_2 represent ideality factor of the first and second diode, respectively.

1.4. Existing Researches

In recent years, the research and development of PSCs have grown rapidly. The optimization of PSCs performance is not only approached by experimental studies, but also by modelling. Modelling of the cells can provide a better insight and understanding of physical behaviour of the cell. It can also be a way to improve the efficiency of the cell. Moreover, in some cases, the analysis result from a model requires further validation from the experimental approach. These following preceding studies have tried to model the PSCs optically and electrically.

1.4.1. Optical model

Several research groups have done the optical simulation of PSCs. Optimization of the power output of PSCs can be approached by modelling the optical losses concerning the reflection and transmission in the device. Taghavi et al. investigated reflection and transmission rate at the interface in any layer using refractive index n and extinction coefficient k. They found out that perovskite materials induce reflection interference [38]. Another research about light interference model in mixed halide PSCs has performed by Sohrabpoor and co-workers [39]. Furthermore, a more interesting optical model demonstrated on the tandem application of perovskite and c-Si solar cell by Santbergen et al. [40]. This study also simulated the optical losses of the device but their focus is on investigating the light scattering surface textures.

1.4.2. Optoelectronic model

Several studies used PSC as the top cell of tandem photovoltaic with silicon as bottom cell for high-efficiency values. A research which has been done by Garnett and co-workers aimed at improving perovskite-silicon tandem cell efficiency by optoelectronic three-dimensional (3D) simulations [41]. Their innovation to use three-terminal (3-T) tandem cell came from preceding studies that two-terminal (2-T) configuration requires current matching due to the series interconnected cell, whereas four-terminal (4-T) tandem cell needs three transparent electrical contact that leads to parasitic absorption. They demonstrated the optical response of the perovskite and silicon that can be used to calculate the charge generation rate (in x, y, z position). Subsequently, this will be utilized as input for the electrical modelling to solve drift-diffusion equations which then resulted in electrical characteristics, e.g. J, V, and FF. An excellent efficiency of the 3-T tandem cell of 35.2% was predicted. It is higher than the maximum possible efficiency of 4-T configuration of 32.8% [41].

Another interesting model was observed by considering the relative humidity (RH) by semi-analytical optoelectronic model. The simulation was based on the drift-diffusion model and on external quantum efficiency (EQE) [42]. In this approach, the goal is identifying the effect of humidity on absorption coefficient and diffusion length. The influence of humidity on the electrical parameters, such as shunt and series resistance, was also taken into account. The simulation dealt with a two-diode equivalent circuit model. The first diode is attributed to the current generated by the diffusion of minority charge carriers in the quasi-neutral region, whereas the second diode indicates the losses occurred in the space charge region. As described earlier, the J-V characteristic of PSCs is extremely affected by hysteresis phenomenon. However, in the study done by Bhatt et al. [42], the analysis of equivalent circuit was

performed without considering the hysteresis effect. Moreover, the calculation of the electrical parameters, such as the current density of the diode and saturation current, were based on some properties, such as diffusion coefficient, intrinsic carrier concentration, and diffusion length. Other interesting researches about the optoelectronic model of PSCs can be found in [11, 26, 43–45].

1.4.3. Equivalent circuit model

The modelling of an equivalent circuit of PSCs has attracted researchers' attention as well. It is because the PSCs exhibit hysteresis phenomenon when it is scanned in forward and reverse direction which does not occur in the widely used silicon solar cell. Thus, there is a possibility that the equivalent circuit of PSCs might not follow the equivalent circuit of ideal solar cell as depicted in Figure 1.7. Several fascinating investigations of equivalent circuit of PSCs has been done based on the J-V characteristic of the device.

Liao *et al.* have noticed that most of the calculated ideality factor *n* of PSCs with various device architecture is larger than 2. In most cases, the ideality factor of solar cell is in the range of 1 up to 2 [4]. This ideality factor implies a measure of the quality of a junction and represents the type of recombination in the device [16]. The minority carrier recombination that occurs in the ideal junction solar cell is represented by ideality factor of 1, while other recombination mechanisms can have ideality factor of 2. High ideality factor indicates high recombination in a solar cell. Thus, Liao and co-workers presented the series double diode equivalent circuit of PSCs. They obtained smaller ideality factor from the new equivalent circuit that represented better PN junction of $TiO_2/CH_3NH_3PbI_{(3-x)}Cl_x$/Spiro-OMeTAD/Au architecture. The Cl^- content was varied which resulted in decreasing ideality factor value [4].

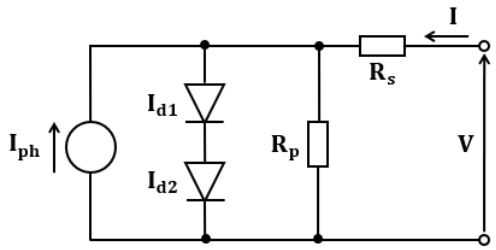


Figure 1.8: Equivalent circuit model with double diodes in series [4].

Next, a study by Seki demonstrated the equivalent circuit of ideal solar cell with additional resistor and capacitor in parallel as depicted in Figure 1.9. The theoretical model of the circuit focused on the produced electric field from the accumulated charged in the charge transport layer. The produced electric field is presumed as the cause of voltage reduction [46]. The study found out that hysteresis increases along with a slower scan rate. It also presented the probability of hysteresis phenomena on PSCs as a function of scanning rates. Furthermore, it will be the fundamental notion to determine the scan rate in this study explained in Chapter 3. The research concluded that higher hysteresis resulted when the voltage was scanned from the open circuit side. Besides, fast scan rate induces less charge accumulation, and hence, the reduction of current density due to charge accumulation can be minimized. Moreover, the study provided hysteresis constant considering the difference maximum PCE of various scan rates that can be used to determine the scan rate in this project.

Another interesting equivalent circuit model of ITO/PEDOT:PSS/$CH_3NH_3PbI_{(3-x)}$/PCBM/Al(Ca) was reported by Cojocaru and co-workers proposing two photodiodes to represent the interfaces of PEDOT:PSS/ $CH_3NH_3PbI_3$ and PCBM/$CH_3NH_3PbI_3$. The basic idea of these diodes came from the different energy level between two semiconductors that form a junction. The junction is then represented by a diode [6]. Moreover, a Schottky diode is used to represent the junction formed when semiconductor and metal with different work function are in contact that behaves like Schottky junction. In the study, this diode reflects the contact between PCBM as semiconductor and Al as metal. They used a packaged Schottky diode that consists of a resistor, a capacitor, and an inductor. The inductor represented the

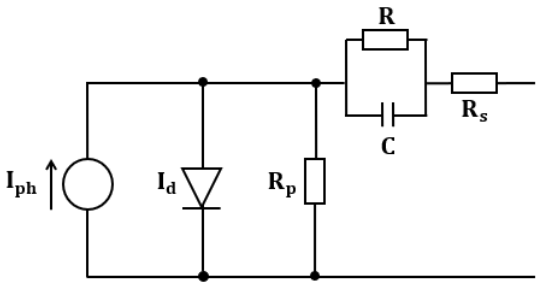


Figure 1.9: Equivalent circuit model of PSCs with additional capacitor and resistor [5].

inductance behaviour exhibited by the change in the interface of PCBM/Al(Ca) originating from the aging of PCBM material. The variation of inductance (0 mH, 50 mH, 500 mH) was performed in the study to observe the effect of inductance on the J-V curve. Higher hysteresis exists in the J-V curve along with the increase of inductance value. Consequently, the metal penetrates to the PCBM layer and induces a trap of charge. Figure 1.10 shows the illustration of equivalent circuit including two photodiodes and Schottky Barrier Diode abbreviated as SBD. However, the idea of using packaged Schottky diode has been opposed by Tada because the inductance is an extrinsic physical property of a packaged diode [47]. Thus, it requires further verification to include the inductor in the packaged SBD. This opposed argument also found out that the experiment by Cojocaru *et al.* used commercial inductor that has windings of wire or magnetic core which is not part of the PSC device. High estimated inductance of 50 and 500 mH is crucial to reproduce hysteresis phenomenon.

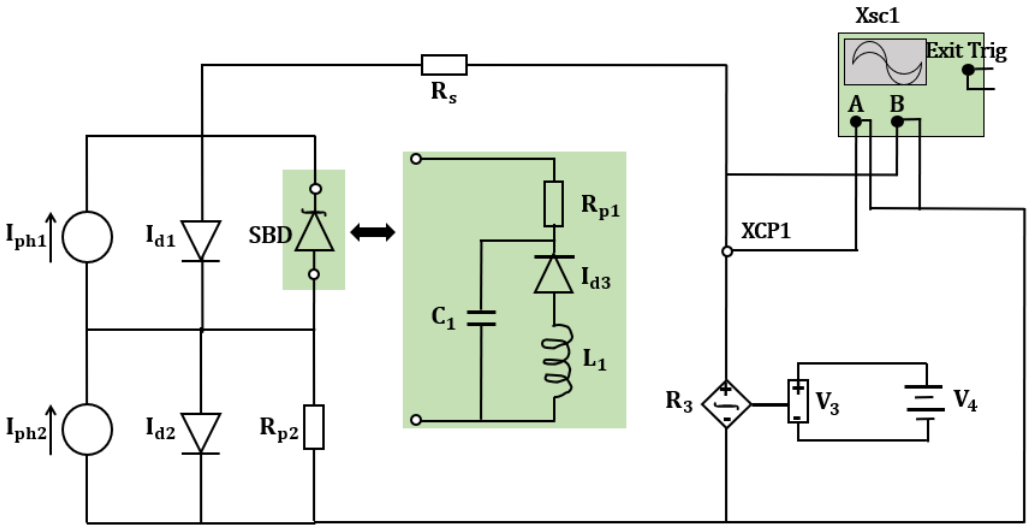


Figure 1.10: Equivalent circuit model of inverted PSCs with two photodiodes and Schottky diode [6].

Furthermore, Cojocaru and co-workers also investigated the origin of hysteresis effect with capacitance model. The device architecture of SnO_2:F/Compact TiO_2/$CH_3NH_3PbI_3$/spiro-OMeTAD/Au was used in the study. They argued that the use of PCBM or passivating the TiO_2 layer by C60 as ETL in PSC could reduce the trap states in the interface of ETL/absorber layer. Consideration of the origin of hysteresis phenomenon determined by the thermal expansion coefficient of TiO_2 and $CH_3NH_3PbI_3$ is also considered. $CH_3NH_3PbI_3$ has higher thermal expansion coefficient of 216 x 10^{-6}/K, while TiO_2 has 23.5 x 10^{-6}/K [48]. The increase of temperature causes interfacial stress at the interface between TiO_2 and $CH_3NH_3PbI_3$. This stress may lead to the defect and thus, reflects as a trap for the charges. These charges accumulated at the interface and it acts as a capacitor [7]. They considered several equivalent circuits of PSC and validated hysteresis exhibited in the I-V characteristics. The simulation was done by using MultiSim Electronic Workbench. First, they modelled the capacitor in parallel with the current source, diode, and shunt resistor. However, the output I-V characteristic did not represent

hysteresis effect similar to the experiment result. Next, they tried a new equivalent circuit model as depicted in Figure 1.11. The consideration of using two capacitors with different values was based on the estimated charge carrier accumulation at the interface of ETL/perovskite and perovskite/HTL. Higher capacitance at the interface of ETL/perovskite was due to the higher lattice mismatch yielded by different thermal expansion coefficient. Subsequently, the I-V curve from this model was fitted to the hysteretic I-V from experiment and gave a good agreement with it. Thus, the related device architecture of PSC in this study was dealt with equivalent circuit model as showed in Figure 1.11.

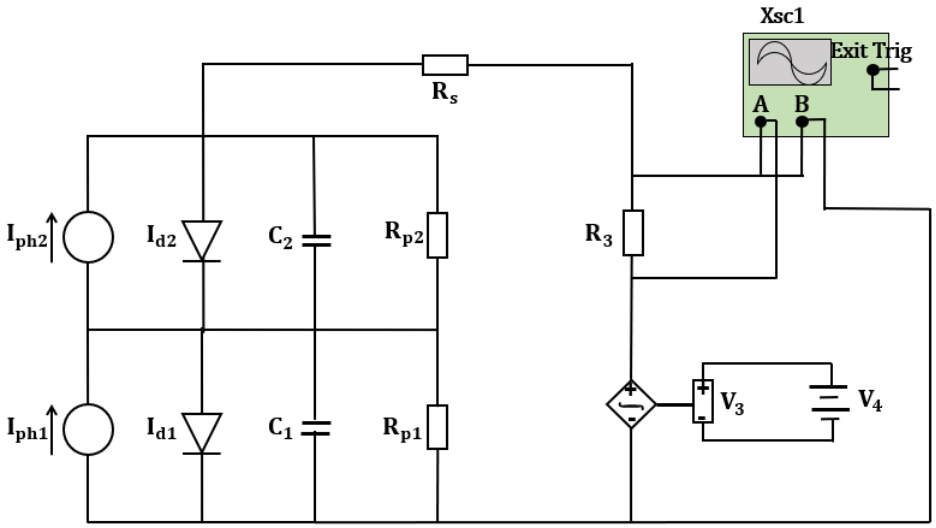


Figure 1.11: Equivalent circuit model of inverted PSCs with two photodiodes and capacitors [7].

1.5. Research gap

Based on existing researches, it can be estimated that equivalent circuit of PSC depends on the materials of the device. In this project, bilayer ETL and mixed organic cation and halide anion perovskite are used. Thus, the equivalent circuit of this device could be different compared to the existing researches. So far researchers have not used band diagram analysis to determine suitable equivalent circuit of PSC device. It would be interesting to done in further research.

Preceding studies have observed the hysteresis phenomenon by I-V curve fitting of the result from experiment and simulation. However, as depicted in Figure 1.6, this hysteresis phenomenon exhibits a capacitive behaviour in the curve of current density as a function of time. The *J(t)* curve is hence, essential to be used to analyze the hysteresis effect in the device. Relatively few studies focus on the *J(t)* characteristic of PSC. Thus, the I-t curve fitting can also be a way to specify the equivalent circuit. Subsequently, it is important to validate the equivalent circuit obtained by band diagram investigation to the *J(t)* curve fitting of the related equivalent circuit.

1.6. Objective and Research questions

The purpose of this project is to investigate hysteresis phenomenon in PSC sample, which was introduced in 1.2.2, by electrical modelling approach. In order to obtain more accurate consideration, electrical device characterization based on the band diagram can be beneficial to get better insight. Furthermore, the peculiar *J(t)* curve from an experiment that shows capacitive behaviour can also be analyzed in this project. The aim of this project will be carried out in the following main research question:

"Is it possible to model hysteresis of the PSC with an equivalent circuit?"

Moreover, these following subquestions are formulated to answer the main research question:
1. Is it possible to understand charge accumulation in a PSC from the band diagram?
2. Can equivalent circuit of PSC be derived from band diagram?
3. Is it possible to study hysteresis phenomenon using time-resolved I-V measurement?
4. Which of the selected circuits best reproduces the measurement result?

1.7. Methodology

To address those research questions, the methodology used in this study is illustrated by a diagram depicted in Figure 1.12. As can be seen in the figure, there are experiment work and simulation done in this project. The experiment aims to measure the I-V of the cell as a function of time by time-resolved measurement. Chapter 3 will explain the experimental setup. The purpose of simulation which is done by Sentaurus TCAD is to simulate the band diagram of PSC sample. The simulated band diagram is worthwhile to determine the equivalent circuit of PSCs. Subsequently, the predicted equivalent circuit will be simulated by QUCS to obtain the I-V curve as function of time. Finally, the I-t curve fitting will be done by Matlab to compare the I-t curve obtained from experiment and simulation by QUCS. This I-t curve fitting results in electrical parameters of the measured PSC.

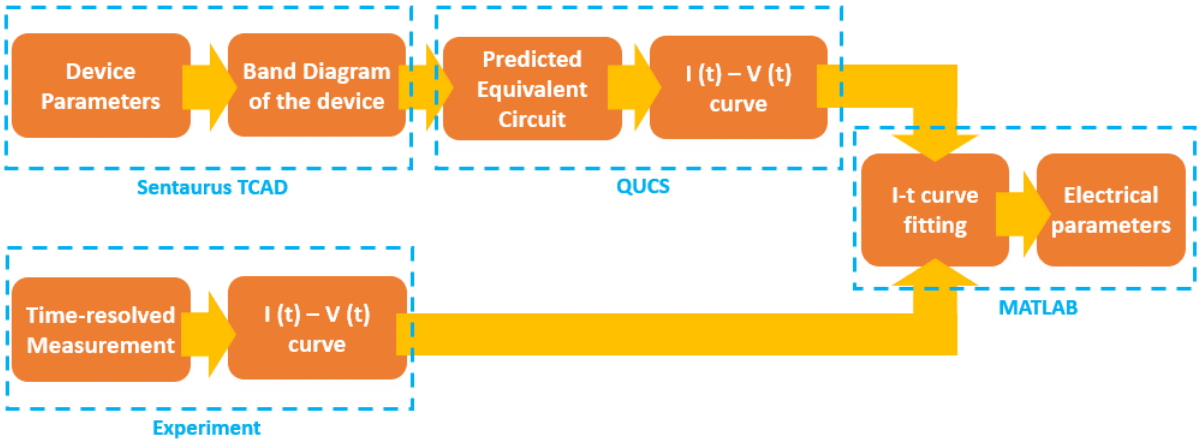


Figure 1.12: Flow diagram of methodology in this study.

1.8. Report structure

The structure of the report is as follows. Chapter 2 will discuss the band diagram investigation of PSC. The band diagram is obtained by modelling each material with Sentaurus TCAD. In this chapter, the determination of the predicted equivalent circuit will be explained. Chapter 3 presents methodology of time-resolved I-V measurement and the measurement results. Chapter 4 will discuss electrical modelling of PSC sample. A description of creating an equivalent circuit in QUCS will be given in this chapter. The *J(t)* curve fitting of equivalent circuits derived from band diagram simulation in Chapter 2 and two additional equivalent circuits will also be explained. Finally, Chapter 5 presents conclusion and recommendation for further research.

2

Investigation of Band Diagram

This chapter is aimed to answer the first and second research questions introduced in subchapter 1.6 which were *"Is it possible to understand charge accumulation in a PSC from the band diagram?"* and *"Can equivalent circuit of PSC be derived from band diagram?"*, respectively. An investigation of band diagram of PSC sample fabricated by Solliance Solar Research was done in this chapter. The PSC sample architecture consisted of ITO/NiO nanoparticles/$Cs_{0.05}(MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.9}Br_{0.1})_3$/PCBM/ZnO nanoparticles/Au. In this chapter, theoretical working principle of a PSC in dark condition and under illumination from a literature will be discussed in subchapter 2.1. Subsequently, the band diagram of PSC sample in dark condition will be presented by modelling each layer of the cell using Sentaurus Technology Computer-Aided Design (TCAD). The simulation method will be explained in subchapter 2.2. Subchapter 2.3 presents analysis of the simulated band diagram.

2.1. Theoretical Working Principle of PSC device

A contact between perovskite and charge-selective transport layer will create a junction. There are two junctions formed in PSC device consisting of a junction between electron transport layer and perovskite and a junction between perovskite and hole transport layer. These junctions have significant roles to the charge carriers collection. Furthermore, to investigate origin of hysteresis in a PSC, it is important to understand the working principle of PSC device at different conditions, i.e. in dark condition and under illumination. This working principle refers to mechanism of charge carriers transport from photoactive layer to the respective electrodes. This mechanism may be investigated through band alignment of the device. In this subchapter, theoretical working principle of PSC in dark condition and under illumination will be discussed although simulation of band diagram in this chapter was only done in dark condition.

2.1.1. Dark condition

When a PSC is in dark and short circuit condition, Fermi level of HTL, absorber layer, and ETL are in the same level E_{F0} and in equilibrium as illustrated in Figure 2.1a [8]. This implies that there is no charge generated in this condition. Perovskite has an inclined band because there is an electric field in this region. This electric field drives electrons to flow to ETL and then, electrons will be collected at back contact. On the other hand, electric field also pushes holes to flow to HTL. As shown in Figure 2.1a, built-in voltage V_{bi} was created due to work function difference of HTL (φ_{HTL}) and ETL (φ_{ETL}). In this project, the simulation of band diagram of PSC in dark condition was done and will be discussed in subchapter 2.2.

2.1.2. Under illumination

In the case that PSC is illuminated by light and at open circuit, the Fermi level of HTL and ETL are split into E_{Fp} and E_{Fn}, respectively. The inclined band of perovskite becomes a flat band. The difference between the split Fermi level indicates open circuit voltage which is generated due to photo-generated

charge carriers under illumination of light. As depicted in Figure 2.1b, the work function of both transport layers limits the generated V_{oc} [8].

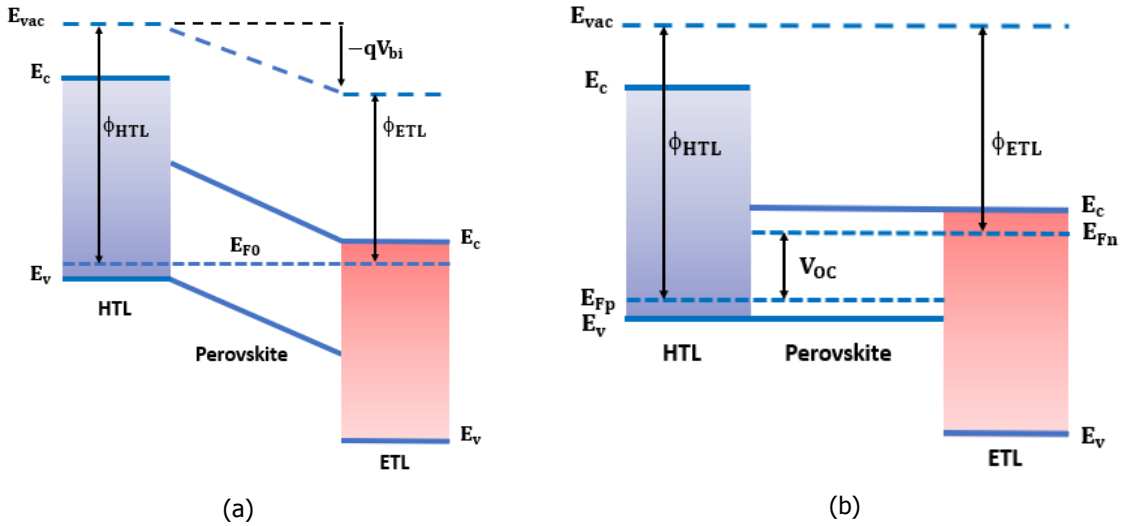


Figure 2.1: The illustration of band diagram of PSC (a) in dark condition and (b) under illumination [8].

2.2. Simulation of the Band Diagram

In this project, Sentaurus TCAD was used to simulate the band diagram of the PSC. It offers the simulation of optical properties, electrical properties, and processing technology [9]. Sentaurus is a comprehensive software which can be used to develop and to optimize various semiconductor devices. This advanced multidimensional (1D/2D/3D) software has attracted researchers' attention. It is because in general research and development of semiconductor device are done in the lab and require high expenses to buy some components. Thus, simulation with the software may lead to less time-consuming and cheaper research and development. In this project, Sentaurus was used to visualize the two-dimensional (2D) band diagram of PSC. Sentaurus provides simulation tools which consist of Sentaurus Workbench, Structure Device Editor (SDE), SNMESH, and SDEVICE tool. Figure 2.2 shows the flowchart of simulation process with Sentaurus consisting those tools.

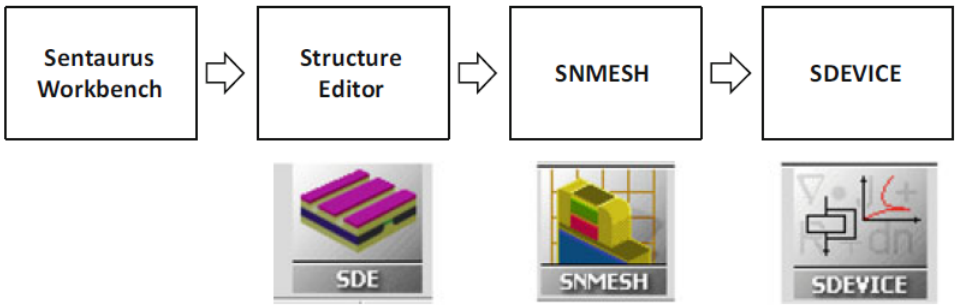


Figure 2.2: The flowchart of basic simulation process with Sentaurus TCAD [9].

2.2.1. Sentaurus Workbench

Sentaurus workbench is a graphical user interface for creating, editing, managing, and observing the process flow. This tool can be used to automate tasks related to running simulations. The tasks are associated with preprocessing the input files, setting up tool, and visualizing the results. In addition, Sentaurus Workbench tool supports library that can be defined by a user [49]. The main view of Sentaurus Workbench is commonly named project editor which provides tools to edit, run, and organize the simulation.

2.2.2. Sentaurus Structure Editor (SDE)

Structure editor is a tool in Sentaurus used to create a 2D or 3D geometric structure of a device which is CAD-based. The geometric structure of a device can be edited and fitted by user with good flexibility [9]. This tool also provides advanced visualization of the geometric structure. Moreover, the user is allowed to select a specific part of the structure to be displayed while other parts are not displayed. In this project, thickness and doping concentration of each material of PSC device are required as input in structure editor to create 2D geometric structure.

2.2.3. SNMESH

SNMESH tool is used to determine mesh of the device structure. This mesh is employed to solve mathematical model, such as Poisson's equation and carriers continuity equations which are represented by equation 2.1 [50], 2.2, and 2.4 [51].

$$\frac{d^2\phi(x)}{dx^2} = -\frac{dE(x)}{dx} = -\frac{\rho(x)}{\epsilon_s} \tag{2.1}$$

where, φ(x) represents the electric potential, E(x) is the electric field, ρ is the volume charge density, and ε represents the permittivity of the material. The electric field drives the electrons and holes in the perovskite layer to flow to ETL and HTL, respectively.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{dJ_n}{dx} + (G - R) \tag{2.2}$$

$$J_n = q\mu_n E - qD_n\frac{dn}{dx} \tag{2.3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\frac{dJ_p}{dx} + (G - R) \tag{2.4}$$

$$J_p = q\mu_p E - qD_p\frac{dp}{dx} \tag{2.5}$$

where, n and p represent electron and hole concentration, respectively, q is the elementary charge, μ_n and μ_p are electron and hole mobility, respectively, D_n represents electron diffusion coefficient, D_p is hole diffusion coefficient, E is the electric field, G and R are generation and recombination rates, respectively.

2.2.4. SDEVICE

Sentaurus device is an advanced tool to simulate optical, electrical, and thermal characteristics of the semiconductor device. In the band diagram simulation, characteristics of each layer in PSC will be used as the input in this tool. These characteristics consist of electron affinity, band gap, electron and holes density of states, and permittivity. In this project, the parameters of those characteristics were obtained from literature and through fitting. These parameters are provided in Appendix A. Furthermore, the result of band diagram simulation using Sentaurus TCAD is depicted in Figure 2.3.

2.3. Analysis of Simulated Band Diagram

The simulation was done in dark condition without applied voltage. As can be seen in Figure 2.3, the Fermi level is the same along the device where quasi-Fermi level of electrons (E_{Fn}) is equal to quasi-Fermi level of holes (E_{Fp}). The conduction and valence band level are represented by E_c and E_v, respectively. The inclined band of perovskite in the simulation is similar to the theory introduced in 2.1. The electric field exists in this inclined band due to the built-in potential created by work function difference of the HTL and ETL materials. The electric field can be determined by Poisson's equation 2.1. Direction of the electric field is in the opposite direction to the electrons flow. The built-in electric field has an essential role in the charge separation in the device. In addition, doping of ETL and HTL leads

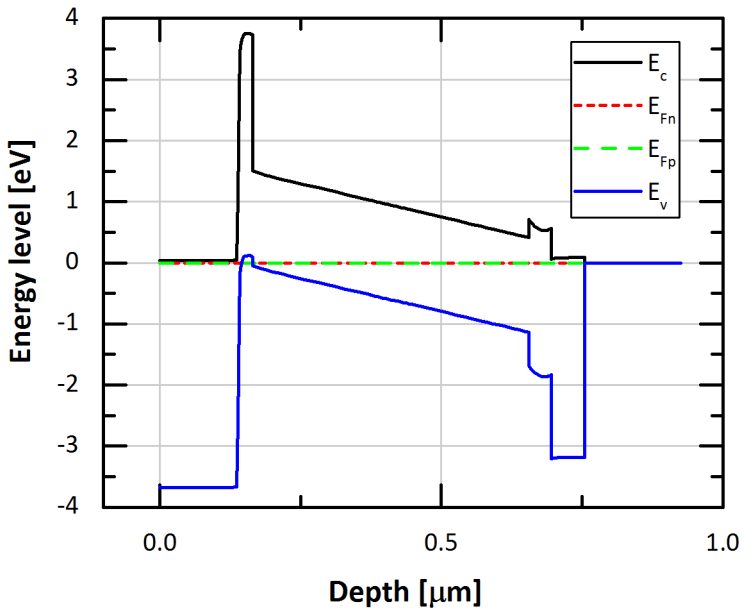


Figure 2.3: The simulated band diagram of PSC sample using Sentaurus TCAD.

to the increase of electric field strength and to the increase of their conductivity which results in higher FF. An illustration of charge flow is depicted in Figure 2.4. Electric field pushes holes and electrons to their respective transport layer. The conduction band level of PCBM is higher than perovskite. Thus, it acts as a small barrier seen by electrons. In contrast, when holes flow to NiO nanoparticles, no barrier formed in the interface of NiO nanoparticles and perovskite. As the conduction and valence band level differences influence charge carrier transport, thus, analysis of conduction and valence band offset is essential. It will be discussed in this subchapter.

2.3.1. Band offset

The analysis of band offset is fruitful to understand the charge transport in the device. Band offset consists of conduction band offset (CBO) and valence band offset (VBO). Figure 2.5 and 2.6 show the illustration of band diagram of semiconductor materials. It provides several parameters that will be used to the discussion in this chapter. As can be seen from the figure, CBO is determined from the difference between electron affinities (χ) of two materials. VBO can be obtained by the difference of electron affinity (χ) and band gap (E_G) of the related materials. Vacuum level used as the reference of energy level. The means that the determination of CBO and VBO in this project is based on the study by Minemoto and Murata [10]. Equation 2.6 and 2.7 are acquired from the illustration of band diagram.

$$CBO = \chi_{absorber} - \chi_{ETL} \tag{2.6}$$

$$VBO = (\chi_{HTL} + Eg_{HTL}) - (\chi_{absorber} + Eg_{absorber}) \tag{2.7}$$

- CBO between ETL and perovskite interface
  The calculation of CBO with Equation 2.6 can result in positive or negative CBO. CBO is a material dependent because it is related to affinity of the materials. Figure 2.7 depicts illustration of these two types of CBO in which negative CBO forms a cliff, while positive CBO establishes a spike shape. This spike acts as a barrier to the electron flows from absorber layer to electrode. In contrast, the cliff does not disrupt the electron collection at the electrode.

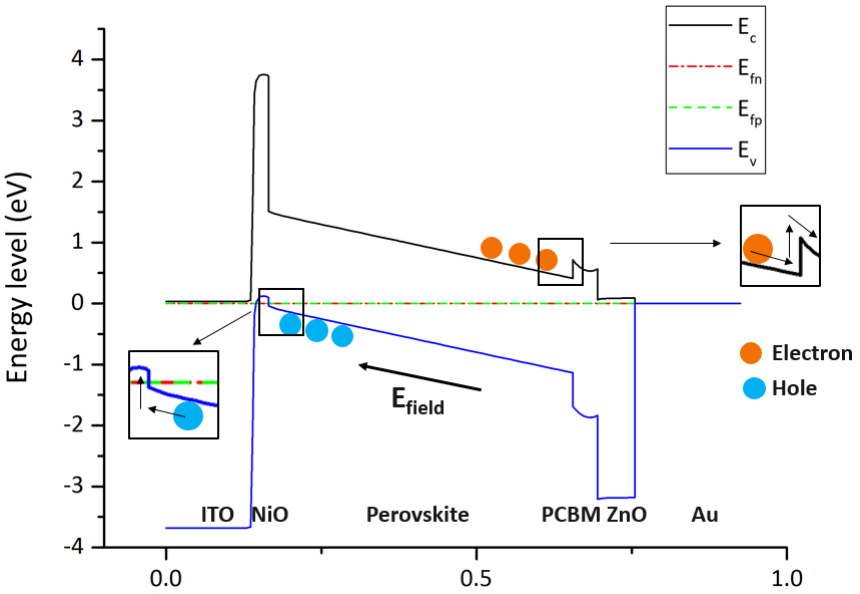


Figure 2.4: The illustration of charge carriers transport in PSC.

CBO of the simulated band diagram in Figure 2.3 forms a spike which implies positive value. It is relevant with calculation using Equation 2.6 resulting in CBO of 0.3 eV. High barrier established by large CBO might induce negatively charge accumulation in the ETL/perovskite interface. The illustration of electron flow from absorber layer to ETL is shown in Figure 2.4. In order to understand the resulted CBO, a comparison to a prior study was done. The simulation done in the study found that CBO between 0 and 0.3 eV resulted in high V_{oc} and FF due to low interface defect density. Subsequently, CBO which is larger than 0.3 eV resulted in poor FF. In the study, VBO was set to be zero whereas in this project, the VBO will be analysed as well. Thus, those results of aforementioned study cannot be implemented directly in this project because the VBO might not zero.

- VBO between perovskite and HTL interface
  The value of VBO can be positive or negative as well. The latter forms a cliff, whereas the other one forms a spike as shown in Figure 2.8. Based on the simulated band diagram of PSC sample, the VBO forms a cliff which facilitates the collection of holes at the electrode. This cliff implies negative VBO which is consistent with the calculated VBO of -0.4 eV. As depicted in Figure 2.3, the thickness of HTL in this project is thin. Thus, a cliff formed at the perovskite/HTL interface is close to ITO electrode. Under illumination condition, recombination of electrons from external circuit and holes transported to HTL may occur in this interface. Based on the literature [10], negative VBO leads to the increase of recombination at perovskite/HTL interface and hence, V_{oc} decreases. When the VBO is 0, 0.1, 0.2 eV, it results in high FF. Nevertheless, VBO which is more than 0.2 eV resulted in a reduction of FF.

2.3.2. Junction between two materials

- ITO/NiO nanoparticles interface

  It is worth noting that ITO is n-type semiconductor material, whereas NiO nanoparticles is highly p-doped material. The high doping of NiO nanoparticles suppresses concentration of electrons. Moreover, it reduces electron mobility and decrease electrons conductivity [52] forming a hole-selective contact. High conduction band level of this HTL material could also create a good hole-selectivity contact since it acts as a large barrier seen by electrons in absorber layer. Furthermore, as can be seen in Figure 2.3, the valence band of NiO nanoparticles is very close to the conduction band of ITO. In this case, holes may tunnel from the valence band of highly p-doped

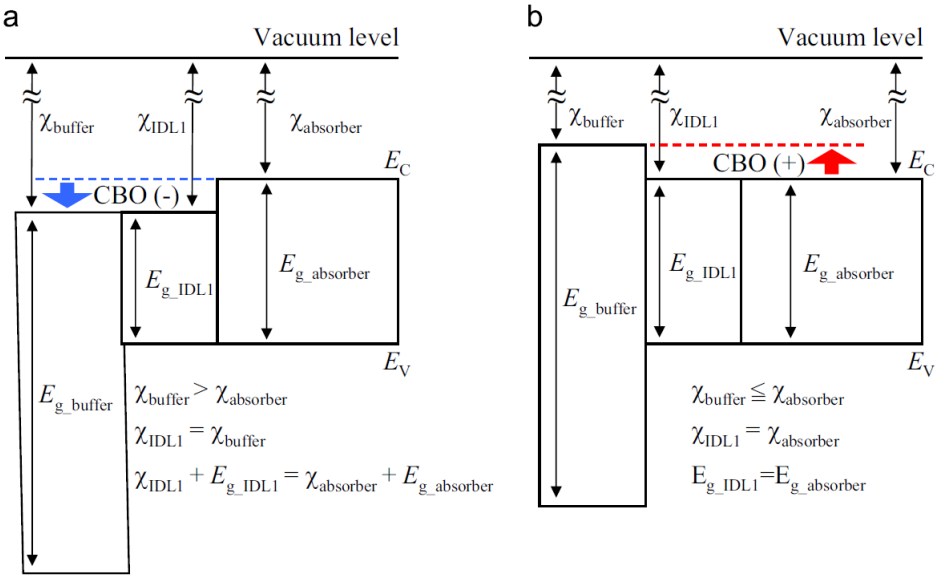


Figure 2.5: Band diagram of device for CBO calculation[10].

NiO nanoparticles into the conduction band of ITO. Thus, it will increase holes extraction at the electrode.

- NiO nanoparticles/perovskite interface

  NiO nanoparticles employed as a hole transport material because its valence band is close to the valence band of perovskite. The difference of valence band of these materials has been discussed with the VBO concept in section 2.3.2. As aforementioned, conduction band level of NiO nanoparticles is much higher compared to perovskite. It can prevent electrons flowing from perovskite to front electrode. Additionally, the use of NiO nanoparticles as hole transport material in a p-i-n PSCs results in lower efficiency than in a n-i-p configuration [53]. Wang and co-workers reported that it can be caused by poor contact of NiO film and absorber layer due to defects induced by low-temperature processing of the NiO nanoparticles. Consequently, this defect can act as a trap for the charge resulting in charge accumulation.

- Perovskite/PCBM interface

  The use of PCBM as the electron transport material can reduce hysteresis occurred in a PSC because there is less trap state at the interface of PCBM and perovskite. Thus, electrons could be transported to back electrode more efficiently [7]. For a comparison, when TiO_2 is used as ETL material, more trap states are exhibited at ETL/perovskite interface. Thus, passivation of TiO_2 layer with fullerene C_{60} is required to minimize the trap states [7]. Moreover, although the use of PCBM may result in negligible hysteresis, there is possibility of defect to occur at the interface of perovskite and PCBM. When temperature increases, there is interfacial stress at perovskite/PCBM interface due to thermal expansion coefficient difference between perovskite (216 x 10−6 /K [48]) and PCBM (62 x 10−6/K [54]). This interfacial stress creates defects at the perovskite/PCBM interface inducing charge accumulation.

- PCBM/ZnO nanoparticles interface

  As introduced in Subchapter 1.2.2, PCBM and ZnO nanoparticles were used as electron transport materials forming bilayer ETL. Figure 2.3 shows that PCBM was placed next to perovskite layer because its conduction band is close to conduction band of perovskite which may facilitate electrons flow. The valence band level of PCBM is lower than the absorber layer. It prevent holes flowing from absorber layer to ETL. Thus, holes will be repelled to the absorber layer. On the other hand, ZnO nanoparticles was placed next to Au back contact. The wide band gap of this material is beneficial to block Au migration.

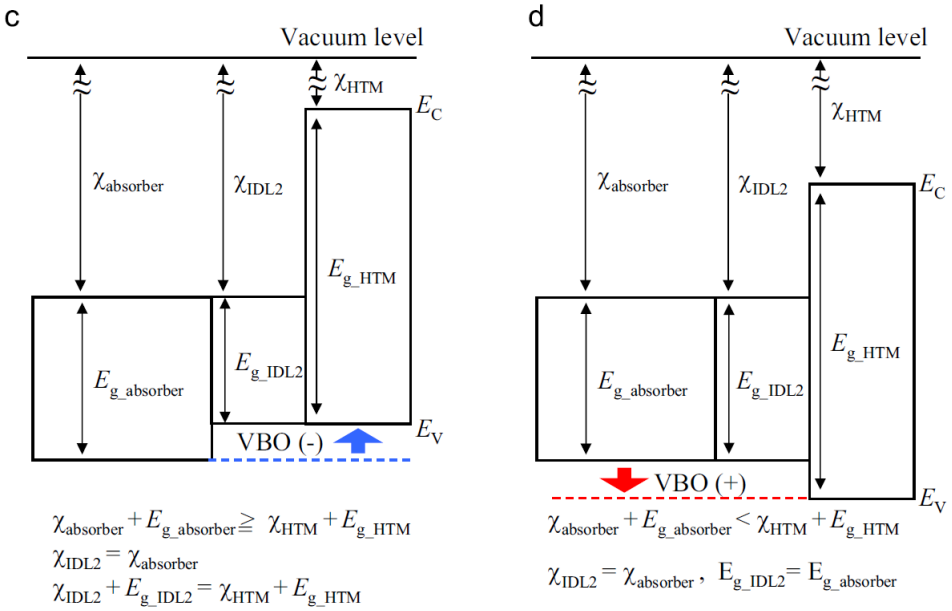


Figure 2.6: Band diagram of device for VBO calculation [10].

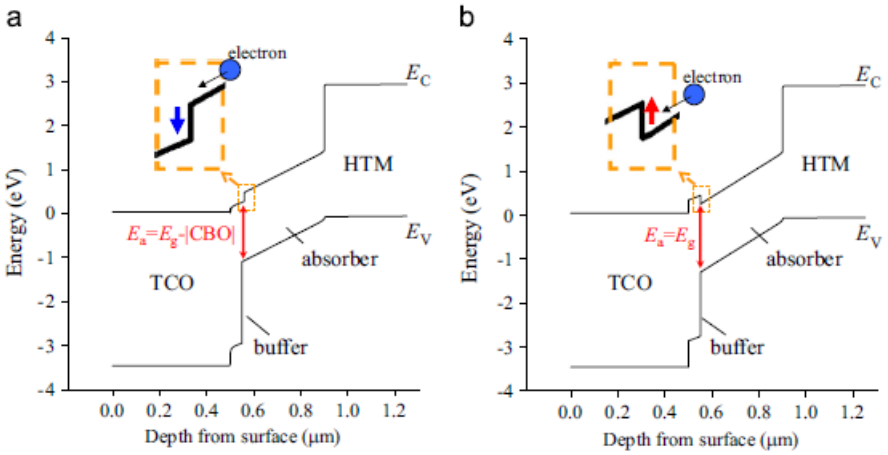


Figure 2.7: Positive and negative CBO [10].

Subsequently, a study reported that the use of PCBM as ETL in PSC device resulted in lower hysteresis compared to ZnO nanoparticle material [55]. It implies that PCBM facilitates electrons transport more efficiently than ZnO nanoparticles. This could be caused by some reasons. For instance, based on the band diagram, the conduction band of ZnO nanoparticles is lower than perovskite creating a cliff. This cliff means that the CBO is negative leading to poor cell performance due to interface recombination. The less efficient electrons transfer of ZnO nanoparticles can alse be caused by lower electron mobility. Additionally, albeit PCBM material produces less hysteresis and higher efficiency than ZnO nanoparticles [55], it suffers from stability issue towards humid condition whereas ZnO nanoparticles has better moisture stability. Thus, the use of PCBM and ZnO nanoparticles as bilayer ETL can be employed to achieve an excellent device with less hysteresis and better stability towards humid condition.

- ZnO nanoparticles/Au interface

  As aforementioned, the wide band gap of ZnO is beneficial to prevent Au migration to the absorber layer. Furthermore, a metal-semiconductor contact is formed between ZnO nanoparticles and Au. This contact creates a Schottky or an Ohmic contact. It can be determined by comparing the work function of those materials. The work function of ZnO nanoparticles and Au is 4

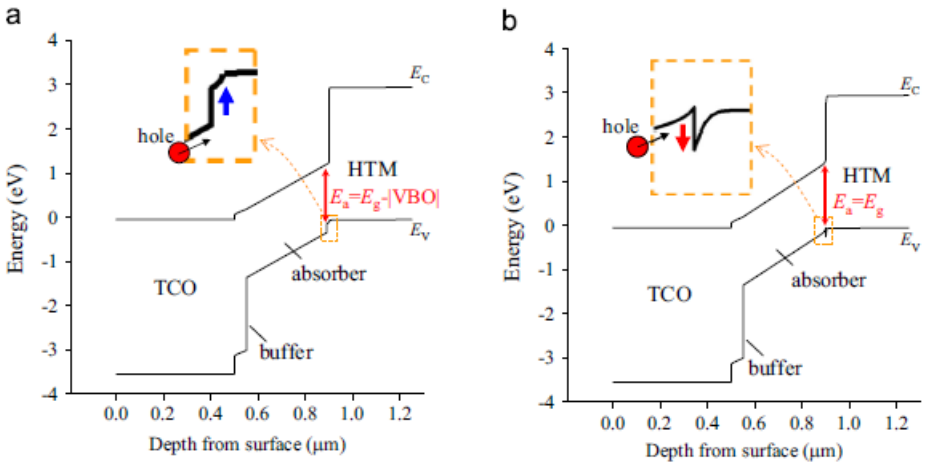


Figure 2.8: Positive and negative VBO [10].

eV [56] and 5.1 eV [50], respectively. The metal electrode has a higher work function than the n-type semiconductor of ZnO nanoparticles. Theoretically, it indicates that the contact of these metal-semiconductor materials forms a Schottky barrier [50]. However, it also depends on the doping of ZnO layer. In our model, the Schottky model was not activated and an ohmic contact was assumed.

2.4. Predicted Equivalent Circuit of PSC

The analysis of simulated band diagram in subchapter 2.3 indicates that the origin of hysteresis effect in PSC device is charge accumulation at the interface of charge carriers transport layer and perovskite layer. Charge accumulation at perovskite and ETL interface is influenced by a spike formed by conduction band of PCBM as ETL acting as a barrier for the electrons. On the other hand, a cliff formed by valence band offset of HTL and perovskite may lead to charge accumulation as well. Furthermore, as discussed in subchapter 1.3.3, prior studies stated that various aspects could be the origin of hysteresis phenomenon in PSC, i.e. trapped/de-trapped charge carriers, ferroelectricity, changes in contact conductivity or absorber, and ion migration [3, 57].

In this project, the possibility of charge accumulation in the bulk of absorber layer will be considered. A study by Sherkar and co-workers reported the mechanism of charge trapped in defect at the grain boundaries of polycrystalline film of perovskite and at the surface of the film [11]. In polycrystalline film, when the orientation of crystal grain is different with grain of neighboring crystal, this can induce defect due to interstitials (misplaced atom), ionic vacancies, and lattice dislocation. The defect can be a trap for the charges. The comparison of trapped charge mechanism between inorganic and perovskite solar cell is illustrated in Figure 2.9.

Based on Figure 2.9, in inorganic solar cell, an empty defect at grain boundary and interface is neutral when there is no charge trapped. Subsequently, when electrons fill the defect, this defect will be negatively charged. A potential barrier is formed and hence, it weakens electron transport. The trapped electron will recombine with hole in valence band. In contrast to this mechanism, an empty defect at grain boundary of perovskite is positively charged because of the accumulation of iodide vacancies. This defect will be neutral when it is filled by electron and no potential barrier is formed. It implies that electron transport is not influenced by potential barrier as occurred in inorganic solar cell [11]. This mechanism is crucial to understand the cause of charge accumulation which takes place in grain boundaries of perovskite and in the interface of ETL/perovskite and perovskite/HTL. Additionally, as explained in Subchapter 1.2.1 that perovskite consists of cation and anion. The iodide vacancies in perovskite is related to the migration of I^- ion. Yuan and Huang reported that ion movement in a solid material is associated with the crystal structure of a material, ionic radius, and the distance of

ion-jumping. Halide ion in perovskite is likely to be the most mobile ion due to the short distance to the nearest iodide vacancy [58].

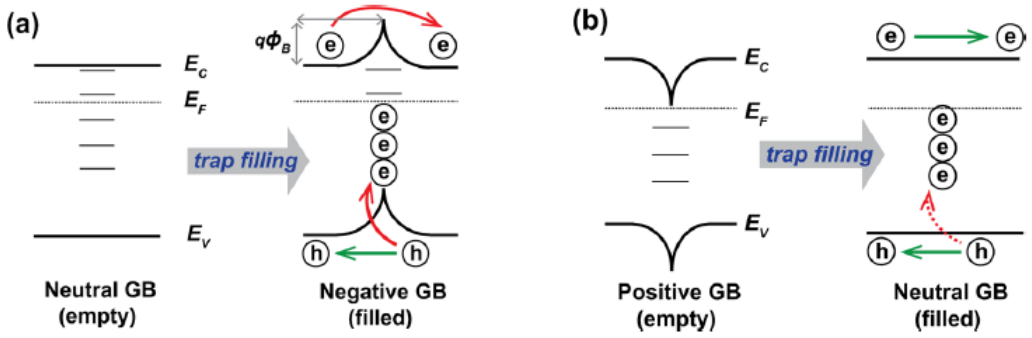


Figure 2.9: An illustration of charge accumulation [11].

The consideration of equivalent circuit of PSC sample is based on charge accumulation occurred in PSC device leading to hysteresis effect. This charge accumulation acts as charge stored in the device. This phenomenon may lead to equivalent circuit which does not follow the general equivalent circuit of solar cell depicted in Figure 1.7. In this project, stored charge due to charge accumulation will be taken into account when proposing an equivalent circuit of a PSC device. Two type of equivalent circuit are proposed in this project. First, an equivalent circuit of solar cell with one capacitor is considered to represent the charge accumulation at grain boundaries of perovskite. The other one is an equivalent circuit with two capacitors which is aimed to reflect charge accumulation at ETL/perovskite and perovskite/HTL interface.

2.4.1. Equivalent Circuit with One Capacitor

In this section, the consideration of equivalent circuit was based on hysteresis originating from charge accumulation at the grain boundaries of perovskite, as reported by Sherkar and co-workers [11]. As depicted in Figure 1.7, the general equivalent circuit of a solar cell consists of a photo-generated current source, a diode, a shunt resistor and a series resistor. The accumulated charges will be represented by one capacitor placed in parallel with photo-generated current source. The photo-generated current source represents charge generation in photoactive layer when light illuminates the device. In a silicon-based solar cell, a diode is used to reflect current flows from cathode to anode of the device through the external circuit. Besides, the J-V characteristic of a pn junction device behaves as an ideal diode [16]. In this project, a p-n junction diode is also employed to represent the junction of HTL/perovskite/ETL of PSC device. The HTL and ETL in the device is a p-doped and n-doped semiconductor, respectively, while perovskite is an undoped material. The diode is assigned in parallel with photo-generated current source and in the opposite direction of the current source. Furthermore, in practice, there is leakage current due to local defect in the junction shunt in the device which leads to a voltage drop [16]. This leakage current is considered by placing a shunt resistor in the equivalent circuit. Finally, a series resistor represents a voltage drop because of resistance that introduced when current from current source flows to the external circuit. The series resistance includes resistance in electrode and bulk of absorber layer [59]. Figure 2.10 depicts the equivalent circuit with one capacitor.

2.4.2. Equivalent Circuit with Two Capacitors in Parallel

Furthermore, the second consideration of the equivalent circuit is based on the charge accumulation occurred at the interface of charge carriers transport layer and perovskite. Two capacitors were used to represent charge accumulation at HTL/perovskite and perovskite/ETL interface. Theoretically, a complete equivalent circuit of a capacitor consists of an ideal capacitor, a series resistor reflecting resistance of the conductive plates, and a parallel resistor related to the leakage current of the dielectric. Figure 2.11 However, resistance of the conductive plates is usually neglected [12]. Thus, in this project, the equivalent circuit of each capacitor only consists of an ideal capacitor and a parallel resistor.

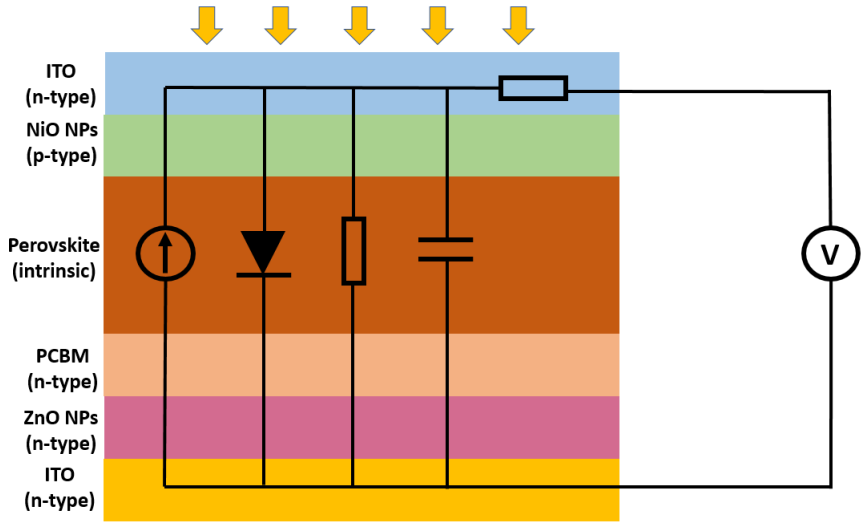


Figure 2.10: Equivalent circuit of PSC with one capacitor.

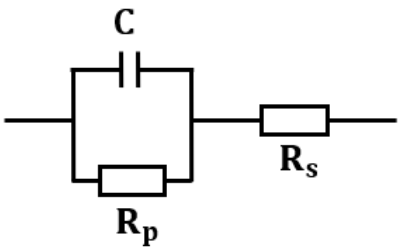


Figure 2.11: An illustration of a complete equivalent circuit of a capacitor [12].

2.5. Conclusion

The purpose of this subchapter is to answer the first research question whether it is possible understand charge accumulation in a PSC from the band diagram and to answer the second research question whether the band diagram can be used to derive an equivalent circuit of PSC. Simulation of band diagram using Sentaurus TCAD was done in dark and short circuit condition. Band alignment of materials composing PSC device was analysed in this chapter.

Based on the simulated band diagram, it was known that the undoped perovskite material has inclined band diagram due to electric field existence in this region. This electric field has significant role to the charge carriers transport. It pushes holes and electron to the hole and electron transport layer, respectively. Band alignment of the materials influences charge carrier selection by HTL and ETL. The conduction band level of PCBM as ETL is close to conduction band of perovskite. However, it forms a spike that would be seen by electrons in perovskite as a barrier. Therefore, when the electric field is insufficient to push the electrons, these negatively charge carriers will be accumulated at the interface of perovskite and PCBM. On the other hand, a highly p-doped NiO nanoparticles was employed as HTL created a good hole-selectivity to the PSC device. The valence band offset of HTL and perovskite formed a cliff which will be beneficial to the holes collection at front electrode. Nevertheless, there is a possibility of charge accumulated in this region which should be considered as the origin of hysteresis phenomenon in PSC device.

The investigation of band alignment shows that there is an indication of charge accumulation occurred at the interface of HTL/perovskite and perovskite/ETL. The charge accumulation acts as charge stored in the device. Furthermore, a study reported that charges can also be accumulated at the bulk of absorber layer [11]. These analyses imply that the equivalent circuit of PSCs may not follow the conventional equivalent circuit of solar cell. Thus, two equivalent circuit topologies were proposed to

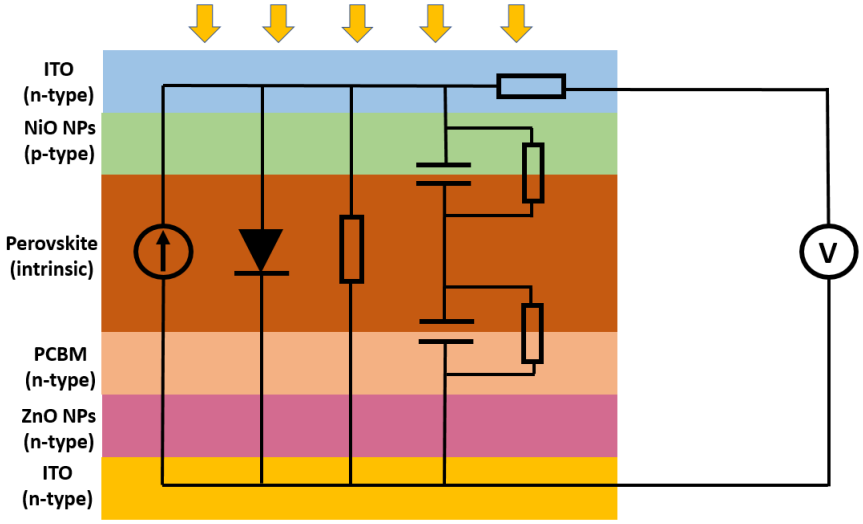


Figure 2.12: Equivalent circuit of PSC with two capacitors.

represent the charge accumulation in PSC device. The first topology leads to one capacitor added to the general equivalent circuit of a solar cell. This capacitor was placed in parallel with the photo-generated current source. It was aimed to reflect accumulated charge at the grain boundaries of absorber layer. The second equivalent circuit refers to an equivalent circuit with two capacitors in parallel. These capacitors represents charge accumulation at the HTL/perovskite and perovskite/ETL interface. Furthermore, verification is required to ensure whether such equivalent circuit can represent the origin of hysteresis effect in a PSC device. This verification will be discussed in Chapter 4.

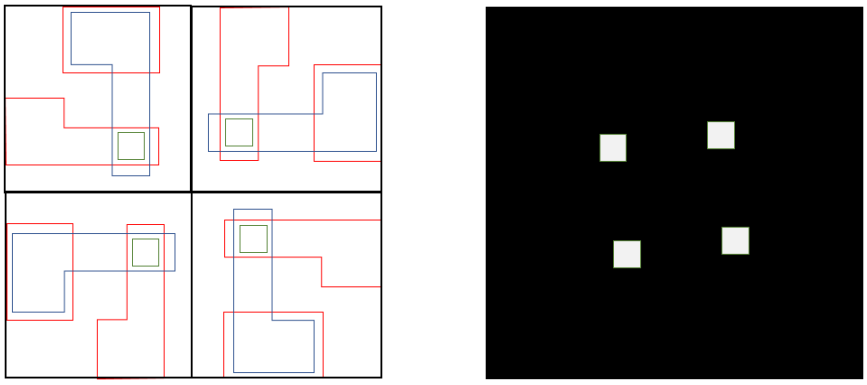
3

Time-resolved I-V measurement

The purpose of this chapter is to investigate hysteresis phenomenon occurring in PSC sample. This purpose is related to the third research question introduced in sub-chapter 1.6 which was *"Is it possible to study hysteresis phenomenon using time-resolved I-V measurement?"*. In order to understand J-V characteristic of the device, time-resolved I-V measurement was performed by measuring *J(t)* as a function of applied voltage. The experimental setup of time-resolved I-V measurement will be discussed in subchapter 3.1. Measurement results will be analyzed in subchapter 3.2. In the measurements, current density *J* was measured as a function of time by applying voltage step. Finally, subchapter 3.3 concludes some findings in this chapter.

3.1. Experimental setup

Time-resolved I-V measurement was done to measure current as a function of time *J(t)* by applying voltage steps. It was measured using Keithley 2601B source meter and a dual light source solar simulator WACOM WXS-156S-10. The dual light source consists of halogen and xenon light bulbs which were used to simulate standard test condition AM1.5 solar spectrum of 1000 W/m^2. Moreover, a sample stage equipped with a temperature controller was used to maintain a standard test temperature condition of 25°C to obtain a reliable result. Before starting the measurement, calibration was done to verify spectral matching of the light source of solar simulator using two monocrystalline silicon Fraunhofer ISE reference cells. During the measurement, our PSC sample was masked using a black paper sheet with an aperture area of 3x3 mm^2. Figure 3.1 depicts a schematic illustration of the cells, which consist of four cells, and the mask. All results showed in next subchapter were based on one cell. The four-point-probes method was used in the measurement to reduce parasitic resistance created between surface of material and probes which touched the surface.



(a) (b)

Figure 3.1: The schematic illustration of PSC sample and the mask.

The time-resolved I-V measurement was done by backward scan (voltage was applied from 1.1 to -0.1 V), followed by forward scan (voltage was applied from -0.1 to 1.1 V), without a waiting time. The waiting time is referred to time between backward and forward scan measurement. The voltage step was created by setting up a voltage increment of 50 mV. The time of each step was determined by a multiplication of total data points and the integration time between two data points. Figure 3.2 shows a schematic illustration of the voltage steps. In this experiment, in order to determine Δt, 500 data points and integration time of 0.2 ms were used as the input leading to time per each step of 100 ms. Scan rate was specified by dividing ΔV with Δt. Various voltage increments were applied to understand the influence of different scan rates on hysteresis phenomenon in the device. The ΔV was varied by 40 mV, 30 mV, 20 mV, and 10 mV. Additionally, Δt was varied by 0.1 s, 0.5 s, and 1 s.

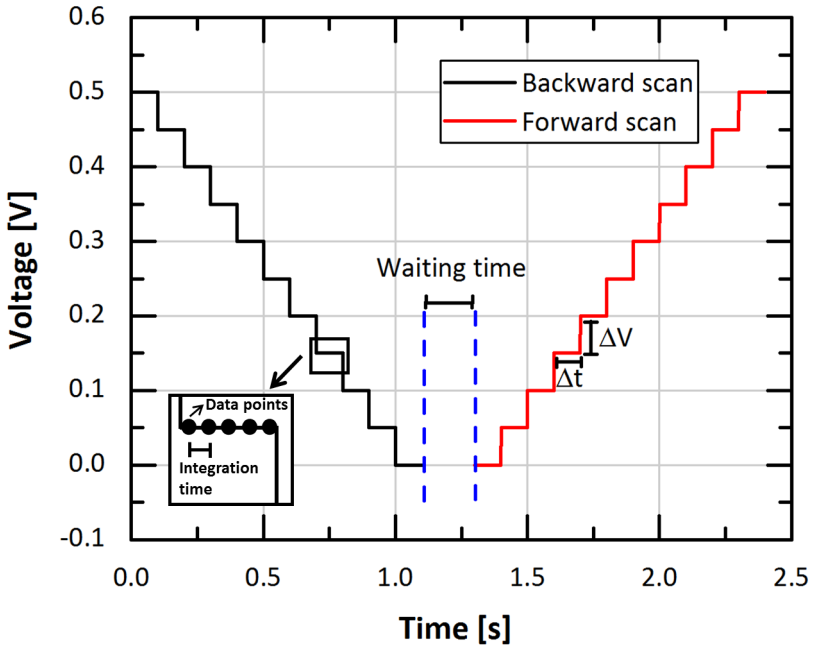


Figure 3.2: An illustration of voltage steps used in the measurement.

3.2. Experimental Result

As explained in subchapter 1.2.2, PSC sample was fabricated by Solliance Solar Research. It had a planar structure consisting of ITO/NiO nanoparticles/$Cs_{0.05}MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.9}Br_{0.1})_3$/PCBM/ZnO nanoparticles/Au. The sample was measured by applying staircase voltage steps resulting in current density as a function of time *J(t)*. It is worth noting that the measurement should be done when the stabilized efficiency has been achieved. The stabilization affects accuracy of the experiment. For instance, when the cell was measured before achieving stabilized efficiency, the result would change for the next measurement. Thus, it might not give an accurate result. The stabilization process was done by tracking the output power for a certain time. In Solliance, the stabilized efficiency was achieved by tracking output power of the device for 300 s. In this project, the stabilization was done manually by placing the cell under illumination for 300 s. The time required for the stabilization process may differ for different device architectures. It considerably relies on materials and on prior measurement of the device.

3.2.1. J-V characteristic

Hysteresis phenomenon is introduced by different maximum power point (MPP) in the J-V curve as an effect of different voltage scan direction. MPP denotes a point on J-V curve at which the device

generates maximum power output [16]. However, the phenomenon occurs in specific PSC devices. It implies that different PSC stack materials arrangements result in different J-V behaviours when voltage is swept in forward and backward scan directions. Thus, J-V characterization of PSC sample was done to analyze the hysteresis effect in the device. Figure 3.3 depicts the J-V curve of the sample when forward and backward scan were applied to the cell. Results were presented as current density by excluding active area of the cell so it would be easier to identify the current generated by the cell was. Based on the measurements, our PSC sample had high J_{sc} and V_{oc} but low FF, leading to efficiency of 11.24% and 11.95% for forward and backward scan, respectively. High V_{oc} is a result of a wide band gap of perovskite material of 1.55 eV.

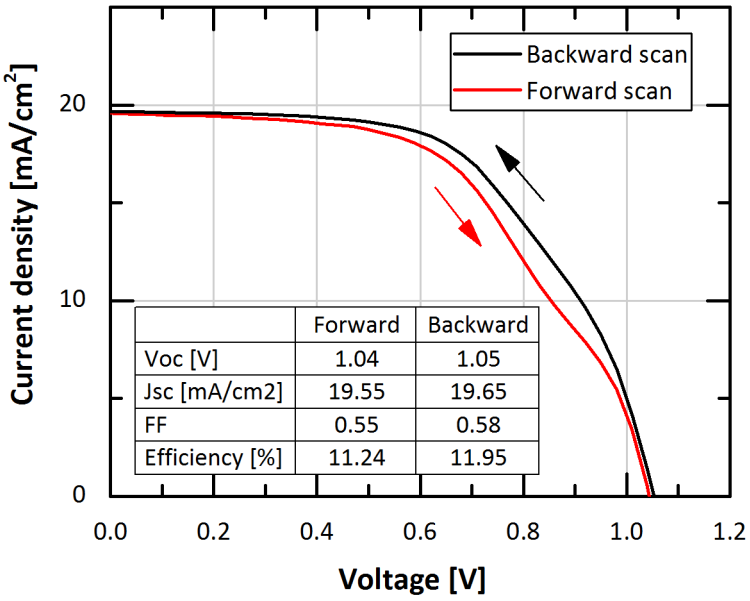


Figure 3.3: The J-V curve of forward and backward scan of PSC sample.

Additionally, hysteresis effect is influenced by scan rates. Thus, measurements using various scan rates were considered in this project. As explained in subchapter 3.1, scan rate was derived by dividing voltage increment ΔV and time of each votage step Δt. Thus, the variation of scan rates can be determined by varying voltage increment or time of each step. In this project, scan rate was varied by altering voltage increment to 50 mV, 40 mV, 30 mV, 20 mV, and 10 mV while maintaining Δt of 0.1 s. It produced a scanning rate of 500, 400, 300, 200, and 100 mV/s. Figure 3.4 depicts all measured J-V curves with various voltage increments of forward and backward scan. It indicates that scan rates influences the hysteresis phenomenon. Theoretically, hysteresis effect is less severe when scan rate decreases [46] because steady-state current density is achieved. However, other studies found that hysteresis effect increased with scan rate reduction [37]. Thus, it is still unclear how hysteresis effect is influenced by the scan rates. Thus, further experiments were done to understand how hysteresis effect altered with different measurement methods consisting of:

- Backward scan followed by forward scan without waiting time
- Backward scan followed by forward scan with waiting time of 12 s
- Forward scan followed by backward scan without waiting time
- Forward scan followed by backward scan with waiting time of 12 s

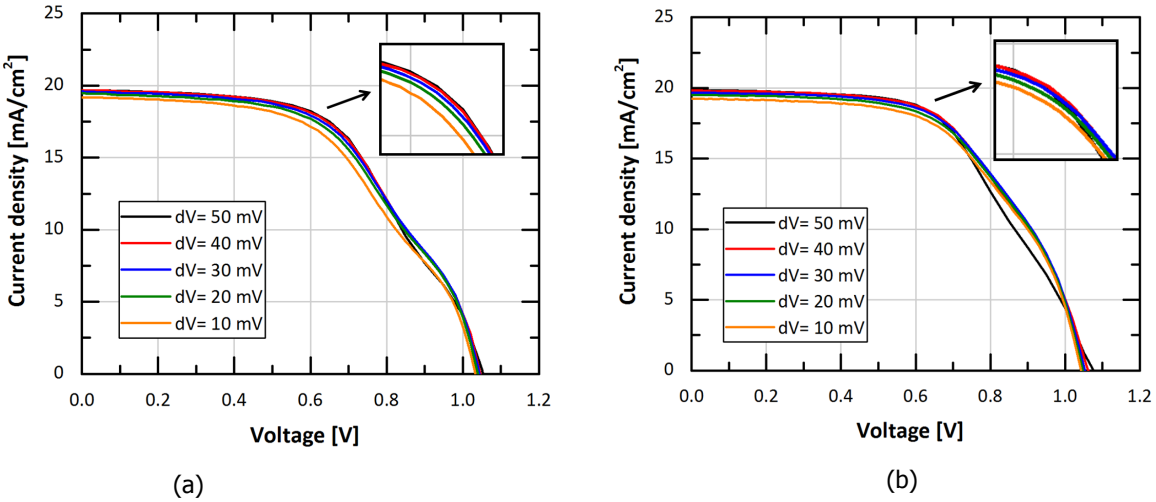


Figure 3.4: The J-V characteristic with various scan rates of (a) forward and (b) backward scan direction.

The waiting time in the measurements was applied manually. During the waiting time, no light illuminated the cell and no voltage was applied. A hysteresis constant was introduced to obtain better comparison of cell performance under various scan rates with different methods. Efficiency will be used to determine a hysteresis constant as a figure of merit for evaluating hysteresis effect severity. Hysteresis constant was calculated by subtracting efficiency of forward from backward scan [46]. Therefore, higher hysteresis constant leads to a more severe hysteresis effect. Figure 3.5 shows the hysteresis constant as a function of scan rate. Positive values of hysteresis constant implies that backward scans have higher efficiency than forward scan. When backward scan was measured before forward scan either with or without waiting time, hysteresis increased with reducing scan rates. In this case, when voltage was swept with fast scan rate, it gave a small chance to the charge accumulation to occur in the device. It will result in higher generated current density and hence, lower hysteresis effect. Conversely, slow scan rate leading to larger chances of charge accumulation in the device and thus, more severe hysteresis phenomenon. When forward scan was measured before backward scan, it resulted in a reduction of hysteresis phenomenon as scan rates decreased. On the other hand, with waiting time, the results showed that waiting time induced higher hysteresis effect than experiment without waiting time.

3.2.2. Transient response on J-V curve as a function of time

Analysis of current responses as a function of time towards staircase voltage sweep was also considered in this project to understand *J(t)* characteristics. The result of time-resolved I-V measurements presented *J(t)* as a function of applied voltage. Figure 3.6 depicts *J(t)* of forward and backward scan. Both forward and backward scan exhibited transient current density responses as voltage steps were applied representing a capacitive behaviour. The under- and overshoot in the transient responses of forward and backward scan were opposite to each other which were in agreement with the transient response introduced in subchapter 1.3.3. Exponential rise and decay in the *J(t)* of forward and backward scan, respectively, increased with applied voltage leading to a non-steady-state current density. The non-steady-state current density will reach a steady-state condition with longer time of each voltage step. In other words, it is related to the variation of Δt as discussed in previous subchapter.

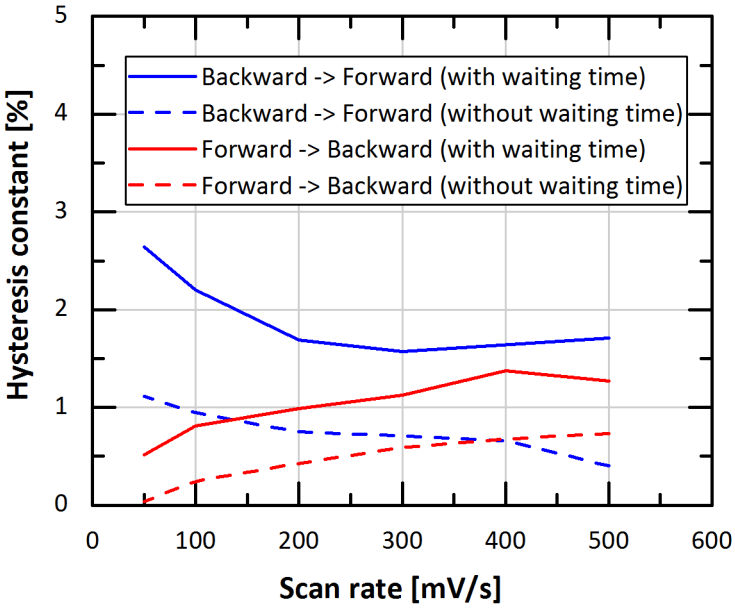


Figure 3.5: Hysteresis constant as a function of scan rates.

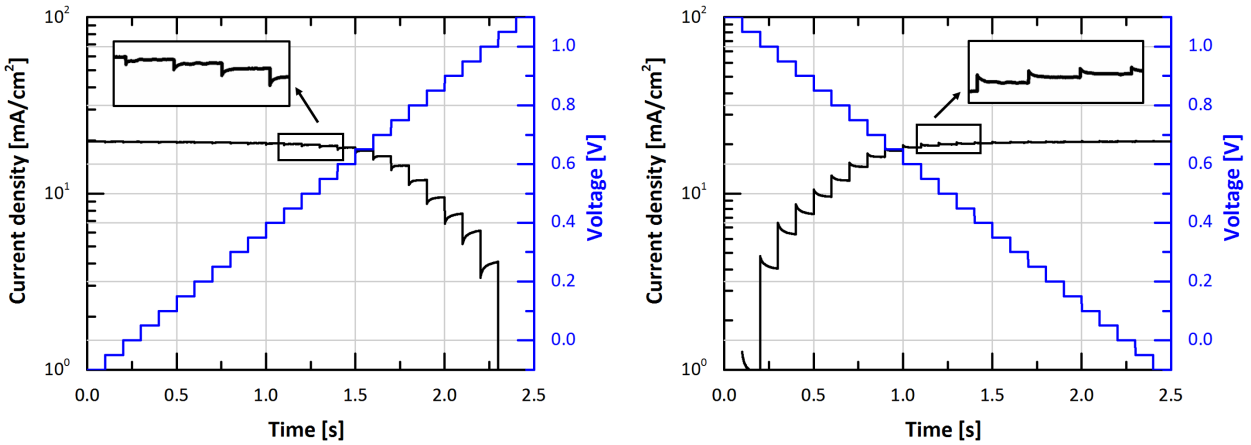


Figure 3.6: The J-V characteristic as a function of time of (a) forward and (b) backward scan direction.

Furthermore, *J(t)* was obtained by considering the exponential function formulated in Equation 3.1, adapted from [3]. In the equation, A is the pre-exponential factor of the transient curve, t_0 represents the starting time of each voltage step, τ defines the time constant, and J_{ss} is the steady-state current density. Figure 3.8a and 3.8b depict the time constant of forward and backward scan of each voltage step from 0.55 to 0.9 V. These time constants were extracted from time-resolved I-V measurement with ΔV of 50 mV and Δt of 0.1 s. The ΔJ represents the difference between current density as a function of time and the steady-state current density formulated by Equation 3.2. Figure 3.7 shows an illustration of *J(t)* at a certain applied voltage step.

$$J(t) = Aexp\left[-\frac{(t-t_0)}{\tau}\right] + J_{ss} \tag{3.1}$$

$$\Delta J = J(t) - J_{ss} \tag{3.2}$$

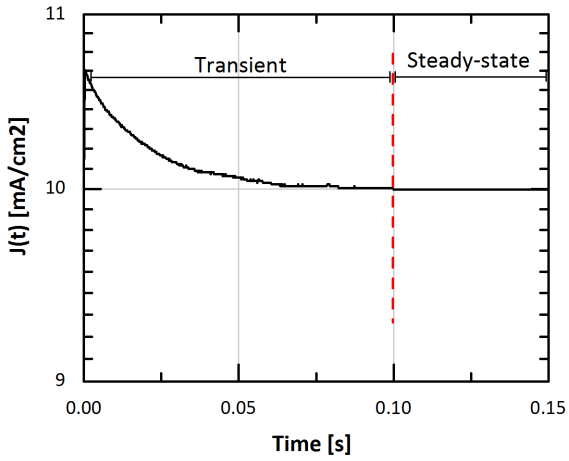


Figure 3.7: An illustration of a transient current density response *J(t)* of a certain voltage step.

- Time constant
  The time constant of forward and backward scan exhibit similar behavior although they are in the opposite to each other. This behaviour refers to the increase of time constant when applied voltage increases. In terms of the equivalent circuit, time constant is related to resistance and capacitance where a multiplication of these parameters yields a time constant. Furthermore, since capacitance is proportional to amount of charges in the device, it indicates that time constant has a correlation with charges storage. The stored charges refers to charge accumulation occurred either in the bulk of perovskite, HTL/perovskite interface, or perovskite/ETL interface. Figure 3.8c and 3.8d depict the distribution of time constant along the staircase voltage sweep of forward and backward scan. These figures provide a significant insight that time constant of each voltage step was not constant. Since time constant was derived from transient current density responses, it can be stated that time constant was a function of applied voltage. Those figures show that a highest time constant of both forward and backward scan was achieved with applied voltage of approximately 0.9 to 1 V. Subsequently, when a larger voltage was applied to the device, time constant tended to decrease.

- Steady-state current density

  Figure 3.9a and 3.9b depict the distribution of steady-state current density J_{ss} of forward and backward scan at ΔV of 50 mV and Δt of 0.1 s. Based on these figures, the J_{ss} decreases with increasing voltage either at forward or backward scan. The non-steady-state and steady-state current density should be considered when plotting the J-V curve of the cell. When J-V characteristic is generated using non-steady-state current density, it may lead to under- or overestimation of efficiency. Additionally, in order to understand correlation between J_{ss} and time per each step, measurements of various Δt were also done. Figure 3.10 depicts a transient current density response of a voltage step when Δt was varied by 0.1, 0.5, and 1 s but ΔV was maintained at 50 mV. Scan rate reduces with increasing Δt. In the figure, Δt was only shown until 0.1 s, which was the smallest Δt, to give better illustration of the comparison of those various Δt. For one voltage step, *J(t)* with Δt of 0.1 and 0.5 s has reach a steady state condition whereas *J(t)* with Δt of 1 s has not reach a steady-state condition. It indicates that the longer Δt the longer time required to reach the steady-state condition.

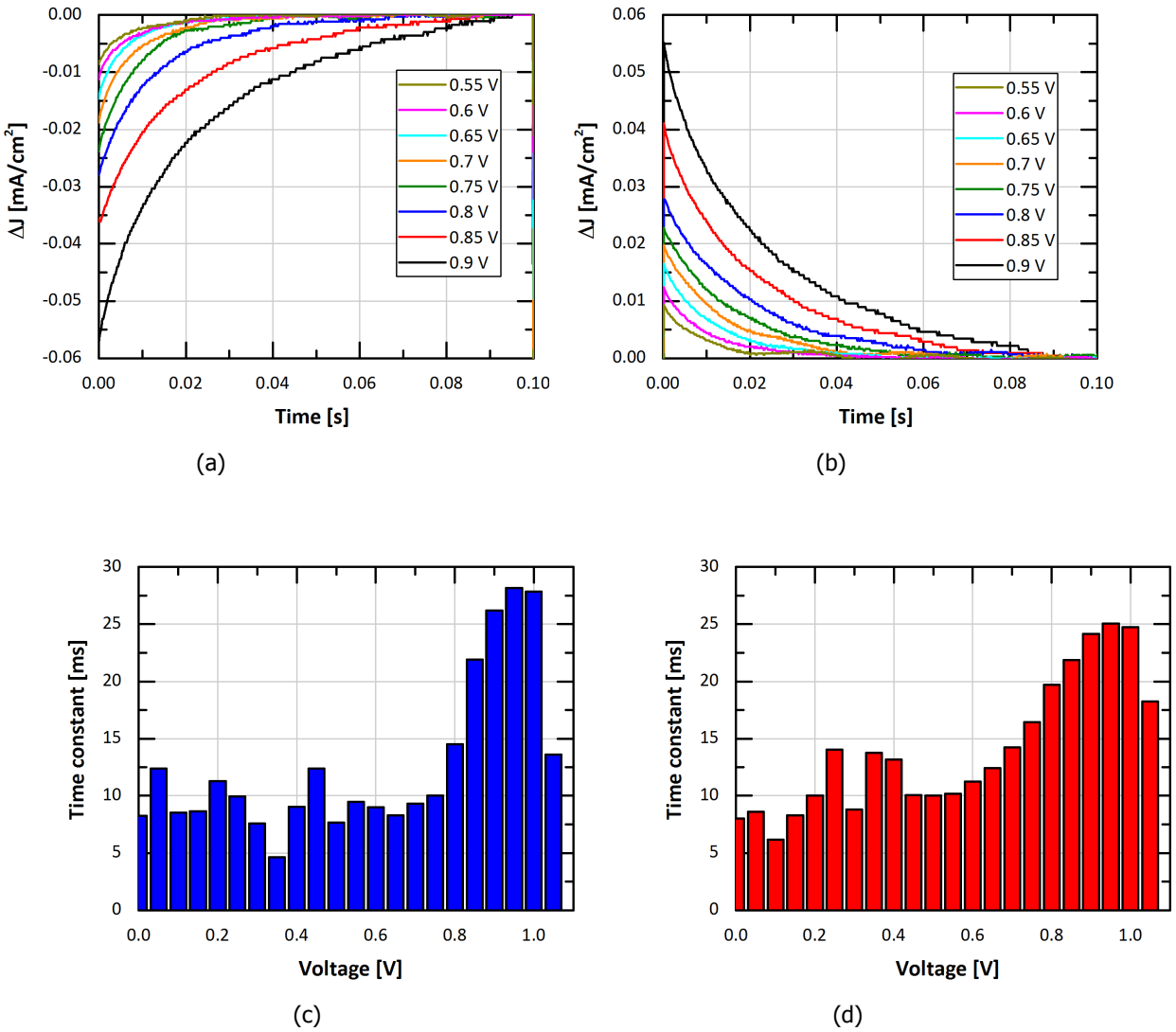


Figure 3.8: Time constant of each voltage step measured at (a) forward and (b) backward scan direction; distribution of time constant of (c) forward and (d) backward scan.

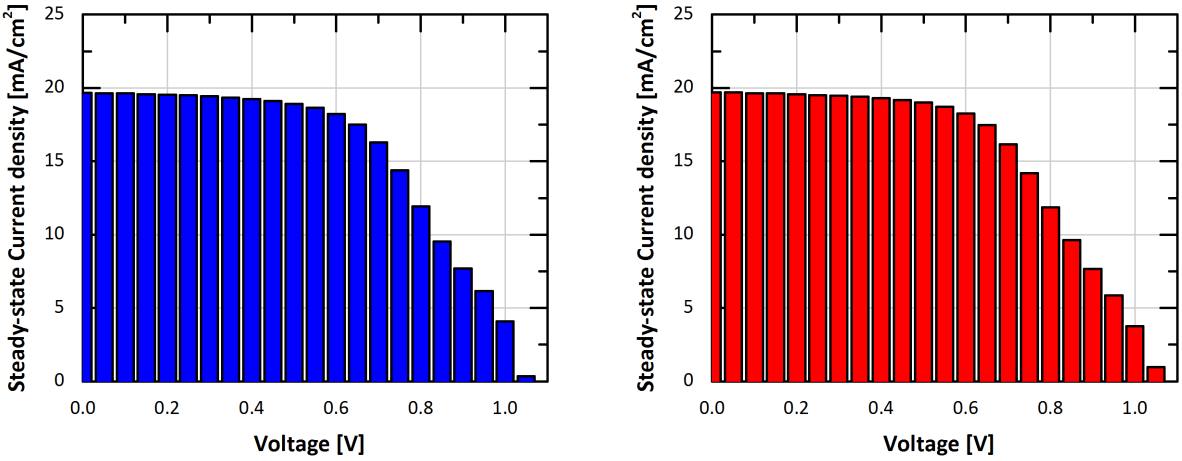


Figure 3.9: Distribution of steady-state current density of (a) forward and (b) backward scan.

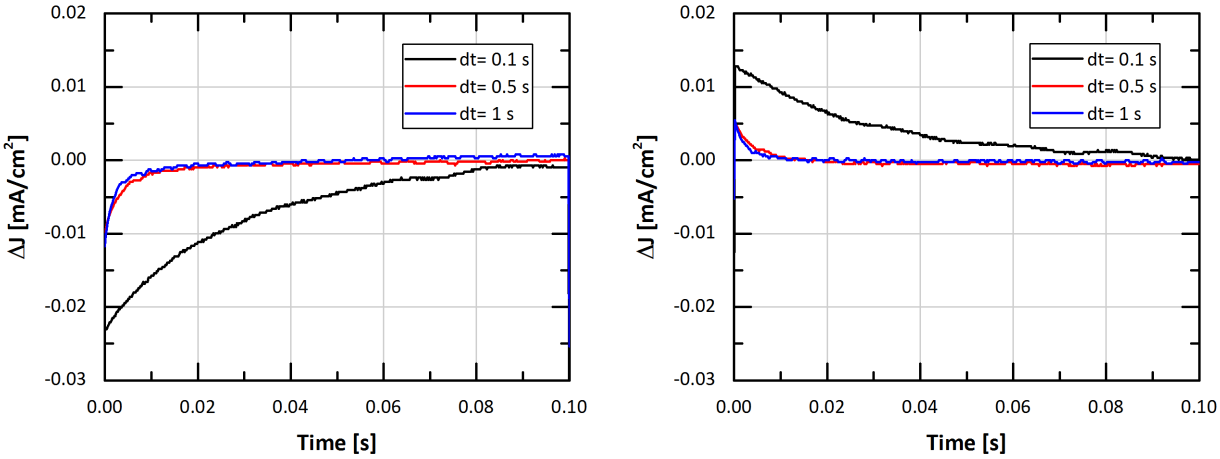


Figure 3.10: A transient current density response of a voltage step with various Δt.

3.2.3. C-V characteristic

Additionally, since time constant is related to capacitance, further analysis of capacitance characteristic as a function of applied voltage is crucial to obtain more insight in charge accumulation in a PSC device. C-V curves of forward and backward scan plotted in Figure 3.11 were derived from time constant. Capacitance was presented as a coefficient obtained by dividing time constant with resistance. The C-V curve shows a non-linear and fluctuate capacitance at low applied bias region. Capacitance increases until it reaches a peak at approximately 0.9 V. Subsequently, it decreases after exceeding the peak.

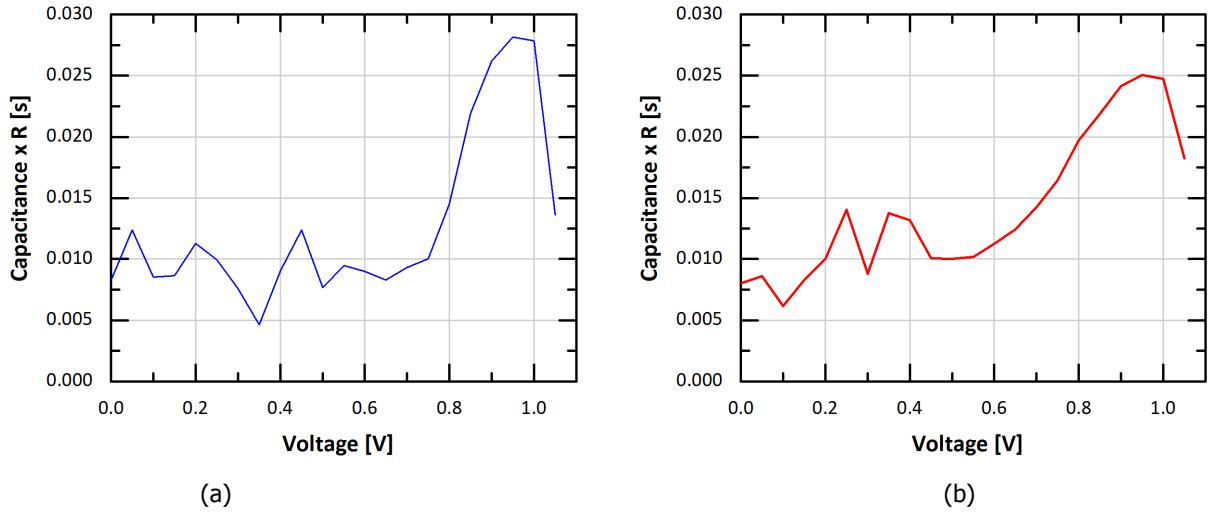


Figure 3.11: C-V characteristic of (a) forward and (b) backward scan.

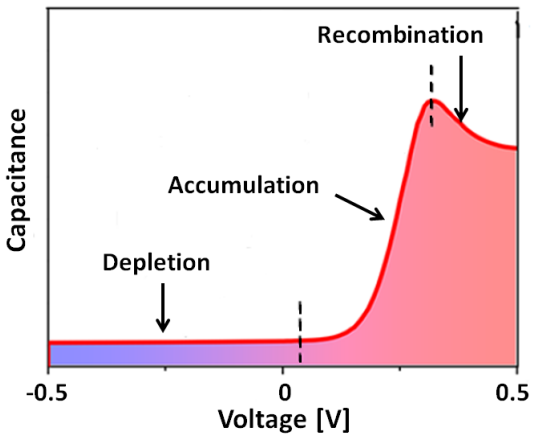


Figure 3.12: The schematic diagram of C-V characteristics [13].

The C-V characteristic in this project corresponds to a study by Wu and co-workers [13] that did a CV measurement of a PSC device. Albeit materials of their PSC were different from materials in this project, a comparison of C-V characteristic can be useful to obtain a better understanding about capacitance on the cell which is dependent on the applied voltage. They reported the correlation of capacitance and applied voltage in a PSC based on a CV measurement. It was done by scanning a dc voltage (from -0.5 to 1.5 V) at a low alternating voltage of 50 mV at 5 kHz under various light intensities from 0.1 to 1 sun illumination. C-V characteristics reported by their study were similar to C-V curve depicted in Figure 3.12 even though the curve was generated from a Silicon-based solar cell. In the figure, C-V curve was divided into three regions consisting of depletion region, charge accumulation region, and charge recombination region. In the research [13], various PSC device architectures were used, i.e. PSC devices with or without Cl^- ion and a PSC without perovskite layer.

Based on Figure 3.12, it is known that when the applied voltage is in the transition of low to high voltage region, built-in voltage reduces leading to charges accumulation. This charge accumulation results in increase of capacitance. Further increase of applied voltage exceeding the peak will decrease the built-in voltage. Thus, a recombination of charge carriers dominates and capacitance diminishes. In this project, the C-V correlation of the device is difficult to analyze since capacitance was only derived from the time constant. However, it shows similar trend to the literature which has a peak at high voltage region and a slope at the region between low and high voltage. A C-V measurement is

required for further research.

3.3. Conclusion

This chapter discussed time-resolved I-V measurement which was done by applying staircase voltage steps to obtain current density as function of time. It was aimed to answer the third research question which was *"Is it possible to study hysteresis phenomenon using time-resolved I-V measurement?"*. As depicted in Figure 3.3, the J-V curve produced by PSC sample had different maximum power point with different voltage scan direction. Backward scan resulted in higher maximum power point compared to forward scan. The J-V curve difference indicates hysteresis effect occurrence in the sample. Thus, it means that it is possible to study hysteresis phenomenon using time-resolved I-V measurement.

Hysteresis phenomenon in a PSC device is not only influenced by scan direction but also scan rate. Thus, in order to obtain more insight about it, further research was performed by varying the voltage increment of 50, 40, 30, 20, and 10 mV, leading to various scan rates. Hysteresis constant was introduced in this chapter to compare how severe hysteresis effect experienced by the cell was. Higher hysteresis constant implies more severe hysteresis phenomenon. Based on measurements, forward scan was measured after backward scan without waiting time. It resulted in less severe hysteresis effect than measurement with waiting time. Furthermore, hysteresis effect became more severe with decreasing scan rate.

The *J(t)* characteristic was also studied in this chapter. A transient current density response was obtained by introducing staircases voltage sweep. The transient response formed an exponential decay for backward scan and an exponential rise for forward scan. This transient current density response reflected time constant of each voltage step. The time constant increases from low to high applied voltage until around 0.9 V and decreases after exceeding 0.9 V. Time constant is related to capacitance. Thus, the increase of time constant with applied voltage resulted in increase of capacitance. Moreover, capacitance corresponds to stored charges in the device. This stored charges refer to charges accumulation at grain boundaries of perovskite or the interface between charge transport layer and perovskite. It is worth noting that with increasing applied voltage, more charges will be accumulated inducing higher capacitance until at a certain voltage. Finally, the J-V characteristic, transient current density response, and C-V characteristic obtained from time-resolved I-V measurements gave a better understanding of hysteresis phenomenon in our PSC sample.

4

Electrical Modeling

This chapter presents simulation of equivalent circuit model of PSC device. The purpose of this chapter is to answer the main scientific research question that was introduced in subchapter 1.6:*"Is it possible to model hysteresis of the PSC with an equivalent circuit?"*. Moreover, we will discuss the design of the equivalent circuit that can reproduce measurement results, referring to the fourth research question. To answer these questions, an appropriate model is required to produce the hysteresis effect occurred in the PSC device. In this study, the equivalent circuit of perovskite solar cell was modelled by Quite Universal Circuit Simulator (QUCS). QUCS is an integrated circuit simulator with a graphical user interface (GUI). It assists the user to setup the circuit by providing the component library. It also supports assorted simulation types, such as DC, AC, S-parameter, parameter sweep, and transient simulation.

4.1. Equivalent Circuit Simulation with QUCS

4.1.1. Introduction of QUCS

QUCS is a free-licensed circuit simulator that can be downloaded from *http://qucs.sourceforge.net*. The GUI is used to create and edit the schematic of an electrical circuit, to display result of the simulation, and provides setup of simulation. Components required to create the schematic are provided by Components tab in Main Dock. It contains lumped components (i.e. resistor, capacitor, ground), source (i.e. AC and DC sources), probes (i.e. current and voltage probe), simulations setups (i.e. AC, DC, and transient simulation), diagram (i.e. cartesian and tabular), etc. Figure 4.1 shows the graphical user interface of QUCS.

In this project, voltage step is used to measure the current response to abrupt changes of applied voltage. A slow current response leads to current lagging and introduces capacitive behavior as explained in subchapter 1.3.3. This capacitive behavior indicates that hysteresis phenomenon occurs in the device. The built-in voltage source provided by source component in QUCS is not sufficient to produce the staircase-like input voltage. Hence, voltage step source should be created by user. The methods will be discuss in subchapter 4.1.2. Furthermore, transient simulation was used to analyze the J characteristics as a function of time by applying voltage steps. The explanation will be provided in subchapter 4.2.2.

4.1.2. Voltage Source Creation

Voltage source implies the bias voltage output of the solar cell which also performed as the source for the load. The purpose of this subchapter is to discuss methods to create voltage source. The voltage source contained several steps establishing staircases. As explained in subchapter 3.2.2, the voltage step is related to the voltage increment and time of each step. The device performance was measured by applying voltage in different scan sweep directions consisting of forward and backward scan direction. Forward scan implies when the voltage is swept from negative to positive voltage, while

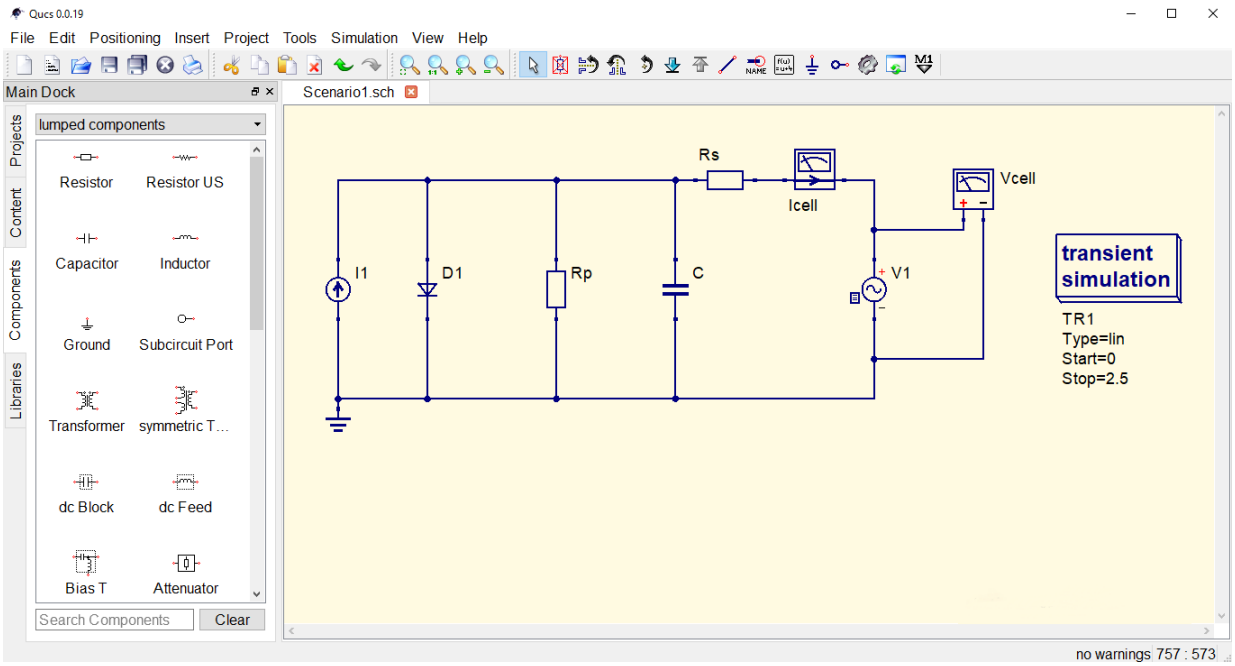


Figure 4.1: The graphical user interface of QUCS.

backward scan is when voltage is swept from positive to negative values [31]. Two methods can be used to create voltage source with QUCS:

- Manual method

  This method refers to a multiple step function to create a staircase voltage source. This voltage source was created by connecting several voltage source elements in series. This voltage source element is provided in the components library in QUCS, named Voltage Pulse. It contains four important parameters, which are U1, U2, T1, and T2. U1 defines the voltage before and after the pulse, U2 represents the voltage of the pulse, T1 is the starting time of the pulse, and T2 implies the finishing time of the pulse. In manual method, there are two approaches to create the voltage source. Firstly, the voltage pulse is maintained for a given time duration. The time duration was defined by the time of each voltage step. When the first pulse ends, the second pulse starts. For instances, in the case of forward scan, a voltage pulse of 0.05 V is maintained for 15 s, which is the time of 1 voltage step. It stops immediately after 15 s. Next voltage pulse starts after the first pulse ends, which is at 0.1 V. It will be maintained for the next 15 s. These steps continue until the final voltage of 0.25 V is achieved. Figure 4.2 depicts the illustration of this first approach for forward scan case.

  The second approach is slightly similar to the first approach. The difference is each voltage pulse will be maintained until the final voltage is achieved. Total time implies duration of time when the first voltage pulse applied until the last pulse ends. Subsequently, when the second pulse starts, the first pulse is still being maintained. In this case, the voltage pulses have the same amplitude and they add up because they remain in the circuit and they are connected in series. This second approach is illustrated in Figure 4.3 in the case of forward scan. In this figure, voltage pulse is kept at 0.05 V from the beginning of pulse into the pulse ended approximately at 100 s. In manual method, voltage source is arranged by a number of voltage pulse elements. Thus, when this voltage source is connected to other elements (i.e diode, series and shunt resistor), a very large equivalent circuit will be formed. Hence, introducing a subcircuit to the main circuit is recommended to simplify the control of simulation. It is done by separating the voltage source from those other elements in different files. These files will be connected by the subcircuit which has two ports. In a file which contains a set of voltage pulse elements, a port is placed on the first voltage pulse element and the other port is placed on the last voltage pulse element. The output voltage will be used as the input to the main circuit. Moreover, a subcircuit is adjusted to

the other simulation file that consist of main elements, i.e. a DC current source, a diode, a series and a shunt resistor. These two approaches of manual method are not effective to handle a large number of voltage steps because of being the time-consuming. Thus, it would be suitable for a small number of voltage steps.

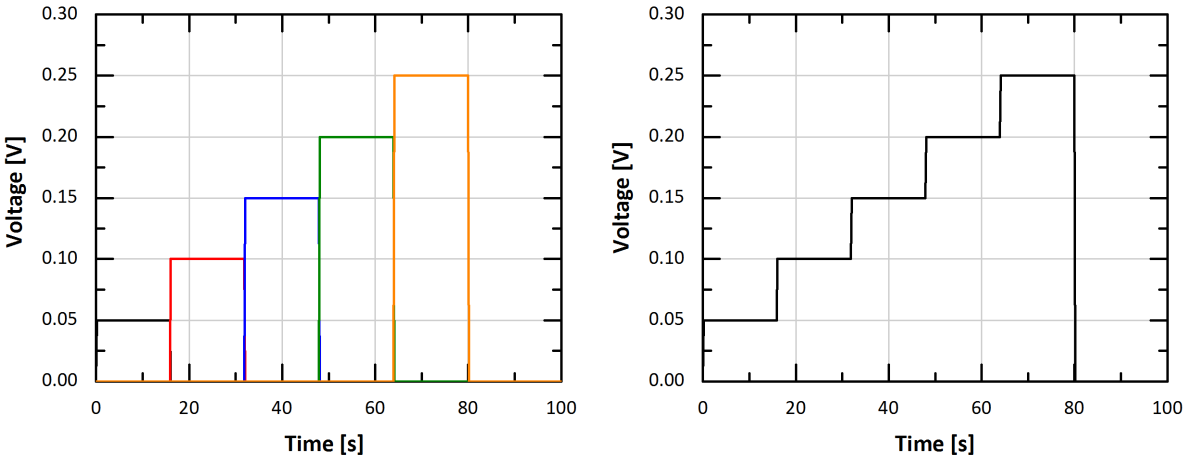


Figure 4.2: An illustration of voltage source creation of forward scan with first approach manual method: (a) voltage pulses and (b) a staircase voltage source.

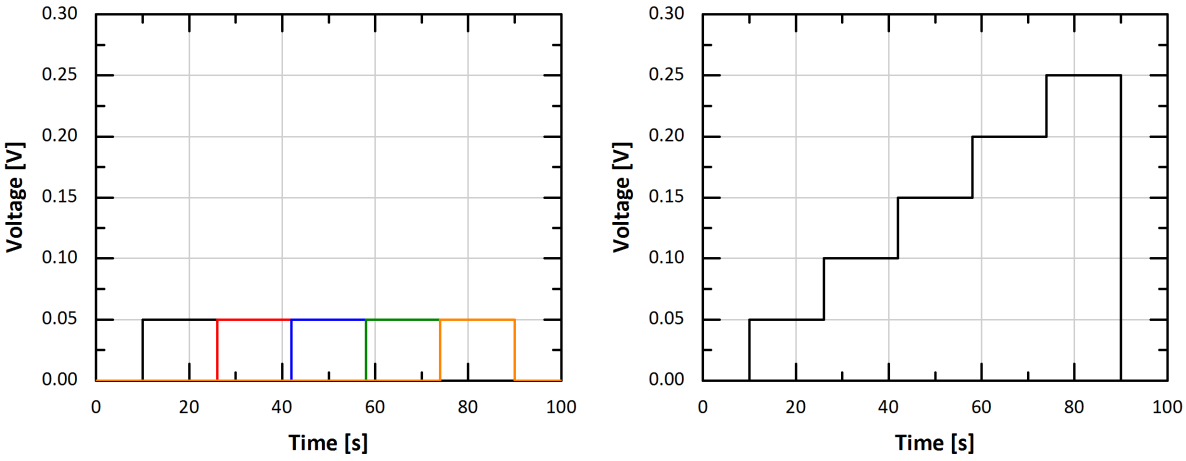


Figure 4.3: An illustration of voltage source creation of forward scan with second approach manual method: (a) voltage pulses and (b) a staircase voltage source.

- File based method

  Additionally, there is a file based method which is simpler and less time-consuming. In this method, a staircase voltage source was created manually using a .dat or .csv format file. The file contains columns of time and voltage. For example, in the case of forward scan when voltage is swept from -0.1 to 1.1 V, the voltage difference is 1.2 V. If a voltage increment of 50 mV is used, 25 voltage steps are established. Time of each step is determined based on the experiment work which is 0.1 s. It implies that every 0.1 s, voltage applied to the device changes. In contrast to

manual method, file based method only requires one voltage source element that makes it easier to handle a large number of voltage steps. Hence, file based method is used in this project.

4.1.3. Transient Simulation

Transient simulation is provided in the components library of QUCS. It is employed to simulate equivalent circuit which contains energy storing components, such as a capacitor and/or an inductor [60]. It implies that transient simulation is related to a network response as a function of time which is relevant to the measurement discussed in subchapter 3.2.1. The *J(t)* characteristic was obtained by time-resolved I-V measurement. Properties of transient simulation are related to parameter of time. They contain start and stop time of a simulation and total number of points for the simulation. In terms of forward scan (from -0.1 to 1.1 V) with certain voltage increment (50 mV) and sweep time (0.1 s per voltage step), the total time sweep is 2.5 s which will be used as an input for stop time. Five hundred data points of each step resulted in total number of points of 12500 in the simulation.

4.2. Simulation Integration of QUCS and Matlab

It is crucial to consider *J(t)* curve result from experiment depicted in Figure 3.6a and 3.6b that exhibit a capacitive behavior. This capacitive behavior might represent charge accumulation occurred in PSC sample. Simulation of *J(t)* curve fitting is essential to compare *J(t)* produced from the predicted equivalent circuit of PSC device in QUCS to *J(t)* from measurement. The *J(t)* curve fitting was done using Matlab. The methodology is provided in this subchapter.

4.2.1. Exporting Equivalent Circuit parameters from QUCS to Matlab

It is worth mentioning that equivalent circuit in QUCS can be exported to Matlab so that the curve fitting can be simulated internally in Matlab. Figure 4.4 shows a schematic diagram of the simulation process.

4.2.2. *J(t)* curve fitting method

After running a simulation in QUCS, a netlist will be created and displayed by text editor in .txt format. The netlist contains simulation information of all components in the circuit and the type of simulation, which is transient simulation in this case. As shown in Figure 4.4, the netlist will be exported to Matlab. Netlist provides parameters of elements that form the equivalent circuit. Some guess parameters are required as input in Matlab. These guess parameters will substitute parameters value in the netlist and thus, a new netlist will be created. This new netlist is imported to QUCS using a *dos* function resulting in *J(t)*. The result is in a file with .dat format. *J(t)* curve fitting was done using *fminsearch* function aiming at minimizing the discrepancy between *J(t)* of measurement and simulation. When the minimum discrepancy has not achieved, Matlab will try other guess parameters until a minimum discrepancy is achieved. The average discrepancy of *J(t)* will be termed as error in this simulation.

4.3. Scenario 1: Equivalent Circuit with One Capacitor

Equivalent circuit with one capacitor is derived from the analysis of band diagram of the PSC sample discussed in Chapter 2. One capacitor is considered to represent charge accumulation occurs in grain boundaries of absorber layer. Based on Chapter 3, it was shown that the capacitance was a voltage-dependent parameter. However, in this simulation, a built-in capacitor component was used as it was provided by library in QUCS. Figure 4.5 shows a schematic overview of the equivalent circuit. In this scenario, there are six parameters that are required as input for guess values.

4.3.1. *J(t)* curve Fitting of Forward and Backward scan with Voltage Increment of 50 mV

Before doing *J(t)* curve fitting, it is important to simulate the J-V generated by the equivalent circuit. The simulation was done with the same parameters for forward and backward scan. It was used to check whether the equivalent circuit can produce hysteresis phenomenon or not. The result of the simulation depicted in Figure 4.6. It shows that simulation produced different J-V curve for forward and backward scan. It gave essential information for further *J(t)* curve fitting simulation that simulation

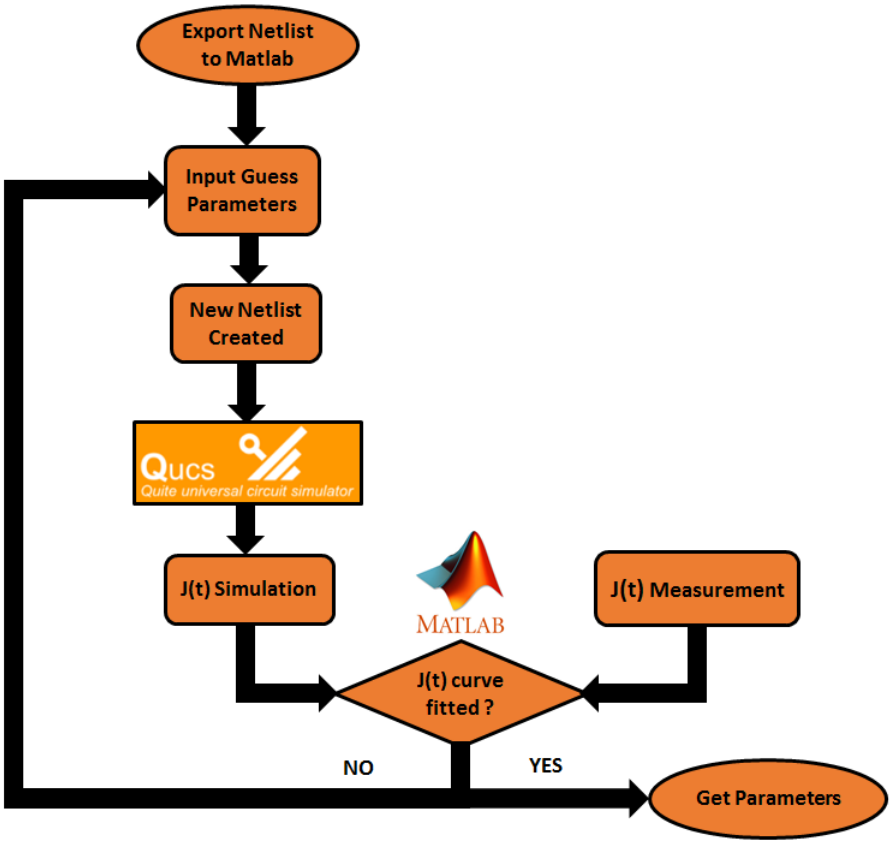


Figure 4.4: A schematic diagram of simulation process.

of equivalent circuit can produce different J-V curves.

As discussed in Chapter 3, the hysteresis phenomenon in a PSC device implies that there is a delay in the device's response to abrupt voltage changes. Consequently, a transient current density response exhibited in the *J(t)* curve. The *J(t)* curves of forward and backward scan measurement which is depicted in Figure 3.6 will be compared to *J(t)* curves from simulation. Figure 4.7 shows result of *J(t)* curve fitting of forward and backward scan.

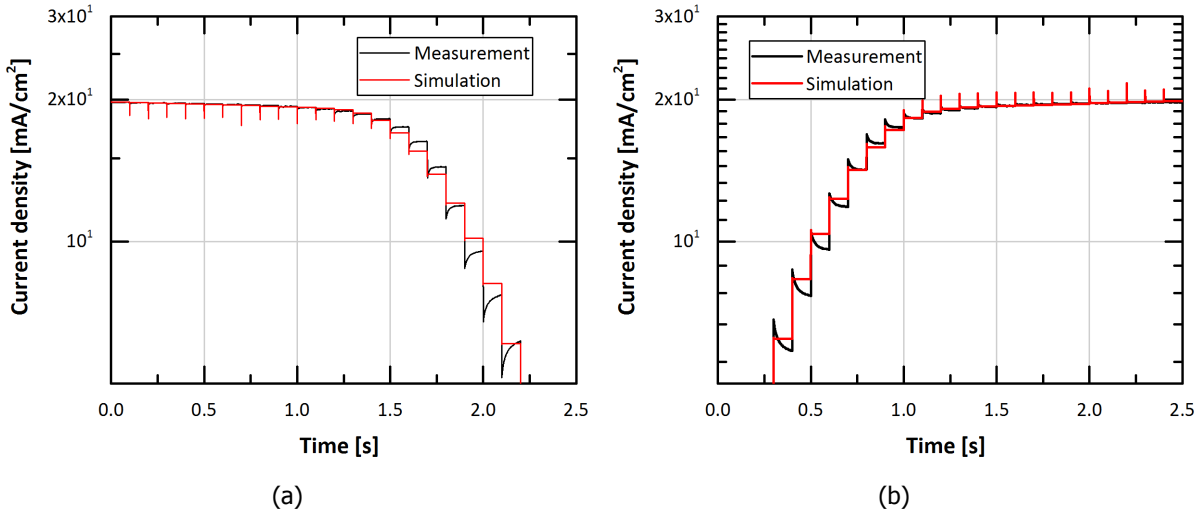


Figure 4.7: The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit with one capacitor.

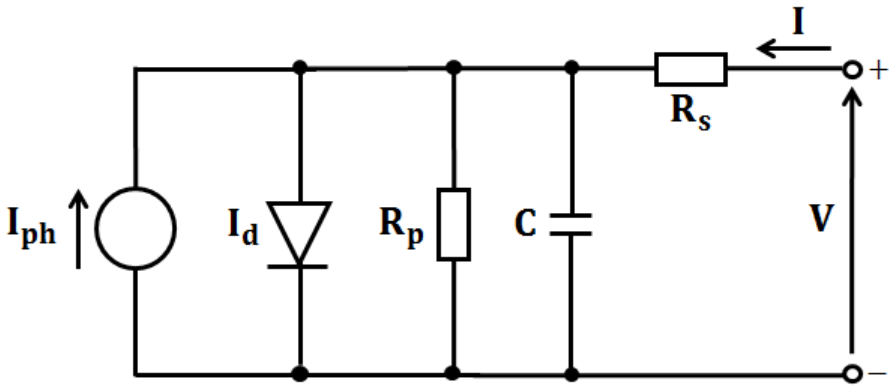


Figure 4.5: A schematic overview of equivalent circuit with one capacitor.

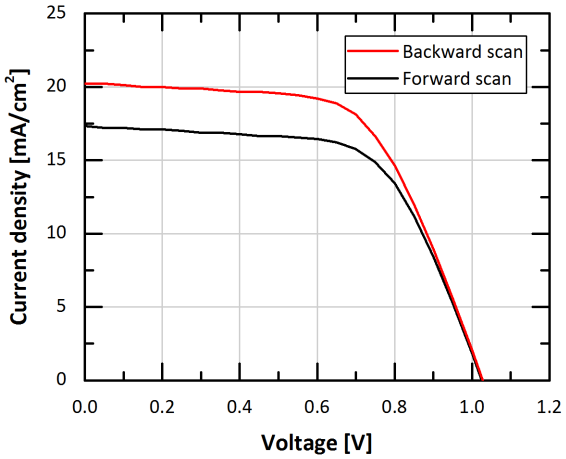


Figure 4.6: J-V curve obtained from simulation.

Table 4.1: Parameters values of equivalent circuit with one capacitors

No.	Parameter	Unit	Forward scan	Backward scan
1.	photo-generated current (I_{ph})	A	0.0018	0.0018
2.	Saturation current (I_s)	A	$1x10^{-9}$	$1x10^{-9}$
3.	Ideality factor (n)	-	1	1
4.	Shunt resistance (R_p)	Ω	10437	10605
5.	Series resistance (R_s)	Ω	233	227
6.	Capacitance (C)	F	$1x10^{-9}$	$1x10^{-9}$
7.	Error	mA/cm^2	0.4609	0.2320

As shown in Figure 4.7, the measured $J(t)$ (black line) shows an exponential trend with a time constant. However, the simulated $J(t)$ shows this behaviour only in the first part of the graph, i.e. for t<1.5 s for forward scan. In other words, transient response exists when voltage is applied from -0.1 to 0.6 V. The same happens in case of backward scan. When the applied voltage step is larger than 0.6 V, the transient response disappears. This capacitor is used to reflect charge accumulation that occurred in bulk of perovskite. However, in the measurement, transient response increases after 0.6 V. It means that charge accumulation increases. Moreover, based on Figure 3.8, transient current density response which is represented by time constant achieves a peak when voltage of 0.9 V is applied to the cell. The time constant is related to capacitance and resistance in the equivalent circuit. Thus, when time constant increases due to the voltage step, it means that the capacitance or resistance changes. Table 4.1 provides the simulation result of forward and backward scan consisting of six parameters and an

error. The error indicates the average difference between *J(t)* from measurement and simulation. Furthermore, as can be seen in the table, parameter values of forward and backward scan are comparable.

4.4. Scenario 2: Equivalent Circuit with Two Capacitors

Based on the discussion in Chapter 2, an equivalent circuit with two capacitors is considered to represent charge accumulation that takes place in the interface of HTL/perovskite and perovskite/ETL. Each capacitor is placed in parallel with a shunt resistor which is related to current leakage in the dielectric of a capacitor device. In this case, nine parameters were used to create the equivalent circuit. These parameters are shown in Figure 4.8.

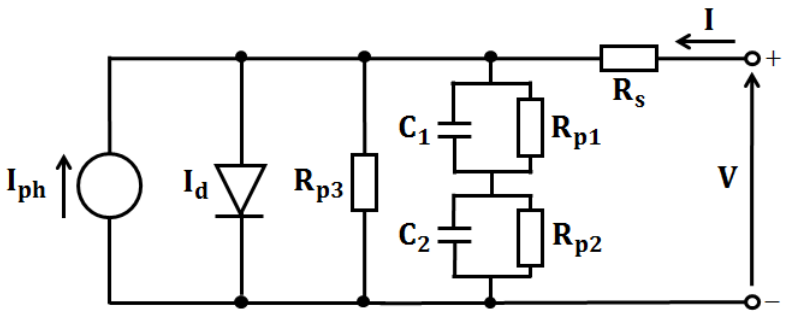


Figure 4.8: A schematic overview of equivalent circuit with two capacitors.

4.4.1. *J(t)* curve Fitting of Forward scan with Voltage Increment of 50 mV

The *J(t)* curve fitting method is also used in this case. Figure 4.7a and 4.7b depict the result of *J(t)* curve fitting for forward and backward scan. In this case, transient current density response of simulation is exhibited when voltage is applied from -0.1 to 0.6 V for both scan directions. This behavior is similar to the behavior of previous topology in subchapter 4.3. However, in this case, the transient response is smaller than transient response in previous topology. At high applied voltage region in which the value is larger than 0.6 V, the transient response does not occur. The parameter values resulted from the *J(t)* curve fitting of forward and backward scan is tabulated in Table 4.2. As can be seen from the table, forward and backward scan have the same order of magnitude for almost all the parameters. However, its saturation current is three orders of magnitude lower than saturation current of forward scan. Furthermore, it is essential to analyze the meaning of saturation current and ideality factor value in a cell because it influences other parameters. A specific discussion of saturation current and ideality factor will be provided in subchapter 4.6. The *J(t)* produced by simulation did not exhibit similar transient response behavior formed in the *J(t)* of measurement. The difference in the capacitance value of first and second capacitor indicates that more charge accumulated in one of the interfaces of charge transport layer and perovskite. Furthermore, there might be other topologies that have better agreement with the measurement to represent hysteresis phenomenon in the PSC device.

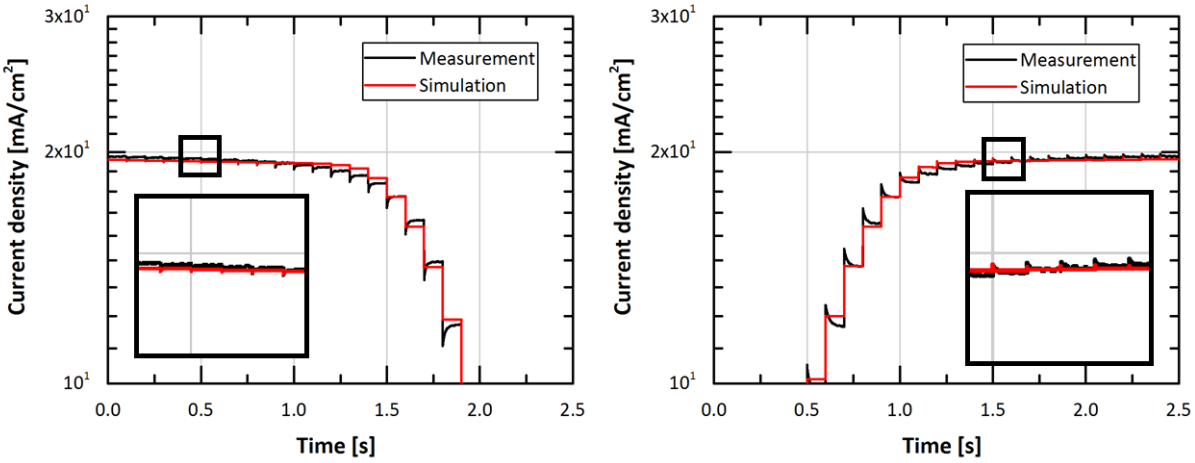


Figure 4.9: The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit with two capacitors.

Table 4.2: Parameters values of equivalent circuit with two capacitors

No.	Parameter	Unit	Forward scan	Backward scan
1.	photo-generated current (I_{ph})	A	0.00074	0.00102
2.	Saturation current (I_s)	A	$2.04\text{x}10^{-14}$	$1.73\text{x}10^{-17}$
3.	Ideality factor (n)	-	1.45	1.47
4.	Shunt resistance 1 (R_{p1})	Ω	7783	12842
5.	Shunt resistance 2 (R_{p2})	Ω	25906	42510
6.	Shunt resistance 3 (R_{p3})	Ω	222787	333884
7.	Series resistance (R_s)	Ω	202	212
8.	Capacitance 1 (C_1)	F	$2.47\text{x}10^{-5}$	$2.34\text{x}10^{-5}$
9.	Capacitance 2 (C_1)	F	$1.46\text{x}10^{-10}$	$1.17\text{x}10^{-10}$
10.	Error	mA/cm²	0.2014	0.2014

4.5. Additional equivalent circuit design of PSC device

Since the two predicted equivalent circuit designs for PSC device do not produce perfectly fit *J(t)* curve, two additional equivalent circuit topologies will be discussed in this study. First, an equivalent circuit of PSC based on a literature that is discussed in subchapter 1.4. Second, a combination of equivalent circuit which is used in subchapter 4.3 and the equivalent circuit from literature. The purpose of these additional topologies is to find a good fit of *J(t)* behavior of measurement and simulation. Thus, a compatible equivalent circuit of PSC sample can be obtained. Consideration of these additional topology will be discussed in section 4.5.2 and 4.5.1.

4.5.1. Scenario 3: Equivalent Circuit based on a Reference Paper

The topology was introduced previously in subchapter 1.6. In this topology, capacitor, which is in parallel with a shunt resistor, is placed in series with the photo-generated current source. It is employed to reflect the charge accumulation in both interfaces of HTL/perovskite and perovskite/ETL [46]. Figure 4.10 presents the schematic overview of the equivalent circuit.

- *J(t)* curve Fitting of Forward scan with Voltage Increment of 50 mV

  In this case, there are seven parameters required as guess values to obtain the best fit to the *J(t)* of measurement. The results are shown in Figure 4.11. As can be seen from the figure, either forward or backward scan exhibits transient current density response, which is more pronounced

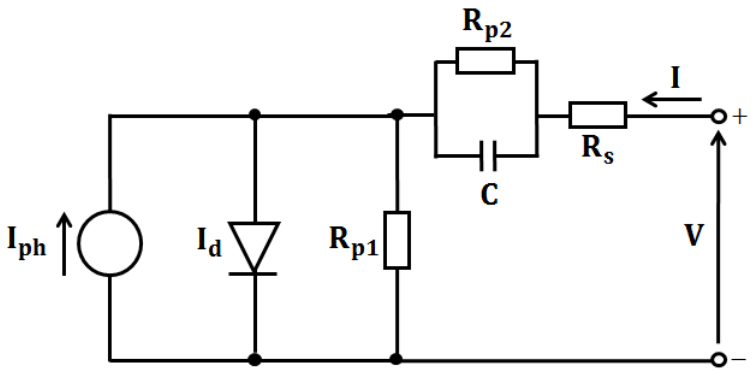


Figure 4.10: A schematic overview of equivalent circuit from a literature.

with increasing applied voltage. This behavior is close to the *J(t)* curve of the measurement. In forward scan, when high voltage is applied, the *J(t)* curve from simulation introduces an increase of undershoot which is followed by an exponential rise. However, the exponential rise curve among the steps is similar which means it does not increase, in contrast to the measurement result.

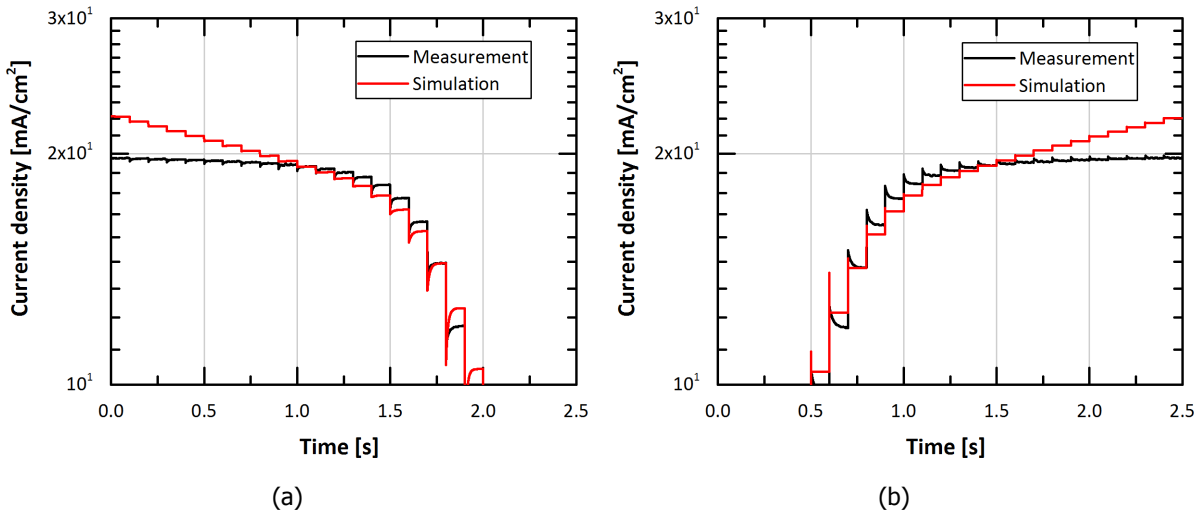


Figure 4.11: The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit from literature.

The result of fitted parameters from the simulation is presented in Table 4.3. Some parameters of both forward and backward scan have the same order of magnitude but certain parameters have not. The ideality factor n of both scan directions are close to 2. When n is equal to 2, there is an indication that charge recombination mechanism dominates. Recombination also influences another parameter, such as shunt resistance. As can be seen that the shunt resistance R_{p1}, which is in parallel with the diode, is small. It implies a high leakage current. Furthermore, capacitance value of forward scan is three orders of magnitude larger than backward scan. Higher capacitance implies more accumulated charge in the interface. The more accumulated charge resulted in lower efficiency and fill factor (FF). Thus, higher capacitance of forward scan induces lower efficiency. It is in agreement with the result of measurement in which forward scan has lower efficiency than backward scan. Nevertheless, since the capacitance value of the capacitor in the simulation is fixed in a specific value, the capacitance value difference exhibits an anomaly. It is because the values strongly depended on the seven guess parameter values. In this scenario, strong under- and overshoots occurred in large voltage regime of the graphs.

Table 4.3: Parameters values of equivalent circuit of scenario 3

No.	Parameter	Unit	Forward scan	Backward scan
1.	photo-generated current (I_{ph})	A	0.0015	0.0025
2.	Saturation current (I_s)	A	$8.22x10^{-16}$	$2.19x10^{-15}$
3.	Ideality factor (n)	-	1.94	1.96
4.	Shunt resistance 1 (R_{p1})	Ω	1632	1717
5.	Shunt resistance 2 (R_{p2})	Ω	139	174
6.	Series resistance (R_s)	Ω	33	13
7.	Capacitance (C)	F	$1.66x10^{-4}$	$1.63x10^{-7}$
8.	Error	mA/cm^2	0.9572	0.7410

4.5.2. Scenario 4: Simulation of Equivalent Circuit Combination of Scenario 1 and 3

This additional equivalent circuit was designed by combining the equivalent circuit from subchapter 4.3 and 4.5.1. It was considered based on the result of simulation from scenario 1 that has transient responses at low voltage region while in scenario 3, the *J(t)* fitted at high voltage region. From the topology standpoints, the purpose of placing these two capacitors are similar to the consideration explained in subchapter 4.3 and 4.5.1. One capacitor which was placed in parallel with photo-generated current source aimed at representing charge accumulation in the bulk of perovskite, while the other capacitor was placed in series with the photo-generated current source to reflect charge accumulation in both interfaces of HTL/perovskite and perovskite/ETL. A schematic illustration of the equivalent circuit of this scenario is shown in Figure 4.12.

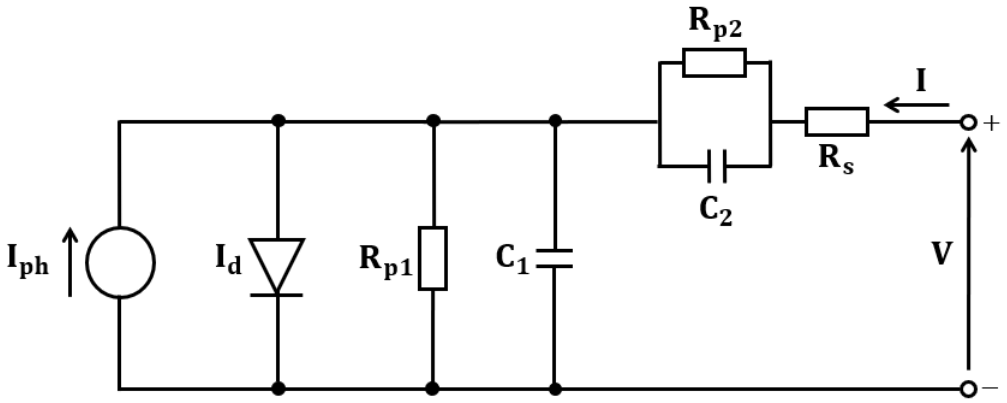


Figure 4.12: A schematic illustration of equivalent circuit of scenario 4.

- *J(t)* curve Fitting of Forward scan with Voltage Increment of 50 mV

  In this scenario, eight parameters were used in the equivalent circuit. It implies that the simulation will be more complicated since there are more parameters that should be optimized to fit *J(t)* curve from measurement. The result of *J(t)* curve fitting of forward and backward scan are shown in Figure 4.13a and 4.13b, respectively. Based on those figures, even though the *J(t)* curves were not perfectly fitted, result from simulation showed transient responses not only at the low voltage region but also at high voltage region. Table 4.4 presents the parameter values resulted from the *J(t)* curve fitting.

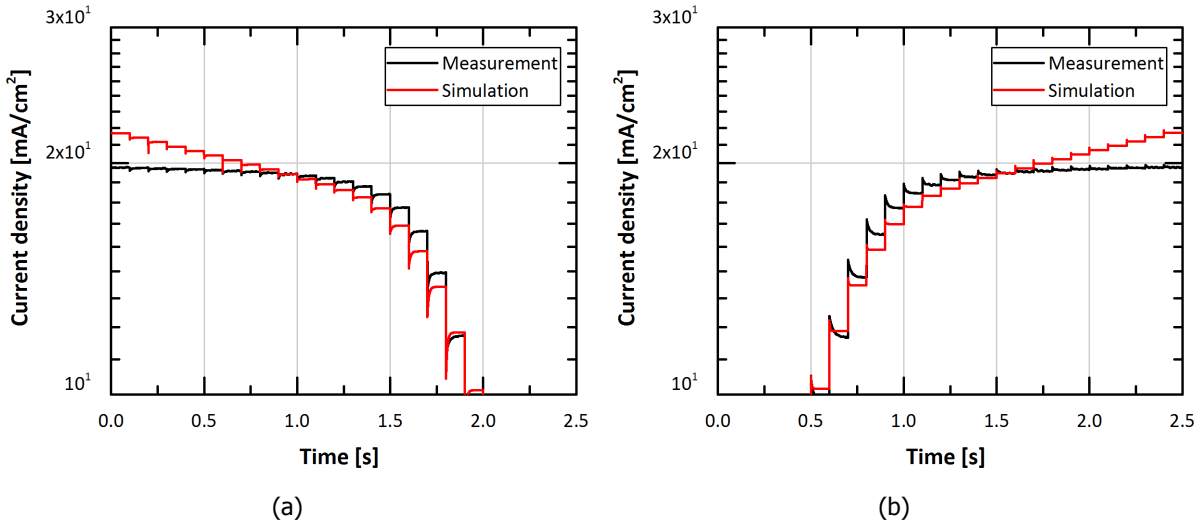


Figure 4.13: The *J(t)* curve fitting of (a) forward and (b) backward scan of equivalent circuit of scenario 4.

Table 4.4: Parameters values of equivalent circuit of scenario 4

No.	Parameter	Unit	Forward scan	Backward scan
1.	photo-generated current (I_{ph})	A	0.0013	0.0046
2.	Saturation current (I_s)	A	$1x10^{-9}$	$1x10^{-9}$
3.	Ideality factor (n)	-	1.22	1.03
4.	Shunt resistance 1 (R_{p1})	Ω	1767	1792
5.	Shunt resistance 2 (R_{p2})	Ω	137	43
6.	Series resistance (R_s)	Ω	88	180
7.	Capacitance 1 (C_1)	F	$2.89x10^{-4}$	$1x10^{-4}$
8.	Capacitance 2 (C_2)	F	$4.23x10^{-8}$	$2.34x10^{-9}$
9.	Error	mA/cm^2	0.9216	0.7207

4.6. Analysis of Saturation Current and Ideality Factor

It is essential to observe the parameter of saturation current I_s and ideality factor n from the simulation. These two parameters are commonly used to indicate the quality of the cell which is also related to recombination. These parameters are crucial parameters that affect the open circuit voltage V_{oc} and thus, FF of the cell. The correlation of these parameters with V_{oc} is shown by equation below [61]:

$$V_{oc} = \frac{nk_BT}{q} ln\left(\frac{J_{sc}}{J_0}\right) \tag{4.1}$$

where k_B is the Boltzmann's constant ($m^2kg/s^2/K$), T is the temperature (K), q is the elementary charge (C), J_{sc} and J_0 represent short-circuit current density and saturation current density (A/m^2), respectively. Based on equation 4.1, when saturation current density increases, the V_{oc} decreases and thus, FF increases. In the simulation, the saturation current of scenario 1 and 4 are approximately 10^{-9} A, whereas scenario 2 and 3 are is in the range of 10^{-14}-10^{-17} A. Theoretically, total current consists of diffusion and recombination current. At low-voltage region when recombination current dominates, the ideality factor is equal to 2. Moreover, at a high-voltage region when diffusion current dominates, the ideality factor is equal to 1 [50]. In other words, when n=1, less recombination occurs in the device. All the *J(t)* curve fitting simulations resulted in ideality factor in the range of 1 to 2. It indicates that both diffusion and recombination current are comparable. Furthermore, based on equation 4.1, ideality factor is proportional with V_{oc}. It implies that higher n leads to higher V_{oc} and consequently, lower FF.

4.7. Discussion

Two topologies were derived from simulation of band diagram as discussed in Chapter 2. First, an equivalent circuit with one capacitor aimed at representing charge accumulation occurs in the grain boundaries in the bulk of perovskite. The result of *J(t)* curve fitting showed that this configuration did not give best fit to the *J(t)* of measurement. It was because the transient current density response from simulation only existed at low voltage region, whereas in the measurement, the *J(t)* curve exhibited increase of transient current density response with increasing applied voltage. Second configuration referred to an equivalent circuit with two capacitors. In this case, two capacitors were used to reflect charge accumulation in the interface of HTL/perovskite and perovskite/ETL. The result showed similar transient current density behavior to the equivalent circuit with one capacitor which was only exhibited at low voltage region. The transient current density is smaller than the first topology. However, its behavior at low voltage region is close to the transient response obtained from measurement. At the high voltage region, the transient current density response disappeared. The *J(t)* curve fitting simulation result showed that this scenario has the smallest error compared to other scenarios.

Two additional equivalent circuit topologies were proposed to obtain better fitted *J(t)* curve. First, a configuration was proposed based on an article introduced in subchapter 1.4. The configuration was depicted in Figure 4.10. In this topology, a capacitor, which was in parallel with a shunt resistor, was placed in series with photo-generated current source. The result showed an increase of transient current density response at high voltage region. This behavior was in contrast to the two prior topologies. Second, an additional equivalent circuit configuration was arranged by combining scenario 1 and 3. It was considered because scenario 1 exhibited transient current density response at low voltage region while the configuration from literature resulted in transient response at high voltage region. The physical meaning of this configuration was to represent charge accumulation in bulk of perovskite and interfaces of charge transport and perovskite. Even though the transient current density response did not increase with increasing voltage. However, the result showed that the transient responses appeared at the low and high voltage region.

In the measurement, the transient response increases with increasing applied voltage. Since the transient response referred to capacitance behavior, it indicated that capacitance in the PSC is a voltage-dependent whereas in the simulation, capacitance was fixed in specific value that was not a voltage dependent. From the quantitative standpoint, scenario 2 gave the best fit to the *J(t)* of measurement. It had the smallest error compared to other scenarios. Moreover, its parameters at forward and backward scan were in the same order of magnitude, except for the saturation current. However, from qualitative standpoint, scenario 4 generated transient current density responses that appeared at all the voltage steps. However, the best fit is far from perfect. This was as expected due to limitations of the simulation software it had to be assumed that the capacitance is constant or independent of voltage.

4.8. Conclusion

This chapter discussed simulation of several equivalent circuit model of PSC. Simulation was done using QUCS and Matlab. Since hysteresis phenomenon in our PSC device derived a transient current response in the *J(t)* curve, a simulation of *J(t)* curve fitting was used in this project. The curve fitting was aimed to find the best fit of *J(t)* curve from measurement and equivalent circuit model. There are four different equivalent circuit configurations or scenarios that discussed in this chapter. Quantitatively, scenario 2 gave the best agreement due to the smallest error. However, the transient current density responses only appeared at the low voltage region. Furthermore, qualitatively, scenario 4 showed transient current density response behavior at all the voltage steps which was similar to the measurement. Nevertheless, the transient current density response did not increase with increasing voltage as shown in the measurement results. These quantitative and qualitative considerations can be used to answer the fourth research question about the best equivalent circuit to reproduce measurement result. Finally, to answer the main research question, simulation in this chapter showed that it is possible to model the hysteresis effect with an equivalent circuit even though the *J(t)* of measurement and simulation were not perfectly fitted. It is worth noting that further simulation with a voltage-dependent capacitor is recommended to obtain better fitted *J(t)* curve.

5

Conclusions and Recommendations

This chapter provides essential conclusions obtained in this master thesis project and recommendations for further research. Our PSC sample was fabricated by Solliance Solar Research. It has a planar structure consisting of ITO/NiO nanoparticles/$Cs_{0.05}(MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.9}Br_{0.1})_3$/PCBM/ ZnO nanoparticles/Au. NiO nanoparticles were employed as hole transport layer (HTL), whereas PCBM and ZnO nanoparticles were used as bilayer electron transport layer (ETL). The main objective of the project is to investigate hysteresis phenomenon in PSC sample using electrical modelling approach. It was carried out by the following main scientific research question:

"Is it possible to model hysteresis of the PSC with an equivalent circuit?"

Four scientific research subquestions were derived based on the main research question. These subquestions will be discussed and answered in the following subchapter. As explained in subchapter 1.3.3, hysteresis phenomenon in an organic-inorganic PSC device can be caused by several reasons. Nevertheless, this project will only focus on hysteresis effect induced by charge accumulation occurred in the cell.

5.1. Conclusions

5.1.1. Simulation of Band Diagram of PSC device

This section is used to answer first and second research subquestion that were introduced in subchapter 1.6. The first question was *"Is it possible to understand charge accumulation in a PSC from the band diagram?"* and the second question was *"Can equivalent circuit of PSC be derived from band diagram?"*. In order to answer these questions, a simulation of band diagram of PSC sample in dark condition was done using Sentaurus TCAD. Input of the simulation was based on fitting from the simulation and on experiment from literature. Detailed explanation and discussion was provided in Chapter 2.

The result of simulation was depicted in Figure 2.3. It was shown that perovskite has inclined band which will benefit charge carrier collection to the electrodes. On the other hand, charge transport was also influenced by internal electric field generated by built-in voltage. Electric field drives electrons and holes to ETL and HTL, respectively. Thus, it leads to a more efficient charge collection. The band alignment strongly depends on the materials forming the PSC device. It means that different device architecture results in different band alignment. In this project, PCBM as ETL has slightly higher conduction band level than the absorber layer leading to the formation of a barrier, which prevents the electrons that flowed from photoactive layer to metal back contact to pass the barrier. Hence, when electric field is not sufficient to push the electrons to pass through the barrier, electrons will accumulate in this area which is the interface between perovskite and ETL. On the other hand, valence band of perovskite and HTL induces a cliff which can lead to more efficient holes collection to the ITO electrode. Nevertheless, it also implies that the charges could accumulate in the interface of HTL/perovskite. Moreover, the conduction band of ITO was close to the valence band of HTL. It indicates that holes will recombine with the electron from an external circuit when the cell placed under

illumination. These explanation indicated that it is possible to understand charge accumulation based on the simulated band diagram, referring to the first research question.

Simulation of band diagram in this project exhibited two possible location for charge accumulation issue inducing hysteresis phenomenon. There were interfaces of HTL/perovskite and perovskite/ETL. Additionally, based on some literature studies, there was an indication that charge accumulation takes place due to ion migration in the grain boundaries of perovskite material that will also be considered in this project. Thus, two equivalent circuit topologies were proposed. First topology referred to charge accumulation in the bulk of perovskite layer. It was represented by a capacitor placed in parallel with the photo-generated current source. The second configuration was arranged by adding two capacitors in parallel to the general equivalent circuit of solar cell. However, in this case, each capacitor was put in parallel with a shunt resistor. These equivalent circuit topologies were suggested to address the second research question.

5.1.2. Hysteresis phenomenon in PSC sample

This section referred to the third research question stated as *"Is it possible to study hysteresis phenomenon using time-resolved I-V measurement?"*. Chapter 3 was aimed to answer this question. As introduced in Chapter 1, hysteresis phenomenon occurred in specific PSC devices. It depends on the materials that composed the device architecture. Thus, a time-resolved I-V measurement was done in this project to measure hysteresis effect of the PSC sample.

The measurement was done with different scan directions containing forward and backward scan. Backward scan was applied to the cell first, followed by forward scan. The J-V characteristics obtained from the measurement showed that short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}) of forward and backward scan were close to each other. Nevertheless, the maximum power point of backward scan was higher than forward scan which led to higher power conversion efficiency. Various scan rates were applied to understand the influence on hysteresis phenomena. It was found that slower scan rates resulted in less severe hysteresis effect.

Additionally, transient current density responses were observed in *J(t)* curve of forward and backward scan as a function of applied voltage. The transient behaviour increased with increasing applied voltage. Furthermore, a time constant can be derived from the transient current density response. It indicated that time constant also increased with increasing applied voltage. The time constant was related to capacitance and resistance. Thus, based on the measurement, it can be concluded that capacitance is a voltage-dependent parameter.

5.1.3. Electrical modelling of equivalent circuit

Chapter 4 was purposed to answer the main research question that was stated in the introduction of this chapter. Moreover, it provided a discussion aimed to answer the fourth research question which was: *"Which of the selected circuits best reproduces the measurement result?"*. Four equivalent circuit topologies were considered to represent the equivalent circuit of PSC device that exhibited hysteresis phenomenon. In these topologies, a capacitor was used to reflect the charge accumulation.

Furthermore, a *J(t)* curve fitting simulation was done to achieve the best fit of *J(t)* from measurement and simulation. This simulation was essential to understand whether the *J(t)* of simulation can produce similar behaviour to *J(t)* from the measurement. As explained in subchapter 5.1.2, transient current density responses, which was exhibited in the measurement, transient current density increased with increasing applied voltage. The fourth research question can be answered based on quantitative and qualitative standpoints. Quantitatively, scenario 2 gave the smallest error compared to other scenarios which was 0.2014 mA/cm^2. Its parameters were at the same order of magnitude, except for saturation current. The transient current density response in this scenario only appeared at low voltage region. It implies that the transient response did not occur at high voltage region. The purpose of this scenario was to represent the charge accumulation at the interface of HTL/perovskite and perovskite/ETL. Moreover, from qualitative standpoint, scenario 4 showed transient current density response at all the voltage steps. This behavior was similar to the *J(t)* of measurement even though

the transient responses did not increase with increasing applied voltage. In this scenario, one capacitor used to reflect charge accumulation occurred at the bulk of perovskite, whereas the other capacitor used to represent charge accumulation at the interface of charge transport layers and perovskite. The error of this scenario was larger than scenario 2. The result of measurement showed that capacitance was a function of voltage, while the capacitance value in the simulation was fixed. It was because the built-in capacitor component in QUCS did not provide setup to set the capacitance as a function of voltage.

5.2. Recommendations

5.2.1. Measurement

It is worth noting that the measurement should be done in a stabilized efficiency. It can be achieved using maximum power tracking method that is equipped with a setup to set time duration of the tracking process. Additionally, in this project, measurement was done with time-resolved I-V measurement method. There are two ways to do the measurement of forward and backward scan: with and without waiting time in between the forward and backward scans. In this project, the Keithley software provides an option to measure backward scan, that directly followed by forward scan, and vice versa. A new option of putting waiting time in between forward and backward scan measurement could be useful to understand J-V characteristic which is influenced by charge distribution and redistribution. Moreover, since the correlation of capacitance and voltage in this project was only derived from transient current density response, further C-V measurement could be done to obtain appropriate C-V correlation. It would also be less time-consuming if the software can give output not only in $J(t)$ as a function of voltage but also J-V curve when forward and backward scans are applied to the cell. In this project, the J-V curve was extracted from $J(t)$ curve with interpolation method using Matlab.

5.2.2. Simulation

In this project, simulation of band diagram was done at dark condition due to limited data. The simulation could also be done for under illumination and applied bias condition. It would be fruitful to have a better understanding of working principle of a PSC device. However, the simulation requires optical and electrical properties data. Measurement could be an option to obtain these properties. Furthermore, in this project, a built-in capacitor component was used because it was provided in QUCS. Nevertheless, the build-in capacitor does not provide a setup to set the capacitance as a function of voltage. Hence, a simulation with a voltage-dependent capacitor should be implemented for further research. It is a crucial aspect to attain a better fit to the measurement result.

Bibliography

[1] I. E. Agency, *Renewables 2017 analysis and forecasts to 2022,* (2017).

[2] N. R. E. Laboratory, Https://www.nrel.gov/pv/ accessed: 08.07.2018.

[3] E. L. Unger, E. T. Hoke, C. D. Bailie, W. H. Nguyen, A. R. Bowring, T. Heumuller, M. G. Christoforo, and M. D. McGehee, *Hysteresis and transient behavior in current-voltage measurements of hybrid-perovskite absorber solar cells,* Energy Environ. Sci. **7**, 3690 (2014).

[4] P. Liao, G. Li, X. Zhao, and M. Wang, *A new method for fitting current–voltage curves of planar heterojunction perovskite solar cells,* Nano-Micro Letters **10** (2017).

[5] K. Seki, A. Furube, and Y. Yoshida, *Theoretical limit of power conversion efficiency for organic and hybrid halide perovskite photovoltaics,* Japanese Journal of Applied Physics **54**, 08KF04 (2015).

[6] L. Cojocaru, S. Uchida, P. V. V. Jayaweera, S. Kaneko, Y. Toyoshima, J. Nakazaki, T. Kubo, and H. Segawa, *Simulation of current–voltage curves for inverted planar structure perovskite solar cells using equivalent circuit model with inductance,* Applied Physics Express **10** (2017).

[7] L. Cojocaru, S. Uchida, P. V. V. Jayaweera, and H. Segawa, *Origin of the hysteresis in i–v curves for planar structure perovskite solar cells rationalized with a surface boundary-induced capacitance model,* Chemistry Letters **44**, 1750 (2015).

[8] I. Mora-Sero, *How do perovskite solar cells work,* Joule **2**, 583 (2018).

[9] Y.-C. Wu and Y.-R. Jhan, *3D TCAD Simulation for CMOS Nanoelectronic Devices* (Springer Nature Singapore Pte Ltd., 2018).

[10] T. Minemoto and M. Murata, *Theoritical analysis on effect of band offsets in perovskite solar cells,* Solar Energy Materials and Solar Cells **133**, 8 (2015).

[11] T. S. Sherkar, C. Momblona, L. Gil□Escrig, H. J. Bolink, and L. J. A. Koster, *Recombination in perovskite solar cells: Significance of grain boundaries, interface traps, and defect ions,* ACS Energy Lett **2**, 1214 (2017).

[12] D. A. Bell, *Fundamentals of Electric Circuit* (Prentice Hall International, Inc., Englewood Cliffs, New Jersey, 1988).

[13] J. Z. P.-Y. L. M. A. S. J. Ting Wu, Liam Collins and B. Hu, *Photoinduced bulk polarization and its effects on photovoltaic actions in perovskite solar cells,* ACS Nano **11**, 11542 (2017).

[14] T. Ibn-Mohammed, S. Koh, I. Reaney, A. Acquaye, G. Schileo, K. Mustapha, and R. Greenough, *Perovskite solar cells: An integrated hybrid lifecycle assessment and review in comparison with other photovoltaic technologies,* Renewable and Sustainable Energy Reviews **80**, 1321 (2017).

[15] Y. Xu, T. Gong, and J. N. Munday, *The generalized shockley-queisser limit for nanostructured solar cells,* Scientific Reports **5** (2015).

[16] A. Smets, O. Isabella, R. van Swaaij, and M. Zeman, *Solar Energy: The Physics and Engineering of Photovoltaic Conversion Technologies and Systems*, International series of monographs on physics (UIT Cambridge Ltd, England, 2016).

[17] S. Phillips and W. Warmuth, *Photovoltaic report,* Fraunhofer Institute for Solar Energy Systems (2018).

[18] M. A. Green, Y. Hishikawa, E. D. Dunlop, D. H. Levi, J. Hohl□Ebinger, and A. W. Ho□Baillie, *Solar cell efficiency tables (version 51),* Progress in Photovoltaics: Research and Applications **26**, 3 (2018).

[19] K. Chu, Y.-H. Zhou, J.-L. Song, and C. Zhang, *An abx 3 organic–inorganic perovskite-type material with the formula (c 5 n 2 h 9)cdcl 3 : Application for detection of volatile organic solvent molecules,* Polyhedron **131**, 22 (2017).

[20] A. Kojima, K. Teshima, Y. Shirai, and T. Miyasaka, *Organometal halide perovskites as visible-light sensitizers for photovoltaic cells,* J. Am. Chem. Soc **131**, 6050 (2009).

[21] F. Ye, W. Yang, D. Luo, and Q. Gong, *Applications of cesium in the perovskite solar cells,* Journal of Semiconductors **38** (2017).

[22] C.-B. Juan-Pablo, A. Abate, M. Saliba, W. Tress, T. Jesper Jacobsson, M. Gratzel, and A. Hagfeldt, *The rapid evolution of highly efficient perovskite solar cells,* Energy Environ. Sci. **10**, 710 (2017).

[23] X. Ziang, L. Shifeng, Q. Laixiang, P. Shuping, W. Wei, Y. Yu, Y. Li, C. Zhijian, W. Shufeng, D. Honglin, Y. Minghui, and G. G. Qin, *Refractive index and extinction coefficient of $ch_3nh_3pbi_3$ studied by spectroscopic ellipsometry,* Optical Materials Express **5**, 29 (2015).

[24] J. Ma and L.-W. Wang, *The nature of electron mobility in hybrid perovskite $ch_3nh_3pbi_3$,* Nano Lett **17**, 3646 (2017).

[25] L. Meng, J. You, T.-F. Guo, , and Y. Yang, *Recent advances in the inverted planar structure of perovskite solar cells,* Acc Chem Res **49**, 155 (2016).

[26] T. S. Sherkar, C. Momblona, L. Gil□Escrig, H. J. Bolink, and L. J. A. Koster, *Improving perovskite solar cells: Insights from a validated device model,* Advanced Energy Materials **7** (2017).

[27] M. Najafi, F. D. Giacomo, D. Zhang, S. Shanmugam, A. Senes, W. Verhees, A. Hadipour, Y. Galagan, T. Aernouts, S. Veenstra, and R. Andriessen, *Highly efficient and stable flexible perovskite solar cells with metal oxides nanoparticle charge extraction layers,* Small **14**, 1702775 (2018).

[28] D. G. Francesco, A. Fakharuddin, R. Jose, and T. M. Brown, *Progress, challenges and perspectives in flexible perovskite solar cells,* Energy Environ. Sci. **9**, 3007 (2016).

[29] M. Saliba, T. Matsui, J.-Y. Seo, K. Domanski, J.-P. Correa-Baena, M. K. Nazeeruddin, S. M. Zakeeruddin, W. Tress, A. Abate, A. Hagfeldt, and M. Gratzel, *Cesium-containing triple cation perovskite solar cells: improved stability, reproducibility and high efficiency,* Energy Environ. Sci. **9**, 1989 (2016).

[30] J. H. Noh, S. H. Im, J. H. Heo, T. N. Mandal, and S. I. Seok, *Chemical management for colorful, efficient, and stable inorganic-organic hybrid nanostructured solar cells.* Nano Lett **13**, 1764 (2013).

[31] L. K. Ono, E. J. Juarez-Perez, and Y. Qi, *Progress on perovskite materials and solar cells with mixed cations and halide anions,* ACS Appl Mater Interfaces **9**, 30197 (2017).

[32] D. R. K. Misra, D. L. Ciammaruchi, S. Aharo, D. D. Mogilyansky, D. L. Etgar, D. I. Visoly□Fisher, and P. E. A. Katz, *Effect of halide composition on the photochemical stability of perovskite photovoltaic materials,* ChemSusChem **9**, 2572 (2016).

[33] A. Babayigit, D. D. Thanh, A. Ethirajan, J. Manca, M. Muller, H.-G. Boyen, and B. Conings, *Assessing the toxicity of pb- and sn-based perovskite solar cells in model organism danio rerio,* Sci Rep **6**, 18721 (2016).

[34] A. Babayigit, M. Muller, A. Ethirajan, and B. Conings, *Toxicity of organometal halide perovskite solar cells,* Nature Materials **15**, 247 (2016).

[35] S. Yuchuan, Y. Fang, T. Li, Q. Wang, Q. Dong, Y. Deng, Y. Yuan, H. Wei, M. Wang, A. Gruverman, J. Shield, and J. Huang, *Grain boundary dominated ion migration in polycrystalline organic-inorganic halide perovskite films,* Energy Environ. Sci. **9**, 1752 (2016).

[36] N. J. Jeon, Y. C. Kim, J. H. Noh, and S. H. Im, *Solvent engineering for high-performance inorganic-organic hybrid perovskite solar cells,* Nature Materials **13**, 897 (2014).

[37] H. J. Snaith, A. Abate, J. M. Ball, G. E. Eperon, T. Leijtens, N. K. Noel, S. D. Stranks, J. T.-W. Wang, K. Wojciechowski, and W. Zhang, *Anomalous hysteresis in perovskite solar cells,* J Phys Chem Lett **5**, 1511 (2014).

[38] M. Taghavi, M. Houshmand, M. H. Zandi, and N. E.Gorji, *Modeling of optical losses in perovskite solar cells,* Superlattices and Microstructures **97**, 424 (2016).

[39] N. E. Gorji and H. Sohrabpoor, *Modeling of light interference in $ch_3nh_3pbi_3cl_x$ and $mapbi_3cl$ perovskite solar cells,* Materials Letters **177**, 143 (2016).

[40] R. Santbergen, R. Mishima, T. Meguro, M. Hino, H. Uzu, J. Blanker, K. Yamamoto, and M. Zeman, *Minimizing optical losses in monolithic perovskite/c-si tandem solar cells with a flat top cell,* Opt Express **24**, A1288 (2016).

[41] G. W. P. Adhyaksa, E. Johlin, and E. C. Garnett, *Nanoscale back contact perovskite solar cell design for improved tandem efficiency,* Nano Lett **17**, 5206 (2017).

[42] P. Bhatt, M. Kumar, C. KantP., M. K. Pandey, and B. Tripathi, *Optoelectronic modelling of perovskite solar cells under humid conditions and their correlation with power losses to quantify material degradation,* Organic Electronics **39**, 258 (2016).

[43] D. Zhang, W. Verhees, M. Dörenkämper, W. Qiu, K. Bakker, A. Gutjahr, S. Veenstra, R. Gehlhaar, U. W.Paetzold, W. Soppe, I. RomijnaL.J.Geerligs, T. Aernouts, and A. Weeber, *Combination of advanced optical modelling with electrical simulation for performance evaluation of practical 4-terminal perovskite/c-si tandem modules,* Energy Procedia **92**, 669 (2016).

[44] A. N. D. amd Sossé Ndiaye, E. H. O. Gueye, A. Dioum, A. A. Diouf, M. B. Abderaman, B. D. Ngom, and A. C. Beye, *Optical and electrical modeling of a hybrid solar cell based on a mesostructured perovskite $ch_3nh_3pbi_3$: Influence of the depth and thickness of the photoactive layer,* American Journal of Nanomaterials **5**, 68 (2016).

[45] Q. Lin, R. Nagiri, A. Armin, and P. Meredith, *Electro-optics of perovskite solar cells,* Nature Photonics **9**, 106 (2014).

[46] K. Seki, *Equivalent circuit representation of hysteresis in solar cells that considers interface charge accumulation: Potential cause of hysteresis in perovskite solar cells,* Applied Physics Letters **109** (2016).

[47] K. Tada, *Comment on "simulation of current–voltage curves for inverted planar structure perovskite solar cells using equivalent circuit model with inductance",* Applied Physics Express **10**, 059101 (2017).

[48] L. Cojocaru, S. Uchida, Y. Sanehira, and H. Segawa, *Temperature effects on the photovoltaic performance of planar structure perovskite solar cells,* Chemistry Letters **44**, 1557–1559 (2015).

[49] Https://www.synopsys.com/silicon/tcad/framework.html accessed: 23.07.2018.

[50] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles, Fourth Edition* (McGraw-Hill Education, New York, 2016).

[51] U. o. G. David Pennicard, *Introduction to sentaurus tcad,* .

[52] J. Melskens, B. H. van de Loo, B. Macco, L. E. Black, S. Smit, and W. M. M. E. Kessels, *Passivating contacts for crystalline silicon solar cells: From concepts and materials to prospects,* IEEE JOURNAL OF PHOTOVOLTAICS **8**, 373 (2018).

[53] Q. Wang, D. C. Chueh, T. Zhao, J. Cheng, P. M. Eslamian, P. W. C. H. Choy, and P. A. K. Jen, *Effects of self□assembled monolayer modification of nickel oxide nanoparticles layer on the performance and application of inverted perovskite solar cells,* ChemSusChem **10**, 3794 (2017).

[54] G. Paternòab, A. J. Warrenc, J. Spencera, G. Evansc, V. G. Sakaid, J. Blumbergera, and F. Cacialli, *Micro-focused x-ray diffraction characterization of high-quality [6,6]-phenyl-c61-butyric acid methyl ester single crystals without solvent impurities,* J. Mater. Chem. C **1**, 5619 (2013).

[55] T. Jiang and W. Fu, *Improved performance and stability of perovskite solar cells with bilayer electron-transport layer,* RSC Adv. **8**, 5897 (2018).

[56] Q. Bao, X. Liu, Y. Xia, F. Gao, L.-D. Kauffmann, O. Margeat, J. Ackermannc, and M. Fahlman, *Effects of ultraviolet soaking on surface electronic structures of solution processed zno nanoparticle films in polymer solar cells,* J. Mater. Chem. A **2**, 17676 (2014).

[57] B. Chen, M. Yang, S. Priya, and K. Zhu, *Origin of j-v hysteresis in perovskite solar cells,* J. Phys. Chem. Lett **7**, 905 (2016).

[58] Yongbo and J. Huang, *Ion migration in organometal trihalide perovskite and its impact on photovoltaic efficiency and stabilty,* Acc. Chem. Res **49**, 286 (2016).

[59] J.-W. Kang, S.-P. Lee, D.-G. Kim, S. Lee, G.-H. Lee, J.-K. Kim, S.-Y. Park, J. H. Kim, H.-K. Kim, and Y.-S. Jeonga, *Reduction of series resistance in organic photovoltaic using low sheet resistance of ito electrode,* Electrochemical and Solid-State Letters **12**, 64 (2009).

[60] Http://qucs.sourceforge.net/tech/node23.html accessed: 02.08.2018.

[61] B. Qi and J. Wang, *Fill factor in organic solar cells,* Phys. Chem. Chem. Phys. **15**, 8972 (2013).

[62] S. AL-Algawi, S. Al-Jawad, and N. Saadoon, *Physical properties of indium tin oxide (ito) nanopartical thin films used as gas sensor,* Eng. Tech.Journal **33**, 141 (2015).

[63] T. Liu, X. Zhang, J. Zhang, W. Wang, L. Feng, L. Wu, W. Li, G. Zeng, and B. Li, *Interface study of ito/zno and ito/sno2 complex transparent conductive layers and their effect on cdte solar cells,* International Journal of Photoenergy , 1 (2013).

[64] S. Weber, T. Rath, J. Mangalam, B. Kunert, A. M. Coclite, M. Bauch, T. Dimopoulos, and G. Trimmel, *Investigation of nio_x- hole transport layers in triple cation perovskite solar cells,* Journal of Materials Science: Materials in Electronic **29**, 1847 (2017).

[65] X. Yin, P. Chen, M. Que, Y. Xing, W. Que, C. Niu, and J. Shao, *Highly efficient flexible perovskite solar cells using solution-derived nio_x hole contacts,* ACS Nano **10**, 3630 (2016).

[66] G. Natu, P. Hasin, Z. Huang, Z. Ji, M. He, and Y. Wu, *Valence band-edge engineering of nickel oxide nanoparticles via cobalt doping for application in p□type dye-sensitized solar cells,* ACS Appl. Mater. Interfaces **4**, 5922 (2012).

[67] J. M. Frost, K. T. Butler, F. Brivio, C. H. Hendon, M. van Schilfgaarde, and A. Walsh, *Atomistic origins of high-performance in hybrid halide perovskite solar cells,* Nano Lett. **14**, 2584 (2014).

[68] F. Brivio, K. T. Butler, and A. Walsh, *Relativistic quasiparticle self-consistent electronic structure of hybrid halide perovskite photovoltaic absorbers,* Physical review B **89**, 155204 (2014).

[69] B. W. Larson, J. B. Whitaker, X.-B. Wang, A. A. Popov, G. Rumbles, N. Kopidakis, S. H. Strauss, and O. V. Boltalinar, *Electron affinity of phenyl$-c_{61}-$butyric acid methyl ester (pcbm),* J. Phys. Chem. Lett. **117**, 14958 (2013).

[70] A. S. Subbiah, A. Halder, S. Ghosh, N. Mahuli, G. Hodes, , and S. K. Sarkar, *Inorganic hole conducting layers for perovskite-based solar cells,* J. Phys. Chem. Lett. **5**, 1748 (2014).

[71] G. Garcia-Belmonte, P. P.Boix, J. Bisquert, M. Sessolo, and HenkJ.Bol, *Simultaneous determination of carrier lifetime and electron density-of-states in p3ht:pcbm organic solar cells under illumination by impedance spectroscopy,* Solar Energy Materials Solar Cells **94**, 366 (2010).

[72] A. Materials, Https://www.azom.com/article.aspx?ArticleID=8417 accessed: 11.06.2018.

A

Device Parameters for Simulation of Band Diagram of PSC

A.1. Input of Sentaurus Structure Editor

Table A.1: Thickness of materials

Materials	Value	Unit	Details
ITO	140	nm	Ref.[38]
NiO nanoparticles	25	nm	Ref.[38]
Perovskite	490	nm	Ref.[38]
PCBM	40	nm	Ref.[38]
ZnO nanoparticles	60	nm	Ref.[38]
Au	170	nm	Ref.[38]

Table A.2: Doping concentration

Materials	Value	Unit	Details
ITO (n-type)	$9.45x10^{18}$	cm^{-3}	Ref.[62]
NiO nanoparticles (p-type)	$1x10^{19}$	cm^{-3}	Fitting
PCBM (n-type)	$1x10^{17}$	cm^{-3}	Fitting
ZnO nanoparticles (n-type)	$1x10^{17}$	cm^{-3}	Fitting

A.2. Input of Sentaurus Structure Device

Table A.3: Parameter of ITO

Parameter	Value	Unit	Details
Electron affinity, χ	4.5	eV	Ref.[63]
Band gap, Eg	3.72	eV	Ref.[63]
Density of States (DoS) of electron, N_c	$4x10^{19}$	cm^{-3}	Ref.[63]
Density of States (DoS) of hole, N_v	$1x10^{18}$	cm^{-3}	Ref.[63]
Permittivity, ε_r	3.3	-	Ref.[63]

Table A.4: Parameter of NiO nanoparticles

Parameter	Value	Unit	Details
Electron affinity, χ	1.85	eV	Ref.[64]
Band gap, Eg	3.7	eV	Ref.[65]
Density of States (DoS) of electron, N_c	$6.8x10^{17}$	cm^{-3}	Ref.[66]
Density of States (DoS) of hole, N_v	$1.2x10^{18}$	cm^{-3}	Ref.[66]
Permittivity, ε_r	11.9	-	Ref.[66]

Table A.5: Parameter of Perovskite

Parameter	Value	Unit	Details
Electron affinity, χ	4.1	eV	Ref.[67]
Band gap, Eg	1.55	eV	Ref.[38]
Density of States (DoS) of electron, N_c	$3.1x10^{18}$	cm^{-3}	Ref.[11]
Density of States (DoS) of hole, N_v	$3.1x10^{18}$	cm^{-3}	Ref.[11]
Permittivity, ε_r	23.3	-	Ref.[68]

Table A.6: Parameter of PCBM

Parameter	Value	Unit	Details
Electron affinity, χ	3.8	eV	Ref.[69]
Band gap, Eg	2.2	eV	Ref.[70]
Density of States (DoS) of electron, N_c	$1x10^{18}$	cm^{-3}	Ref.[71]
Density of States (DoS) of hole, N_v	$1x10^{18}$	cm^{-3}	Fitting
Permittivity, ε_r	3.9	-	Ref.[26]

Table A.7: Parameter of ZnO nanoparticles

Parameter	Value	Unit	Details
Electron affinity, χ	4	eV	Ref.[63]
Band gap, Eg	3.27	eV	Ref.[63]
Density of States (DoS) of electron, N_c	$1x10^{19}$	cm^{-3}	Ref.[63]
Density of States (DoS) of hole, N_v	$2.4x10^{18}$	cm^{-3}	Ref.[63]
Permittivity, ε_r	8.5	cm^{-3}	Ref.[72]

Table A.8: Parameter of Au

Parameter	Value	Unit	Details
Work function, ψ	5.1	eV	Sentaurus library
Permittivity, ε_r	6.9	cm^{-3}	Sentaurus library