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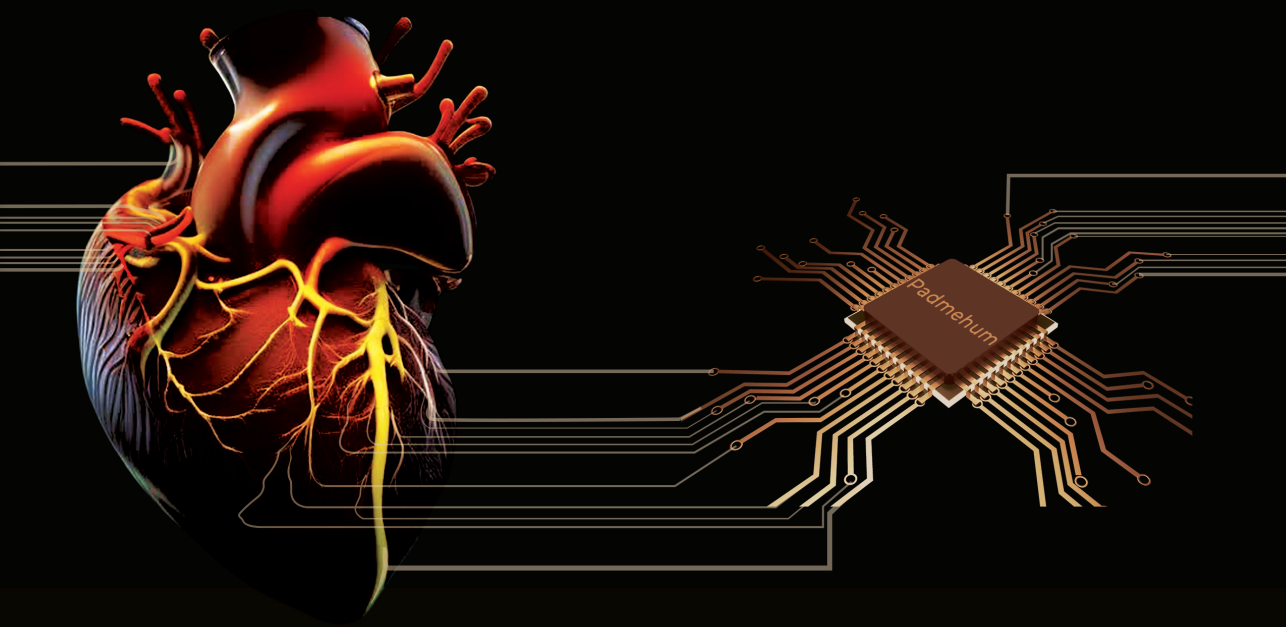

Samprajani Rout

Analog front-end and algorithm co-design for efficient biosignal acquisition

And its application to cardiac signal monitoring

Analog front-end and algorithm co-design for efficient biosignal acquisition

And its application to cardiac signal monitoring

Dissertation

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chair of the Board for Doctorates
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by

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Not just beautiful, though — the stars are like the trees in the forest, alive and breathing. And they're watching me. What I've up till now, what I'm going to do — they know it all.

Haruki Murakami

To my teachers

Contents

Summary

Cardiovascular diseases (CVDs) claimed 17.9 million lives annually (2019), representing 32% of total deaths, with 85% attributed to heart attacks and strokes [1] worldwide. Atrial fibrillation (AF) is the most frequent type of cardiac arrhythmia that has a worldwide prevalence of 46 million individuals worldwide [2]. The absence of P-waves in the electrocardiogram and irregular heartbeat characterize AF. Although the awareness and diagnostic methods of AF have improved over the past years, precision and timely diagnosis are required for effective prevention. Electrophysiological recording serves as the gold standard for diagnosing cardiac abnormalities. There currently exist two major fundamental approaches for monitoring the heart from an electrophysiological point of view. The most common approach is the measurement of the ECG (electrocardiogram), which is recorded on the surface of the human body at specific points. A more recent approach (but less commonly used) is the measurement of the AEG (atrial electrogram), which is recorded on the surface of the human heart with higher spatial resolution than ECG. ECG is a technique used to monitor the heart's electrical activity non-invasively, whereas AEG is used to obtain more profound and detailed insights into the electrical conduction pathways of the heart invasively. AEGs are used to localize the origin of AF for appropriate treatment. Chapter 2 elaborates on the application, the associated technological challenges, and the existing solutions in the literature concerning cardiac signal acquisition.

The first approach (most commonly used) for diagnosing cardiac abnormalities is recording the ECG, with a high signal-to-noise-and-interference ratio and sufficient bandwidth using a single-channel analog front-end. One of the main challenges with acquiring ECG is baseline wandering (BW), which refers to low-frequency variations affecting the baseline of the recorded waveform. BW occurs due to body movement or poor contact between the body surface and electrodes. The impact of BW on the ECG signal quality can be twofold: (a) Saturation of the CMOS analog front-end leading to loss of information, and (b) Distortion of the ECG waveform leading to misdiagnosis. In order to prevent or suppress the impact of BW on the ECG waveform, the analog front-end requires a high-pass filter with high linearity and accuracy to minimize distortion.

The information in an ECG signal lies between 0.5-200 Hz. Implementing a filter cut-off in the sub-Hz region while maintaining high linearity and accuracy is challenging. Sub-Hz filter implementation translates to large area occupation on silicon and is thus expensive. Although there are several techniques to realize large time constants on-chip, there does not exist a highly linear high-pass transfer characteristic for Sigma-Delta ($\Sigma\Delta$) analog-to-digital converters (ADCs). The first part of the thesis addresses the implementation of large time constants with high linearity and accuracy. Chapter 3 of the thesis focuses on the design and analysis of a high-pass $\Sigma\Delta$ (HP$\Sigma\Delta$) analog-to-digital converter (ADC) that aims to achieve high linearity for the high-pass (HP) filter cut-off. State-space topologies, commonly used for optimizing filters, are proposed for developing the HP$\Sigma\Delta$

modulator topologies. A ΣΔ modulator can be represented as a linear model that consists of integrators and a quantizer, with the quantization noise modeled as additive white noise. By employing the state-space synthesis method, it becomes possible to develop arbitrary transfer functions for the signal and quantization noise of the state-space ΣΔ topologies. The dynamic range of the ΣΔ topology is optimized by signal and noise scaling. Through sensitivity analysis, the impact of coefficient variations in the different integrators on the overall performance and stability of the modulator is determined. Comparative analysis reveals that the orthonormal ΣΔ modulator outperforms the observable canonical state-space-based topology. The experimental results demonstrate that the orthonormal HPΣΔ ADC achieves a figure of merit (FoM) of 5.35 pJ/conv while occupying an area of 0.126 mm^2. The orthonormal HPΣΔ ADC also achieves a peak SNDR of 69.8 dB, corresponding to 11.3 bits of ENOB for a signal bandwidth of 3 kHz.

The second approach (and less commonly used) for diagnosing cardiac abnormalities is recording the AEG, targeting high spatial resolution using a multi-channel analog front-end. The primary difficulties encountered when acquiring multiple inputs are associated with a proportional increase in area, power consumption, and the number of outgoing wires. In order to mitigate the resource requirements and develop a compact solution for the multi-input system, channel-sharing techniques such as time-division multiplexing, frequency-division multiplexing, and code-division multiplexing (CDM) can be effectively incorporated. These techniques enable the efficient utilization of shared resources, optimizing the overall performance and reducing the system's complexity. CDM offers enhanced capacity by enabling multiple users to effectively share the same frequency band. It improves signal quality by effectively suppressing interference and band-limited noise, resulting in higher fidelity and more reliable transmission. The second part of this thesis (Chapter 4) focuses on acquiring multi-input AEG signals using CDM. It presents a systematic classification of modulation strategies based on their degrees of freedom to identify suitable techniques for analog signal acquisition. This work also introduces a design method for creating efficient spread-spectrum analog front-ends. Based on the proposed design strategy, spread-spectrum codes can be selected for a given application requirement (high or low-resolution acquisition). The modulation frequency and code length can be determined for optimal performance for the total number of inputs. A 4-input spread-spectrum recording system fabricated in a 0.18 μm CMOS process validates the proposed design method. With a 7-bit Gold code generator (L = 127), the maximum achievable crosstalk performance is -40 dB, and the thermal noise density of the system is 224 nV/$\sqrt{(}$Hz). The system includes shared components such as an amplifier, an analog-to-digital converter (ADC), and an on-chip Gold code generator, with a compact footprint and low power consumption per channel input of 0.067mm^2 and 23μA, respectively.

Recording AEGs using a high-density array of flexible electrodes leads to generating large amounts of data. A significant amount of area (for storage) and power (for data transmission) are required to handle the data. A custom-fabricated flexible multi-electrode array that contains 192 electrode sites is used to acquire the AEGs. Nine such sections are required to cover the entire area of an average adult heart. Chapter 5 focuses on the compressibility of AEGs. Standard compressed sensing is typically used to reduce the data using sub-Nyquist domain sampling on-chip and reconstruction using optimal algorithms off-chip. Signal statistics are not taken into account in standard CS. Both standard and

rakeness-based compressed-sensing are applied on atrial electrograms for data compression in this thesis. Rakeness-based compressed-sensing (CS), which uses the signal statistics of the known input signal, is proposed for compressing AEGs. Incorporating signal statistics in the random matrix in rakeness CS leads to better reconstruction performance at higher compression ratios. A similarity analysis is also conducted to quantitatively assess the quality of the reconstructed AEGs during sinus rhythm (SR) and atrial fibrillation. Also, a team of clinicians has visually inspected the reconstructed waveforms to check their suitability for generating an activation map (to map the wavefront of the signal that propagates through the heart). From the survey, it is found that for SR AEG signals up to a compression ratio (CR) of 4.26, the signal is considered clean. However, at CR = 5.1, it becomes noisier but remains suitable for specific applications. In contrast, AF AEG signals exhibit a faster decline in signal quality at higher CRs, attributed to increased activity and distinctive features of AF signals. Even at CR = 5.1, the signal can be used to estimate local activation times but lacks detail for comprehensive feature computation.

In summary, this thesis addresses numerous pivotal challenges, namely enhancing the linearity and accuracy of the HP filter cut-off for single-channel cardiac signal acquisition and maximizing resource efficiency for multi-channel cardiac acquisition. We have taken steps towards designing compact application-specific integrated circuits (ASICs) for recording and diagnosing cardiac abnormalities, such as AF. Understanding the underlying biological mechanisms through recording AEGs is crucial for early detection and monitoring of such conditions, which can significantly affect the course of disease progression.

Samenvatting

Hart- en vaatziekten (CVDs) eisen jaarlijks 17,9 miljoen levens (2019), wat neerkomt op 32% van alle sterfgevallen, waarvan 85% te wijten is aan hartaanvallen en beroertes [1] wereldwijd. Atrium-fibrilleren (AF), ook wel boezemfibrilleren genoemd, is het meest voorkomende type hartritmestoornis met 46 miljoen gevallen wereldwijd [2]. AF wordt gekarakteriseerd door de afwezigheid van P-golven op het elektrocardiogram en een onregelmatige hartslag. Hoewel de kennis en de diagnostische methoden voor AF de afgelopen jaren zijn verbeterd, zijn precisie en tijdige diagnose nodig voor effectieve behandeling. Elektrofysiologische metingen dienen als de gouden standaard voor het diagnosticeren van hartafwijkingen. Momenteel bestaan er twee belangrijke fundamentele benaderingen voor het monitoren van het hart vanuit een elektrofysiologisch standpunt. De meest voorkomende vorm is het ECG (elektrocardiogram), dat wordt opgenomen op het oppervlak van het menselijk lichaam op specifieke punten. Een nieuwere benadering (maar minder vaak gebruikt) is de meting van het AEG (atriaal elektrogram), dat wordt opgenomen op het oppervlak van het menselijk hart met een hogere ruimtelijke resolutie dan ECG. ECG is een techniek die wordt gebruikt om de elektrische activiteit van het hart op een niet-invasieve wijze te monitoren, terwijl AEG wordt gebruikt om diepgaandere en gedetailleerdere inzichten te verkrijgen in de elektrische geleidingspaden van het hart op een invasieve manier. AEG's worden gebruikt om de oorsprong van AF te lokaliseren voor een geschikte behandeling. Hoofdstuk 2 gaat dieper in op de toepassing, de bijbehorende technologische uitdagingen en de bestaande oplossingen in de literatuur met betrekking tot de acquisitie van hartsignalen.

De eerste benadering (en de meest gebruikte) voor het diagnosticeren van hartafwijkingen is het opnemen van het ECG, met een hoge signaal-ruis-en-interferentieverhouding en voldoende bandbreedte, met behulp van een enkelkanaals analoge front-end. Een van de belangrijkste uitdagingen bij het verkrijgen van ECG is baseline wandering (BW), wat verwijst naar laagfrequente variaties die de basislijn van de opgenomen golfvorm beinvloeden. BW treedt op door beweging van het lichaam of slecht contact tussen het lichaamsoppervlak en de elektroden. De impact van BW op de kwaliteit van het ECG-signaal kan tweeledig zijn: (a) verzadiging van het CMOS analoge front-end leidt tot informatieverlies, en (b) vervorming van de ECG-golfvorm leidt tot misdiagnose. Om de impact van BW op de ECG-golfvorm te voorkomen of te onderdrukken, vereist het analoge front-end een hoogdoorlaatfilter met hoge lineariteit en nauwkeurigheid om vervorming te minimaliseren.

De informatie in een ECG-signaal ligt tussen 0.5-200 Hz. Het implementeren van een filter-kantelfrequentie in het sub-Hz regime met hoge lineariteit en nauwkeurigheid is uitdagend. Sub-Hz filterimplementatie leidt vaak tot een grote oppervlakte op silicium en is dus duur. Hoewel er verschillende technieken bestaan om lange tijdconstanten on-chip te realiseren, bestaat er geen zeer lineaire hoogdoorlaatkarakteristiek voor Sigma-Delta ($\Sigma\Delta$) analoog-naar-digitaal converters (ADCs). Het eerste deel van dit proefschrift behan-

delt de implementatie van lange tijdconstanten met een hoge lineariteit en nauwkeurigheid. Hoofdstuk 3 behandelt het ontwerp en de analyse van een hoogdoorlaat ΣΔ (HPΣΔ) ADC waarmee een hoge lineariteit behaald kan worden voor het hoogdoorlaat filter. Een toestandsbeschrijving (Engels: state-space description), een veelgebruikte manier om filters te optimaliseren, wordt voorgesteld om de HPΣΔ topologie te ontwikkelen. Een ΣΔ modulator kan worden voorgesteld als een lineair model dat bestaat uit integratoren en quantizers, waarbij quantisatieruis gemodelleerd wordt als additieve witte ruis. Door gebruik te maken van de state-space synthese-methode wordt het mogelijk om elk gewenste overdrachtsfunctie voor het signaal en de quantisatieruis te realiseren. Het dynamisch bereik van de ΣΔ topologie wordt geoptimaliseerd met behulp van signaal- en ruis-schaling. Een analyse van de gevoeligheid van het systeem voor variaties in de coefficienten van de verschillende integratoren op de stabiliteit en prestaties van het totale systeem wordt uitgevoerd. Deze analyse laat zien dat een orthonormale ΣΔ modulator beter presteert dan een topologie gebasseerd op een observable canonical state - space. Experimentele resultaten laten zien dat de orthonormale HPΣΔ ADC een figure of merit (FoM) heeft van 5,35 pJ/conv met een oppervlakte van 0,125 mm^2. De orthonormale HPΣΔ behaalt een piek SNDR van 69.8 dB, hetgeen overeenkomt met een ENOB van 11,3 bits voor 3 kHz signaal-bandbreedte.

De tweede (minder gebruikte) benadering voor het diagnosticeren van hartafwijkingen is het opnemen van een AEG, waarbij een hoge spatiele resolutie wordt verkregen door middel van een multi-kanaals analoog front-end. De primaire uitdagingen voor een multi-kanaals systeem zijn een proportionele toename in oppervlakte, stroomverbruik en het aantal draden. Een compacter en efficienter multi-input systeem kan worden verkregen door middel van technieken zoals time-division multiplexing, frequency-division multiplexing en code-division multiplexing (CDM). Deze technieken zijn efficient, optimaliseren de algemene prestaties en reduceren de complexiteit van het systeem. CDM verbetert de capaciteit door verschillende gebruikers dezelfde frequentieband te laten gebruiken. Het verbetert de signaalkwaliteit door interferentie en band-begrensde ruis te onderdrukken en resulteert in een betere kwaliteit en verbeterde betrouwbaarheid. Het tweede deel van dit proefschrift (Hoofdstuk 4) behandelt de acquisitie van meerkanaals AEG signalen door gebruik te maken van CDM. Een systematische klassificatie van verschillende modulatie-technieken wordt gepresenteerd om geschikte technieken te identificeren voor signaal-acquisitie. Tevens zal een ontwerpmethode gepresenteerd worden voor efficiente spread-spectrum analoge frontends. De voorgestelde strategie maakt het mogelijk spread-spectrum coderingen te selecteren op basis van specifieke eisen van de toepassing (zoals een hoge of lage resolutie). De frequentie van de modulatie en de lengte van de code kan worden bepaald op basis van de optimale prestaties voor het totale aantal inputs. Metingen aan een 4-kanaals spread-spectrum acquisatie-systeem gemaakt in een 0,18 μm CMOS process valideren de voorgestelde ontwerpmethode. Met een 7-bit Gold-code generator (L = 127) is de maximaal haalbare crosstalk -40dB en de thermische ruis van het systeem is 224 nV/$\sqrt{}$(Hz). Het systeem bevat gedeelde componenten zoals een versterker, een analoog-naar-digitaal converter en een on-chip Gold-code generator en heeft een compacte opppervlakte en laag stroomverbruik per kanaal van respectievelijk 0,067 mm^2 en 23μA.

Het uitlezen van AEGs met behulp van een flexibele electrode-array met hoge dicht-

heid leidt tot het generen van een grote hoeveelheid data. Een significante hoeveelheid oppervlak (voor opslag) en vermogen (voor data transmissie) zijn nodig. Een speciaal ontworpen flexibele multi-elektrode array met 192 electroden wordt gebruikt om AEGs te meten. In totaal zijn negen van dit soort arrays nodig om het volledige oppervlak van een menselijk hart te bedekken. Hoofdstuk 5 behandelt het comprimeren van AEGs. Standaard compressed-sensing wordt vaak toegespast om de data met behulp van sub-Nyquist domein sampling te reduceren op de chip en vervolgens buiten de chip te reconstrueren met behulp van optimale algoritmes. De statistische eigenschappen van het signaal worden niet gebruikt voor standaard compressed sensing. In dit proefschrift worden zowel standaard als rakeness-gebaseerde compressed-sensing toegepast op AEGs voor data compressie. Rakeness-gebaseerde compressed-sensing gebruikt de statistische eigenschappen van het ingangs-signaal en kan worden toegepast om AEGs te comprimeren. Het gebruikt van de statistische eigenschappen van het signaal in de random matrix in rakeness gebaseerde compressed sensing leidt tot betere reconstructie en hogere compressieverhoudingen. Een overeenkomsten-analyse wordt toegepast om de kwaliteit van de gereconstrueerde AEGs quantitatief te analyseren tijdens het sinusritme (SR) en het boezemfibrilleren. Een team van clinici heeft de gereconstrueerde signalen visueel geinspecteerd op hun geschiktheid om een activatie-plattegrond (om het verloop van het signaal dat door het hart beweegt in kaart te brengen). De analyse laat zien dat SR AEG signalen met een compressie-verhouding van 4.,6 leiden tot een voldoende resultaat. Wanneer een compressie-verhouding van 5,1 gebruikt wordt, bevat het resultaat meer ruis, maar is het nog geschikt voor bepaalde toepassingen. AF AEG signalen laten een snellere achteruitgang in signaal kwaliteit zien voor hogere compressie-verhoudingen, hetgeen veroorzaakt wordt door de hogere activiteit en specifieke eigenschappen van AF signalen. Zelfs voor een compressie-verhouding van 5,1 kan het signaal gebruikt worden om locale activatie te schatten, maar het heeft onvoldoende detail voor een uitgebreide analyse.

Samenvattend behandelt dit proefschrfijt verschillende doorslaggevende aspecten: het verbeteren van de lineariteit en nauwkeurigheid van de hoogdoorlaatfilter-karakteristiek van enkel-kanaals elektrocardiogrammen en het maximaliseren van de efficientie van multi-kanaals signaal-acquisitie. Er zijn stappen gezet om een compacte applicatie-specifieke geintegreerde schakeling (ASIC) te ontwerpen voor het opnemen en dagnostiseren van hartafwijkingen, zoals AF. Het begrip van de onderliggende biologische mechanismen door middel van het opnemen van AEGs is cruciaal voor het vroegtijdig detecteren en monitoren van dit soort aandoeningen, hetgeen de progressie van de ziekte significant kan beinvloeden.

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गुरुर्ब्रह्मा गुरुर्विष्णुः गुरुर्देवो महेश्वरः।
गुरुः साक्षात् परब्रह्म तस्मै श्री गुरवे नमः॥

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Samprajani
Delft, June 2024

1

Introduction

This chapter presents a short overview of cardiac electrophysiology, including the characteristics of the cardiac signals. It also elaborates on the importance of high-density atrial electrograms and the technological challenges associated with acquiring cardiac signals. Finally, the structure of the thesis and the outline are presented.

1

In this section, we provide a summarized overview of the background of cardiac electrophysiology and emphasize the importance of cardiac signal recording in diagnosing and treating cardiac abnormalities.

Cardiovascular diseases (CVDs) refer to a group of disorders of the heart that include cardiac arrhythmias, congenital heart disease, and heart failure and are one of the leading causes of death worldwide. According to the World Health Organization (WHO) factsheet, about 17.9 million [1] people, representing 31% of all deaths, die each year due to CVDs. To be able to treat cardiac arrhythmias with a higher success rate, it is necessary to detect and diagnose the abnormalities of the heart early on in order to have more treatment options and increase the chances of survival. Typically, individuals suffering from CVDs report to the hospitals due to pain or discomfort when the disease has already progressed to an advanced stage. Atrial fibrillation (AF), a commonly occurring cardiac arrhythmia, poses a challenge to doctors and clinicians due to the limited understanding of its physical progression.

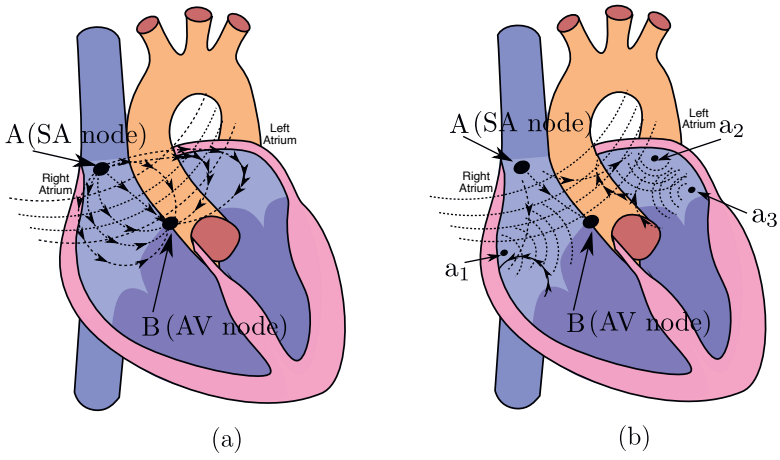


Figure 1.1: Illustration of (a) Sinus rhythm (SR), and (b) Atrial fibrillation (AF).

Figure 1.1 depicts the state of the heart in both a normal and an abnormal condition. Figure 1.1a represents the heart in sinus rhythm (SR), the normal functioning condition. Point *A* refers to the sinoatrial node (SA node) located in the right atrium, which is the heart's natural pacemaker. Point *B* refers to the atrioventricular node (AV node) responsible for regulating the electrical impulses that travel from the atria to the ventricles. During sinus rhythm, the electrical impulse is generated at point *A*, passes through the heart's atrial chambers, and reaches node *B*. The electrical impulses reaching the AV node are delayed there. The delay through various paths gives an appropriate amount of time for the atria and ventricles to contract in a coordinated manner to optimize the efficiency of blood flow. The figure shows that the wavefront is traversing in a single direction. On the other hand, Figure 1.1b depicts the pathological state of the heart characterized by atrial fibrillation, an abnormal cardiac rhythm disorder. Points a_1, a_2, and a_3 represent the secondary foci that lead to abnormal electrical conduction pathways and blocks, which characterizes AF. As shown in the figure, multiple secondary wavefronts are generated due to the foci

leading to the irregular beating of the heart.

AF is commonly characterized by the absence of P-waves and irregular RR intervals seen on an ECG and is the most frequently occurring arrhythmia in clinical practice. It is estimated to affect more than 24 million individuals in the developed world by 2060 [3] and poses a global health burden. The currently available therapies for AF include drug therapy, catheter-based ablation, and stimulation using implantable defibrillators. These therapies are only partially effective since the exact underlying mechanisms of the propagation of the signal through the cardiac tissue and the degeneration of tissue causing changes in the electrical pathways are not yet fully understood.

Conventionally, AF is diagnosed through recordings of electrophysiological signals, which has been the gold standard for detecting and treating cardiac diseases. Electrophysiological signals such as the electrocardiogram (ECG) and the atrial electrogram (AEG) captures the electrical activity that contains information about the polarization and subsequent contraction of the atrium of the heart. A combination of two approaches can be taken to diagnose AF early on and to understand the mechanisms that govern the propagation of electrical signals in the heart. First, ECG can be recorded on the surface of the human body, a non-invasive procedure that can be used as a screening tool for continuously monitoring patients at higher risk. Second, to gain an understanding of the propagation of signals at the tissue/cellular level, high-density spatiotemporal AEGs can be recorded invasively.

The need for a high-density mapping of AEGs targeting high spatial resolution is explained in Section 1.1. The nature of the cardiac waveforms involved is described in Section 1.2. The thesis objectives and challenges are elaborated in Section 1.3. Finally, the organization of the thesis and the original contributions are summarized in Section 1.4.

1.1 Need for high-density atrial electrograms

ECG is recorded on the body's surface and is a vector summation of the electrical activity occurring within the heart [4]. While it provides information on the overall functioning of the heart, ECG offers low spatial resolution and hardly any insight into the way the signals propagate through the heart. To understand the tissue/cellular mechanisms of the propagation of signals, i.e., the flow of electrical activity followed by the mechanical pumping of blood, it is necessary to record signals with a higher spatial resolution and closer to the location of the generation of these signals [5]. Therefore, the signals are recorded invasively on the surface of the heart. This way, tissue properties that govern the direction of propagation of signals can be studied. During AF, the signal is chaotic and gives rise to secondary wavefronts, as shown in Fig. 1.1. Due to the incoherency in the electrical impulse received at the AV node, the heart rate is irregular. At an early stage, such a condition occurs only intermittently. As the arrhythmia progresses, the occurrence of such events becomes more frequent and may result in cardiac arrest. In the following section, we delve into the nature of the cardiac signals to gain a more comprehensive understanding of the cellular-level processes involved.

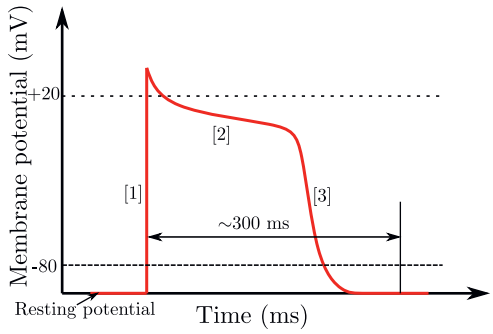


Figure 1.2: Action potential of a cardiomyocyte.

1.2 Characteristics of cardiac signals and commercially used high-density mapping catheters

The heart wall is a three-layered structure consisting of the myocardium, epicardium, and endocardium. The myocardium, also known as the cardiac muscle tissue, forms the bulk of the heart. The epicardium on the outside covers the myocardium, while the endocardium covers the inner cardiac chambers. A cardiomyocyte is a cardiac muscle cell that resides in the myocardium. The excitation and contraction of the cardiomyocytes are regulated by action potential (AP). AP, shown in Fig. 1.2, refers to the generation of an impulse due to the changes in membrane potential across a cell. In a cardiac system, the AP controls the excitation of cardiac fibers. All the cardiac fibers contract in coordination as one unit. The depolarization wave travels throughout the heart through the gaps between the fibers. The action potential of a cardiomyocyte is generated by the exchange of charged ions, namely sodium (Na^{2+}), calcium (Ca^{2+}) and potassium (K^{+}) ions through the ion channels across the cell membrane as shown in Fig. 1.2. During the first phase, due to the influx of extracellular Na^{2+} ions in the fast voltage-gated Na^{2+} channels, the AP rises from a resting potential of -90 mV to about +30 mV as illustrated in Fig. 1.2. During the second phase, Ca^{2+} ions enter through the slow voltage-gated Ca^{2+} channels characterized by a plateau phase. During the third phase, the Ca^{2+} ion channels deactivate and open the K^{+} channels. Due to the loss of K^{+} ions, the membrane potential comes back to its resting voltage. The three phases constitute a complete AP of the cardiomyocyte. As a side note, in a nervous system, the AP (as shown in Fig 1.3) transmits information in the impulses between neurons.

At the cellular level, different locations, such as the SA node, atrial muscle, AV node, bundle of His, Purkinje fibers, and ventricular muscles, give rise to various shapes of the cardiac action potential. The surface of the heart, also referred to as the epicardium, receives various signals that are vectorially added, resulting in composite signals, which are recorded over the electrode surface area. Flexible and biocompatible electrode arrays [5] can be used to record signals originating from the epicardium (the outer wall of the heart) and the endocardium (the inner wall of the heart), which represent the exposed portions of the heart wall. Table 1.2 summarizes the characteristics of the signals recorded at various locations in the heart. It also enlists the type of recording (invasive/minimally

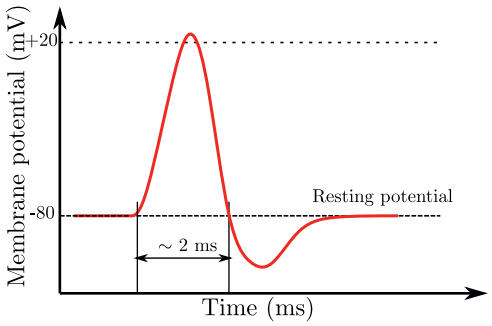


Figure 1.3: Action potential of a neuron.

Table 1.1: Characteristics of cardiac signals

Signal	Location	Technique	Inter-electrode dist. (mm)	Amplitude (mV)	Frequency (Hz)
ECG	Body surface	Non-invasive	2 - 20	0.5 - 3	0.5 - 200
Epicardial AEG	Heart's outer wall	Invasive	2	1 - 10	0.5 - 400
Endocardial AEG	Heart's inner wall	Minimally invasive	2 - 6	20 - 80	0.5 - 400
Cardiomyocytes AP	Myocardium	Invasive	< 1	0.1 - 0.5	1 - 10k

invasive/non-invasive) for various signal waveforms and the preferred inter-electrode distance. Atrial electrograms can be recorded on the epicardium or the endocardium. A few commercially used catheters targeting minimally invasive applications that map the electrograms are the Orion from Boston Scientific [6] and the HD Grid from Abbott [7]. [8] uses the Octaray and Pentaray from Biosense Wester and compares the high-density catheters' performance. The electrode count of the catheters varies from 16 - 64 and has an interelectrode distance varying from 2 - 6 mm. The electrode length varies from 0.2 to 1 mm.

1.3 Thesis objectives and challenges

The primary aim of this dissertation is twofold. Firstly, it focuses on examining various approaches and design techniques aimed at achieving high linearity and accuracy for implementing large on-chip time constants to acquire cardiac signals and other biosignals. Secondly, it investigates compact and efficient multiplexing strategies for acquiring signals from a multi-electrode array while concurrently reducing the number of outgoing wires.

An analog front-end is needed to transform the analog signal that is recorded by means of an electrode into a digital signal that can be stored/transmitted/analyzed further. As the ECG/AEG signal is analog (continuous-time and continuous-magnitude) in nature, relatively weak and contaminated by unwanted signals and noise that, a.o., manifest themselves at other frequencies, an ECG/AEG analog front-end usually implements the following functions: 1. amplification, 2. filtering, and 3. analog-to-digital conversion. In acquiring cardiac signals, the design of analog front-ends faces several challenges. These challenges are addressed under single-channel and multi-channel acquisition front-ends in the following sub-sections.

1

1.3.1 Single-channel front-end to record electrocardiograms (ECG)

In the design of single-channel front-ends aimed at clinical diagnosis, implementing the high-pass filter cut-off with sufficient accuracy is a significant challenge.

Baseline wandering and accuracy of filter cut-off frequency

ECGs are used to record signals on the surface of the human body, i.e., non-invasively on the chest. The relevant frequency band of an ECG signal lies between 0.5-200 Hz and, within that band, the ECG signal has an amplitude of about 1-5 mVp-p. Depending on the application of the ECG, such as ST-segment monitoring, R-peak detection, or QRS detection, the analog front-end can be designed to meet the amplitude and frequency specifications. One key limitation in single-channel acquisition has been baseline wandering and accuracy of the high-pass filter cut-off frequency [9]. Due to the inaccuracies of the filter cut-off frequency, the signals appear distorted and can lead to inaccurate diagnosis. Since the signals lie in the low-frequency regime, the implementation of the associated large time constant usually leads to large area consumption on a chip.

1.3.2 Multi-channel front-end to record atrial electrograms (AEG)

In the design of multi-channel front-ends for the acquisition of AEGs [5], the challenges are as follows:

- A large number of recording channels leads to a large amount of data.
- If each channel is implemented separately, a large number of channels results in a large number of outgoing wires.
- A large number of outgoing wires impacts the flexibility and maneuverability of the electrode array.
- If the electrode array is at a relatively large distance from and thus not integrated with its readout electronics, interference will be picked up that is not easy to separate from the information-carrying signals.

The above-listed challenges are further elaborated in the following sub-sections.

Generation of large amount of data

A large number of electrodes and monitoring of signals for a long time pose a challenge to the amount of data to handle. AEGs are acquired with a high-resolution multi-electrode array and an acquisition module. The electrode array used to record AEGs [5] consists of 192 electrodes. Nine such sections are required to cover an entire average adult heart. To record signals from 1728 (= 9 x 192) electrodes, with a resolution of 16 bits, and a sampling rate of 10 kHz, the total data rate required is 16 x 10 × 10^3 x 1728, or 276 Mbit/s, resulting in ≈ 16.6 Gbit/min [10]. The required hardware resources to handle the data are enormous. A significant amount of power and hardware resources in terms of memory and area are needed to transmit and store the data, making the acquisition module expensive. Therefore, compression methods can be applied for efficient data recording and transmission to reduce the power consumption and the footprint of the electronics. Compressed sensing allows simultaneous acquisition and compression of the signals and can be used to acquire AEGs [10].

Interference and constraint on outgoing cable wires

There is a need to acquire signals from multiple electrodes efficiently and compactly. Sharing resources such as amplifiers, analog-to-digital converters, and cables across multiple electrodes reduces power and area consumption. Commonly used approaches for acquiring multi-channel signals include time-domain multiplexing (TDM) [11], frequency-domain multiplexing (FDM) [12] and code-division multiplexing (CDM) [13].

Practically, time-domain multiplexing requires a dedicated amplifier (due to the dynamic (time-dependent) behavior of the amplifier) per electrode, which increases power and area as the number of electrodes increases. In FDM, a dedicated oscillator is required for each electrode, which makes it unsuitable for large electrode count applications. However, CDM can acquire signals from several electrodes simultaneously with a shared front-end, making it attractive as a low-power and compact solution. As each signal is encoded with a unique code, it suffers from lower interference and noise than TDM or FDM, owing to the advantages of spread-spectrum modulation. Also, as a consequence of the multiplexing, a single wire can be used to transmit the digital data out of the analog front-end. Integrating the electrode array and the electronics module alleviates the need for a long multi-wire cable between the patient and the acquisition module, thus providing a maneuverable prototype.

A detailed review of the state-of-the-art architectures to solve the challenges listed above is described in Chapter 2. In the next section, the outline of the thesis, along with the original contributions, is summarized.

1.4 Thesis outline

This thesis consists of three major parts. Following the review provided in Chapter 2, the first part (Chapter 3) focuses on the design strategy and implementation of state-space based ΣΔ modulators. It introduces the design of an HPΣΔ ADC. Multi-channel strategies are investigated in the second part (Chapter 4). The design and optimization of a spread-spectrum analog front-end using shared resources are presented. The third part (Chapter 5) presents rakeness-based compressed sensing for atrial electrograms.

Chapter 2 reviews the current state-of-the-art techniques for efficiently and accurately acquiring single-channel and multi-channel cardiac signals. This review discusses the existing methods and summarizes the main challenges faced by the state-of-the-art techniques. By exploring the strengths and limitations of these techniques, the chapter sets the stage for the subsequent chapters.

Chapter 3 introduces a state-space approach to optimize the dynamic range of ΣΔ ADCs. This approach offers a systematic approach for designing ΣΔ modulators with arbitrary signal-transfer functions. The chapter delves into the details of the state-space approach design method and illustrates its practical application through experimental results.

Chapter 4 presents a spread-spectrum approach specifically designed to address the challenges of physical area requirements in acquiring multiple-channel atrial electrocardiograms (AEGs). By employing spread-spectrum techniques, this approach enables efficient and simultaneous acquisition of multiple AEGs, making it suitable for multi-channel applications. The chapter discusses the design considerations, implementation details, and

performance evaluation of the spread-spectrum approach, highlighting its effectiveness in achieving power and area efficiency.

Chapter 5 delves into compressed sensing techniques for atrial electrograms. Compressed sensing allows for reconstructing high-quality AF signals from significantly fewer measurements by exploiting the inherent sparsity or structure in the electrograms. This chapter explores how the characteristics of the input signals can be leveraged to enhance the reconstruction performance, leading to improved accuracy in AF detection.

Chapter 6 serves as the concluding chapter of the thesis, providing a comprehensive summary of the scientific contributions made throughout the study. It highlights the essential findings and advancements in the earlier chapters, emphasizing their significance in cardiac signal acquisition. Additionally, this chapter discusses future research directions and potential areas for further exploration, outlining the broader implications of the thesis and its potential impact on advancing the field of cardiac signal acquisition.

1.5 Original contributions

The original contributions of this work are summarized from Section 6.2 as follows:

1. A state-space design method for dynamic-range optimization of HPΣΔ ADCs and their application to acquire single-channel electrocardiograms accurately (Chapter 3).

2. The design and implementation of highly accurate and linear HPΣΔ ADCs (Chapter 3).

3. A spread-spectrum design method for power- and area-efficient acquisition of multiple-channel AEGs (Chapter 4).

4. The design and implementation of an analog front-end based on spread-spectrum modulation using an on-chip PRBS code generator (Chapter 4).

5. Compressed sensing of atrial electrograms for the detection of AF using input-signal characteristics to improve the reconstruction performance (Chapter 5).

2

Review of state-of-the-art architectures of biopotential read-out front-ends

This chapter presents an overview of the techniques for acquiring single-channel and multi-channel biosignals, focusing on non-invasive and invasively acquired cardiac signals. The cardiac signal acquisition challenges, such as accuracy and linearity of the input-output relation in case of a high-pass filter characteristic for a single-channel front-end, maneuverability, reduced outgoing wire count, and compact solution for a multi-channel recording front-end, are discussed. The chapter reviews the state-of-the-art solutions for acquiring cardiac signals invasively and non-invasively.

2.1 Introduction

The heart is a primary organ of the circulatory system and is responsible for pumping blood throughout the body and maintaining the heart rate and blood pressure. During regular operation of the heart, the heart rate is generally consistent. During abnormal operation of the heart, the heart rate is inconsistent. The heart-rate abnormality is intermittent in the early stages of cardiovascular diseases (CVDs). Gradually, the heart rate becomes consistently abnormal. Heart attacks and strokes are acute events that occur due to the progression of CVDs. According to WHO, 17.9 million people died from CVDs in 2019, which represents 32% of all global deaths [1]. About 85% of these deaths were due to heart attacks and strokes. Atrial fibrillation, a type of cardiac arrhythmia, is the most frequently occurring arrhythmia in clinical practice [3]. AF can be detected using the recordings of electrophysiological signals such as the electrocardiogram (ECG) on the surface of the body, endocardial atrial electrogram on the inner layer of the heart (endocardial recordings), and epicardial atrial electrogram on the outer layer of the heart (epicardial recordings).

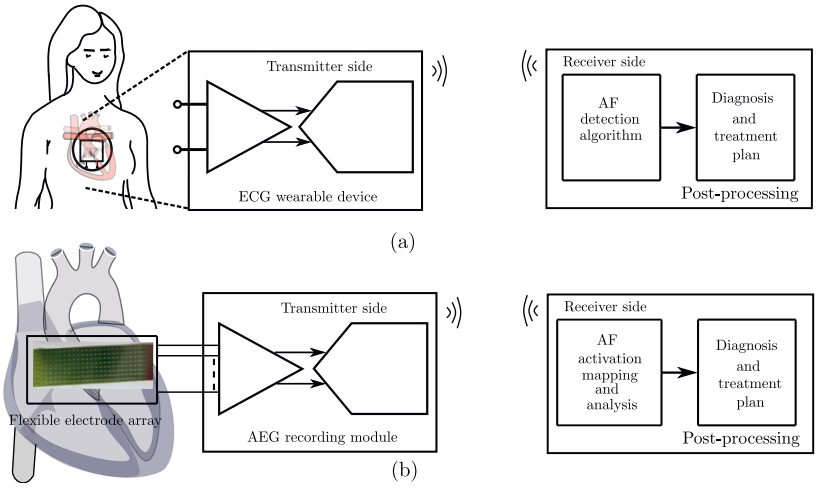


Figure 2.1: Block diagram of a wireless (a) ECG front-end (surface of the body), and (b) AEG front-end (surface of the heart).

For recording the ECG, a single-channel front-end with high resolution can be used as shown in Fig 2.1a. For recording the AEG invasively, a multi-channel flexible electrode array can be used to map the epicardial surface of the atria with high spatial resolution [5] as shown in Fig 2.1b. For minimally invasive recording, catheter-based systems [14] (with a much lower number of electrodes) can be inserted via the blood vessels and used to record the inner surface of the heart (i.e., the endocardial surface). The main challenges in acquiring cardiac signals can be summarized as follows.

- Firstly, signals recorded on the body surface suffer from motion artifacts due to patient movement, poor contact between the body and the electrodes, and respiration. An accurate high-pass filter is required to suppress the impact of large low-amplitude baseline variation and thus prevent saturation of the front end. At the same time, preserving the linearity of the transfer function at the cut-off frequency is vital to suppress distortions of the acquired waveform.

- Secondly, acquiring data from several electrodes simultaneously increases power and area consumption linearly with the number of inputs. Also, having many outgoing wires from the acquisition module is inconvenient. Optimal circuit techniques are required to share resources among the inputs and reduce the outgoing wire count.

- Thirdly, for handling the large amounts of data generated from a high-density mapping application, compression techniques are required to minimize the power consumption and area consumed due to transmission and data storage.

This chapter focuses on state-of-the-art architectures and solutions to address the abovementioned challenges.

2.2 Single-channel cardiac acquisition systems

Single-channel cardiac acquisition analog front-ends (AFEs) are critical to modern electrocardiogram (ECG) recording systems. These systems are used to monitor and diagnose various heart conditions by measuring the electrical activity of the heart. Single-channel cardiac acquisition AFEs play a crucial role in diagnosing various heart conditions, such as arrhythmias, ischemia, and heart failure. The AFE is responsible for acquiring the raw ECG signals from the electrodes attached to the patient's chest and processing them to produce a high-quality, low-noise output signal. The single-channel AFE is designed to process the signals from a single ECG lead, which consists of two electrodes placed at specific locations on the chest. The AFE typically consists of several amplification stages, filtering, and signal conditioning to remove noise and other unwanted artifacts from the ECG signal. The output of the AFE is then digitized using an analog-to-digital converter.

One of the critical challenges in acquiring accurate and high-resolution biosignals is baseline wandering (BW), which refers to a low-frequency drift or fluctuation in the signal's baseline. Baseline wandering is observed in signals such as electrocardiograms (ECG), electroencephalograms (EEG), and electromyograms (EMG) and occurs due to electrode movement, breathing, or patient movement. BW can make it challenging to analyze the physiological activity of interest and even obscure important signal features. Therefore, removing baseline wandering from the signal is essential before further analysis, which can be done using high-pass filtering, wavelet-based methods, or baseline correction techniques. In [15], a method for tracking the baseline is suggested that involves digitally extracting the DC offset and subtracting it from the front-end amplifier adaptively to correct the baseline of the signals. However, it uses a microcontroller to compute the offset. [16] proposes an adaptive DC-level control using ICA (independent component analysis) implemented on an FPGA to reduce the impact of baseline wandering. [17]

proposes wavelet filtering to suppress motion artifacts in ambulatory ECG. The abovementioned techniques work on digitized data and require memory and computational power to extract the baseline. Analog filtering, such as done by a passive first-order RC filter, is simple but can consume an enormous amount of chip area for sub-Hz implementations. Active-RC filter implementations, such as a MOSFET-C filter, can introduce significant distortion to the waveform since the terminal voltages of the MOSFET modulate the resistance. The frequency content of biosignals typically lies below 1 kHz. With the bandwidth of the ECG signal extending from sub-Hz to 200 Hz [18], a significant challenge for an ECG readout system lies in implementing the sub-Hz high-pass cut-off frequency as this translates into the realization of large time constant. Acquiring cardiac signals with high resolution and high accuracy of the time constant is a challenge, particularly if an integrated-circuit solution is aimed for. To realize large time constants in the order of a few seconds, there exist techniques that employ pseudo-resistors [19], [20], [21] or g_m blocks [22] or off-chip solutions such as using an IIR-filter [23] or a resistor [24].

Although these techniques realize large time constants in an area and power-efficient manner; they are heavily limited in accuracy. The existing solutions do not focus on achieving good linearity around the HP cut-off frequency. However, it is an important performance metric to acquire a low-distortion bio-signal waveform, especially in the case of cardiac signals aimed at diagnostic quality ECGs [18]. Also, pseudo-resistors are not very robust to PVT variations. Hence, when better linearity and accuracy are required, alternative techniques need to be developed. To address acquiring ECG signals with a linear input-output relation and accuracy of the filter cut-off frequency and a sufficiently large signal-to-noise ratio, a synthesis procedure for the design of high-pass sigma-delta modulator topologies that are optimized for linearity, low noise, and minimum sensitivity to component and other variations, will be presented in Chapter 3.

2.3 Multi-channel cardiac acquisition systems

In a traditional N-input system, the total number of amplifiers, ADCs, and outgoing wires equals the number of inputs, thus scaling the system's area, power consumption, and outgoing wire count linearly by N. To address these limitations, one can use channel-sharing techniques such as time-division multiplexing (TDM), frequency-division multiplexing (FDM), or code-division multiplexing (CDM) as illustrated in Fig. 2.2 and which are elaborated in the following paragraphs.

TDM is a multiplexing technique that divides the available acquisition time into time slots, each assigned to a different input. Each input is assigned a unique time slot to acquire, process, or transmit data. As an example, TDM is commonly used in cellular phone networks, where each connection is assigned a dedicated time slot during which the transmitter and the receiver can exchange information. [11] uses a dedicated amplifier per input and does not utilize the total bandwidth of the ADC effectively. Each input is processed using dedicated programmable gain amplifiers and band-pass filters. A shared ADC is used to digitize the inputs. The order of the inputs is essential for reconstruction in the digital domain, which is coordinated by digital control. [25] uses TDM to acquire signals after the electrode but requires a high-bandwidth front-end to meet the settling and noise requirements. The input capacitors, amplifier, filter, and ADC are shared among all the inputs. Sharing of input capacitors could lead to significant amplitude errors due to

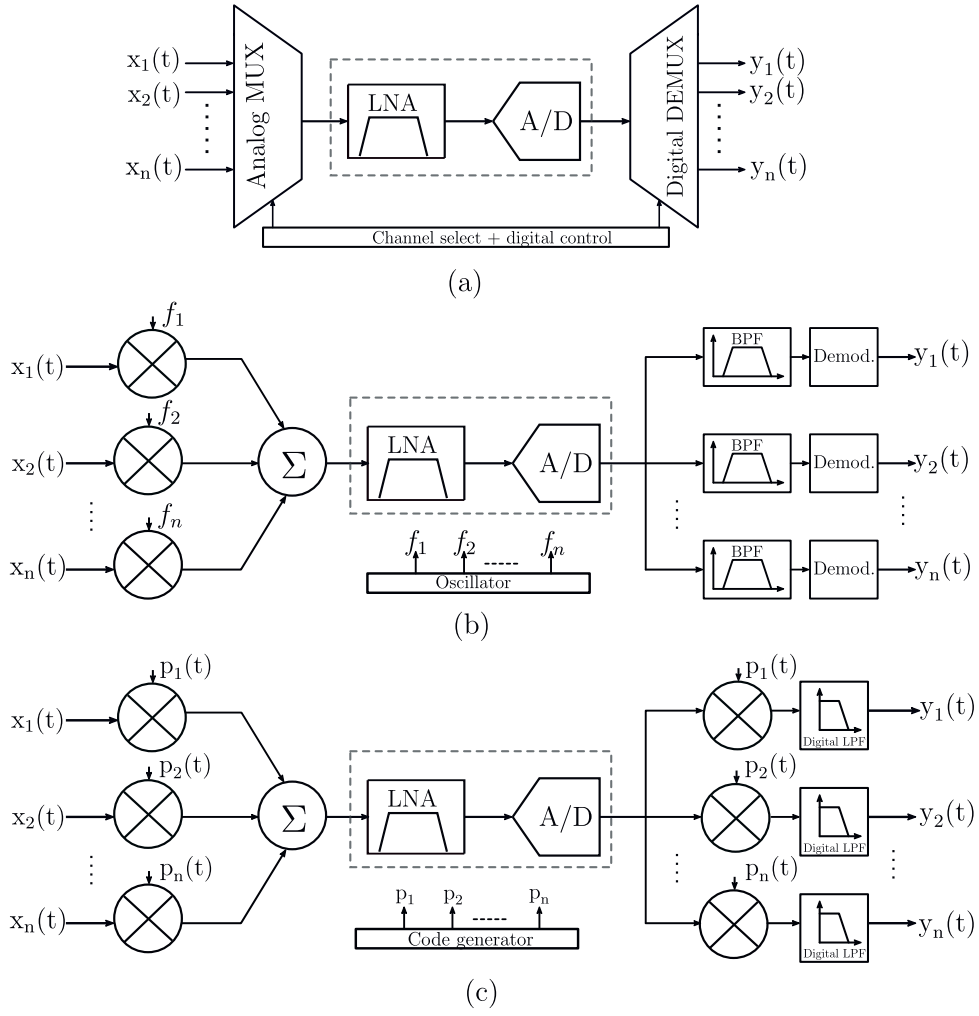


Figure 2.2: Illustration of (a) TDM, (b) FDM, (c) CDM for the acquisition of biosignals.

charge residue while switching between inputs. Fig 2.2a demonstrates an implementation of a TDM AFE. An analog multiplexer selects an input, $x_n(t)$, in a given time slot through the channel selector and uses a shared channel consisting of a low-noise amplifier (LNA) and an ADC to digitize the analog signal. The demultiplexer receives the time-division-multiplexed signal and separates the samples into their respective inputs.

FDM is a multiplexing technique that divides the total available frequency band into smaller frequency bands, with each band assigned to a different user or input. Each user or input transmits its data through the assigned sub-band. FDM is commonly used in radio and television broadcasting systems, where different radio stations or television channels are assigned different frequency bands. In [12], FDM based on frequency modulation (FM) uses separate frequency bands simultaneously and requires a dedicated oscillator, a band-pass amplifier, and an off-chip high-Q inductor per input, which poses a constraint on the area and power. FDM based on amplitude modulation (AM) would require a very high dynamic range (>100 dB) ADC due to voltage summation of all inputs [12]. Fig 2.2b demonstrates an implementation of FDM. In FDM, each signal $x_n(t)$ is assigned a different frequency band or sub-channel. The signals are then modulated with carrier waves $f_n(t)$ generated by oscillators, and the modulated signals are combined and transmitted over the same channel. After digitization, the signals are separated by using band-pass filters and subsequently demodulated.

CDM is a multiplexing technique that allows multiple users or inputs to share the entire frequency band simultaneously by assigning each user or input a unique code. These codes are referred to as spread-spectrum codes. Each input is assigned a unique code to transmit and receive data. The receiver uses the same code to decode the transmitted data. CDM is commonly used in wireless communication systems, such as some cellular phone networks, where multiple users can transmit and receive data simultaneously using the same frequency band. In the acquisition of biosignals, [26] implements CDM using a dedicated amplifier and filter circuitry before code modulation, whereas [27] modulates the signals at the input using orthogonal codes. CDM offers (a) increased capacity, allowing multiple users to share the same band, (b) improved signal quality as it suppresses interference and band-limited noise, (c) improved security since a unique code encodes each input, and (d) simpler implementation, as compared to FDM. Fig 2.2c demonstrates an implementation of CDM. The modulator can be positioned at the beginning or end of the signal chain, either preceding the LNA, following the LNA, or following the ADC. In this case, the modulator is situated near the input signal to allow for the sharing of the amplifier and the ADC. Each signal $x_n(t)$ is assigned a unique code $p_n(t)$ that is used to modulate the signal. The modulated signals are combined and transmitted over a shared channel using an amplifier and an ADC. After digitization, a replica of the codes is used to retrieve the individual signals by demodulation.

2.4 Data compression

For the diagnosis of diseases that require continuous monitoring of biosignals such as the electrocardiogram (ECG), the electroencephalogram (EEG), the electromyogram (EMG), and photoplethysmography (PPG) for the detection of intermittently occurring abnormal events, a high-resolution analog front-end is used for recording and transmitting data to the base station. Cumulatively, several such point-of-care non-invasive devices generate

a large amount of data. An example of invasive recording is the acquisition of atrial electrograms on the surface of the heart [5]. They are acquired with a high spatial resolution from a high-density multi-electrode array to capture the wavefront during signal propagation in the heart. Using a custom fabricated multi-electrode array with an inter-electrode distance of 2 mm, 1728 recording sites are required to cover the entire heart [10]. A large amount of data is generated, posing a practical challenge in storage and transmission. Compressed sensing, also known as compressive sensing, allows for data reduction and alleviates the burden on available resources by employing sub-Nyquist-domain sampling techniques. [28] discusses the design considerations for acquiring ECG and EMG signals using a compressed-sensing approach. The sparsity control and thresholding of the input signal determine the compression factor. If, for example, the application requires coarse features such as heart rate or sudden specific movements, the input signal can be made highly sparse via thresholding in the temporal domain to detect specific events. A compression factor can be selected based on the sparsity of the signal in a specific domain. [29] presents a randomly modulated pre-integration (RMPI) based architecture that exploits the rakeness or the signal characteristics of the input signal to improve reconstruction performance. A compression factor of about 8-10 is achieved from measurement tests on ECG and EMG. [30] presents a compressed-sensing architecture for multi-channel cortical acquisition. A dedicated preamplifier and front-end filtering circuit per channel with a shared summing stage and a successive approximation register ADC are implemented. However, the extent to which the AEG signals can be compressed using the compressed sensing approach has never been studied. Therefore, compressed sensing of AEGs is the focus of the third major part of this thesis.

2.5 Conclusions

This chapter reviews the state-of-the-art literature for single- and multi-channel cardiac acquisition systems. It presents the background of the application area and the relevance of cardiovascular diseases in society. It also discusses the challenges of acquiring single- and multi-channel biosignals. It delves into the limitations of current approaches for single-channel cardiac acquisition systems that employ highly linear, large-time-constant techniques. It also explores strategies for acquiring signals from multiple sites while optimizing resource utilization to minimize power consumption and chip area in multi-electrode applications. It also explores data compression as a potential technique to manage the substantial volume of data generated by multi-channel acquisition systems. In the following chapters, each of these challenges will be addressed individually, and a solution is proposed to solve them.

3

A state-space approach for optimal design of ΣΔ converters

Cardiac signal acquisition with high linearity and accuracy of the high-pass cut-off frequency imposes a challenge on the implementation of analog preprocessing and analog-to-digital converter. This chapter describes a state-space-based methodology for designing high-pass sigma-delta (HPΣΔ) topologies, targeting high accuracy and linearity of the high-pass cut-off frequency and filter transfer. Intermediate functions are evaluated mathematically to compare the proposed HPΣΔ topologies with respect to dynamic range. A sensitivity performance analysis of the noise transfer function with respect to integrator non-idealities and coefficient variations is also described.

To illustrate the design approach, a complete analog front-end (AFE) consisting of a pre-amplifier, a mixed-signal feedback loop that implements the HP transfer function, and an orthonormal ΣΔ modulator is implemented in 0.18 µm CMOS technology and validated by electrical characterization and acquiring real ECG signals from a live subject. The single-channel AFE consumes 63.4 µA and achieves a linearity of 60 dB at the high-pass cut-off frequency. The orthonormal ΣΔ modulator achieves an SNDR of 69.8 dB for a signal bandwidth of 3 kHz, while consuming 45 µA from a 1.8 V power supply, resulting in an FoM of 5.35 pJ/conv.

This chapter is partly based on *S. Rout and W. Serdijn: Structured electronic design of high-pass ΣΔ converters and their application to cardiac signal acquisition, proc. ISCAS'17* [31] and *S. Rout and W. Serdijn. High-pass ΣΔ converter design using a state-space approach and its application to cardiac signal acquisition, IEEE TBioCAS, 2018* [32].

3.1 Introduction

To diagnose and understand the underlying mechanisms of cardiac arrhythmia, a high-resolution and large-bandwidth analog front-end recording electrocardiogram and atrial electrogram signals aimed at clinical research purposes is required. This chapter describes a state-space-based methodology for designing high-pass sigma-delta (HPΣΔ) topologies, targeting high linearity and accuracy of the high-pass cut-off frequency. Based on the proposed state-space method for the optimal design of ΣΔ converters, an orthonormal ΣΔ converter is implemented. To illustrate the design approach, a complete analog front-end consisting of a pre-amplifier and an orthonormal HPΣΔ modulator is implemented in 0.18 μm CMOS technology, and is tested with a real ECG signal from a live subject.

This chapter is organized as follows. Section 3.2 presents the state-space design approach, noise analysis using intermediate functions and testing the orthonormal HPΣΔ topology with real-prerecorded ECG signals. Section 3.3 presents the design, implementation, and validation of a complete analog front-end for the acquisition of cardiac signals using an orthonormal ΣΔ ADC in a 0.18μm CMOS process. Section 3.4 presents the conclusions of the chapter.

3.2 High-pass ΣΔ converter design using a state-space approach

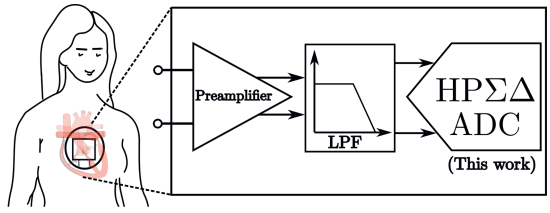


Figure 3.1: Analog front-end for ECG acquisition

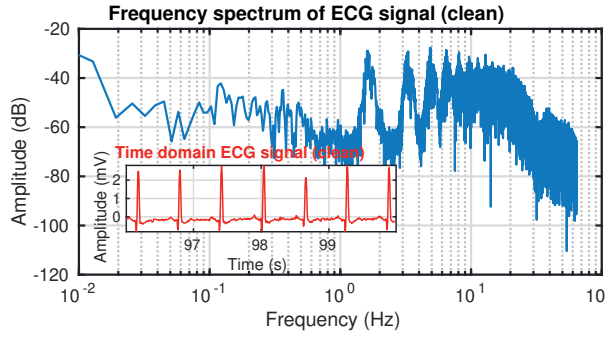
Electrocardiography (ECG), the recording of electric signals generated by the heart is used as a diagnostic monitoring method for cardiovascular diseases (CVDs). It contains specific physiological information about the functioning of the heart. To meet the growing demand of the geriatric population and to reduce the burden on the public health-care system, there is a requirement of compact, inexpensive health-care devices that enable continuous ECG recording for the detection of cardiac arrhythmias that manifest themselves as aperiodic events over a period of days or weeks. Acquisition of the ECG is faced with the challenge of removal of the baseline wandering due to respiration or movements while recording. Baseline wandering (BW), which contributes to low-frequency-interference, is responsible for distortion of the acquired waveform and poses a challenge in accurate interpretation of the CVDs. In order to minimize the effect of baseline wandering, it is necessary to implement a high-pass filter with high linearity and an accurate cut-off frequency. As per the International Electrotechnical Commission (IEC) standards, the recommended ECG bandwidth extends from 50 mHz to 200 Hz. However, the baseline wander, which could be lying inband at the lower end, may require a higher high-pass cut-

off frequency for its removal [9, 33]. It can be observed in Fig. 3.2a, derived from the MIT-BIH normal sinus rhythm database (Record 17453) [34, 35], that there is a large amount of signal energy around the sub-Hz region. Fig. 3.2b, derived from the MIT-BIH normal sinus rhythm database (Record 16773), shows the effect of baseline wandering resulting from low-frequency interference lying in the sub-Hz region.

With the bandwidth of the ECG signal extending from sub-Hz to 200 Hz [36], a major challenge for an ECG readout system lies in implementing the sub-Hz high-pass cut-off frequency (f_{hpf}) as this translates into the realization of large time constants. To realize large time constants in the order of a few seconds, there exist techniques that employ pseudo-resistors [19–21] or g_m blocks [22] or off-chip solutions such as using an IIR-filter [23] or a resistor [24]. Recently, a new technique to implement large time-constants has been introduced, employing duty-cycled resistors [37]. Although this technique is an attractive alternative, the position of the high-pass pole is still determined by the product of R and C, which is less accurate than a switched capacitor implementation. Moreover, the resistance would occupy a larger area as compared to a small sampling capacitor for the same f_{hpf}. Pseudo-resistors, designed using transistors biased in the cut-off region to obtain extremely large resistances are not very robust to process, voltage, and temperature variations. As these transistors are intrinsically non-linear, the resistances vary with the signal level, eventually leading to clipping at the extremes [38]. As there is quite some energy in the spectrum around the highpass cutoff frequency, a.o., due to baseline wandering, this leads to a reduced dynamic range. Also, as the momentary value of the resistance depends on the momentary value of the input signal, the RC time constant is not fixed. Note, in such a case it would be better to talk about the dynamic eigenvalue of the non-linear differential equation implemented by the pseudo-resistor-capacitor combination. Depending on the choice of the implementation of the resistance, there is a trade-off between the area consumption, linearity around f_{hpf} and the accuracy of f_{hpf}. The existing solutions do not focus on achieving the same linearity around the high-pass cut-off frequency as the rest of the signal band. However, it is an important performance metric in order to acquire a low-distortion bio-signal waveform, especially in the case of cardiac signals aimed at diagnostic monitoring quality. Hence, when better linearity and accuracy are required, alternative techniques need to be developed.

In this section, a synthesis procedure for developing HPΣΔ converters suitable for designing the high-pass filtering analog front-end for ECG signal acquisition is proposed. ΣΔ ADCs take advantage of their noise-shaping property to achieve low quantization noise and the use of a 1-bit digital-to-analog converter (DAC) ensures inherent linearity. As opposed to conventional low-pass ΣΔ converters, a signal transfer that accommodates a general filter transfer is considered. Intermediate transfer function analysis evaluates the signal-handling capabilities and the noise contributions of each of the integrators and thus helps in the overall ranking of the developed HPΣΔ topologies. Sensitivity of the developed HPΣΔ topologies to coefficient variations and non-idealities of the integrator is also investigated.

The rest of the subsections are organized as follows. In Subsection 3.2.1, the methodology to develop HPΣΔ topologies is proposed. The entire design procedure is demonstrated through design examples and compared qualitatively. In Subsection 3.2.2, intermediate functions are derived for quantitative evaluation of the topologies. Further, the sensitiv-



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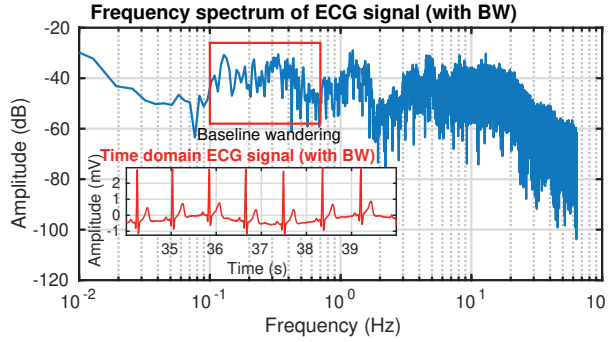


(b)

Figure 3.2: Power spectral density of ECG: (a) Clean ECG; (b) ECG with baseline wandering. (Data courtesy: MIT-BIH database [35])

ity to coefficient variations and integrator non-idealities are described and evaluated in subsection 3.2.3. Circuit design, simulation results and comparison with related prior art are explained in Subsection 3.2.4. Finally, the conclusions are summarized in Subsection 3.2.5.

3.2.1 Proposed methodology

System design incorporating digitization and filtering using an orthogonal design methodology allows us to arrive at topologies satisfying the signal and noise transfer function requirements while optimizing the performance metrics relevant to low-power and low-voltage designs, such as dynamic range and sensitivity to coefficient variations. Conventionally, ΣΔ modulator topologies have a low-pass filter signal transfer characteristic. However, in this approach, to accommodate a general signal transfer function including low-pass, high-pass, notch, and band-pass filter characteristics, state-space forms can be used to design application-specific ΣΔ-modulator topologies. For the target application, viz., acquisition of a cardiac signal whose bandwidth extends from sub-Hz to 200 Hz [36], it is possible to implement the low-pass and the high-pass cut-off frequency separately. Implementing the low-pass cut-off frequency can be readily merged with the front-end

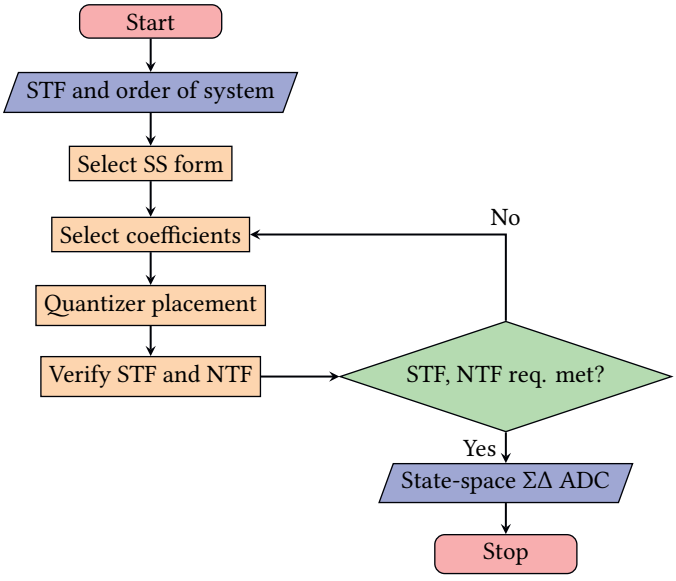


Figure 3.3: Flowchart of the state-space based approach for ΣΔ topologies.

amplifier and can serve as an anti-aliasing filter, and this will not be discussed in this chapter. The high-pass transfer function with good linearity and accuracy is embedded in the ΣΔ converter, thus eliminating the need for a dedicated high-pass filter.

The coefficients are evaluated for their contributions to the signal and noise transfer function requirements for a given state-space form. In this analysis, we have focused only on the inband properties of the modulator. The influence of the sampler on the transfer function in this region is negligible due to the large oversampling ratio (OSR). The placement of the quantizer depends on the requirement of the quantization noise transfer. A single quantizer is considered. Multiple quantizers can also be used and would lead to alternative topologies with different constraints [39], but this is considered beyond the scope of the thesis. For the sake of simplicity and clarity, a 3^{rd}-order system is considered. A first-order high-pass filter is considered sufficient for the application [40]. A higher-order high-pass filter would come at an additional power and area cost. However, the approach can be extended to higher orders per the application specifications. The requirements of the transfer function for a 3^{rd}-order system are:

- Signal transfer function (STF): a high-pass filter characteristic with at least one pole, the location of which can be set independently;
- Noise transfer function (NTF): a high-pass filter characteristic with all real zeros at the origin, leading to a 40 dB/dec slope in the signal band;

Fig. 3.3 shows the design procedure proposed to develop the desired state-space-based high-pass ΣΔ topologies. Based on the resolution and the signal transfer requirements of the target application, the STF type, the order of the system, and the state-space form can be chosen. The coefficients of the state-space forms correspond to physical components

to be realized in silicon that play an essential role in determining the noise, area, and power consumption. The quantizer is placed such that the quantization NTF is satisfied. The STF and NTF of the topologies are verified through transfer function calculations. If the STF and NTF requirements are not met, the coefficients are re-evaluated until all the requirements are satisfied.

A linear, time-invariant dynamic system can be described using a set of first order differential equations. The general state-space description of an n^{th} order system is given by

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t) \\ y(t) &= \mathbf{c}^{\mathbf{T}}\mathbf{x}(t) + du(t) \end{aligned} \tag{3.1}$$

where $\mathbf{x}(t)$ is an n x 1 vector representing the integrator states or outputs, where n is the number of integrators, ideally equal to the order of the system, $\mathbf{A}$ is an n x n state matrix that describes how the integrators are interconnected through feedback and feedforward paths, $\mathbf{b}$ is an n x 1 vector that describes how the input signal is applied to the integrators, $\mathbf{c}$ is an n x 1 vector that contains the set of coefficients that multiply the output states and are summed together and d is a scalar that represents the feedthrough component from the input directly to the output. $u(t)$ and $y(t)$ are the input and the output signal, respectively. To illustrate the design procedure, observable canonical, biquad and orthonormal based HPΣΔ ADC topologies are designed that satisfy the NTF and STF requirements, as described in the following paragraphs.

The observable canonical state-space form [41, 42] is investigated first. The observable canonical state-space form is used to develop the observable canonical ΣΔ topology. The output of the system is fed back to the input of each of the integrators through coefficients that determine the poles of the system. The block diagram and the linear model of the observable canonical HPΣΔ ADC topology are shown in Fig. 3.4. k_1, k_2 and k_3 are the integrator scaling coefficients of the first, second and the high-pass integrator, respectively. The linear model of the quantizer is modeled as a gain k_q, a quantization error $e(s)$, and a summing node. The value of k_q is given by $2/a_N$ where a_N is the coefficient of the last integrator, for a single-bit, N^{th}-order modulator as described in [39]. In the proposed design, a_N is given by the scaling coefficient of the second integrator.

The STF and NTF of the observable canonical HPΣΔ topology can be expressed as

$$\begin{aligned} \mathrm{STF} &= \frac{\mathrm{s}p_1\mathrm{k}_1\mathrm{k}_2\mathrm{k}_\mathrm{q}}{\mathrm{s}^3 + \mathrm{k}_\mathrm{q}\mathrm{k}_2\mathrm{q}_2\mathrm{s}^2 + \mathrm{k}_\mathrm{q}\mathrm{k}_1\mathrm{k}_2\mathrm{q}_1\mathrm{s} + \mathrm{k}_\mathrm{q}\mathrm{k}_1\mathrm{k}_2\mathrm{k}_3\mathrm{q}_0} \\ \mathrm{NTF} &= \frac{\mathrm{s}^3}{\mathrm{s}^3 + \mathrm{k}_\mathrm{q}\mathrm{k}_2\mathrm{q}_2\mathrm{s}^2 + \mathrm{k}_\mathrm{q}\mathrm{k}_1\mathrm{k}_2\mathrm{q}_1\mathrm{s} + \mathrm{k}_\mathrm{q}\mathrm{k}_1\mathrm{k}_2\mathrm{k}_3\mathrm{q}_0} \end{aligned} \tag{3.2}$$

From (3.2), it can be seen that the STF and NTF requirements of the observable ΣΔ topology are met. For the STF, there is at least one zero at DC (single-pole roll-off), and the three zeros at DC for the NTF. On solving the characteristic equation (CE) of (3.2), given by

$$s^3 + k_\mathrm{q}k_2q_2s^2 + k_\mathrm{q}k_1k_2q_1s + k_\mathrm{q}k_1k_2k_3q_0 = 0, \tag{3.3}$$

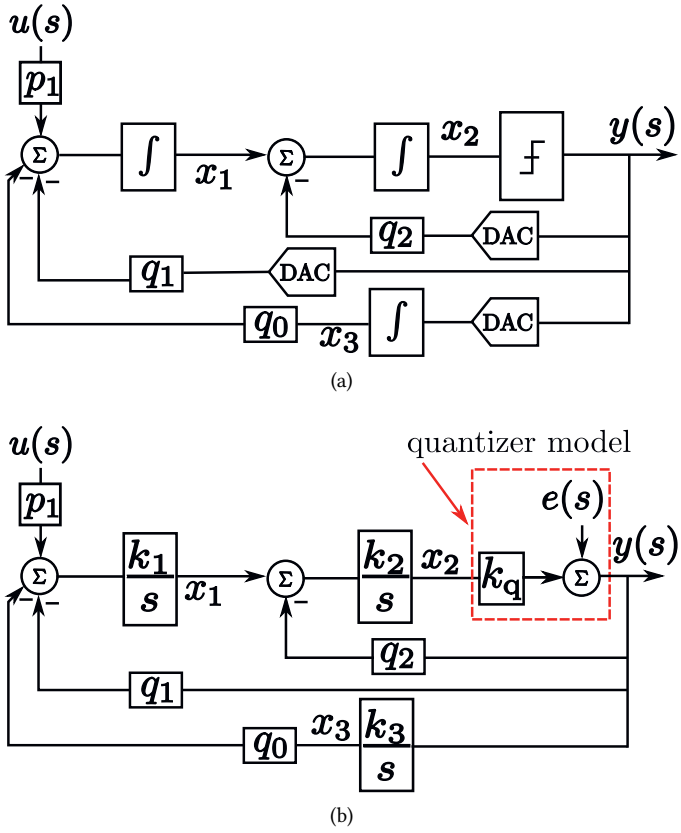
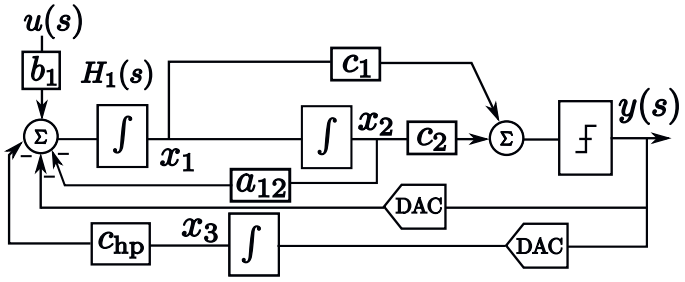


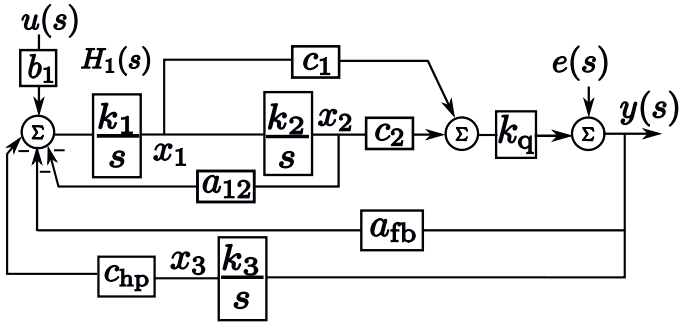
Figure 3.4: 3rd-order observable canonical HPΣΔ topology: (a) Block diagram; (b) Linear model.

Table 3.1: State-space based HPΣΔ topologies: A qualitative comparison

SS topology	Biquad HPΣΔ	Observable canonical HPΣΔ	Orthonormal HPΣΔ
Disadvantage	Biquads in cascade can be used to realize higher order structures but may require modification for stability.	The output is fed back to the input of each of the integrators which imposes tough swing requirements on the integrator.	Existing orthonormal state-space form has to be modified in order to satisfy the STF requirement.
Advantage	Each biquad can be tuned independently while imposing relaxed swing requirements on the integrators.	Only real NTF zeros can be produced while the rest of the topologies can produce real and/or complex zeros.	Unique set of coefficients can be derived for any given stable transfer function. The calculation of the coefficients can be automated.



(a)



(b)

Figure 3.5: 3rd-order biquad HPΣΔ topology: (a) Block diagram; (b) Linear model.

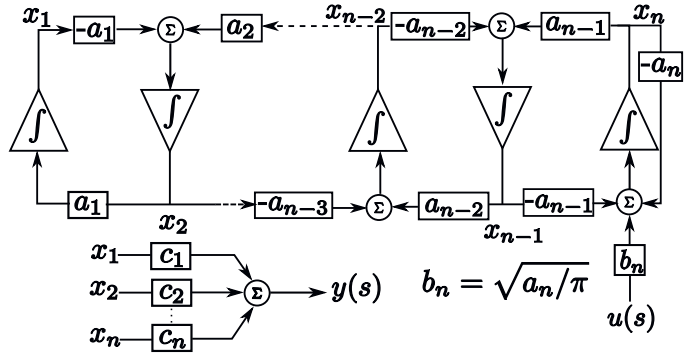
the location of the high-pass pole close to DC can be determined. The location of the pole predominantly depends on the value of q_0, q_1 and k_3.

Figures 3.5a and 3.5b show the biquad HPΣΔ ADC and its linear model, respectively. The STF and the quantization NTF of the biquad HPΣΔ ADC can be written as

$$\begin{aligned} \text{STF} &= \frac{\mathrm{s b_1 k_1 k_q (c_1 s + k_2 c_2)}}{\mathrm{s^3 + a_{12} k_1 k_2 s + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})}} \\ \text{NTF} &= \frac{\mathrm{s(s^2 + a_{12} k_1 k_2)}}{\mathrm{s^3 + a_{12} k_1 k_2 s + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})}} \end{aligned} \tag{3.4}$$

As can be seen from (3.4), the STF and the NTF satisfy the requirements.

Orthonormal ladder filters [43], a state-space structure that is scaled for optimum dynamic range and less sensitive to component variations, can be used for realizing higher-order arbitrary stable transfer functions [44]. Figures 3.6a, 3.6b and 3.6c show the generalized state-space form, the HPΣΔ topology and the corresponding linear model of an example 3rd-order orthonormal HPΣΔ ADC. k_1, k_2, and k_3 are the integrator scaling coefficients of the first, second, and high-pass integrators, respectively. Also, a_1 is replaced by k_2. The STF and the NTF equations of the orthonormal ΣΔ topology can be written as



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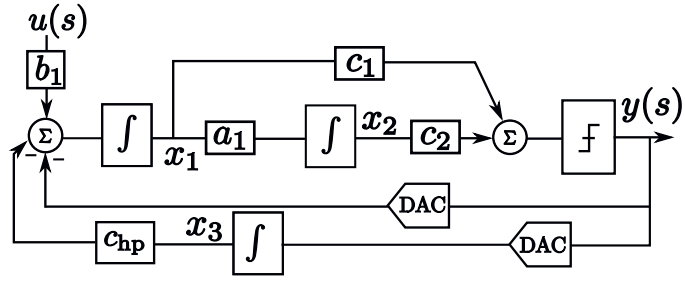

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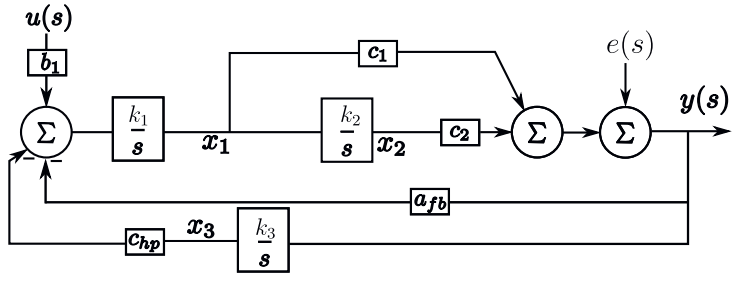


(c)

Figure 3.6: (a) is an n[th] - order orthonormal filter topology; (b) 3[rd]-order orthonormal HPΣΔ topology; (c) and its linear model.

Table 3.2: Coefficients of the HPΣΔ topologies

Coeff.	Orthonormal HPΣΔ	Coeff.	Observable canonical HPΣΔ
b_1	0.5	p_1	0.5
k_1, k_2	0.5	k_1, k_2	0.5
a_{fb}, c_{hp}	1	q_1	0.5
c_1, c_2	0.5	q_2, q_0	1
k_3	0.001	k_3	0.001

$$\begin{aligned} \mathrm{STF} &= \frac{\mathrm{s b_1 k_1 k_q (c_1 s + k_2 c_2)}}{\mathrm{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})}} \\ \mathrm{NTF} &= \frac{\mathrm{s^3}}{\mathrm{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})}} \end{aligned} \tag{3.5}$$

From (3.5), it can be seen that the STF has one zero at the origin. Also, the NTF has three zeros at the origin. The poles can be determined by solving the characteristic equation given by

$$s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp}) = 0 \tag{3.6}$$

For frequencies very close to DC, the characteristic equation can be approximated as

$$s \approx -\frac{c_{hp} k_3}{a_{fb}} \Longrightarrow f_{hpf} = \frac{1}{2\pi} \frac{c_{hp} k_3}{a_{fb}} f_s \tag{3.7}$$

and the high-pass pole location can be set. Note that the quantizer gain k_q does not impact the location of the pole. This implies that the signal-dependent gain associated with k_q and thus the momentary value of the input signal of the ADC does not change the exact value of the location of the pole, unlike in the case of pseudo-resistors.
For the orthonormal HPΣΔ topology, the equations can be written as:

$$\left[u(s) b_1 - a_{fb} y(s) - c_{hp} x_3(s)\right] \frac{k_1}{s} = x_1(s), \tag{3.8}$$

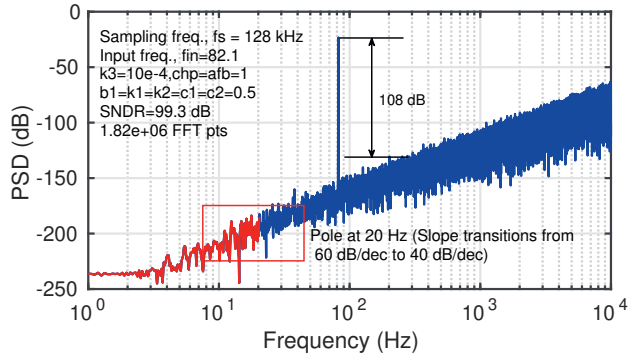
$$x_1(s) \frac{k_2}{s} = x_2(s), \tag{3.9}$$

$$\frac{k_3}{s} y(s) = x_3(s), \tag{3.10}$$

and

$$\left[x_1(s) c_1 + x_2(s) c_2\right] k_q + e(s) = y(s), \tag{3.11}$$

where $u(s)$ and $y(s)$ are the input and the output of the system, respectively, and $x_1(s)$, $x_2(s)$ and $x_3(s)$ are the integrator outputs of the first, second and the high-pass integrator,



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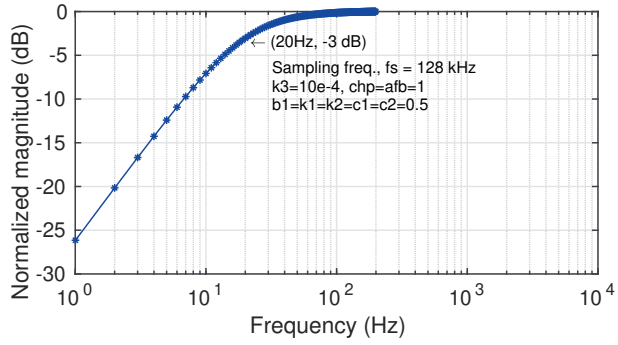


(b)

Figure 3.7: System level plots of the 3rd-order orthonormal HPΣΔ topology: (a) NTF, (b) STF.

respectively. After solving the algebraic equations, we obtain the signal transfer function and the quantization noise transfer function given by

$$\mathrm{STF} = \frac{k_1 b_1 s(c_1 s + k_2 c_2) k_q}{s^3 + k_q k_1 (s^2 c_1 a_{fb} + s(k_2 c_2 a_{fb} + k_3 c_{hp} c_1) + k_2 k_3 c_2 c_{hp})}, \tag{3.12}$$

and

$$\mathrm{NTF} = \frac{s^3}{s^3 + k_q k_1 (s^2 c_1 a_{fb} + s(k_2 c_2 a_{fb} + k_3 c_{hp} c_1) + k_2 k_3 c_2 c_{hp})} \tag{3.13}$$

respectively. The poles can be determined by solving the characteristic equation given by

$$s^3 + k_q k_1 \left[s^2 c_1 a_{fb} + s(k_2 c_2 a_{fb} + k_3 c_{hp} c_1) + k_2 k_3 c_2 c_{hp} \right] = 0 \tag{3.14}$$

Solving a cubic equation is non-trivial and to calculate the pole located very close to DC, (3.14) can be approximated to a 2^{nd}-order equation and can be written as

$$k_q k_1 \left[s^2 c_1 a_{fb} + s(k_2 c_2 a_{fb} + k_3 c_{hp} c_1) + k_2 k_3 c_2 c_{hp} \right] = 0 \tag{3.15}$$

or a 1^{st}-order equation given by

$$k_q k_1 \left[s(k_2 c_2 a_{fb} + k_3 c_{hp} c_1) + k_2 k_3 c_2 c_{hp} \right] = 0 \tag{3.16}$$

Assuming that k_3 is very small, the associated term can be made zero. 3.16 can be written as

$$s \approx -\frac{c_{hp} k_3}{a_{fb}}, \tag{3.17}$$

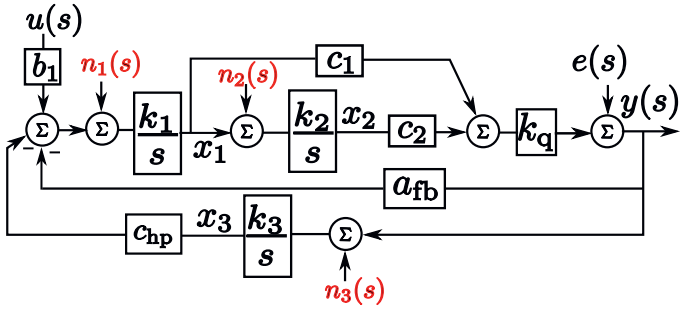
which defines the location of the high-pass pole.

Figures 3.7a and 3.7b show the plots of NTF and STF of the orthonormal HPΣΔ topology, respectively. Sampling frequency f_s = 128 kHz, scaling coefficient k_3 = 0.001 and a_{fb} = 1 result in an high-pass cut-off frequency f_{hpf} of 20 Hz, selected to observe the slope change clearly. A desired f_{hpf} can be selected by appropriately setting k_3.

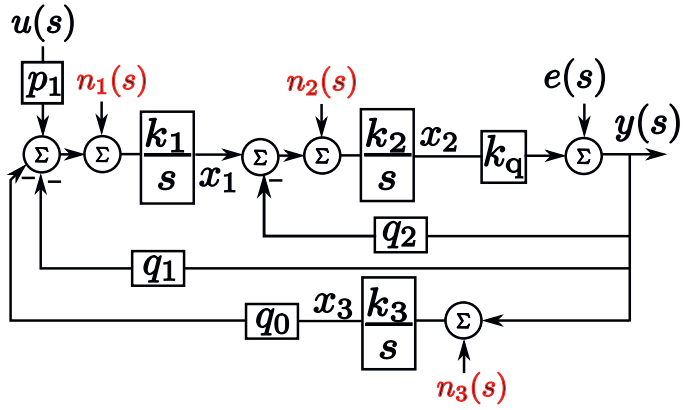
Table 3.1 summarizes the advantages and disadvantages posed by the various HPΣΔ topologies. While biquads can be tuned independently, they may be unstable at higher orders and require modifications to stabilize the system. For this reason, we will discuss only the orthonormal and observable canonical HPΣΔ topologies in the sequel.

3.2.2 Intermediate functions

In this section, the sets of intermediate transfer functions (IF) [43] are derived to compare the thermal noise contributions and internal states magnitudes of the integrators of the HPΣΔ topologies. Flicker noise is not considered here since circuit techniques to reduce its effect can be found in the literature, and the reader is referred to [45] and [46] for more details. Although both thermal and flicker noise contribute to the total noise of the system, they are minimized through independent circuit techniques. The first set of intermediate functions, from the input of the integrators to the output of the system, **g**(s), and the second set, from the input of the system to the output of the integrators, **f**(s), as shown in Fig. 3.9, can be expressed as



(a)



(b)

Figure 3.8: Integrator input referred thermal noise sources: (a) Orthonormal HPΣΔ; (b) Observable canonical HPΣΔ topology.

$$f_i(s) \triangleq \frac{x_i(s)}{u(s)}; \qquad g_i(s) \triangleq \frac{y(s)}{n_i(s)}; \tag{3.18}$$

where $u(s)$ and $y(s)$ denote the input and the output of the system, and $n_i(s)$ and $x_i(s)$ represent the input thermal noise source and output of the i^{th} integrator, respectively.

The IF $\mathbf{f}(s)$ of the orthonormal HPΣΔ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by:

$$f_1(s) = \frac{b_1 k_1 s^2}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + + k_2 k_3 c_2 c_{hp})} \tag{3.19}$$

$$f_2(s) = \frac{b_1 k_1 k_2 s}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{3.20}$$

$$f_3(s) = \frac{b_1 k_1 k_3 k_q (s c_1 + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{3.21}$$

The IF **g**(s) of the orthonormal HPΣΔ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by:

$$g_1(s) = \frac{k_1 k_q s(c_1 s + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{3.22}$$

$$g_2(s) = \frac{k_2 k_q c_2 s^2}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{3.23}$$

$$g_3(s) = \frac{k_1 k_3 k_q c_{hp} (s c_1 + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{3.24}$$

The IF **f**(s) of the observable canonical HPΣΔ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by:

$$f_1(s) = \frac{s p_1 k_1 (s + k_2 q_2 k_q)}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.25}$$

$$f_2(s) = \frac{s p_1 k_1 k_2}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.26}$$

$$f_3(s) = \frac{p_1 k_1 k_2 k_3 k_q}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.27}$$

The IFs **g**(s) of the observable canonical HPΣΔ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by:

$$g_1(s) = \frac{k_1 k_2 k_q s}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.28}$$

$$g_2(s) = \frac{k_2 k_q s^2}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.29}$$

$$g_3(s) = \frac{k_1 k_2 k_3 k_q q_0}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{3.30}$$

From Fig. 3.9, we can observe that the noise from the first, second and third integrator in the orthonormal HPΣΔ modulator is first-order high-pass, second-order high-pass and low-pass filtered, respectively. It can be observed that the input signal is high-pass filtered with a slope of 20 dB/dec, while the quantization noise initially begins with a slope of 60 dB/dec but transitions to 40 dB/dec on encountering the pole associated with the high-pass cut-off frequency. Similar frequency response trends as shown in Fig 3.9 are also obtained for observable HPΣΔ modulator. The coefficients of both topologies are given in Table 3.2.

To quantitatively evaluate the performance of the HPΣΔ topologies, a mathematical norm is necessary to measure the magnitudes of the signal level. The two signal types that are often used in such a performance analysis are:

- A sinusoidal input: for a sinusoidal input with a peak amplitude A_p, an appropriate mathematical norm of the signal is the L_∞ norm.

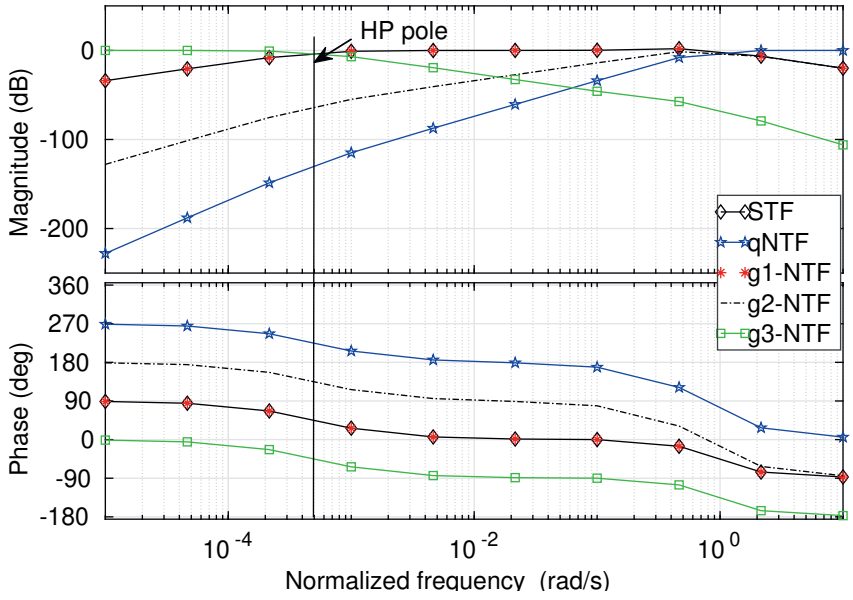


Figure 3.9: Frequency response of the signal transfer function (STF), the quantization noise transfer function (qNTF) and the 3 intermediate noise transfer functions g_1, g_2 and g_3 of the orthonormal HPΣΔ topology.

Table 3.3: L_2-norm calculations of the HPΣΔ topologies

Int.	Before scaling $\|f_i\|_2$	Before scaling $\|g_i\|_2$	Factor α_i	After scaling $\|f_i\|_2$	After scaling $\|g_i\|_2$
Orthonormal HPΣΔ					
First integrator	0.354	0.866	2.8277	1	0.3063
Second integrator	0.25	0.7073	4.001	1	0.1768
High-pass integrator	0.0158	0.0158	63.23	1	0.00025
$\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$	1.2506			0.12506	
Observable canonical HPΣΔ					
First integrator	0.7501	0.707	1.33	1	0.5304
Second integrator	0.177	1.00	5.66	1	0.1768
High-pass integrator	0.0158	0.0158	63.238	1	0.00025
$\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$	1.5006			0.31266	

- A power spectrum: if the input signal is assumed to be white, i.e., have a constant power spectral density, the output power spectrum at the output of the integrators is calculated and the root-mean-square value is given by the L_2 norm of the signal.

The L_2-norm of signal $v(t)$ is given by,

$$\|v\|_2 = \left(\int_0^\infty v(t)^2 dt \right)^{\frac{1}{2}} \tag{3.31}$$

The dynamic range, given by the ratio of the maximum signal handling capability and the minimum level as determined by the internally generated noise, can be optimized through scaling of the integrators. Integrator scaling is the process of readjusting the internal gain coefficients in order to adjust the internal signal swing to a range appropriate for the supply voltage such that the overall transfer function from the input to the output remains unchanged [47]. The L_2-norms of the set of IF's **f**(s) and **g**(s) are calculated and are tabulated in Table 3.3. A scaling factor, α_i, is calculated for each integrator, given by

$$\alpha_i = \frac{M}{\|f_i\|_2}, \tag{3.32}$$

where M is the maximum acceptable signal magnitude at the integrator outputs. After **f**(s) has been scaled, **g**(s) is scaled by the inverse factor $(\frac{1}{\alpha_i})$ as given in Table 3.3. The total noise power of the integrators, given by $\sum_i \|g(j\omega)\|_2^2$, can be evaluated and used as a figure of merit [5] for comparing the noise performance of the HPΣΔ topologies. The total noise power for a 3$^{\text{rd}}$-order system, given by $\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$ for the orthonormal HPΣΔ is 0.12,

which is smaller than that of the observable HPΣΔ, which is 0.31, which is a significant 3.9 dB difference. Therefore, the orthonormal HPΣΔ is a preferred choice for circuit implementation. The noise performance of the HPΣΔ topologies can be further improved by balancing the integrator noise contributions, i.e., making g_i of the integrators equal. This can be carried out by appropriate capacitance sizing of the integrators while keeping in mind the practical tradeoffs between noise and current consumption. The noise contributions of individual integrators can be seen in Table 3.3. It can be observed that the total noise contribution of the observable canonical HPΣΔ ADC is about 1.25 times that of the orthonormal HPΣΔ ADC before scaling, while it is three times that after scaling. Therefore, the orthonormal HPΣΔ ADC is a better topology with respect to noise performance.

Following the intermediate function analysis from a linearized model, the topologies are compared using a non-linear model of the HPΣΔ topologies, which models the quantizer as a *sign* function on MATLAB. Fig. 3.10 shows the dynamic range comparison between the observable canonical and orthonormal HPΣΔ topologies. It can be observed that the orthonormal HPΣΔ topology has a larger dynamic range and can handle larger input signal amplitudes.

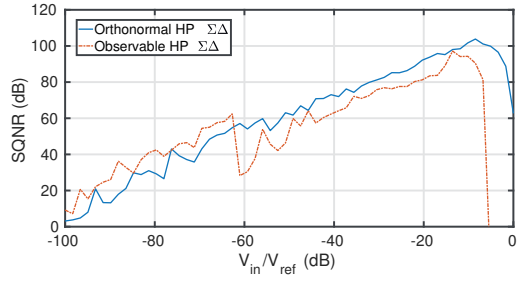


Figure 3.10: Simulated dynamic range performance of the HPΣΔ topologies

From system simulations, it follows that the difference between the noise performance of these types of modulators becomes more pronounced for higher orders, in favor of the orthonormal HPΣΔ modulator topology.

3.2.3 Sensitivity

In this section, the sensitivity of the transfer function to integrator non-idealities and coefficient variations is discussed. In order to determine the impact of integrator errors on the transfer function of the HPΣΔ topologies, the integrator errors are modeled and simulated at the system level. The effects of finite DC gain, finite GBW and time-constant variation of the integrators on the performance of the system are investigated. Assuming an RC implementation, the ideal integrator transfer function (ITF) can be expressed as

$$ITF_{RC,i} = \frac{k_i f_s}{s} = \frac{1}{sRC} = \frac{\omega_u}{s} \tag{3.33}$$

Taking the finite DC gain effect of the integrator into account, the non-ideal integrator transfer function can be expressed as

$$ITF_{A_0,i} \approx \frac{k_i f_s}{s + \frac{k_i f_s}{A_0}}, \tag{3.34}$$

where A_0 is the finite DC gain of the integrator. Comparing (3.34) to the ideal ITF expressed in (3.33), it is observed that the pole is displaced from the origin to $\frac{k_i f_s}{A_0}$.

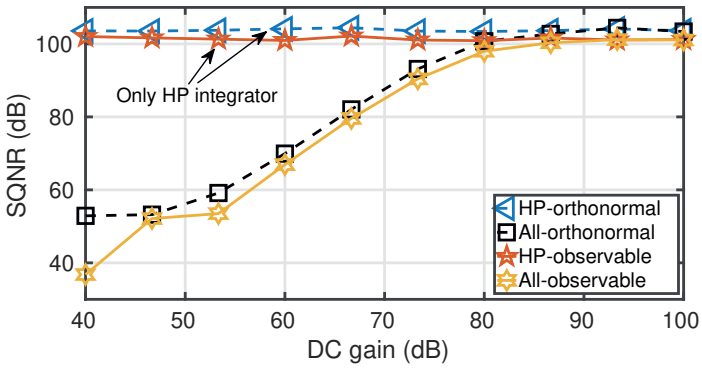


Figure 3.11: Effect of finite DC gain on the performance of the HPΣΔ topologies

Fig. 3.11 shows the impact of finite DC gain of the high-pass integrators and compares the signal-to-quantization-noise ratio (SQNR) performance between orthonormal and observable canonical HPΣΔ ADC topologies. It can be observed that, on lowering the DC gain of the high-pass integrator alone, the performance of the topologies does not degrade. The overall performance of the topologies mainly depend on the first or the second integrator.

The non-ideal ITF due to finite GBW can be expressed as [39]

$$ITF_{\mathrm{GBW,i}} = \frac{\frac{k_i f_s}{s}\frac{GBW}{GBW+k_i f_s}}{1+\frac{s}{GBW+k_i f_s}}, \tag{3.35}$$

where GBW is the gain-bandwidth product of the integrator.

From Fig. 3.12, one can observe how the performance of the HPΣΔ topologies depend on the GBW of the integrators. As the GBW product of the high-pass integrator decreases, the performance of the modulator degrades only marginally. At the lower end, the GBW values of the 1st and 2nd integrator are important to maintain the performance of the HPΣΔ topologies. To minimize the effect of finite GBW, a GBW value of $0.7 \cdot f_s$ or higher would suffice.

The non-ideal ITF due to RC mismatch can be expressed as

$$ITF_{RC,\Delta_{RC}} = \frac{1}{sRC} \cdot \frac{1}{(1+\Delta_{RC})} = \frac{k_i f_s}{s} \cdot \frac{1}{(1+\Delta_{RC})} \tag{3.36}$$

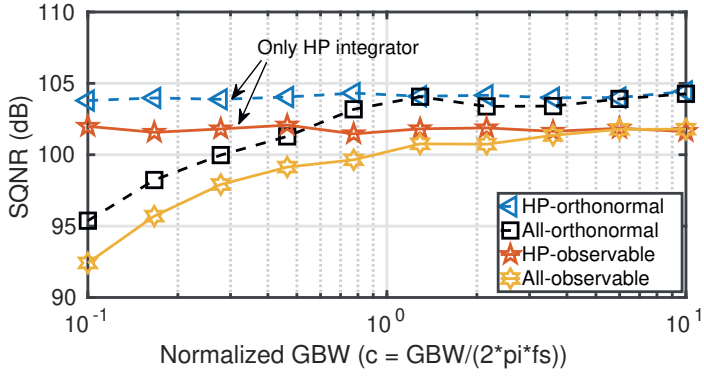


Figure 3.12: Effect of finite GBW on the performance of the HPΣΔ topologies

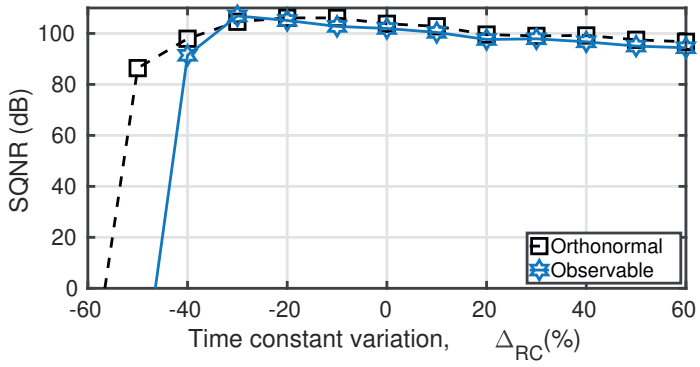


Figure 3.13: Effect of time constant variation on the performance of the HPΣΔ topologies.

When the time constant increases, i.e., the gain of the integrator decreases, the performance of the HPΣΔ topologies degrades. The trend is similar to the effect of finite GBW on the performance. When the time constant decreases, i.e., the gain of the integrator increases, the modulator can become unstable beyond a threshold, as can be seen in Fig. 3.13. The overall performance of the high-pass modulator mainly depends on the first or the second integrator and not on the feedback integrator.

In the case of filters, the sensitivity of the transfer function to the integrator non-idealities is dependent on the integrator time constant [43]. A higher integrator gain would result in larger sensitivity to the integrator non-idealities. Given that the gain of the integrator is proportional to the row sum given by [43]

$$|A_{ij}| + |b_i|, \tag{3.37}$$

where A_{ij} and b_i are elements of the **A** and **b** matrices, respectively, the first and second integrator are expected to be more sensitive to the integrator non-idealities than the high-pass integrator, which confirms the observations made in Figures 3.11, 3.12 and 3.13. The

row sum of the high-pass integrator is very low; therefore, the sensitivity to finite DC gain, finite GBW, and time-constant variation is marginal. However, the row sums of the first and second integrators are quite large compared to those of the high-pass integrator, and hence, they suffer from larger sensitivities to integrator non-idealities. In general, the larger the row sum of the integrator, the larger the sensitivity to its non-idealities. We can conclude that the orthonormal HPΣΔ modulator is always less sensitive to the above non-idealities than the observable HPΣΔ modulator. For this reason, orthonormal HPΣΔ architecture is chosen for circuit implementation.

3.2.4 Circuit implementation and simulation results

Illustrated in Fig. 3.14 is the top-level schematic of the proposed orthonormal HPΣΔ topology targeting the implementation of the high-pass cut-off frequency with good accuracy and linearity. Opamp-RC integrators are used to realize the first and second integrators to achieve good linearity. The amplifiers are designed using a two-stage opamp topology for the high current driving capability required to drive the large capacitances, minimizing the performance degradation due to slewing. A multiple-input dynamic comparator is used to realize the summer and the quantizer. A very large time-constant, parasitic-insensitive, and area-efficient switched-capacitor Nagaraj integrator [48] as shown in Fig. 3.15 is used to implement the high-pass integrator in the feedback loop. The location of the high-pass pole is determined by ratios of capacitors and by the clock frequency and, as such, offers high accuracy and is robust to PVT variations. c_{hp} and a_{fb} are implemented as a ratio of resistors, while k_3 is implemented as a ratio of capacitors, both of which can be very accurate. The circuit consists of three different capacitors and operates in two non-overlapping phases. The input voltage is attenuated and integrated by capacitor C_{I}. A charge equivalent to $C_{\mathrm{a}}V_{\mathrm{in}}$ is transferred to the large capacitor C_{I} during the first phase. In the second phase, the charge is redistributed between C_{I} and C_{b}. Large capacitance C_{I} is used for attenuation and integration, thus saving area. The gain and the unity gain frequency, f_u of the integrator are given by the factor $(\frac{C_{\mathrm{a}}}{C_{\mathrm{I}}})(\frac{C_{\mathrm{b}}}{C_{\mathrm{I}}})$ and

$$f_{\mathrm{u}} = \frac{1}{2\pi}\frac{1}{\left[1+\frac{C_{\mathrm{b}}}{C_{\mathrm{I}}}\right]}\frac{C_{\mathrm{a}}}{C_{\mathrm{I}}}\frac{C_{\mathrm{b}}}{C_{\mathrm{I}}}f_{\mathrm{s}}, \tag{3.38}$$

respectively, where f_{s} is the clock frequency and is equal to the sampling frequency of the ΣΔ modulator.

To avoid long simulation times, f_{hpf} is set at 1 Hz, and the circuit is tested for linearity at the same frequency. Lower f_{hpf} can be realized by appropriately selecting the values of capacitances and the clock frequency at the cost of larger area and power. To obtain a cut-off frequency of 1 Hz, C_{a} = 0.5 pF, C_{I} = 45 pF and C_{b} = 0.2 pF are chosen to realize the scaling coefficient of $5{\cdot}10^{-5}$ that follows from (3.7) and (3.38). In the designed modulator, the high-pass cut-off frequency is implemented using ratios of capacitors, which is more accurate and robust to PVT variations than pseudo-resistors or g_m based techniques. The first, the high-pass, and the second integrator consume 76.6, 65.4, and 3.7 μW, respectively, while the digital blocks consume 0.4 μW. To get an estimate of the noise contributions of the passive components, the thermal noise of the opamps, and the quantization noise, a transient noise simulation is run with noise f_{min} and f_{max} being 1 Hz and 200 Hz respec-

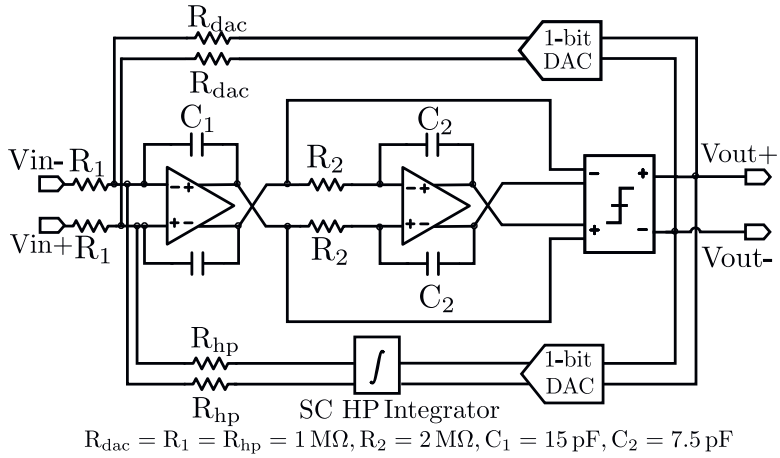


Figure 3.14: Top level circuit block diagram of the CT orthonormal HPΣΔ modulator [31]

Table 3.4: Performance of the CMOS orthonormal HPΣΔ modulator

Technology	0.18 μm AMS
Supply voltage	1.8 V
Sampling frequency	128 kHz
Signal Bandwidth	1 - 200 Hz
HD_3@f_{in}=1.1 Hz,V_{in} = 100 mVp	-78 dB
SNDR[1]	68.1 dB
ENOB	11.02 bits
Total capacitance	148.4 pF
Total power consumption	146μW

[1] Transient thermal noise from noise $f_{min} = 1$ to $f_{max} = 200$ Hz; flicker noise disabled

tively, after disabling the effect of flicker noise, and is shown in Figure 3.16. Assuming that the flicker noise of the opamps can be optimized with available state-of-the-art circuit techniques, the signal energy at the high-pass cut-off frequency region can be acquired with high fidelity. The 3rd harmonic distortion is at -78 dB for an input signal of 100 mV (peak value) at an input frequency of 1.1 Hz, as shown in Figure 3.16b, which is better than the state-of-the-art performance. Designed and simulated in AMS 0.18 μm CMOS IC technology and taking resistor noise, switched capacitor noise, opamp thermal noise, quantization noise, and harmonic distortion into account, the orthonormal HPΣΔ ADC achieves an effective number of bits (ENOB) of 11.02 bits. Table 3.10 summarizes the performance of the designed modulator.

The proposed implementation of the high-pass cut-off frequency is compared with that of a "Harrison amplifier," i.e., the combination of an amplifier and a high-pass filter, as shown in Fig. 3.15 [19]. Figures 3.16 and 3.17 show the performance of the orthonormal HPΣΔ modulator and the Harrison amplifier, respectively. The proposed design is benchmarked against a Harrison amplifier that consists of pseudoresistors designed using PMOS transistors [19] and an ideal amplifier. The high-pass filter is implemented using the pseudoresistors in parallel with the feedback capacitors C_B. The linearity at the high-

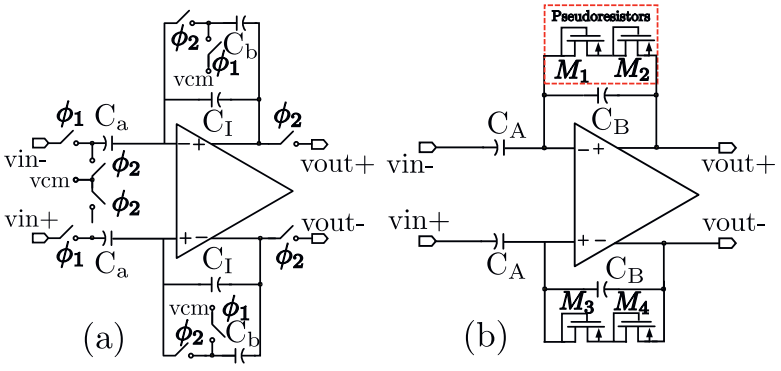


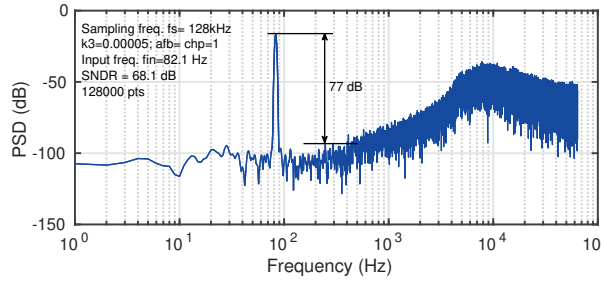
Figure 3.15: Implementation of the high-pass cut-off frequency a) SC Nagaraj integrator [48] b) Harrison amplifier [19]

pass cut-off frequency of the Harrison amplifier is tested and is shown in Fig. 3.17. The amplifier achieves an HD_3 of about -40 dB for an input amplitude of 10 mV at an input frequency of 1.1 Hz. The relative accuracy of the unity gain frequency of the SC integrator is better than 0.1%. Together with the inaccuracies resulting from the ratio of resistances, the accuracy of the proposed method can be better than 1%. Monte Carlo simulations, accounting for process and mismatch variations, comparing the accuracies of the high-pass cut-off frequency set by the SC Nagaraj integrator and the Harrison amplifier, are shown in Figure 3.18.

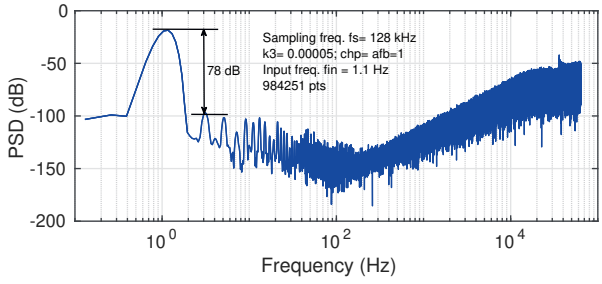
Testing with pre-recorded ECG signal

The orthonormal HPΣΔ modulator is tested with a pre-recorded ECG signal from the MIT-BIH Normal Sinus Rythym database (nsrdb [49]) numbered as Record 16773 (Signal: ECG1). The designed system is run with 3 seconds of the ECG input signal to observe the effect of baseline wandering and the output is post-processed in MATLAB. The acquired digital signal output is low-pass filtered using a third-order Butter-worth filter and is reconstructed in the analog time domain. Fig. 3.19 shows the pre-recorded time-domain ECG input signal, the reconstructed signal from the output of the orthonormal HPΣΔ modulator and the signal from the output of the Harrison amplifier, which are benchmarked against a MATLAB high-pass filtered signal of the raw ECG with BW. The distortion components present in the ECG signal acquired using pseudoresistors (with an ideal amplifier having no swing limitations) can be clearly seen in the time-domain. Distortion around the high-pass cut-off frequency of ECG signal can make accurate medical diagnosis a challenge. However, the waveform acquired by the orthonormal HPΣΔ modulator has much better linearity and is closer to the MATLAB filtered waveform.

Given that the signal is normal sinus rhythm and assuming that the strength of the beat is fairly uniform, the R-R interval is about 0.8 sec and the amplitude of the P-wave peak of the input ECG signal ranges from -0.054 to 0.058 mV, whereas, the reconstructed ECG peaks vary from 0 to 0.048 mV, which is a much smaller range. The occurrence of the P-wave peak for the input ECG with baseline wander and the reconstructed ECG are tabulated in Table 3.6. It can be observed that the effect of baseline wandering is greatly



(a)



(b)

Figure 3.16: Orthonormal HPΣΔ circuit simulations: (a) Output spectrum for f_{in} = 82.1 Hz, (b) Output spectrum for f_{in} = 1.1 Hz.

Table 3.5: Comparison of the implementation of high-pass cut-off frequency (f_{hpf}) with related work

	This work	[Mohan]	[Harrison]	[Muller]	[Rezaee]
Year	2017	ISCAS 2013 [22]	JSSC 2003 [19]	JSSC 2012 [23]	JETCAS 2011[20]
Architecture	2^{nd} HPΣΔ	1^{st} HPΣΔ	amplifier	boxcar ADC	amplifier
Domain	mixed-signal	mixed-signal	analog	digital	analog
Bio-signal	ECG	ECG	neural	neural	neural
HPF technique	SC Nagaraj integrator	g_{m}, current sources	pseudoresistors	IIR-filter (off-chip)	pseudoresistors
Bandwidth [Hz]	1-200	1-200	0.025-7.2k	300-10k	0.5-10k
HD_3 [dB]	-78 @f_{in} = 1.1 Hz	-62 @f_{in} = 2.1 Hz	>-40 @f_{in} = 1.1 Hz	-	>-40 @f_{in} = 1.1 Hz
Accuracy of f_{hpf}	high	process sensitive	process sensitive	very high	process sensitive
Technology	0.18 μm	0.18 μm	1.5 μm	65 nm	0.18 μm

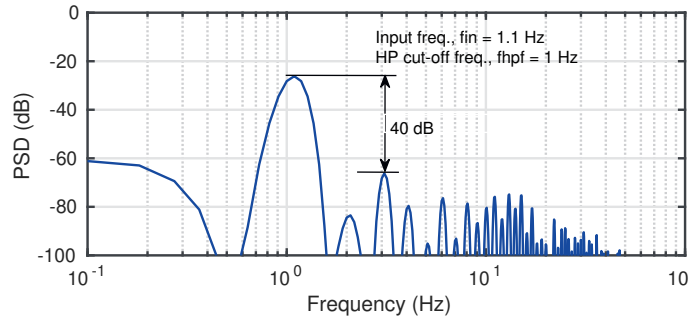
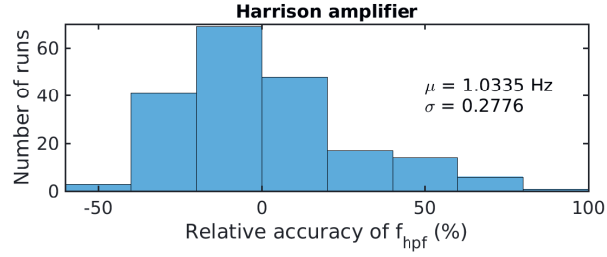
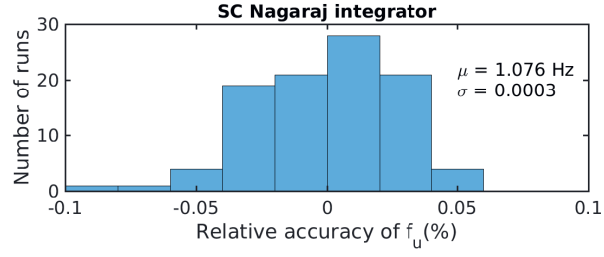


Figure 3.17: Output spectrum of Harrison amplifier for f_{in}= 1.1 Hz



(a)



(b)

Figure 3.18: Histogram of the relative accuracies of the high-pass cut-off frequency: (a) Harrison amplifier, (b) SC Nagaraj integrator

reduced in the reconstructed signal.

Comparison with related work

Comparing the performance of the orthonormal HPΣΔ modulator to the Harrison amplifier, it can be seen that the orthonormal HPΣΔ topology offers a much better alternative for the implementation of the high-pass cut-off frequency, in terms of linearity and accuracy. Pseudoresistors are used in [19] and [20] for lower area and power consumption at the expense of poor linearity and accuracy of the high-pass cut-off frequency. Due to process (P), voltage (V), and temperature (T) variations and poor circuit structures, pseudoresistors achieve a linearity of about -40 dB and compromise the accuracy of the implementation

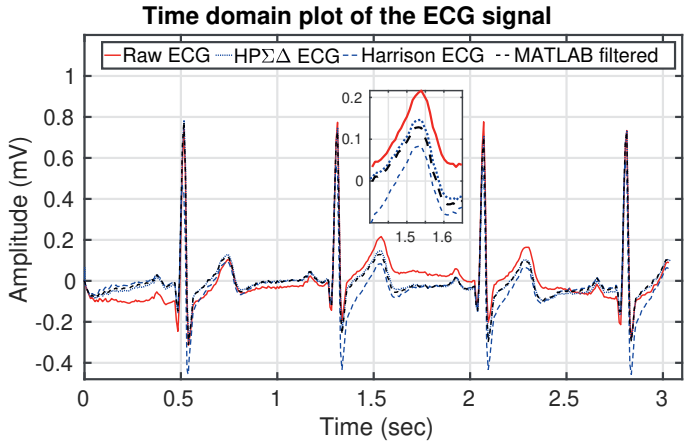


Figure 3.19: Time-domain ECG signal from the orthonormal HPΣΔ modulator output compared with raw ECG (MIT-BIH), Harrison amplifier and MATLAB filtered output

Table 3.6: Reduction of baseline wandering

ECG P-wave	1^{st} (s, mV)	2^{nd} (s, mV)	3^{rd} (s, mV)	4^{th} (s, mV)
Raw ECG	(0.37, -0.054)	(1.17, 0.024)	(1.93, 0.058)	(2.65, -0.015)
Rec. ECG	(0.38, 0.015)	(1.17, 0.048)	(1.93, 0.012)	(2.66, 0)

of the high-pass cut-off frequency. Although the use of a g_m stage in combination with current sources [22] leads to a power-efficient solution, the g_m of any transistor is inherently non-linear and is less robust to P, V, and T variations. Off-chip digital solutions [23] can be used to obtain a highly accurate and linear high-pass cut-off frequency at the expense of power. Table 3.5 summarizes the metrics that characterize the implementation of a high-pass cut-off frequency involving large time constants. For integrated on-chip solutions, the proposed system is among the most promising approaches for applications where good linearity and accuracy of the high-pass cut-off frequency are desired.

3.2.5 Conclusions on the proposed state-space methodology

This chapter proposes a state-space-based design methodology to develop HPΣΔ ADC topologies. By using the state-space synthesis approach, ΣΔ converters with arbitrary signal and quantization noise transfer functions can be synthesized. State-space techniques allow dynamic range optimization of the ΣΔ converters with respect to signal swing and noise through state and noise scaling, respectively. This also minimizes the sensitivity of the topology to component variations [50]. From the intermediate-function analysis, it is seen that the noise from the high-pass integrator is low-pass filtered. Also, the L_2-norm calculations show that the orthonormal HPΣΔ ADC gives better noise performance than the observable HPΣΔ ADC. Sensitivity analysis is carried out to investigate the impact of coefficient variations and non-idealities of the integrator. Finally, schematic simulations of a circuit designed in AMS 0.18 μm CMOS IC technology verify the findings and

match the system-level results. The designed orthonormal HPΣΔ is also tested with a real pre-recorded ECG input signal and successfully reduces baseline wandering.

3.3 A single-channel integrated circuit for acquiring cardiac signals using an orthonormal ΣΔ ADC

3.3.1 Introduction

Recordings of cardiac signals, both electrocardiograms (ECG) and atrial electrograms (AEG) provide insights into the functioning of the heart. To diagnose cardiac abnormalities, the ECG is non-invasively recorded on the surface of the heart. Specific features of the ECG waveform reveal the state of normalcy or abnormalcy pointing to the corresponding location in the heart. In addition to this, to obtain a deeper understanding of the progression of cardiac arrhythmia concerning the conduction and blockages of electrical signal paths at the tissue or the cellular level, signals recorded on the surface of the heart, called the atrial or ventricular/epicardiac and endocardiac electrograms electrograms can aid the research on epicardiac mapping [51][52].

Typically, the energy of an ECG waveform lies between 1-200 Hz and has an amplitude of 1-5 mV. The energy of cardiac electrograms measured on the epicardium and endocardium lies between 1 Hz and 2.5 kHz [51]. The typical peak-peak amplitude of epicardial and endocardial electrograms is about 10 and 30 mVpp, respectively. In the acquisition setup currently used to acquire electrograms at the Erasmus Medical Centre, Rotterdam [5], the bandwidth is limited to 400 Hz by a maximum sampling rate of 1 kS/s for a single channel. To generate an activation map based on the epi- and endocardiac electrograms, a bandwidth of 400 Hz is sufficient. To record complex fractionated atrial electrograms (CFAE) in the atria, higher bandwidths extending beyond 1 kHz are required [52].

Depending on the size, type, and electrodes used to record the signals, the interface between the electrode and the skin/tissue can be modeled by means of a resistive-capacitive network [53]. According to the IEC 60601-2-47 standard for the acquisition of ambulatory ECG, the noise levels should be lower than 50 μV pp ($\approx$ 18 μVrms) [36]. The noise generated due to the electrode-tissue interface depends on the effective impedance and the total signal bandwidth. In order to have a negligible impact on the overall noise performance, the total noise of the CMOS circuits dominated by thermal, shot, and flicker noise should be minimized. A maximum signal amplitude of 30 mVpp can be expected for atrial electrograms. Thus, to acquire a raw waveform and to be able to detect changes in the amplitude of small local potentials for research purposes, a high-resolution front-end targeting an ENOB of 12 bits and a minimum bandwidth of 1 kHz is required.

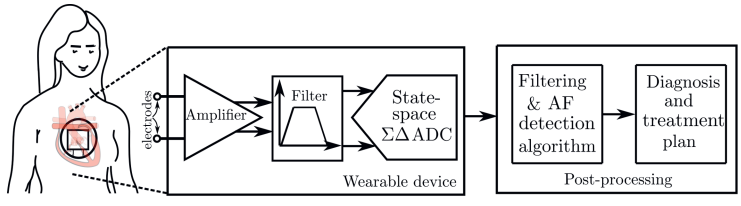
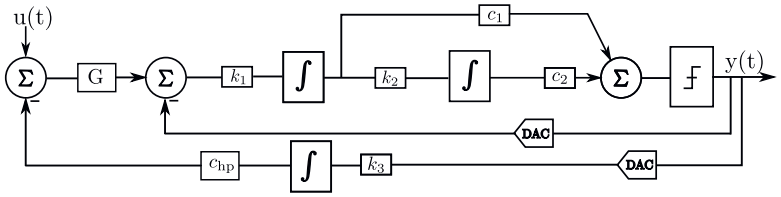
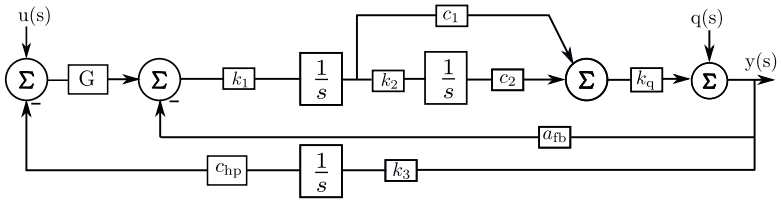


Figure 3.20: Proposed ECG acquisition system for AF diagnosis.



(a) Block diagram



(b) Linear model

Figure 3.21: Block diagram and linear model of the proposed analog front-end

In this chapter, we implement the design of a single-channel analog front-end based on the state-space design approach [32] that is fully-integrated in 0.18 μm CMOS technology. Figure 3.20 shows the conceptual diagram of the acquisition of cardiac signals. Section 3.3.2 presents the system overview. Section 3.3.3 details the design of the fully-integrated analog front-end implementation. We present the measurement results in Section 3.3.4 and, finally, conclusions in Section 3.3.5.

3.3.2 System overview

To accommodate a range of biosignals such as electrocardiogram, atrial electrogram (AEG), electroencephalogram (EEG) or electromyography (EMG), with varying frequency characteristics, the front-end is designed for a bandwidth of 3 kHz. Based on the state-space

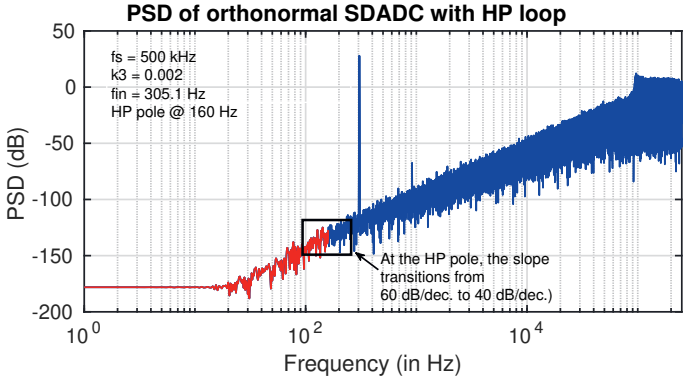


Figure 3.22: PSD of the output spectrum of the orthonormal ΣΔ ADC with HP loop.

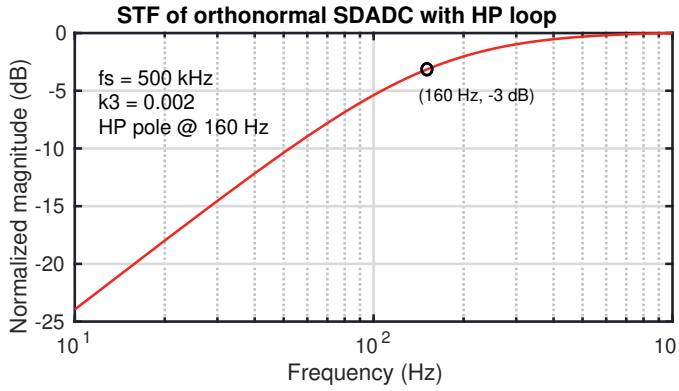


Figure 3.23: Signal transfer function of the orthonormal ΣΔ modulator with HP loop.

Table 3.7: Parameters of the proposed front-end based on orthonormal ΣΔ modulator

Parameter	Value
k_1	0.5
k_2	0.5
a_{fb}	1
c_1, c_2	1
c_{hp}	0.01
k_3	0.002
G	100
f_s	500 kHz

design approach for optimal dynamic-range ΣΔ ADCs, an orthonormal ΣΔ topology is selected [32]. To achieve a resolution of 12-bits, a 2nd order orthonormal modulator with a sampling frequency of 500 kHz and an over-sampling rate of 80 is selected. A first-order roll-off implements the high-pass filter cut-off frequency. The coefficients of the topology are tabulated in Table 3.7. Figure 3.21 shows the block diagram and the linear model of the proposed front-end. The signal transfer function and the quantization noise transfer function equations of the proposed front-end using an orthonormal ΣΔ modulator topology with a first-order high-pass loop can be written as:

$$\mathrm{STF} = \frac{\mathrm{sGk_1k_q(c_1s + k_2c_2)}}{\mathrm{s^3 + s^2c_1k_1k_qa_{fb} + s(c_1k_1k_3k_qc_{hp}G + a_{fb}k_1k_2k_qc_2) + k_qk_1k_2k_3c_2c_{hp}G}} \tag{3.39}$$

$$\mathrm{qNTF} = \frac{\mathrm{s^3}}{\mathrm{s^3 + s^2k_1k_qa_{fb}c_1 + s(k_1a_{fb}k_2c_2k_q + k_1k_3k_qc_1c_{hp}G) + k_qk_1k_3k_2c_2c_{hp}G}} \tag{3.40}$$

Solving the characteristic equation, the very low frequency high-pass pole is located at,

$$s \approx \frac{1}{2\pi}\frac{k_3 c_{hp} G}{a_{fb}} \cdot f_s. \tag{3.41}$$

where f_s is the sampling frequency and k_3, c_{hp}, G and a_{fb} are parameters of the modulator. Equations 3.39 and 3.40 show the signal and quantization noise transfer function of the ΣΔ converter topology, respectively. Figures 3.22 and 3.23 show the PSD of the

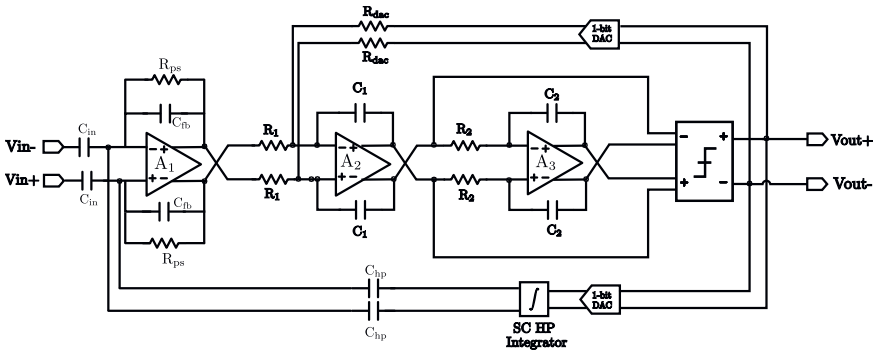


Figure 3.24: Architecture implementation of the proposed front-end with orthonormal ΣΔ ADC

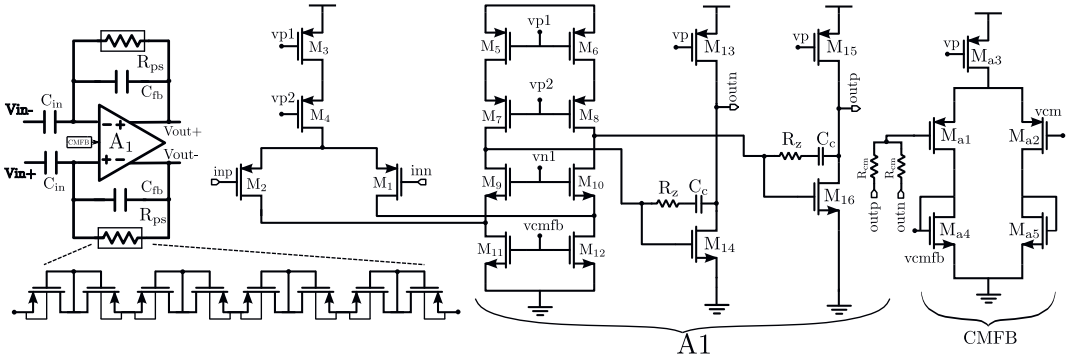


Figure 3.25: Implementation of preamplifier: Schematic of 2-stage opamp (A_1) and CMFB circuit

output spectrum with noise-shaping characteristics and the signal transfer of the entire front-end, respectively, that are simulated behaviourally. The high-pass pole is located at 160 Hz to demonstrate the slope transitions clearly. For a lower high-pass filter cut-off frequency, coefficient k_3 can be chosen accordingly. The parameters are chosen such that the contribution of the quantization noise to the total noise is negligible.

3.3.3 Architecture and circuit design

Figure 3.24 shows the top-level block diagram of the single-channel cardiac analog front-end. The output of the amplifier is connected to a 2^{nd}-order ΣΔ ADC. A 1-bit DAC converts the digital bitstream into an analog signal and is connected to the Nagaraj integrator. The Nagaraj switched-capacitor integrator in negative feedback between the modulator's output and the pre-amplifier input implements the high-pass loop.

Pre-amplifier

The cardiac signals are recorded by electrodes that are placed in contact with the body surface or the tissue surface. Due to the electrode-tissue interface, a capacitive electrical double-layer is formed, which generates a DC offset. According to the IEC standards [18],[36], a maximum of +/-300 mV offset can be expected for gel-based electrodes. The

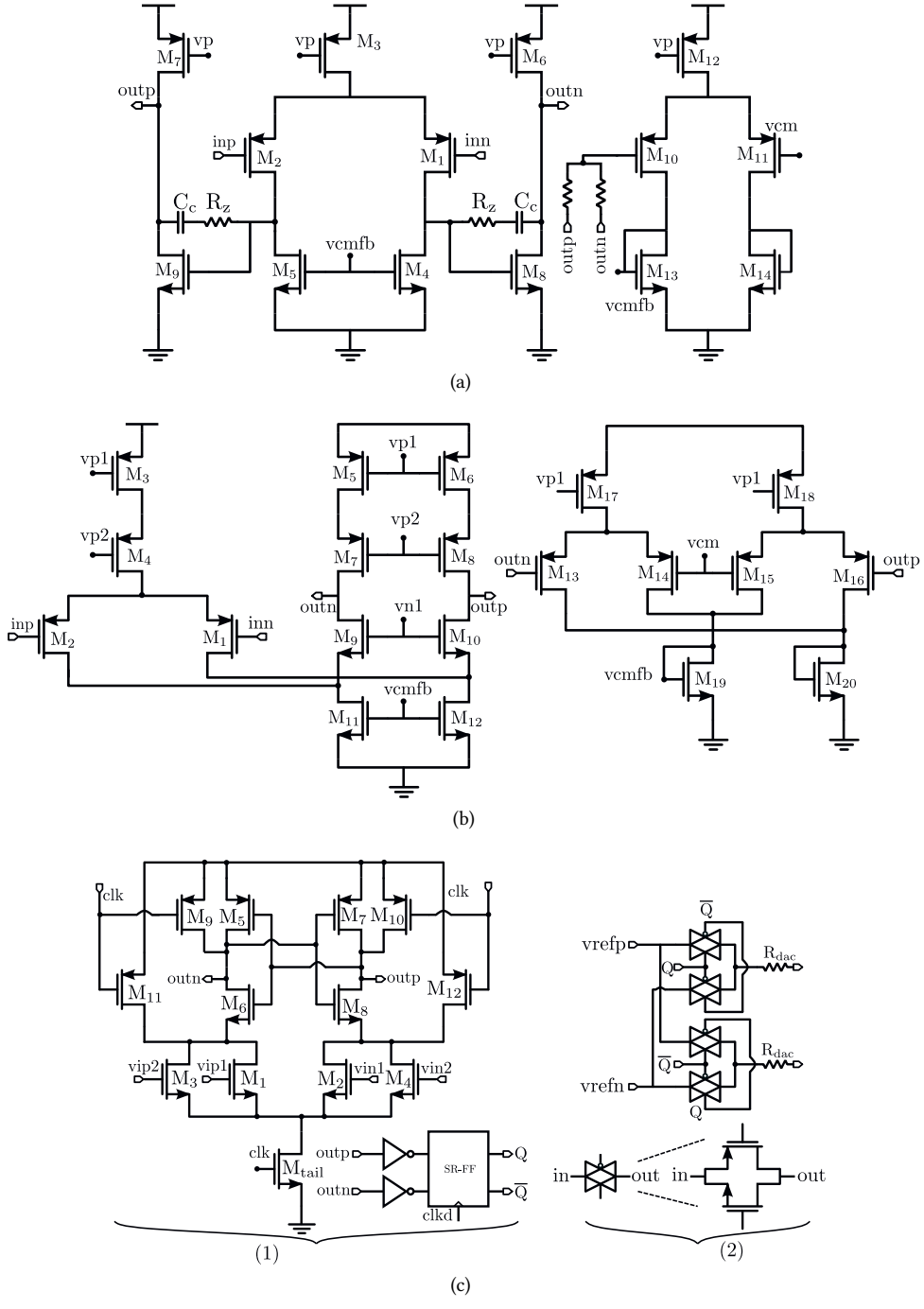


Figure 3.26: Implementation of ΣΔ modulator: (a) A_2 and CMFB circuit, (b) A_3 and CMFB circuit, (c) Dynamic comparator and a 1-bit DAC

AEGs are recorded using gold-plated (Au) electrodes without gel in the presence of a finite amount of blood. So, the expected offset can be much lower. The implemented front-end consists of a capacitively-coupled pre-amplifier to reject DC offset with a closed-loop gain of 100 or 40 dB.

Figure 3.25 shows the implementation of the preamplifier consisting of A_1, a 2-stage opamp, and a common-mode feedback (CMFB) control circuit. The CMFB block uses two resistors to extract the common-mode output voltage and an amplifier that drives the common-mode feedback control point $vcmfb$ in the opamp. The pre-amplifier is capacitively-coupled with a closed-loop gain of 100. The values of C_{in} and C_{fb} are 20 pF and 0.2 pF, respectively. C_{fb} is selected as 0.2 pF to implement a gain of 100. With a unit capacitance of 100 fF, the capacitors are implemented using a common-centroid layout technique to achieve high gain accuracy and minimize differential mismatch.

At the maximum input signal frequency of 1kHz, and for an input capacitance of 20 pF, the input impedance value of the pre-amplifier is given by $\frac{1}{2\pi f C_{in}} \approx 8$ MΩ. If higher input impedances are required (Z_{in} >> 10 x $Z_{electrode}$), lower values of C_{in} can be selected or other techniques, such as partial positive feedback can be applied.

The pseudoresistors are implemented by PMOS transistors due to their area and power-efficient design. They set the DC bias voltage at the input. The pseudoresistors and the feedback capacitance C_{fb} implement the high-pass filter cut-off. For the implementation of the opamp, a 2-stage topology is chosen as it provides high DC gain and is well suited to drive a resistive load. A folded-cascode topology implements the first stage. Cascoding improves the gain by increasing the output impedance at the expense of voltage headroom. The second stage is a common-source topology and provides a large output swing. The first stage dominates the noise. The input-referred noise of the input differential pair of a transistor biased in the subthreshold region is given by:

$$V_{ni,rms} = \sqrt{\frac{4kT \cdot U_T}{\kappa^2 \cdot I_D} \frac{\pi}{2} \cdot BW} \tag{3.42}$$

where k is Boltzmann's constant, T is the absolute temperature, κ is the subthreshold slope factor, U_T is the thermal voltage, kT/q, approximately 26 mV at body temperature, I_D is the current through the input transistor, and BW is the -3 dB bandwidth of the amplifier. The current through the input transistors can be increased to reduce noise at the expense of a higher power consumption. To characterize the efficiency of the bio-amplifier, its noise efficiency factor (NEF) can be calculated, which is given by [54] :

$$NEF = \sqrt{\frac{2I_{tot}}{4kT \cdot U_T \cdot \pi \cdot BW}} \tag{3.43}$$

PMOS input transistors are selected for lower flicker noise as compared to NMOSTs. The input PMOS differential pair M_1, M_2 is biased in the subthreshold saturation region (or weak-inversion saturation, WI-sat) to maximize the gain (viz., the transconductance g_m) for a given drain current. As the input-referred noise voltage is inversely proportional to g_m, a higher transconductance leads to lower input-referred noise voltage. PMOS transistors M_5, M_6 and NMOS transistors M_{11}, M_{12} are for biasing purposes only and therefore

Table 3.8: Device dimensions and operating point of the pre-amplifier

Devices	W/L (μm)	I_D (μm)	g_m/I_D (V^{-1})	V_{EFF}=V_{GS}-V_t (V)
M_1, M_2	300/4	2	24.5	0.081
M_3, M_4	40/8	4	10	-0.12
M_5, M_6	5/8	1	10	-0.12
M_7, M_8	10/8	1	12.9	-0.062
M_9, M_{10}	2.5/8	1	13.2	0.07
M_{11}, M_{12}	14.5/32	1	7	0.186
M_{13}, M_{15}	20/8	2	10	-0.12
M_{14}, M_{16}	5/4	2	13.4	0.07
M_{a1}, M_{a2}	1/1	0.25	16	-0.016
M_{a3}	5/8	0.5	10	-0.12
M_{a4}, M_{a5}	0.85/18	0.25	8.8	0.186

biased in strong inversion (SI), minimizing their g_m values and thereby their noise contribution. Since the voltage headroom consumed by devices operating in the SI region is higher than WI, there is a tradeoff between noise contribution and the available output swing. Table 3.8 summarizes the device dimensions and operating points. The common-mode voltage is maintained at 0.9V. A resistive-based CMFB circuit is implemented for higher linearity at the expense of power and area consumption and consumes 0.5 μA. The resistance values are 500 kΩ. Lower resistive values can be more area-efficient at the expense of higher current consumption.

From simulation results, it is seen that the 2-stage opamp has an open-loop gain of 112 dB, a phase-margin of 85° and a unity-gain bandwidth of 360 kHz. The total input referred noise is 2.3μVrms, while it consumes 10μA from a 1.8V supply. The closed-loop bandwidth of the amplifier is 3.5 kHz. The simulated NEF for the designed amplifier is 4.

SC Nagaraj integrator

To implement a high-pass cut-off frequency with high accuracy and linearity, a very large time-constant switched-capacitor Nagaraj integrator is implemented, as shown in Figure 3.27. The circuit operates in two non-overlapping phases, ϕ_1 and ϕ_2, generated by a non-overlapping clock phase generator. C_2 is the integration capacitor that attenuates the signal. The value of the unity-gain frequency, f_{ugb}, of the integrator is determined by:

$$f_{ugb} = \frac{1}{2\pi} \frac{1}{\left[1 + \frac{C_3}{C_2}\right]} \frac{C_1}{C_2} \frac{C_3}{C_2} f_{clk}. \tag{3.44}$$

Since the cut-off frequency is set by capacitor ratios and f_{clk}, a high accuracy (> 99%) can be expected [32]. For the selected values f_{clk}=500 kHz, C_I=30 pF and C_1 = C_3 = 0.1 pF, the f_{hpf} of the integrator is located at 0.88 Hz. The value of C_{hp} is equal to 0.2 pF, the same as the feedback capacitance of the pre-amplifer. The opamp chosen is a folded-cascode topology. Since the time-constant is very large, the requirement of the DC gain, UGB, and slew-rate are relaxed [32].

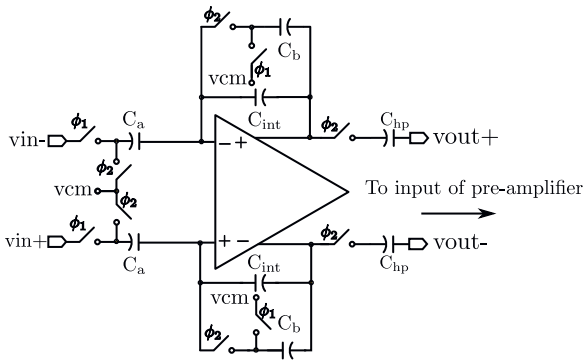


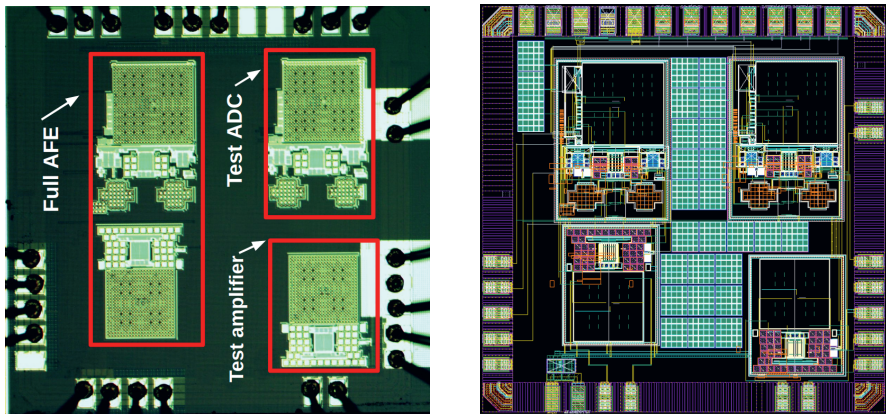
Figure 3.27: SC Nagaraj integrator

2^{nd}-order ΣΔ ADC

For achieving a high-resolution analog front-end, we implement a fully-differential 2^{nd} order orthonormal ΣΔ ADC modulator as shown in Figure 3.21. The sampling frequency of the modulator is 500 kHz for a signal bandwidth of 2 kHz with an oversampling ratio of 125. The coefficients are given in Table 3.7 and are selected for the high dynamic range and stability of the modulator. The transistor-level implementation is shown in Figure 3.26. A single-bit quantizer is used to sample the output, which is stored in an SR flip-flop. A 1-bit DAC is used to convert the digital output to an analog value which is fed back at the input of the first integrator. The continuous-time loop filter is implemented using opamp-RC integrators, which offer high linearity at the expense of slightly higher power consumption as compared to other alternatives. g_mC integrators can be chosen for lower power consumption at the expense of reduced linearity.

Integrators suffer from non-idealities that lead to degradation of modulator performance such as finite DC gain, finite unity-gain bandwidth (UGB), and finite slew rate. Since the overall performance of the modulator is dominated by the first integrator, it should satisfy the requirements and be designed carefully. From behavioral simulations, it is found that the minimum DC gain required for the first integrator to have negligible degradation of performance is 80 dB. For the second integrator, a DC gain of 60 dB is sufficient. To minimize the impact of finite GBW, a GBW value of at least 1 f_s is required [32]. For stable single-loop modulators, variations in RC products lead to minor degradation in modulator performance. From behavioral simulations, there is no significant degradation in performance up to ± 40% time-constant variation.

Design of the first integrator: As shown in Figure 3.26, a 2-stage opamp is chosen for implementing the opamp (A_2) used in the first integrator to achieve high DC gain and large output swing. To maintain high linearity and to ensure that the output does not saturate at large output swing values, a CMFB block that uses two resistors to extract the common-mode output voltage and an amplifier that drives the $vcmfb$ point in the opamp is used (Fig 3.26). The input stage consists of large area PMOS transistors with a W/L= 300 μm/4μm for lower flicker noise that are biased in their WI-sat region for maximum power efficiency. The opamp is frequency-compensated by pole-zero cancellation using a capacitance C_c of 5pF and a resistor R_z of 44 kΩ. M_3, M_4 and M_5 are biased in SI-sat to minimize g_m,



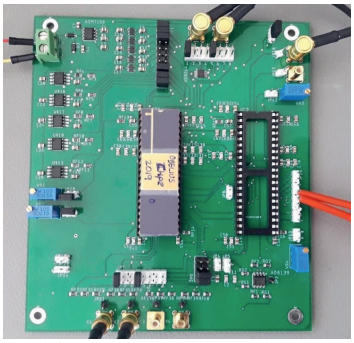
(a) (b)

Figure 3.28: Chip (a) micrograph and (b) layout.

and thus their noise contributions. The second integrator (A_3) is implemented as a folded-cascode opamp with power-efficient CMFB as shown in Figure 3.26b. It has relaxed DC gain, swing, linearity, slew-rate, and loading requirements. The values of the resistances and capacitances are $R_1 = R_2 = 1M\Omega$ and $C_2 = C_2 = 3.6pF$, respectively.

Design of the 1-bit comparator: For single-bit quantization, a two-input dynamic comparator based on the strong-arm latch comparator [55] is used. It performs weighted addition (coefficients c_1, c_2) and implements a 1-bit quantizer in a power- and area-efficient manner. The comparator consists of one tail transistor M_{tail}, 4 input transistors, M_1, M_2, M_3 and M_4, 4 reset transistors M_9, M_{10}, M_{11} and M_{12}, and 4 cross-coupled transistors M_5, M_6, M_7 and M_8. By using a large-width tail transistor, a higher dynamic current can be supplied, thus reducing the decision time. When the clk goes low, the tail transistor is OFF, and the internal nodes are charged to V_{DD}, thus resetting the output nodes. When the clk goes high, M_{tail} switches ON, allowing a path for discharge. Depending on the difference between the differential input voltages, slightly different currents flow through the branches, thus discharging at different rates. Based on the voltage level at the output nodes, either M_5 or M_7 turns ON while the other turns OFF, which is reinforced through the cross-coupled structure. One of the outputs reaches V_{DD} while the other node is pulled to GND. The output of the comparator is connected to an SR flip-flop through inverters, which hold the final value.

Design of the 1-bit DAC: The output of the comparator is connected to a 1-bit DAC, which is in turn fed to the input of the first integrator through resistances R_{dac}. The 1-bit DAC consists of 4 switches implemented by transmission gates (T-gates). A T-gate implementation is used for rail-to-rail operation and reduced ON-resistance of the switches. The positive ($vrefp$ = 1.1 V) and negative ($vrefn$ = 0.7 V) DAC reference voltages are switched by the comparator outputs Q and $\bar{Q}$, which are connected to R_{dac}. The value of R_{dac} equals R_1, implementing a gain factor of 1.



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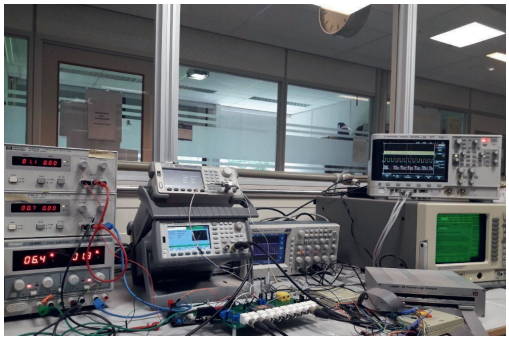


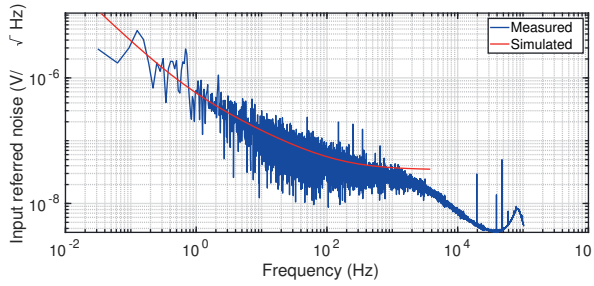
(b)

Figure 3.29: (a) Custom evaluation board, (b) Measurement setup.

3.3.4 Measurement results

The analog front-end for ECG signal acquisition has been fabricated in TSMC 1P6M 0.18 μm CMOS process. The prototype chip, including the main core, test structures, and the IO ring, measures 1.6 mm x 1.6 mm and consists of a single-channel analog front-end, a test ADC, and a test amplifier, as shown in Figure 3.28a. Figure 3.28b shows the layout of the entire chip. The active area of a single-channel front-end, which includes the pre-amplifier, the 2^{nd} order ΣΔ modulator and the HP loop is 0.448 mm^2. The resistors and capacitors are implemented using metal-insulator-metal capacitors and high-res polysilicon resistors, respectively. The bit-stream output of the ΣΔ converter is acquired using a 5442D MSO Picoscope, and the performance is analyzed using MATLAB. The digital and analog core circuits are powered by separate 1.8V power supplies and grounds to minimize noise. Also, decoupling capacitors implemented using MOM capacitors are connected between the power supply and ground to reduce power supply noise. The fabricated prototype is packaged in a DIP-40 package for testing using a custom-designed PCB Obelius.

Figure 3.29a shows the implementation of PCB Obelius for testing the fabricated chip. The measurement setup is shown in Figure 3.29b. To power up the PCB, a lab DC power supply is used to power a master low dropout regulator (LDO), ADM7150, which powers fixed-voltage LDOs (1.8V, 3.3V), voltage buffers, and adjustable reference voltage sources. The adjustable reference voltage sources are implemented using buffers and resistive dividers. A reference bias current (1 μA) is generated using a potentiometer. The device under test (DUT) is excited by sinusoidal signals generated by a signal generator connected to the PCB via SMB connectors. Clock sampling frequencies of 500 kHz and 2 MHz are generated by Agilent waveform generators. A Picoscope is used to acquire the digital output data and sends it through a USB cable connected to the PC. The generated bit-stream is processed in MATLAB using digital filters, and the performance is analyzed using an FFT test bench. A Kaiser window is used to measure the performance metrics and is compared against simulation results.



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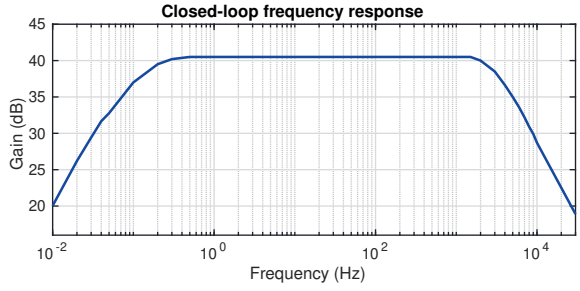

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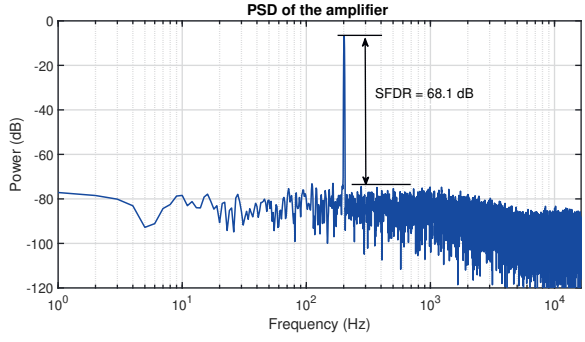


(c)

Figure 3.30: Measured performance of the pre-amplifier: (a) Input-referred noise, (b) AC response of the pre-amplifier, (c) Linearity of the amplifier (THD = 0.17 % @ 14 mVp input, f_{in} = 200 Hz)

Table 3.9: Measured performance of the pre-amplifier

Technology	0.18 μm TSMC
Supply voltage	1.8 V
Current (opamp+CMFB)	10.5 μA
Total current (incl. bias)	15.5 μA
Amplifier Bandwidth	150 mHz - 3 kHz
Closed-loop gain	40.5 dB
Gain accuracy	1.25 %
Input ref. noise	6.3 μVrms (BW=1Hz to 3 kHz)
Input referred-offset	564 μV
NEF (excl. bias current)	14.3
CMRR	67 dB
THD (14mVp input, f_{in}=200Hz)	0.17%

Performance results

Table 3.10 tabulates the measured performance of the ECG recording system. Figure 3.30 shows the measurement results of the pre-amplifier: (a) the input-referred noise voltage spectral density; (b) the closed-loop gain as a function of frequency and, (c) the output frequency spectrum for a 200-Hz, 14-mVp input signal. The gain can be made variable by incorporating a capacitor bank and switches at the input (C_{in}) if a variable gain is desired. Fig. 3.30a shows the measured and simulated input-referred noise of the pre-amplifier. The measurement is carried out using Dynamic Signal Analyzer from Stanford Research Systems (SR785). The measured thermal and simulated noise levels are at $38nV/\sqrt{Hz}$ and $36nV/\sqrt{Hz}$, respectively. The measured flicker corner is at 500 Hz. Flicker noise and thermal noise contribute to 6 μVrms and 1.97 μVrms, respectively, totaling upto 6.3 μVrms in the signal bandwidth extending from 1Hz to 3 kHz. The measured fixed gain of the AC-coupled amplifier is 105 as shown in Figure 3.30b. Figure 3.30c shows the THD performance of the pre-amplifier and measures 0.17% for an input amplitude of 14 mVp and an input frequency of 200 Hz. Table 3.9 summarizes the performance results of the pre-amplifier. Fig 3.31 shows the power consumed by various blocks.

Figure 3.32 shows the FFT spectrum of the orthonormal ΣΔ ADC for an input frequency of 200 Hz and an amplitude of -1.4 dBFS ($dBFS = 20 \cdot \log_{10} \frac{Vin}{Vref}$ where 0 dbFS refers to 0.8 Vp-p. Figure 3.33 shows the measured SNDR performance versus input amplitude, demonstrating a peak SNDR of 72.5 dB for a bandwidth of 1 kHz and 69.8 dB for a bandwidth of 3 kHz and a dynamic range of 77 dB for an input amplitude of -1.4 dBFS. The Walden FoM (linear form) of the ADC is given by:

$$FoMw = \frac{P}{2^{ENOB} \cdot 2 \cdot BW} \tag{3.45}$$

and equals 5.35 pJ/conv. The Walden FoM (logarithmic form) of the ADC is given by:

$$FoMw = SNDR + 10 \cdot log10\left(\frac{BW}{P}\right) \tag{3.46}$$

and equals 145.5 dB.

Table 3.10: Measured performance of the proposed 2nd order orthonormal ΣΔ ADC

Technology	0.18 μm TSMC
Supply voltage	1.8 V
Total current (incl. bias)	36.4 μA
Signal bandwidth (f_b)	3 kHz
Sampling frequency	500 kHz
Peak SNDR	69.8 dB (f_b=3 kHz); 72.5 dB (f_b=1 kHz)
ADC power	81 μW
SFDR	79.68 dB
DR	78 dB
ENOB	11.3
Walden ADC FoMw (linear form)	5.35 pJ/conv.

The Schreier FoM (logarithmic form) of the ADC is given by:

$$FoMs = DR + 10 \cdot log10\left(\frac{BW}{P}\right) \tag{3.47}$$

and equals 152.7 dB.

The measured system transfer for various signal amplitudes is plotted in Fig. 3.34. A high-pass pole resulting from the pseudoresistor and C_{fb} occurs at 0.1 Hz, as shown in the figure. C_{hp} introduces a zero in the path which reduces the reduces the impact of the feedback loop beyond the -3 dB point of the SC integrator. Figure 3.34 shows the measured system transfer for different amplitudes.

The linearity performance achieved by SC Nagaraj integrator and capacitor ratios is compared with pseudoresistors in Figure 3.35. Figure **??** presents the SFDR performance of the high-pass loop at f_{in} = 8 Hz close to the pole location (12 Hz). Figure 3.35b presents the SFDR performance at f_{in} = 0.3 Hz close to the pole location (0.1 Hz). Figure 3.36 shows the variation of SFDR with respect to the input frequency. It can be seen that at lower frequencies, the SFDR value drops. Figure 3.37 shows the measured PSD of the complete AFE with a 100 Hz input sinusoidal signal with an amplitude of 3.4 mVp. It also shows the PSD of the system with shorted inputs. The measured input referred noise of the entire system, including the ADC and the HP loop, is 9.7 μVrms. The prototype is validated by acquiring ECG from a live subject, as shown in Figure 3.38. Table 3.11 compares the results of the proposed front-end with other state-of-the-art solutions.

3.3.5 Conclusions on the design of orthonormal HPΣΔ modulator architecture

In this section, we described the design of an analog front-end based on the state-space approach for optimal ΣΔ architectures outlined in Section 3.2 targeting the acquisition of cardiac signals. Measurement results show that the orthonormal ΣΔ converter has a peak SNDR of 69.8 dB, corresponding to 11.3 bits of ENOB, for a signal bandwidth of 3 kHz while consuming 40.5 μA from a 1.8 V supply. The fabricated prototype is tested and validated by acquiring a real ECG waveform from a live subject.

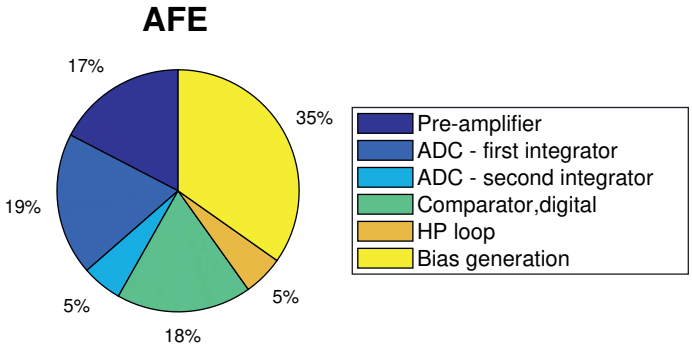


Figure 3.31: Power distribution among blocks of the AFE

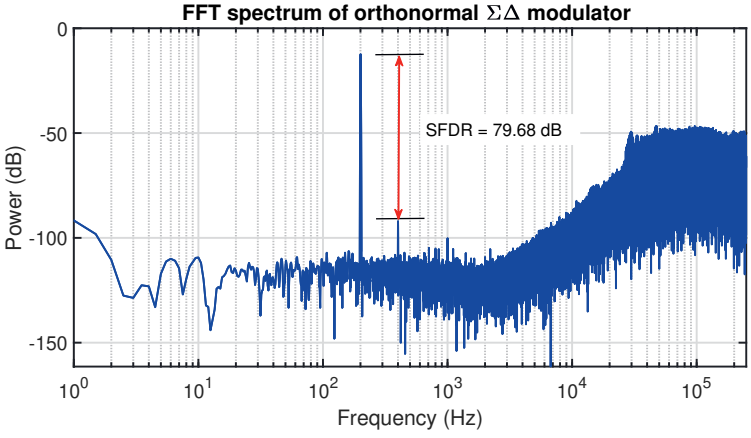


Figure 3.32: PSD of orthonormal ΣΔ ADC for -1.4 dBFS input signal at 200 Hz.

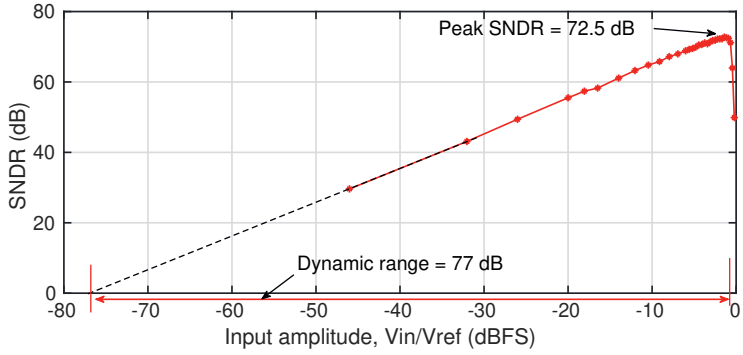


Figure 3.33: Measured SNDR versus input amplitude of orthonormal ΣΔADC.

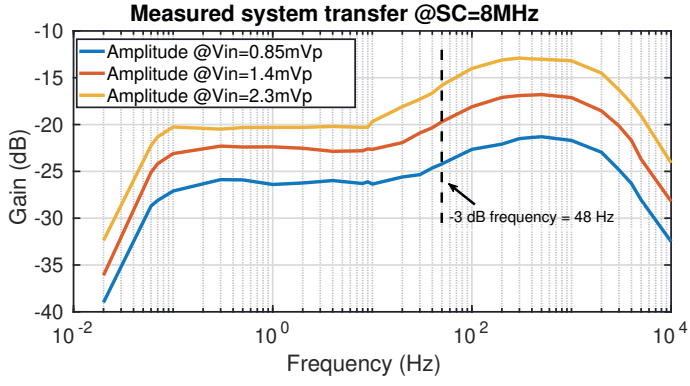
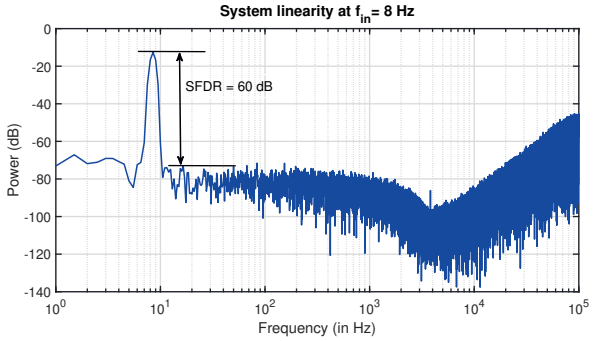
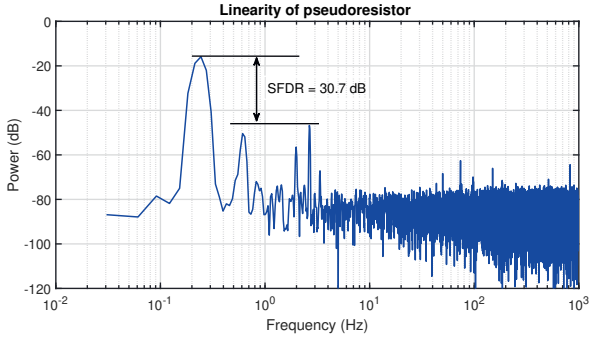


Figure 3.34: Measured system transfer at SC = 8 MHz for varying amplitudes (G=100).



(a) Proposed f_{hpf} using very large time-constant SC integrator: output spectrum for f_{in} = 8 Hz



(b) Harrison amplifier using pseudoresistors: Output spectrum for f_{in} = 0.3 Hz

Figure 3.35: Linearity comparison

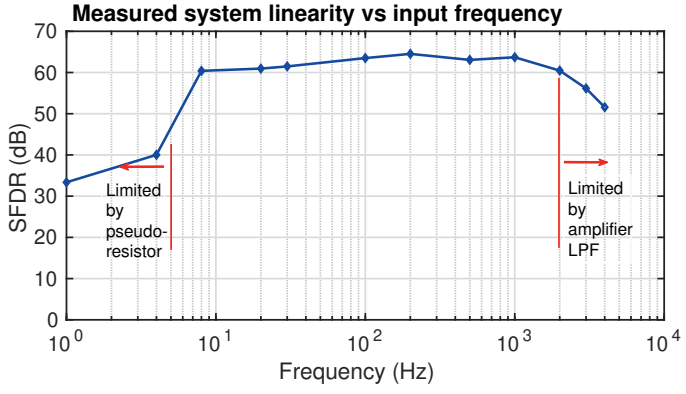


Figure 3.36: Measured linearity versus input frequency of the system AFE @ $0.7V_{FS}$.

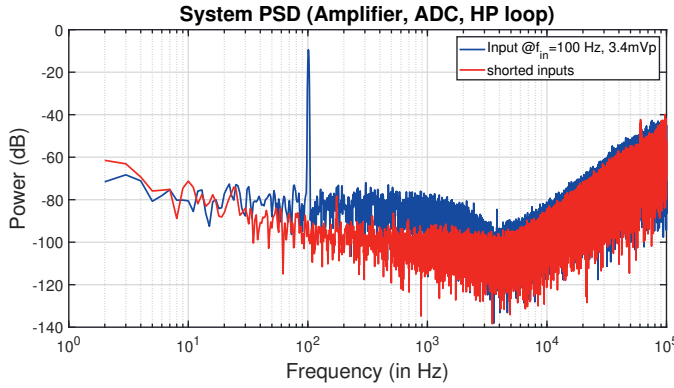


Figure 3.37: Measured power spectral density of the system with a 100 Hz sinusoidal input.

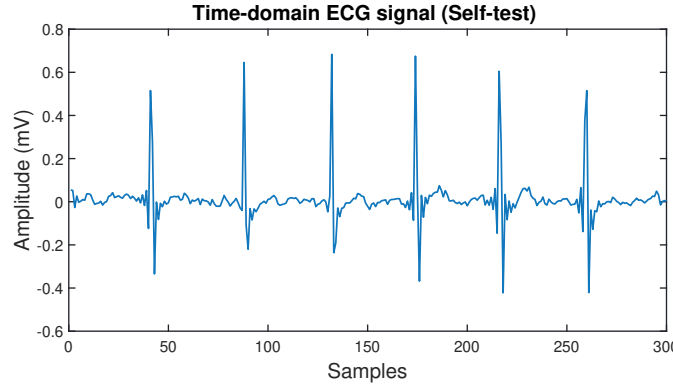


Figure 3.38: Validation with ECG measurement on a live subject

Table 3.11: System performance comparison with state-of-the-art HP cut-off frequency techniques and ΣΔ modulators for biosignal acquisition

	This work	[Melo]	[Somappa]	[Lee]	[Harrison]	[Rout]
Year	2021	TCAS-I 2019 [56]	TCAS-I 2020 [57]	TBCAS 2021[58]	JSSC 2003 [19]	TBCAS 2018 [32]
ΣΔ design method	State-space	Genetic algorithms	NA	NA	NA	State-space
ADC architecture	CT Orthonormal HP 2^{nd} ΣΔ	CT Pseudo-passive 3^{rd} ΣΔ	CT Fully-passive 2^{nd} ΣΔ	Modulated HP 2^{nd} ΣΔ	NA	CT Orthonormal HP 2^{nd}ΣΔ
Blocks included	Pre-amplifier, ADC	ADC	ADC	Pre-amplifier, ADC	Amplifier	ADC
Bio-signal	Cardiac (ECG, AEG)	General purpose	Bio-signals	ECG	Neural	ECG
Bandwidth	1 Hz-3 kHz	2 MHz	10 kHz	200 Hz	0.025 Hz-7.2kHz	1 Hz-0.2 kHz
HPF transfer	Yes	No	No	Yes	Yes	Yes
HPF technique	SC. int, cap. ratio	NA	NA	HP integrator	Pseudoresistors	SC. int, res. ratio
Linearity at f_{hpf} [dB]	60	NA	NA	NA	NA	76
System noise (with HP loop)	9.71 μVrms	NA	NA	NA	NA	NA
Supply voltage [V]	1.8	0.7	1	1.8	±2.5	1.8
ADC SNDR [dB]	69.8	69.1	49.8	64.8	NA	76
ADC DR [dB]	78	76.2	55.3	82	NA	NA
ADC power [μW]	81	256	0.61	5.2	NA	146
Sampling frequency	500 kHz	320 MHz	2.56 MHz	25.6 kHz	NA	128 kHz
Results type	Measurement	Measurement	Measurement	Measurement	Measurement	Simulation
FOM [pJ/conv]	5.35	0.027	0.5	9.1	NA	70.7
Walden ADC FoMw [dB]	145.5	168.02	151.96	140.7	NA	137.3
Schreier ADC FoMs [dB]	152.7	174.9	157.4	157.9	NA	NA
Technology [nm]	180	65	180	180	150	180

3.4 Conclusions

In this chapter, a state-space approach for ΣΔ modulators targeting a desired arbitrary signal transfer and noise transfer functions while optimizing their dynamic range is proposed, verified, implemented, and demonstrated in standard CMOS technology.

In the first part of the chapter (Section 3.2), the proposed state-space design method for ΣΔ ADCs for acquiring cardiac signals with high linearity and high accuracy are discussed and analyzed. The impact of the integrator noise sources and state excitations is investigated through intermediate function calculations. It is seen that for very small integrator coefficients, the impact of integrator non-idealities on the overall ADC is almost negligible. Finally, an orthonormal ΣΔ topology offers better performance than an observable canonical ΣΔ architecture.

In the second part of the chapter (Section 3.3), a complete analog front-end consisting of a pre-amplifier and an orthonormal ΣΔ ADC with a high-pass loop is implemented to demonstrate the proposed state-space design approach for acquiring cardiac signals. Measurement results of chip Obelius validate the proposed methodology in a standard CMOS IC technology. The proposed orthonormal HPΣΔ ADC achieves an FoM of 5.35 pJ/conv while occupying an area of 0.126 mm^2.

4

Spread-spectrum modulated multi-channel biosignal acquisition

The key challenges in designing a multi-channel biosignal acquisition system for an ambulatory or invasive medical application with a high channel count are reducing area and power consumption and the outgoing wire count. This chapter proposes a spread-spectrum modulated biosignal acquisition system using a shared amplifier and an ADC. We propose a design method to optimize a recording system for a given application based on the required SNR performance, number of inputs, and area. The proposed method is tested and validated on real pre-recorded atrial electrograms and achieves an average percentage root-mean-square difference (PRD) performance of 2.65% and 3.02% for sinus rhythm (SR) and atrial fibrillation (AF), respectively by using pseudo-random binary-sequence (PRBS) codes with a code-length of 511, for 16 inputs. We implement a 4-input spread-spectrum analog front-end in a 0.18 µm CMOS process to demonstrate the proposed approach. The analog front-end consists of a shared amplifier, a 2^{nd} order ΣΔ ADC sampled at 7.8 MHz, used for digitization, and an on-chip 7-bit PRBS generator. It achieves a number-of-inputs to outgoing-wire ratio of 4:1 while consuming 23µA/input, including biasing from a 1.8 V power supply and 0.067 mm^2 in area.

This chapter is partly based on S. Rout et al. Spread-spectrum modulated multi-channel biosignal acquisition using a shared analog CMOS front-end, *TBCAS 2023* [59] and S. Auerbach, W. A. Serdijn, and S. Rout. Compressed-sensing of spatiotemporally-correlated and/or rakeness-processed electrograms. *US Patent App. 16/846,551* [60].

4.1 Introduction

Atrial electrograms (AEGs) are biosignals recorded on the surface of the atria, whereas electrocardiograms (ECGs) are recorded on the surface of the body, both of which help doctors and medical researchers understand the propagation of electrical signals in the heart and diagnose cardiac abnormalities such as atrial fibrillation (AF). ECGs are vector summations of the epicardial signals acquired non-invasively on the body surface, whereas AEGs offer high spatio-temporal information acquired invasively on the epicardial or the endocardial surface [5]. AEGs are obtained invasively or minimally invasively during open-heart surgery or a catheter operation, respectively. For minimally invasive surgeries, typically, a 6 Fr (2 mm) catheter tube is used, which poses a strict constraint on the area and the maximum number of outgoing wires. Current techniques for acquiring AEGs require a long cable connecting a multi-electrode flexible array[5] placed on the epicardial surface and an acquisition module for high-density mapping. The limitations of the current solution can be listed as follows: a) interference due to the long cable degrading signal quality; b) limited maneuverability as the number of outgoing wires from the array is equal to the number of electrode inputs, and c) area constraints for minimally invasive applications.

In a traditional N-input system, the total number of amplifiers, ADCs, and outgoing wires equals the number of inputs N; thus, scaling area, power, and outgoing wire count linearly by N. To address these limitations, one can use channel-sharing techniques such as time-division (TDM), frequency-division (FDM), or code-division multiplexing (CDM). TDM requires a dedicated amplifier per input [11] and does not utilize the total bandwidth of the ADC effectively. The order of the inputs is also important for signal reconstruction in the digital domain. [25] uses TDM to acquire signals after the electrode but requires a high-bandwidth front-end to meet settling and noise requirements. FDM based on frequency modulation (FM) uses separate frequency bands simultaneously [12] and requires a dedicated oscillator, a bandpass amplifier, and an off-chip high-Q inductor per input posing a constraint on the area and power. FDM based on amplitude modulation (AM) would require a very high dynamic range (>100 dB) [12] ADC due to voltage summation of N inputs. [26] implements CDM using a dedicated amplifier and filter circuitry before code modulation, whereas [27] modulates the signals at the input using orthogonal codes. CDM offers (a) increased capacity, allowing multiple users to share the same band; (b) improved signal quality as it suppresses interference and band-limited noise; (c) improved security, a unique code encodes each input, and (d) simpler implementation, as compared to FDM. Therefore, as illustrated in Fig 4.1, CDM is chosen as the channel-sharing technique in this work.

Fig. 4.1 shows the block diagram of conventional spread-spectrum digital (Fig. 4.1a) and analog (Fig. 4.1b) front-end (FE), which requires dedicated FE resources per input. Fig. 4.1c shows the proposed spread-spectrum FE. Modulating the signal early in the signal chain can minimize the effects of unwanted band-limited signals with finite power, such as electromagnetic interference or $\frac{1}{f}$ noise, and offset of the following CMOS blocks. Fig. 4.2 shows a linear model of the proposed spread-spectrum FE for acquiring atrial electrograms. The proposed approach a) enables high-density signal-wavefront mapping from a 2D electrode array while reducing the outgoing wire count, (b) reducing area by

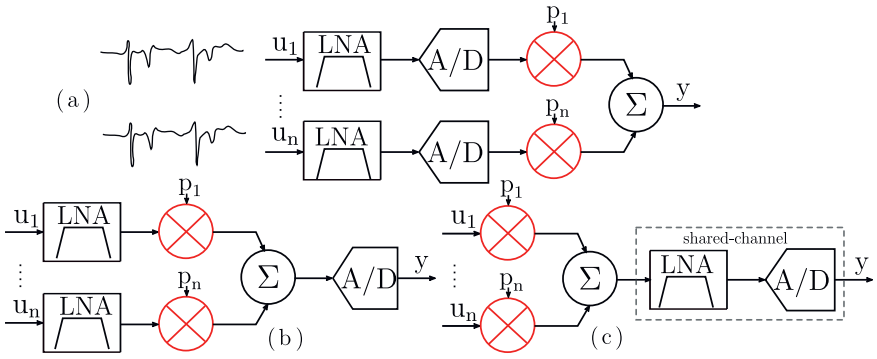


Figure 4.1: Approaches to implementing spread-spectrum modulation: (a) in the digital domain (conventional), (b) in the analog domain, after amplification (conventional), and (c) in the analog domain, before amplification (proposed).

sharing FE channel resources, and (c) reducing flicker noise and offset of the FE CMOS block. The acquired signal is written as,

$$y(t) = \{\sum_{i=1}^{N} u_i(t)p_i(t) + n_f(t) + n_{th}(t) + n_{emi}(t)\}A + n_{q,adc}(t) \tag{4.1}$$

where $y(t)$ is the total signal acquired, $u_i(t)$ is the signal from the i_{th} electrode and $p_i(t)$ is the code-sequence uniquely assigned to the i_{th} signal, $n_f(t)$ is band-limited $\frac{1}{f}$ noise, $n_{th}(t)$ is wide-band thermal noise, $n_{emi}(t)$ is interference due to EMI, $n_{q,adc}(t)$ is the quantization noise of the ADC, and N is the number of inputs. The received signal is correlated with the replica of the code sequence on the receiver side. The reconstructed signal, $y_i(t)$, can be written as,

$$y_i(t) = y(t)p_i(t) \tag{4.2}$$

$$= p_i(t)A\sum_{i=1}^{N} u_i p_i(t) + p_i(t)\{A(n_f(t) + n_{emi}(t)) + n_{q,adc}(t)\} \tag{4.3}$$

$$= Au_i(t) + p_i\{A(n_f(t) + n_{emi}(t)) + n_q(t)\} \tag{4.4}$$

Given that the the signal energy of p_i is distributed over a large frequency band, from Eq. (4.4), the u_i^{th} signal is recovered while $\frac{1}{f}$ noise, electromagnetic interference and offset are modulated by the p_i^{th} sequence and are filtered out using a low-pass filter.

The rest of the chapter is organized as follows. In Section II, a classification of existing modulation schemes is proposed. In Section III, a method to optimize a spread-spectrum FE for acquiring biosignals by selecting code-length, modulation frequency, and the number of inputs is discussed. This approach has been validated using real pre-recorded biosignals using two types of commonly used codes, Walsh-Hadamard (WH) and pseudo-random codes. Section IV describes the system architecture and circuit implementation of

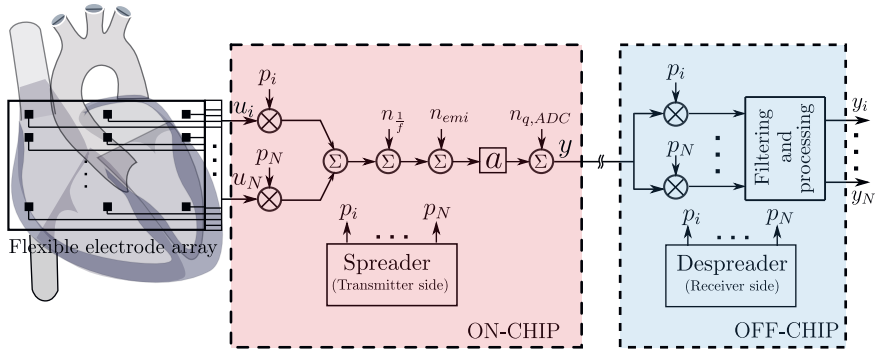


Figure 4.2: Linear model of the proposed spread-spectrum front-end for atrial electrogram acquisition.

the spread-spectrum modulated FE. Measurement results of a 4-channel spread-spectrum amplifier with a ΣΔ modulator implemented in 0.18 μm CMOS technology are presented in Section V. Finally, conclusions are drawn in Section VI.

4.2 Proposed classification

In this section, we propose a classification of modulation techniques based on the properties (or degrees of freedom) of the modulating signal (also known as the carrier wave), as shown in Figure 4.3. The degrees of freedom are (a) periodicity, (b) discretization in time, and (c) discretization in amplitude of the carrier wave, as shown along the x-, y-, and z-axis, respectively. To the authors' best knowledge, such a classification does not yet exist in the literature. Such a classification can give rise to newer modulation approaches that may or may not have been explored. Subsections 4.2.1 through 4.2.3 describe the degrees of freedom. Subsection 4.2.4 elaborates on the existing modulation approaches.

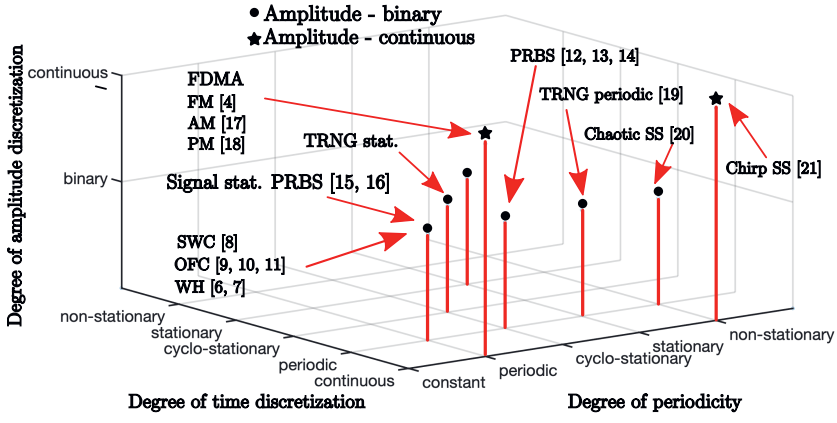


Figure 4.3: Proposed classification of modulation techniques

4.2.1 Degree of periodicity

The degree of periodicity of modulating signals refers to the occurence of symbols 0's and 1's and can be categorized into constant, periodic, stochastic-stationary, stochastic-cyclostationary and stochastic non-stationary, respectively.

- Constant: The symbols of the modulating waveform do not change (i.e., remain constant).
- Periodic: The signal is completely specified with respect to time and repeats with a period T_o.
- Stochastic-stationary: The signal is not fully specified with respect to time. However, the statistics are time-invariant. The mean is constant. The autocorrelation $R_X(t_1, t_2)$ only depends on time lag τ and is not a function of time t.
- Stochastic-cyclostationary: The statistics of the signal may vary periodically with time. The mean is cyclic in time t with a period T_o. Autocorrelation is a function of time period T_o.
- Stochastic non-stationary: The statistics change over time, i.e., the mean changes with time. Autocorrelation is a function of time t.

4.2.2 Degree of time discretization

Time discretization refers to the sampling instant in time and can be categorized as:

- Continuous: Time is continuous.
- Periodic: The sampling frequency is fixed.
- Stochastic-stationary: The sampling frequency is randomly varying but is stationary.
- Stochastic-cyclostationary: The sampling frequency is randomly varying , and the statistics vary periodically with time with a time period T_o. If the sampling instant of the signal is determined by other parameters, such as thresholding of the input signal, then the clock incorporates the properties of the input signal. In case of adaptive sampling, the rate of the clock depends on the activity of the input signal.
- Stochastic-non-stationary: The sampling frequency is randomly varying , and its statistics change with time.

4.2.3 Degree of amplitude discretization

Amplitude discretization can be categorized as:

- Discrete-M-ary values: The signal can assume a value from a well-defined set of outcomes. In general, a set of 2 (e.g., {0,1} or {-1,1} are binary sets), a set of 3 (e.g., {-1, 0, 1} is a ternary set) or a limited set of values (e.g., M-ary set) can be used. The total probability of all outcomes is the summation of individual probabilities and equals 1.
- Continuous values: The signal can assume any real value.

Table 4.1: Some example modulation techniques and applications

Paper	Technique	Application
[61]	Square-wave chopping (SWC)	Performance enhancement
[62],[63],[64]	Orthogonal freq. chop. (OFC)	Multi-channel recording
[26],[27]	Walsh Hadamard (WH)	Multi-channel recording
[65],[66],[67]	Pseudo-random binary seq. (PRBS)	Performance enhancement
[10]	Pseudo-random binary seq.(PRBS)	Compressed sensing
[68]	Signal stat. PRBS modulation	Single-channel recording
[12]	Frequency modulation (FM)	Single-channel recording
[69]	Amplitude modulation (AM)	Communication systems
[70]	Phase modulation (PM)	Communication systems
[71]	True random number gen. (TRNG)	Hardware security
[72]	Chaotic modulation	Communication systems
[73]	Chirp modulation	Communication systems
This work	PRBS modulation	Multi-channel recording

4.2.4 Existing modulation techniques

Input signals can be modulated with a waveform resulting from the orthogonal combination of the above-mentioned degrees of freedom. In this sub-section, a few existing modulation techniques are classified and placed on the three axes of a 3D grid to accommodate the three degrees of freedom, as shown in Fig. 4.3. Table 4.1 summarizes the modulation type and its corresponding application. [61] uses square-wave modulation (chopping) for improving the circuit's performance, i.e., reducing offset and flicker noise. Spread-spectrum clocking can be used with a chopper-stabilized amplifier, which reduces inter-modulation distortion [65, 66]. PRBS modulation is used together with a $\Sigma\Delta$ modulator to reduce substrate noise [67]. [62–64] are examples of an orthogonal modulation technique, also referred to as 'multi-frequency chopping'. All these techniques lie at $\{periodic, periodic, binary\}$ in Fig. 4.3. The modulating wave is characterized by orthogonal periodic sequences that assume binary amplitude values, i.e., ±1. Conventional code-division multiplexing (CDM) lies at $periodic$ (orthogonal) or $cyclostationary$ on the x-axis, $periodic$ on the y-axis and $binary$ on the z-axis. [27] and [26] use orthogonal Walsh-Hadamard codes to acquire signals from multiple channels. [12], [69] and [70] are examples of conventional frequency division multiplexing (FDM) which lie at $\{periodic, continuous, continuous\}$. [68] acquires signals from a single input using pseudo-random binary sequences (PRBS) while the sampling frequency varies in a stochastic-cyclostationary fashion based on the input signal. Here, the carrier signal is statistically correlated to the input. Another example of a correlated chipping sequence with respect to the input-signal statistics is rakeness-based compressed sensing [10]. The carrier waveform can be either correlated or uncorrelated with the input signal. In standard compressed sensing, the input matrix is uncorrelated with the input signal characteristics [28].

4.3 Proposed design methodology

In this section, we propose a design method based on spread-spectrum modulation for multi-channel bio-signal acquisition. For a given number of channels, power consumption,

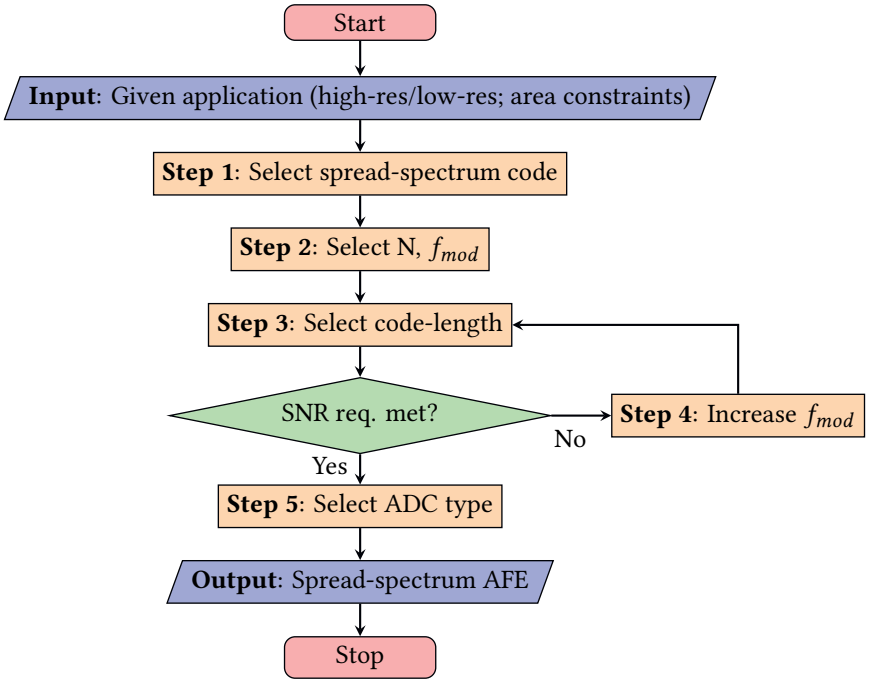


Figure 4.4: Design strategy for multi-channel spread-spectrum analog front-ends.

area, and application-derived performance requirements, the proposed design method can be carried out as illustrated in Figure 4.4. Starting with the target application as the input, the design strategy follows from 5 steps, as described in sub-sections 4.3.1 to 4.3.4, arriving at an optimal spread-spectrum AFE at the output. In sub-section 4.3.5, the proposed method is compared with other approaches. Finally, sub-section 4.3.6 illustrates the proposed design method on real pre-recorded AEGs.

4.3.1 Input: Application requirement

Based on the target application, one or more design parameters, such as power consumption, area, and resolution are more critical than the others. We consider two application cases of the acquisition of multi-channel AEGs here:

- Multi-channel PRBS codes for low-resolution recording.
- Multi-channel WH codes for high-resolution recording.

Multi-channel PRBS codes can, e.g., be used when we wish to track the propagation of the cardiac wavefront and generate an activation map [5], which requires only low-resolution and low-bandwidth signals. Multi-channel WH orthogonal codes can be used when we wish to acquire high-resolution signals for identification of detailed features of the AEG [74].

4.3.2 Step 1: Selection of codes

Based on the degree of periodicity from the proposed classification, modulation codes can be periodic, cyclostationary random or stationary random. Fig. 4.5 shows the time-domain and frequency-domain representations of periodic, cyclostationary, and stationary random codes, which are elaborated in the following paragraphs.

Periodic codes: An example of a periodic modulating signal (or square-wave signal) is conventional chopping, as shown in Fig. 4.5a where f_{ch} is the chopping frequency. Consider a periodic train of pulses characterized by amplitude ±A and a duration of τ. Let $v(t)$ be a periodic signal with period $T_{ch} = \frac{1}{f_{ch}}$ defined by,

$$v(t \pm mT_{ch}) = v(t), \quad -\infty < t < \infty \tag{4.5}$$

where m is an integer. The spectrum of a signal is computed using the Fourier integral. Since the integrability condition is not met, the Fourier integral cannot be directly computed [75]). To calculate the Fourier integral, the signal is truncated, and the range of integration over $\frac{-T_{ch}}{2} \leqslant t \leqslant \frac{T_{ch}}{2}$ is taken, where

$$v(t) = \left\{ \begin{array}{ll} A, & \text{for } |t| \leq \tau/2 \\ 0, & \text{for } |t| \geq \tau/2 \end{array} \right\}$$

The Fourier expansion is given by $v(t) = \sum_{n=-\infty}^{\infty} c_n e^{j2\pi n f_{ch} t}$, for $n = 0, 1, 2$, where $c_n = \frac{A\tau}{T_{ch}} sinc\{nf_{ch}\tau\}$. Note that, for periodic signals, the amplitude spectrum consists of a line spectrum where the lines have uniform spacing f_{ch}. By the Wiener-Khinchine theorem, the power of the signal is given by $P_v(f) = \sum_{n=-\infty}^{\infty} |c_n^2| \delta(f - nf_{ch})$.

Orthogonal codes such as WH codes also lie at $periodic$ on the degree of periodicity axis, as shown in Fig. 4.3. The WH transform is a non-sinusoidal orthogonal transformation technique that decomposes an arbitrary vector of dimension 2^m into a set of basis functions called Walsh functions, which are square or rectangular waves with values +1 or -1. It performs an orthogonal symmetric and linear operation on the input vector.

Spread-spectrum codes: Random codes can be used to spread the energy of the input signal to a larger bandwidth. For a random signal, the spreading bandwidth is infinite since an infinitely long sequence leads to a continuous spectrum. The PSD of a random signal $v(t) = \sum_{n=-\infty}^{\infty} a_n f(t - nT_{mod})$, where T_{mod} is the duration of 1 bit, is given by $P_v(f) = T_{mod}(sinc\pi f T_{mod})^2$ [76] as also shown in Fig. 4.5c. However, in practice, random code sequences are generated using pseudo-random generators since a replica of the code sequence is needed to recover the input signal. Pseudo-random binary sequences (PRBS) are cyclostationary, as shown in Figure 4.5c. A popular choice for implementing PRBS codes is employing linear feedback shift registers (LFSRs). In the design of an LFSR, the code sequences are replicated by choosing the same initial state and coefficients. Let $p(t)$ be a cyclostationary sequence that assumes an amplitude of 1 randomly at a rate of f_{mod} and the sequence repeats after code length L, given by the time period $T_0 = LT_{mod}$, where $T_{mod} = \frac{1}{f_{mod}}$, $L = 2^n - 1$, and n is the number of bits of the LFSR. $p(t) = \sum_k a_k q(t - kT_0), k \in Z$, $a_k \in [1, -1]$ is a cyclostationary sequence and $q(t) = \sum_{n=0}^{L-1} c_n s(t - nT_{mod}), c_n \in Z$ is a stationary random sequence whose length is given by L. Since the function $p(t)$ is periodic with

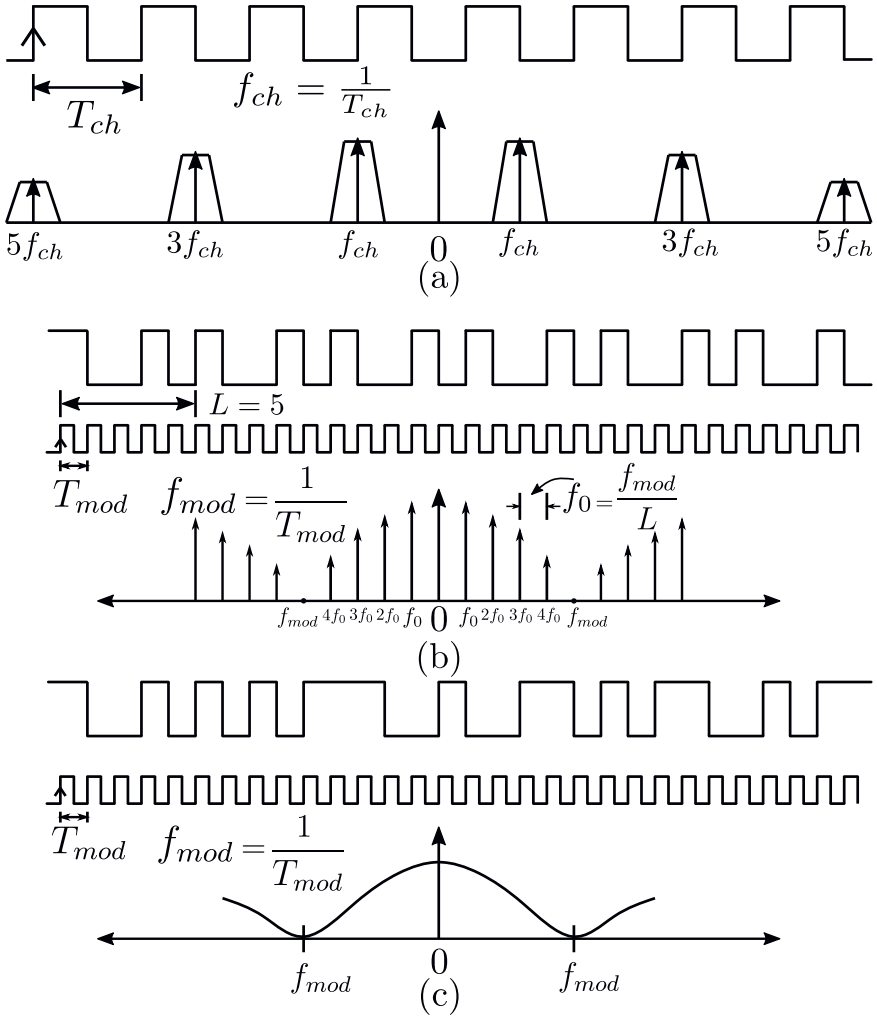


Figure 4.5: Time-domain and frequency-domain representation of modulation signals: a) Periodic; b) Cyclostationary random; c) Stationary random. f_{ch} and f_{mod} refer to the modulation frequency of periodic and (pseudo-) random signals, respectively.

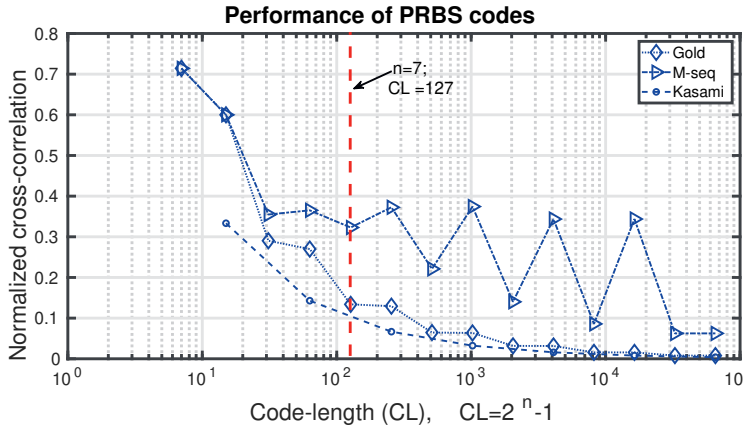


Figure 4.6: Theoretical limit of cross-correlation of PRBS codes. Note: Y-axis plots normalized cross-correlation (= ratio of peak cross-correlation to peak auto-correlation).

T_0, by the Wiener Khinchine theorem, the PSD is a line spectrum given by,

$$S_p(f) = \left[\sum_{m=-\infty}^{\infty} \delta(f - mf_o)\right] \frac{L+1}{L^2} \left(\frac{sin\pi f/f_c}{\pi f/f_c}\right)^2 + \frac{1}{L^2}\delta(f) \tag{4.6}$$

where $f_0 = \frac{1}{T_{mod}}$. An example with $L = 5$ is shown in Figure 4.5b.

Some examples of PRBS codes are maximum-length (ML) sequences, Gold codes, and Kasami codes, and they are used in communication systems to encode multiple signals. These codes are non-orthogonal and have varying cross-correlation properties, as shown in Fig. 4.6. The most important selection criterion in acquiring multiple biosignals is suppressing interference from other signals in the shared channel. The code length, L, is given by $L = 2^n - 1$, where n is an integer corresponding to the polynomial order used to generate the code. n is *odd* for ML, Gold, and *even* for Kasami codes. The peak auto-correlation is given by L. The peak cross-correlation values for Gold codes is given by $t(n)$, where $t(n) = 2^{(n+1)/2}$, m is odd; $2^{(n+2)/2}$, in case n is even; for Kasami codes, $t(n)$ is given by $2^{n/2} + 1$ [77–79]. Fig. 4.6 shows that the cross-correlation performance improves with increasing n bit (or L) for ML, Gold, and Kasami codes. Secondly, we can observe that for a given L, Kasami codes are optimal as they approach the Welch lower bound on peak cross-correlation [80]. However, the performance gap between Kasami and Gold codes reduces at higher values of L. Kasami codes offer marginal performance enhancement over Gold codes at the cost of higher implementation complexity. Thirdly, odd-order ML and Gold sequences offer lower cross-correlation performance than even-order.

4.3.3 Step 2,3: Selection of number of inputs and modulation frequency

In this sub-section, the number of inputs, N, the code length (L), and the selection of the modulation frequency, f_{mod}, are discussed. If the interfering signals are unknown

but have finite power, the input signal may overlap with the interferer. If the interferers are known (e.g., flicker noise), the input signal can be spread to a non-overlapping frequency band. In Figure 4.7, it can be seen that spread-spectrum modulation suppresses $\frac{1}{f}$ noise. As an example, in Figure 4.7a, a 3-bit PRBS code (L=7) with a modulation frequency f_{mod}=12.8 kHz is used to modulate and demodulate an input signal, f_{in}=0.108 kHz with a bandwidth f_b=0.4kHz. It can be observed that the $\frac{1}{f}$ noise reduces and the lowest tone f_0 is at $\frac{f_{mod}}{7}$=1.8kHz. Figure 4.7b shows the effect of L for varying values of the spreading gain G, given by: $G = \frac{f_{mod}}{f_b}$ on the SNR performance. At lower values of G, there is a marginal improvement of SNR even when the number of LFSR bits increases. For a given G, there is an optimal value of L at which the SNR is maximal. The peak shifts with increasing G. After the peak, the curve shows a decrease in SNR. This decrease is because the smallest tone given by f_0 is within the signal band, and some of the $\frac{1}{f}$ noise is in-band. A larger L implies a larger spreaded bandwidth. However, f_{mod} should be high enough to push f_0 beyond f_b. The two blue dashed lines show the minimum and maximum achievable SNR levels corresponding to with and without $\frac{1}{f}$ noise, respectively.

Impact of limited AFE bandwidth: The AFE is responsible for amplifying the entire spectrum, and it requires a minimum bandwidth equal to the modulation frequency, denoted as f_{mod}. If the amplifier's bandwidth is lower than f_{mod}, some of the signal will be lost and cannot be recovered. When using shorter code-lengths, a significant amount of information is lost at a given f_{mod}. On the other hand, increasing the code-length spreads the signal over a wider bandwidth, resulting in improved performance. However, when the code-length is large and f_0 falls within the signal bandwidth, the SNR performance drops which is clearly demonstrated in Figure 4.7c.

Multi-channel acquisition: For acquiring multiple inputs using a shared channel, the maximum number of inputs for a given n-bit LFSR is given by Euler's totient equation, $C = \frac{1}{N}\Pi\{P_i^{\alpha_i-1} \cdot (P_i - 1)\}$, where P_i are the prime factors of L and α_i is the power of the ith factor [81]. In Table 4.2, the acquisition performance is shown for N = 2, 4, 8, 16 and 32 for f_b=100 Hz and f_{mod}= 153.6 kHz. A smaller signal bandwidth allows for either (a) a smaller modulation frequency (f_{mod}) and thus a smaller amplifier bandwidth ($f_{BW,AFE}$) for the same code length (L) and number of channels (N), or (b) a larger L, and thus a larger signal-to-noise ratio (SNR), for the same f_{mod}, N and $f_{BW,AFE}$, or (c) a large N and a larger L for the same f_{mod}, SNR and $f_{BW,AFE}$. As given in the table, using a code-length of 127 (which can be generated by a 7-stage PRBS generator), the maximum SNR that can be achieved is 39 dB for a 2-input shared channel, given that the smallest tone (f_0) lies outside the signal bandwidth. For a shared channel, the maximum average SNR decreases with an increasing number of inputs. On the highlighted row in Table 4.2, for a 4-input channel, the maximum achievable SNR is 39 dB. If a higher average SNR is desired, it can be achieved by increasing f_{mod} and selecting a longer L.

4.3.4 Step 4, 5 Optimization of modulation frequency

The modulation frequency can be increased linearly to achieve higher performance at a corresponding code length. In Fig. 4.8, it is shown that for a 16-input shared channel, an

Table 4.2: Performance of PRBS codes on multi-channel acquisition

n	$L(=2^n\text{-}1)$	No. of codes	Avg. SNR (in dB)				
			N=2	N=4	N=8	N=16	N=32
3	7	2	16.90	-	-	-	-
4	15	2	23.52	-	-	-	-
5	31	6	29.82	27.16	-	-	-
6	63	6	35.98	33.32	-	-	-
7	127	18	42.07	39.40	38.14	36.27	-
8	255	16	48.13	45.46	44.18	42.31	-
9	511	48	54.16	51.49	50.21	48.35	43.91
10	1023	60	45.10	30.63	29.56	22.19	20.61
11	2047	176	31.73	29.23	24.95	21.87	17.87
12	4095	144	32.94	28.36	23.68	20.16	17.01
13	8191	630	30.94	26.42	23.17	19.53	16.67
14	16383	756	30.77	26.95	22.87	19.97	16.69
15	32767	1800	28.32	27.04	24.38	20.23	16.88
16	65535	2048	31.04	26.26	22.56	19.35	16.55

average SNR of 64 dB can be achieved by using a code-length of 2047 at a modulation rate of 572.8 kHz for a total signal bandwidth of 1.6 kHz (16 x 100 Hz). Also, it can be seen that using a 7-bit LFSR @f_{mod}=40.5 kHz, for 16 channels, the maximum SNR that can be achieved is 35.8 dB.

4.3.5 Comparison with other modulation techniques

In this sub-section, the requirements of PRBS modulation, WH modulation, and orthogonal frequency chopping are qualitatively compared in terms of bandwidth and area. Consider a signal bandwidth f_b, number of inputs N, and a code length = 128. For PRBS modulation, the minimum required modulation frequency is given by f_{mod} = 2 × 127 × f_b, with a maximum capacity of N = 18, whereas, for WH modulation, it is given by f_{mod} = 2 × 128 × f_b with a maximum capacity of N = 128. For orthogonal frequency chopping, the minimum required frequency is f_{mod} = 2 × 2^7 × f_b, with a maximum capacity of N = 7. So, for a given total bandwidth, WH modulation is most efficient, followed by PRBS codes and orthogonal frequency chopping. From a hardware viewpoint, PRBS codes are easy to generate since they require a few digital gates and consume negligible power and area [82]. The number of D flip-flops in a PRBS generator for a given L scales with $log_2(L)$. Implementing orthogonal codes requires look-up tables whose length scales with the power of 2 as the number of inputs increases. In practice, orthogonal codes have non-zero cross-correlation, as shown in [27]. In this work, we select Gold codes since they consume the least area for the required performance.

4.3.6 Illustration of the design method: validation on real pre-recorded AEG signals

The proposed technique is tested and validated without pre-processing on real pre-recorded atrial electrograms from the Erasmus Medical Centre, Rotterdam. Hospital recordings tend to be less clean (due to noise and interference) than synthetically modeled datasets or clean datasets available in public databases (e.g., MIT-BIH). The amplitude of AEGs varies from 1-10 mVpp depending on the size and the recording location in the heart. The signal bandwidth typically extends from 0.5 Hz to 200 Hz. The flexible electrode array contains 192 electrodes, each with a diameter of 0.45 mm and an inter-electrode distance of 2 mm [5]. Increasing the electrode diameter may lead to loss of spatial information while decreasing it will increase the electrode impedance. 16 sinus rhythm (SR) and atrial fibrillation (AF) AEG signals as shown in Figs. 4.9a - 4.9b are encoded using spread-spectrum codes, summed, and demodulated. Figures 4.9c - 4.9f show the performance of PRBS modulation using L=127 and 511, at f_{mod}=35 kHz and 140 kHz, respectively for SR (input 2) and AF AEG (input 2). AF exhibits a larger residual error than SR AEG, as seen in Figs. 4.9g-4.9h, due to significantly higher signal activity. SR exhibits a worse performance in certain parts of the segment than AF due to sharp peaks and loss of those peaks in the reconstructed signal. SR yields better average recovery at higher parameter settings than AF, as shown in Table 4.3. The effectiveness of PRBS and Walsh-Hadamard codes with different parameter configurations can be compared using the percentage root-mean-square difference (PRD), which quantifies the similarity between the original and reconstructed signal. A lower PRD value indicates better performance. The average PRD values are obtained by calculating over AEGs lasting 2 s and averaging over 16 inputs. For a bandwidth of f_b = 200 Hz and L = 127, the optimum modulation frequency is 70 kHz with mean PRD values of 10.8% and 13.1% for SR and AF, respectively. The PRD performance for SR and AF improves to 2.65% and 3.02%, respectively, when L = 511 and f_{mod} = 280 kHz. In this illustration, the optimal parameters for a given code length for PRBS and Walsh codes are shown in the highlighted row of Table 4.3. A marginal improvement in PRD performance is observed beyond the optimum f_{mod} for both PRBS and WH codes. The proposed technique was evaluated using PRBS codes on 4 inputs with a code length of 127. At f_{mod} = 35 kHz, the PRD performance for SR and AF improved to 4.7% and 3.1%, respectively, compared to higher values of 14.9% and 13.78% when 16 inputs were employed.

Table 4.3: Average PRD performance

Parameter setting				Average PRD (%)	
Type of code	No. of inputs	Code-length	Modulation freq.	SR AEG	AF AEG
PRBS	16	127	20 kHz	42.9	50.7
PRBS	16	127	35 kHz	14.9	13.78
PRBS	16	127	70 kHz	10.8	13.1
PRBS	16	127	140 kHz	10.7	13.1
PRBS	16	511	80 kHz	23.1	27.45
PRBS	16	511	140 kHz	6.2	3.6
PRBS	16	511	280 kHz	2.65	3.02
PRBS	16	511	560 kHz	2.5	3.01
Walsh	16	16	4 kHz	36.3	23.6
Walsh	16	16	8 kHz	6.9	1.2
Walsh	16	16	16 kHz	0.25	0.39
Walsh	16	16	32 kHz	0.1	0.2
PRBS	4	127	20 kHz	30.6	32.5
PRBS	4	127	35 kHz	4.7	3.1
PRBS	4	127	70 kHz	2.3	2.47
PRBS	4	127	140 kHz	2.3	2.4

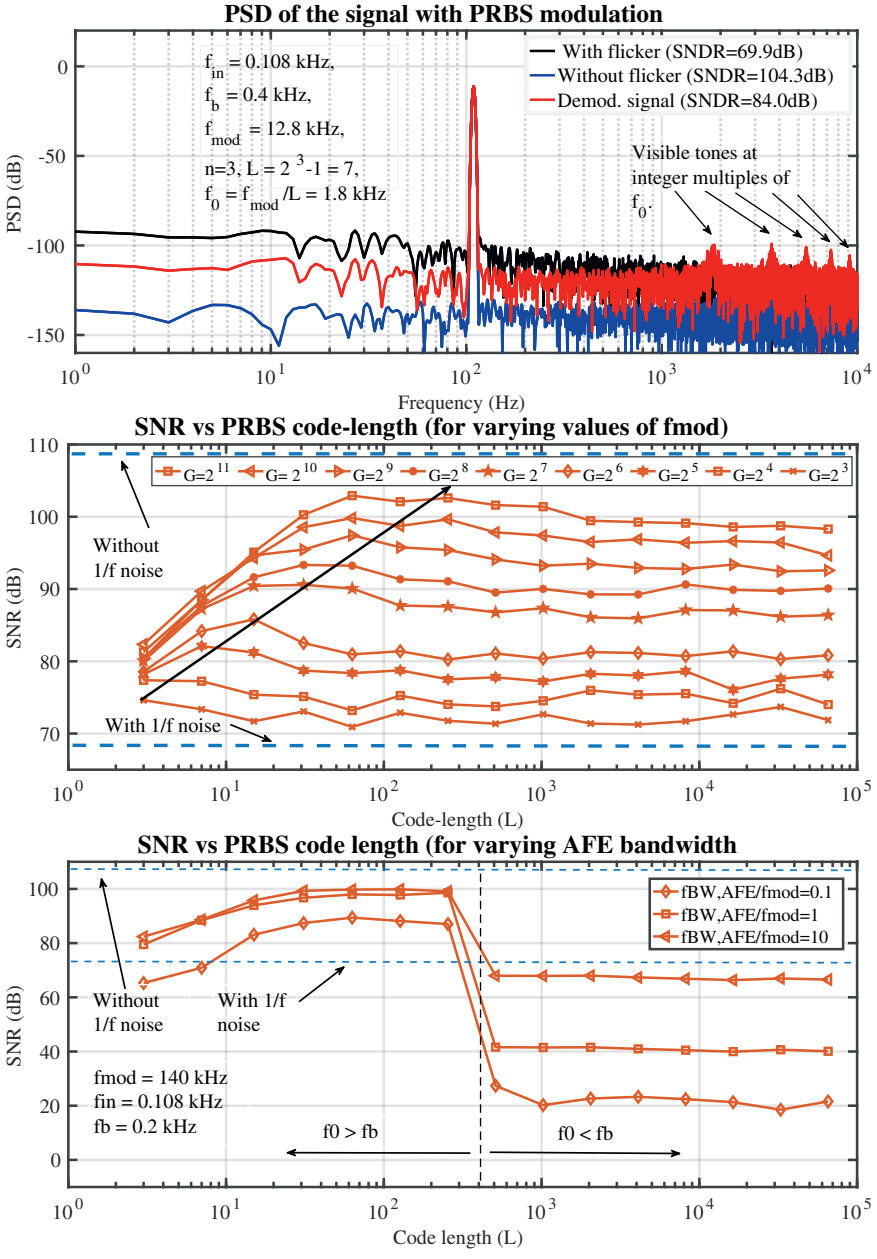


Figure 4.7: Single channel PRBS modulation. (a) PSD of a single channel modulated and demodulated with a 3-bit PRBS code. (b) Effect of spreading gain (G = $\frac{f_{mod}}{f_b}$). As G increases, f_0 (= $\frac{f_{mod}}{L}$) moves higher. (c) Effect of AFE bandwidth.

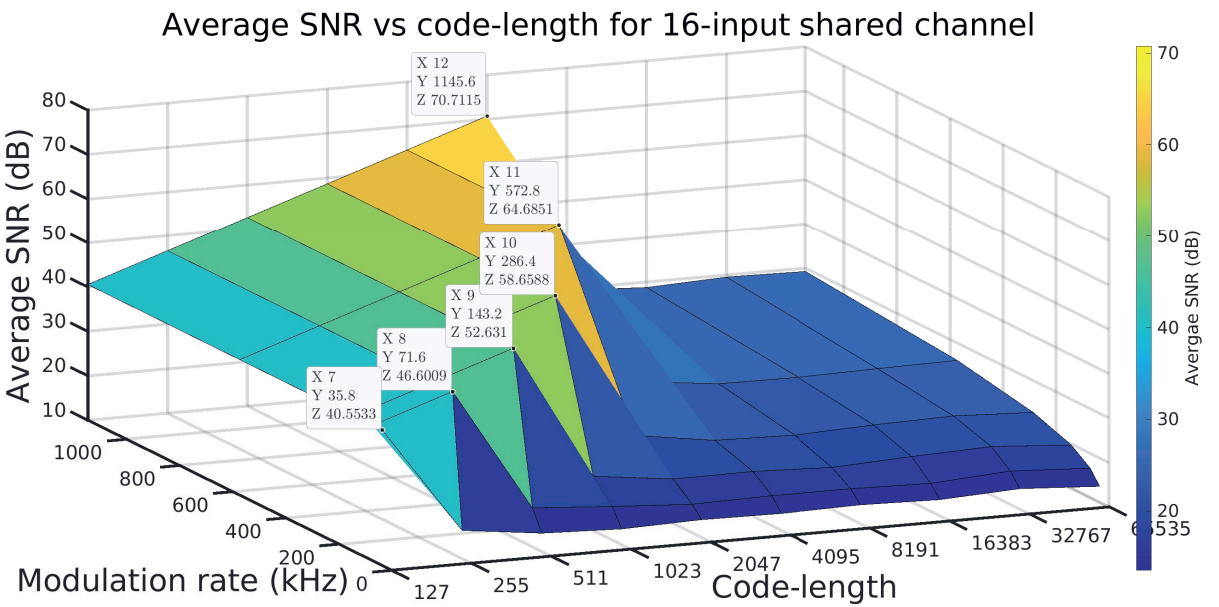


Figure 4.8: Multi-channel acquisition for 16-input shared channel with varying modulation frequency. The modulation frequency can be increased linearly to achieve higher performance at a corresponding code length.

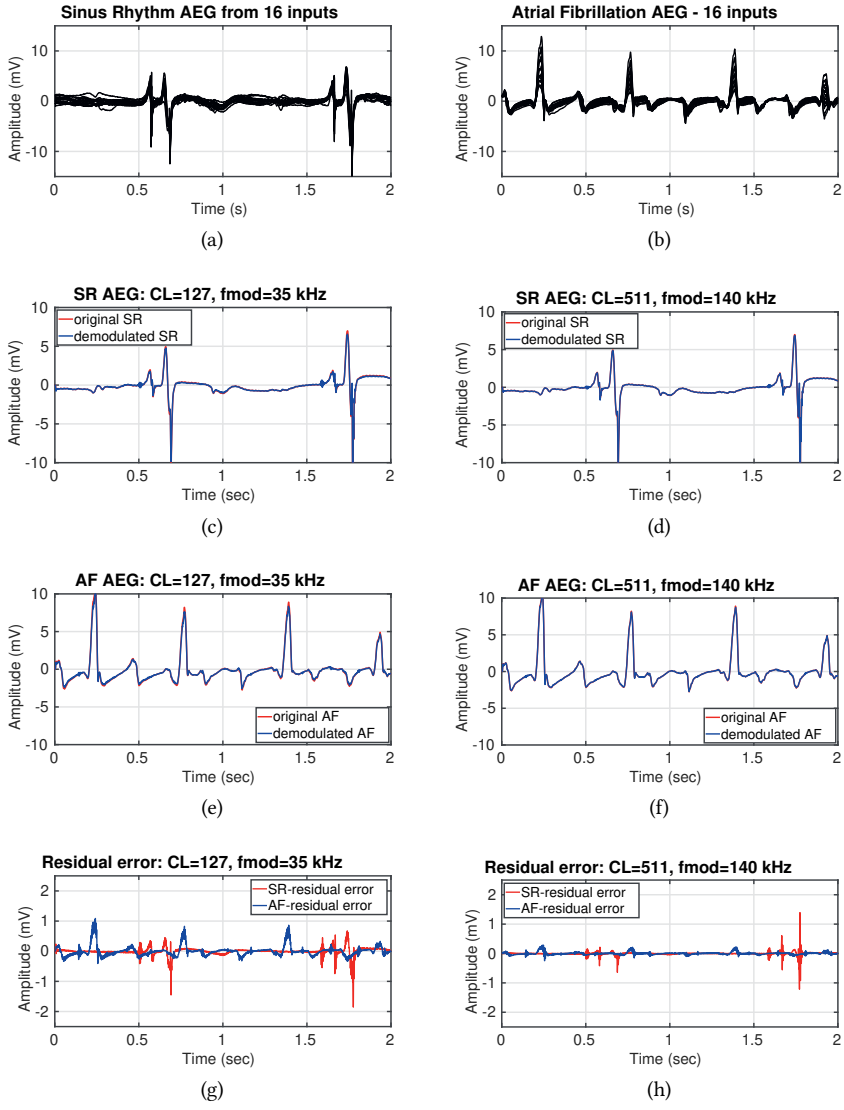


Figure 4.9: Validation of PRBS modulation on pre-recorded (a) SR and (b) AF AEGs from 16 inputs. Demodulated (c) SR and (b) AF AEG with L = 127, f_{mod}=35 kHz. Demodulated (e) SR and (f) AF AEG with L = 511, f_{mod}=140 kHz. Residual error given by the difference between original and demodulated signals for (g) L = 127, f_{mod}= 35 kHz and (h) L = 511, f_{mod}=140 kHz.

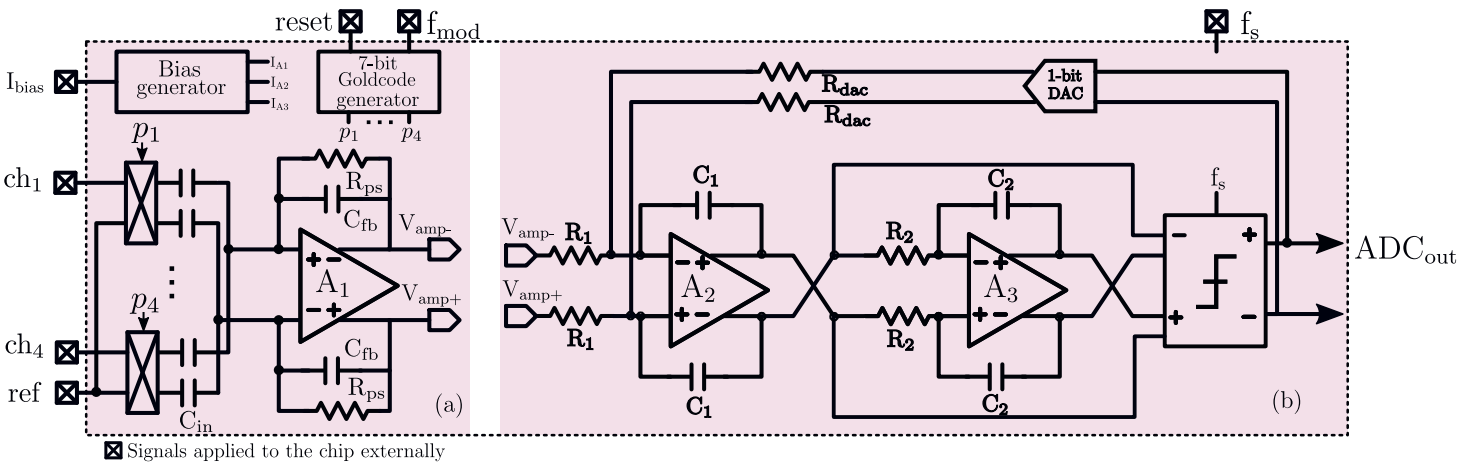


Figure 4.10: Circuit block diagram of the proposed architecture:(a) PRBS-modulated amplifier, (b) ΣΔ modulator.

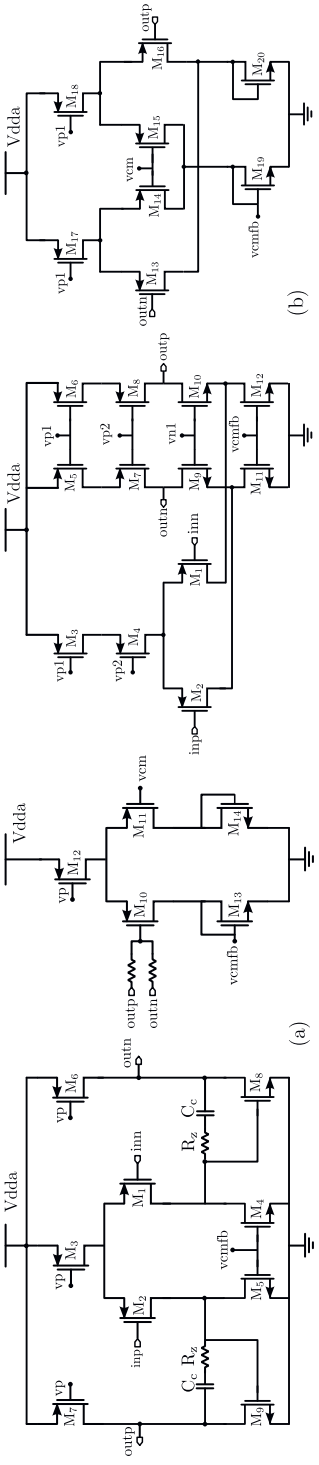


Figure 4.11: Schematic implementation: (a) 2-stage opamp (A1, A2) & CMFB, (b) Folded-cascode opamp (A3) & CMFB.

4.4 System architecture and circuit implementation

To validate the proposed design strategy for spread-spectrum acquisition of AEGs, a 4-input shared amplifier and a ΣΔ ADC are implemented in a standard 0.18 μm CMOS IC process. AEGs are unipolar recordings and the reference is shared across all the inputs. The reference electrode is large and its impedance does not add considerably to the total impedance seen by each channel. Mismatch between electrodes leads to negligible common-mode to differential-mode conversion as the input impedance of the front-end is much larger than the mismatch in electrode impedance. Each input utilizes a large off-chip decoupling capacitor to block any resulting DC offset due to the gold metal and cardiac tissue interaction. Figure 4.10 shows the block diagram of the proposed system architecture. Subsections 4.4.1 - 4.4.3 elaborate on the various blocks.

4.4.1 Analog front-end

Each channel consists of a modulator, a shared amplifier, and a shared ADC. The signals are multiplied by spread-spectrum codes p_i, i ∈ [1,4]. Input capacitances (C_{in}) convert the input voltage signals into currents. The summation of these currents takes place at the virtual ground node of the opamp. Four gain settings (G=4/8/16/32) are available for different input amplitude ranges (10/5/2.5/1.25 mVpp) corresponding to AEGs recorded on the epicardium. The gain settings are implemented by the ratio of capacitances C_{in} and C_{fb}. C_{in} is implemented as a variable capacitor bank (400fF, 800fF, 1.6pF, 3.2pF) with CMOS transmission gate (TG) switches controlled digitally. The modulator is implemented by four switches that are driven by a non-overlapping clock generator. The switch is implemented by a CMOS TG, which offers a higher linearity for large amplitude signals than NMOS or PMOS switches. The effective ON resistance of the switch of a TG is lower than that of an NMOS or a PMOS switch. The switches are sized optimally for lower ON resistance and lower charge injection. Off-chip capacitors are used with the flexible-electrode array to ensure patient safety. Since the electrodes are used directly on the surface of the heart and do not use gel, the expected DC offset level at the tissue-electrode interface is low. Therefore, this architecture does not employ a dedicated high-pass loop per channel to reject offset, which would otherwise saturate the amplifier [32].

The opamp is implemented by a two-stage Miller-compensated topology, as shown in Fig 4.11a. A two-stage opamp with continuous-time common-mode feedback (CMFB) is chosen to achieve high DC gain, high linearity, and to drive the input resistance of the ADC. The second stage is designed to meet the high signal-swing requirements for four inputs. To achieve lower $1/f$ noise, the first stage has a PMOS differential input pair biased

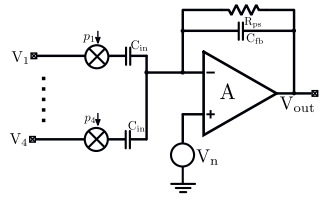


Figure 4.12: Noise analysis of an N-input spread-spectrum amplifier

in weak-inversion saturation. The simulated DC gain of the two-stage opamp is 100 dB. The AC bandwidth extends from sub-Hz to 150 kHz. Pseudo-resistors R_{ps} are implemented using PMOS transistors biased in weak-inversion triode and provide a DC path from the output to the input, thereby setting the input common-mode voltage equal to V_{cm}= (0.9 V). The total power consumption of the spread-spectrum amplifier, including biasing and CMFB is 23 μA from a 1.8 V supply, corresponding to 5.75 μA per input.

To ensure sufficient accuracy, the value of C_{fb} is chosen equal to 100 fF with a unit capacitance of 50 fF. Higher values of C_{fb} would lead to higher C_{in} values for the given gain settings and thus lower impedances. For 4 inputs and a 7-bit Gold-code generator, a modulation frequency of 16 kHz or 32 kHz is sufficient. For f_{mod} = 35 kHz and L=127, the tones lie between 32 kHz and 251 Hz ($f_0 = \frac{32kHz}{127}$). The input capacitance C_{in}, combined with the mixer switch driven by modulation frequency f_{mod}, forms an impedance Z_{in} given by $1/(2f_{mod}C_{in})$. Assuming a maximum capacitance of C_{in} = $3.2pF$, the worst-case impedance ranges from 4.9 MΩ to 622 MΩ for f_{mod} and f_0, respectively.

From Fig. 4.12, the signal and noise gain of an N-input spread-spectrum amplifier can be written as:

$$V_{sig} = V_{in}(-\frac{C_{in}}{C_{fb}}); \tag{4.7}$$

$$V_{n,out} = V_n(1 + \frac{N \cdot C_{in}}{C_{fb}}) \tag{4.8}$$

The input-referred noise is N times higher for an N-input amplifier as compared to a single-channel amplifier. On the other hand, N times more power can be spent on this single N-input amplifier, which results in an equal noise contribution per channel of both an N-input amplifier and N single-channel amplifiers. In other words, if N single-channel amplifiers each consume $1/N$ times the power of the multiplexed amplifier, the total input-referred noise is the same in both situations. Note that flicker noise is suppressed if the signal is modulated before the amplifier.

4.4.2 ΣΔ ADC

For digitizing the modulated and summed signal inputs, a continuous-time ΣΔ modulator is implemented for its inherent anti-aliasing property. For the target application, there is a need to minimize the number of outgoing wires. Other ADCs, such as SAR have the number of outputs equal to the number of bits. Additional circuitry, such as an SPI, is required to reduce the number of outgoing wires, which might consume more area and power. For a total input bandwidth of 32 kHz and a resolution of 10 bits, a 2^{nd} order orthonormal feed-forward topology low-pass ΣΔ ADC [32] designed to operate at 7.8 MHz is selected for its optimal performance. The integrators are implemented using opamp-RC filters due to their high linearity. Alternative implementations such as g_mC integrators are more power-efficient as compared to opamp-RC integrators; however, they offer poorer linearity.

The performance of the modulator is determined by the first integrator stage. The errors originating in the second integrator and the following blocks are suppressed by the gain of the preceding blocks. For lower noise, a smaller input resistance (< 300 kΩ) can be chosen. For a given integrator constant, for lower noise, a larger capacitance value is

required, leading to a higher opamp power consumption. To reduce the loading of the previous stage and trading noise for lower power, R_1=R_2= 512 kΩ and C_1=C_2= 0.5 pF have been chosen. The common-mode voltage is at VCM=0.9 V. R_{dac} is chosen as 256 kΩ. The non-idealities of the integrator performance are simulated through behavioral simulations. To minimize the effect of finite DC gain and GBW on the performance of the modulator, a DC gain > 85 dB and GBW > 0.7 x f_s or 5 MHz would be sufficient. The impact of time-constant (RC) variations of the integrators is also modeled. For a variation up to ±30%, there is a slight degradation in the performance. However, beyond ±40%, the performance degrades significantly and may even become unstable. To achieve a high DC gain and high output swing, A_2 is implemented by a 2-stage opamp and A_3 by a folded-cascode opamp as shown in Fig. 4.11. A 1-bit comparator quantizes the signal, and a 1-bit DAC with four switches is implemented for its inherent linearity. To implement the 1-bit comparator and the summer, a multi-input two-stage dynamic comparator is implemented for its power efficiency. Its first stage provides amplification and is followed by a latching stage.

4.4.3 Generation of spread-spectrum codes

The PRBS codes are generated by a 7-stage Gold-code generator using two LFSRs, generating up to a maximum of 18 codes (See Table 4.2). Four of these codes are required to modulate four inputs. Each LFSR has 7 delay flip-flops (DFF). At the start of the acquisition, all the outputs are cleared to 1 through a reset signal. The DFFs consume negligible area and power compared to the rest of the circuitry. For an increasing number of input signals, the area occupied by the WH code generator increases exponentially, whereas for PRBS codes, the area of the corresponding generator increases by a few more gates.

4.5 Measurement results

The prototype has been implemented in a standard 180 nm CMOS technology. Fig 4.13 shows the die photograph with a total chip area of about 5.12 mm ^{2} (3.2 mm x 1.6 mm), including the test structures and the IO ring. Fig 4.14a-b show the area and power breakdown, respectively. A programmable-gain amplifier, a Gold-code based PRBS generator, and a 2nd order ΣΔ modulator with a single outgoing wire is integrated for amplifying,

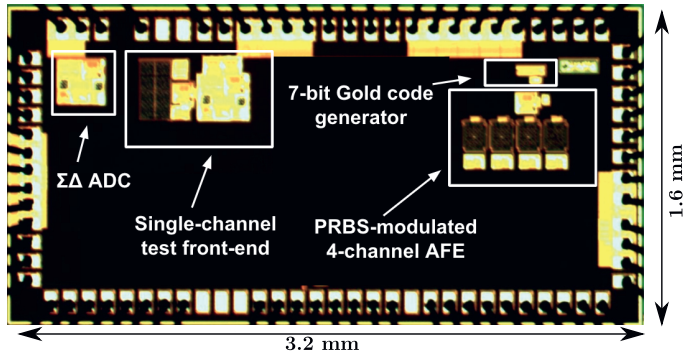


Figure 4.13: Chip microphotograph

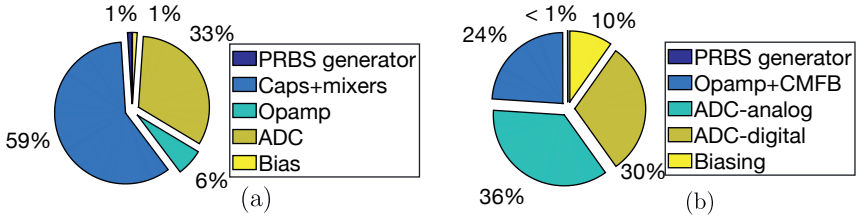


Figure 4.14: (a) Area and (b) Power breakdown.

Table 4.4: Measured performance of 2nd order ΣΔ modulator

Parameter	Specification
Process	180 nm CMOS
Supply voltage	1.8 V
Current	36.3 μ A
Bandwidth	16 kHz
Sampling frequency	7.8 MHz
SNDR	57.8 dB @ 16 kHz/50 dB @ 32 kHz
Dynamic range	68 dB
Walden FOM	0.87 pJ/conv.
Area	$0.09 mm^2$

digitizing, and reading out cardiac signals. The proposed PRBS-modulated multi-channel amplifier and ΣΔ ADC, including biasing, operate from 1.8 V and draw 91.9 μA. The PRBS-modulated multi-channel amplifier, PRBS generator, and ADC occupy only 0.27 mm^2.

Fig. 4.15 shows the performance of the ADC. It achieves a peak SNDR of 57.8 dB measured at f_{in}= 5 kHz and V_{in}@-2.4 dBFS), for a bandwidth of 16 kHz. For input signals lower than -52 dBFS, the curve is extrapolated. As the input amplitude approaches its maximum limit, the curve becomes flatter, but it remains stable [32]. The overall performance is summarized in Table 4.4. Fig. 4.16 shows the input-referred noise spectrum of the amplifier characterized by using a dynamic signal analyzer (SR785, Stanford Research Systems) capable of capturing low-frequency behavior from 100 mHz. It shows the measured input referred noise before and after demodulation with f_{mod} = 5 kHz. The noise floor is flat down to 1 Hz, showing that $1/f$ noise is removed using PRBS modulation. The integrated noise for a bandwidth of 39 Hz is about 1.4 μVrms. The thermal noise density is at 224 nV/sqrt(Hz). Fig. 4.17 characterizes the PRBS-modulated amplifier at f_{mod} = 5 kHz, 10 kHz and 32 kHz. For an f_{mod}@5 kHz, the lowest tone, f_0 is given by $\frac{5kHz}{127}$, i.e., 39 Hz, which sets the maximum usable bandwidth, whereas, @10 kHz and 32 kHz, it occurs at 78 Hz and 251 Hz, respectively, as shown in Fig. 4.17a. It can be seen that the noise floor is higher for higher values of f_{mod}. Charge injection and clock feed-through associated with the MOSFET switches of the input chopper give rise to significant chopper noise. The magnitude of chopper noise increases proportionately with the modulation frequency, as observed and described in [83] and [84].

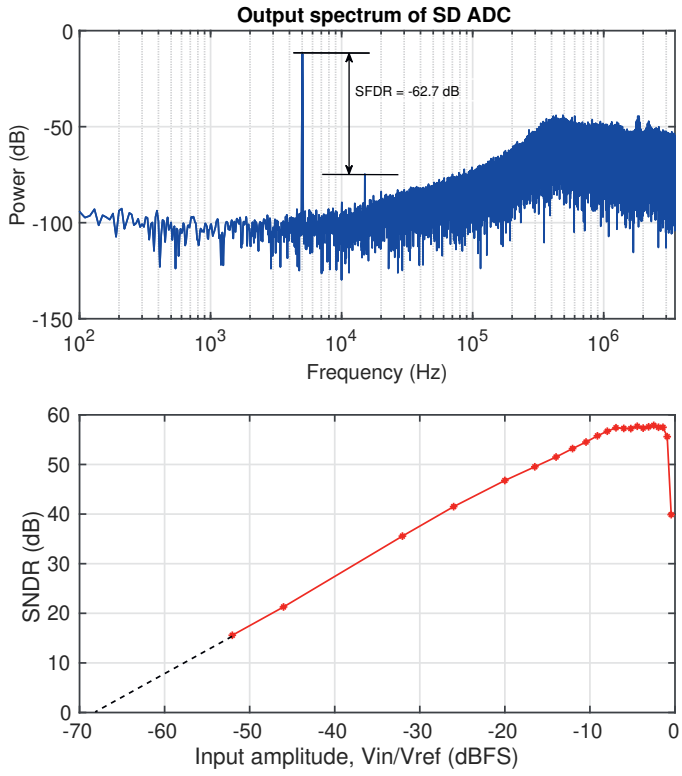


Figure 4.15: Measured ΣΔ modulator performance (a) PSD plot for -2.4 dBFS input signal at 5 kHz (b) SNDR versus the input signal amplitude.

In order to test the performance of the prototype, each of the channel inputs is simultaneously stimulated with a 5 mV_{pp} single-tone sinusoidal signal with a unique frequency, i.e., 15 Hz, 17 Hz, 21 Hz and 25 Hz at a gain of 4 and modulated at 10 kHz. The Gold codes are already known since the initial state of the DFFs is set to 1. For synchronization with the replica of the codes at the receiver end, one of the outputs of the generator is read out. A custom synchronization script is then used to reconstruct the other codes based on the known code sequence at 10 kHz. The combined output is read out from the chip. Post-processing carried out on MATLAB involves demodulation using replicated codes and filtering with a 10^{th}-order digital low-pass filter (LPF) on the receiver side. Using a lower-order filter such as a 2^{nd}- or a 3^{rd}-order LPF results in lower performance, as also shown in [26]. In Fig 4.18, the measured performance is compared with the results obtained from MATLAB simulations. With a 7-bit Gold-code generator (L = 127), the maximum achievable crosstalk performance is -40 dB, as shown in Fig. 4.18b. In Fig. 4.18a, the measured crosstalk performance varies between -32 dB and -40 dB depending on the Gold codes. The degradation in crosstalk performance in the practical setup can be attributed to non-zero cross-correlation between the codes and the use of a shared reference [85]. PRBS modulation upmodulates flicker noise and offset to the tones at f_0, $2\times f_0$ ... f_{mod}. For large

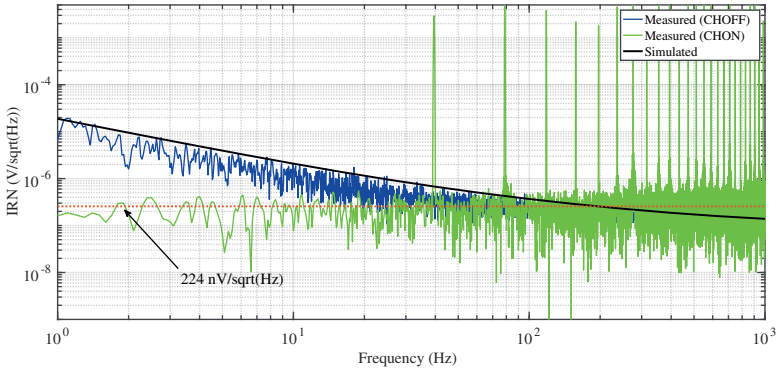


Figure 4.16: Input-referred noise with PRBS modulation ON/OFF.

circuit offset, the tones are larger. In Fig. 4.18b, the tones present between 40 Hz and 78 Hz are intermodulation tones. The intermodulation tones result from the interaction between the signal inputs and the modulation frequency. The inputs at 15 Hz, 17 Hz, 21 Hz, and 25 Hz result in intermodulation tones at 63 Hz, 61 Hz, 57 Hz, and 53 Hz due to f_0 tone at 78 Hz. The low-pass filter attenuates the input frequencies closer to its cut-off frequency (ch3 and ch4) due to its 10^{th} - order roll-off. The slight variation in amplitude between ch1 (-40.4 dB) and ch2 (-40.1 dB) could be attributed to a mismatch in gain between the channels. Fig. 4.19 shows the recovered inputs in the time domain.

Table 4.5 presents a summary of the proposed system performance and a benchmark with state-of-the-art modulation approaches for multi-channel recording systems. The proposed system is designed for acquiring unipolar atrial electrograms with a shared reference. Compared with systems that use orthogonal codes such as [27], which requires look-up tables (or on-chip memory), the proposed system includes an integrated PRBS generator, which consumes negligible power and area. Also, the number of bond pads/input in the proposed approach is 1×, whereas other implementations such as [27], [62] or [26] use 2× the number of inputs. Compared to [12] and [62], the proposed system consumes less area/channel. The proposed method is attractive for applications with strict area constraints for low-resolution signal acquisition, such as wavefront mapping.

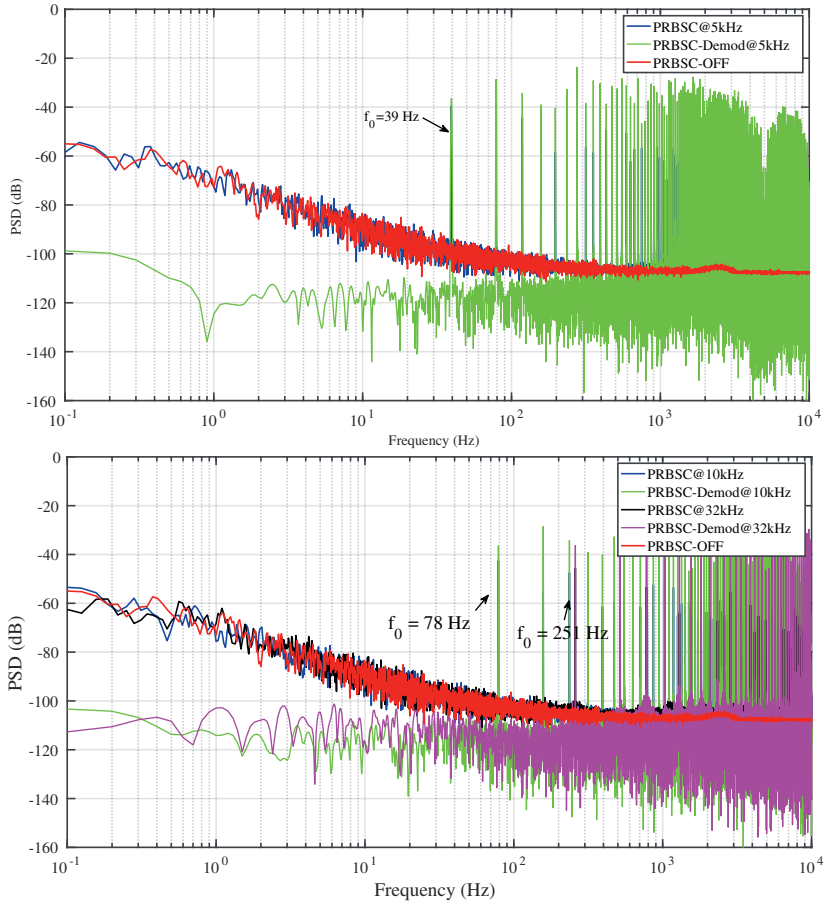


Figure 4.17: Measured input-referred noise using PRBS modulation. (a) f_{mod} = 5 kHz, (b) f_{mod} = 10 kHz, f_{mod} = 32 kHz.

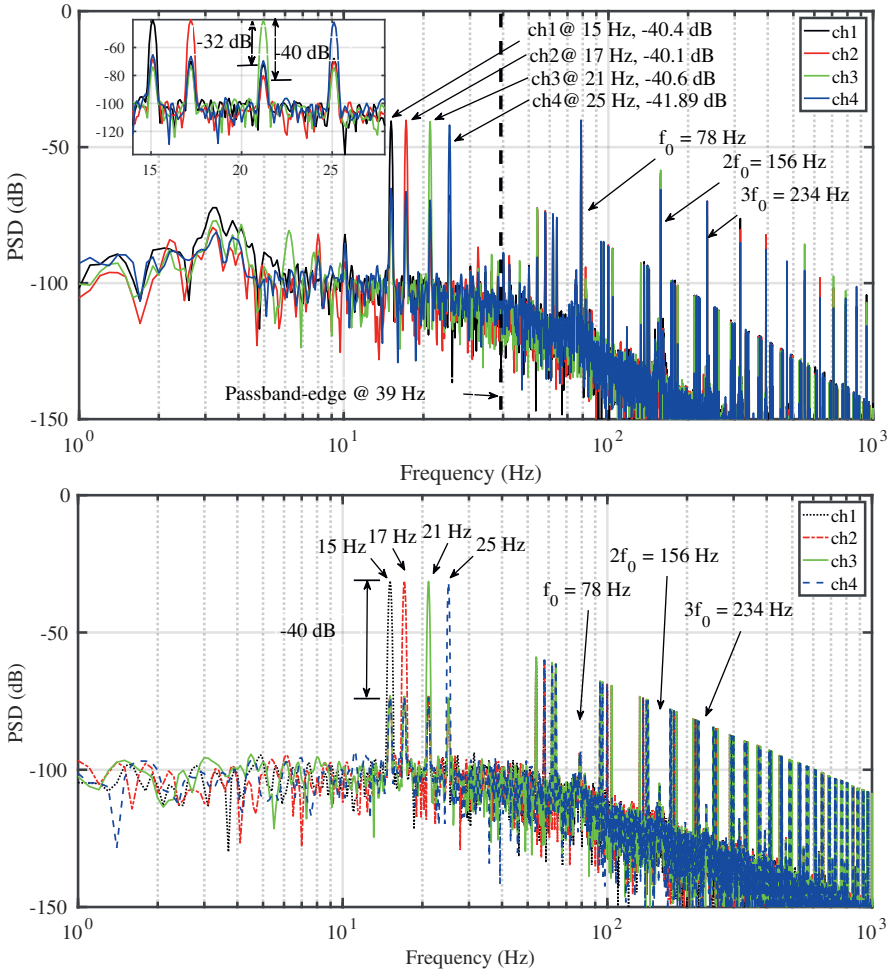


Figure 4.18: (a) Measured spectrum of the demodulated and filtered signals upto a bandwidth $f_0/2$ at a modulation frequency of 10 kHz using a 2nd order digital low-pass filter; (b) Simulated spectrum on MATLAB.

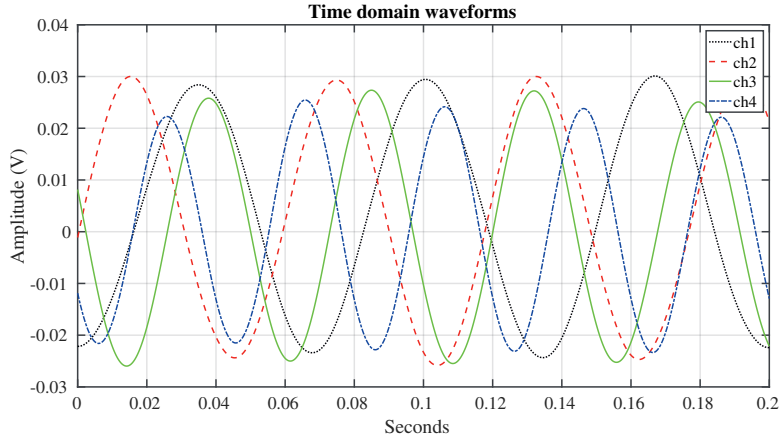


Figure 4.19: Time-domain waveforms of the demodulated and filtered signals upto a bandwidth $f_0/2$ at a modulation frequency of 10 kHz using a 10^{th}-order digital low-pass filter.

Table 4.5: Comparison with modulation approaches for multi-channel systems

	JSSC'20 [27]	TCAS'21 [26]	TBCAS'19 [12]	TVLSI'19 [62]	This work
Modulation/Mutliplexing	WH/CDM	WH/CDM	FM/FDM	OFC/CDM	PRBS/CDM
Type of biosignal	EMG	EEG	EEG	ECG	AEG
Type of recording	Bipolar	Bipolar	Unipolar	Bipolar	Unipolar
Reference electrode	Dedicated	Dedicated	Shared	Dedicated	Shared
Look-up table required	Yes	Yes	No	No	No
Bondpads/input	2	2	1	2	1
No. of channels	15	4	4	2	4
Shared blocks	LNA,ADC	ADC	ADC	LNA	LNA,ADC
ADC architecture	Async.	SAR	SAR	-	$\Sigma\Delta$
Serializer	Yes	Yes	Yes	No	Yes
Wirecount ratio	15:1	4:1	4:1	1:1	4:1
Current/channel (uA)	9.2	1.5	190	0.36	20.7
Noise density $\frac{nV}{\sqrt{Hz}}$	155	95.9	63	130	224
LNA Gain (dB)	40-56	45.3	-	40	12-30.1
Area/ch (mm^2)	0.019	0.08	1	0.34	0.067
Process (μm)	0.18	0.18	0.35	0.13	0.18

4.6 Conclusions

This chapter proposes a novel design strategy to develop optimal spread-spectrum analog front-ends. A structured classification of modulation strategies orthogonalized by their degrees of freedom is proposed to identify possible techniques for acquiring analog signals. The proposed design method is validated by implementing a 4-input PRBS modulated spread-spectrum recording system in a $0.18\mu m$ CMOS process, which consists of a shared amplifier, a shared $\Sigma\Delta$ ADC, and an on-chip Gold code generator occupying 0.067 mm^2 and consuming 23 μA per channel input.

5

Compressed-sensing of atrial electrograms for the detection of AF

Atrial electrograms (AEGs) acquired with a high spatio-temporal resolution are a promising approach for early detection, analysis, and understanding of the electropathology underlying atrial fibrillation. Due to the high data rate, transmission of AEG signals is expensive in terms of power consumption and resources, making its adoption a challenge for low-power wireless devices. In this chapter, we investigate the feasibility of using compressed sensing (CS) for the acquisition of AEGs while reducing redundant data without losing information. We apply two CS approaches, standard CS and rakeness-based CS (rak-CS), on a data set composed of real AEG recordings. We find that the AEGs are compressible in time and, more interestingly, in the spatial domain. The performance of rak-CS is better than standard CS, especially at higher compression ratios (CR), both during sinus rhythm (SR) and atrial fibrillation (AF). The difference in the achieved average reconstruction signal-to-noise ratio (ARSNR) in rak-CS and standard CS, for CR = 4.26, in the time domain is 7.7 dB and 2.6 dB for AF and SR, respectively. Multi-channel data is modeled as a multiple-measurement-vector problem, and the mixed norm is used to exploit the group structure of the signals in the spatial domain to obtain improved reconstruction performance over l_1 norm minimization. Using the mixed-norm recovery approach, for CR = 4.26, the difference in achieved ARSNR performance between rak-CS and standard CS is 5 dB and 2 dB for AF and SR, respectively.

To validate the usability of the reconstructed signals, the quality of the signals is evaluated by a team of clinical experts. Upto CR = 4.25, the signals are generally clean and useful. The visual performance of SR AEG is much better than AF AEG, as also observed in the quantitative analysis. Using rak-CS, at CR = 4.26, the percent root mean square difference for SR is 7.1 %, whereas, for AF, it is 9.2 %.

This chapter is partly based on S. Rout et al. Rakeness-based compressed sensing of atrial electrograms for the diagnosis of atrial fibrillation, *ISCAS 2019* [10] and S. Auerbach, W. A. Serdijn, and S. Rout. Compressed-sensing of spatiotemporally-correlated and/or rakeness-processed electrograms. *US Patent App. 16/846,551* [60].

5.1 Introduction

About 17.9 million individuals die from cardiovascular diseases (CVDs) annually [1]. In order to have better treatment alternatives, it is necessary to diagnose patients with cardiac abnormalities early on. One of the ways to diagnose abnormalities is by recording electrophysiological signals, which has been the gold standard for detecting and treating heart diseases. While ECG records on the surface of the heart and can only offer a very coarse look at the heart's health, atrial electrograms recorded on multiple electrode sites are used to obtain a high-resolution wavefront map to track the conduction pathways in the heart. However, using several hundred recording sites generates a massive amount of data. In order to reduce the data rate, compression algorithms are used. This chapter describes compressed sensing techniques applied to atrial electrograms during sinus rhythm and atrial fibrillation.

This chapter is organized as follows. Section 5.2 presents the performance of rakeness-based CS and standard CS on atrial electrograms. For validating the usability of the compression technique, the reconstructed signals are evaluated by a team of clinical experts, and the results are presented in Section 5.3. Section 5.4 presents similarity analysis, which quantifies the performance of compressed sensing in terms of average reconstruction signal-to-noise ratio and percent root-mean-square difference. Section 5.5 presents the conclusions of the chapter.

5.2 Rakeness-based compressed sensing of atrial electrograms for the diagnosis of atrial fibrillation

5.2.1 Introduction

Atrial electrograms (AEG) are a class of signals that are recorded on the surface of the heart. Contrary to electrocardiogram (ECG), which is recorded on the surface of the human body, the AEG has the potential to offer deeper insights into the signal propagation in the heart, specifically the atria, located in the upper part of the heart. AEGs can be used to study the progression of atrial fibrillation (AF), a cardiac abnormality of the atria. Irregular R-R intervals [18] and the absence of P-waves characterize AF in an ECG recording. Although characterization of AF in AEGs is not straightforward, it is usually identified with irregular and rapidly varying signals. The phenomena governing the propagation of the wavefront during AF is poorly understood, and the current understanding is limited due to the lack of efficient high-resolution mapping systems [14, 86].

In comparison to recording ECG signals, AEGs are acquired with a high-resolution multi-electrode two-dimensional array, which requires unbounded and continuous acquisition, storage, and transmission of a large amount of data. Due to the data-intensive nature of the acquisition of AEGs, developing portable devices for continuous monitoring in the clinical setting is challenging. In particular, for the early diagnosis of AF and understanding of the complex spatio-temporal behavior of the signals recorded on the surface of the heart, both during sinus rhythm (SR) and atrial fibrillation (AF), there is a need for high-resolution data acquisition system. The acquisition and transmission of high-resolution data poses a constraint on the power consumption. A system-level diagram of the acquisition of the AEGs is shown in Figure 5.1, where the signals are recorded using a flexible electrode array and a recording module and transmitted to a base station

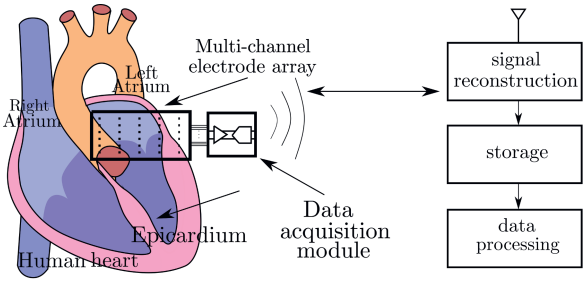


Figure 5.1: System-level diagram of the acquisition of atrial electrograms.

for further processing. With a minimum interelectrode distance of 2 mm, at least 1728 recording sites are required to cover the entire atrium, which includes the right atrium, the left atrium, and Bachmann's bundle [5]. For recording signals from 1728 electrodes at a resolution of 16 bits and a sampling frequency of 10 kHz, the total data rate required is $16 \times 10^3 \times 1728$, or 276 Mbit/s, resulting in $\approx$ 16.8 Gbit/min. The acquisition and processing of such a large amount of data for a portable device is a practical challenge due to the needed power and memory requirements.

One of the innovative points of our work is to investigate the compressibility of a new class of signals, i.e., AEGs, both in the time and the spatial domain. Compressed sensing (CS) is a relatively recent paradigm that allows simultaneous acquisition and compression of a signal by means of sampling it below the Nyquist rate. In the state-of-the-art literature, CS has been successfully applied to various bio-signals, such as ECG, EMG, and EEG [28–30, 87], thanks to the property of these signals to be inherently sparse in a certain domain. In details, we will investigate the sparsity properties of the AEG signal and compute the expected CS performance with varying compression ratios. In this section, we will focus both on single-channel compression in the temporal domain and on multi-channel compression by exploiting the expected similarity among the signals coming from adjacent leads. In Section 5.2.2, the compressed sensing approach for single-channel and multi-channel AEG signals is explained. In Section 5.2.3, the performance evaluation of the proposed approach is described. Finally, the conclusions are summarized in Section 5.2.4.

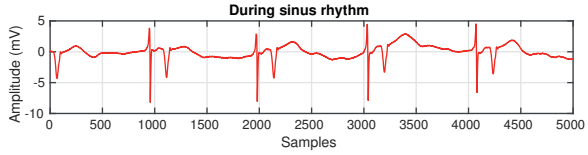
5.2.2 Compressed sensing

Single channel compressed sensing

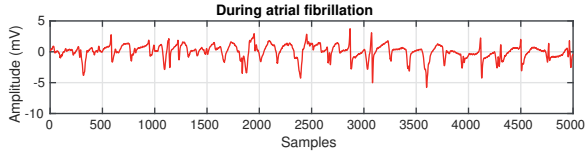
Compressed sensing is a method for sampling and reconstruction of signals that are known to be sparse in some basis [88, 89]. An input signal x recorded from a single electrode, represented in an N-dimensional vector space, which is sparse in a certain basis and acquired with a sensing matrix Φ, can be formulated as a single-measurement-vector (SMV) problem. The measurement vector y obtained can be written as

$$y = \Phi x + n \tag{5.1}$$

where $y \in \mathbb{R}^M$, $\Phi \in \mathbb{R}^{M \times N}$, $x \in \mathbb{R}^N$and $n \in \mathbb{R}^M$ is the measurement noise, modeled as additive white Gaussian noise in the temporal domain. Given that signal x is K-*sparse* in



(a)



(b)

Figure 5.2: Time-domain waveforms of (a) Sinus rhythm, and (b) Atrial fibrillation (Data courtesy of Erasmus Medical Center, Rotterdam).

an arbitrary basis $\Psi = [\psi_1, \psi_2 ..., \psi_N]$, $\psi_i \in \mathbb{R}^{N \times N}$, x can be represented as

$$x = \Psi \alpha \tag{5.2}$$

where α is an N-dimensional vector with only $K \ll N$ non-zero elements in matrix Ψ. K and N are related by *sparsity* which is given by $(1 - K/N) \times 100\%$. From the compressed measurement samples, the signal can be reconstructed by solving the minimization problem given by

$$\hat{\alpha} = \arg \min_{\alpha} \|\alpha\|_1 \quad \text{subject to} \quad y = \Phi \Psi \alpha \tag{5.3}$$

where $\|\alpha\|_1$ is the l_1 norm of the signal. Further, the reconstructed input signal is given by $\hat{x} = \Psi \hat{\alpha}$.

Standard CS only accounts for the sparsity of a signal in an arbitrary basis. However, for a proper class of signals, it is possible to exploit the signal energy distribution, i.e, the localization [90], to improve the performance of the CS reconstruction. The localization of the signal energy in a certain basis leads to the rakeness-based approach which incorporates the input signal second-order statistics in the design of the measurement matrix. The idea is to increase the average energy (information) of the measurement vector elements by a soft adaptation of the statistics of the rows of Φ to the correlation matrix characterizing the class of acquired signals having, as a consequence, a reduction in the reconstruction error $||x - \hat{x}||_2$ after the solution of (5.3). Rakeness ρ between two processes Φ and x can be defined as [90, 91],

$$\rho(\Phi, x) = \mathbf{E}_{\Phi,x} \left[\left| \langle \Phi, x \rangle \right|^2 \right] \tag{5.4}$$

where $\mathbf{E}_{\Phi,x}$ refers to the expectation with respect to the two processes and ρ maximizes the signal energy.

Multi-channel compressed sensing

Consider a 2-D array of L electrodes where the signal $\mathbf{X}$ is acquired from various channels with a sensing matrix Φ and the measurement matrix $\mathbf{Y}$ can be described as

$$\mathbf{Y} = \Phi\mathbf{X} + \mathbf{n} \tag{5.5}$$

where $\mathbf{Y} \in \mathbb{R}^{M\times L}$, $\Phi \in \mathbb{R}^{M\times N}$, $\mathbf{X} \in \mathbb{R}^{N\times L}$ and $\mathbf{n} \in \mathbb{R}^{M\times L}$ is the measurement noise, modeled as spatio-temporally white Gaussian noise. Here, $\mathbf{X} = [x_1, x_2, \ldots, x_L]$, where x_j is the signal acquired from the j-th electrode. Let $\mathbf{A} = [\alpha_1, \alpha_2, \ldots, \alpha_L]$ be a matrix composed from a sparse representation of vectors $[x_1, x_2, \ldots, x_L]$, with $x_j = \Psi\alpha_j$, $j = 1, 2, \ldots L$ or, with a more compact notation, $\mathbf{X} = \Psi\mathbf{A}$.

The multi-channel atrial electrograms share similarities among the adjacent channels, which can be exploited for an improved reconstruction performance. Multi-channel CS acquisition can be formulated as a multiple-measurement-vector (MMV) problem and can be solved with jointly sparse recovery algorithms [92]. The aim of MMV compressed sensing is to recover the jointly sparse $\mathbf{A}$, which can be formulated as [93]

$$\hat{\mathbf{A}} = \arg\min_{\mathbf{A}} \|\mathbf{A}\|_{1,2} \quad \text{subject to} \quad \mathbf{Y} = \Phi\Psi\mathbf{A} \tag{5.6}$$

where the joint *sparsity* in $\mathbf{A}$ is induced by the $l_{1,2}$ mixed norm defined by:

$$\|\mathbf{A}\|_{1,2} = \left(\sum_{j=1}^{L}\left(\sum_{i=1}^{N}\left|\mathbf{A}_{i,j}\right|\right)^2\right)^{1/2}.$$

5.2.3 Results

Method of data acquisition

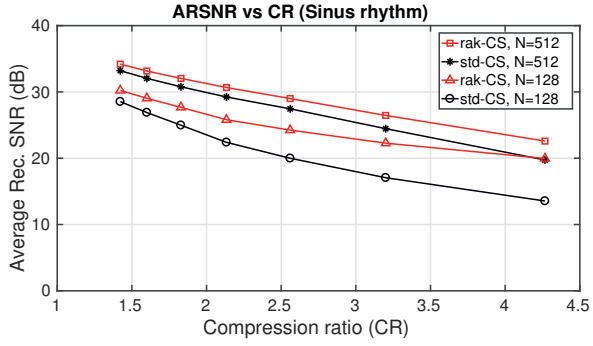
Atrial electrograms are recorded on the epicardium, the surface of the heart, using a custom-made 46 mm by 14 mm flexible multi-electrode array with 192 gold-plated electrodes and a 256-channel data-acquisition system [5]. The data is acquired using an analog front-end module that consists of an amplifier with a gain of 60 dB, a bandpass filter with a bandwidth extending from 0.5 to 400 Hz, and an analog-to-digital converter with a resolution of 16 bits, which samples the analog signal at 1 kHz. A total of 10 electrode array sections are required to cover the entire surface area of the atria. For rak-CS, one of the recorded sections is used as a reference for the correlation matrix estimation. Using the SPGL[1] toolbox, we use the CS decoders to reconstruct the signals by solving (5.3) and (5.6), where Ψ is the Symmlet6 transformation basis. Symmlet6 is chosen as the wavelet basis for its high reconstruction SNR performance when applied to compressed AEGs.

Performance evaluation

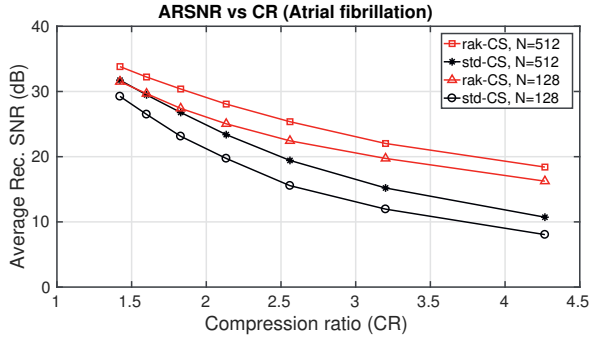
The reconstructed signal is compared to the original signal using the performance metric, reconstruction signal-to-noise ratio (RSNR) given by

$$\text{RSNR}_{\text{dB}} = 20\log\left(\frac{\|x\|_2}{\|x - \hat{x}\|_2}\right) \tag{5.7}$$

[1] http://www.cs.ubc.ca/ mpf/spgl1/



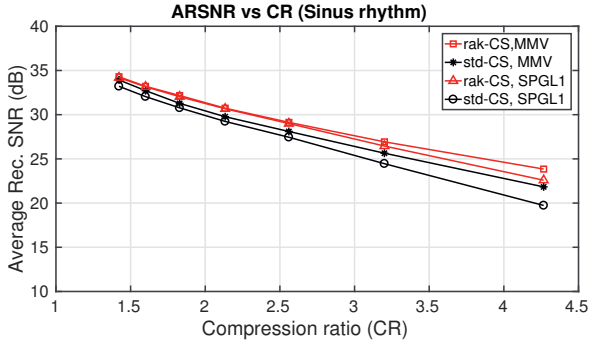
(a) Normal sinus rhythm



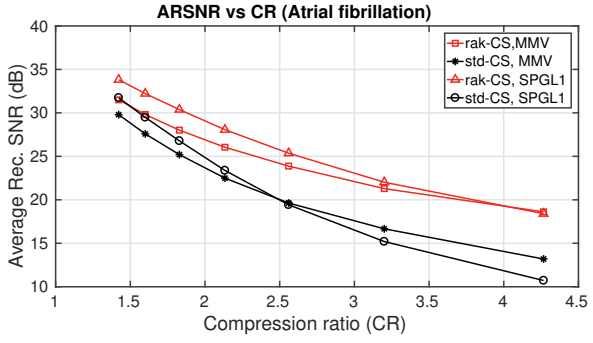
(b) Atrial fibrillation

Figure 5.3: Time-domain ARSNR vs CR for the atrial electrograms during: (a) SR (b) AF.

where $\|x\|_2$ refers to the l_2 norm of vector x. The RSNR is averaged over all the channels and 9 blocks of the signal for standard-CS and rak-CS in the time domain. Firstly, it can observed that rak-CS performs better than standard CS. The difference in the achieved average reconstruction SNR (ARSNR) performance between the two approaches increases with increase in the compression ratio. In case of SR, at CR = 4.26, rak-CS outperforms standard CS by almost 9 dB, as shown in Figure 5.3a. In case of atrial fibrillation, at CR = 4.26, rak-CS outperforms standard CS by 7.7 dB, as shown in Figure 5.3b. Rak-CS accounts for the localization of the signal energy due to which there is a significant improvement in performance at higher CRs (See Section 5.2.2).



(a) Normal sinus rhythm

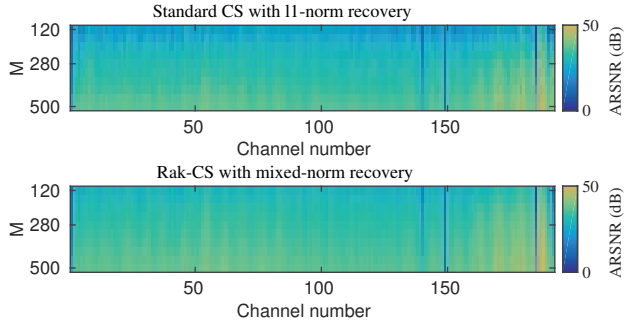


(b) Atrial fibrillation

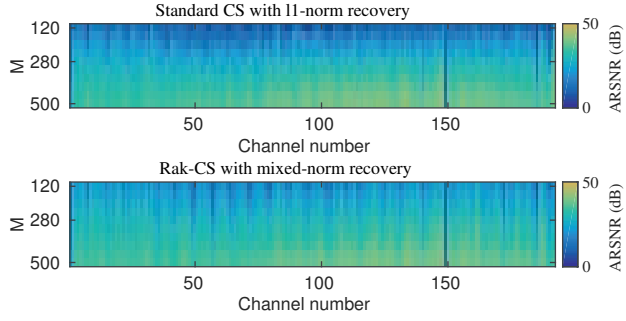
Figure 5.4: Spatial-domain ARSNR using mixed-norm recovery and l_1 norm minimization (for N=512)

The reconstruction performance of the SPGL1 recovery method, which minimizes only the l_1 norm, is compared with the mixed norm recovery approach and is as shown in Figures 5.4a and 5.4b. It can be seen that the reconstruction performance of the jointly sparse recovery approach is better than independent l_1 minimization recovery, and the difference is more pronounced at higher compression ratios. Also, standard CS is compared with rak-CS using the multiple-measurement-vector approach. At CR = 4.26, the ARSNR of the rak-CS approach using the mixed norm recovery is 24.4 dB, which is 4.6 dB better than standard CS with the l_1 norm minimization recovery method in the case of SR.

The ARSNR varies over different channels and compression ratios, showing significant

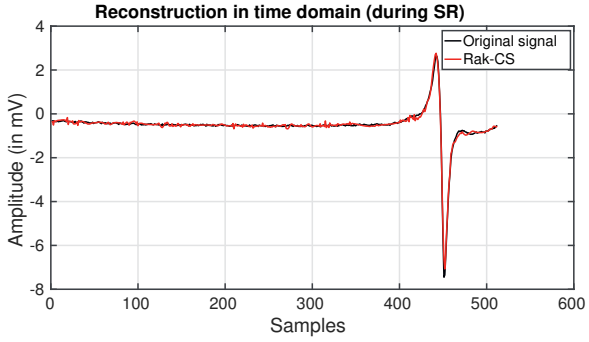


(a) Normal sinus rhythm

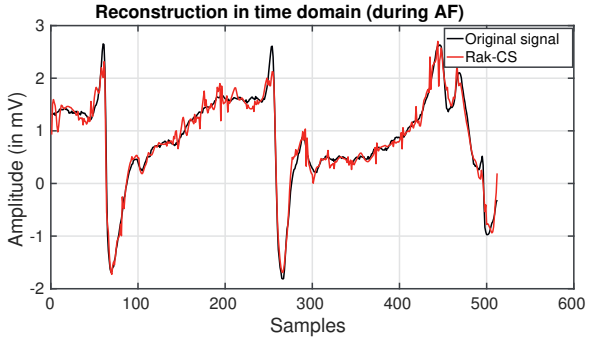


(b) Atrial fibrillation

Figure 5.5: ARSNR for 192 channels in case of: (a) SR (b) AF.



(a) Normal sinus rhythm



(b) Atrial fibrillation

Figure 5.6: Reconstruction of the time-domain waveform of atrial electrograms at CR = 4.26 (N=512)

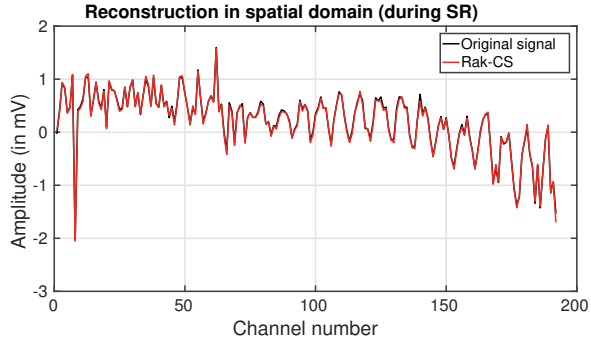
differences in the case of SR and AF, as shown in Figures 5.5a and 5.5b. The fixed dark blue lines on the figures correspond to reference signals. One can observe that the group structure is preserved in the case of SR, but the signals are not very similar in the case of AF. This points to the fact that during atrial fibrillation, the signals are not coherent, and the signal propagation takes place depending on the conduction paths and blocks in the atria.

Figures 5.6a and 5.6b show the reconstruction of the atrial electrograms in the time domain during SR and AF, respectively, for an arbitrarily selected channel number (ch = 90). Figures 5.7a and 5.7b show the reconstruction of the AEGs in the spatial domain, during SR and AF, respectively for an arbitrarily chosen time instant. We can see that the reconstruction of the signal during sinus rhythm is better than during atrial fibrillation for the same compression ratio. i.e, CR = 4.26.

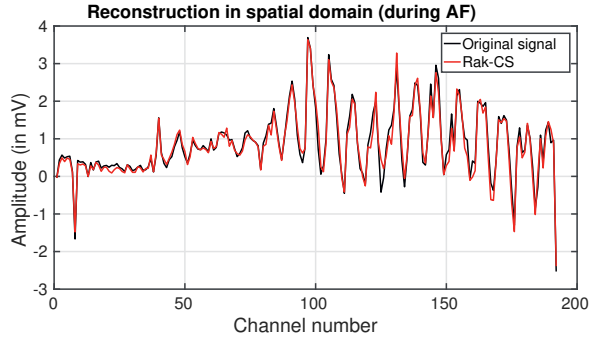
5.2.4 Conclusions

The main findings of the work can be summarized as :

- For the application of AEGs, rak-CS performs better than standard CS at all CRs in both the time- and spatial-domains.



(a) Normal sinus rhythm



(b) Atrial fibrillation

Figure 5.7: Reconstruction of the spatial-domain waveform of atrial electrograms at CR=4.26 (N=512)

- At lower CRs, mixed-norm recovery works better in the case of SR since the signals are coherent.
- In time-domain and spatial-domain, AF has worse absolute performance than SR because of incoherence among signals recorded in different channels and the much larger energies involved.
- For the detection of AF, rak-CS is a better choice, as the performance is significantly better than standard CS at higher CRs.

One distinguishing feature of AEGs from other biosignals, such as EEG or EMG, is the direction of the signal propagation. As the composite cardiac signal propagates in a specific direction, the absence of strong spatial correlations can detect the presence of AF. Finally, the rakeness-based compressed sensing approach holds the potential to reconstruct AF signals with a high ARSNR, which makes it a strong candidate for the acquisition of AEGs for the detection of AF, especially when aiming for hardware- and power-efficient implementation.

5.3 Visual inspection and the doctors' opinion

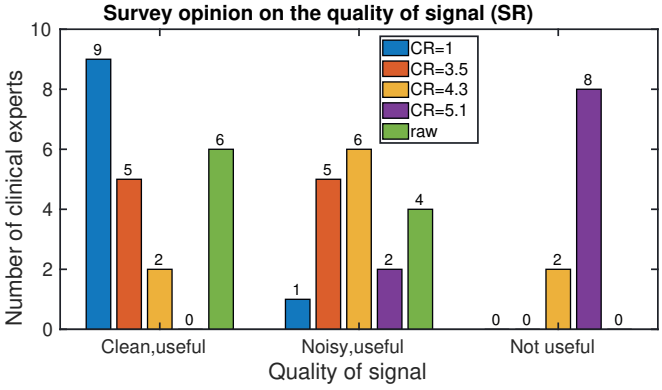
A team of hospital researchers and doctors visually inspected the results of the compression technique and validated the usability of the compressed signals to map the wavefront of the propagating atrial electrograms and diagnose atrial fibrillation. The survey analysis was conducted using feedback on the quality of signals given by clinical researchers and experts in epicardial mapping. A total of 10 experts participated in the survey. When compression is applied to signals, the resulting quality of the reconstructed signals should satisfy the requirement of the application. Some examples of applications are: estimation of local activation times for generating a wavefront map, investigating detailed fractionations, and, in specific cases studying conduction pathways and blocks. The motivation behind applying compression is to generate the wavefront map in the most data-efficient manner.

Based on the settings for compression used in Section 4.1, we survey the quality of signals for compression ratios (CR) = 1, 3.5, 4.2, and 5.1 as compared to a reference signal (original pre-recorded signal), in terms of whether the quality is clean and acceptable, or noisy, but acceptable or unacceptable for reliable detection and diagnosis of AF. Figure 5.8 shows the outcomes of the performance.

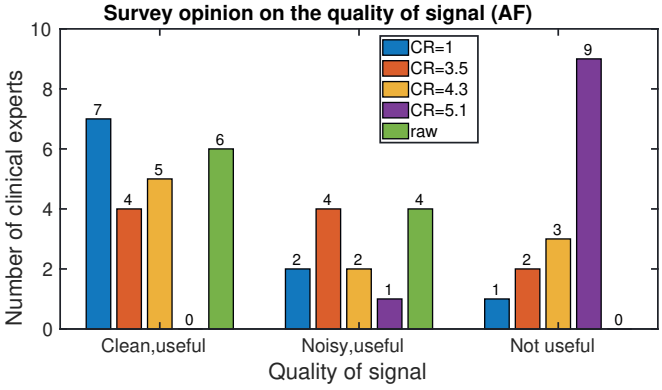
Significance of the performance survey: From Figure 5.8, it can be seen that as the compression ratio (CR) increases, the signal can become noisy and lose some of the features. The reconstructed signals are first-order low-pass filtered up to 400 Hz (bandwidth of AEG signals). A moving average filter with a window width of 4 is used to counter any noise on the reconstructed signal and smoothen the output waveform. In the case of SR AEG signals (Fig 5.8a), up to the value of CR = 4.26, it is accepted as clean and useful. At CR = 5.1, the signal quality is noisier, though it is still suitable for some applications, such as estimating local activation times used to generate the wavefront map. However, it may not be suitable for the detection of fractionated electrograms. In the case of AF AEG signals (Fig 5.8b), at CR = 1, which means that the algorithm is applied on the signals with no compression, we can observe that the signal looks "cleaner," which is due to filtering

out some amount of baseline noise due to reconstruction. The signal quality of AF AEG drops faster than the SR AEG signal at higher compression rates, which can be attributed to a higher amount of activity and features that characterize an AF signal. At CR = 5.1, most agree that the signal is not helpful in computing detailed features. However, even at this compression ratio, the signal can still be used to estimate local activation times as it requires a coarse resolution of the signal. In order to benchmark the results obtained from a custom-designed 192 inputs flexible electrode array, we compare it to the publicly available atrial electrograms on the *Intracardiac Atrial Fibrillation Database* from the MIT-BIH database [49]. From Figure 5.8c, we can see that most of them agree that the signals are generally "not useful." The same sparsity basis (Symmlet) is used in both cases (AEG from EMC and AEG from MIT-BIH database). A different sparsity basis should be used for better performance. The atrial electrograms segments available from the MIT-BIH database are bipolar recordings, whereas the custom 192-electrode array acquires unipolar recordings. Also, these signals could have a higher amount of noise. The features captured in these signals depend on the location of the electrodes. Also, signals from only 4 locations are recorded, which is far lower than the 192 electrodes used in the case of EMC AEG acquisition. Therefore, to generate a wavefront activation map, these signals may not be entirely suitable.

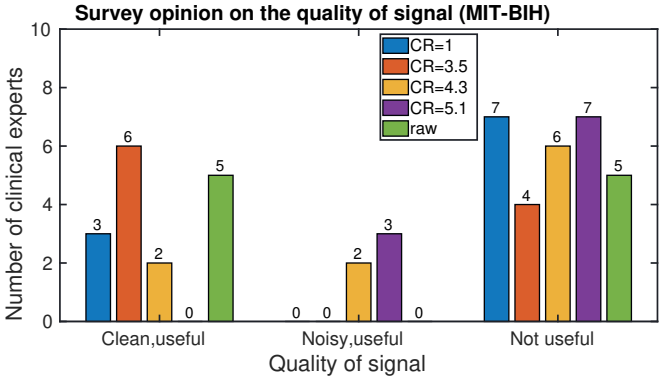
Figures 5.9, 5.10 and 5.11 show the waveforms of sinus rhythm atrial electrogram, atrial fibrillation atrial electrogram and bipolar atrial electrogram, respectively.



(a) Normal sinus rhythm



(b) Atrial fibrillation



(c) MIT-BIH AEG signals

Figure 5.8: Survery performance

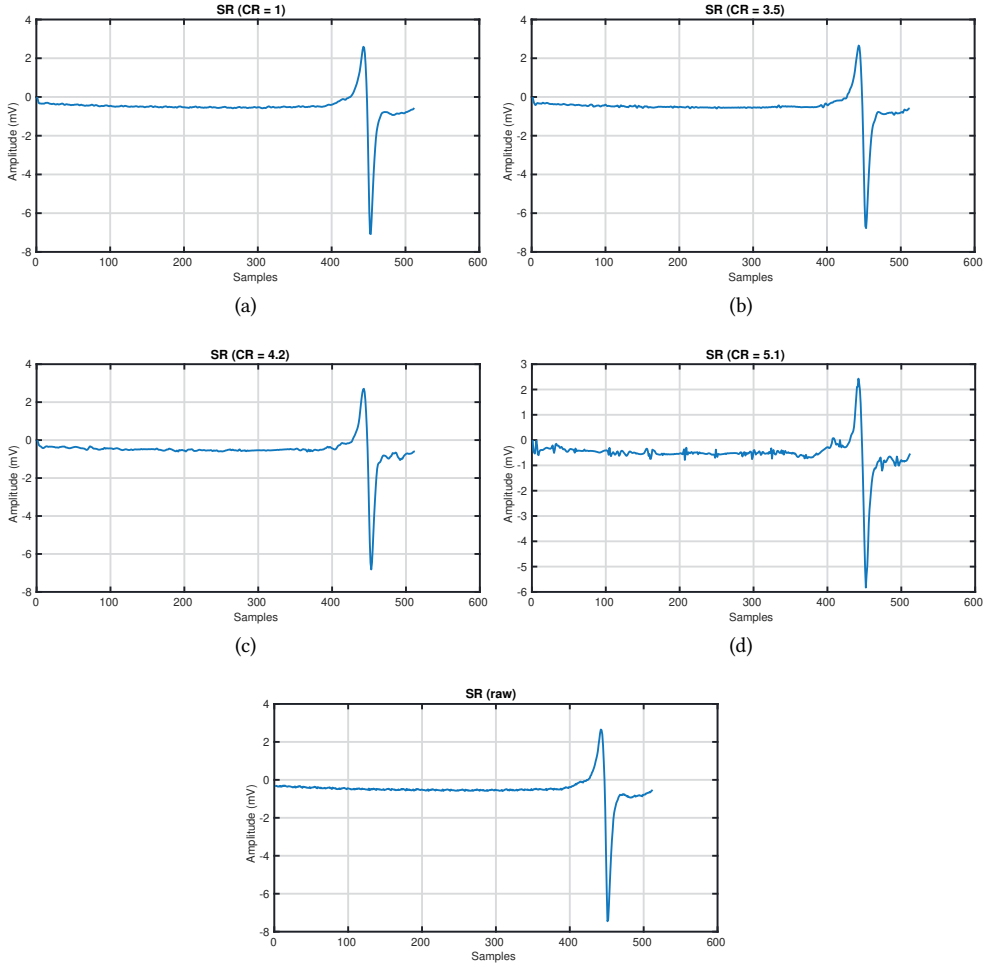


Figure 5.9: Reconstructed SR signals

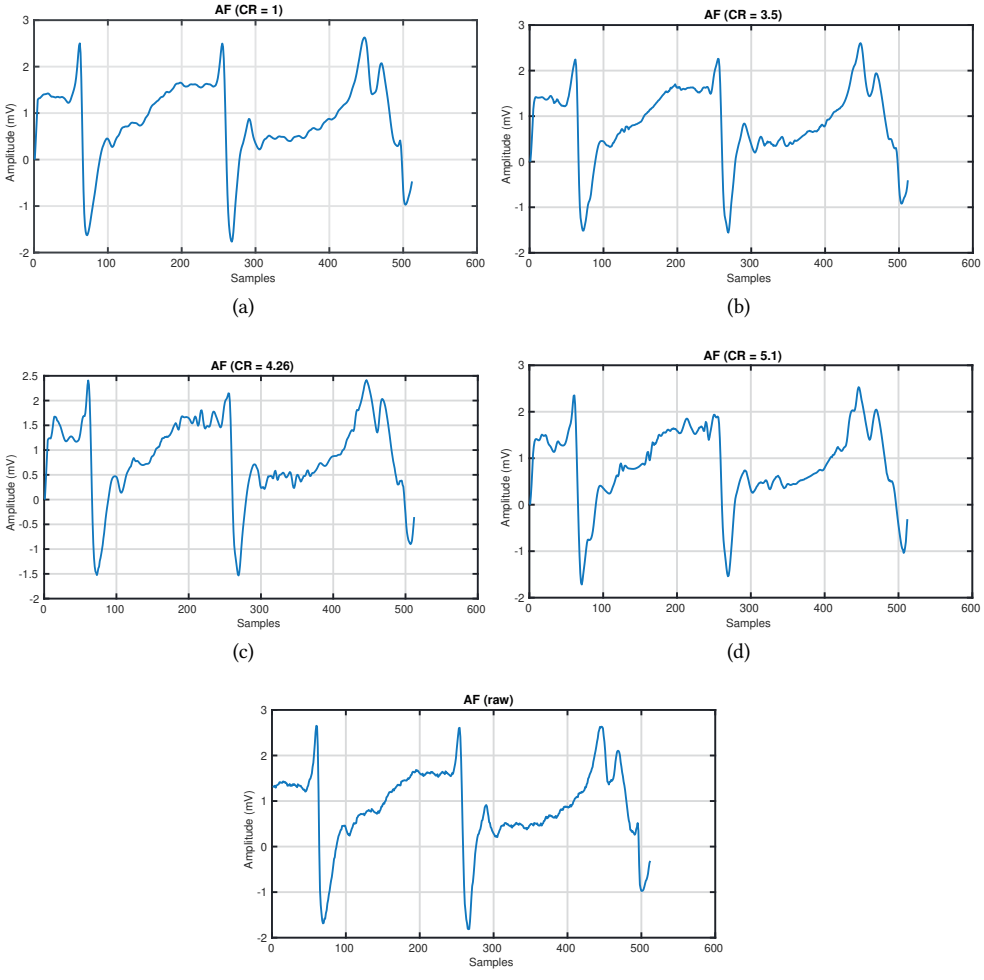


Figure 5.10: Reconstructed AF signals

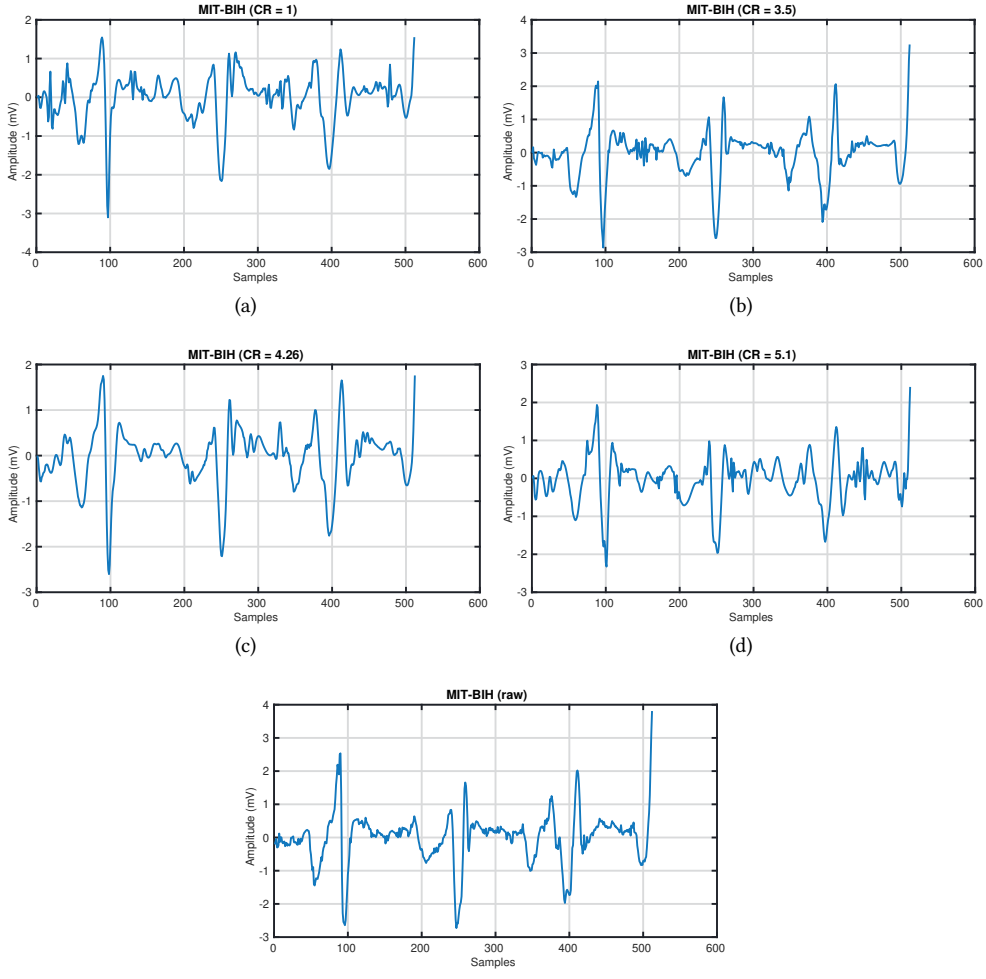


Figure 5.11: Reconstructed AEG signals. Source: MIT-BIH database

5.4 Similarity analysis

In Tables 5.1 to 5.3, we tabulate the quantitative performance of compressed sensing on atrial electrograms during SR and AF, and compare the results with signals from the MIT-BIH database. The same compression and reconstruction algorithm settings are used in all three cases. In order to compare the performance of the reconstructed signals with respect to the original signals, we use the average reconstruction signal-to-noise ratio (SNR) in dB, and percent root-mean-square difference (PRD), in %.

In Table 5.1, during SR, for a compression ratio setting of 5.12, PRD values of 7.55 % and 12.3 % are obtained when rakeness compressed sensing (rak-CS) and standard CS are used, respectively. A 5-dB improvement in SNR value is obtained while using rak-CS as compared to standard CS.

In Table 5.2, during AF, with an increase in CR, the performance drops much faster than in the case of SR. While the overall performance is worse than SR, rak-CS performs significantly better than standard CS at high CR values by more than 8 dB at CR = 5.12.

In Table 5.3, the performance of the intracardiac AEG signals from the MIT-BIH database is summarized. Overall, the performance of the proposed algorithms is worse in the case of AEG from the Intracardiac database than the AEG signals from EMC. It can be seen that rakeness CS performs much better than standard CS.

Table 5.1: Quantitative performance of the signals: AEG - Sinus Rhythm (EMC)

Compression Ratio	Std. CS SNR (in dB)	Std. CS PRD (in %)	Rake-CS SNR (in dB)	Rake-CS PRD (in %)
CR=5.12	18.189	12.333	23.321	7.5509
CR=4.26	21.753	8.2943	23.93	7.1425
CR=3.5	25.309	5.4279	28.257	3.9661
CR=1	38.404	1.2025	38.118	1.244

Table 5.2: Quantitative performance of the signals: AEG - Atrial Fibrillation (EMC)

Compression Ratio	Std. CS SNR (in dB)	Std. CS PRD (in %)	Rake-CS SNR (in dB)	Rake-CS PRD (in %)
CR=5.12	11.42	27.182	19.827	10.625
CR=4.26	12.068	25.231	20.721	9.2369
CR=3.5	15.408	16.968	23.091	7.0752
CR=1	39.629	1.0437	39.266	1.0883

Table 5.3: Quantitative performance of the signals: AEG - Intracardiac database (MIT-BIH)

Compression Ratio	Std. CS SNR (in dB)	Std. CS PRD (in %)	Rake-CS SNR (in dB)	Rake-CS PRD (in %)
CR=5.12	1.0213	88.907	8.1692	39.043
CR=4.26	3.0083	70.727	9.3036	34.263
CR=3.5	5.6758	52.025	11.374	26.995
CR=1	38.949	1.1287	37.454	1.3407

5.5 Conclusions

In this chapter, rakeness-based compressed sensing as a potential technique for compression of atrial electrograms is proposed, implemented, and verified on real pre-recorded

atrial electrograms.

In the first part of the chapter (Section 5.2), it is shown that rak-CS performs better than standard CS in both time and spatial domains. For the detection of atrial fibrillation, rak-CS is better than standard CS at higher compression rates.

In the second part of the chapter (Section 5.3), the quality of the reconstructed signals is assessed by a team of clinical experts at the Erasmus Medical Center Rotterdam to check for its suitability in the generation of an activation map. Up to a compression rate of 5.12, the signals are suitable for coarse-resolution applications such as wavefront map generation. The performance of the reconstructed signals is also quantitatively evaluated in terms of their similarity with respect to the original waveform. Using rakeness CS at CR = 5.12, the percent root-mean-square difference for SR is 7.5 %, whereas, for AF, it is 10.625 %.

6

Conclusions

This thesis focuses on the CMOS architectures based on hardware-algorithm co-design for acquiring cardiac signals. It aims to explore the design trade-offs to implement an accurate, compact, power- and area-efficient analog front-end targeted at the diagnosis of atrial fibrillation based on the electrocardiogram (ECG) and the atrial electrogram (AEG). Clinically, the goal is to diagnose atrial fibrillation (AF) early for better treatment alternatives based on understanding the disease progression. This concluding chapter presents an overview of the thesis outcome while summarizing the main findings and original contributions. Based on the results, recommendations for future work are presented.

6.1 Thesis outcomes

Cardiac signals can either be non-invasively recorded on the surface of the body in the form of an ECG or invasively mapped from the surface of the heart in the form of AEG signals. The key challenges associated with designing a compact, accurate, and efficient analog electronic front-end are discussed in Chapter 1. The existing techniques and state-of-the-art implementations to solve the challenges in acquiring cardiac signals in the context of the work described in this thesis are discussed in Chapter 2.

Targeting single-channel front-ends, a design method based on a state-space approach for ΣΔ ADCs targeting desired arbitrary signal-transfer and noise-transfer functions while optimizing their dynamic range are presented in Chapter 3. The approach targets the acquisition of cardiac signals with high accuracy of the high-pass filter function and suppresses baseline wandering. By computing the intermediate functions, the impact of non-idealities of the integrator(s) on the overall performance of the ADC is presented. From calculations and simulations, it is shown that for very small integrator coefficients, the non-ideal effects of the integrator on the overall ADC are negligible. From the analysis, it is shown that an orthonormal ΣΔ topology offers better performance than the observable canonical ΣΔ architecture. A complete analog front-end consisting of a pre-amplifier and an orthonormal ΣΔ ADC with an integrating feedback loop is implemented in 0.18μm standard IC technology and illustrates the proposed approach. From measurements, it is shown that using the integrating feedback loop, a high-pass characteristic filter transfer can be obtained, the cutoff frequency of which can be changed by varying the switched-capacitor clock frequency, thus reducing baseline wandering in ECG signals. The ADC consumes 81 μW at a sampling rate of 500 kHz and occupies an area of 0.126 mm^2.

Targeting multi-channel front-ends, a design method to develop optimal spread-spectrum-based analog front-ends, is developed in Chapter 4. A structured classification of modulation strategies orthogonalized by their degrees of freedom is also proposed to identify possible techniques for acquiring multiple analog signals simultaneously using a single analog front-end. Using the design method, real pre-recorded atrial electrograms (both during sinus rhythm and atrial fibrillation) are used to verify the concept. The performance of the PRBS and Walsh-Hadamard codes for different parameter settings are quantified by percentage root-mean-square difference (PRD). For a bandwidth f_b = 200 Hz and code length (L) = 127, the optimum modulation frequency, f_{mod} is 70 kHz with a mean PRD of 10.8 and 13.1 for SR and AF, respectively. The PRD performance improves to 2.65 and 3.02 for SR and AF, when L = 511 and f_{mod} = 280 kHz. AF performs worse than SR due to the much higher signal activity. SR exhibits a worse performance in certain parts of the segment than AF due to sharp peaks and loss of those peaks in the reconstructed signal.

The spread-spectrum modulation design method is validated by implementing a 4-channel PRBS-modulated spread-spectrum recording system in a 0.18μm CMOS process, which consists of a shared amplifier, a shared ΣΔ ADC, and an on-chip Gold code generator occupying 0.067mm^2 and consuming 20.7μA per channel input.

Rakeness-based compressed sensing (CS) targeting compression of atrial electrograms is presented in Chapter 5 and verified on real pre-recorded atrial electrograms. Rakeness CS and standard CS are used to compress AEG signals in the time and spatial domains. The results show that rakeness CS performs better than standard CS in the compression

of AEG signals. It is also shown that for the detection of atrial fibrillation, rakeness CS is better than standard CS at higher compression rates. For the purposes of diagnosing the arrhythmia, the proposed compression technique can be used on high-density electrode array mapping of atrial signals in low data-rate settings. In addition to these results, the quality of the reconstructed signals was assessed by a team of clinical experts at the Erasmus Medical Center (EMC), Rotterdam, to check for its suitability in the generation of an activation map. Up to a compression rate of 5.12, the signals are suitable for coarse-resolution applications such as wavefront map generation. The performance of the reconstructed signals is also quantitatively evaluated in terms of their similarity with respect to the original waveform. Using rakeness CS, at CR =5.12, the percent root-mean-square difference for SR is 7.5 %, whereas for AF it is 10.625 %.

6.2 Main contributions and discussions

The main and original contributions made in this thesis are summarized as follows:

- A state-space based design method for designing ΣΔ ADCs targeting desired arbitrary signal-transfer and noise-transfer functions while optimizing their dynamic range (Chapter 3)
- Measurement results of an orthonormal ΣΔ modulator with a high-pass loop demonstrating the proposed design method in a 0.18 μm CMOS process technology (Chapter 3)
- A structured classification of modulation strategies orthogonalized by their degrees of freedom to identify possible techniques for acquiring analog signals (Chapter 4)
- A design method and identification of trade-offs in acquiring analog signals optimally using spread-spectrum analog front-ends (Chapter 4)
- Measurement results of a 4-input PRBS modulated spread-spectrum recording system in 0.18μm CMOS technology (Chapter 4)
- Rakeness-based compressed sensing can be used in the compression of atrial electrograms (Chapter 5)
- Rakeness-based compressed sensing performs better than standard compressed sensing in the detection of atrial fibrillation at higher compression rates (Chapter 5)

6.3 Recommendations for future research

This thesis investigates the design of CMOS front-ends to acquire cardiac signals efficiently and accurately. Some ideas for further investigations are as follows:

- The proposed high-pass orthonormal ΣΔ ADC cannot adaptively change its high-pass filter cut-off frequency. An area-efficient on-chip solution to process and adaptively change the cut-off frequency in real-time based on the bandwidth of the input signal and the accompanying motion artifacts (baseline wandering) is worth investigating.

- The designed prototypes can be integrated with the custom-fabricated flexible electrode array or a commercially available endocardiac electrode array for testing on animals as a first step towards a compact integrated module for recording cardiac signals during open-heart surgery.
- If designed prototypes are used in an implantable device, an increase in the number of channels leads to an increase in the data rate. Transmitting a large amount of data leads to high power consumption. On-chip data-compression methods such as compressed sensing can be investigated for efficient data transmission.
- In this work, we have focussed on acquiring the raw data efficiently for use in detecting atrial fibrillation and generating the wavefront activation map. A dedicated AF detection algorithm, e.g., thresholding, or classifiers such as SVM or more sophisticated artificial neural network techniques can be implemented on-chip to compute the abnormalities in the signals can be used.
- Rakeness-based compressed sensing compresses the atrial electrograms with satisfactory recovery results. As a future work, the proposed approach can be verified and demonstrated through a silicon prototype.

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Curriculum Vitæ

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1990/11/30	Born in Cuttack, Odisha, India.

Education

2/2017–2/2022	Ph.D. Student, Bioelectronics group, Department of Microelectronics, Delft University of Technology, The Netherlands. *Thesis: Analog front-end and algorithm co-design for efficient biosignal acquisition* Advisor: Prof. Dr. Wouter A. Serdijn Promotors: Prof. Dr. Wouter A. Serdijn, Prof. Dr. Gianluca Setti
8/2014–10/2016	MSc. Electrical Engineering, Department of Microelectronics, Delft University of Technology, The Netherlands. *Thesis: Structured electronic design of HPΣΔ converters for cardiac signal acquisition*
8/2008–-6/2012	BE. Electrical and Electronics Engineering, Sri Jayachamrajendra College of Engineering, Mysore, India. *Thesis: Electron transport characteristics of carbon nanotubes for gas sensing applications*
4/1996–-3/2008	Primary, Secondary and Secondary High School, Kendriya Vidyalaya, Indian Institute of Science (K.V. IISc), Bangalore, India.

Experience

2/2022–-Present	Analog Mixed Signal designer, Analog Mixed Signal Competence Centre, NXP Semiconductors, Eindhoven, The Netherlands
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10/2012–4/2014	Low Voltage Motor Designer Asea Brown Boveri (ABB), Peenya, Bangalore.
1/2012–6/2012	Bachelor thesis researcher, Instrumentation and Applied Physics, Indian Institute of Science, Bangalore, India.
6/2011–-8/2011	Summer research intern, Nano-devices and Sensors Lab, CENSE lab, Indian Institute of Science, Bangalore, India.
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Academic service

Reviewer	IEEE ISCAS 2018, 2019, 2020, 2021 IEEE BioCAS 2018, 2019, 2020 IEEE APCCAS 2019 IEEE TBCAS (Since 2018) IEEE TCAS II (Since 2021)
(Co-)Supervisor	Aurojyoti Das's master thesis, "Multichannel LC ADC to Record Atrial Electrograms", 2018-2019 Anirudh Kumar Parag's master thesis, "Energy Module for Self-Sustainable Wearable Sensors", 2018-2019
Teaching assistant	Technical Medicine, Prof. dr. Wouter A. Serdijn, 2017-2018

List of Publications

1. **Samprajani Rout**, Wouter A. Serdijn: Structured electronic design of high-pass ΣΔ converters and their application to cardiac signal acquisition. IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 2017.

2. **Samprajani Rout**, Wouter A. Serdijn: High-Pass ΣΔ Converter Design Using a State-Space Approach and Its Application to Cardiac Signal Acquisition. IEEE Transactions on Biomedical Circuits and Systems (TBCAS), 2018.

3. **Samprajani Rout**, Mauro Mangia, Fabio Pareschi, Gianluca Setti, Riccardo Rovatti, Wouter A. Serdijn: Rakeness-based compressed sensing of atrial electrograms for the diagnosis of atrial fibrillation. IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019.

4. Shmuel Auerbach, Wouter A. Serdijn, **Samprajani Rout**: Compressed-sensing of spatiotemporally correlated and/or rakeness processed electrograms, US patent, US20200337579A1, 2020.

5. **Samprajani Rout**, Bert Monna, Fabio Pareschi, Gianluca Setti and Wouter A. Serdijn: Spread-spectrum modulated multi-channel biosignal acquisition using a shared analog CMOS front-end. IEEE Transactions on Biomedical Circuits and Systems (TBCAS), 2023 & IEEE International Symposium on Integrated Circuits and Systems (ISICAS), Jeju, Korea, 2023.

6. Aurojyoti Das, **Samprajani Rout**, Alessandro Urso, Wouter A. Serdijn: Activity Dependent Multichannel ADC Architecture using Level Crossing Quantisation for Atrial Electrogram Recording, IEEE Biomedical Circuits and Systems Conference (BioCAS), Nara, Japan, 2019.

7. **Samprajani Rout**, Samaneh Babayan, Wouter A. Serdijn: A subthreshold source-coupled logic based time-domain comparator for SAR ADC based cardiac front-ends. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Bangkok, Thailand, 2019.

Included in this thesis.

Atrial fibrillation (AF) is a type of cardiac arrhythmia affecting over 46 million people worldwide. Despite advancements in awareness and diagnostic methods, precision and timely diagnosis remain essential for effective preventive care. Two major electrophysiological monitoring approaches exist: ECG (electrocardiogram), recorded on the body surface, and AEG (atrial electrograms), recorded on the heart surface with higher spatial resolution. Developing compact application-specific integrated circuits (ASICs) is crucial for recording and diagnosing cardiac abnormalities such as AF. This thesis addresses key challenges in enhancing the linearity and accuracy of high-pass filter cut-offs for single-channel cardiac signal acquisition and maximizing resource efficiency for multi-channel acquisition. Understanding the biological mechanisms through AEG recordings is vital for early detection and monitoring of AF, significantly influencing disease progression.