

Microstructural and micromechanical characterization of sintered nano-copper bump for flip-chip heterogeneous integration

Ji, Xinrui; Du, Leiming; He, Shan; van Zeijl, Henk; Zhang, Guoqi

DOI

[10.1016/j.microrel.2023.115180](https://doi.org/10.1016/j.microrel.2023.115180)

Publication date

2023

Document Version

Final published version

Published in

Microelectronics Reliability

Citation (APA)

Ji, X., Du, L., He, S., van Zeijl, H., & Zhang, G. (2023). Microstructural and micromechanical characterization of sintered nano-copper bump for flip-chip heterogeneous integration. *Microelectronics Reliability*, 150, Article 115180. <https://doi.org/10.1016/j.microrel.2023.115180>

Important note

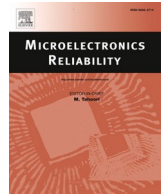
To cite this publication, please use the final published version (if applicable). Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.



Microstructural and micromechanical characterization of sintered nano-copper bump for flip-chip heterogeneous integration

Xinrui Ji^{a,*}, Leiming Du^a, Shan He^b, Henk van Zeijl^a, Guoqi Zhang^a

^a Department of Microelectronics, Delft University of Technology, Delft, the Netherlands

^b Microlab, Civil Engineering and Geosciences, Delft University of Technology, Delft, the Netherlands

ARTICLE INFO

Keywords:

Cu sintering
Flip-chip
Nanoindentation
Micromechanical properties
Microstructural characterization

ABSTRACT

Copper nanoparticles (CuNPs) sintering for flip-chip interconnects is a promising solution for 3D and heterogeneous integration to overcome the limitation of solder materials. To this end, we perform the photolithographic stencil printing method to pattern CuNPs, and the form of flip-chip interconnects is completed after CuNPs sintering process. This paper aims to study the effect of sintering processing parameters (time, pressure, temperature) on the mechanical properties of CuNPs bumps when applying the novel method to approach the Cu interconnects. We fabricated seven groups of specimens of sintered CuNPs bumps, built with a diameter of 100 μm and sintered. The nanoindentation tests assessed the mechanical property to get Young's modulus and hardness. Results clarify that Young's modulus is strongly affected by pressure. An suggested combination of parameters (the 25 MPa and 260 $^{\circ}\text{C}$ for 15 min) give the highest modulus of 126 GPa and the hardness of 1.76 GPa. Moreover, the observations by scanning electron microscopy (SEM) reveal the microstructure and porosity evolution versus different processing parameters.

1. Introduction

With the scaling down of transistors, investigation of interconnects and integration will produce more microelectronic functions on smaller substrates at lower costs in the recent semiconductor industry. Meanwhile, Moore's Law of integrated circuits does not conform to the development of the microelectronics manufacturing industry [1]. The high-end system in package (SiP) and heterogeneous integration (HI) are the global solutions toward the "More than Moore" application [2]. In addition, chip-to-chip (C2C) and chip-to-wafer (C2W) are adopted to miniaturize the multi-functional integrated application [3]. The flip-chip bonding technology for C2C and C2W is wildly utilized as the basic building block of 3D stacking architecture. The decreasing interconnect size should undertake higher heat dissipation, current density, and thermal strain, which raises higher requirements in response to reliability. Solder materials have been widely used for flip-chip integration. However, solder materials' low melting temperatures (220–255 $^{\circ}\text{C}$) are currently challenging compatibility for harsh environment applications [4,5]. Although, current nano copper formulations sintering temperatures are 200–260 $^{\circ}\text{C}$, close to solder reflow temperatures, the sintering material has a high melting temperature and can

survives in a high temperature environment [6]. In addition, the current-induced electromigration failures limit the current- and temperature capacity in solder-based Cu μbump interconnects [7]. The nano copper materials having better electromigration resistance property and higher melting point than solder are considered a promising replacement for solder material [8,9], referred to as "all-Cu interconnects" for improving reliability.

Recently, nano copper sintering technology has been developed for flip-chip packaging but has been widely used in die-attach technology. For nanosilver sintering, shear strength is commonly used to characterize the mechanical properties [10–12]. Similarly, Zhang et al. [13] studied the effect of the process parameter on the in-air sintering nano copper paste in high-power electronics. Maximum shear strength was obtained at in-air sintering parameters of 240 $^{\circ}\text{C}$, 25 MPa, and 3 min, being 41.63 ± 4.35 MPa. Liu et al. [14] also investigated the influence of sintering parameters in the N_2 atmosphere, and the best die shear strength was 116 MPa when the die was sintered at a temperature of 250 $^{\circ}\text{C}$ and a pressure of 30 MPa for 3 min. The sintered CuNPs are mainly used as the die-attach materials in high-power devices. In the last decade, a few works investigated the mechanical reliability of CuNPs joint flip-chip through shear tests [15–17]. Moreover, the

* Corresponding author.

E-mail address: x.ji@tudelft.nl (X. Ji).

microstructure-related mechanical properties of sintered CuNPs are crucial for studying interconnects in flip-chip integration.

Nanoindentation is commonly used to investigate the mechanical properties of nanoscale materials. Some valuable information can be derived from the load-displacement curve, such as elastic modulus and hardness. As reported in [29], elastic modulus, yield stress and hardness are crucial in terms of mechanical reliability. Nanoindentation can be used as a measurement technique to assess all of these properties. The mechanical properties of nanoporous materials were characterized through the load-displacement curve by the nanoindentation test [18–21]. Fan et al. [22] reported the high-temperature deformation behaviors of sintered nano copper using the nanoindentation test. The continuous stiffness measurement (CSM) technique has recently significantly improved the traditional nanoindentation test, which can directly measure the dynamic contact stiffness and accurately observe the micro/nanoscale deformation during indentation loading [23]. Fakiri et al. [26] proposed that the mechanical properties of porous materials at micro- and nanoscale can be determined through nanoindentation using the CSM method. The nanoindentation test enables multi-point testing of different CuNPs bumps on a sample with a specific sintering parameter to characterize the mechanical properties of the nanostructure. Once sintered at relatively low temperatures, the sintered material properties approach that of the bulk materials, enabling the integration of high melting materials into chip assembly.

In this study, nanoindentation tests are performed to investigate the mechanical properties of CuNPs bumps. Seven groups of specimens under different processing parameters, including sintering time, pressure and temperature, are fabricated. A combination of processing parameters related to Young's modulus and hardness is recommended. Based on the SEM observation and analysis of porosity, the relationship between microstructure evolution and processing parameters is revealed and discussed.

2. Experimental section

2.1. Cu nanoparticles

In this study, an in-house produced CuNPs paste was applied to fabricate CuNPs bumps for flip chip integration. To characterize the Cu nanoparticles (NPs) before the sintering process, a thin layer of the CuNPs paste was first spread on the substrate and then dried for 15 min at 110 °C in the ambient. The morphology of Cu NPs was observed by scanning electron microscopy (SEM, FEI Helios G4 CX), as shown in Fig. 1a. The size distribution of as-treated CuNPs was counted on the SEM images using image processing software (ImageJ), as illustrated in Fig. 1b. The majority of CuNPs have a diameter of about 100 nm to 300 nm with a quasi-spherical shape. Some adjacent NPs agglomerate together because the CuNPs have high activity. The composition of the CuNPs was investigated using EDX (ThermoFisher) to show the detailed information of the CuNPs paste. Fig. 1c shows the EDX results at the

position indicated in the corresponding Fig. 1a, observing the NPs are predominantly copper and only a few oxygen elements (~3.46 wt%), which mainly originated from the organic additives inside the CuNPs paste. Therefore, the samples have not been oxidized during preservation and pretreatment.

2.2. Test nano-copper bumps fabrication

It is well known that stainless steel foils are commonly used as stencil masks to pattern paste-based materials in the industry. The product technique limits the pattern size of the conventional stencil. Therefore, a novel process called photolithographic stencil printing (LSP) enables the patterning and definition of CuNPs patterns at the wafer level, with the advantages of high throughput and high resolution. During LSP process, the photoresist acts as the stencil mask, and a photoresist lift-off process is applied to remove the photoresist stencil and excess nano-Cu paste.

To implement the flip chip interconnects, we designed an array of 200 μm pitch CuNPs interconnects with a diameter of 100 μm on 10×10 mm dies. We prepared a double-side polished 500 μm silicon (Si) wafer, and the sample fabrication process is illustrated in Fig. 2. The Si wafer was first insulated with 300 nm low-pressure silicon nitride (SiNx) by low-pressure chemical vapor deposition (LPCVD) to protect the Si substrate from copper diffusion. Then, a 300 nm Cu conductive layer and a 2/25 nm Ti/TiN adhesion layer were deposited on the prepared Si wafer using sputtering deposition (Trikon Sigma 204 Dealer). Subsequently, a 10 μm positive photoresist (AZ-12XT) was spin-coated on the substrate. The photoresist was exposed (ASML PAS 5500/80 wafer-stepper) and developed to obtain an array of opening holes with a diameter of 100 μm , as shown in Fig. 2c. Then, a small quantity of nano-Cu paste was dispensed and manually distributed by a silicon squeegee on the test wafer. The test wafer was dried in an oven at 80 °C for 10 min for the next step. The step in Fig. 2d and e was repeated to improve the uniformity of patterned CuNPs, a small additional amount of CuNPs paste was evenly applied again on the test wafer to dry at 110 °C for 10 min.

In the subsequent photoresist lift-off process, the prepared wafer was immersed in *N*-methyl-2-pyrrolidone (NMP) and stirred at room temperature to strip the photoresist. After rinsing with DI water and drying steps, the 100 μm nano-Cu bumps array remained on the substrate of the process wafer. The resulting wafer after LSP process was diced into 10×10 mm² chips, and the remaining CuNPs bumps were observed and estimated using the 3D profilometer (Keyence VK-X250).

2.3. Sintering of CuNPs bump

This study fabricated the stack-integrated samples with CuNPs bumps for sintering process investigation. The bare Si wafer was diced into 6×6 mm² dies, called dummy dies, which were then flipped and placed onto 10×10 mm² chips with CuNPs patterns under microscopy for alignment. A wafer bonder (AML-AWB-04 waferbonder) performed

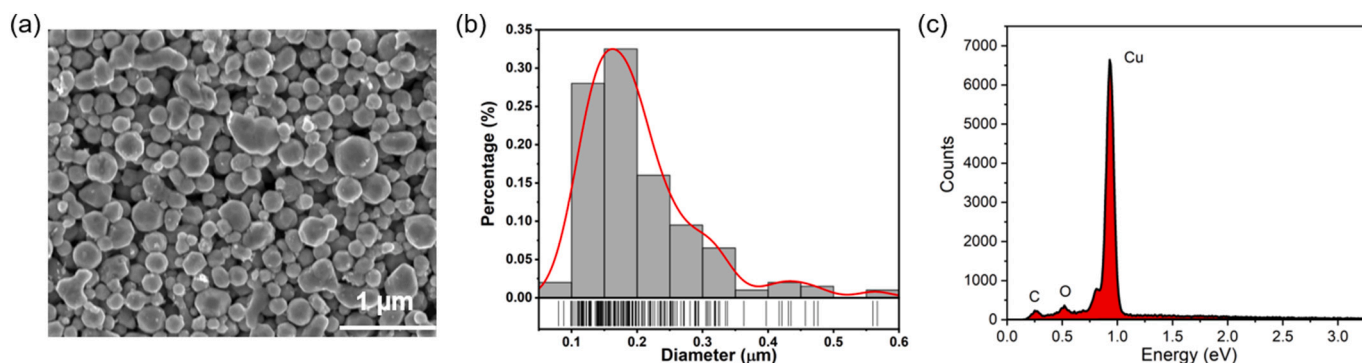


Fig. 1. (a) SEM image of CuNPs in this study, (b) size distribution of the CuNPs indicating in (a) and (c) EDX results of the CuNPs.

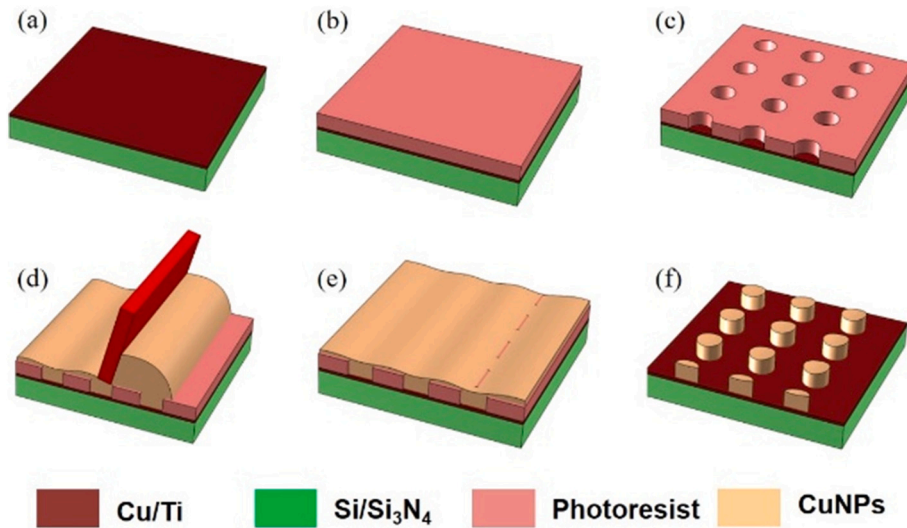


Fig. 2. An overview of the patterns transferring process using photolithography screen printing on photoresist mask and sequential lift-off process.

the pressure-assisted sintering process in a high vacuum environment ($\sim 1 \times 10^{-3}$ mbar) to prevent oxidation of CuNPs. Fig. 3a depicts a schematic of the cross-section of the flip chip bonding setup for CuNPs interconnects. The top and bottom bonding plates applied sintering temperature (220–300 °C), sintering time (15–60 min) and sintering pressure (20–30 MPa) to seven stacking dies, respectively. The design of experiment (DOE) for the pressure-assisted sintering process in this study is shown in Table 1. After the sintering process, since no sintering phenomena occurred at the interface between the Si top die and the CuNPs on the surface of the CuNPs bump, the top Si die was easily peeled off from the bottom die and the CuNPs bumps were retained, as illustrated in Fig. 3b. Finally, the resulting samples with sintered CuNPs bumps were used for the nanoindentation test.

2.4. Nanoindentation test

The traditional nanoindentation test displays a typical load-displacement curve, as in Fig. 4a, with the load and unload performance. The hardness and the elastic modulus are the mechanical properties measured using nanoindentation. The diamond tip is pressed into the surface of a sample; meanwhile, plastic and elastic deformation occurs. During loading, the shape of the tip and indentation depth determines the contact area to calculate the hardness of materials. When unloading the tip, the elastic deformation is recovered. According to the load-displacement curve, the hardness can be derived from the peak load P_{max} :

$$H = \frac{P_{max}}{A} \tag{1}$$

where A is the projected area of the contact surface as a function of the contact depth h_c and the shape of tip as:

Table 1

Design of experiment for sintering process parameter study.

Nr.	Pressure (MPa)	Temperature (°C)	Time (min)
1	20	300	60
2	20	300	30
3	20	300	15
4	20	260	15
5	15	260	15
6	25	260	15
7	20	220	15

$$A = f(h_c) \tag{2}$$

$$h_c = h_{max} - S(h_{max} - h_r) \tag{3}$$

where h_{max} and h_r are the maximum indentation depth and the final depth after complete unloading, as shown in Fig. 4b. S represents the contact stiffness at the initial unloading, which is defined as the slope of the initial unloading curve. The elastic modulus can be derived from the contact stiffness as follows

$$S = 2\beta\sqrt{\frac{A}{\pi}}E_r \tag{4}$$

where β is the geometric constant of the indenter [27] and E_r is the reduced elastic modulus, which is related to elastic modulus E and Poisson's ratio ν , as the following relationship:

$$E_r = \frac{1 - \nu^2}{E} + \frac{1 - \nu_i^2}{E_i} \tag{5}$$

For the diamond Berkovich indenter, $E_i = 1141$ GPa, $\nu_i = 0.07$ and $\beta = 1.034$ [28], as well as the projected area A is given by $24.56h_c^2$.

Compared to the conventional method of determining stiffness from the slope at the top of the unloading curve, CSM significantly enhances the nanoindentation test. The advantage of the CSM mode is that the contact stiffness can be measured continuously in one loading experiment without needing an unloading process. The contact stiffness at any loading point can be deduced by analyzing the system's dynamic response. And the time constant of CSM is at least three orders of magnitude lower than traditional methods [23]. The CSM is conducted by applying harmonic forces to the nominally increasing load on the indenter, as illustrated in Fig. 4c.

In this study, the nanoindentation test was conducted in the Nano

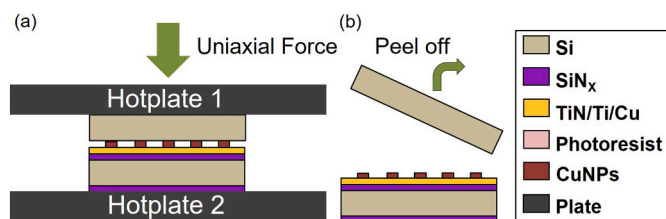


Fig. 3. Schematic of CuNPs pressure-assisted sintering bonding process and the fabrication of the samples for nanoindentation test.

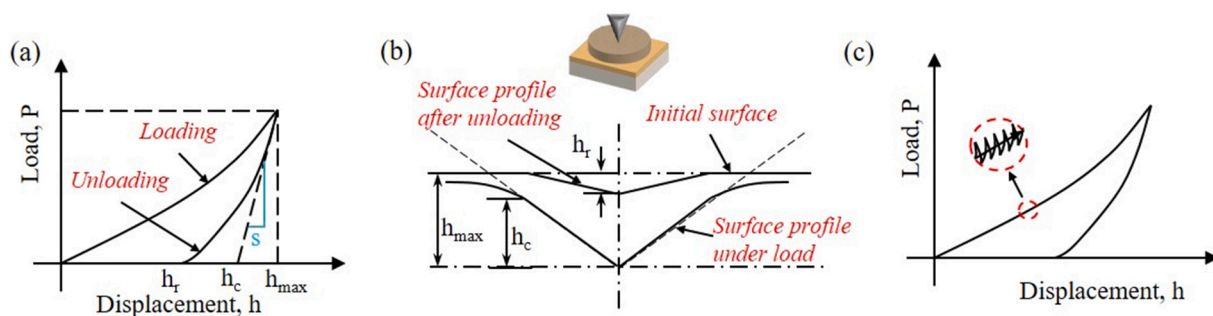


Fig. 4. (a) A typical load-displacement curve, (b) schematic of the deformation of the sample during and after indentation [27] and (c) a sketch of the CSM loading cycle.

indenter G200, which is equipped with a diamond Berkovich tip indenter at room temperature. The nanoindentation test was performed on the surface of sintered CuNPs bumps under different sintering conditions using the same process to study the sintering process parameters. For each sintering process parameter according to DoE, three CuNPs bumps on the same substrate were selected, indented and measured at one position of each bump. For the characterization of the surface CuNPs materials to achieve the improved nanoindentation test results, the CSM mode was applied during measurement and the indentation distance was set from 0 μm to 2 μm into the surface, using a surface approach velocity of 10 nm/s, a harmonic displacement of 2 nm and a frequency of 45 Hz. The Poisson's ratio is set to 0.3 for calculation. Finally, the effect of the sintering process parameters on the nanoindentation performance was investigated and analyzed by the load-displacement curve and the measured hardness, contact stiffness, and Young's modulus.

3. Results and discussion

3.1. Test CuNPs bumps inspection

To inspect and compare the morphologies of CuNPs bumps after LSP

and sintering processes, a 3D optical and laser profiling analyzer combined with a 3D profilometer (Keyence VK-X250) were used to characterize the as-printed and sintered CuNPs bumps. Fig. 5a and b shows the 2D optical images and 3D laser image of the as-printed CuNPs bumps. It is observed that most of the CuNP bumps present a circular shape and the same pitch, although there are still some nano copper clusters attached to the bumps. The good patterns after the LSP process will promise the success in the following sintering process. Besides, to estimate and compare the average height of the CuNPs bumps, ten profile lines at intervals of 1.5 μm on a row of non-sintered and sintered CuNPs bumps were characterized and averaged, respectively, which are indicated by the blue lines in Fig. 5a and d. Fig. 5c shows the height distribution measured from 3D profilometer of the as-printed CuNPs bumps indicated by the blue line in Fig. 5a. It is observed that almost all the as-printed bumps present a valley shape. On the one hand, the solvent was evaporated due to the drying progress under 110 $^{\circ}\text{C}$ (Fig. 2e), which caused the shrinkage of the CuNPs bump. On the other hand, the boundary of the CuNPs bumps was squeezed by the thermal expansion of the photoresist. Figs. 5d and e shows the surface morphologies of the CuNPs bumps sintered at 260 $^{\circ}\text{C}$ with a pressure of 15 MPa for 15 min (sample 5). It is seen from Fig. 5e that the surface of the sintered CuNPs

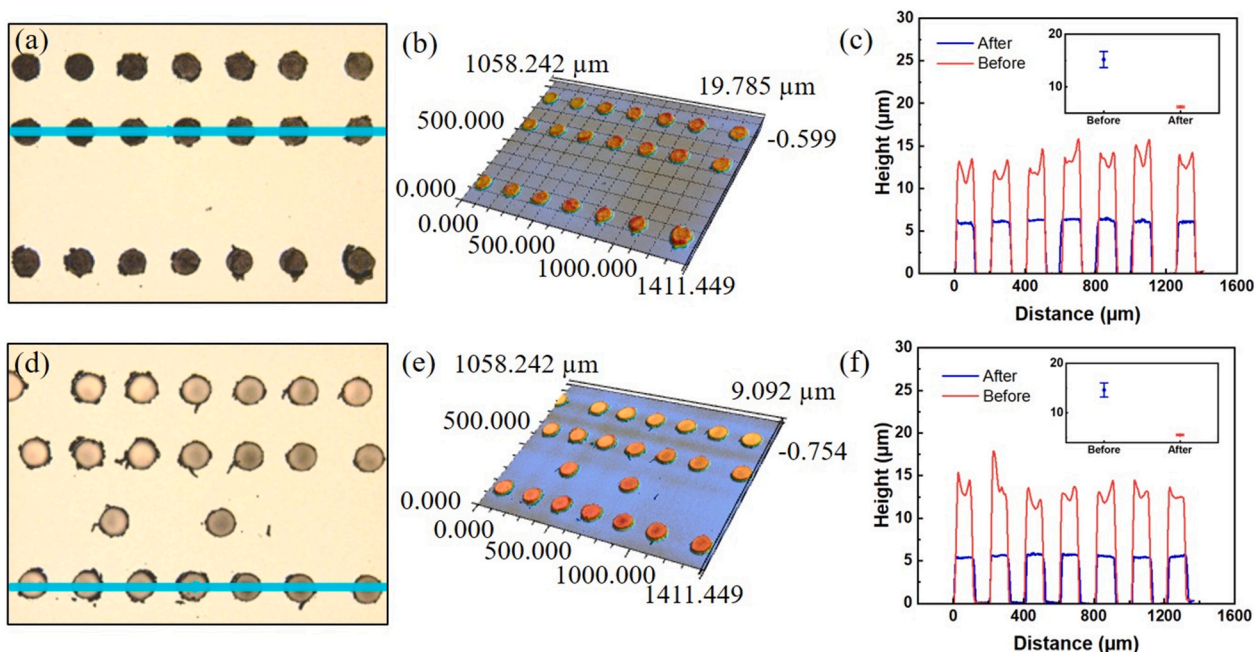


Fig. 5. Inspection of CuNPs bump sintered at 260 $^{\circ}\text{C}$ for 15 min with different pressure of (a)–(e) 15 MPa and (f) 25 MPa. (a) and (b) represent the top view of microscopy image for the sample before and after sintering, (b) and (e) represent 3D image of CuNPs bumps before and after sintering, (c) and (f) represent the profile of the CuNPs bumps sintered at 15 and 25 MPa, showing the profile before and after sintering in red and blue lines. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

bumps is more smooth than the as-printed CuNPs bumps in Fig. 5b.

Fig. 5c shows the height distribution of the CuNPs bumps after the sintering process, where the blue lines represent the profile of non-sintered and sintered CuNPs bumps, respectively. Obviously, the CuNPs bumps show almost the same height after the sintering process, which is caused by the compressive stress during the sintering process. For as-printed bumps, the highest height point on the top surface is selected to calculate the average height of the CuNPs bumps. The average heights of as-printed and sintered CuNPs bumps are around 15.18 μm and 6.19 μm and the height deviation is 1.65 μm and 0.18 μm , respectively. The height of sintered CuNPs bumps is only 59.22 % of the height of as-printed CuNPs bumps. Fig. 5f compares the average height profile of the CuNPs bumps (sample 6, sintered at 260 $^{\circ}\text{C}$, 25 MPa, 15 min) with sample 5. It is observed that as the pressure increase to 25 MPa, the average height of as-printed and sintered CuNPs bumps are around $14.63 \pm 1.54 \mu\text{m}$ and $5.55 \pm 0.16 \mu\text{m}$, respectively. The height of the CuNPs bumps is reduced by 62.08 % after sintering. It can be seen that the higher sintering pressure leads to higher compressibility.

3.2. Nanomechanical analysis of sintered CuNPs

To investigate the micro-scale mechanical properties of the CuNPs bumps, the CSM nanoindentation tests were performed under different maximum indented depths. Fig. 6 shows the stiffness-displacement curves of CuNPs bumps with different sintering parameters. Three groups of CSM nanoindentation tests were repeated for each sintering parameter. Fig. 6a–c presents the effects of sintering time, temperature, and pressure on the contact stiffness, respectively. For each group, a clearly aligned contact stiffness curve is selected to indicate the micro-scale mechanical properties of the sintered CuNPs material. Fig. 6d–f shows the performance of Young's modulus as a function of indented depth for the sintered CuNPs bumps. As reported by Li and Bhushan [23], the uniform material shows a linear relationship between indented depth and contact stiffness. This means that as the material becomes progressively harder, the contact stiffness increases with an ascending

slope when the contact depth increases. On the contrary, for a progressively softer material, the contact stiffness rises with a decreasing slope with increasing contact depth. Fig. 6a shows the contact stiffness of sintered CuNPs bumps with different sintering time (15, 30, 60 min) under 20 MPa and 300 $^{\circ}\text{C}$. For the samples sintered for 60 min, the slope of the contact stiffness decreases rapidly, while Young's modulus decreases with the contact depth, as shown in Fig. 6d, which indicates that the sintered CuNPs become softer from the surface to the deep location. In the cases of the samples sintered for 15 min and 30 min, the contact stiffness slope increases slightly with the contact depth, and Young's modulus has the same trend shown in Fig. 6d. It can be concluded that the samples sintered for 15 and 30 min present better homogeneity compared to the sample sintered for 60 min. To study the effect of sintering pressure and temperature on contact stiffness and Young's modulus, some samples were sintered at 260 $^{\circ}\text{C}$ for 15 min with different pressure (15, 20, and 25 MPa), and the other samples were sintered for 15 min with 20 MPa at different temperatures (220, 260, and 300 $^{\circ}\text{C}$). Fig. 6b shows the relationship between contact stiffness and indented depth under 15, 20, and 25 MPa. It is shown that both the contact stiffness and Young's modulus increase when the sintering pressure increases from 15 MPa to 25 MPa. However, when the sintering temperature increased from 220 $^{\circ}\text{C}$ to 300 $^{\circ}\text{C}$, the contact stiffness and Young's Modulus did not show a dependence on temperature.

Fig. 7 shows Young's modulus (black) and hardness (red) of the sintered CuNPs bumps under different process parameters. Fig. 7a illustrates the effect of sintering time (15, 30, 60 min) on modulus and hardness. First, Young's modulus remains at the same level of 116 GPa when the sintering time increases from 15 to 30 min; meanwhile, the hardness drops from 1.74 GPa to 1.59 GPa. Then, when the sintering time increases to 60 min, Young's modulus drops to 92 GPa, and the hardness increases to 1.77 GPa. It is reported that the modulus decreases continually when the sintering temperature is set at 300 $^{\circ}\text{C}$, which is attributed to the softening behavior between 200 and 300 $^{\circ}\text{C}$ [24]. As reported, the hardness of pure copper remains unchanged under annealing at 200 $^{\circ}\text{C}$, however, it reduces significantly after 300 $^{\circ}\text{C}$

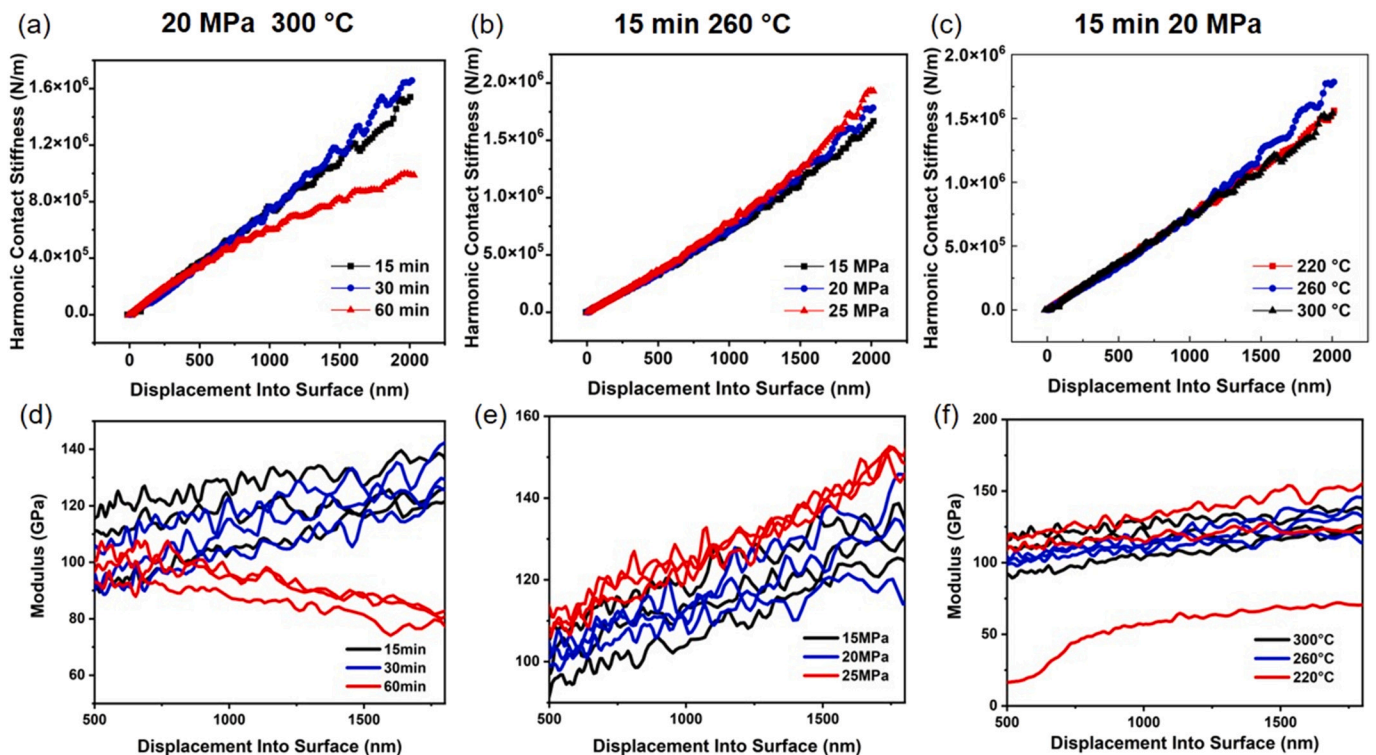


Fig. 6. Contact stiffness and modulus as a function displacement into the surface of CuNPs bumps with different (a) and (d) sintering temperatures of 15, 30, 60 min, (b) and (e) sintering pressure of 15, 20, 25 MPa, (c) and (f) sintering temperature of 220, 260, 300 $^{\circ}\text{C}$.

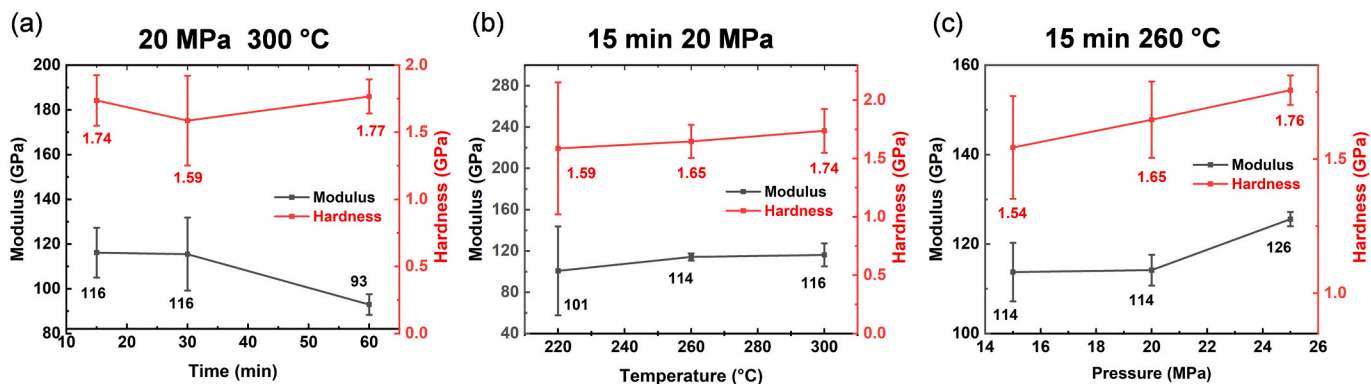


Fig. 7. The effect of sintering time of (a) 15, 30, 60 min, sintering temperature of (b) 220, 260, 300 °C and sintering pressure of (c) 15, 20, 25 MPa on the modulus and hardness.

annealing. The longer annealing time causes a more significant decrease in hardness. Young's modulus and hardness are to some extent coupled, so Young's modulus for the sample sintered with 60 min is lower than other samples. However, there is an increase in hardness for the sample sintered with 60 min.

Fig. 7b displays the effect of sintering temperature on Young's modulus and hardness of sintered CuNPs. The evolution of modulus and hardness exhibits a similar trend under different temperatures. When the sample was sintered at 220 °C, it presented that the average values of the modulus and hardness are 101 GPa and 1.59 GPa, respectively.

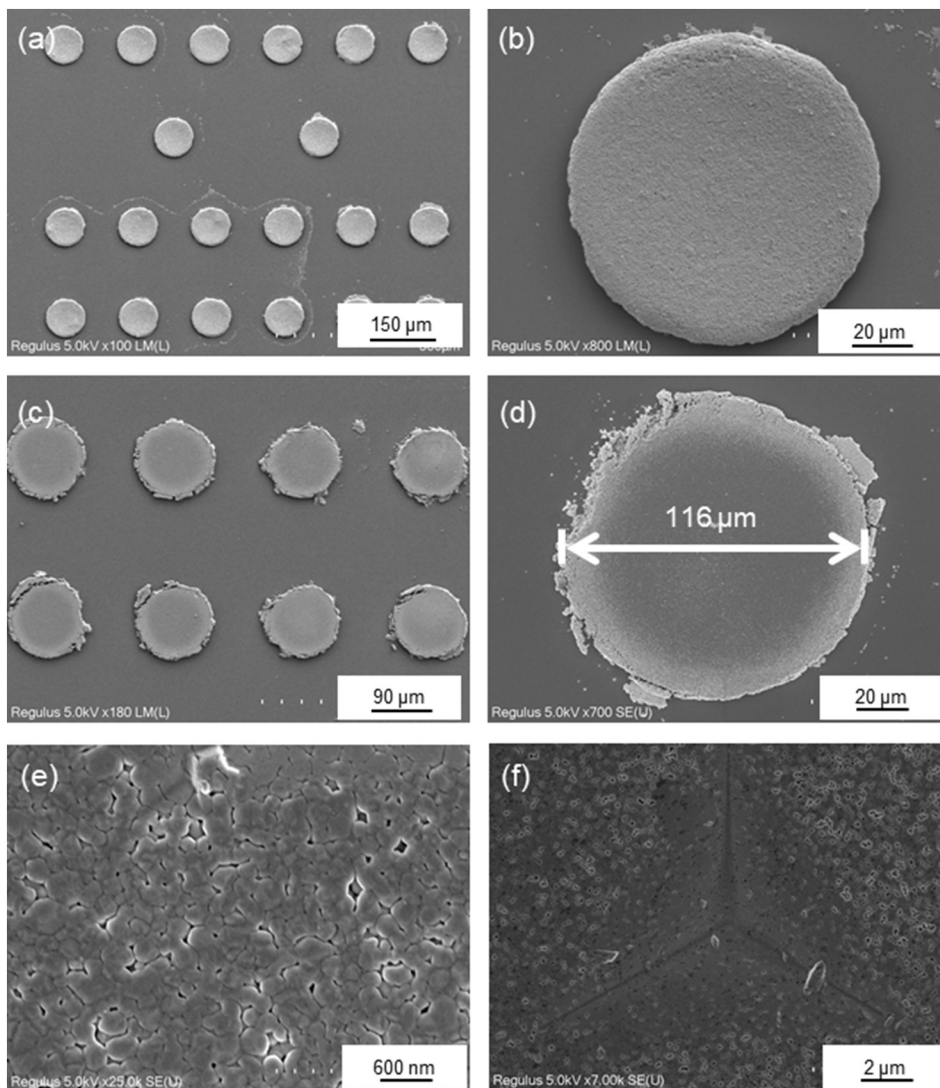


Fig. 8. (a) and (b) The SEM image of CuNPs bumps before sintering, (c)–(e) the SEM image of CuNPs sintered at 15 MPa and 260 °C for 15 min and (f) the SEM image of indentation test point.

When the sintering temperature increases to 260 °C, the modulus significantly improves, reaching 114 GPa with a 14.0 % increase rate, and the hardness is measured to be from 1.59 GPa to 1.65 GPa. With further increasing the sintering temperature to 300 °C, the result does not improve substantially in both modulus and hardness. At 300 °C, the modulus only slightly increases to 116 GPa, representing an increase rate of 1.8 %, while the hardness reaches 1.74 GPa, indicating a 5.5 % increase rate. Based on the above results, we selected the sintering temperature of 260 °C to investigate the effect of different pressures.

Fig. 7c shows the relationship among sintering pressure, Young's modulus and hardness. As the sintering pressure increases from 15 MPa to 20 MPa, Young's modulus remains constant at 114 GPa. Simultaneously, the hardness of the material increases from 1.54 GPa to 1.65 GPa. When a higher pressure of 25 MPa is applied, the modulus significantly increases to 126 GPa, corresponding to a 10.5 % increase. Compared to 128 GPa for bulk Cu, the sample sintered at 25 MPa is reasonable and approaches the ideal situation [25]. Additionally, the hardness at this pressure reaches 1.76 GPa. As discussed above, we achieved the highest modulus with 25 MPa pressure-assisted sintering at 260 °C for 15 min, based on the average value of modulus.

Actually, Young's modulus is highly determined by the microstructure of the sintered CuNPs. In this study, the sintering parameters (260 °C, 25 MPa) is recommended for this novel processing as sintered CuNPs under such temperature and pressure give stable and high Young's modulus and hardness. Meanwhile, the sintering time of 15 min is recommended for this processing. On the one hand, Young's modulus remains almost the same with the sintering time of 15 and 30 min. On the other hand, the less time will help to enhance the high throughput of packaging based on this processing.

3.3. Micro- and nanostructural analysis of sintered CuNPs

A Hitachi Regulus 8230 scanning electron microscope (SEM) was used to observe the micro- and nanostructure of CuNPs. Fig. 8a and b shows the SEM images of the non-sintered CuNPs array at different magnifications. It can be observed that the patterned CuNPs bumps have regular round shapes and smooth edges, corresponding to the photoresist mask after photolithography, as indicated in Fig. 2c. There are only a few bright copper nanoparticles on the substrate, which is due to the fact that the organic residue (NMP) with dissolved nanoparticles was not rinsed clean enough by deionized water after the lift-off process. These remaining CuNPs are bare; hence, there are no interconnects between neighboring CuNPs bumps. Consequently, the patterning process is completed successfully.

Fig. 8c and d shows the top view of sintered CuNPs bumps on a sample sintered at 15 MPa and 260 °C for 15 min (sample 5) after the dummy die peeled off from the substrate chip. Since the top dummy die is bare silicon, the CuNPs cannot be sintered on the silicon interface and can be detached easily. Peeling off the top die does not influence the CuNPs bump substrate. It can be observed from Fig. 8d that a central relatively dark area and a brighter edge area refer to the sintered and unsintered areas of CuNPs, respectively, which is caused by the compression of the uneven surface during sintering process. The surface of sintered CuNPs is illustrated in higher magnification in Fig. 8e, on which the indenter was imprinted to measure the CSM nanoindentation. It can be observed that the CuNPs on the upper surface are still quasi-spherical and constitute a porous network structure with the formation of sintering necks between adjacent CuNPs. The SEM image of the indentation spot on sample 5 is shown in Fig. 8f. As reported [26], a rapid change occurs at the beginning of the indentation measurement due to the observed compaction phenomenon until about 200 nm of penetration. The measurement data of nanoindentation were not stable near the surface of the CuNPs bumps, so we used the average data of the mechanical properties of CuNPs bumps from 0.2 μm of penetration of the indenter to the depth.

The cross-section of the sintered CuNPs bump on sample 5 (15 MPa,

260 °C, 15 min) was obtained by using focused ion beam milling (SEM-FIB, FEI Helios G4 CX), as illustrated in Fig. 9a. It is observed that sintered CuNPs is a porous structure and the formation of the sintering neck establishes a network on the cross-section. Nanoparticles were compressed in the vertical direction. The composition of the sintered CuNPs was analyzed using EDX to evaluate the oxygen content of the sintered CuNPs bump on sample 5. Fig. 9b shows the EDX result at the position indicated in the corresponding location in Fig. 9a. It is observed that there is only a small amount of oxygen, which is attributed not only to the residual organic additives but also to a slight surface oxidation on individual CuNP at the vacuum atmosphere. As a result, oxidation is not significantly detrimental to the sintering process, and vacuum sintering conditions are feasible for flip-chip interconnects.

Fig. 9c shows the SEM-FIB image of the cross-section for sample 1, which was sintered at 20 MPa, 300 °C for 60 min, leading highly sintered structures and extremely low porosity. It is observed that the CuNPs are almost a polycrystalline copper material. This sintering parameter combination can promote densification and reduce porosity in the sintered material. However, as discussed in the previous section, copper will present softening effect at the temperature of 300 °C, and the hardness has been enhanced when the sintering time increases from 15 to 30 min. As indicated by the red curve in Fig. 7a, the hardness of this sample was higher than those samples sintered for 15 and 30 min.

3.4. Electrical conductivity of sintered CuNPs

Electrical conductivity is essential for interconnect application of sintered CuNPs. An individual CuNPs bump on sample 5 (15 MPa, 260 °C, 15 min) was characterized in this study to measure the resistivity. The schematic of the four-point measurement setup is shown in Fig. 10a. Voltage was applied to the top left and right edge of the bump. Meanwhile, the voltage difference can be measured by landing the probes on the bottom left and right edge of the bump, and the current on the top-side contact can be characterized to eliminate contact resistance. A force voltage was applied to the CuNPs bumps sweeping from -0.5 to 0.5 V. The I-V characteristics are plotted in Fig. 10b, where the measurement data are fitted as a lineal relationship between voltage difference and force current. The measured resistance was extracted as 3.28 mΩ. Then, the resistivity of sintered CuNPs bump was derived from:

$$\rho = 4.532 \cdot t \cdot R \quad (6)$$

where t is the thickness of sintered bump, combined with the previously mentioned thickness of the bumps on sample 5 as 6.19 μm. R presents the measured resistance as 3.28 mΩ, extracted from the I-V curve. The resistivity of sample 5 is $9.2 \times 10^{-6} \Omega \cdot \text{cm}$, which is 5 times of the bulk Cu of $1.7 \times 10^{-6} \Omega \cdot \text{cm}$ due to its porous structure and slight oxidation. The resistivity of sintered CuNPs is related to their porosity and indicates the sintering quality. As a result, it can be concluded that the sintering parameter of sample 5 is feasible for the flip-chip interconnects in the aspect of electrical conductivity.

4. Conclusion

In this study, firstly, we developed a novel CuNPs patterning method for flip chip integration fabrication. The thickness of CuNPs interconnects bumps was determined by the photoresist thickness during the LSP process and the sintering parameter. The higher applied sintering pressure induced the higher compression of sintered bumps. The LSP process enables more freedom in the form of factor and thickness for CuNPs interconnects, which will contribute to the fabrication of dedicated stress relieve structures. Then, the mechanical properties of CuNPs material under different sintering parameters were evaluated by using CSM nanoindentation. Young's modulus and hardness were utilized to assess the homogeneity and the strength of sintered material. The less

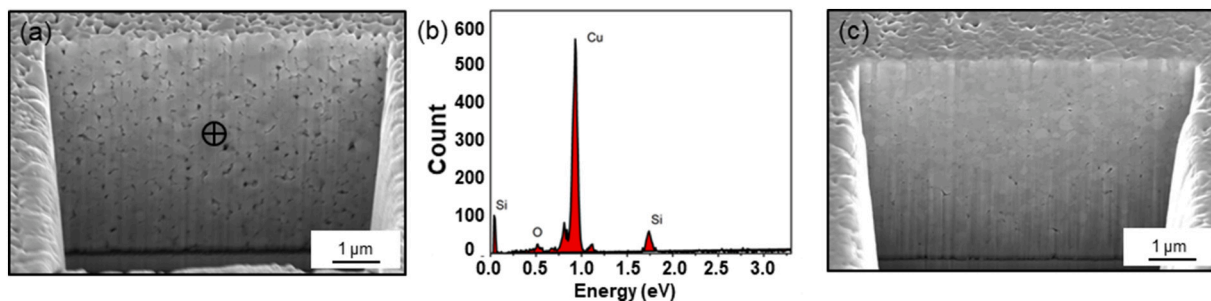


Fig. 9. (a) and (c) represent FIB/SEM images of the cross-section of the CuNPs bumps sintered at 15 MPa, 260 °C, 15 min and 20 MPa, 300 °C, 60 min, respectively.

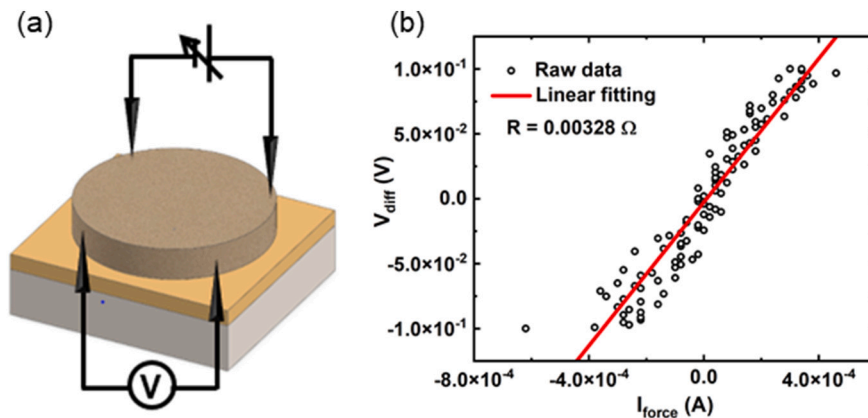


Fig. 10. (a) A sketch of a four-point measurement and (b) the I-V characteristics.

sintering time was beneficial to achieve a homogenous material and increased the productivity in the industry. The sintering temperature was adjusted to reach a suitable temperature of 260 °C. The increasing sintering pressure improved the sintering neck formation to strengthen the hardness of sintered CuNPs material. The combination of sintering parameters at 260 °C, 15 min, and 25 MPa is recommended, not only because it yields the highest Young's modulus of 126 GPa but also due to its high throughput during fabrication. Moreover, the sintered CuNPs have a nanoporous structure with slight oxidation. Therefore, they are more ductile than bulk Cu. In addition, the resistivity of sintered CuNPs was $9.2 \times 10^{-6} \Omega\text{-cm}$, which is 5 times of the bulk state. Therefore, these experiments revealed the optimal sintering parameter for CuNPs as an interconnect material and provided a high-throughput solution for CuNPs bumps patterning in the flip chip integration application.

CRedit authorship contribution statement

Xinrui Ji: Conceptualization, Methodology, Investigation, Writing – original draft. **Leiming Du:** Methodology, Investigation, Writing – review & editing. **Shan He:** Investigation. **Henk van Zeijl:** Writing – review & editing. **Guoqi Zhang:** Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgment

We would like to acknowledge the Penta Call 3 project SunRise ref. 17004 funding. We thank Dr. Xu Liu for providing the in-house nano copper paste and all staff in Else Kooi Laboratory for their technical support.

References

- [1] R.R. Tummala, Moore's law for packaging to replace Moore's law for ICS, in: 2019 Pan Pacific Microelectronics Symposium (Pan Pacific), 2019, pp. 1–6.
- [2] G.Q. Zhang, F. van Roosmalen, M. Graef, The paradigm of "more than Moore", in: 2005 6th International Conference on Electronic Packaging Technology, 2005, pp. 17–24.
- [3] R. Beica, Flip chip market and technology trends, in: 2013 European Microelectronics Packaging Conference (EMPC), 2013, pp. 1–4.
- [4] T. Siewert, S. Liu, D.R. Smith, J.C. Madeni, Properties of lead-free solders. Database for solder properties with emphasis on new lead-free solders, in: Release, vol. 4, NIST, 2002.
- [5] H.G. Song, J.W. Morris, F. Hua, The creep properties of lead-free solder joints, JOM. 54 (2002) 30–32.
- [6] H.W. Van Zeijl, Y. Carisey, A. Damian, R.H. Poelma, A. Zinn, C.Q. Zhang, Metallic nanoparticle based interconnect for heterogeneous 3D integration, in: 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016, pp. 217–224.
- [7] H.H. Yao, A. David Trigg, C.T. Chong, Study of electromigration behavior of Cu pillar with micro bump on fine pitch chip-to-substrate interconnect, in: 2014 IEEE 16th Electronics Packaging Technology Conference (EPTC), 2014, pp. 841–844.
- [8] D. Save, F. Braud, J. Torres, F. Binder, C. Müller, J.O. Weidner, W. Hasse, Electromigration resistance of copper interconnects, Microelectron. Eng. 33 (1997) 75–84.
- [9] A.O. Watanabe, Y. Wang, N. Ogura, P.M. Raj, V. Smet, M.M. Tentzeris, R. Tummala, Low-loss additively-deposited ultra-short copper-paste interconnections in 3D antenna-integrated packages for 5G and IoT applications, in: 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), 2019, pp. 972–976.
- [10] H. Yang, Study on the preparation process and sintering performance of doped nano-silver paste, Rev. Adv. Mater. Sci. 61 (2022) 969–976.
- [11] S.A. Paknejad, S.H. Mannan, Review of silver nanoparticle based die attach materials for high power/temperature applications, Microelectron. Reliab. 70 (2017) 1–11.

- [12] T. Wang, X. Chen, G.-Q. Lu, G.-Y. Lei, Low-temperature sintering with nano-silver paste in die-attached interconnection, *J. Electron. Mater.* 36 (2007) 1333–1340.
- [13] B. Zhang, A. Damian, J. Zijl, H. van Zeijl, Y. Zhang, J. Fan, G. Zhang, In-air sintering of copper nanoparticle paste with pressure-assistance for die attachment in high power electronics, *J. Mater. Sci. Mater. Electron.* 32 (2021) 4544–4555.
- [14] X. Liu, S. Li, J. Fan, J. Jiang, Y. Liu, H. Ye, G. Zhang, Microstructural evolution, fracture behavior and bonding mechanisms study of copper sintering on bare DBC substrate for SiC power electronics packaging, *J. Mater. Res. Technol.* 19 (2022) 1407–1421.
- [15] L. Del Carro, J. Zürcher, U. Drechsler, I.E. Clark, G. Ramos, T. Brunchwiler, Low-temperature dip-based all-copper interconnects formed by pressure-assisted sintering of copper nanoparticles, *IEEE Trans. Compon. Packag. Manuf. Technol.* 9 (2019) 1613–1622.
- [16] N. Shahane, K. Mohan, G. Ramos, A. Kilian, R. Taylor, F. Wei, P.M. Raj, A. Antoniou, V. Smet, R. Tummala, Enabling chip-to-substrate all-Cu interconnections: design of engineered bonding interfaces for improved manufacturability and low-temperature bonding, in: 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), 2017, pp. 968–975.
- [17] J. Zürcher, L.D. Carro, G. Schlottig, D.N. Wright, A.-S.B. Vardoy, M.M.V. Taklo, T. Mills, U. Zschenderlein, B. Wunderle, T. Brunchwiler, All-copper flip chip interconnects by pressureless and low temperature nanoparticle sintering, in: 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016, pp. 343–349.
- [18] N.J. Briot, T.J. Balk, Focused ion beam characterization of deformation resulting from nanoindentation of nanoporous gold, *MRS Commun.* 8 (2018) 132–136.
- [19] Y. Champion, M. Laurent-Brocq, P. Lhuissier, F. Charlot, A. Moreira Jorge Junior, D. Barsuk, Understanding the interdependence of penetration depth and deformation on nanoindentation of nanoporous silver, *Metals* 9 (2019) 1346.
- [20] N. Huber, I. Ryl, Y. Wu, M. Hablitzel, B. Zandersons, C. Richert, E. Lilleodden, Densification of nanoporous metals during nanoindentation: the role of structural and mechanical properties, *J. Mater. Res.* 38 (2023) 853–866.
- [21] X. Long, B. Hu, Y. Feng, C. Chang, M. Li, Correlation of microstructure and constitutive behaviour of sintered silver particles via nanoindentation, *Int. J. Mech. Sci.* 161–162 (2019), 105020.
- [22] J. Fan, D. Jiang, H. Zhang, D. Hu, X. Liu, X. Fan, G. Zhang, High-temperature nanoindentation characterization of sintered nano-copper particles used in high power electronics packaging, *Results Phys.* 33 (2022), 105168.
- [23] X. Li, B. Bhushan, A review of nanoindentation continuous stiffness measurement technique and its applications, *Mater. Charact.* 48 (2002) 11–36.
- [24] X. Zhang, Y. Yuan, S. Zhao, J. Zhang, Q. Yan, Microstructure stability, softening temperature and strengthening mechanism of pure copper, CuCrZr and Cu-Al₂O₃ up to 1000 °C, *Nucl. Mater. Energy* 30 (2022), 101123.
- [25] G. Eason, B. Noble, I.N. Sneddon, J.E. Lennard-Jones, On certain integrals of Lipschitz-Hankel type involving products of Bessel functions, *Philos. Trans. R. Soc. Lond. Ser. A Math. Phys. Sci.* 247 (1997) 529–551.
- [26] S. Fakiri, A. Montagne, K. Rahmoun, A. Iost, K. Ziouche, Mechanical properties of porous silicon and oxidized porous silicon by nanoindentation technique, *Mater. Sci. Eng. A* 711 (2018) 470–475.
- [27] W.C. Oliver, G.M. Pharr, Measurement of hardness and elastic modulus by instrumented indentation: advances in understanding and refinements to methodology, *J. Mater. Res.* 19 (2004) 3–20.
- [28] D. Tabor, *The Hardness of Metals*, OUP Oxford, 2000.
- [29] A.A. Volinsky, W.W. Gerberich, Nanoindentation techniques for assessing mechanical reliability at the nanoscale, *Microelectron. Eng.* 69 (2003) 519–527.