Monolithically fabricated flexible graphene-based active implant

MSc. Biomedical Engineering

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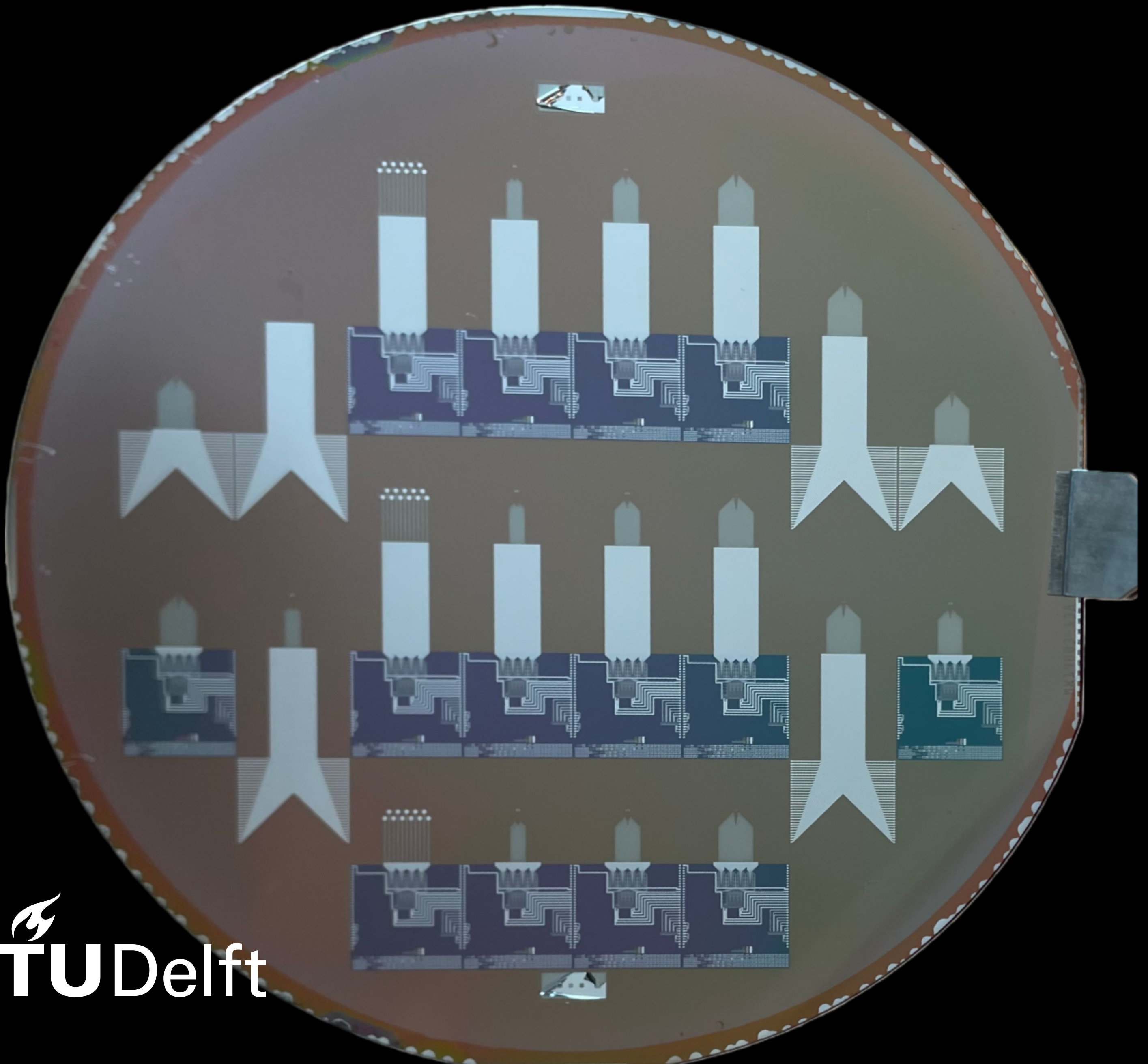

TU Delft

Monolithically fabricated flexible graphene-based active implant

by

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Cover Image: Fully processed wafer of the reported process

TU Delft

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Abstract

Treatment of diseases, illnesses or disorders are always sought without any undesired side-effects and complications. Neurological disorders, such as Epilepsy and Parkinson's, are currently treated using pharmaceuticals. However, drugs have a low specificity and lose their effectiveness after several years. In addition, prolonged drug usage often leaves patients with many side-effects and complications.
Development in neuroscience indicate the treatment of such neurological disorders via neuro-stimulation. Currently, research in understanding the mechanisms behind neuronal stimulation is carried out by research institutes all around the globe. There are three modes for neuronal stimulation, electrical, optical and lastly the use of ultrasonic waves. As optogenetics provides a more specific technique in neuronal stimulation and electrical recording can provide high spatial resolution data, it is sought to combine this two modes.

This work reports the development of a monolithically fabricated active implant, with optogenetic compatibility using transfer-free graphene electrodes. To achieve this desired goal, a microfabrication process is developed, which is reproducible and scalable with modern day microfabrication technology. In order to be compatible with optogenetics, graphene electrodes are used, as these are transparent and allow for neuronal stimulation using light. The graphene electrodes are grown on a pre-defined molybdenum catalyst, allowing for a transfer-free chemical vapor depostion (CVD) of graphene. Micro-electrode-arrays (MEAs) are developed, using graphene electrodes, that include different sized electrodes and different amount of electrodes. The amount being constrained by the available space on the cortex of a mouse.

The aim of this work was to be able to control or read out these MEAs using electronics developed alongside the electrodes. As graphene is grown at a temperature above the melting point of aluminium, conventional CMOS technology can not be used in combination with graphene electrodes. The process developed, did not include any materials which would be damaged during the graphene growth. The metal gate is replaced by a polysilicon gate and the metal interconnects connecting the active devices and the MEAs are defined after the growth of graphene. Resulting in an active implant which is monolithically fabricated in combination with a transfer-free graphene process.

Monolithically fabricating an active graphene based implant, comes with complications. Delamination of the passivisation layer occurred whilst trying to open contact openings to and from the active devices. This was resolved using a more appropriate chemical etchant.

A fully monolithically fabricated active graphene-based implant was obtained. Electrical measurements showed that the active devices did not behave as expected. Revisiting simulations, it was established that there was leakage of dopants from the gate to the channel. This results in the NMOS devices to be always on and the PMOS devices to have a higher threshold voltage.

However, this particular wafer, had many high temperature steps after the doping of the polysilicon. Reduction of these high temperature steps result in less doping getting into the channel. Alternatively, a thicker gate oxide can be used, to serve as a more robust barrier. A last proposed solution is the reduction of the doping concentration and doping energy of the polysilicon, which would result in less dopant being near the gate oxide interface and thus less dopant leaking into the channel.

There are wafers included in this work with less high temperature steps. However, due to time limitation it was not possible to finish production of these wafer in order to confirm it experimentally. Nevertheless, it is believed that with minor adjustments, this research project is a viable foundation for active graphene based implants and structures.

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Nomenclature

Abbreviations

Abbreviation	Definition
AED	Anti-Epileptic Drug
QOL	Quality Of Life
CMOS	Complementary Metal-Oxide-Semiconductor
TCAD	Technology Computer Aided Design
SPICE	Simulation Program with Integrated Circuit Emphasis
MEA	Micro-Electrode-Array
AP	Action Potential
DBS	Deep Brain Stimulation
ROI	Region Of Interest
SNR	Signal-to-Noise Ratio
ADC	Analogue-to-Digital Converters
ITO	Indium-Tin-Oxide
EKL	Else Kooi Lab
BICMOS	Bipolar CMOS
TEOS	TetraEthyl OrthoSilicate
GPOS	Graphene-compatible-Polysilicon-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
CO	Contact Opening
IC	Inter-connects
LOCOS	LOCal Oxidation of Silicon
STI	Shallow Trench Isolation

Symbols

Symbol	Definition	Unit
V_{th}	Threshold voltage	[V]
C_{ox}	Gate oxide capacitance	[F]
$R_{\square}$	Sheet resistance	[$\Omega/\square$]
X_j	Junction Depth	[m]
t_{ox}	Gate oxide thickness	[m]
N	Doping concentration	$atoms \cdot cm^{-3}$
BHF	Buffered HydroFluoric Acid	(1:7)
HF	HydroFluoric Acid	(0.55%)
H_3PO_4	Phosphoric Acid	(85%)
PES	Phosphoric Acid Etching Mixture	(77-19-4)
HNO_3	Nitric Acid	(69.5%) and (99%)

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1
Introduction

In the field of human healthcare it is always sought to achieve the targeted treatment of diseases and illnesses. This includes avoiding undesired side-effects and complications. Conditions such as epilepsy and Parkinson's are associated with a neurological disorder and are currently mostly treated via pharmaceutical approaches.

Epilepsy is a disorder, in which the brain activity becomes abnormal causing seizures, periods of unusual behaviour or sensation, and sometimes loss of awareness. The symptoms can vary widely, and having a single seizure doesn't mean you have epilepsy. Having two unprovoked seizures within 24 hours is often required for an epilepsy diagnosis. For the treatment of epilepsy there are several drugs that can be prescribed, these all fall under the umbrella of anti-epileptic drugs (AEDs). Choosing a drug is patient dependent, whether they are pregnant, elderly, overweight and many other factors, even including the type of seizure. The most suitable treatment is only established via trial and error [1].

Epilepsy is one of the most common neurological disorders, affecting over 70 million people worldwide [2]. Current data suggests that epilepsy is occurring more often in poor countries, in particular rural areas [3]. This is most likely due to the lack of education and access to treatment via AEDs. The type of seizures can be divided up into 3 main categories, partial seizures, generalised tonic-clonic seizures and absence seizures.

Another neurological disorder is Parkinson's. Parkinson's is a disorder which causes movement problems, such as rigidity, slowness and tremors. It occurs when nerve cells in the basal ganglia become impaired or start to die. These neurons usually produce dopamine, and as the production of dopamine gradually become less due to the disorder, the symptoms become more severe [4]. Parkinson disease has multiple non-motoric symptoms, such as depression, dementia, sleep disorders and autonomic dysfunctions [5]. Due to the severe symptoms, one third of people suffering from Parkinson's lose employment within a year after diagnosis, and the majority are no longer full-time employed within 5 years [6].

Globally, 6.1 million individuals are diagnosed with with Parkinson disease, which is 2.4 times higher than in 1990. This increase is attributed to improved methods in the detection and diagnosis of Parkinson's. Also, due to the larger awareness, higher life expectancy and possibly due to increased environmental exposures, such as pesticides, solvents and metals [7]. The course of the disease varies considerably, but those diagnosed early in adulthood live longer with the disease than those diagnosed later in life [8]. Currently Parkinsons is incurable, but current pharmaceutical therapies can improve the quality of life (QOL) for several years. However, these drugs have low specificity and lose their effectiveness after several years, leaving patients helpless with many side-effects from prolonged drug usage. Current developments in neuroscience enable a more targeted approach to the treatment of these neurological diseases, which leads to less side-effects and complications with similar improvement to the QOL.

Neural stimulation for the treatment of neurological diseases has been an active research field for several decades now. Work done in recording and understanding the neural response has given healthcare an opportunity to seize control. It has already been shown that neuronal stimulation can be an effective and useful alternative to the treatment for certain illnesses.

A thoroughly investigated topic within the field of neuroscience has been optogenetics, as it offers advantages over traditionally used electrical stimulation. As for cell to be stimulated using optogenetics, it is required to first genetically modify the cells so that they are sensitive to light, greatly enhancing the resolution of activation that can be achieved. However, understanding the biological mechanisms behind stimulation of tissue requires measurements of the stimulated tissue.

Combining the fields of optogentics with devices which operate in the electrical domain could offer the solution. By using optogenetics to stimulate the desired neuronal tissue whilst simultaneously recording the electrical activity using electrodes. Or visa versa, using electrical stimulation and recording neuronal response using optics. Unfortunately, conventional electrodes are often made using non-transparent metals, like titanium, limiting the use in combination with optics. Graphene has been proposed as a solution, boasting high mobility, low electric noise and transparency.

Several methods are developed to fabricate graphene, but the use of chemical vapor deposition (CVD) on a metal catalyst is currently regarded the most promising in regards to large area synthesis. In order to achieve the full potential of graphene, the metal catalyst used needs to be removed. Resulting in methods being developed for transferring graphene onto dies. However, transferred graphene often suffers from poor adhesion and reduced quality of the graphene due to the transfer. As the transferring process is so challenging, large scale production, high yield, wafer-to-wafer uniformity and production time are limited. As such, this work incorporates a transfer-free, CMOS compatible graphene fabrication process. Also the incorporation of electronics in combination with graphene is desired to further miniaturise the devices. Miniaturisation is desired as implants are often restricted in size due to the site of implantation.

1.1. Aim of the project

As previously mentioned, a solution for simultaneous stimulation and recording is desired in the field of neuroscience. This work we will take a closer look at improving neuronal stimulation by trying to bring the field of electrical neurological stimulation and the field of optogenetics closer together. The use of transparent electrodes enables the simultaneous use of both optogenetics and electrical stimulation or recording.

With this goal in mind, several research questions are addressed in this work. For instance, can a graphene electrode array be manufactured on the same wafer as active devices? How can a small circuit be designed for single electrode read-out? Can a small enough electrode array be manufactured for single cell recording?

Therefore, the aim of this work is to prove the development by means of a single wafer microfabrication, a graphene-based active implant that has the prospect for optical stimulation and simultaneous single-cell electrical recording of neuronal tissue via a MEA.

The proposed solution is the use of graphene electrodes, but as the growth of graphene is yet not incorporated monolithically with complementary metal-oxide-semiconductor (CMOS) technology due to several challenges. One challenge is the material choices, as the materials need to be resilient against the high temperatures during the growth of graphene. This means that the melting point of all materials must be much higher then the temperature at which graphene is grown. Also, the high temperature during CVD graphene growth can cause the active devices to act differently due to unpredictable diffusion of the active regions. To avoid this, simulations of device characteristics should be made. For real-world testing, various test-structures are used to confirm proper device functionality.

This work will demonstrates the use of this new technology with simple digital circuits for reading out the electrodes. Challenges will include the design of these circuits, before having the technology characterised. Preliminary designing the circuitry is a more cost-effective and time efficient method, and ensures that it can be included within the time span of this work. Technology computer aided design (TCAD) simulation data is fed into Simulation Program with Integrated Circuit Emphasis (SPICE) models, which then can be used to simulate circuitry. Test structures of these circuits are also placed, so that measurements can confirm proper circuit functionality.

Lastly this works aims to design micro-electrode-arrays (MEAs) that can be used within the small space available of a mouse's brain. These size limitations need to be taken into account when designing the MEAs. And as the diameter of the electrodes are reduced for a higher spatial resolution, the wiring of these electrodes becomes a larger challenge. A concept of the envisioned device can be found in figure 1.1, in which the electronics are depicted by the brown square and the MEAs are located on the tip of the suspended structure.

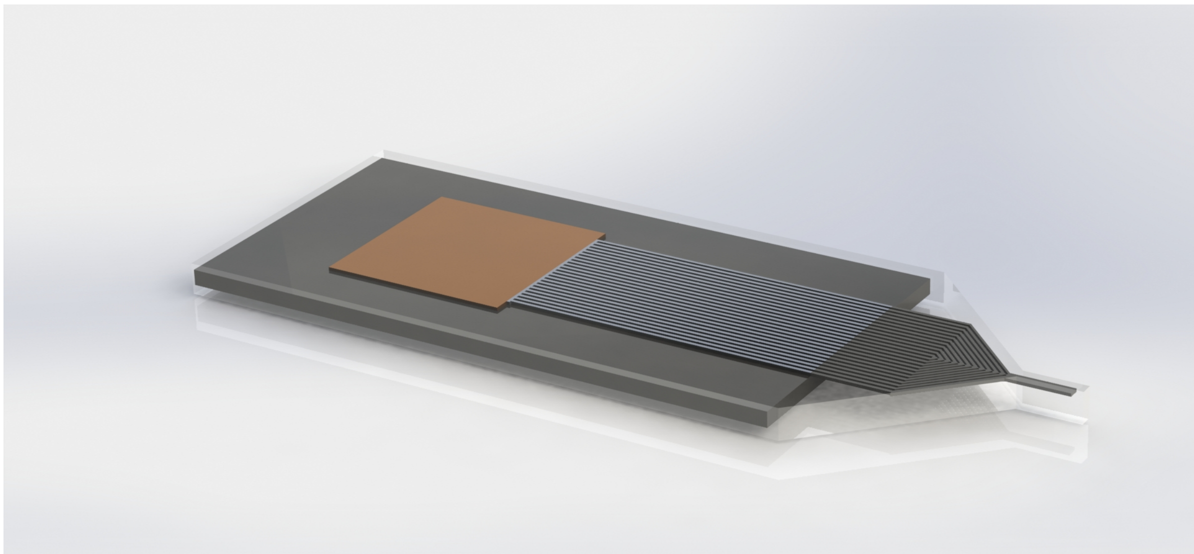


Figure 1.1: Envisioned device with selected materials per region.

2 State of the art

Neurons are fundamental cells of the brain and the nervous system and the cell bodies have an approximate diameter of 15 μm to 20 μm [9]. These cells are responsible for receiving and transporting electrical signals from and to organs within an organism. The electrical signals are carried via the neurons cell membrane, which is kept at a resting potential of about -75 mV [10]. Excitation of these cells trigger an action potential (AP) which is then carried along the neurons to other neurons and eventually to their target organs. A low-intensity depolarising stimulus produces a graded response, but only a large enough stimulus exceeding a critical value will trigger an AP. When the stimulus is above this threshold value, the APs waveform is independent of the intensity of the stimulus.

There are several methods in triggering an AP, research has been done in chemical, optical, mechanical, magnetic and most commonly electrical stimulation. To achieve targeted treatment, it is important to be able to target specific neurons. Single cell stimulation has been achieved using aforementioned techniques [11]. For electrical stimulation MEAs are used to target single-cells or a specific area of cells. In the optical domain single cell stimulation has been demonstrated using techniques such as two-photon optogenetics. Making use of red-shifted chimeric opsin, activation of selected neurons in 3 dimensions can be achieved [12].

Just like pharmaceuticals, these techniques also have their drawbacks. Even though MEAs enable targeted stimulation of single cells, simultaneous monitoring of the excited cells is still a gap. Current state of the art devices used in neuronal stimulation or recording still lack this capability and also come with issues regarding spatial resolution due to the distance between electronics and electrodes. The use of transparent electrodes would enable simultaneous monitoring or stimulation in combination with optical imaging, closing the loop between recording and stimulation. Using optogenetics for stimulation would also be beneficial as this would mean an increase in the resolution of activation in comparison to electrical stimulation. This is because for cells to be activated using optogenetics it is required to first genetically modify the cells. The high specificity in which the cells can be modified and the high precision that can be achieved with focused light, gives optogenetics the highest selectivity in single-cell stimulation.

Currently, electrical stimulation of the cells is the most common approach in triggering or inhibiting an AP. For the treatment of neurological diseases, the electrodes need to be implanted near the site associated with the disease. This is also the case for recording electrodes, in order to measure the desired signal, the electrodes have to be near the tissue.

As discussed in chapter 1, for many neurological diseases the site associated is deep within the brain. To stimulate these sites a method known as deep brain stimulation (DBS), which is a highly invasive procedure, is often used. But as it is shown that the referral to a neurologist in cases of individuals suffering from Parkinson disease is associated with a decrease in morbidity, mortality and nursing home placements [13].

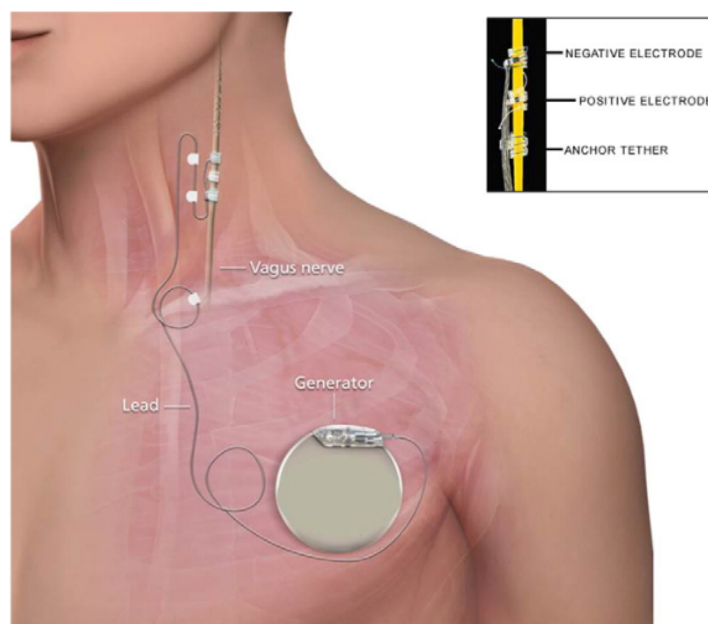


Figure 2.1: Vagus nerve stimulation device placement in upper chest. [16]

Current development in neurology indicates also treatment of neurological diseases via stimulation of the vagus nerve [14], avoiding the invasive procedure required for DBS. An example of such a device implanted is depicted in figure 2.1. Devices, such as *Percept PC A*, are hermetic sealed devices implanted around the upper chest. Long leads are then needed to connect the devices to the electrodes. As the pulse generator is large, the upper chest is the closest place it can be implanted, but still causing a large uncomfortable bulge. Furthermore, as relative movement between the site of implantation of the electrode and the pulse generator, the leads connecting these two are under heavy load and have risk of breaking. The need for the leads to be implanted along the neck is also an extremely difficult surgical endeavour. The shear size of these devices, due to the large metal housing and the large batteries, leave a mismatch between the devices and the human body and can cause a lack in the well-being and comfort of the patients. The complicated procedure to implant such a device can also cause infections and other complications after implantation[15].

It is therefore desired to have a much smaller device, with material properties similar to the surrounding tissue. This reduction in size enables the implantation of such devices directly near the region of interest (ROI). Rigid shanks with MEAs on the tip would allow for DBS, whereas flexible MEAs would allow for peripheral nerve stimulation.

The reduction in size is not only beneficial for the patients comfort and health, it also improves the quality of therapy that can be provided, as the electronics can be brought closer to the recording site, which has several benefits. An obvious benefit is in amount of available channels, which improves the spatial resolution of the device. A widely used approach to achieve a better understanding of the neuronal network properties is the use of MEAs. Reduction of the electrodes size allow for recording in sub-cellular resolution, improving the understanding of neuronal activity. As depicted in figure 2.2, a high spatial resolution MEA allows for recording at several location of a single neuron. Furthermore, fitting more of these smaller electrodes into the device allow for a larger area to be recorded. The combination can unlock the capability for constraining full-compartmental neuron models.

The reduction of the distance between the site of recording and the electronics has the benefit that it improves the quality of the measured signal. It is important to have a sufficiently high enough signal-to-noise ratio (SNR). There are multiple factors contributing to the noise during a recording. The major contributors can be split up in three categories, the noise due to the tissue around the ROI, the noise due to the interface between the ROI and the device and lastly the noise contributed by the device itself.

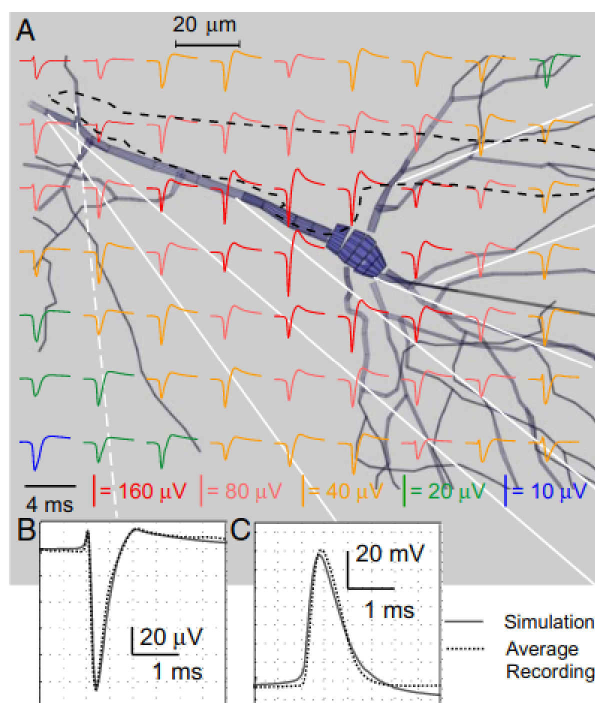


Figure 2.2: (A) The extracellular action potentials (EAPs) in a grid plotted over a neuron. **(B)** Enlarged image of EAP **(C)** Comparison of simulated intracellular signal to the recording. [17]

The most important contributor from these is the noise contributed by the tissue around the ROI, also known as the biological noise. This noise stems from the electrical activity of other cells around the ROI. This can be the APs of other cells or even due to the stochastic nature of synaptic transmission between neurons. From experimental and theoretical studies it has been shown that neurons can contribute to the recording of the ROI located farther than 100-150 μm from the recording electrode [18] [19]. To be able to work with this noise contributor it is important to be able to also model it. Efforts have been made in creating models that describe the contribution of biological noise to electrical recording [20]. These models allow for more accurate simulations and thus leading in more accurate devices.

The second contributor to the noise is the electrode-electrolyte interface. At lower frequencies, the interface can produce noise with a steep roll-off of $1/f$ or even $1/f^2$ [21]. However, this is at frequencies below 5-10Hz, the more pressing noise contributor at the interface is at higher frequencies. As at higher frequencies the thermal noise will start to play a bigger role. Studies on the use of platinum electrodes for neural recording show that, in a frequency band from 100 Hz to 10 kHz, the noise is the same as the thermal noise from the real part of the electrode impedance. This is a summation of the polarisation resistance and the access resistance of the electrodes [22].

Lastly, a major source of noise is the device noise. This includes the noise caused by the wires and the electronics. Even with a sufficiently thick passivisation layer, the wires still have parasitic noise contribution which is dependent on their dimensions. To increase the SNR for this contribution a sufficient amplification of the signal has to be done before the signal is passed through the wire. In other words, the front-end amplifier should be placed as close as possible to the electrode. This does make the noise from the front-end amplifier the largest contributor of noise from the electronics, but reduction of this contribution is well studied within the realm of micro-electronics.

The inclusion of electronics near the electrodes have another benefit, especially for electrodes used in combination with shanks, as this add the possibility to reduce the amount of wiring and contact pads needed. Often connectivity of shanks are limited, as wiring to and from the electrodes usually can not be done all around the electrodes, but instead often have to go into a singular direction of the shank. In-

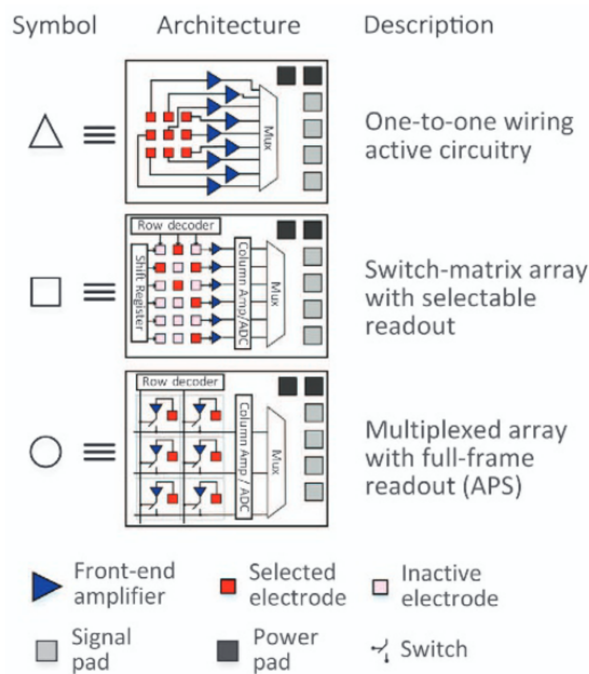


Figure 2.3: Common architectures used for front-end read out circuits [23]

creasing the amount of electrodes subsequently increase the amount of wires needed. And increasing the width of the shank containing the wires beyond 50-80 μm, a noticeable loss of neural signals can be noted, making this range the upper limit [23]. And as the width of the wires is limited by the technology used, and taking in account that each wire has to be adequately spaced, the device is limited in the maximum amount of electrodes that can be used.

However, the integration of electronics closer to the electrodes, can lead to reduction in the width of the shank needed and an increase of the electrodes that can be used. This can be achieved using several methods, each having their advantages and disadvantages. These methods, listed in figure 2.3, mainly involve moving the electronics close to the electrodes, so that only a few essential connection are needed to communicate with or power the device. These electronics usually also include analogue-to-digital converters (ADCs) for data serialisation, to even further reduce the wiring needed.

Besides miniaturisation of the device, it is also important to take the working of the device in account. And unfortunately, electrical stimulation also has its drawbacks. Foremost, the large stimulation artefacts during the use of electrical stimulation of tissue. As the electrical stimulus will leak to surrounding tissue, instead of purely focusing on the ROI. A solution is found in the combination of the electrical and optical domain. As optogenetics allows to target specific neural sub-circuits, through genetic manipulation [24]. It is therefore sought to combine the power of optogentics with electrical recording, in order to create a closed loop between stimulation and recording. The three limiting factors in order to combine electrical stimulation and optical imaging is the transparency and the conductivity and flexibility of the material. Common materials for bio-compatible electrodes, such as titanium, lack the transparency required to perform simultaneous imaging.

Indium-tin oxide (ITO) has been demonstrated as a alternative material, which enables simultaneous optical stimulation and electrical recording. Unfortunately, ITO is also known to be a brittle material, and thus incompatible with the flexibility required for implantation in the body [25]. Graphene electrodes have also been proposed as an alternative material for the electrodes. It has been demonstrated that graphene electrodes can be used for optical imaging compatible neural implants. However, the combination of electronics with graphene in a monolithic fashion still remains a challenge. Previous works already demonstrated the creation of active graphene electrodes, using flip-chip bonding techniques. However, this leads to thick structures around the chip area, which can cause issues with the encapsulation of the entire device. Therefore, a monolithic approach is preferred.

2.1. Approach for monolithic fabrication of envisioned device

There are several approaches to achieve monolithic fabrication of the device. You can divide the process up in 3 important stages. Active component definition, graphene electrode definition and encapsulation. It is evident that encapsulation of the devices should be done last. But one could argue between first defining the electrodes followed by the active device definition or the other way around. However, it is important to note that graphene is highly contaminating and extreme fragile. So in order to be able work with CMOS compatible machines and to protect the graphene during the harsh environments of producing CMOS technology, it is desired to do graphene definition as far towards the end of the process. For this reason the approach will be to first fabricate the graphene-compatible active device technology, followed by the graphene electrode definition and lastly the encapsulation of the device.
This work will try to show that it is possible to work with graphene inside a CMOS production line. As cleanrooms that produce such active devices are extremely aware of their cleanroom environment and possible contaminates. Also Else Kooi Lab (EKL) is aware of possible contaminates, so after the contaminating process of graphene growth, certain machines are not allowed to be used.

3

Development of graphene compatible polysilicon oxide semiconductor (GPOS)

Firstly, a novel technology is presented which is compatible with the use of graphene and reproducible within the cleanroom facilities of EKL. As presented in chapter 1, it is desired to first define the active areas before defining the MEAs. Currently *BICMOS5* is the most common technology used within EKL. This technology combines two semiconductor technologies, Bipolar and CMOS technology in a simple manner. As this process is widely used within EKL, this technology is already well defined, and it allows the IC designer the use of multiple active components, such as NMOS, PMOS, BJTs and diodes. The *BICMOS5* technology consists of a simple silicon oxide gate, aluminium gate and a Tetraethyl orthosilicate (TEOS) passivisation layer which will form silicon oxide. The active devices are built within an epitaxial silicon layer, which is p-type doped with boron.

However, for this work the active devices, including the gate, have to be manufactured before the graphene is grown. It is important to note that as graphene is grown at a temperature of 935 °C, and most metals can not be used during the manufacturing of the active devices. And as *BICMOS5* makes use of an aluminium gate, this technology is not compatible with the desired order of production.

A possible solution is to use polysilicon, as the melting point of polysilicon is around 1400 °C. Another solution is to still use the existing technology, but to replace the aluminium gate with another metal, a metal which is resistant to the high temperature during the growth of graphene. Most modern CMOS technology nodes already make use of such metals, as there are also several issues with the use of polysilicon as the gate material. As these more exotic materials are unavailable within the cleanroom facilities of EKL, it is still chosen to use polysilicon as the gate material.

As for these reasons, a new technology was developed. This technology is compatible with the high temperature required to grow graphene and is also compatible with the available facilities in EKL. The technology is named appropriately graphene-polysilicon-oxide-semiconductor (GPOS).

3.1. GPOS technology features

As this is an undefined technology, the first step is to choose the desired features that shall be included within this technology. However, during selection of these features it is important to take in consideration the limited available facilities within EKL.

The first decision to be made is to choose the substrate, as this affects all consecutive decisions. Just like many other technologies it is desired to choose a p-type substrate. The reason for this is that stems from the fundamental working principle of NMOS an PMOS devices. When a n-type substrate is used, the NMOS devices need to be manufactured inside of a p-well. For a p-type substrate, the PMOS devices need to be manufactured within a n-well. But to obtain the fastest NMOS speed, it is preferred to use the higher resistivity p-type wafer over the higher doped p-well in a n-type substrate, which would lead do a lower resistivity in the bulk.

The second feature that is critical in the GPOS technology is the use of an epitaxial layer, as depicted in figure 3.5a. Building the active devices in an epitaxial layer has two major advantages over using the substrate. Firstly, the epitaxial layer can be tuned precisely to change the doping concentration of the layer. Whereas this is not possible when using diffusion or ion implantation techniques, which would be needed to change the doping concentration of the wafers. Secondly, as the physical and chemical properties of epitaxial layer can be tuned to be different to the bulk material, which can be advantageous for devices that would for example require a lower doped region on top of a higher doped region. As this is unachievable using implantation of diffusion.

The third decision is the inclusion or exclusion of bipolar transistors. It is possible to include bipolar transistors similar as has been done in the *BICMOS5* process. To include bipolar transistors it is needed to have an extremely good control of the diffusion. The yet unknown influence of the CVD graphene growth step makes it that the bipolar transistor are excluded in the design of the technology, simplifying the process.

For most active devices the use of NMOS as well as PMOS devices is needed. As for this reason the NMOS and PMOS devices can be located closely next to each other. Local Oxidation of Silicon (LOCOS) is used to avoid unwanted electric current leakage between adjacent devices, limiting cross-talk but more importantly preventing latch-up. The implementation of this feature can be seen in figure 3.5c. There are also other possible features to resolve the cross-talk issue, such as the now more common shallow trench isolation (STI), but these features are more complex and often can not be made within the facilities of EKL.

As previously discussed the gate will be made using polysilicon, but just pure polysilicon is a semiconductor and needs to be doped in order to be used as the gate material. The polysilicon is doped using phosphorous (P^{+}). Phosphorous is a n-type dopant, as the defects that are caused implanting this atom will have a free electron when replacing a silicon atom in the crystal lattice. The fact that polysilicon is a semiconductor works again in the favour of creating devices for biomedical applications. To understand why, we must look at the physics in play. After doping the polysilicon there are free flowing electrons available in the polysilcon. As the epitaxial layer is p-type, this layer has free flowing holes. For a NMOS, when a positive bias is applied to the gate, the electrons will collect at the the top of the gate. Creating a positively charged surface at the bottom, this surface can more easily push away the holes that are present in the bulk, easing the opening of the gate as can be seen in figure 3.3. This is known as the polysilicon depletion effect and reduces the threshold voltage (V_{th}). For biomedical application this is advantageous as this means that the voltage required to open the gates is reduced, and thus if designed correctly, reducing the overall power consumption of the device. A smaller threshold voltage can also increase the leakage current as the device will not turn ”off” as well, resulting in a larger sub-threshold conduction.

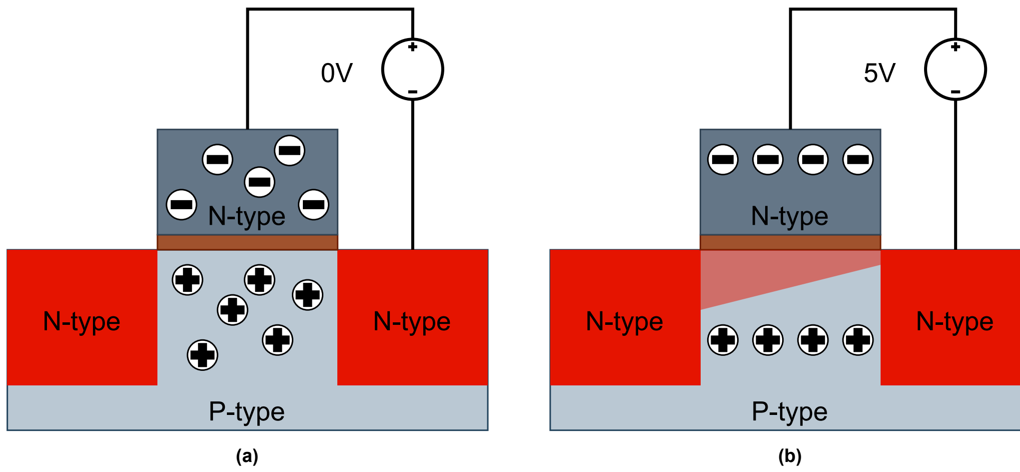


Figure 3.1: Polysilicon depletion effect in a NMOS transistor

There is another advantage of using polysilicon as the gate material. This is has to do with the fact that the gate definition can be done before the source and drain regions are defined. As there is a high temperature annealing step needed for the SN and SP regions, a metal gate has to be defined after the source and drain regions are defined, leaving it dependent on high-resolution lithography for sub-micron channels and possible misalignment as can be seen in figure 3.2. To resolve this misalignment, the gate is often placed on top of the source drain regions. However, this will cause a larger parasitic gate-source and gate-drain capacitance as can be seen in figure 3.3. The gate-source capacitance (C_{gs}) but more importantly the gate-drain capacitance (C_{gd}) reduces the switching speed of a transistor drastically, as can be seen in formula 3.1. As C_{gd} becomes larger, the time for V_{gs} to switch also becomes larger.

$$V_{gs} = R_g \cdot C_{gd} \cdot \frac{dv}{dt} \tag{3.1}$$

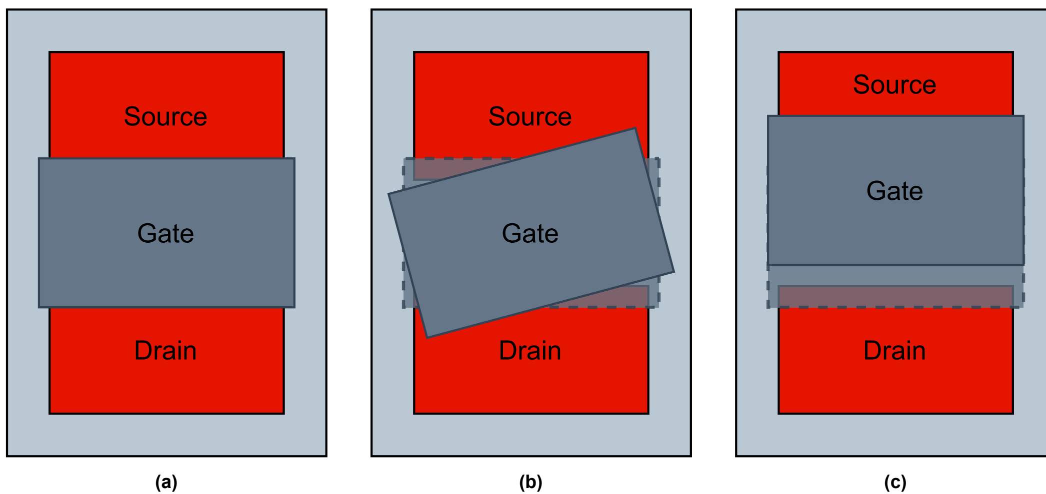


Figure 3.2: Possible missallignment of gate, with **a)** correct allignment, but overlay is needed, **b)** rotational missallignment and **c)** transitional missallignment

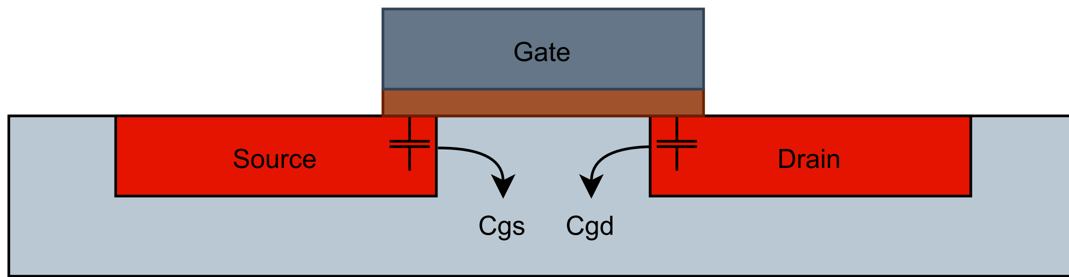


Figure 3.3: Parasitic gate capacitance when source and drain regions are defined before gate

But whilst for this technology polysilicon is used, the gate can be defined before the source and drain regions as can be found in figure 3.5d. This also has the advantage that the source and drain of the transistors can be self-aligned, reducing the parasitic gate capacitance's. Spacers next to the gate have also been added as a feature, this has to do with the combination of the self-aligned gate. The spacers will further help to reduce the parasitic capacitance as described before as can be seen in figure 3.4. This is because during the annealing of the source and drain regions, the dopant in these regions will also diffuse laterally.

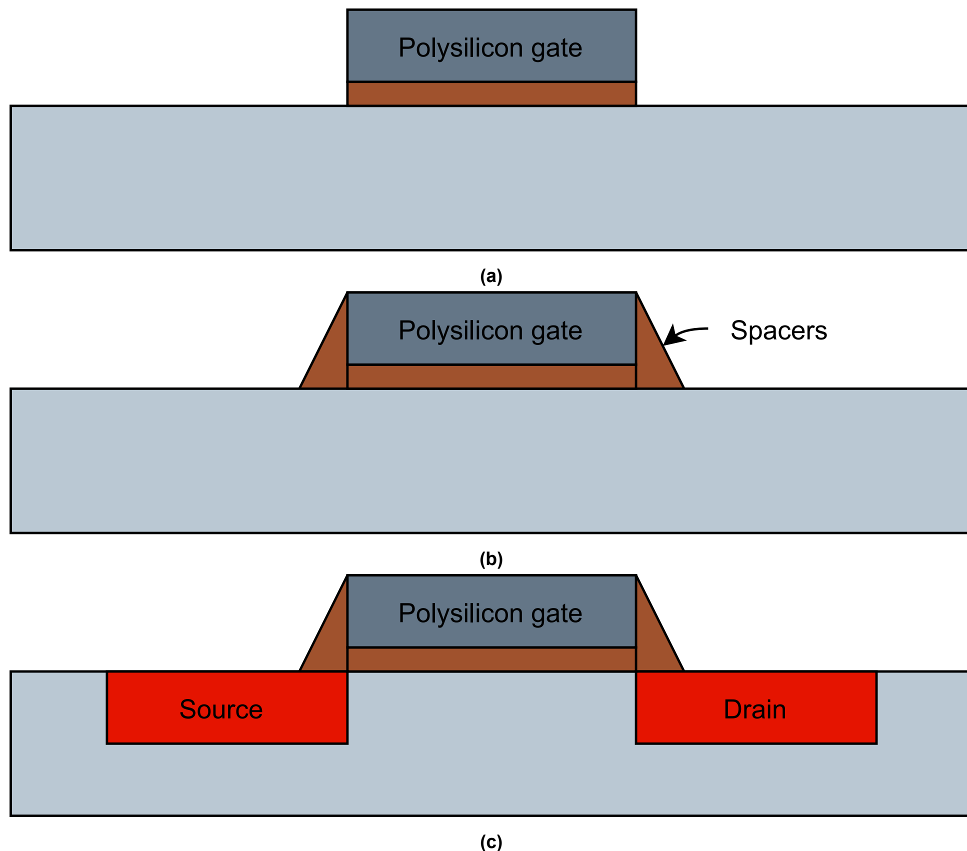


Figure 3.4: Moving polysilicon gate definition before source and drain region defintions, with **a)** gate definition, **b)** spacer definition and **c)** source and drain region definitions

A final reason for using polysilicon as the gate material is the operating voltage of the devices. Whilst the devices will be used in bio-applications, a lower operating voltage is desired, as this means lower power consumption. As the operating voltage of a MOSFET is limited by the threshold voltage, reduction of the threshold voltage is a common solution. The threshold voltage for an NMOS can be calculated via formula 3.2 and the threshold voltage for a PMOS can be calculated via formula 3.3.

$$V_{th} = \phi_M - \chi - \frac{E_g}{2q} + |\phi_B| + \frac{\sqrt{2K_s\epsilon_0 q N_B(2|\phi_B| + V_{BS})}}{C_{ox}} - \frac{Q_{tot}}{C_{ox}} \tag{3.2}$$

$$V_{th} = \phi_M - \chi - \frac{E_g}{2q} - |\phi_B| - \frac{\sqrt{2K_s\epsilon_0 q N_B(2|\phi_B| - V_{BS})}}{C_{ox}} - \frac{Q_{tot}}{C_{ox}} \tag{3.3}$$

$$|\phi_B| = \frac{kT}{q} \cdot ln(\frac{N_B}{n_i}) \tag{3.4}$$

The final layer before graphene can be grown, is the passivation layer as depicted in figure 3.5g. This layer is a dielectrical layer which insulates the active components from further components on top of this layer, in this work being the graphene electrodes. The passivation layer is made using TEOS based silicon dioxide (SiO_2).

The contact openings (CO) and the inter-connects (IC) are made after the graphene growth as depicted in figure 3.5h, to protect the active devices during the growth of graphene. In an usual process two or even three metallisations are the bare minimum, due to inevitability of crossing metal tracks. As the metallisation is done after graphene growth as the deposition and patterning of the metal layer can damage the graphene tracks, it is desired to keep the amount of metal layers to a minimum. In the GPOS technology, only one metal layer is required, as the underpasses of tracks can be done using polysilicon. A complete overview of the chosen features and how they come together can be found in figure 3.5.

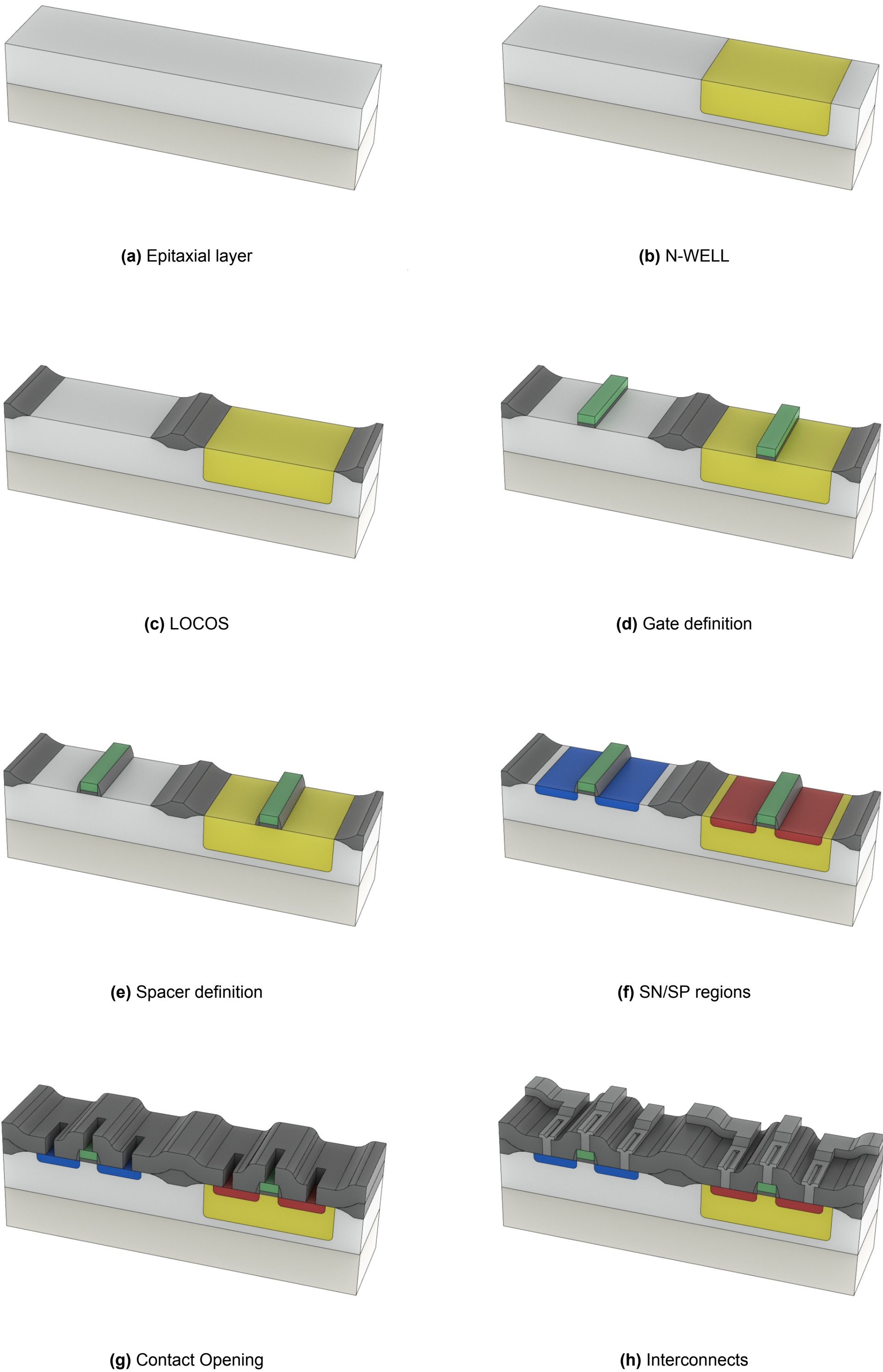


Figure 3.5: Process simulation steps

3.2. Process simulations using *TSUPREM-4*

Based on the general design, the process is then simulated. *TSUPREM-4* is an advanced TCAD software package that allows for its user to define and simulate their process in 2D. It is used to develop and optimise process technologies. *TSUPREM-4* runs the script sequentially, meaning line by line. As processes are also defined sequentially, working with *TSUPREM-4* is fairly straight forward, the complete scripts used to simulate the process can be found in appendix B

Process simulations have countless variables, it is therefore important to first define the process as global steps. The process is divided up in 7 major sections. Each section defines a major addition to the process, and consists of multiple smaller processing steps. It is important to note that in order to save on simulation time, only half the device is simulated and then mirrored around the centre of the gate.

The first step in simulating the process is to define the substrate. The standard at EKL is silicon with a 100 crystal orientation, p-type, boron doped wafers with a resistivity of 2 to 5 $\Omega \cdot cm$, this will therefore be the substrate as depicted in figure 3.6.

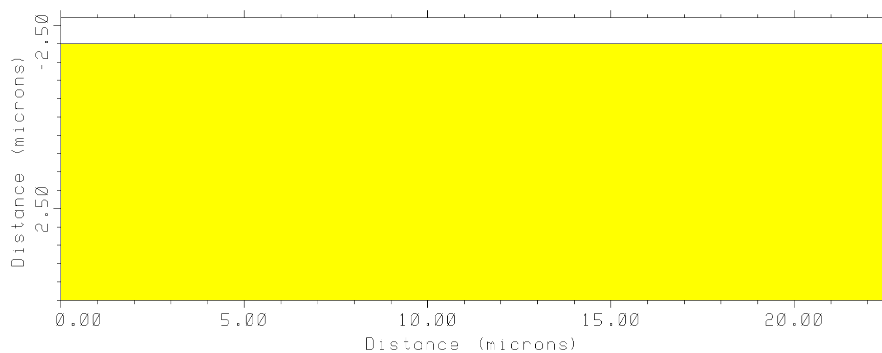


Figure 3.6: Definition of substrate in *TSUPREM4*

As been described, the first process step will be the growth of an epitaxial layer. The deposition time, temperature and impurity concentration can be adjusted. In this work the epitaxial layer is grown at a temperature of $1050\ °C$, with a thickness of $2\ \mu m$ and a boron impurity concentration of $1 \cdot 10^{16}\ atoms \cdot cm^{-3}$.

This step is followed by the implantation of the N-WELL regions, which defines the bulk for the PMOS transistors. Before implantation a $22\ nm$ silicon oxide dirt-barrier is grown, which collects any co-implanted particles. A $2.1\ \mu m$ layer of photoresist is deposited and patterned, followed by the phosphorous implantation. The implantation is done at an energy of $150\ keV$ and a dose of $5 \cdot 10^{12}\ atoms \cdot cm^{-3}$. To avoid unwanted channelling-effect that might occur during implantation, the wafer is rotated and tilted 22 ° and 7 °, respectively. The N-WELL is then annealed after the removal of the photoresist at a temperature of $1150\ °C$ for 480 minutes under the presence of nitrogen and oxygen. This results in a $2.5\ \mu m$ deep N-WELL as can be seen in figure 3.7.

The next step in the process is the definition of the LOCOS. The previous oxide layer is removed and a new SiO_2 seed layer of $22\ nm$ is formed using dry thermal oxidation. Which is then followed by the deposition of a $100\ nm\ SiN_x$ layer. The silicon nitride layer is then patterned using photoresist, and serves as a hard mask for the LOCOS definition. The LOCOS is then grown using wet thermal oxidation at a temperature of $1000\ °C$ for 200 minutes. As the oxygen can creep underneath the nitride layer, there is a formation of the so called bird-beak as can be seen in figure 3.8.

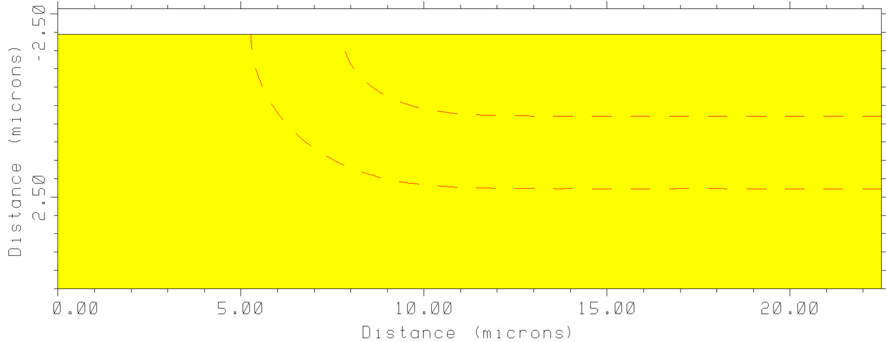


Figure 3.7: Definition of NWELL in *TSUPREM4*

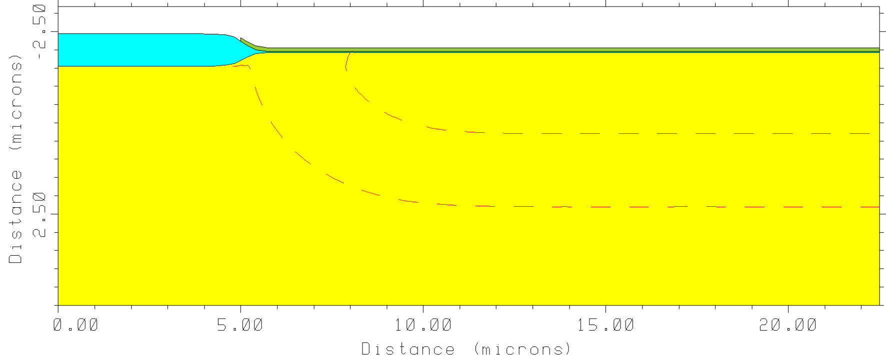


Figure 3.8: Definition of LOCOS in *TSUPREM4*

As the nitride layer is removed, the oxygen seed layer can now serve as the dirt-barrier for the implantation of the V_{th} adjust, which will be done over the entire wafer. The threshold adjustment implantation is done using boron at an energy of $25\ keV$ and a dose of $3 \cdot 10^{11} atoms \cdot cm^{-3}$, as depicted in figure 3.9.

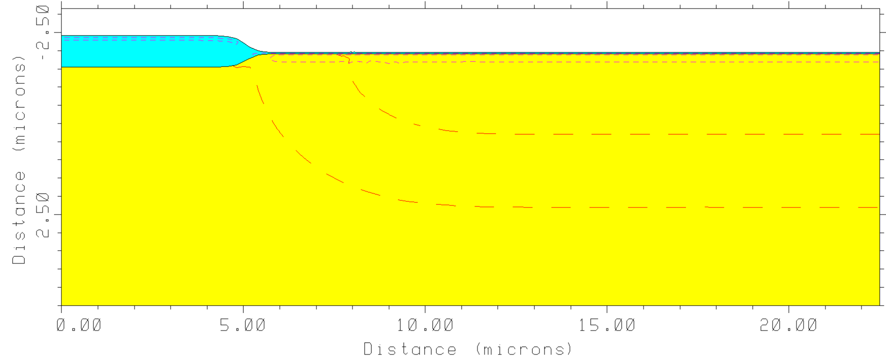


Figure 3.9: The threshold adjustment in *TSUPREM4*

The seed oxide layer is removed, which exposes the silicon. On which the gate oxide of $50\ nm$ is grown using dry thermal oxidation at $950\ °C$. On top a $500\ nm$ layer of polysilicon is deposited and implanted using phosphorous. The implantation is done at an energy of $100\ keV$ with a high dose of $3 \cdot 10^{15}\ atoms \cdot cm^{-3}$. Before annealing, a $300\ nm$ protective layer of SiN_x is deposited. Directly followed by the annealing required at a temperature of $950\ °C$ for 30 minutes. These process steps can be seen in figure 3.10.

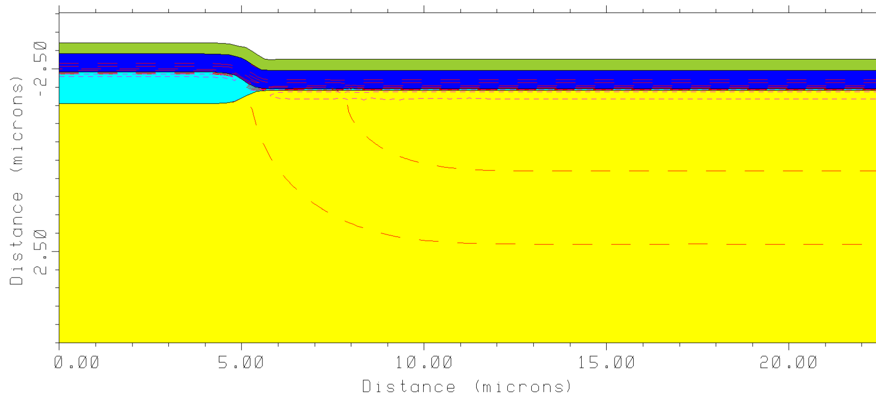


Figure 3.10: Polysilicon deposition in *TSUPREM4*

Using photoresist, the gate is defined. First the protective nitride is etched, followed by the polysilicon. The gate oxidation stays untouched, as this serves as the dirt-barrier during source and drain implantations. These steps can be seen in figure 3.11.

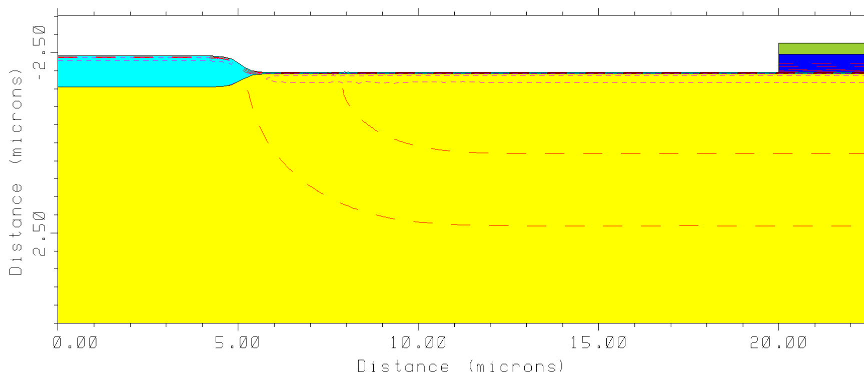


Figure 3.11: Definition of the gate in *TSUPREM4*

After this, $200\ nm$ of SiO_2 is deposited, which is then anisotropically dry etched, leaving two spacers next to the gate as can be seen in figure 3.12.

The next step is to deposit a layer of photoresist to define the shallow-n (SN) regions. Which are then implanted using arsenic at an energy of $40\ keV$ and a dose of $5 \cdot 10^{15}\ atoms \cdot cm^{-3}$. Removing the photoresist and reapplying another layer of photoresist which is then patterned to define the shallow-p (SP) regions. Which are then implanted using boron at an energy of $25\ keV$ and a dose of $6 \cdot 10^{15}\ atoms \cdot cm^{-3}$. Both these regions are then annealed at a temperature of $950\ °C$ for 35 minutes. Which is then followed by the removal of the remaining protective SiN_x layer and the remaining SiO_2 on top of the silicon as can be seen in figure 3.13.

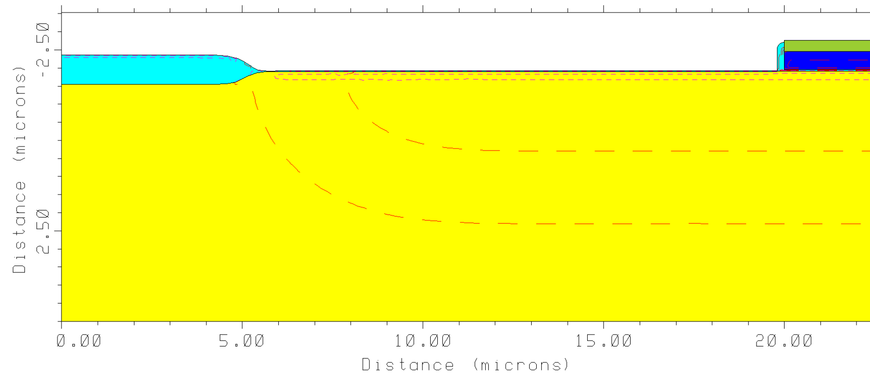


Figure 3.12: Definitino of the spacers in *TSUPREM4*

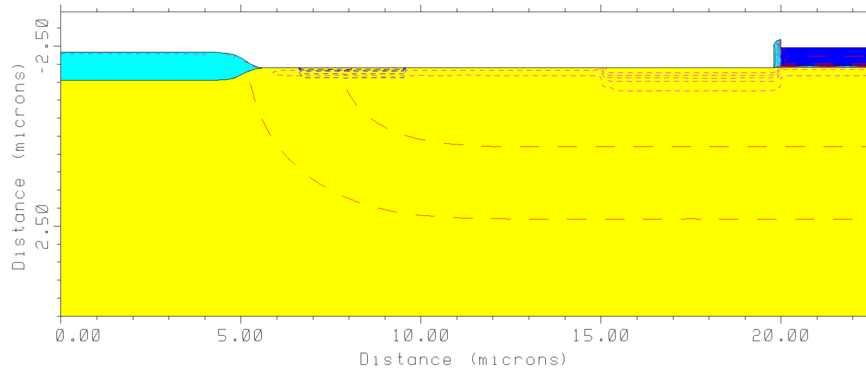


Figure 3.13: Definition of the SN and SP regions in *TSUPREM4* for the PMOS device. The SP located near the gate and the SN near the LOCOS.

The devices are then passivated using a $1\mu m$ SiO_2 layer, after which the graphene growth is modelled as a diffusion step. Lastly, the contact openings (COs) are made using patterned photoresist, which are then filled with a $1.25\mu m$ layer of aluminium. Which is also patterned using photoresist to form the interconnects (ICs). The structures are then mirrored leading to the final devices as can be seen in figure 3.14 and 3.15.

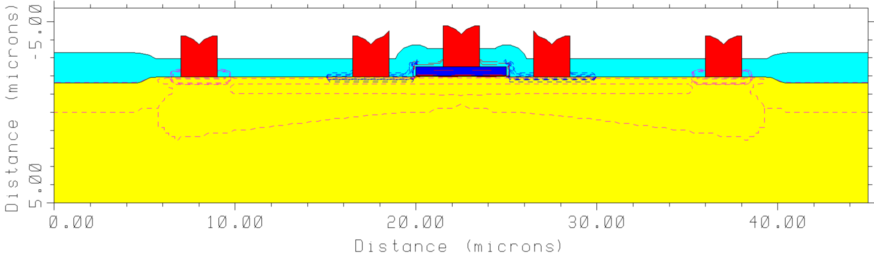


Figure 3.14: Process simulation of NMOS device

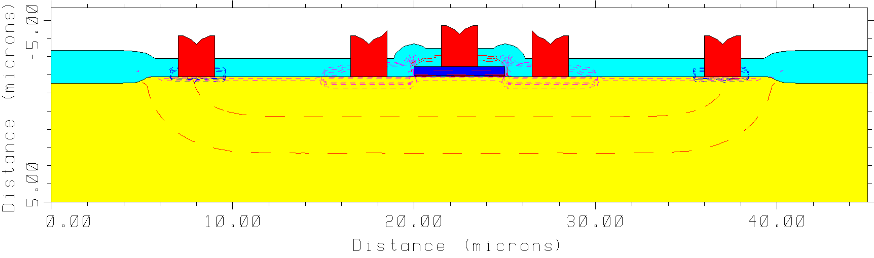


Figure 3.15: Process simulation of PMOS device

3.3. Device simulation using *MEDICI*

Now that the active device structures have been defined, the structure can be transferred to a device simulator. For this purpose, *MEDICI* is used. *MEDICI* is a 2D device simulator that is capable to simulate electrical characteristics of semiconductor devices. *MEDICI* uses the simulated process file from *TSUPREM-4* to simulate and model electrical characteristics of created semiconductor devices. This can be done by first defining the different contacts that exist in the device. *MEDICI* also needs to know which models it needs to use for the simulations. Once this is defined electrical input can be defined, allowing *MEDICI* to calculate the electrical output of the device. The devices as used in *MEDICI* can be seen in figure 3.16 and figure 3.17.

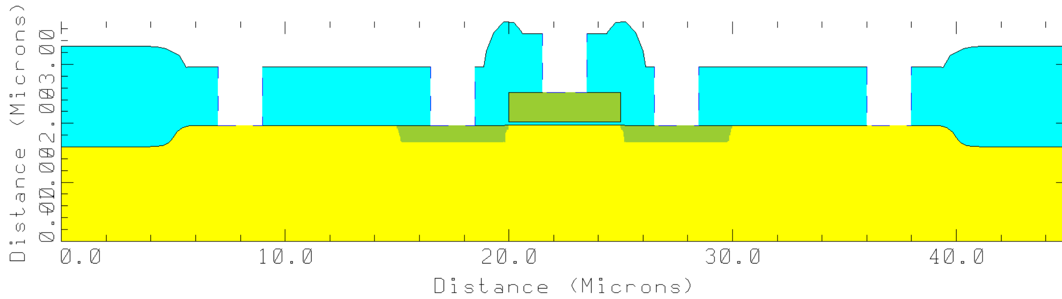


Figure 3.16: Device simulation of NMOS device

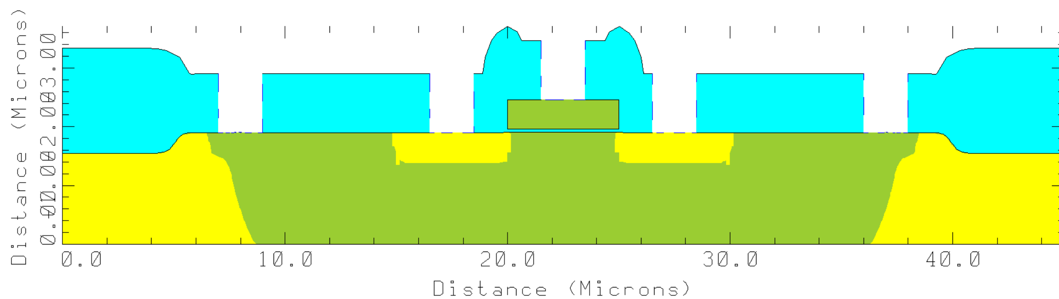


Figure 3.17: Device simulation of PMOS device

In *MEDICI* the used models during simulation are of the utmost importance. It not only determines the electrical characteristics of the atoms, it also defines the physical model used for the simulation. As there are many different models to define physical characteristics of atoms and its electrical behaviour. A summary of the used models are given in table 3.1.

Model name	**Short explanation of model**
CONSRH	Shockley-Read-Hall recombination is used with concentration dependent lifetime.
AUGER	Auger recombination is used.
BGN	Band-Gap-Narrowing is used.
FLDMOB	Mobility model using parallel electrical field components.
CONMOB	Mobility tables are used to model the dependence of carrier mobility on impurity concentration.
SRFMOB2	Specifies that an enhanced surface mobility model is used along semiconductor surfaces which accounts for phonon scattering, surface roughness scattering and charged impurity scattering.

Table 3.1: Summary of models used during device simulations

3.3.1. Mesh size and selection

For any CAD based simulation, meshing of the structures is an important step. Determining the mesh size on certain locations doesn't only improve accuracy, it also determines if the simulations will converge. The mesh size can be determined based on the impurity profiles and materials. As there is a change in impurity levels, there is a finer mesh needed to solve this region. Also if there is a change in material, there is need for a finer mesh size. Using these two criteria, the mesh can be made automatically, giving the meshes as can be seen in figure 3.18.

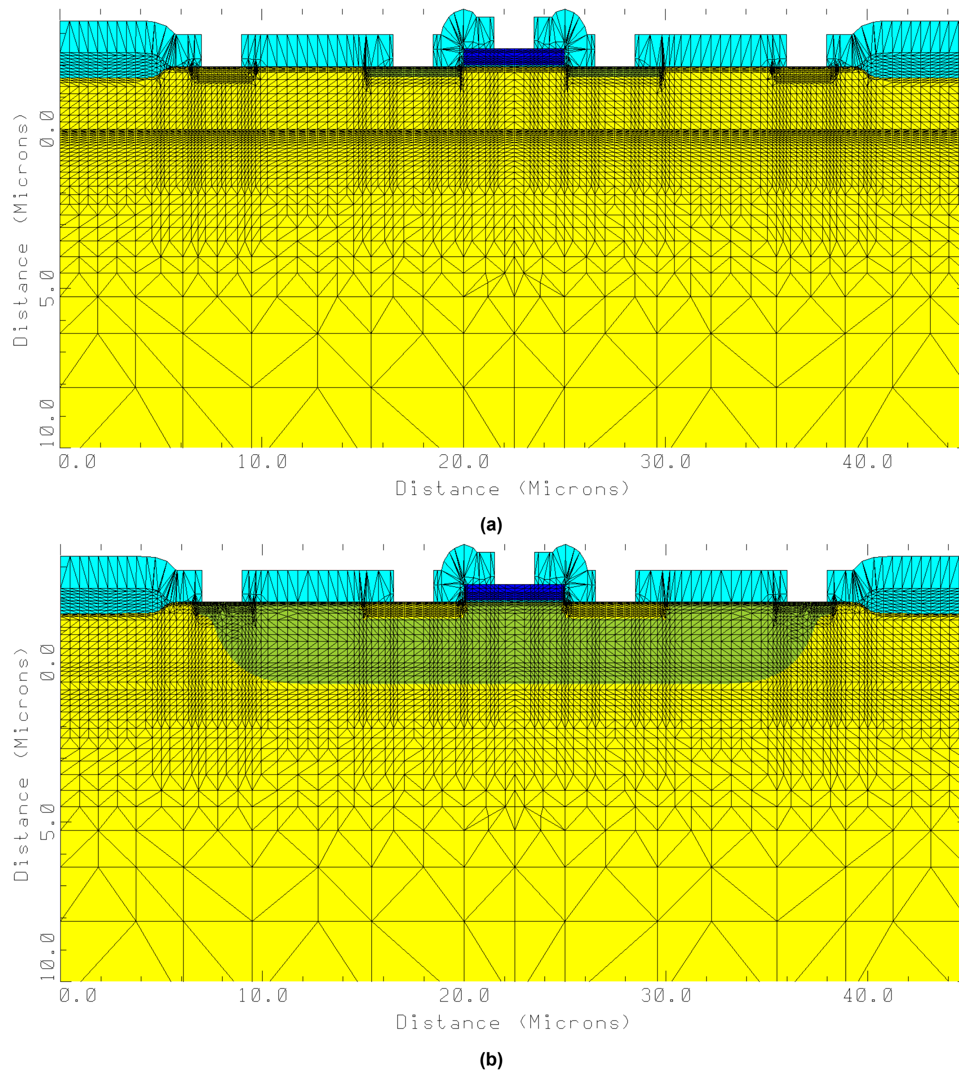


Figure 3.18: Used mesh during device simulation of **a)** the NMOS device and **b)** the PMOS device

3.3.2. Impurity profile extraction

The first device simulation is the extraction of the impurity profile along the different regions of the devices. These simulations and extracted plots allow for adjustment of the doping concentration and implantation energy. Using this information, it is also possible to calculate the sheet resistance of the materials, which allow to check if the doped materials were conductive enough.

The first plot would be that of the gate impurity profile of the NMOS and PMOS devices as can be found in figure 3.19. As can be seen, the polysilicon gate is highly doped. Also, the effect of the V_{th} adjust can be seen, as it is a boron doping, the NMOS devices have a lower surface doping after the gate. Whereas the PMOS devices have a slightly higher doping directly after the gate.

Also impurity profiles of the source and drain regions can be plotted and adjusted accordingly. As can be seen in figure 3.20, the source and drain regions of the NMOS devices is shallower than those of the PMOS devices. This is can be adjusted by changing the dose and implantation energy. Lastly, the impurity profiles of the bulk contact are also extracted and plotted, as depicted in figure 3.21.

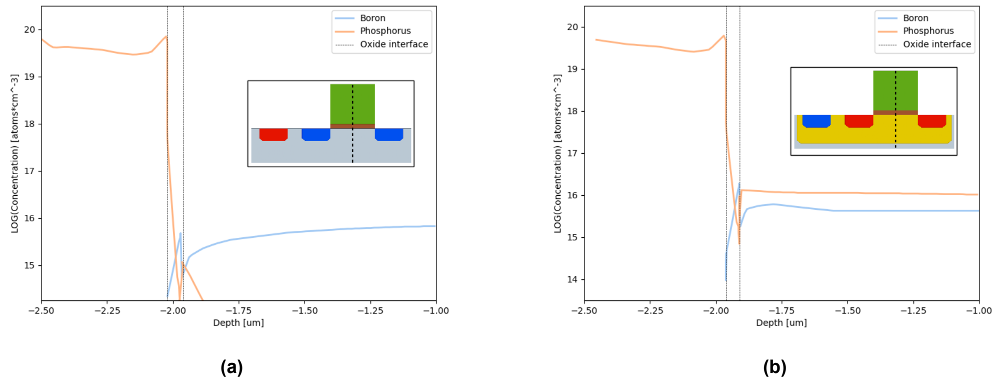


Figure 3.19: Impurity plotted through the depth along the gate for **a)** the NMOS device and **b)** the PMOS device

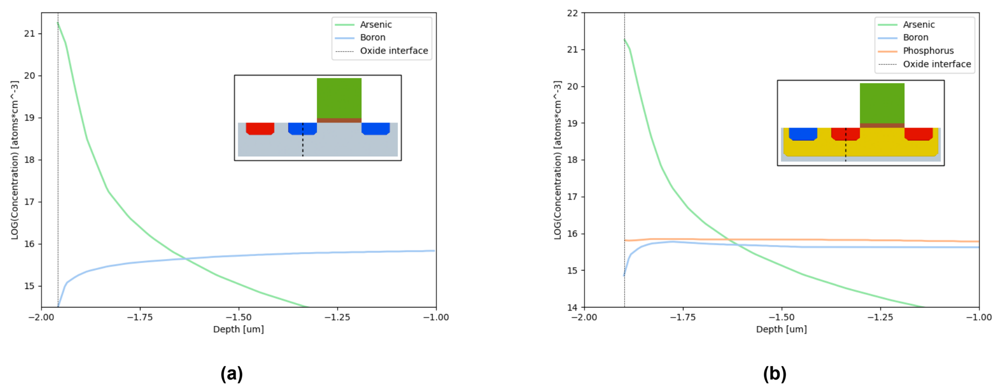


Figure 3.20: Impurity plotted through the depth along the source/drain for **a)** the NMOS device and **b)** the PMOS device

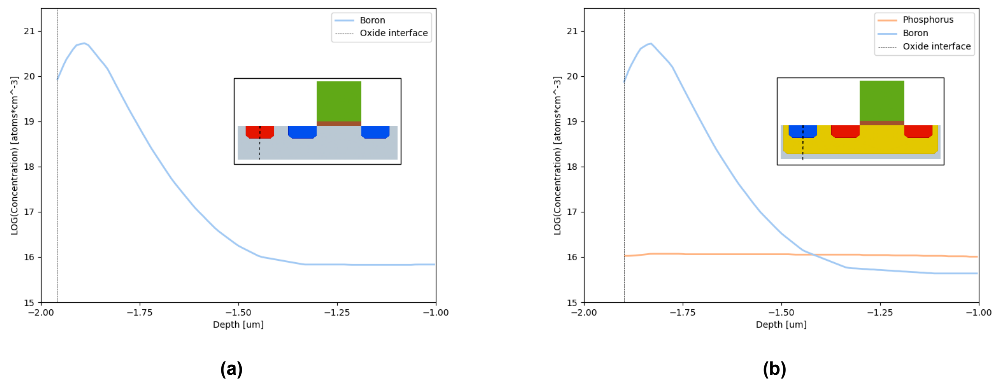


Figure 3.21: Impurity plotted through the depth along the bulk contact for **a)** the NMOS device and **b)** the PMOS device

3.3.3. Electrical characteristics extraction

Not only the impurity profiles are of importance, also the electrical characteristics of the devices can be plotted. In figure 3.22 the drain current is plotted as the gate voltage is ramped.

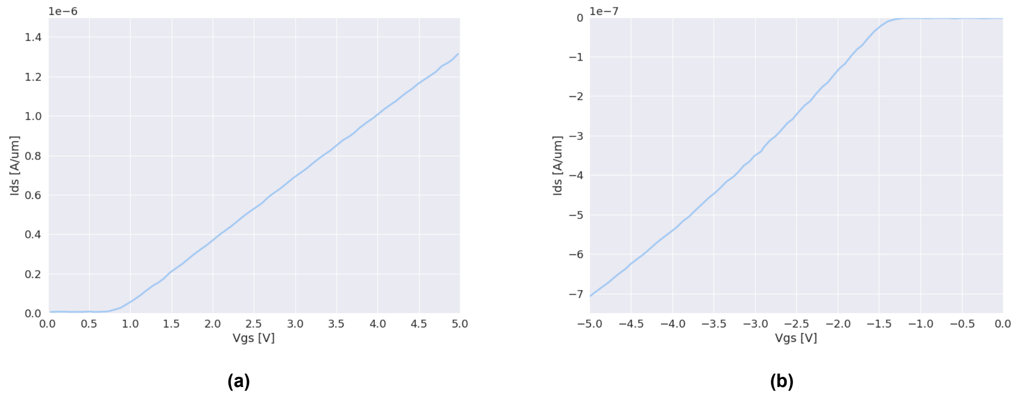


Figure 3.22: Drain current (I_d) versus gate voltage (V_g) for **a)** the NMOS device and **b)** the PMOS device

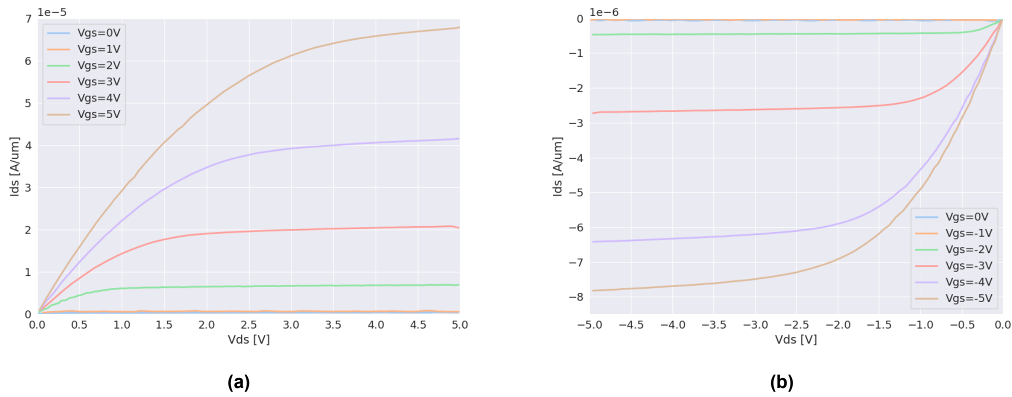


Figure 3.23: Drain current (I_d) versus drain voltage (V_d) with varying gate voltage (V_g) for **a)** the NMOS device and **b)** the PMOS device

3.4. Test structures for characterisation of GPOS

The simulations only provide a glance in the electrical characteristics that define the active devices. There is also a need to design devices and structures that allow the complete characterisation of the newly developed technology. The testing of these structures can be performed using the 4-point probe station.The main boundary condition regarding the use of this machine is that the pads of the device should be large enough and spaced adequately apart from each other enough. Therefore, the contact pads in this work have been designed to be 80 μm by 80 μm and have a pitch of 160 μm.

There are several test structures that exist, which can aid in setting up an electrical model for the NMOS and PMOS devices. The simplest option is to have multiple NMOS and PMOS devices that can directly be characterized. As the gate length and width can be adjusted to change device characteristics, there are several NMOS and PMOS devices with varying gate lengths and widths. This variation is so that the technology can be characterised over a broader range of devices. An overview of these devices is given in table 3.2.

Also several van der Pauw test structures are designed to measure the sheet resistance of several important layers, an overview of each layer with a van der Pauw structure can be found in figure 3.24 The structure has 4 contact points, 2 for voltage connections and 2 for current connections.

For resistivity measurements, a current is applied along on edge of the structure and the voltage is measure along the other edge. Using Ohm's law (formula 3.5) the resistance of the layer along a edge can be calculated taking in account the van der Pauw constant of $\frac{\pi}{ln(2)}$.

NMOS and PMOS	
Gate width $[\mu m]$	Gate length $[\mu m]$
20	10
20	5
20	2
20	1
20	0.5
50	10
50	5
50	2
50	1
50	0.5

Table 3.2: Overview of the different sized NMOS and PMOS devices

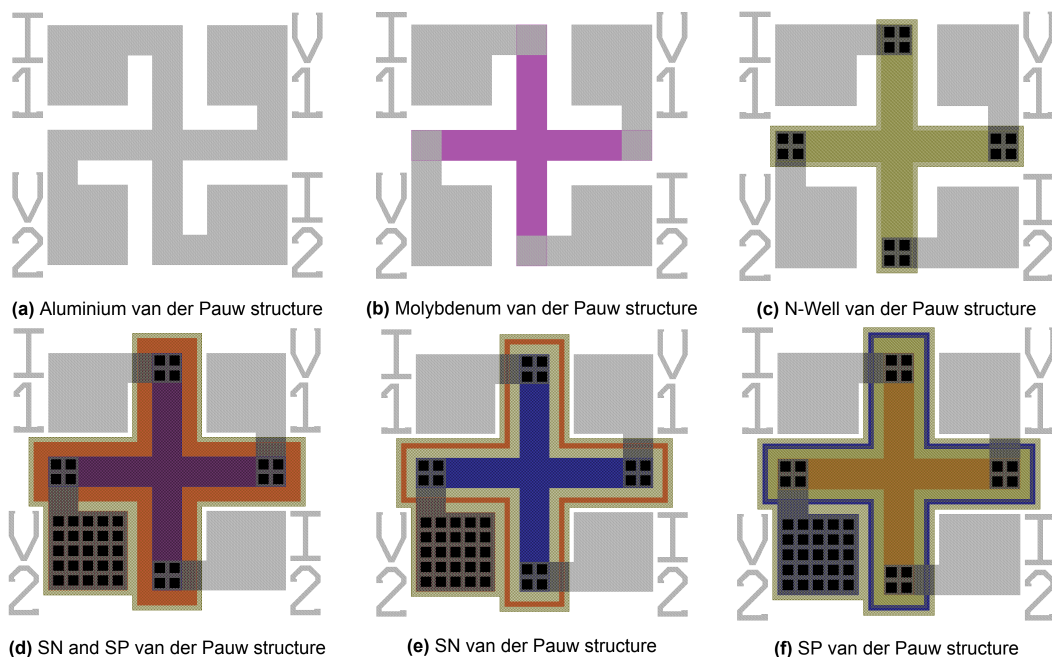
$$R_{vertical,horizontal} = \frac{V_{12}}{I_{12}} \cdot \frac{\pi}{ln(2)} \tag{3.5}$$

Using the sheet resistance, the sheet density (n_S) can be calculated using formula 3.6. Where q is the unit charge, and μ_m is the majority carrier concentration.

$$n_s = \frac{1}{R_s \cdot q \cdot \mu_m} \tag{3.6}$$

Using the sheet resistance and the calculated sheet density, the majority carrier mobility can be calculated using formula 3.7.

$$\mu_m = \frac{1}{q \cdot n_s \cdot R_s} \tag{3.7}$$

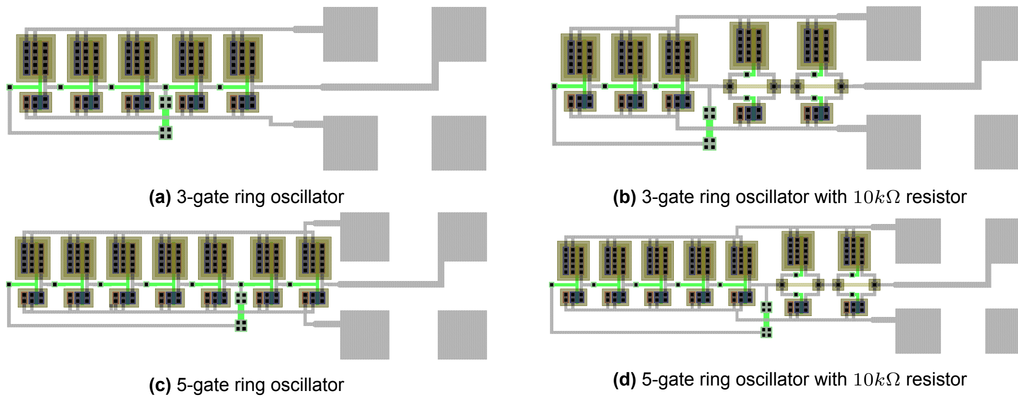


(a) Aluminium van der Pauw structure **(b)** Molybdenum van der Pauw structure **(c)** N-Well van der Pauw structure

(d) SN and SP van der Pauw structure **(e)** SN van der Pauw structure **(f)** SP van der Pauw structure

Figure 3.24: Van der Pauw test structures

The test structures also include 4 types of ring oscillators. There are 2 ring oscillators with 3 stages, of which one oscillator has a $10k\Omega$ resistor. The two other oscillators are compromised of 5 stages, also one of these oscillators has a $10k\Omega$ resistor at the output. These oscillators can be seen in figure 3.25. These oscillators can be used to determine quantities such as frequency, leakage and active current.



(a) 3-gate ring oscillator

(b) 3-gate ring oscillator with $10k\Omega$ resistor

(c) 5-gate ring oscillator

(d) 5-gate ring oscillator with $10k\Omega$ resistor

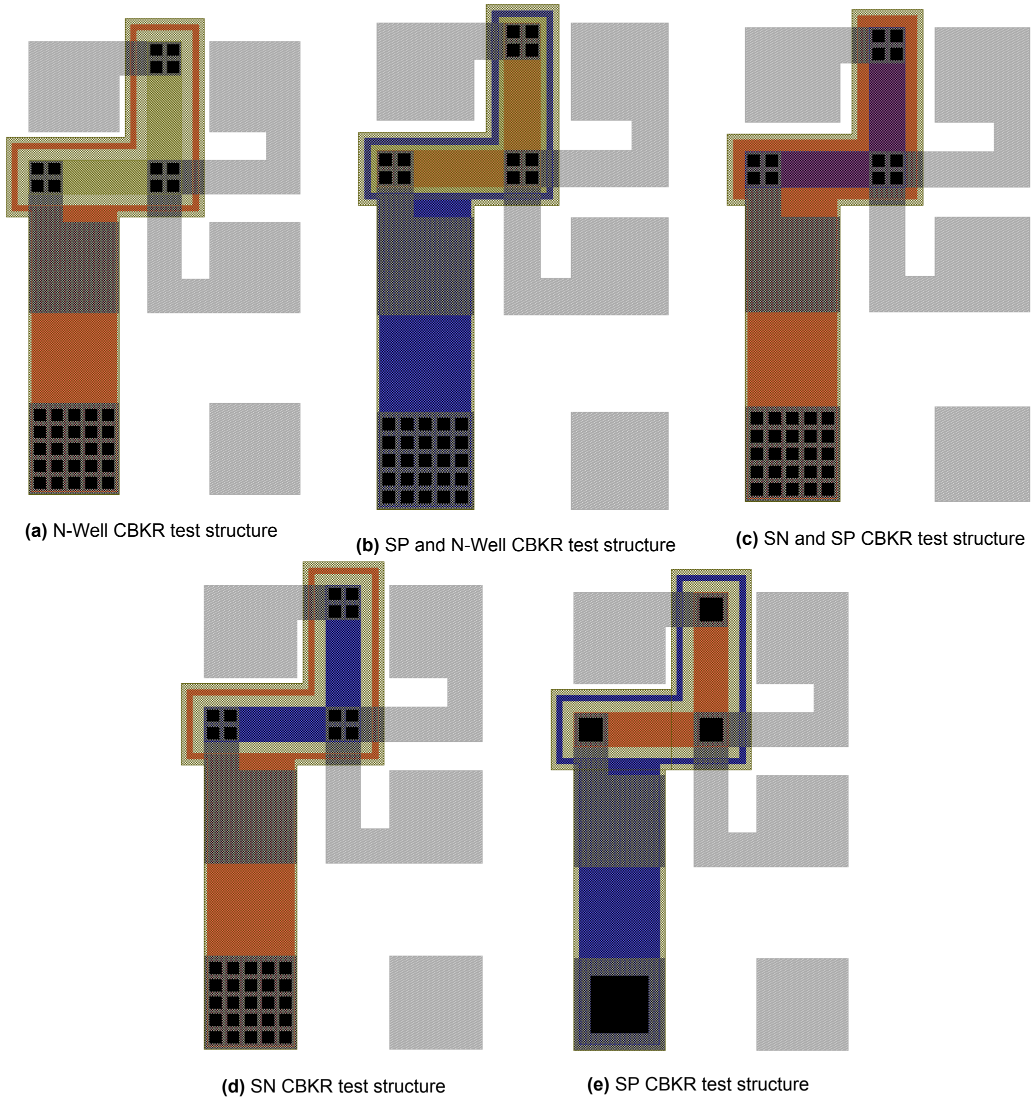
Figure 3.25: Ring oscillator test structures

Another set of test structures are Cross-Bridge Kelvin Resistors (CBKR). These structures are used determining the contact resistance between a specific layer and the metal interface. It allows also for the characterization of the contact interface. The structures used are depicted in figure 3.26.

The next set of test structures are Electric Line Measurements (ELM). These measurements allow for the characterisation of the different linewidths. Which would allow for electrical characterisation of the process layers. As can be seen in figure 3.27, for each layer of interest there are 3 separate line widths used. These measurements give a voltage drop and a certain current accross a fixed length of the layer. Using the measured sheet resistances from the van der Pauw structures, it is possible to then calculate the width of these lines using formula 3.8. Where $R_{\square}$ is the sheet resistance measured from de van der Pauw structures, V_{diff} is the voltage drop accross the length of the wire (L_w) and I_m the measured current through the wire.

$$w_m = \frac{R_{\square} \cdot L_w}{V_{diff}/I_m} \tag{3.8}$$

The last test structure is to see if the contact opening are fully opened to the required regions as shown in figure 3.28. This structure is simply a large area of the layer that requires contacting, and a large area that represents the contact opening. This measurement can be done visually after the contact openings have been made.



(a) N-Well CBKR test structure

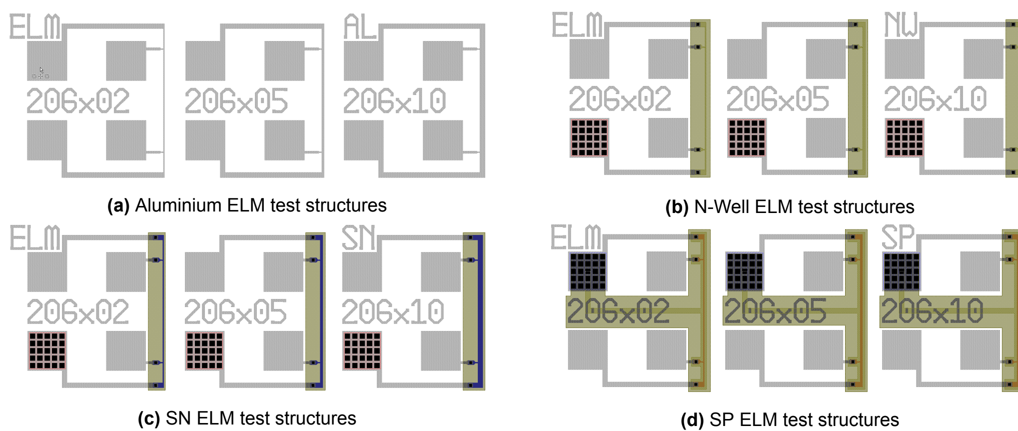
(b) SP and N-Well CBKR test structure

(c) SN and SP CBKR test structure

(d) SN CBKR test structure

(e) SP CBKR test structure

Figure 3.26: Cross-Bridge Kelvin Resistor (CBKR) test structures



(a) Aluminium ELM test structures

(b) N-Well ELM test structures

(c) SN ELM test structures

(d) SP ELM test structures

Figure 3.27: Electrical Line Measurement (ELM) test structures

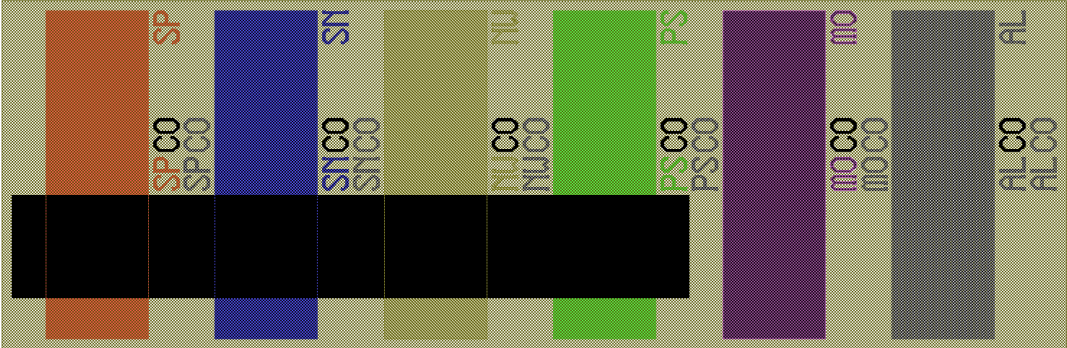
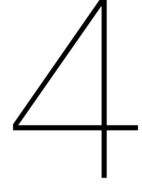


Figure 3.28: Contact opening test structure



Layout and Process flow

4.1. Development of digital circuitry

4.1.1. LTSPICE simulations

Now that the process is fully defined the next step is to define the electronics on the chip. This requires for the electrical circuits and its components need to be designed and simulated. The electrical parameters extracted from MEDICI can now be used within a SPICE model. To create a fully defined spice model, it is needed to first create the actual devices and extract all the parameters from here. But as GPOS technology is closely related to the *BICMOS5* technology, the SPICE parameters of the *BICMOS5* are used and adjusted with the extracted parameters from *MEDICI* using *MOS.PARA*. The extracted parameters can be found in table 4.1.

	S_{lin} $[\frac{A}{\mu m \cdot V}]$	V_{th} $[V]$	$V_{th,sat}$ $[V]$	S_{sub} $[\frac{mV}{dec}]$
NMOS	$3.226 \cdot 10^{-7}$	0.8548	0.6689	82.63
PMOS	$2.397 \cdot 10^{-7}$	-1.373	-1.203	98.57

Table 4.1: Extracted MOS parameters from *MEDICI*

From *MEDICI* it is also possible to already extract other *BSIM3V3* parameters that have an influence on the device characteristics. An overview of the adjusted parameters can be found in table 4.2. X_j is the junction depth which can be extracted from the impurity profiles. t_{ox} is the gate oxide thickness, which is extracted from *TSUPREM4* using the *THICKNESS* command. V_{th0} is the threshold voltage of a long channel device at $V_{bs} = 0V$ and a small V_{ds} and is extracted using *MOS.PARA*. N_{GATE} is the polysilicon gate doping concentration and can be extracted using the impurity profiles. N_{SUB} is the substrate doping concentration and can also be extracted from the impurity profiles. N_{CH} is the peak doping near the interface, this parameter is also extracted from the impurity profiles.

Besides these parameters, also K_1 and K_2 are adjusted, which are the first-order, second-order body effect coefficients respectively. K_1 can be calculated using formula 4.1 and K_2 from formula 4.2. The variables needed to calculate these are determined from the impurity plots and electrical simulations. Where, γ_1 is given by formula 4.3, γ_2 is by formula 4.4 and ϕ_s by formula 4.5. Within these equations, n_i is given by formula 4.6, $E_g(T)$ by formula 4.7 and V_T by formula 4.8. These equations are from the *BSIM3v3* model.

Looking at the lateral diffusion of the source and drain regions, the reduction or increase in gate length or width can be calculated. Which translates to the W_{int} and L_{int} parameters in the *BSIM3v3* model.

$$k_1 = \gamma_2 + 2 \cdot k_2 \cdot \sqrt{\phi_s - V_{BS}} \tag{4.1}$$

$$k_2 = \frac{(\gamma_2 - \gamma_1) \cdot (\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s})}{2 \cdot \phi_s \cdot (\sqrt{\phi_s - V_{BM}} - \sqrt{\phi_s}) + V_{BM}} \quad (4.2)$$

$$\gamma_1 = \frac{\sqrt{2 \cdot q \cdot N_{ch} \cdot \epsilon_{Si}}}{C_{ox}} \quad (4.3)$$

$$\gamma_2 = \frac{\sqrt{2 \cdot q \cdot N_{sub} \cdot \epsilon_{Si}}}{C_{ox}} \quad (4.4)$$

$$\phi_s = 2 \cdot V_T \cdot ln(\frac{N_{ch}}{n_i}) \quad (4.5)$$

$$n_i = 1.45 \cdot 10^{10} \cdot (\frac{T}{300.15})^{15} \cdot \text{exp}(21.5565981 - \frac{q \cdot E_g(T)}{2 \cdot k_B \cdot T}) \quad (4.6)$$

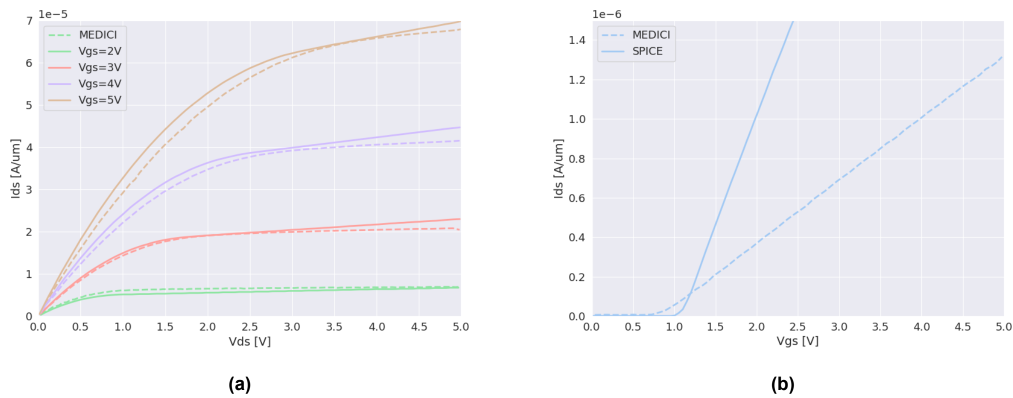
$$E_g(T) = 1.16 - \frac{7.02 \cdot 10^{-4} \cdot T^2}{T + 1108} \quad (4.7)$$

$$V_T = \frac{k \cdot T}{q} \quad (4.8)$$

BSIM3v3 parameter	New value for NMOS	New value for PMOS
X_j $[nm]$	335.71	480.16
V_{th0} $[V]$	0.855	-1.373
t_{ox} $[nm]$	50.0	50.0
N_{GATE} $[\frac{atoms}{cm^3}]$	$4 \cdot 10^{19}$	$4 \cdot 10^{19}$
N_{SUB} $[\frac{atoms}{cm^3}]$	$1 \cdot 10^{16}$	$1 \cdot 10^{16}$
N_{CH} $[\frac{atoms}{cm^3}]$	$1 \cdot 10^{15}$	$1 \cdot 10^{16}$
K_1 $[\sqrt{V}]$	0.8342	0.8342
K_2 [-]	-0.0186	0.0186
W_{int} $[\mu m]$	-0.01420878	-0.9993817
L_{int} $[nm]$	0	0

Table 4.2: Adjusted parameters in *BSIM3v3* model

Inserting these parameters in the existing *BICMOS5* model, the electrical behaviour of the transistors can be modeled in LTSpice. As a comparison with the the electrical simulations done in *MEDICI*, the $I_d - V_g$ curve and the $I_d - V_d$ curves are simulated. The resulting plots can be found in figures 4.1 and 4.2.



(a) **(b)**

Figure 4.1: Drain current (I_d) versus gate voltage (V_g) for **a)** the NMOS device and **b)** the PMOS device

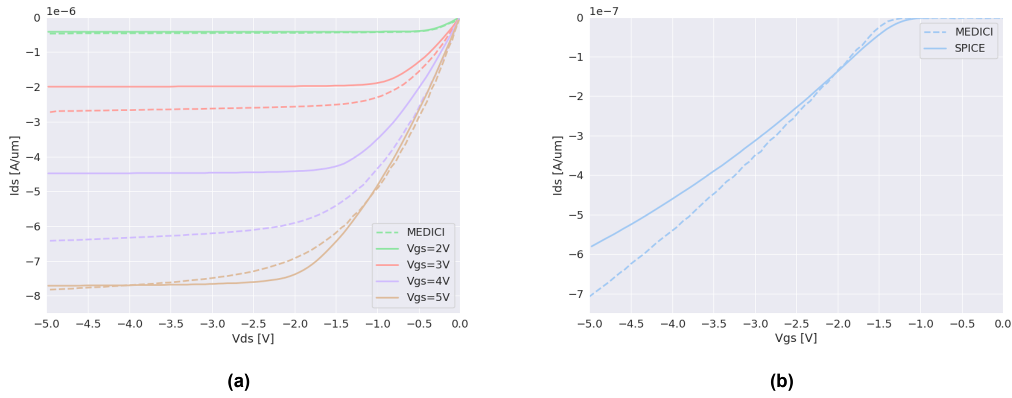


Figure 4.2: Drain current (I_d) versus drain voltage (V_d) with varying gate voltage (V_g) for **a)** the NMOS device and **b)** the PMOS device

The gate oxide capacitance can also be calculated using formula 4.9, where ϵ_0 is the vacuum permittivity in $\frac{F}{\mu m}$, ϵ_r is the relative permittivity of SiO_2 and t_{ox} is the oxide thickness in μm.

$$C_{ox} = \epsilon_0 \cdot \frac{\epsilon_r}{t_{ox}} = 6.91 \cdot 10^{-16} \frac{F}{\mu m^2} \tag{4.9}$$

Before the circuitry can be designed, the sizing of the transistors needs to be determined. As the transistors will be used in digital circuitry, the propagation delay difference between the pull-up and the pull-down network should be kept at a minimum. This means for the devices, that their on-resistance (R_{on}), should be equal. This is the resistance that can be found by using the first derivation of the linear region of the transistor. An overview of the found resistances at different gate-source voltages for the NMOS and PMOS devices can be found in table 4.3. Also the ratio between the size of the NMOS and PMOS transistor are given. Important to note is that the widths of the transistors are optimised for the NOT gate, as this is the simplest type of gate.

V_{gs} [V]	$R_{on,\textbf{nmos}}$ [$\frac{\Omega}{m}$]	$R_{on,\textbf{pmos}}$ [$\frac{\Omega}{m}$]	$W_{\textbf{nmos}}$:$W_{\textbf{pmos}}$
3	0.067	0.313	1:4.67
4	0.041	0.191	1:4.66
5	0.031	0.169	1:5.45

Table 4.3: Transistor width ratio for varying V_{gs}

The width of the NMOS is set to be $20\ \mu m$, meaning that the width of the PMOS will need to be $100\ \mu m$ for a NOT gate. The width of the PMOS has actually been set to $50\ \mu m$, as it is yet untested technology.

4.1.2. Design of digital circuitry

The models of the transistors can now be used in designing the digital circuitry. The desired functionality of the electronics is to demonstrate the use of digital logic in combination with the graphene MEAs. Keeping this simplicity in mind, it is chosen to create an array selector which opens and closes in-line transmission gates. The transistor level design of the transmission gates used is depicted in figure 4.3. The full digital logic of the array selector can be found in figure 4.4.

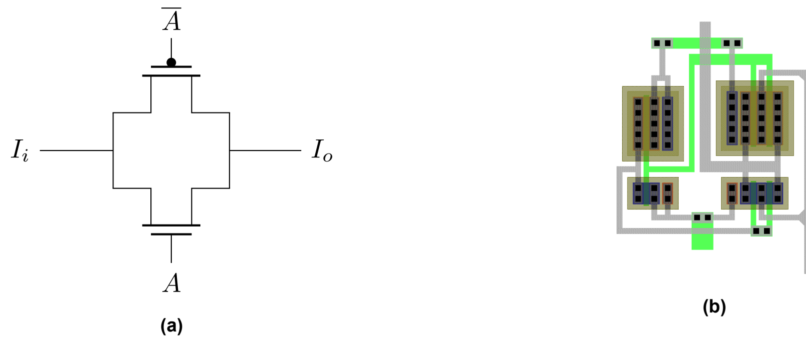


Figure 4.3: Transmission gate and included NOT gate with **a)** circuit representation and **b)** layout design

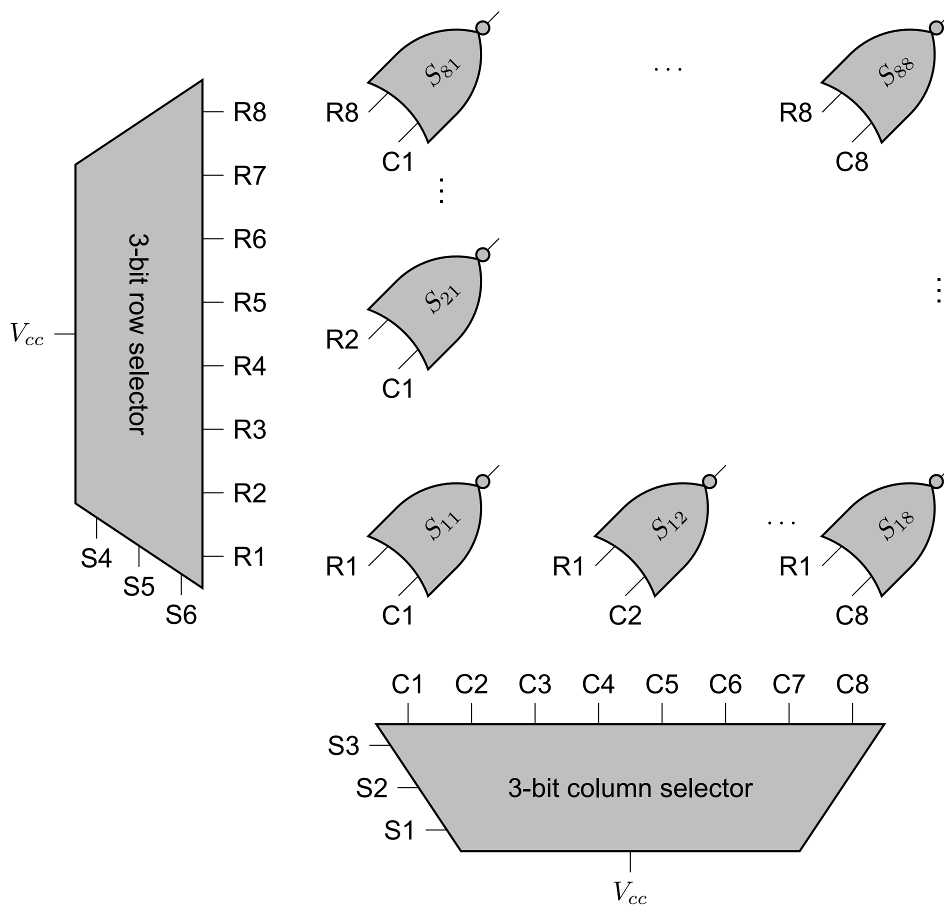


Figure 4.4: 6-bit array selector

For this selector there are several basic logical gates needed as shown. Firstly, there are two seperate 3-bit selectors needed, the circuit logic for this can be found in figure 4.5. There are therefore only 3 basic logic gates needed for the entire array selector, a NOT-gate, a 2-input NOR-gate and a 3-input NAND gate. The transistor level design of these gates are depicted in figure 4.6, 4.7 and 4.8.

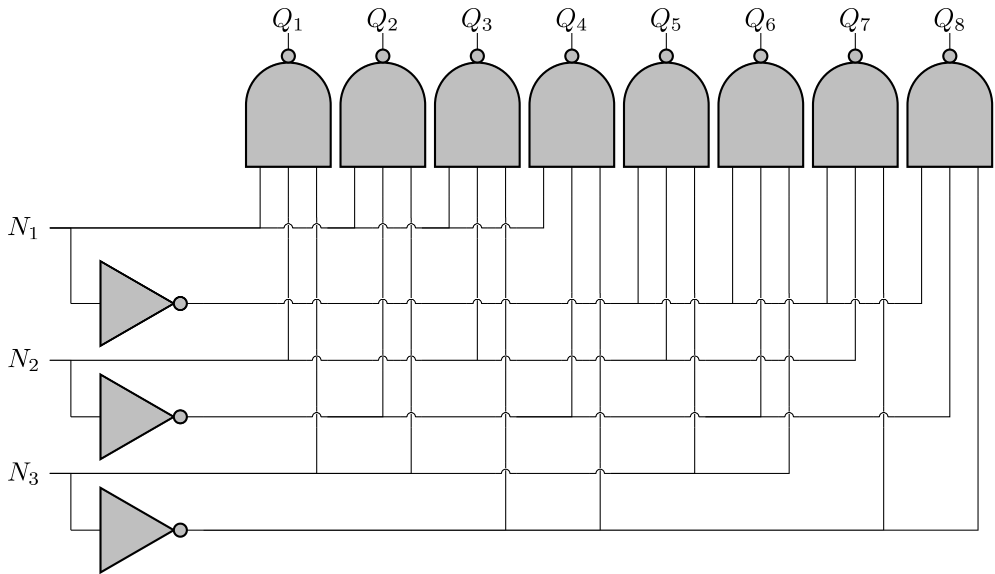


Figure 4.5: 3-bit selector

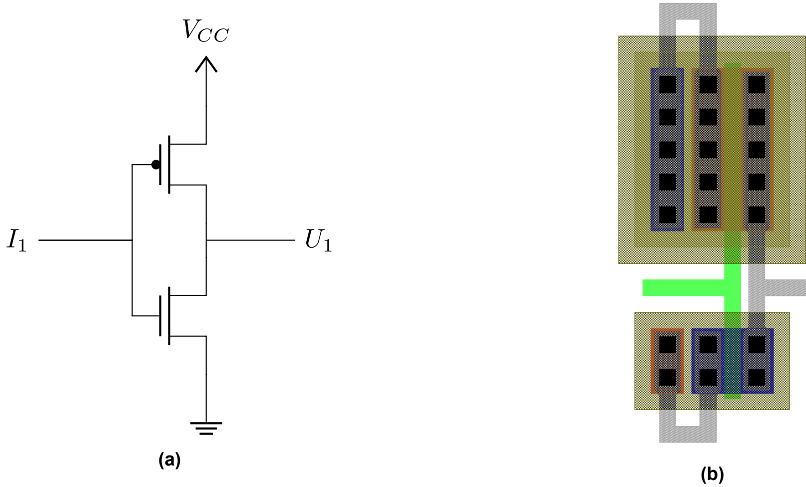


Figure 4.6: Transistor level of NOT gate with **a)** circuit representation and **b)** layout design

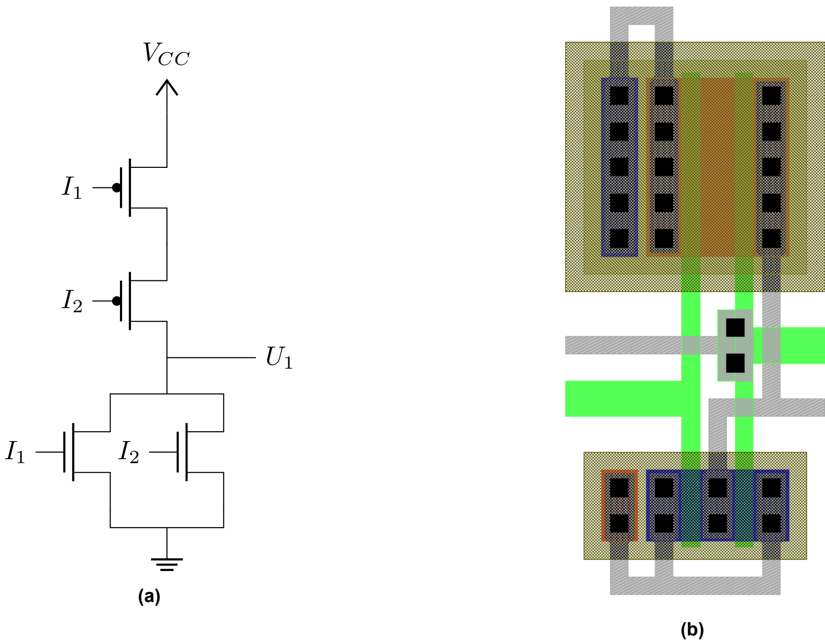


Figure 4.7: Transistor level of 2-input NOR gate with **a)** circuit represantation and **b)** layout design

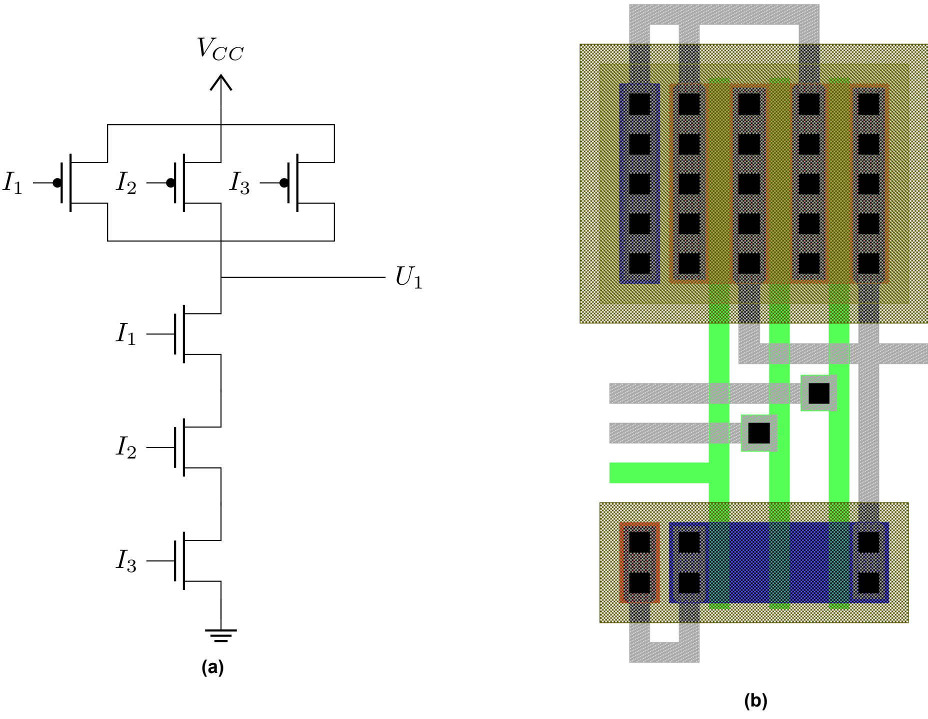


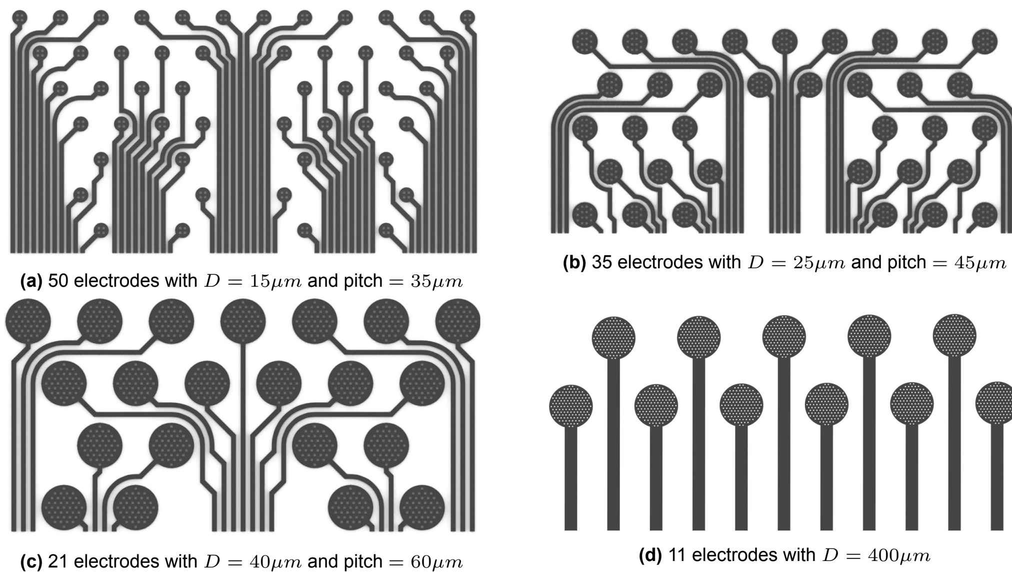
Figure 4.8: Transistor level design of 3-input NAND gate with **a)** circuit representation and **b)** layout design

4.2. Development of MEAs

The electronics will interface with aforementioned MEAs. The design of the MEAs are limited by parameters given by EMC, as there is an interest in using these electrodes in optical imaging of the cortex of a mouse. Limiting the maximum area to $400\ \mu m$ x $200 \mu m$, due to the small region of interest in imaging microscopy.

Another important parameter is the distance between the individual electrodes, which is limited to $20\ \mu m$ due to limitations in single cell measurements. To have as many electrodes as possible within these boundary conditions, the diameter of each electrode has to be made as small as possible. However, in order to ensure manufacturing is still possible, the lower limit for the the electrode diameter is $15\ \mu m$, meaning that the pitch between electrodes is $35\ \mu m$. This limitation is given by wiring complications if the diameter is reduced even further.

The resulting MEA consists of 50 electrodes, as shown in figure 4.9a. There are also designs made with slighly larger electrode sizes in case of complications with the smaller electrodes. Firstly, a MEA with electrodes with a diameter of $25\ \mu m$ and pitch of $45\ \mu m$, which consists of 35 separate electrodes as depicted in figure 4.9b. Also a MEA with electrodes with a diameter of $40\ \mu m$ and pitch of $60\ \mu m$, which consist of 21 separate electrodes as depicted in figure 4.9c. Lastly a larger array of electrodes is also designed, which enables easier testing of the final device. This array consists of electrodes with a diameter of $400\ \mu m$ and 11 electrodes as can be seen in figure 4.9d.



(a) 50 electrodes with $D = 15\mu m$ and pitch $= 35\mu m$

(b) 35 electrodes with $D = 25\mu m$ and pitch $= 45\mu m$

(c) 21 electrodes with $D = 40\mu m$ and pitch $= 60\mu m$

(d) 11 electrodes with $D = 400\mu m$

Figure 4.9: Micro Electrode Arrays (MEAs)

4.3. Development of monolithic process

In this section the previous designs will be combined in a monolithic process. Firstly, the active components will be defined using the GPOS technology and the electronics as described in chapters 3 and 4. Secondly the graphene MEAs will be defined, of which the design is outlined in chapter 4.2. After this the interconnects between the active devices and the MEAs are made. Lastly, the entire devices is encapsulated using paralyne and the contact opening to the electrodes and contact pads are made, to demonstrate a biocompatible interface layer.

The substrate on which the devices will be manufactured is chosen to be a p-type, boron doped, single-side-polished (SSP), 4” wafer with a <100> crystal orientation. This crystal orientation is often chosen to manufacture active devices in. When this orientation is compared to other crystal orientations, the amount of silicon atoms on the surface is lower, giving a lower interface state density when compared to the other available crystal orientations. An overview of the substrate and its parameters can be found in table 4.4.

The active devices will be defined inside an epitaxial layer, this layer is grown using the *ASMI EpisoIn One*. The layer specification are similair to the simulations, a $2\mu m$ layer grown at $1050°C$ and a pressure of $60Torr$.

Type	p-type, boron
Crystal orientation	<100>
Resistivity	2-5 $\Omega \cdot cm$
Thickness	525 $\pm$ 15 μm
Diameter	100 $\pm$ 0.2 mm
Finishing	Single-side-polished (SSP)

Table 4.4: Material properties of 4” single-side-polished (SSP) p-type wafer

The next step in manufacturing is the definition of the zero layer (ZE). This layer is used to align all regions which are defined during the whole process. The ZE is etched into the silicon using Cl_2 and HBr inside of the *Trikon Omega 201*, creating approximately $120nm$ deep trenches inside the EPI layer.

The next step is then the definition of the active devices, as can be seen in figure 4.10a. The process steps used are similar to the process simulation as described in chapter 3, but important steps are outlined below.

The first step for the definition of the active devices is the definition of the N-WELL regions. Before implantation a dirt-barrier oxide of $22nm$ is thermally grown under presence of only oxygen at a temperature of $950°C$ for a duration of 35 minutes. The phosphorus ions are then implanted and annealed similar to the simulations.

For the LOCOS definition the nitride is etched using C_2F_6 at a RF power of $250W$ in the *Drytek Triode 384T*. After the wet oxidation of the LOCOS, the nitride is chemically wet-etched using $H_3PO_4(85\%)$ at $157°C$. But before this step, an oxide dip step is performed in $HF(0,55\%)$ for 1 minute to remove the oxide layer formed on the surface of the nitride. As the etch rate for SiN_x is approximately $2.7nm/min$, the wafers are etched for approximately 40 minutes. The actual total etch time is determined using a test wafer with a similar pattern, as this influences the etch rate.

After the implantation of the V_{th} adjust, the remaining oxide layer which was underneath the nitride is etched using $BHF(1:7)$. As the following step is the gate definition, it is important to ensure that the native oxide on the silicon surface is completly removed. This is done using the Marangoni unit, which etches the native oxide in $HF(0,55\%)$ for 4 minutes after which the surface is treated using IPA vapor, which protect the silicon surface.

The gate oxidation is directly performed after this step, which is thermally grown grown at a temperature of $950°C$ under a pure oxygen environment for a duration of 132 minutes. The polysilicon is deposited in a LPCVD oven using SiH_4 at a temperature of $570°C$, directly followed by an anneal step at $605°C$ for 1 hour. The polysilicon is then doped before pattering using phosphorus, which is then annealed in an argon environment at $950°C$. A $300nm$ layer of SiN_x is then deposited on top using SiH_2Cl_2 and NH_3 at a temperature of $806°C$. After this the gate is defined by etching the nitride using C_2F_6 and the polysilicon is etched using Cl_2 and CF_4.

The spacers next to the gate are then defined using TEOS deposited using a LPCVD furnace, which are etched using a C_2F_6 and CHF_3 chemistry. The SN and SP regions are then defined using the same parameters as during the simulations. Which are then can be annealed in a Ar rich environment at $950°C$ for 50 minutes.

The remaining oxide is then removed using $HF(0,55\%)$ and the remaining nitride on top of the polysilicon is etched using $H_3PO_4(85\%)$. On top of the active devices a passivation layer of TEOS is deposited with a thickness of $1\ \mu m$ at a temperature of $850\ °C$ using LPCVD.

The next step will be defining the graphene electrodes. Before the deposition of the molybdenum, a $2.1\ \mu m$ layer of positive photoresist is deposited and patterened. Which serves as the mask to partially etch the contact openings to the active devices using plasma etching in the Drytek Triode 384T, as shown in figure 4.10b. Only $800\ nm$ of the TEOS is etched, leaving $200\ nm$ to protect the active devices during the graphene growth from the formation of SiC. This step is also needed to reduce the chance of damaging the graphene electrodes, when opening the last portion of contact openings. The photoresist layer is then removed using oxygen enhanced plasma etching in the Tepla.

A $50\ nm$ layer of molybdenum is then deposited using the Trikon Sigma sputter coater at a lowe temperature of $50°C$. A $2.1\ \mu m$ layer of positive photoresist is deposited and patterend to serve as a mask for patterning the molybdenum. Which is done using plasma etching in the Trikon Omega. The photoresist layer is then striped using again oxygen enhanced plasma etching in the Tepla. The graphene layer is then grown on top of the molybdenum catalyst in the Aixtron BlackMagic Pro at a temperature of $935\ °C$, as shown in figure 4.10c.

A $200\ nm$ layer of TiN is deposited on the backside using the Trikon Sigma sputter coater, this layer has excellent barrier properties and it can thus serve as a clean backside. The remaining TEOS of the contact opening is then etched using $BHF(1:7)$, which exposes the source, drain and gate of the active devices. For the connections between the active devices and the connections to and from the graphene electrodes, a layer of $100\ nm$ of titanium and $500\ nm$ aluminium is deposited and patterned using a $3.1\ \mu m$ photoresist mask, as can be seen in figure 4.10d. The titanium layer is first deposited to create a better adhesion with the graphene electrodes, when compared to directly using aluminium. The metals are depostED at a low temperature of $50°C$ The titanium and aluminium are removed using $HF(0,55\%)$.

The photoresist is removed using aceton and IPA. To finalise the device before encapsulation, the molybdenum is removed using H_2O_2, as can be seen in figure 4.10e.

The devices are then encapsulated with $2\ \mu m$ paralyne-C using CVD. In order to create the contact opening to the contactpads and the electrodes, a $500\ nm$ layer of aluminium is deposited to serve as a hard mask. To pattern the aluminium, a $4\ \mu m$ layer of photoresist is deposited and patterned. The aluminium is etched using plasma etching in the Trikon Omega, as depicted in figure 4.10f and 4.10g. The photoresist layer is removed using aceton and the contact openings to the electrodes and the polymer is then etched using plasma etching in the trikon omega. The aluminium hard mask is then removed using $BHF(1:7)$, as shown in figure 4.10g.
The final step is to expose the graphene electrodes by removing the aluminium and titanium on top, this is done using $BHF(1:7)$ locally on the electrodes, resulting in the final device as shown if figure 4.10h. The complete flowchart of the process can be found in appendix D.

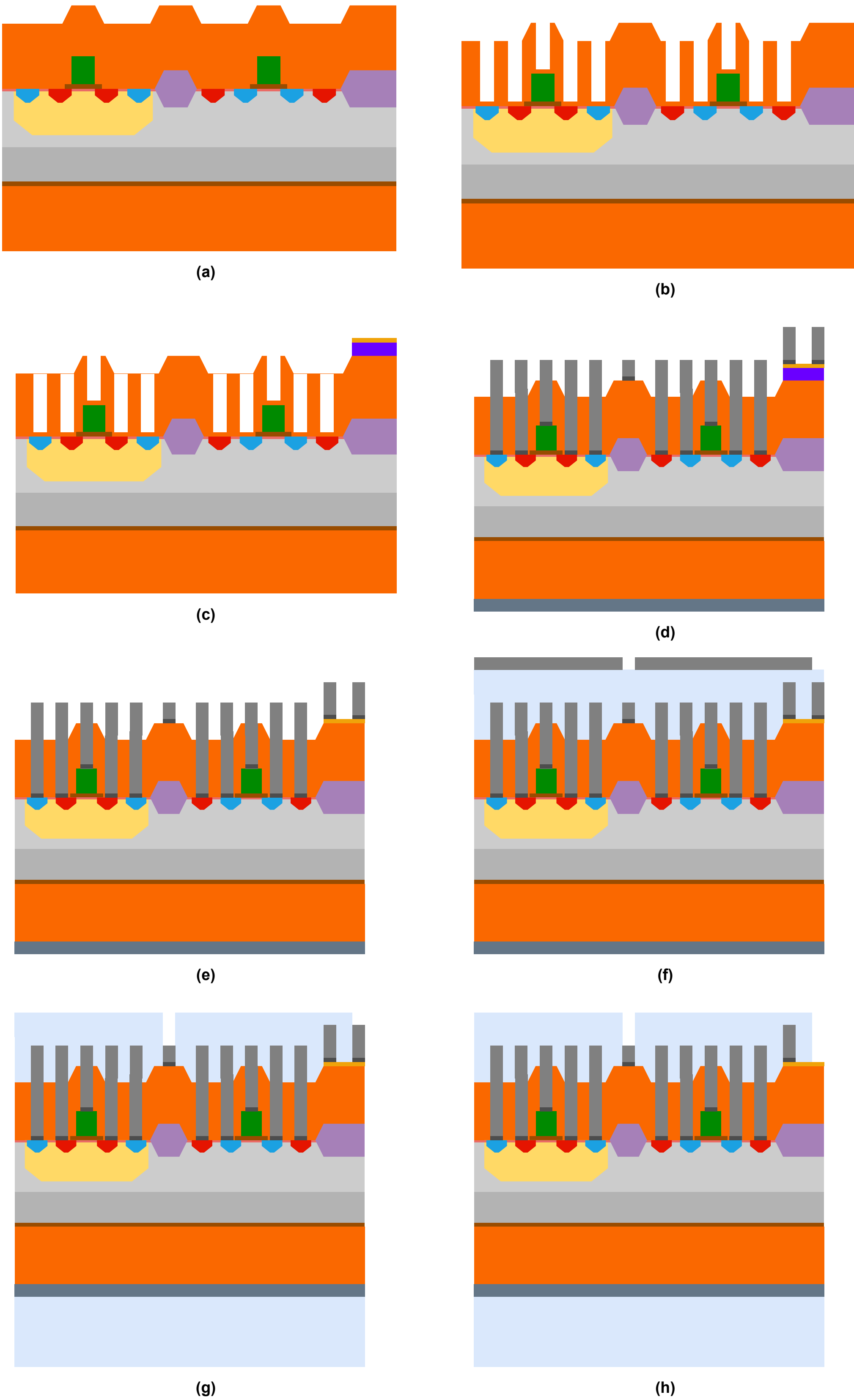


Figure 4.10: Flowchart of final steps

5 Results

For the production, the microfabrication facilities of EKL were used and the implantation facilities of IBS. As this work develops a new technology and process, intermediate and full-scale wafer measurements are required to ensure a positive outcome. As described in chapter 3, several test structures are used to measure an characterise the new technology.

To determine the impact of certain technology features, a variation between these technology features have been made using separate wafers. These varied features are the inclusion or exclusion of graphene, V_{th} adjust doping, gate spacers and an anneal step of the SN and SP. An overview of the wafers with or without these features is given in table 5.1.

As the production of this new technology is uncharted waters, a staggered production process is chosen. This means that at certain critical processing steps a certain amount of wafers were held back, and were only continued if the step was as desired.

Wafer ID number	Graphene	V_{th} adjust	Gate spacer	SN/SP anneal
[061]	■		■	
[064]	■			
[138]	■	■	■	■
[139]	■	■	■	
[140]	■	■		■
[141]	■	■		
[142]		■	■	
[143]		■		
[144]			■	■

Table 5.1: Overview of variation in process wafers

5.1. Characterisation of GPOS process

During production several measurements and dummy wafers are made to confirm that each process step works as expected. From simulations, the dry oxidation of the gate oxide should lead to an oxide thickness of $51.7nm$. However, thin film measurements, using the Woollam ellipsometer and a reflectometer, showed that the actual thickness is $55.7nm$.

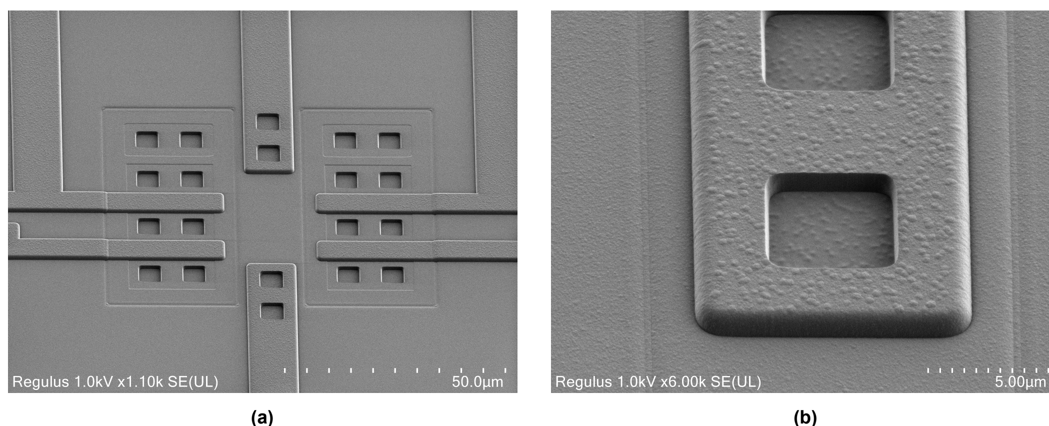
The deposition time for the polysilicon was determined from logbook data inside EKL. The deposition rate was calculated to be $2.5nm/min$, resulting in a deposition time of 200 minutes for a $500nm$ layer thickness. However, the polysilicon layer was measured to be only $426nm$.

Initially it was sought to use $HF(0.55\%)$ for the oxide removal formed on top of the SiN_x after the polysilicon annealing. However, as this oxide was thermally grown, it couldn't be removed using this chemical as it etches thermally grown oxide extremly slow. Instead, $BHF(1:7)$ was used to remove this thin layer of oxide on before the nitride was removed in $H_3PO_4(85\%)$ at $157°C$.

For the etching of the polysilicon, a chlorine based chemistry was used in the *Drytek Triode 384T*, due to machine malfunction, wafer [141] was over-etched by 500 nm. Therefore, this wafer was used as a dummy wafer for further processing.

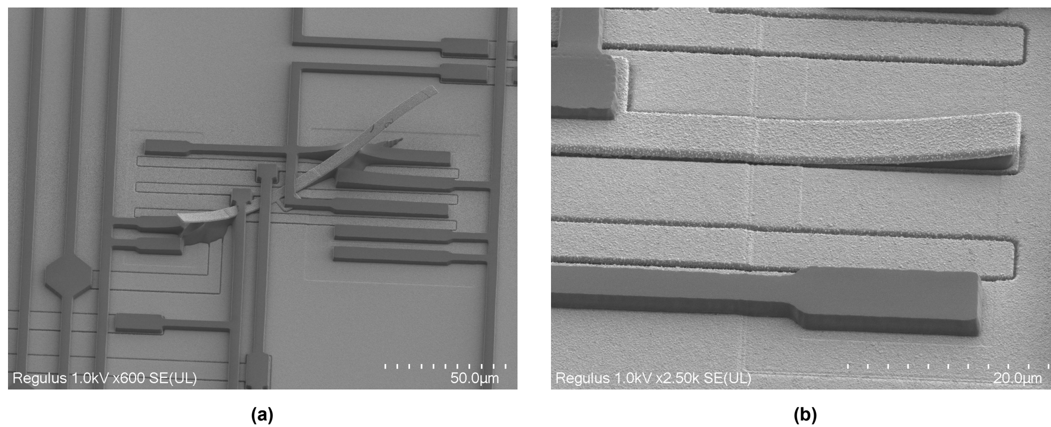
Due to device malfunctioning and time limitations, the passivation layer was changed from LPCVD TEOS to PECVD SiO_2, further processing steps were also adjusted accordingly whilst the etch rate for PECVD oxide is higher then LPCVD. However, during the breakthrough of CO using $BHF(1:7)$, as depicted in figure 4.10c, the oxide layer on top of the polysilicon structures released. This is likely due to the poor adhesion in combination with the poor step coverage of PECVD SiO_2. As can be seen in figure 5.1 the poor stepcoverage creates indentations along the polysilicon structures, this in turn was etched quickly by the wet etchant, leading to the release of these structures as can be seen in figure 5.2.

To resolve this, a photoresist layer was deposited and patterened using the CO mask. This covered and thus protected all areas except the COs during the wet etching. Furthermore, the wet etching was done staggered, going back and forth between short etching and measuring the remaining oxide thickness. From this it can be determined that the oxide etch rate was aproximatly $90nm/min$. The photoresist mask was then stripped using $aceton$ for 3 minutes and IPA for 3 minutes.



(a) (b)

Figure 5.1: SEM image of SiO_2 on top of the polysilicon structures

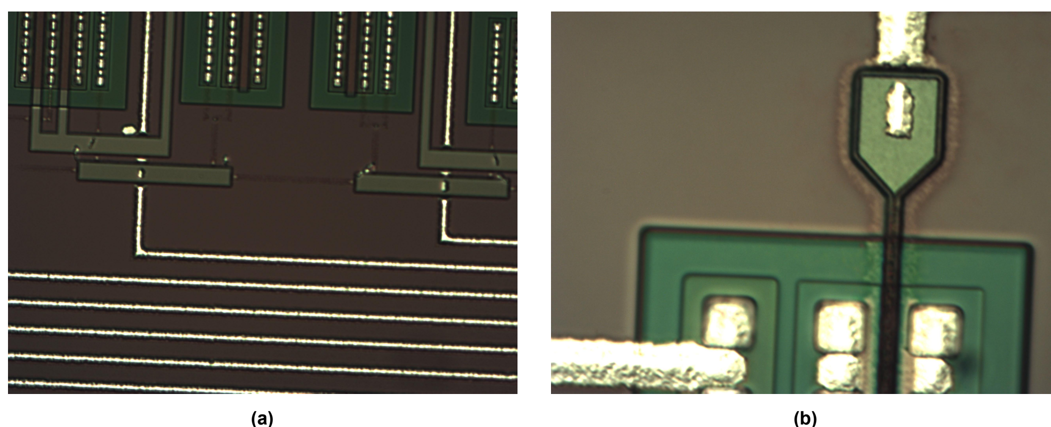


(a) **(b)**

Figure 5.2: SEM images of released SiO_2 structures after $BHF(1:7)$

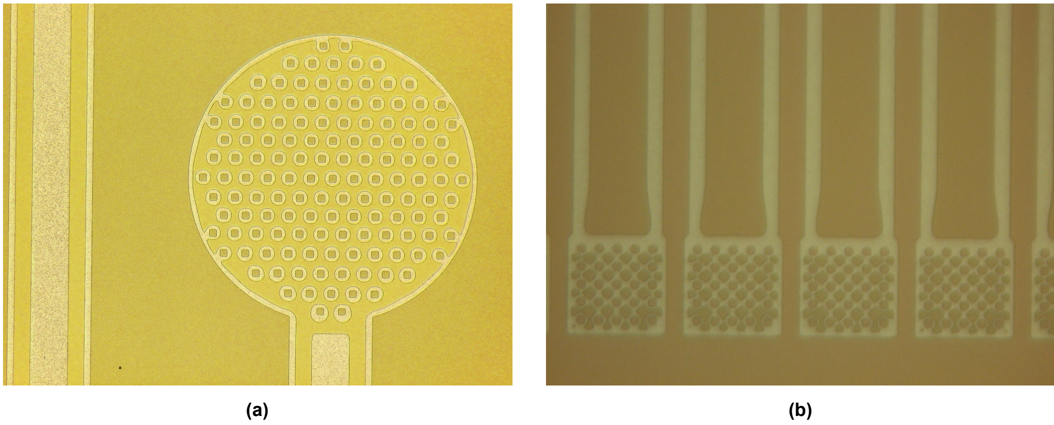
For the metal interconnects, instead of a combination of Ti and $AlSi(1\%)$, a combintation of Ti and pure Al was used. This was due to machine malfunction. These metal tracks were then etched using $HF(0.55\%)$, however as the etch rate for Ti is much faster then that of Al in this solution, the metal lines were over etched or released, as can be seen in figure 5.3. Instead, PES was used to etch the Al followed by $HF(0.55\%)$ to etch the Ti. This method of defining the IC is extremly time sensitive, as PES also etches Mo, as it contains HNO_3. But as the Ti layer in between acts as a barrier, the timing is crucial, the wafers must be removed in time such that the PES does not come in contact with the Mo layer. It was visually determined when the aluminium was removed using PES, as the dies turned a metal brown color, which indicated that the titanium layer was reached. As the total etch time was 2 minutes and 57 seconds for a $500\ nm$ layer of Al in PES, the etch rate can be calculated to be $170nm/min$. The etching of Ti was also done using visual inspection, the wafers were submerged in $HF(0.55\%)$ until bubbles appeared, indicating explosive etching, upon which the wafer was removed and cleaned in DI water. This process was repeated until the dies had a black colour. The bubbles appeared approximately after the wafers were sumberged for 25 seconds. The total etch time until the dies were black of colour was 53 seconds, resulting in an etch rate of $1.89nm/s$.

Due to machine malfunction of the Blackmagic, wafers [061], [139] and [140] were damaged. The Mo tracks appeared to be etched, as can be seen in figure 5.4. Further measurements are required in order to determine if graphene was deposited in the etched regions. But these results were not reproducible, as the remaining wafers did not show similar results when processed two weeks later. Causes of these results therefore require further investigation, but it is believed that due to work on the gas system around that time, the Blackmagic did not function within spec.



(a) **(b)**

Figure 5.3: IC traces after wet etching in $HF(0.55\%)$



(a) (b)

Figure 5.4: Damages to Mo after graphene growth

5.2. Electrical characterisation of GPOS

Due to machine malfuction and time limitations, it was only possible to complete wafer [138], all other wafers only require a metal deposition and patterning step. Full-wafer measurements were done using the Cascade 4-probe station. This tool allows for a forced current or voltage to be applied trough a probe, which also can sense current or voltage. Using this tool, measurements of the different test structures can be done.

Firstly, resistance measurements are conducted, using the measured current and voltage data from the different van der Pauw structures as described in figure 5.5. The sheet resistance of the different layers is then determined using formula 5.1, where R is the slope of the current-voltage plot of the van der Pauw structure. An overview of the determined sheet resistances are given in table 5.2.

$$R_s = \frac{\pi \cdot R}{ln(2)} \tag{5.1}$$

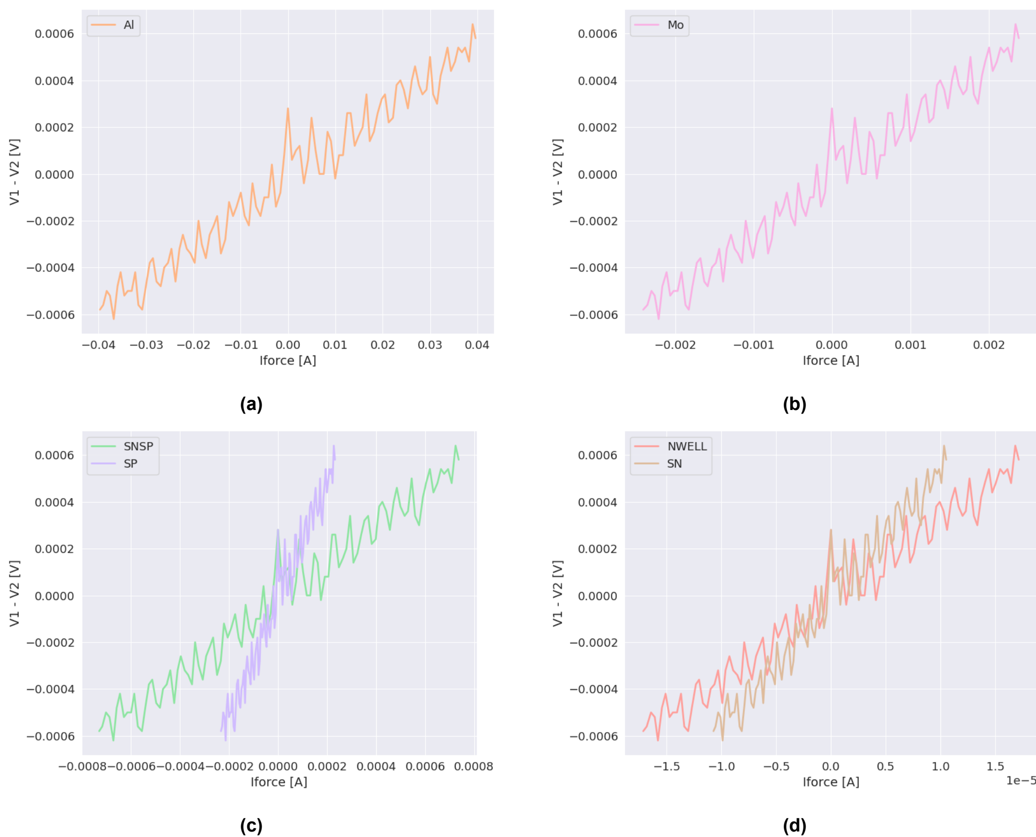


Figure 5.5: Electrical measurements van der Pauw structures for layers **a)** Aluminium, **b)** Molybdenum, **c)** SP and SN/SP and **d)** N-WELL and SN

As can be seen from this table, the sheet resistance of the SN region is extremely high. This error manifest itself in further measurements results as well. To determine wether it is due to a large lateral diffusion, the ELM structures are measured, resulting in a line width measurement which then can be used to determine the lateral diffusion. The results of these measurements are summarised in table 5.3

The $I_d - V_{gs}$ characteristics of the devices are plotted in figure 5.6 and the $I_d - V_{ds}$ characteristics in figure 5.7. From figure 5.6c, it can be seen that there is a large leakage current in the NMOS device. Furthermore, the PMOS device also has different characteristics then simulated, as can be seen in figure 5.6d. It is clear that the V_{th} is shifted.

Material type	Sheet Resistance $[\Omega_\square]$
Al	0.065
SN and SP	151
N-Well	3076
SP	150
SN	3064
Mo	6.39

Table 5.2: Sheet resistance measurements of wafer [138]

Material type	w_m for $w = 2\ \mu m$	w_m for $w = 5\ \mu m$	w_m for $w = 10\ \mu m$
N-Well	27.65	27.83	35.14
SP	2.63	5.49	10.31
SN	23.76	28.42	35.28

Table 5.3: Measured line widths using ELM structures

It can also be seen that the $I_d - V_{ds}$ characteristics are also different then expected from simulation. From these measurements it is clear that there is a large leakage current in the NMOS devices.

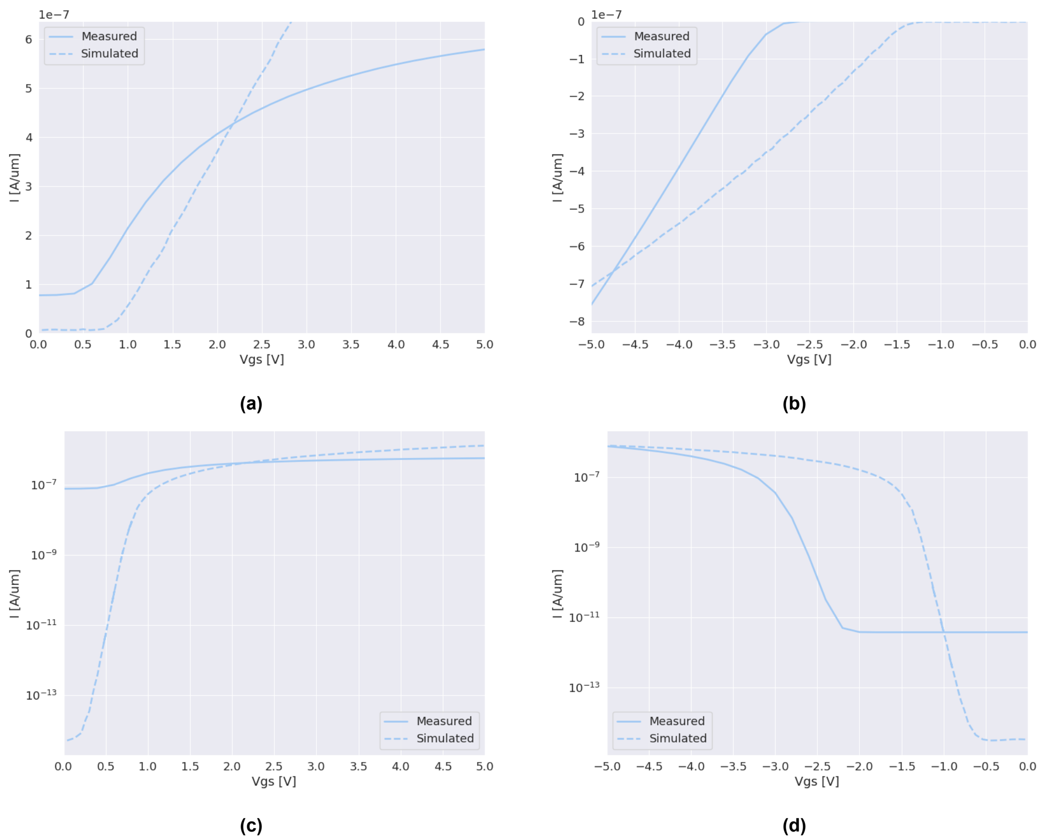
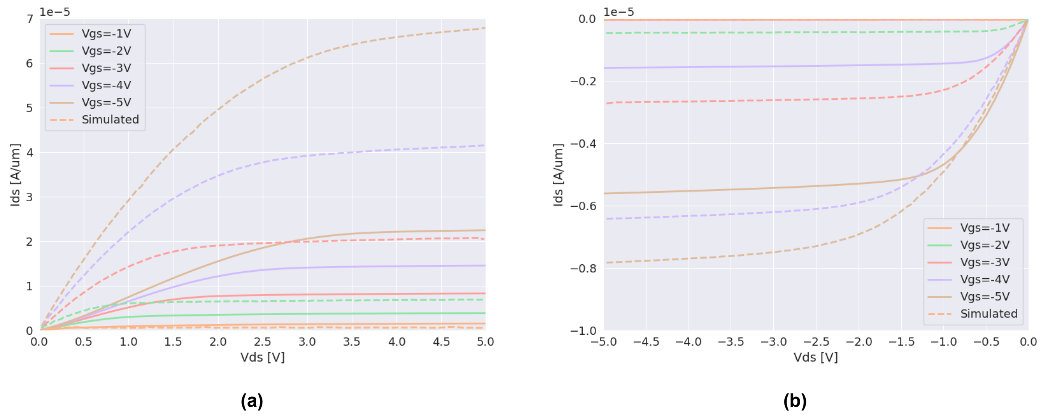


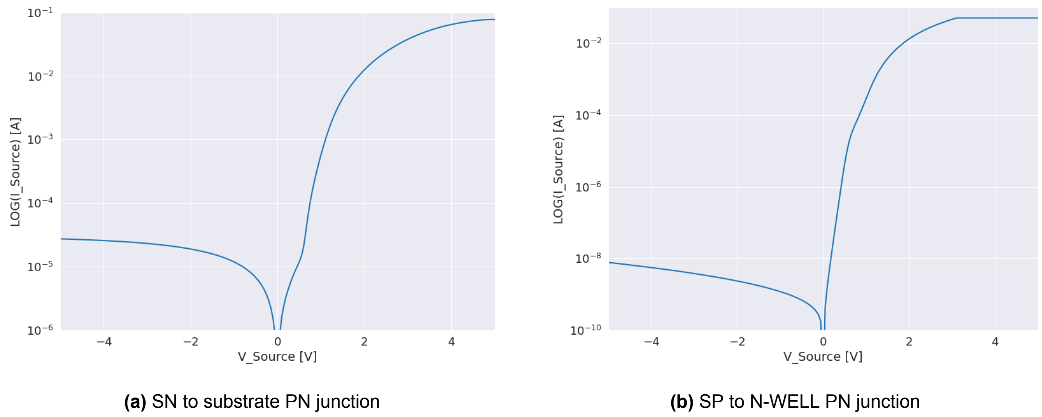
Figure 5.6: $I_d - V_{gs}$ measurements versus simulations for **a)** NMOS device and **b)** PMOS device also plotted logarithmically for **c)** NMOS device and **d)** PMOS device. The devices have a gate length of $5\ \mu m$ and gate width of $50\ \mu m$

To further characterize this unexpected behaviour, measurement of the PN junction between the source/drain regions of the NMOS and PMOS devices were done. The results of these measurements can be found in figure 5.8. It can be seen, that in reverse bias, the current from SN to substrate is orders of magnitude higher when compared to the SP to the NWELL.



(a) (b)

Figure 5.7: $I_d - V_{ds}$ measurements versus simulations for **a)** NMOS device and **b)** PMOS device with gate length of $5\ \mu m$ and gate width of $50\ \mu m$



(a) SN to substrate PN junction

(b) SP to N-WELL PN junction

Figure 5.8: PN junctions of SN and SP to their respective substrates

From these measurements, the most likely explanation would be a wrongly doped region or a unexpected diffusion from a region. This behaviour would indicate the presence of more n-type dopant in the channel of the NMOS and PMOS devices, which could be the case, as the polysilicon is n-type doped and it might have diffused in the top layer of the substrate.

5.3. Simulation revisit and process optimisation

Possible causes of the unexpected behaviour were investigated by revisiting the simulations. Unfortunately, *TSUPREM4* and *MEDICI* didn't not show any discrepancies in the process and the electrical behaviour respectively. It was found that *MEDICI* also has the capability to plot the diffusion regions of the dopants and their junctions, which revealed the issue with the technology. The simulations were repeated using the actual thickness of the polysilicon, which was measured to be $426\ nm$. The gate oxide was also adjsuted to be the real value of $55\ nm$. The simulations revealed that the P^+ dopant in the polysilicon diffuses through the gate oxide in the surface of the substrate, as can be seen in figure 5.9. This creates a n-type channel from source to drain in the NMOS transistor, effectively shorting the source and drain. For the PMOS transistor this extra n-type dopant in the channel makes it harder to open the channel, explaining why the threshold voltage is shifted and why there is a large leakage current from the source to drain for the NMOS device.

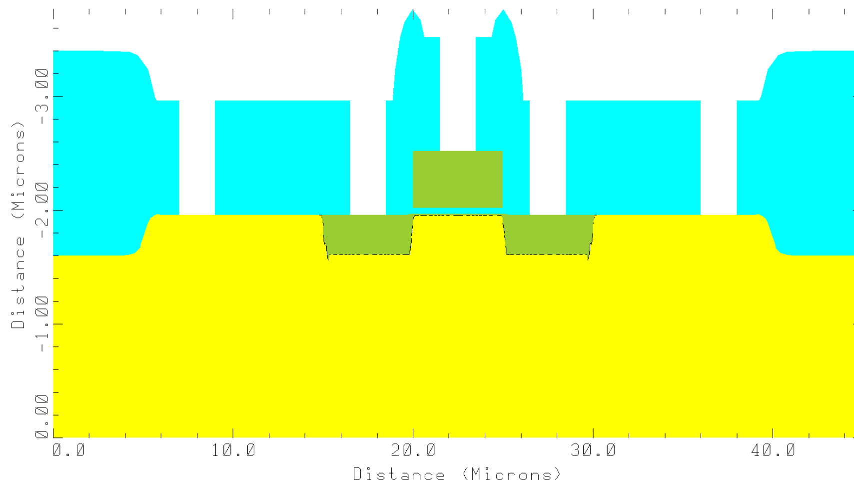


Figure 5.9: Revisit device simulation of NMOS

The leakage of the dopant is caused due to high temperature steps after the doping of the polysilicon gate. In this work, wafers were included which did not include high temperature steps after the gate definition. However, due to machine malfunction, it was not possible to evaluate the performance of these wafers.

Simulations were done for the process of wafer [142], in which the SN/SP anneal was done at a lower temperature of $850°C$. Also, the dry oxidation of the dirt-barrier for the SN/SP was removed as this is done at $950°C$. This resulted in the almost complete removal of the channel formed, as can be seen in figure 5.10.

An alternative solution, is the reduction of the dose and energy during the implantation of the polysilicon. A lower dose lowers the imbalance between the polysilicon and the substrate, leading to less diffusion to the substrate. The lower energy, implants the dopant less deep in the polysilicon, making it more resilient against the high temperature steps. However, this does increase the resistivity of the polysilicon slightly but has to be experimentally confirmed. This can however keep the process intact as currently defined. The resulting depletion region of the channel can be seen in figure 5.11, where the polysilicon dopant dose has been reduced by three to $1 \cdot 10^{15} atoms \cdot cm^{-2}$ and the energy been reduced from $100keV$ to $80keV$.

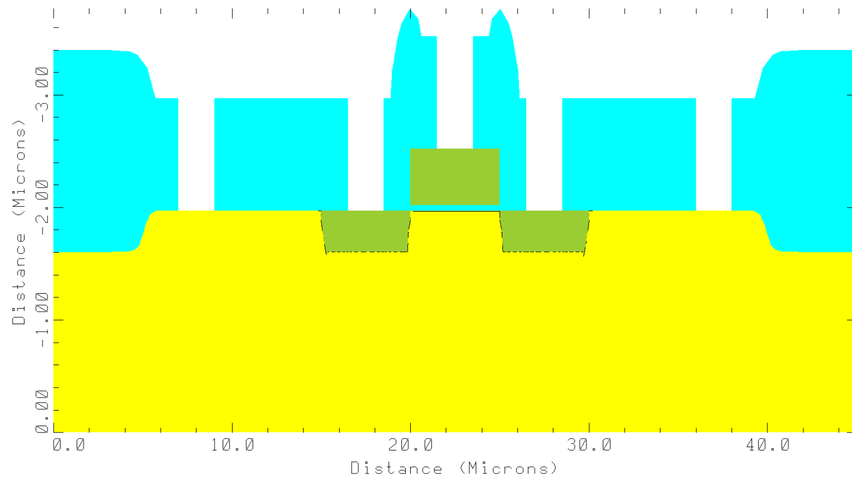


Figure 5.10: Revisit device simulation of NMOS with removal of high temperature steps

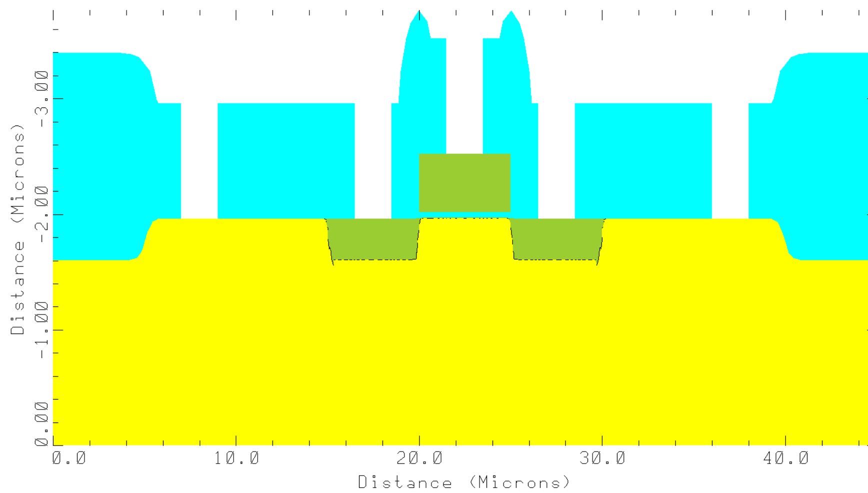


Figure 5.11: Revisit device simulation of NMOS with reduction of dose and energy in polysilicon doping

Another alternative, is to double the thickness of the gate oxide to $100nm$. This increases the barrier thickness, resulting in less dopants being able to cross this barrier, resulting in less n-type dopant in the surface of the substrate as can be seen in figure 5.12. To even further reduce the diffusion of P^+ the oxide can be made even thicker. However, this will change electrical behaviour of the active devices.

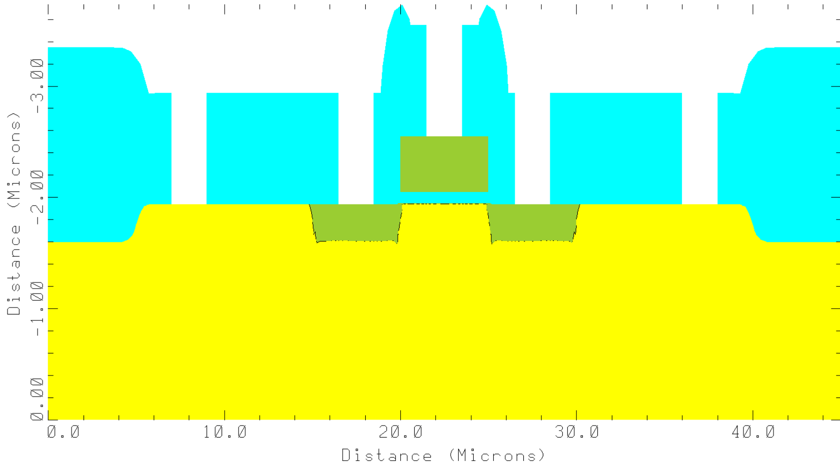


Figure 5.12: Revisit device simulation of NMOS with increase in thickness of gate oxide

6
Conclusion

Multimodal neural interfaces have been gaining a lot of interest in the neuroscience community. As exact mechanisms behind vagus nerve stimulation are still unknown, high end stimulation and recording platforms of neuronal tissue allows for a better understanding of these mechanisms. Combining optogenetics with electrical recording, brings neuroscience yet another step closer. With this work is a step closer to now also possibly integrate circuitry closer to the implantable device, increasing the capabilities of the device and unlocking more research possibilities. The objective of this thesis was to develop by means of a single wafer microfabrication, a fully implantable, graphene-based active implant with soft and flexible encapsulation that could be used for optical stimulation and simultaneous single-cell electrical recording of neuronal tissue.

A process has been demonstrated, which allows for the incorporation of graphene in a CMOS production flow. Firstly, polysilicon was chosen as gate material, for its high melting point and as it is a common gate material. Process simulations and electrical simulated were executed to ensure proper device functionality, and the CVD graphene growth was modelled as a temperature step only. It was furthermore demonstrated that using only simulation data a simple approximation of device functionality can be made using a LEVEL 1 *SPICE* model. Enabling the pre-characterisation design of digital read-out circuitry. Also 3 MEA designs are reported, which theoretically allow for neuronal recording down to single cell precision. Unfortunately, during measurements the transistor showed unwanted behaviour, this was not foreseen due to a error with the simulation or simulation software. However, methods are presented which would ensure proper device functionality.

Due to time limitation this work did not show experimentally the release of the electrodes and the encapsulation of the device. However, these release and encapsulation processes are included within this work. Also characterisation of the the electronics are excluded, as they are not representative of previous simulations due to the error in the functionality of the active devices. And due to time limitations, the MEAs are not characterised, it is however believed that the graphene electrodes are functional as they are based on previous works and no further processing was done once these were defined.

This project has novelty in different aspects. Firstly, the development of a technology that is resilient against the harsh environment whilst growing graphene. It is believed that this technology can be used with minor adjustments to the process. These adjustments have been made and presented, as the understanding of the process had been improved. This work also shows the novelty of a monolithic approach for the development of transparent, flexible active graphene based electrodes. Microfabrication is the majority of this work, and intermediate evaluation of the process was necessary to ensure proper functioning of each process step. As shown, the adhesion problem of the SiO_2 layer was solved, leading to measurable devices.

6.1. Future work

This work successfully reported the development of a monolithic approach for the development of active graphene based implants. However, there is still a need for optimisation of the reported fabrication process. As shown in section 5.2, due to diffusion of P^+ from the polysilicon gate to the substrate surface, the active devices did not perform as expected. This work demonstrated that the mechanism of this is due to the high annealing steps performed after the gate definition. This includes the dirt-barrier, the SN/SP anneal aswell as the graphene growth. As the measurements were conducted on a wafer which had all these features included, it should be noted that this diffusion should be less for the wafers which did not have one or more of these features included. However, due to time limitation it was not possible to further verify this.

As reported, it is also possible to reduce the doping dose, the doping energy or both in order to have less dopants in the polysilicon, resulting in less or no diffusion through the gate oxide. This approach will lead to a higher resistive gate, and as it is also used as the second interconnect layer, higher resistivity in the interconnects. However, this can be resolved by having wider interconnect tracks if made out of polysilicon. A second possible approach would be to increase the gate oxide thickness, as this would result in a larger barrier for the P^+ to diffuse through. This would lead to different device characteristics, but that can be taken into account whilst designing circuitry. Reduction of the high temperature steps after the gate definition in combination with a slightly reduced implantation dose and energy of the polysilicon is most likely the optimal way, resulting in functional active devices.

As this work did not include the actual production of the release of the electrodes and the encapsulation of the device, it is recommended that future work includes this in the production resulting in a bio-compatible, monolithically fabricated, optogenetic compatible, graphene based implant.

As this work also used a standard thickness wafer of $525\mu m$, it is also recommended to explore the possibility of fabrication using the reported process using a thinner wafer. Also as the diesize of the chip was set to be a standard size of $10x10mm$, it could be explored in reducing the footprint of the active area.

Apart from process optimisations, the characterisation of the graphene electrodes in combination with a newly developed circuitry can be explored in future work. As this work was mainly focused on the development of a new technology, which serves as the foundation for graphene compatible circuitry.

Lastly, after an extensive in-vitro characterisation of a fully developed device, it is also recommended to explore in-vivo experiments using the device. It is important to first understand the effect of optical imaging or optogenetics on the behaviour of the graphene electrodes.

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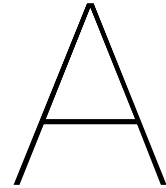


Summary of important commands

Command	Explanation	Usage example
ASSIGN	Assign a value to a variable	ASSIGN NAME=NWDOSE N.VALUE=5E12
MESH	Define the mesh during process simulation	MESH GRID.FAC=1
MASK	Define the mask file, which contains masking information	MASK IN.FILE=mask.tl1
INITIAL	Define the initial data the simulation should start with	INITIAL <100> BORON=1E16 CONCENTR
EPITAXY	Define the deposition of an epitaxial layer	EPITAXY THICKNES=2 SPACES=9 TEMP=1050 BORON=1E16 TIME=180
DIFFUSION	Define a thermal step using diffusion, allows the specification of gasses	DIFFUSION TIME=5 TEMP=800 F.N2=8
DEPOSITION	Define the deposition of a certain material	DEPOSITION NITRIDE THICKNES=0.1 TEMP=800
ETCH	Define the wet or dry etching of a certain material	ETCH NITRIDE DRY THICKNES=0.1
EXPOSE	Define the exposement during the process using a mask from the mask file	EXPOSE MASK=LS
DEVELOP	Define that the photoresist is ready for development	DEVELOP
IMPLANT	Define the implantation of a certain ion during the process	IMPLANT PHOSPHOR DOSE=@NWDOSE ENERGY=@NWENEGRY TILT=7 ROTATION=22

Table A.1: Summary of important commands in the usage of *TSUPREM-4*

Commands	Explanation	Usage example
MESH	Define the process simulation file and mesh characteristics	MESH TSUPREM4 IN.FILE=../process/res
MODELS	Define the models used during the simulations	MODELS CONSRH AUGER BGN SRFMOB2
SYMB	Define the symbolic carrier information	SYMB NEWTON CARRIERS=2 HOLES
METHOD	Define the	
SOLVE	Define the bias that needs to be solved	SOLVE V(d)=0.1
PLOT	Define the output plot	PLOT.1D Y.AXIS=I(d) X.AXIS=V(g) TITLE="Drain characteristics"

Table A.2: Summary of important commands in the usage of *MEDICI*

B

TSUPREM4 scripts used for process simulation

```
1  $ GMOS PROCESS - PMOS DEVICE
2  $ WRITTEN BY: A.T. KARIM
3
4  $ Initialize parameters
5  ASSIGN NAME=SNDOSE N.VALUE=5E15
6  ASSIGN NAME=SNENERGY N.VALUE=40
7  ASSIGN NAME=SPDOSE N.VALUE=6E15
8  ASSIGN NAME=SPENERGY N.VALUE=25
9  ASSIGN NAME=NWDOSE N.VALUE=5E12
10 ASSIGN NAME=NWENERGY N.VALUE=150
11 ASSIGN NAME=VTDOSE N.VALUE=3E11
12 ASSIGN NAME=VTENERGY N.VALUE=25
13 ASSIGN NAME=POLYDOSE N.VALUE=3E15
14 ASSIGN NAME=POLYENERGY N.VALUE=100
15
16 $ Define the grid
17 MESH  GRID.FAC=1
18 $METHOD ERR.FAC=2.0
19
20 $ Read the mask definition file
21 MASK  IN.FILE=mask.tl1
22
23 $ Initialize the structure
24 INITIALIZE <100> BORON=1E16 CONCENTR
25
26 $ 01. EPI-layer growth
27 EPITAXY THICKNES=2 SPACES=9 TEMP=1050 BORON=1E16 TIME=180
28
29 $$ LOCOS definition $$
30 $ 02. DRY oxidation
31 DIFFUSION TIME=5   TEMP=800  F.N2=8
32 DIFFUSION TIME=10  TEMP=800  F.N2=3
33 DIFFUSION TIME=15  TEMP=800  F.N2=3  T.RATE=10
34 DIFFUSION TIME=10  TEMP=950  F.N2=3
35 DIFFUSION TIME=35  TEMP=950  F.O2=3
36 DIFFUSION TIME=30  TEMP=950  F.N2=3  T.RATE=-5
37 DIFFUSION TIME=10  TEMP=800  F.N2=3
38
39 $ 03. Nitride deposition
40 DEPOSITION NITRIDE THICKNES=0.1 TEMPERAT=806
41
42 $ 04. COATING/BAKING/EXPOSURE/DEVELOP
43 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
44 EXPOSE MASK=LS
45 DEVELOP
46
47 $ 05. Etching of nitride/photoresist/oxide
```

```
48 ETCH NITRIDE DRY THICKNES=0.2
49 ETCH PHOTORES ALL
50
51 $ 06. Wet oxidation LOCOS growth
52 DIFFUSION TIME=5    TEMP=800   F.N2=6 F.O2=0.6
53 DIFFUSION TIME=10   TEMP=800   F.N2=6 F.O2=0.6
54 DIFFUSION TIME=20   TEMP=800   F.N2=6 F.O2=0.6 T.RATE=10
55 DIFFUSION TIME=15   TEMP=1000 F.N2=6 F.O2=0.6
56 DIFFUSION TIME=1    TEMP=1000 F.N2=2 F.O2=4
57 DIFFUSION TIME=220 TEMP=1000 F.O2=5 F.H2=8.5
58 DIFFUSION TIME=30   TEMP=1000 F.N2=9
59 DIFFUSION TIME=35   TEMP=1000 F.N2=6 T.RATE=-10
60 DIFFUSION TIME=5    TEMP=600   F.N2=6
61
62 $ 07. Etching of nitride
63 ETCH NITRIDE ALL
64
65 $$ SAVE FILE NWELL $$
66 SAVEFILE OUT.FILE=GPMOSNW
67 SAVEFILE OUT.FILE=GPMOSNWM MEDICI ^POLY.ELEC
68
69 $ 08. VT adjust
70 IMPLANT BORON DOSE=@VTDOSE ENERGY=@VTENERGY TILT=7 ROTATION=22
71
72 $ 09. Etching oxide before gate oxide
73 ETCH OXIDE THICKNES=0.03
74
75 $ 10. Gate oxide defintion (FLOW-48)
76 DIFFUSION TIME=5 TEMP=600 F.N2=6
77 DIFFUSION TIME=15 TEMP=600 F.N2=6
78 DIFFUSION TIME=35 TEMP=950 F.N2=6 T.RATE=10
79 DIFFUSION TIME=15 TEMP=950 F.N2=6
80 DIFFUSION TIME=132 TEMP=950 F.O2=6
81 DIFFUSION TIME=120 TEMP=950 F.N2=6 T.RATE=-10
82 DIFFUSION TIME=5 TEMP=600 F.N2=6
83
84 $$ POLYGATE DEFINITION $$
85 $ 11. Polysilicon deposition (FLOW-52)
86 DEPOSITION POLYSILI THICKNES=0.5 TEMPERAT=570
87
88 $ 12. Dirtbarrier on poly (FLOW-53)
89 DIFFUSION TIME=5   TEMP=800 F.N2=8
90 DIFFUSION TIME=10 TEMP=800 F.N2=3
91 DIFFUSION TIME=15 TEMP=800 F.N2=3 T.RATE=10
92 DIFFUSION TIME=10 TEMP=950 F.N2=3
93 DIFFUSION TIME=35 TEMP=950 F.O2=3
94 DIFFUSION TIME=35 TEMP=950 F.N2=3 T.FINAL=800
95 DIFFUSION TIME=5   TEMP=800 F.N2=3
96
97 $ 13. Arsenic implantation polysilicon (FLOW-54)
98 IMPLANT PHOSPHORUS DOSE=@POLYDOSE ENERGY=@POLYENERGY TILT=7 ROTATION=22
99
100 $ 14. Etch dirtbarrier
101 ETCH OXIDE ALL
102 DEPOSITION NITRIDE THICKNES=0.3 TEMP=400
103
104 $ 15. Anneal polysilicon (FLOW-55)
105 DIFFUSION TIME=5   TEMP=800   F.N2=6
106 DIFFUSION TIME=10 TEMP=800   F.N2=6
107 DIFFUSION TIME=15 TEMP=800   F.N2=6 T.RATE=10
108 DIFFUSION TIME=30 TEMP=950 F.N2=6
109 DIFFUSION TIME=30 TEMP=950 F.N2=6 T.RATE=-5
110 DIFFUSION TIME=5   TEMP=800   F.N2=6
111
112 $ 16. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-56/58)
113 DEPOSITION POSITIVE PHOTORES THICKNES=2.1
114 EXPOSE MASK=PG
115 DEVELOP
116
117 $ 17. Etching oxide/polysilicon (FLOW-64)
118 ETCH OXIDE DRY THICKNES=0.35
```

```
119 ETCH NITRIDE DRY THICKNES=0.4
120 ETCH POLYSILI DRY THICKNES=0.6
121 ETCH PHOTORES ALL
122
123 $ 18. TEOS as Spacer
124 DEPOSITION OXIDE THICKNES=0.2 TEMP=400
125
126 $ 19. Etching Spacer
127 ETCH OXIDE DRY THICKNES=0.255
128
129 $$ SAVE FILE NWELL $$
130 SAVEFILE OUT.FILE=GPMOSPS
131 SAVEFILE OUT.FILE=GPMOSPSM MEDICI ^POLY.ELEC
132
133 $$ SN-DEFINITION $$
134 $ 20. Dirtbarrier
135 DIFFUSION TIME=5   TEMP=800  F.N2=8
136 DIFFUSION TIME=10  TEMP=800  F.N2=3
137 DIFFUSION TIME=15  TEMP=800  F.N2=3  T.RATE=10
138 DIFFUSION TIME=10  TEMP=950  F.N2=3
139 DIFFUSION TIME=35  TEMP=950  F.O2=3
140 DIFFUSION TIME=30  TEMP=950  F.N2=3  T.RATE=-5
141 DIFFUSION TIME=10  TEMP=800  F.N2=3
142
143 $ 21. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-68/70)
144 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
145 EXPOSE MASK=SN
146 DEVELOP
147
148 $ 22. Arsenic inmplantation
149 IMPLANT ARSENIC DOSE=@SNDOSE ENERGY=@SNENERGY TILT=7 ROTATION=22
150
151 $ 23. Photoresist removal
152 ETCH PHOTORES ALL
153
154 $ 24. Anneal SN (FLOW-X) - Skipped
155 $DIFFUSION TIME=5  TEMP=600 F.N2=6
156 $DIFFUSION TIME=10 TEMP=600 F.N2=6
157 $DIFFUSION TIME=30 TEMP=600 F.N2=6 T.RATE=10
158 $DIFFUSION TIME=30 TEMP=900 F.N2=6
159 $DIFFUSION TIME=60 TEMP=900 F.N2=6 T.RATE=-5
160 $DIFFUSION TIME=5  TEMP=600 F.N2=6
161
162 $$ SP-DEFINITION $$
163 $ 25. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-68/70)
164 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
165 EXPOSE MASK=SP
166 DEVELOP
167
168 $ 26. BORON inmplantation
169 IMPLANT BORON DOSE=@SPDOSE ENERGY=@SPENERGY TILT=7 ROTATION=22
170
171 $ 27. Photoresist removal
172 ETCH PHOTORES ALL
173
174 $ 28. Anneal SP (FLOW-X)
175 DIFFUSION TIME=5  TEMP=600 F.N2=6
176 DIFFUSION TIME=10 TEMP=600 F.N2=6
177 DIFFUSION TIME=25 TEMP=600 F.N2=6 T.RATE=10
178 DIFFUSION TIME=15 TEMP=950 F.N2=6
179 DIFFUSION TIME=50 TEMP=950 F.N2=6 T.RATE=-5
180 DIFFUSION TIME=5  TEMP=600 F.N2=6
181
182 $ 29. Etch gate nitride and remaining oxide
183 ETCH NITRIDE THICKNES=0.35
184 ETCH OXIDE THICKNES=0.0255
185
186 $$ SAVE FILE NWELL $$
187 SAVEFILE OUT.FILE=GPMOSDS
188 SAVEFILE OUT.FILE=GPMOSDSM MEDICI ^POLY.ELEC
189
```

```
190 $$ PASSIVATION DEFINITION $$
191 $ 30. TEOS OXIDATION (FLOW-82)
192 DEPOSITION OXIDE THICKNES=1 TEMP=850
193
194 $$ Graphene growth as thermal anneal $$
195 $ 31. Graphene as anneal (FLOW-91)
196 DIFFUSION TIME=4  TEMP=50  F.N2=3 T.RATE=125
197 DIFFUSION TIME=2  TEMP=550 F.N2=3
198 DIFFUSION TIME=4  TEMP=550 F.N2=3 T.RATE=50
199 DIFFUSION TIME=2  TEMP=750 F.N2=3
200 DIFFUSION TIME=6  TEMP=750 F.N2=3 T.RATE=30
201 DIFFUSION TIME=25 TEMP=930 F.N2=3
202 DIFFUSION TIME=10 TEMP=930 F.N2=3 T.RATE=-25
203
204 $$ CO DEFINITION $$
205 $ 32. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-93/95)
206 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
207 EXPOSE MASK=CO
208 DEVELOP
209
210 $ 33. Wet etching for CO (FLOW-97)
211 ETCH OXIDE DRY THICKNES=1.8
212 ETCH NITRIDE DRY THICKNES=0.6
213 ETCH PHOTORES ALL
214
215 $ 34. Aluminium deposition
216 DEPOSITION ALUMINUM THICKNES=1.25 TEMP=300
217
218 $ 35. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-93/95)
219 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
220 EXPOSE MASK=IC
221 DEVELOP
222
223 $ 36. Etching of aluminium
224 ETCH ALUMINUM DRY THICKNES=2
225 ETCH PHOTORES ALL
226
227 $ MIRROR AND COPY STRUCTURE TO COMPLETE
228 STRUCTURE REFLECT RIGHT
229
230 $$ SAVE FILE NWELL $$
231 SAVEFILE OUT.FILE=GPMOSAL
232 SAVEFILE OUT.FILE=GPMOSALM MEDICI ^POLY.ELEC
233
234 $$ PREPARE FILE FOR MEDICI ELECTRICAL SIMULATIONS $$
235 LOAD IN.FILE=GPMOSAL
236 SELECT Z=DOPING
237 PRINT LAYERS X.V=5
238 ELECTRODE NAME=P0 X=8 Y=-3
239 ELECTRODE NAME=P1 X=37 Y=-3
240 ELECTRODE NAME=S X=17.5 Y=-3
241 ELECTRODE NAME=D X=27.5 Y=-3
242 ELECTRODE NAME=G X=22.5 Y=-3
243
244 SAVEFILE OUT.FILE=res MEDICI ^POLY.ELEC
245
246 STOP
```

Listing B.1: Process simulation for NMOS device.

```
1 $MASK TYPE AND LENGTH$
2 TL1 100
3 1E2
4 0 2250
5 7
6
7 $NWELL MASK WITH 1 SLID, BETWEEEN 0 TO 800$
8 NW 1
9 0 800
10
11 $LOCOS MASK WITH 1 SLID, BETWEEEN 500 TO 2250$
```

```
LS 1
500 2250

$POLYSILICON MASK WITH 1 SLID, BETWEEEN 2000 TO 2250$
PG 1
2000 2250

$SHALLOW-N MASK WITH 2 SLIDS, BETWEEEN 0 TO 650 AND 950 TO 2250$
SN 2
0 650
950 2250

$SHALLOW-P MASK WITH 1 SLID, BETWEEN 0 TO 1500$
SP 1
0 1500

$CONTACT OPENING MASK WITH 3 SLIDS, BETWEEN 0 TO 700, 900 TO 1650 AND 1850 TO 2150$
CO 3
0 700
900 1650
1850 2150

$INTERCONNECT MASK WITH 3 SLIDS, BETWEEN 700 TO 900, 1650 TO 1850 AND 2150 TO 2250$
IC 3
700 900
1650 1850
2150 2250
```

Listing B.2: Mask file for NMOS device.

```
$ GMOS PROCESS - PMOS DEVICE
$ WRITTEN BY: A.T. KARIM

$ Initialize parameters
ASSIGN NAME=SNDOSE N.VALUE=5E15
ASSIGN NAME=SNENERGY N.VALUE=40
ASSIGN NAME=SPDOSE N.VALUE=6E15
ASSIGN NAME=SPENERGY N.VALUE=25
ASSIGN NAME=NWDOSE N.VALUE=5E12
ASSIGN NAME=NWENERGY N.VALUE=150
ASSIGN NAME=VTDOSE N.VALUE=3E11
ASSIGN NAME=VTENERGY N.VALUE=25
ASSIGN NAME=POLYDOSE N.VALUE=3E15
ASSIGN NAME=POLYENERGY N.VALUE=100

$ Define the grid
MESH  GRID.FAC=1
$METHOD ERR.FAC=2.0

$ Read the mask definition file
MASK  IN.FILE=mask.tl1

$ Initialize the structure
INITIALIZE <100> BORON=6E15 CONCENTR

$ 01. EPI-layer growth
EPITAXY THICKNES=2 SPACES=9 TEMP=1050 BORON=1E16 TIME=180

$$ N-WELL definition $$
$ 02. Dirt barrier
DIFFUSION TIME=5  TEMP=800 F.N2=8
DIFFUSION TIME=10 TEMP=800 F.N2=3
DIFFUSION TIME=15 TEMP=800 F.N2=3 T.FINAL=950
DIFFUSION TIME=10 TEMP=950 F.N2=3
DIFFUSION TIME=35 TEMP=950 F.O2=3
DIFFUSION TIME=35 TEMP=950 F.N2=3 T.FINAL=800
DIFFUSION TIME=5  TEMP=800 F.N2=3

$ 03. Coating/Baking/Expose/Develop
DEPOSITION POSITIVE PHOTORES THICKNES=2.1
EXPOSE MASK=NW
```

```
42 DEVELOP
43
44 $ 04. Implantation phosphorus n-well
45 IMPLANT PHOSPHOR DOSE=@NWDOSE ENERGY=@NWENERGY TILT=7 ROTATION=22
46
47 $ 05. Photoresist removal
48 ETCH PHOTORES ALL
49
50 $ 06. Annealing n-well drive in
51 DIFFUSION TIME=5   TEMP=600  F.N2=3
52 DIFFUSION TIME=10  TEMP=600  F.N2=3
53 DIFFUSION TIME=55  TEMP=600  F.N2=3 F.O2=0.3 T.FINAL=1150
54 DIFFUSION TIME=10  TEMP=1150 F.N2=3 F.O2=0.3
55 DIFFUSION TIME=480 TEMP=1150 F.N2=3 F.O2=0.3
56 DIFFUSION TIME=90  TEMP=1150 F.N2=3 T.FINAL=600
57 DIFFUSION TIME=5   TEMP=600  F.N2=3
58
59 $ 07. Oxide removal
60 ETCH OXIDE ALL
61
62 $$ LOCOS definition $$
63 $ 08. DRY oxidation
64 DIFFUSION TIME=5   TEMP=800  F.N2=8
65 DIFFUSION TIME=10  TEMP=800  F.N2=3
66 DIFFUSION TIME=15  TEMP=800  F.N2=3  T.RATE=10
67 DIFFUSION TIME=10  TEMP=950  F.N2=3
68 DIFFUSION TIME=35  TEMP=950  F.O2=3
69 DIFFUSION TIME=30  TEMP=950  F.N2=3  T.RATE=-5
70 DIFFUSION TIME=10  TEMP=800  F.N2=3
71
72 $ 09. Nitride deposition
73 DEPOSITION NITRIDE THICKNES=0.1 TEMPERAT=806
74
75 $ 10. COATING/BAKING/EXPOSURE/DEVELOP
76 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
77 EXPOSE MASK=LS
78 DEVELOP
79
80 $ 11. Etching of nitride/photoresist/oxide
81 ETCH NITRIDE DRY THICKNES=0.2
82 ETCH PHOTORES ALL
83
84 $ 12. Wet oxidation LOCOS growth
85 DIFFUSION TIME=5   TEMP=600  F.N2=8
86 DIFFUSION TIME=15  TEMP=600  F.N2=6
87 DIFFUSION TIME=40  TEMP=600  F.N2=6 F.O2=0.6 T.RATE=10
88 DIFFUSION TIME=15  TEMP=1000 F.N2=6 F.O2=0.6
89 DIFFUSION TIME=1   TEMP=1000 F.N2=2 F.O2=4
90 DIFFUSION TIME=20  TEMP=1000 F.O2=2.5 F.H2=4.25
91 DIFFUSION TIME=200 TEMP=1000 F.O2=5 F.H2=8.5
92 DIFFUSION TIME=1   TEMP=1000 F.O2=9
93 DIFFUSION TIME=135 TEMP=1000 F.N2=6 T.FINAL=600
94 DIFFUSION TIME=5   TEMP=600  F.N2=6
95
96 $ 13. Etching of nitride
97 ETCH NITRIDE ALL
98
99 $$ SAVE FILE NWELL $$
100 SAVEFILE OUT.FILE=GPMOSNW
101 SAVEFILE OUT.FILE=GPMOSNWM MEDICI ^POLY.ELEC
102
103 $ 14. VT adjust
104 IMPLANT BORON DOSE=@VTDOSE ENERGY=@VTENERGY TILT=7 ROTATION=22
105
106 $ 15. Etching oxide before gate oxide
107 ETCH OXIDE THICKNES=0.03
108
109 $ 16. Gate oxide defintion (FLOW-48)
110 $$ FURNACE D1 RECIPE
111 DIFFUSION TIME=5     TEMP=600  F.N2=6
112 DIFFUSION TIME=15    TEMP=600  F.N2=6
```

```
113 DIFFUSION TIME=35    TEMP=950  F.N2=6 T.RATE=10
114 DIFFUSION TIME=15    TEMP=950  F.N2=6
115 DIFFUSION TIME=132   TEMP=950  F.O2=6
116 DIFFUSION TIME=120   TEMP=950  F.N2=6 T.RATE=-10
117 DIFFUSION TIME=5     TEMP=600  F.N2=6
118
119 $$ POLYGATE DEFINITION $$
120 $ 17. Polysilicon deposition (FLOW-52)
121 DEPOSITION POLYSILI THICKNES=0.5 TEMPERAT=570
122
123 $ 18. Dirtbarrier on poly (FLOW-53)
124 DIFFUSION TIME=5  TEMP=800 F.N2=8
125 DIFFUSION TIME=10 TEMP=800 F.N2=3
126 DIFFUSION TIME=15 TEMP=800 F.N2=3 T.RATE=10
127 DIFFUSION TIME=10 TEMP=950 F.N2=3
128 DIFFUSION TIME=35 TEMP=950 F.O2=3
129 DIFFUSION TIME=35 TEMP=950 F.N2=3 T.FINAL=800
130 DIFFUSION TIME=5  TEMP=800 F.N2=3
131
132 $ 19. Arsenic implantation polysilicon (FLOW-54)
133 IMPLANT PHOSPHORUS DOSE=@POLYDOSE ENERGY=@POLYENERGY TILT=7 ROTATION=22
134
135 ETCH OXIDE ALL
136 DEPOSITION NITRIDE THICKNES=0.3 TEMP=400
137
138 $ 20. Anneal polysilicon (FLOW-55)
139 DIFFUSION TIME=5  TEMP=800  F.N2=6
140 DIFFUSION TIME=10 TEMP=800  F.N2=6
141 DIFFUSION TIME=15 TEMP=800  F.N2=6 T.RATE=10
142 DIFFUSION TIME=30 TEMP=950 F.N2=6
143 DIFFUSION TIME=30 TEMP=950 F.N2=6 T.RATE=-5
144 DIFFUSION TIME=5  TEMP=800  F.N2=6
145
146 $ 21. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-56/58)
147 DEPOSITION POSITIVE PHOTORES THICKNES=2.1
148 EXPOSE MASK=PG
149 DEVELOP
150
151 $ 22. Etching oxide/polysilicon (FLOW-64)
152 ETCH OXIDE DRY THICKNES=0.35
153 ETCH NITRIDE DRY THICKNES=0.4
154 ETCH POLYSILI DRY THICKNES=0.6
155 ETCH PHOTORES ALL
156
157 $ 23. TEOS as barrier
158 DEPOSITION OXIDE THICKNES=0.2 TEMP=400
159
160 $ 24. Etching oxide
161 ETCH OXIDE DRY THICKNES=0.255
162
163 EXTRACT OXIDE THICKNESS X=22
164
165 $$ SAVE FILE NWELL $$
166 SAVEFILE OUT.FILE=GPMOSPS
167 SAVEFILE OUT.FILE=GPMOSPSM MEDICI ^POLY.ELEC
168
169 $$ SN-DEFINITION $$
170 $ 25. Dirtbarrier
171 DIFFUSION TIME=5   TEMP=800  F.N2=8
172 DIFFUSION TIME=10  TEMP=800  F.N2=3
173 DIFFUSION TIME=15  TEMP=800  F.N2=3  T.RATE=10
174 DIFFUSION TIME=10  TEMP=950  F.N2=3
175 DIFFUSION TIME=35  TEMP=950  F.O2=3
176 DIFFUSION TIME=30  TEMP=950  F.N2=3  T.RATE=-5
177 DIFFUSION TIME=10  TEMP=800  F.N2=3
178
179 $ 26. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-68/70)
180 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
181 EXPOSE MASK=SN
182 DEVELOP
183
```

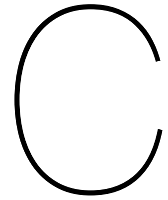
```
184 $ 27. Arsenic inmplantation
185 IMPLANT ARSENIC DOSE=@SNDOSE ENERGY=@SNENERGY TILT=7 ROTATION=22
186
187 $ 28. Photoresist removal
188 ETCH PHOTORES ALL
189
190 $ 29. Anneal SN (FLOW-X) - skipped
191 $DIFFUSION TIME=5  TEMP=600 F.N2=6
192 $DIFFUSION TIME=10 TEMP=600 F.N2=6
193 $DIFFUSION TIME=30 TEMP=600 F.N2=6 T.RATE=10
194 $DIFFUSION TIME=30 TEMP=900 F.N2=6
195 $DIFFUSION TIME=60 TEMP=900 F.N2=6 T.RATE=-5
196 $DIFFUSION TIME=5  TEMP=600 F.N2=6
197
198 $$ SP-DEFINITION $$
199 $ 30. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-68/70)
200 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
201 EXPOSE MASK=SP
202 DEVELOP
203
204 $ 31. BORON inmplantation
205 IMPLANT BORON DOSE=@SPDOSE ENERGY=@SPENERGY TILT=7 ROTATION=22
206
207 $ 32. Photoresist removal
208 ETCH PHOTORES ALL
209
210 $ 33. Anneal SP (FLOW-X)
211 DIFFUSION TIME=5  TEMP=600 F.N2=6
212 DIFFUSION TIME=10 TEMP=600 F.N2=6
213 DIFFUSION TIME=25 TEMP=600 F.N2=6 T.RATE=10
214 DIFFUSION TIME=15 TEMP=850 F.N2=6
215 DIFFUSION TIME=50 TEMP=850 F.N2=6 T.RATE=-5
216 DIFFUSION TIME=5  TEMP=600 F.N2=6
217
218 $ 34. Etch gate nitride and remaining oxide
219 ETCH NITRIDE THICKNES=0.35
220 ETCH OXIDE THICKNES=0.0255
221
222 $$ SAVE FILE NWELL $$
223 SAVEFILE OUT.FILE=GPMOSDS
224 SAVEFILE OUT.FILE=GPMOSDSM MEDICI ^POLY.ELEC
225
226 $$ OXIDATION DEFINITION $$
227 $ 35. TEOS OXIDATION (FLOW-82)
228 DEPOSITION OXIDE THICKNES=1 TEMP=850
229
230 $$ Graphene growth as thermal anneal $$
231 $ 36. Graphene as anneal (FLOW-91)
232 DIFFUSION TIME=4  TEMP=50  F.N2=3 T.RATE=125
233 DIFFUSION TIME=2  TEMP=550 F.N2=3
234 DIFFUSION TIME=4  TEMP=550 F.N2=3 T.RATE=50
235 DIFFUSION TIME=2  TEMP=750 F.N2=3
236 DIFFUSION TIME=6  TEMP=750 F.N2=3 T.RATE=30
237 DIFFUSION TIME=25 TEMP=930 F.N2=3
238 DIFFUSION TIME=10 TEMP=930 F.N2=3 T.RATE=-25
239
240 $$ CO DEFINITION $$
241 $ 37. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-93/95)
242 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
243 EXPOSE MASK=CO
244 DEVELOP
245
246 $ 38. Wet etching for CO (FLOW-97)
247 ETCH OXIDE DRY THICKNES=1.8
248 ETCH NITRIDE DRY THICKNES=0.6
249 ETCH PHOTORES ALL
250
251 $ 39. Aluminium deposition
252 DEPOSITION ALUMINUM THICKNES=1.25 TEMP=300
253
254 $ 40. COATING/BAKING/EXPOSURE/DEVELOP (FLOW-93/95)
```

```
255 DEPOSITION POSITIVE PHOTORES THICKNES=1.4
256 EXPOSE MASK=IC
257 DEVELOP
258
259 $ 41. Etching of aluminium
260 ETCH ALUMINUM DRY THICKNES=2
261 ETCH PHOTORES ALL
262
263 $ MIRROR AND COPY STRUCTURE TO COMPLETE
264 STRUCTURE REFLECT RIGHT
265
266 $$ SAVE FILE NWELL $$
267 SAVEFILE OUT.FILE=GPMOSAL
268 SAVEFILE OUT.FILE=GPMOSALM MEDICI ^POLY.ELEC
269
270 $$ PREPARE FILE FOR MEDICI ELECTRICAL SIMULATIONS $$
271 LOAD IN.FILE=GPMOSAL
272 SELECT Z=DOPING
273 PRINT LAYERS X.V=5
274 ELECTRODE NAME=N0 X=8    Y=-3
275 ELECTRODE NAME=N1 X=37   Y=-3
276 ELECTRODE NAME=S  X=17.5 Y=-3
277 ELECTRODE NAME=D  X=27.5 Y=-3
278 ELECTRODE NAME=G  X=22.5 Y=-2.5
279
280 SAVEFILE OUT.FILE=res MEDICI ^POLY.ELEC
281
282 STOP
```

Listing B.3: Process simulation for PMOS device.

```
1 TL1 100
2 1E2
3 0 2250
4 7
5
6 NW 1
7 0 800
8
9 LS 1
10 500 2250
11
12 PG 1
13 2000 2250
14
15 SN 2
16 0 650
17 950 2250
18
19 SP 1
20 0 1500
21
22 CO 3
23 0 700
24 900 1650
25 1850 2150
26
27 IC 3
28 700 900
29 1650 1850
30 2150 2250
```

Listing B.4: Mask file for PMOS device.



MEDICI scripts used for process simulation

flowchart

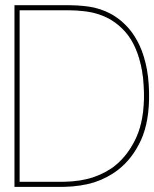
```
mesh tsuprem4 in.file=../process/res
contact name=g
contact name=d
contact name=s
contact name=n1
contact name=n0

MODELS CONSRH AUGER BGN FLDMOB CONMOB
SYMB NEWTON CARRIER=0
SOLVE V(d)=0 V(s)=0 V(g)=0 V(n1)=0 V(n0)=0

COMMENT Setup log file for IV data
MODELS CONSRH AUGER BGN SRFMOB2
SYMB NEWTON CARRIERS=2 HOLES
LOG OUT.FILE=GATE.IVL

COMMENT Do a Poisson solve only to bias the gate
SYMB CARRIERS=2 HOLES
METHOD ICCG DAMPED
SOLVE V(d)=-0.1
SOLVE V(g)=0 ELEC=g VSTEP=-0.1 NSTEP=50

COMMENT Plot Ids vs Vds
PLOT.1D Y.AXIS=I(d) X.AXIS=V(g) POINTS COLOR=2 TITLE="Drain Characteristics"
```

Listing C.1: Id-Vg curve extraction

```
mesh tsuprem4 in.file=../process/res
contact name=g
contact name=d
contact name=s
contact name=n1
contact name=n0

MODELS CONSRH AUGER BGN FLDMOB CONMOB
SYMB NEWTON CARRIER=0
SOLVE V(d)=0 V(s)=0 V(g)=0 V(n1)=0 V(n0)=0

COMMENT Setup log file for IV data
MODELS CONSRH AUGER BGN SRFMOB2
SYMB NEWTON CARRIERS=2 HOLES
METHOD ICCG DAMPED
SOLVE V(g)=-0

SYMB NEWTON CARRIERS=2 HOLES
LOG OUT.FILE=DPdrainIV00.out
```

```
20 SOLVE V(d)=0 ELEC=d VSTEP=-0.1 NSTEP=50
21
22 SYMB NEWTON CARRIERS=2 HOLES
23 METHOD ICCG DAMPED
24 SOLVE V(g)=-1.0
25
26 SYMB NEWTON CARRIERS=2 HOLES
27 LOG OUT.FILE=DPdrainIV10.out
28 SOLVE V(d)=-5.0 ELEC=d VSTEP=0.1 NSTEP=50
29
30 SYMB NEWTON CARRIERS=2 HOLES
31 METHOD ICCG DAMPED
32 SOLVE V(g)=-2.0
33
34 SYMB NEWTON CARRIERS=2 HOLES
35 LOG OUT.FILE=DPdrainIV20.out
36 SOLVE V(d)=0 ELEC=d VSTEP=-0.1 NSTEP=50
37
38 SYMB NEWTON CARRIERS=2 HOLES
39 METHOD ICCG DAMPED
40 SOLVE V(g)=-3.0
41
42 SYMB NEWTON CARRIERS=2 HOLES
43 LOG OUT.FILE=DPdrainIV30.out
44 SOLVE V(d)=-5.0 ELEC=d VSTEP=0.1 NSTEP=50
45
46 SYMB NEWTON CARRIERS=2 HOLES
47 METHOD ICCG DAMPED
48 SOLVE V(g)=-4.0
49
50 SYMB NEWTON CARRIERS=2 HOLES
51 LOG OUT.FILE=DPdrainIV40.out
52 SOLVE V(d)=0 ELEC=d VSTEP=-0.1 NSTEP=50
53
54 SYMB NEWTON CARRIERS=2 HOLES
55 METHOD ICCG DAMPED
56 SOLVE V(g)=-5.0
57
58 SYMB NEWTON CARRIERS=2 HOLES
59 LOG OUT.FILE=DPdrainIV50.out
60 LOG OUT.FILE=GATE2.IVL
61 SOLVE V(d)=-5.0 ELEC=d VSTEP=0.1 NSTEP=50
62
63 PLOT.1D IN.FILE=DPdrainIV50.out Y.AXIS=I(d) X.AXIS=V(d)
64 + LINE.TYP=4 SYMBOL=4 POINTS COLOR=4 UNCHANGE
65
66 PLOT.1D IN.FILE=DPdrainIV40.out Y.AXIS=I(d) X.AXIS=V(d)
67 + LINE.TYP=5 SYMBOL=5 POINTS COLOR=5 UNCHANGE
68
69 PLOT.1D IN.FILE=DPdrainIV30.out Y.AXIS=I(d) X.AXIS=V(d)
70 + LINE.TYP=6 SYMBOL=6 POINTS COLOR=6 UNCHANGE
71
72 PLOT.1D IN.FILE=DPdrainIV20.out Y.AXIS=I(d) X.AXIS=V(d)
73 + LINE.TYP=7 SYMBOL=7 POINTS COLOR=7 UNCHANGE
74
75 PLOT.1D IN.FILE=DPdrainIV10.out Y.AXIS=I(d) X.AXIS=V(d)
76 + LINE.TYP=8 SYMBOL=8 POINTS COLOR=8 UNCHANGE
77
78 PLOT.1D IN.FILE=DPdrainIV00.out Y.AXIS=I(d) X.AXIS=V(d)
79 + LINE.TYP=9 SYMBOL=9 POINTS COLOR=9 UNCHANGE
80
81 LABEL LABEL= "Vgs = -5V" X=-0.75 Y=-8.0E-6 COLOR=4
82 LABEL LABEL= "Vgs = -4V" X=-0.75 Y=-7.6E-6 COLOR=5
83 LABEL LABEL= "Vgs = -3V" X=-0.75 Y=-7.2E-6 COLOR=6
84 LABEL LABEL= "Vgs = -2V" X=-0.75 Y=-6.8E-6 COLOR=7
85 LABEL LABEL= "Vgs = -1V" X=-0.75 Y=-6.4E-6 COLOR=8
86 LABEL LABEL= "Vgs = 0V"  X=-0.75 Y=-6.0E-6 COLOR=9
```

Listing C.2: Id-Vd curve extraction



Flowchart used for production

GRAPHENE-BASED ACTIVE FLEXIBLE IMPLANT

FLOWCHART

VERSION 01

25/11/2021

BATCH INFORMATION			
NAME OF OWNER:	TAWAB KARIM	MASK SET:	PDM 16
NAME OF MENTOR:	STEN VOLLEBREGT	MASK BOX:	496 and 501
RUN NUMBER:	EWI5	DIE SIZE:	10 by 10 mm
WAFER AMOUNT:	9	START DATE:	11/12/2022
SUBJECT TO PCC:		PCC APPROVED:	

DELFT UNIVERSITY OF TECHNOLOGY ELSE KOOI LABORATORY		
Adress	:	Feldmannweg 17, 2628 CT Delft, The Netherlands
P.O. Box	:	5053, 2600 GB Delft, The Netherlands
Phone	:	+31 - (0)15 - 2783868
Fax	:	+31 - (0)15 - 2622163
Website	:	www.tudelft.nl/ewi/onderzoek/faciliteiten/else-kooi-lab

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Detailed information about possible contamination:

Place/Clean Rooms used in process:

- **Write the sequence of used labs from start to finish.**
- **Which (Non-standard) materials or process steps.**
- **Process step number.**
- **What kind of process or machine was used?**
- **The other materials or wafers that contain non-green metals that are also processed in this machine.**

Lab/Clean Room	Non-standard materials	Process step	Machine process	Other materials used in machine
CR100	No	-	-	-
CR10000	Yes, graphene	114	Blackmagic	Cu, Pt, Ni
CR100	Yes, graphene	118	PAS5500/80	
SAL	Yes, graphene	124	SAL	

If there are custom steps in a standard process or possible cross contamination materials are used: Write down the

- **Step number**
- **Material**
- **Machine/tool where the process is done**
- **Pre- and post-process step numbers that are used to prevent cross contamination**

Step number	Material	Machine/Tool/Lab	Process steps to prevent cross contamination
115	Graphene, Cu, Ni	Trikon Sigma	Use own dedicated transport wafers and cassette for contaminated wafers.
117	Graphene, Cu, Ni	EVG 120	TiN backside in step 113
118	Graphene, Cu, Ni	PAS5500/80	TiN backside
125	Graphene, Cu, Ni	PDS 2010 LABCOTER 2	Use own dedicated transport wafers and cassette for contaminated wafers.
126	Graphene, Cu, Ni	Trikon Sigma	Use own dedicated transport wafers and cassette for contaminated wafers.
127	Graphene, Cu, Ni	Brewer science	Use own dedicated transport wafers and cassette for contaminated wafers.
128	Graphene, Cu, Ni	Suss MicroTec	Use own dedicated transport wafers and cassette for contaminated wafers.
129	Graphene, Cu, Ni	Brewer science	Use own dedicated transport wafers and cassette for contaminated wafers.
130	Graphene, Cu, Ni	Axiotron	Use paper underneath wafer
131	Graphene, Cu, Ni	Trikon Omega	Use own dedicated transport wafers and cassette for contaminated wafers.
133	Graphene, Cu, Ni	Trikon Omega	Use own dedicated transport wafers and cassette for contaminated wafers.

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GENERAL RULES

CLEANROOM BEHAVIOUR

Always follow the "**Security and Behaviour**" rules when working in the EKL laboratories.

Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible!!

Use cleanroom gloves when working with vacuum equipment. Do not touch the inside or carriers with bare hands.

Always check equipment and process conditions before starting a process. Do **NOT** make unauthorized changes!

Directly notify the responsible staff member(s) when there are problems with equipment (like malfunction or contamination). Put the system down in the Phoenix reservation system, and turn the equipment status sign from UP or Usable to DOWN.

DO NOT TRY TO REPAIR OR CLEAN EQUIPMENT YOURSELF, and **NEVER** try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

PCC RULES

All substrates, layers and chemicals which are not CMOS compatible are considered to be "**NON-STANDARD**" materials, and may be contaminating.

The use of "non-standard" materials for processing in the class100 and SAL cleanroom must **ALWAYS BE EVALUATED AND APPROVED** by your mentor and in agreement with the PCC document.

Wafers that are contaminated may **NEVER** be processed in any of the equipment without permission of the Equipment owner Special precautions may have to be taken, like the use of a special substrate holder or container.

Check the PCC "Rules & Instructions" - available on the "EKL intranet webpage" - for more details.

CLASS 100 RULES

CLEANING OF WAFERS

After several hours (4 hours max) of storage wafers must always be cleaned before performing a **COATING, FURNACE, EPITAXY** or **DEPOSITION** step.

Use the correct cleaning procedure:

• Tepla stripper	⇨	for removal of implanted or plasma etched photoresist
• Acetone	⇨	for removal of photoresist that is not implanted or plasma etched
• HNO_3 99% (Si)	⇨	for IC compatible wafers which do not need a HNO_3 69.5% step
• HNO_3 99% (Al)	⇨	for wafers which are or have been in contact with one of the following metals: like Al, Al(1%Si), Ge, Ti, Zr
• HNO_3 99% (Si) + HNO3 69.5% (Si)	⇨	for all other IC compatible wafers

Note:

· The above described cleaning procedures are only valid for IC compatible wafers with "standard" materials on them. **In all other situations follow the PCC rules (Previously to be discussed with the mentor).**

· Wafers do not have to be cleaned **after** a furnace, epitaxy or deposition step if the next process step will be performed immediately, unless the wafers are covered with particles.

FURNACE RESTRICTIONS

Wafers that are covered with photoresist or a metal layer may **NEVER** be processed in any of the furnaces. This also applies for wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

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MEASUREMENTS

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the result tables that can be found at some of the equipment!!** The results are used to check the condition of the processes and/or equipment.

It is possible to use the following Class 100 equipment to measure directly onto your (IC compatible) process wafers:

- The Leitz MPV-SP, the WOOLLAM and the SAGAX. These systems are used for thickness measurements of transparent layers. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface (contact measurement), which can be destructive for structures.
- The XL50 SEM. It can be used for inspection of your wafers and for width, depth or thickness measurements.

Note: **After certain measurements cleaning of your wafers may be required for further processing.**

An extra wafer must be processed when other measurement methods will be used (like sheet resistance and junction depth measurements). These wafers cannot be used for further processing.

STARTING MATERIAL

Type:	p-type. boron
Orientation:	<100>
Resistivity:	2-5 Ω·cm
Thickness:	525 ± 15 μm
Diameter:	100 mm ± 0.2 mm
Finishing:	Single side polished
Number of wafer:	14

Wafer no.	Steps	Reason
	All (2x)	Including electrodes
	All (2x)	Including electrodes, do until CO definition
	All	Including electrodes, do until IC definition. To confirm AlSi usage or just Al usage
	All (2x)	Including electrodes, include backside etching. Do until CO definition
	All minus graphene definition (2x)	Only IC.
	All minus graphene definition (2x)	Only IC. No Vt-adjust
	28-31 38-40	Oxide and nitride thicknesses before LOCOS LOCOS thickness
	51-53 61-68	Gate oxide and polysilicon thicknesses Gate oxide after SiN and PolySi etch
	71-75	Leave gate oxide when TEOS is being etched. CONTINUE WITH PREVIOUS WAFER!
	71-75 119	Leave 50 nm TEOS Wet etch remaining TEOS

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1. **START MATERIAL: Silicon wafer p-type (SSP)**

Type: p-type, boron
Orientation: <100>
Resistivity: 2-5 Ω·cm
Thickness: 525 ± 15 µm
Diameter: 100 mm ± 0.2 mm
Finishing: Single side polished

2. **CLEANING: HNO_3 99% and 69.5% (Si cleaning)**

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

Note: not needed if wafers are fresh out of a new box.

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3. LAYER STRIPPING: Native Oxide + Marangoni Drying

Tool(s): Wet bench, modules MARAGONI Si (maximal 6 wafers per cycle)
Location: Class 100 tunnel 5
Manual: See printed manual under the module
Recipe name(s): Manual operation
Settings: Clear the bath with DI water before starting the process

Process conditions		
Prepare	DI water	Rinse the process bath with DI water
Fill with 0.55% HF	0.55% HF	fill the bath with "0.55% HF" (room temperature).
Load wafers		Load the wafers in the carrier slots and activate the lift to lower the carrier into the HF solution.
Etch	DI water	Etch in 0.55% HF for 4 minutes
IPA vapor film	IPA	Switch on the IPA vapor flow for 1 minute
IPA Dry	IPA	Activate the lift to move the carrier out of the solution, the IPA flow is still on.
Shutdown and unload wafers		Turn all the valves to “off” Unload the wafers from the carrier slots

Note: not needed if wafers are fresh out of a new box.

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EPI DEFINITION

4. EPITAXY: P-Type epitaxial film [2um]

Tool(s): ASMI Epsilon One
Location: Class 100 tunnel 4
Manual: See printed manual at the module
Recipe name(s): dimes03

Use the standard dimes03 program designed to grow epi on a buried layer. Modify this program to obtain an epitaxial film with layer characteristics are given below.

Process conditions		
Doping	Boron	1e16 atoms/cm^3, thickness: 2 µm, temperature: 1050 °C, pressure: 60 Torr.

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ZERO LAYER DEFINITION

5. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Co-3012-zero layer – no EBR
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"1 - Co – 3012 – zero layer – no EBR"**.

6. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Litho\ZEFWAM
Settings: Layer ID: 1, Mask ID: COMURK, Exposure energy: 120 mJ/cm^2
Dies: Full wafer

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose mask "COMURK" with job "Litho\ZEFWAM. Use the correct exposure energy (check the energy table).

Note: This should create stepper markers, contact alignment markers and the ZE verniers!

7. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP-no PEB

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

Note: No Post Exposure Bake if dual exposure needed in previous step

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8. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

9. WAFER NUMBERING

Tools(s): Glass pen
Location: Class 100 tunnel 1B

Use the glass pen in the lithography room to mark the wafers with the **BATCH** and **WAFER** number. Write the numbers in the photoresist, just above the waferflat. Always do this after exposure and development! It is **NOT** allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

Note: Write wafer SN in logbook – keep track of which wafer goes through which track!

10. PLASMA ETCHING: Alignment markers (URK's) into EPI

Tool(s): Trikon Ωmega 201
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): URK_NPD
Settings: 20 °C platen temperature

Use the Trikon Ωmega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is **NOT** allowed to change the process conditions and times from the etch recipe!

Use sequence **URK_NPD** (with a platen temperature of **20 °C**) to etch 120 nm deep ASM URK'S into the EPI.

Process conditions						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. Breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. Stabilize	Cl_2/HBr = 80/40 sccm	60 mTorr	00 W	000 W	20 °C	0'15"
3. Bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

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11. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 1**: 1000 watts power and automatic endpoint detection plus a 2 minute over etch.

12. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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NW DEFINITION

13. DRY OXIDATION: Dirt barrier (to collect co-implanted particles)

Tool(s): Furnace A1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): DIBAR
Settings: N13
Time: 115 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	800	Nitrogen: 8.0	5	
Stabilize	800	Nitrogen: 3.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0	15	
Stabilze	950	Nitrogen: 3.0	10	
Oxidation	950	Oxygen: 3.0	35	
Cool down	-5 °C/min	Nitrogen: 3.0	35	
Boat out	800	Nitrogen 3.0	5	

14. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: <50 nm auto5pts

Expected layer thickness: 20-22 nm

15. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): CO - 3012 - 2.1μm - no EBR
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"CO – 3012 – 2.1μm – no EBR"**.

NOTE: A 2.1 μm photoresist because of the phosphorus penetration

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16. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: 1, Mask ID: COMURK, Exposure energy: 260 mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-NW-SN-SP-CO"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "1"**

17. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

18. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

19. IMPLANTATION: Phosphorus N-WELL

Tool(s): Implanter - external
Location: France

Process conditions		
Ion	P^+	5e12 ions/cm^2, Energy: 150 keV **Remarks:** The angle of implant is standard 7°. The flat side of the wafer must be turned 22° north east.

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20. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 4**: 1000 watts power for 15 minutes.

21. CLEANING: HNO_3 99% (Si+ cleaning)

Tool(s): Wet bench, modules, HNO_3 99%, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99% and rinse 2, use the wafer carrier with the red dot for rinse 3.

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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22. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

23. ANNEALING: N-WELL drive in

Tool(s): Furnace A1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): OA002
Settings: N5
Time: 415 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	600	Nitrogen: 3.0	5	
Stabilize	600	Nitrogen: 3.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0 Oxygen: 0.3	55	
Stabilize	1150	Nitrogen: 3.0 Oxygen: 0.3	10	
Drive-in	1150	Nitrogen 3.0 Oxygen 0.3	240	
Cool down	-5 °C/min	Nitrogen: 3.0	90	Wait for operator
Boat out	600	Nitrogen 3.0	5	

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24. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: >50 nm manual

Expected layer thickness 100 nm

25. WET ETCHING: Dirt barrier oxide etch

Tool(s): Wet bench, modules BHF (1:7) Etching Line, Semitool
Location: Class 100 tunnel 4
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool

Process conditions		
Etch 1	BHF solution	Etch time dependent on oxide thickness. Etch rate is **1.3±0.2 nm/s** at **20 °C**. Etch until wafer is fully **Hydrophobic on both sides!**
Clean 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Semitool	Use the standard program. Always use the special orange carrier.
Inspection	Floodlight	Visually inspect the wafers, both sides should be hydrophobic!

26. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110°C, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110°C

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 °C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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LOCOS DEFINITION

27. DRY OXIDATION: Dirt barrier

Tool(s): Furnace A1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): DIBAR
Settings: N13
Time: 115 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	800	Nitrogen: 8.0	5	Temperature goes to 800 °C
Stabilize	800	Nitrogen: 3.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0	15	
Stabilze	950	Nitrogen: 3.0	10	
Oxidation	950	Oxygen: 3.0	35	TSUPREM4: 21.8 nm
Cool down	-5 °C/min	Nitrogen: 3.0	35	
Boat out	800	Nitrogen 3.0	5	

28. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: <50 nm auto5pts

Expected layer thickness: 20-22 nm

29. DEPOSITION: Stoichiometric silicon nitride [100 nm]

Tool(s): Furnace E2
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): 4INCHST
Settings: N5
Time: Determine time based on previous deposition times. (17/11/2021 – 8.07 nm/min)

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	Temperature (in °C)	Time (in min)
SiH_2Cl_2/NH_3 = 315/85	150	806	**Variable time**

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30. MEASUREMENT: Nitride thickness

Tool(s):	Woollam Ellipsometer
Location:	Class 100 tunnel 2
Manual:	See printed manual at the module
Recipe name(s):	Th. SiN on Si
Settings:	>50 nm auto5pts

Expected layer thickness: 100 ± 10 nm

31. COATING AND BAKING

Tool(s):	EVG120 system
Location:	Class 100 tunnel 1B
Manual:	See printed manual at the module
Recipe name(s):	CO 3012 – 1.4µm – no EBR
Settings:	Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"CO 3012 – 1.4µm – no EBR"**.

32. ALIGNMENT AND EXPOSURE

Tool(s):	ASML PAS5500/80
Location:	Class 100 tunnel 1B
Manual:	See printed manual at the module
Recipe name(s):	Special\2021-jobs\GMOS_10x10_4img
Settings:	Layer ID: 1, Mask ID: COMURK, Exposure energy: 115 mJ/cm^2
Dies:	Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-LO-PS-MO-AL"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "1"**

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33. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

34. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:
- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

35. PLASMA ETCHING: Nitride frontside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): Stdsin
Settings: Change etch time to accommodate 100 nm (18s + 2s overetch)

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Time (in min)
C_2F_6 = 65	130	250	**Variable time**

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

36. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 4**: 1000 watts power for 15 minutes

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37. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

38. WET OXIDATION: LOCOS [850nm]

Tool(s): Furnace D1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): WET1000
Settings: N4
Time: 341 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	600	Nitrogen: 8.0	5	
Stabilize	600	Nitrogen: 6.0	10	
Heat up	+10 °C/min	Nitrogen: 6.0 Oxygen: 0.6	40	
Stabilze	1000	Nitrogen: 6.0 Oxygen: 0.6	15	
Purge	1000	Nitrogen: 2.0 Oxygen: 4.0	1	
Oxidation	1000	Oxygen: 5.0 Hydrogen: 8.5	220	TSUPREM4: 895 nm
Purge	1000	Oxygen: 9.0	1	
Cool down	-10 °C/min	Nitrogen: 6.0	135	Wait for operator
Boat out	600	Nitrogen 6.0	5	

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39. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: >50 nm auto5pts

Expected layer thickness: 820 - 880 nm

40. WET ETCHING: Oxide dip etch from nitride layer

Tool(s): Wet bench, modules BHF (1:7), QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the 3 blue dot wafer carrier labelled with the red dot for the cleaning in BHF.

Process conditions		
Clean 1	BHF	Immerse the wafers for 1 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Avenger Ultra pure-6	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a black dot.

Note: Don't use the rinse module with Triton X-100

41. WET ETCHING: Nitride stripping

Tool(s): Wet bench, modules H_3PO_4 85% 157 °C, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the H_3PO_4 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the brown dot for the cleaning in H_3PO_4 85%, rinse 1. Check if the temperature of the H_3PO_4 85% is 157 ºC

Process conditions		
Etch	H_3PO_4 85%	Immerse the wafers for 45 min. Temperature is 157 °C. Etching selectivity of nitride over thermal oxide is ± 30:1. Etchrate of LPCVD nitride is ±2.7 nm/min at 157 °C. **Note:** Etch until the frontside and backside of the wafer is cleared
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Avenger Ultra pure-6	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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42. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s):	Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location:	Class 100 tunnel 5
Manual:	Manual operation for the HNO_3 modules
Recipe name(s):	Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings:	Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ^{o}C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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Vt ADJUST

43. IMPLANTATION: Boron Vt adjust

Tool(s): Implanter - external
Location: France

Process conditions		
Ion	B^+	3e11 ions/cm^2, Energy: 25 keV **Remarks:** The angle of implant is standard 7°. The flat side of the wafer must be turned 22° north east.

44. CLEANING: HNO_3 99% (Si+ cleaning)

Tool(s): Wet bench, modules, HNO_3 99%, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99% and rinse 2, use the wafer carrier with the red dot for rinse 3.

Process conditions		
Clean 2	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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45. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ^{o}C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

46. WET ETCHING: Dirt barrier oxide etch

Tool(s): Wet bench, modules BHF (1:7) Etching Line, Semitool
Location: Class 100 tunnel 4
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool

Process conditions		
Etch 1	BHF solution	Etch time dependent on oxide thickness. Etch rate is **1.3±0.2 nm/s** at **20 °C**. Etch until wafer is fully **Hydrophobic on back sides!**
Clean 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Semitool	Use the standard program. Always use the special orange carrier.
Inspection	Floodlight	Visually inspect the wafers, both sides should be hydrophobic!

Note: Check if Maragoni step can also remove oxide by leaving in HF longer. If so, this and next step can be skipped!

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47. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

48. LAYER STRIPPING: Native Oxide + Marangoni Drying

Tool(s): Wet bench, modules MARAGONI Si (maximal 6 wafers per cycle)
Location: Class 100 tunnel 5
Manual: See printed manual under the module
Recipe name(s): Manual operation
Settings: Clear the bath with DI water before starting the process

Process conditions		
Prepare	DI water	Rinse the process bath with DI water
Fill with 0.55% HF	0.55% HF	fill the bath with "0.55% HF" (room temperature).
Load wafers		Load the wafers in the carrier slots and activate the lift to lower the carrier into the HF solution.
Etch	DI water	Etch in 0.55% HF for 4 minutes
IPA vapor film	IPA	Switch on the IPA vapor flow for 1 minute
IPA Dry	IPA	Activate the lift to move the carrier out of the solution, the IPA flow is still on.
Shutdown and unload wafers		Turn all the valves to “off” Unload the wafers from the carrier slots

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GATE DEFINITION

49. DRY OXIDATION: Gate oxide (50 nm)

Tool(s): Furnace D1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): DRY950
Settings: N10
Time: 210 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	600	Nitrogen: 8.0	5	
Stabilize	600	Nitrogen: 6.0	15	
Heat up	+10 °C/min	Nitrogen: 6.0	35	
Stabilze	950	Nitrogen: 6.0	15	
Oxidation	950	Oxygen: 6.0	132	TSUPREM4: 51.7 nm
Cool down	-10 °C/min	Nitrogen: 6.0	120	Wait for operator
Boat out	600	Nitrogen 6.0	5	

Note: Perform this step directly after previous step!

50. DEPOSITION: Low stress polysilicon (500 nm)

Tool(s): Furnace E3
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): LPOLYBIN
Settings: N1
Time: 407 min

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	Temperature (in °C)	Time (in min)
SiH_4 = 45	150	570	**VARIABLE TIME**

Note: Perform this step directly after previous step! Determine deposition rate from logbooks! LPOLYBIN includes an anneal step of 605 °C for 1 hour!

51. MEASUREMENT: Polysilicon thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. Si on SiO2
Settings: >50 nm auto5pts

Expected layer thickness: 500 nm

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52. DRY OXIDATION: Dirt barrier

Tool(s): Furnace A1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): DIBAR
Settings: N13
Time: 115 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	800	Nitrogen: 8.0	5	Temperature goes to 800 °C
Stabilize	800	Nitrogen: 3.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0	15	
Stabilze	950	Nitrogen: 3.0	10	
Oxidation	950	Oxygen: 3.0	30	Oxide growth is faster on polysilicon
Cool down	-5 °C/min	Nitrogen: 3.0	35	
Boat out	800	Nitrogen 3.0	5	

53. IMPLANTATION: Phosphorous doping

Tool(s): Implanter - external
Location: France

Process conditions		
Ion	P^+	3e15 ions/cm^2, Energy: 100 keV **Remarks:** The angle of implant is standard 7°. The flat side of the wafer must be turned 22° north east.

54. CLEANING: HNO_3 99% (Si+ cleaning)

Tool(s): Wet bench, modules, HNO_3 99%, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99% and rinse 2, use the wafer carrier with the red dot for rinse 3.

Process conditions		
Clean 2	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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55. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

56. ANNEALING: Doped polysilicon anneal

Tool(s): Furnace C2
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): TST_VART
Settings: N16
Time: 125 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	800	Nitrogen: 6.0	5	
Stabilize	800	Nitrogen: 6.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0	15	
Stabilize	950	Nitrogen: 3.0	10	
Drive-in	950	Nitrogen 3.0	20	
Cool down	-5 °C/min	Nitrogen: 3.0	30	Wait for operator
Boat out	800	Nitrogen 8.0	5	

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57. WET ETCHING: Dirt barrier oxide etch

Tool(s): Wet bench, modules BHF (1:7) Etching Line, Semitool
Location: Class 100 tunnel 4
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool

Process conditions		
Etch 1	BHF solution	Etch time dependent on oxide thickness. Etch rate is **1.3±0.2 nm/s** at **20 °C**. Etch until wafer is fully **Hydrophobic on both sides!**
Clean 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Semitool	Use the standard program. Always use the special orange carrier.
Inspection	Floodlight	Visually inspect the wafers, both sides should be hydrophobic!

58. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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59. DEPOSITION: Stoichiometric silicon nitride [300 nm]

Tool(s): Furnace E2
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): 4INCHST
Time: Variable

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	Temperature (in °C)	Time (in min)
SiH_2Cl_2/NH_3 = 315/85	150	806	**Variable time**

Note: The final thickness of the layer depends on the deposition time, which can be calculated from the average deposition rate.

60. MEASUREMENT: Nitride thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiN on Si
Settings: >50 nm auto5pts

Expected layer thickness: 300 ± 10 nm

61. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): CO 3012 – 2.1μm – no EBR instead
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"CO 3012 – 2.1μm – no EBR"**.

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62. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: TOPLEFT, Mask ID: COMURK, Exposure energy: - mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-LO-PS-MO-AL"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "TOPLEFT"**

63. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 ºC for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 ºC for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

64. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

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65. PLASMA ETCHING: Nitride frontside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): Stdsin
Settings: Change etch time to accommodate 300 nm

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Time (in min)
C_2F_6 = 65	130	250	**Variable time**

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

66. PLASMA ETCHING: Polysilicon frontside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): C3DMPOLY (Faulty recipe, needs correction!)
Settings: Change etch time to accommodate 500 nm

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

Process conditions				
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Gasses (in Torr)	Time (in s)
Cl_2/CF_4 = 20/200	165	175	Helium: 12.0	35
Cl_2/CF_4 = 20/200	165	50	Helium: 12.0	33
Cl_2 = 100	125	70	Helium: 12.0	75

67. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 4**: 1000 watts power for 15 minutes.

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68. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s):	Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location:	Class 100 tunnel 5
Manual:	Manual operation for the HNO_3 modules
Recipe name(s):	Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings:	Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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SPACER DEFINITION

69. DEPOSITION: TEOS [200 nm]

Tool(s): Furnace E1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): NEWTEOS
Settings: N1
Time: Variable

Process conditions			
Gasses & Flows (in sccm)	Pressure (in mTorr)	Temperature (in °C)	Time (in min)
TEOS	250	700	**Variable command**

Note: The final thickness of the layer depends on the deposition time, which can be calculated from the average deposition rate

70. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: >50 nm auto5pts

Expected layer thickness: 340 - 360 nm

71. PLASMA ETCHING: Oxide backside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): STDOXIDE or OXSFTLND (soft landing preferred) – used C3DMTEOS (36sec)
Settings: Change etch time to accommodate 330 nm

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

Process conditions: CD3MTEOS				
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Gasses (in Torr)	Time (in s)
C2F6/CHF3 = 12/108	180	300	Helium: 12.0	**Variable command**

Note: The final thickness of the layer depends on the deposition time, which can be calculated from the average deposition rate

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72. PLASMA ETCHING: Oxide frontside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): STDOXIDE or OXSFTLND (soft landing preferred) – used C3DMTEOS (36sec)
Settings: Change etch time to accommodate 330 nm

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

Process conditions: CD3MTEOS				
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Gasses (in Torr)	Time (in s)
C2F6/CHF3 = 12/108	180	300	Helium: 12.0	**Variable command**

Note: The final thickness of the layer depends on the deposition time, which can be calculated from the average deposition rate

73. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: >50 nm auto5pts

Expected layer thickness: 10-30 nm

74. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110°C, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110°C

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 °C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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SN DEFINITION

75. DRY OXIDATION: Dirt barrier (to collect co-implanted particles)

Tool(s): Furnace A1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): DIBAR
Settings: N13
Time: 115 min

Process conditions				
Process	TEMPERATURE (in °C)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
Boat in	800	Nitrogen: 8.0	5	Temperature goes to 800 °C
Stabilize	800	Nitrogen: 3.0	10	
Heat up	+10 °C/min	Nitrogen: 3.0	15	
Stabilze	950	Nitrogen: 3.0	10	
Oxidation	950	Oxygen: 3.0	35	
Cool down	-5 °C/min	Nitrogen: 3.0	35	
Boat out	800	Nitrogen 3.0	5	

76. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: Class 100 tunnel 2
Manual: See printed manual at the module
Recipe name(s): Th. SiO2 on Si
Settings: <50 nm auto5pts

Expected layer thickness: 20-22 nm

77. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Co-3012-1.4μm – no EBR
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"1 - Co – 3012 – 1.4μm – no EBR"**.

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78. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: TOPLEFT, Mask ID: COMURK, Exposure energy: - mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-NW-SN-SP-CO"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "TOPLEFT"**

79. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

80. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

81. IMPLANTATION: Arsenic SN

Tool(s): Implanter - external
Location: France

Process conditions		
Ion	As^+	5e15 $ions/cm^2$, Energy: 40 keV **Remarks:** The angle of implant is standard 7°. The flat side of the wafer must be turned 22° north east.

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82. LAYER STRIPPING: Photoresist

Tool(s):	Tepla Plasma 300
Location:	Class 100 tunnel 5
Manual:	See printed manual at the module
Recipe name(s):	Program 1
Settings:	1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 4**: 1000 watts power for 15 minutes.

83. CLEANING: HNO_3 99% (Si+ cleaning)

Tool(s):	Wet bench, modules, HNO_3 99%, QDR, Avenger Ultra pure-6
Location:	Class 100 tunnel 5
Manual:	Manual operation for the HNO_3 modules
Recipe name(s):	Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings:	Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99% and rinse 2, use the wafer carrier with the red dot for rinse 3.

Process conditions		
Clean 2	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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84. CLEANING: HNO_3 99% AND 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ^{o}C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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SP DEFINITION

86. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Co-3012-1.4µm-no EBR
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"1 - Co – 3012 – 1.4µm – no EBR"**.

87. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: TOP RIGHT, Mask ID: COMURK, Exposure energy: - mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-NW-SN-SP-CO"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "TOP RIGHT"**

88. DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

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89. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:
- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

90. IMPLANTATION: Boron SP

Tool(s): Implanter - external
Location: France

Process conditions		
Ion	B^+	6e15 ions/cm^2, Energy: 20 keV **Remarks:** The angle of implant is standard 7°. The flat side of the wafer must be turned 22° north east.

91. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 4**: 1000 watts power for 15 minutes.

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92. CLEANING: HNO_3 99% (Si+ cleaning)

Tool(s): Wet bench, modules, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99% and rinse 2, use the wafer carrier with the red dot for rinse 3.

Process conditions		
Clean 2	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

93. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the HNO_3 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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94. WET ETCHING: Oxide dip etch from nitride layer

Tool(s): Wet bench, modules 0.55% HF, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the 3 blue dot wafer carrier labelled with the red dot for the cleaning in BHF.

Process conditions		
Clean 1	BHF	Immerse the wafers for 1 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Avenger Ultra pure-6	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a black dot.

Note: Don’t use the rinse module with Triton X-100

95. WET ETCHING: Nitride stripping

Tool(s): Wet bench, modules H_3PO_4 85% 157 °C, QDR, Avenger Ultra pure-6
Location: Class 100 tunnel 5
Manual: Manual operation for the H_3PO_4 modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings: Use the white wafer carrier labelled with the brown dot for the cleaning in H_3PO_4 85%, rinse 1. Check if the temperature of the H_3PO_4 85% is 157 ℃

Process conditions		
Etch	H_3PO_4 85%	Immerse the wafers for 130 min. Temperature is 157 °C. Etching selectivity of nitride over thermal oxide is ± 30:1. Etchrate of LPCVD nitride is ±2.7 nm/min at 157 °C. **Note:** Etch until the frontside of the wafer is cleared
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Avenger Ultra pure-6	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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96. WET ETCHING: Dirt barrier oxide etch

Tool(s): Wet bench, modules BHF (1:7) Etching Line, Semitool
Location: Class 100 tunnel 4
Manual: Manual operation for the BHF modules
Recipe name(s): Default recipe for the Avenger Ultra pure-6 rins/dry tool

Process conditions		
Etch 1	BHF solution	Etch time dependent on oxide thickness. Etch rate is **1.3±0.2 nm/s** at **20 °C**. Etch until wafer is fully **Hydrophobic on both sides!**
Clean 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Semitool	Use the standard program. Always use the special orange carrier.
Inspection	Floodlight	Visually inspect the wafers, both sides should be hydrophobic!

97. PLASMA ETCHING: Polysilicon backside etching

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): C3DMPOLY (Recipe broken, need another one)
Settings: Change etch time to accommodate 500 nm

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

Process conditions				
Gasses & Flows (in sccm)	Pressure (in mTorr)	RF Power (in W)	Gasses (in Torr)	Time (in s)
Cl_2/CF_4 = 20/200	165	175	Helium: 12.0	35
Cl_2/CF_4 = 20/200	165	50	Helium: 12.0	33
Cl_2 = 100	125	70	Helium: 12.0	75

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98. CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s):	Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location:	Class 100 tunnel 5
Manual:	Manual operation for the HNO_3 modules
Recipe name(s):	Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings:	Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ^{o}C
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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CO DEFINITION

99. DEPOSITION: TEOS (1000 nm)

Tool(s): Furnace E1
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): 4INCHST
Time: Variable

Process conditions from recipe LN100			
Gasses & Flows (in sccm)	Pressure (in mTorr)	Temperature (in °C)	Time (in min)
TEOS	250	700	**Variable command**

Note: The final thickness of the layer depends on the deposition time, which can be calculated from the average deposition rate. Only do 500 nm per run!

100. COATING AND BAKING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1 - CO – 3012 – no EBR
Settings: Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"1 – CO – 3012 – 2.1um – no EBR"**.

101. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: BOTTOM RIGHT, Mask ID: COMURK, Exposure energy: - mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-NW-SN-SP-CO"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "BOTTOM RIGHT"**

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102.DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

103.INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

104. PLASMA ETCHING: TEOS [950 nm]

Tool(s): Drytek Triode 384T
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): STDOXIDE
Settings: Change etch time to accommodate 950 nm

Follow the operating instructions from the manual when using this machine. It is **not** allowed to change process conditions from the etch recipe, except for the etch time!

105.LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 1**: 1000 watts power and automatic endpoint detection plus a 2 minute over etch.

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106.CLEANING: HNO_3 99% and 69.5% (Si cleaning)

Tool(s):	Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location:	Class 100 tunnel5
Manual:	Manual operation for the HNO_3 modules
Recipe name(s):	Default recipe for the Avenger Ultra pure-6 rins/dry tool
Settings:	Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if the temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 110 ^oC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the black dot.
Rinse 3 /Dry	DI water	Use the Avenger Ultra pure-6 "rinser/dryer" with program, and the white carrier with a red dot.

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GRAPHENE DEFINITION

107.DEPOSITION: Molybdenum catalyst

Tool(s):	Trikon Sigma sputter coater
Location:	Class 100 tunnel 3
Manual:	See printed manual at the module
Recipe name(s):	Mo_50nm_50C
Settings:	50 degree

Use recipe Mo_50nm_50C to obtain a 50nm thick layer.

NOTE: Visual inspection, the wafer must look shiny.

108.COATING AND BAKING

Tool(s):	EVG120 system
Location:	Class 100 tunnel 1B
Manual:	See printed manual at the module
Recipe name(s):	1-Co-3012-1.4μm-no EBR
Settings:	Relative humidity of 48 ± 2%

Use the coater of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HDMS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- A soft bake at 95 ℃ for 90 seconds

Always check the relative humidity (48 ± 2%) in the room before coating and follow the instructions for this equipment.

Use program **"1 - Co – 3012 – 2.1um – no EBR"**.

109.ALIGNMENT AND EXPOSURE

Tool(s):	SUSS MicroTec MA/BA8
Location:	Class 100 Tunnel 1B
Manual:	See printed manual at module
Recipe name(s):	softcontact
Settings:	Mask ID: MO, Exposure energy: - mJ/cm^2

Processing will be performed on the SUSS MicroTec MA/BA8 contact allignerr. Follow the operating instructions from the manual when using this machine.

Note: Use contaminated chuck for contaminated wafers!

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110.DEVELOPING

Tool(s): EVG120 system
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): 1-Dev-SP

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- A post-exposure bake at 115 ºC for 90 seconds
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100 ºC for 90 seconds

Always follow the instructions for this equipment.

Use program **"1-Dev-SP"**.

111.INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:
- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

112.PLASMA ETCHING: Molybdenum [50 nm]

Tool(s): Trikon Ωmega 201
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): MO-TEST2
Settings: 25 ºC platen temperature

Use the Trikon Ωmega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is **NOT** allowed to change the process conditions and times from the etch recipe!

Use sequence **MO-TEST2** (with a platen temperature of **25 ºC**) to etch 50 nm deep. Check the time, normally 1:10

113.LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: Class 100 tunnel 5
Manual: See printed manual at the module
Recipe name(s): Program 1
Settings: 1000 W power and automatic endpoint detection + 2 min over etching. Use quartz carrier.

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 1**: 1000 watts power and automatic endpoint detection plus a 2 minute over etch.

Note: Check if all photoresist is removed, crucial before growing graphene!

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114.LAYER GROWTH: Graphene

Tool(s): AIXTRON BlackMagic Pro
Location: Class 10000
Manual: See printed manual at the module
Recipe name(s): Mo_New_935C_20minCH4_20min pre-annealing
Settings: 1000 °C for 40 min.

Grows graphene layers on top of the Mo using LPCVD.

NOTE: Use graphene reactor interior, Cu contaminated! Use white blister with Cu written on it. Use contaminated tweezers for handling. And red box for Cu contaminated wafers!

115.DEPOSITION: Backside TiN

Tool(s): Trikon Sigma sputter coater
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): Ti10_TiN_200_50C
Settings: 50 degree

NOTE: Use dedicated Cu carrier wafer! Use dedicated cassette for contaminated wafers!

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CO BREAKTHROUGH DEFINITION

116.COATING AND BAKING

Tool(s): Brewer science manual spinner
Location: Class 100 Tunnel 1 (PolymerLab)
Manual: See printed manual at module
Recipe name(s): 3012_2.1um

First do a **10 min HDMS** treatment (Hexamethyldisilazane vapor with nitrogen as a carrier gas). Followed by photoresist coating of **3012 with a thickness of 2.1um**. **Soft bake** on the hotplate for **90 min at 95 °C**.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

117.ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: BOTTOM RIGHT, Mask ID: COMURK, Exposure energy: - mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-NW-SN-SP-CO"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "BOTTOM RIGHT"**

Note: Use wafer carriers for contaminated wafers!

118.DEVELOPING

Tool(s): Brewer science manual spinner
Location: Class 100 tunnel 1 (PolymerLab)
Manual: See printed manual at the module
Recipe name(s): MF322

Use the manual developer station to develop the wafers. The process consists of:

- A post-exposure bake at 115 °C for 60 seconds.
- Developing with AZ400k for 60 seconds.
- A hard bake at 100 °C for 60 seconds

Always follow the instructions for this equipment.

Use developer **"MF322"**.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

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119.INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

120.WET ETCHING: CO

Tool(s): BHF (1:7)
Location: SAL
Manual:
Recipe name(s):

Note: Check etch rate, 1.3nm/s and time! TEOS etch rate is different then thermal oxide!

121.LAYER STRIPPING: PHOTORESIST

Tool(s): Glass beker
Location: SAL
Manual: See printed manual at the module
Recipe name(s): Aceton (3 min) + IPA (3 min)

Use developer **"Aceton"** and **"IPA"** for 3 min each to remove the photoresist layer.

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IC DEFINITION

122.METALIZATION: Ti [100 nm] and Al [500 nm]

Tool(s): Trikon Sigma 204
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): 100nm Ti@50 and 500nm Al@50C
Settings: Deposit Titanium followed by Aluminium directly without removal from machine!

123.COATING AND BAKING

Tool(s): Brewer science manual spinner
Location: Class 100 Tunnel 1 (PolymerLab)
Manual: See printed manual at module
Recipe name(s): 3027_3.1um

First do a **10 min HDMS** treatment (Hexamethyldisilazane vapor with nitrogen as a carrier gas). Followed by photoresist coating of **3027 with a thickness of 3.1um**. **Soft bake** on the hotplate for **90 min at 95** °C.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

124. ALIGNMENT AND EXPOSURE (FOR WAFERS WITHOUT GRAPHENE)

Tool(s): ASML PAS5500/80
Location: Class 100 tunnel 1B
Manual: See printed manual at the module
Recipe name(s): Special\2021-jobs\GMOS_10x10_4img
Settings: Layer ID: BOTTOM RIGHT, Mask ID: COMURK, Exposure energy: 115 mJ/cm^2
Dies: Only A dies

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **"EC2201-GMOS-LO-PS-MO-AL"** with job **"special\2021-jobs\GMOS_10x10_4img"** for custom die layout and with job **"litho\10x10_4img"** for a full wafer exposure. Use the correct exposure energy (check the energy table). Use **layer ID: "BOTTOM RIGHT"**

125.ALIGNMENT AND EXPOSURE (FOR WAFERS WITH GRAPHENE)

Tool(s): SUSS MicroTec MA/BA8
Location: Class 100 Tunnel 1B
Manual: See printed manual at module
Recipe name(s):
Settings: Use Aluminium contact aligner mask

Processing will be performed on the SUSS MicroTec MA/BA8 contact allignerr. Follow the operating instructions from the manual when using this machine.

Note: Use contaminated chuck for contaminated wafers!

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126.DEVELOPING

Tool(s): Brewer science manual spinner
Location: Class 100 tunnel 1 (PolymerLab)
Manual: See printed manual at the module
Recipe name(s): MF322

Use the manual developer station to develop the wafers. The process consists of:

- A post-exposure bake at 115 ºC for 60 seconds.
- Developing with AZ400k for 60 seconds.
- A hard bake at 100 ºC for 60 seconds

Always follow the instructions for this equipment.

Use developer **"MF322"**.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

127. INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:

- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

128.WET ETCHING: Al/Ti

Tool(s): HF 0.55%
Location: SAL
Manual: See printed manual at module

Note: Directly do after developing, otherwise another bake is required!

129. LAYER STRIPPING: Photoresist

Tool(s): Aceton/IPA
Location: SAL
Manual: See printed manual at module

130. WET ETCHING: Mo etching

Tool(s): H_2O_2, DI
Location: SAL

Etch the Mo layer away underneath the graphene to form graphene tracks without using transfer methods. Etching usually takes ~5 minutes. First try with one wafer. Follow this by rinsing in DI water (gently!). If necessary, dry in air instead of using the spinner.

Note: Use contaminated glass ware

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POLYMER DEFINITION

131. DEPOSITION: Paralyne [2 um]

Tool(s): PDS 2010 LABCOTER 2
Location: MEMS travee 2
Manual: See printed manual at module
Settings: 20 grams of dimer. Use A-174 Silane promotor before deposition

For this purpose, use 20 grams of dimer to have 10um paralyne. Follow the instructions for parylene deposition. Also use A-174 Silane adhesion promotor before deposition.

Note: Use Cu contaminated carrier and carrier wafers!

132.METALIZATION: Al [500nm]

Tool(s): Trikon Sigma 204
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): AlSi_500nm_1kW_25C
Settings: Deposit Aluminium

Note: Use own dedicated transport wafers and cassette for contaminated wafers! Also perform LUR before deposition!

133.COATING AND BAKING

Tool(s): Brewer science manual spinner
Location: Class 100 Tunnel 1 (PolymerLab)
Manual: See printed manual at module
Recipe name(s): AZ_ECI-3027-4000nm

First do a **10 min HDMS** treatment (Hexamethyldisilazane vapor with nitrogen as a carrier gas). Followed by photoresist coating of **AZ_ECI-3027-4000nm**. **Soft bake** on the hotplate for **90 min at 95 °C**.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

134.ALIGNMENT AND EXPOSURE

Tool(s): SUSS MicroTec MA/BA8
Location: Class 100 Tunnel 1B
Manual: See printed manual at module
Recipe name(s):
Settings:

Expose **"FILL IN"** with job **"FILL IN"**. Use the correct exposure energy (check the energy table).

Processing will be performed on the SUSS MicroTec MA/BA8 contact allignerr. Follow the operating instructions from the manual when using this machine.

Note: Use contaminated chuck for contaminated wafers!

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135.DEVELOPING

Tool(s): Brewer science manual spinner
Location: Class 100 tunnel 1 (PolymerLab)
Manual: See printed manual at the module
Recipe name(s): AZ400k

Use the manual developer station to develop the wafers. The process consists of:
- A post-exposure bake at 115 ºC for 60 seconds.
- Developing with AZ400k for 60 seconds.
- A hard bake at 100 ºC for 60 seconds

Always follow the instructions for this equipment.

Use program **"AZ400k"**.

Note: Use contaminated chuck for contaminated wafers. Also, use dedicated hotplate for contaminated wafers!

136.INSPECTION

Tool(s): Microscope Axiotron
Location: Class 100 tunnel 1B
Manual: See printed manual at the module

Visually inspect the wafers through a microscope:
- No resist residues are allowed
- Check the linewidth of all the structures
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

Note: Use a paper underneath wafer, to avoid contamination!

137.PLASMA ETCHING: Al [500 nm]

Tool(s): Trikon Ωmega 201
Location: Class 100 tunnel 3
Manual: See printed manual at the module
Recipe name(s): al05 350
Settings: 25 ºC platen temperature

Use the Trikon Ωmega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is **NOT** allowed to change the process conditions and times from the etch recipe!

Use sequence **al05 350** (with a platen temperature of **25 ºC**) to etch 500 nm deep. Check the time.

Note: Use own dedicated transport wafers and cassette for contaminated wafers!

138. LAYER STRIPPING: Photoresist

Tool(s): Aceton, IPA
Location: Class 100 Tunnel 1 (PolymerLab)
Manual: See printed manual at module

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139.PLASMA ETCHING: Paralyne PCO

Tool(s): Trikon Ωmega 201
Location: Class 100 tunnel3
Manual: See printed manual at the module
Recipe name(s): Par1 ER (187nm/min) or Par3 ER (940nm/min)
Settings: 20 °C platen temperature

Use the Trikon Ωmega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is **NOT** allowed to change the process conditions and times from the etch recipe!

Note: Use own dedicated transport wafers and cassette for contaminated wafers! Also perform LUR before deposition! Also do LUR test before etching!

140.WET ETCHING: Al hardmask

Tool(s): BHF (1:7)
Location: SAL
Manual: See printed manual at module
Settings: Room temperature, etch rate 1um/min

141.WET ETCHING: Al/Ti electrodes

Tool(s): BHF (1:7)
Location: SAL
Manual: See printed manual at module
Settings: Room temperature, etch rate 1um/min

Note: Only etch the electrodes, to remove the remaining aluminium and titanium.

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