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A Compact 10-MHz *RC* Frequency Reference With a Versatile Temperature Compensation Scheme

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***Abstract*— This article presents the design and implementation of a compact CMOS *RC* frequency reference. It consists of a frequency-locked loop (FLL) that locks the period of a voltage-controlled oscillator (VCO) to the time an *RC* network takes to charge to a reference voltage. Conventionally, an *RC* time constant with a near-zero temperature coefficient (TC) is realized by using a trimmed network of resistors with different TCs. In this work, such a network is used to realize a temperature-dependent reference voltage whose TC cancels that of a single-resistor *RC* time constant. Compared with the conventional approach, which requires resistors with TCs of opposite polarity, the proposed approach can be implemented with resistors with TCs of similar polarity, and so it can be implemented in most CMOS processes. To compensate for *RC* spread, a trimmed capacitor is used to adjust the nominal frequency. Two prototype chips were made, one based on p-/n-polysilicon resistors and other based on silicided/p-diffusion resistors. Fabricated in a standard 180-nm CMOS technology, the polysilicon-based prototype has an active area of 0.01 mm^2 and an absolute inaccuracy of ±2800 ppm from −45 °C to 125 °C with a fixed TC-trim and a one-point frequency trim. After one week of accelerated aging at 150 °C, however, significant drift (5000 ppm) was observed. The diffusion-based prototype exhibits greater inaccuracy (±14 400 ppm) but much less drift (600 ppm).**

***Index Terms*— CMOS frequency reference, on-chip trimming, resistor aging, temperature compensation.**

I. Introduction

MOST electronic systems require frequency references for timing, communication, and synchronization. Crystal oscillators have traditionally been used because of their excellent accuracy and low jitter [1]. Being discrete components, however, they tend to be bulky and costly, making them less suitable for low-cost applications, such as wake-up timers [2], [3] and micro-controllers [4].

Recently, various alternatives to crystal oscillators have been proposed, including oscillators based on micro-electromechanical system (MEMS) [5], bulk acoustic wave (BAW) [6] resonators, as well as thermal-diffusivity-based [6], *LC*-based [9], [10], and *RC*-based [11], [12], [13], [14], [15], [16] frequency references. Of these, oscillators based on MEMS and BAW resonators can achieve similar accuracy and jitter performance [5], [6]. However, their fabrication is not CMOS compatible, resulting in two-die solutions. While thermal-diffusivity-based frequency references [6] are CMOS-compatible, they rely on a power-hungry heater (several milliwatts) to establish well-defined thermal delays. *LC*-based frequency references can achieve excellent jitter and accuracy, but they typically operate at gigahertz (GHz) frequencies, consume milliwatts of power, and occupy significant chip area [9], [10], making them unsuitable for the targeted applications.

RC-based relaxation oscillators are better suited for applications with strict area and power constraints. Previous designs can achieve sub-0.01-mm^2 active area and consume only tens of microwatts [15], [16]. Over temperature, however, they typically suffer from frequency errors in the order of several 1000 ppm. By replacing their comparators with a loop filter and a voltage-controlled oscillator (VCO), relaxation oscillators can be transformed into frequency-locked loops (FLLs) [13]. Their short-term inaccuracy can then be improved to 100-ppm levels by using high-resolution compensation and trimming techniques, such as delta–sigma ($\Delta\Sigma$) [11], [12] or pulse density modulation [13], but at the expense of chip area. However, their long-term stability is limited by resistor aging, which is now the subject of much research [17], [18], [19].

This article describes a compact FLL-based *RC* frequency reference. It locks the period of a VCO to the time an *RC* network takes to charge to a reference voltage established by a resistive divider. By adjusting the TC of the resistive divider instead of that of the *RC* network, 1st-order temperature compensation can be flexibly achieved with resistors with TCs of the same polarity, which are available in most CMOS processes. To investigate the long-term drift of different types of resistors, two prototype chips were fabricated, one based on polysilicon (poly) resistors (with negative TCs) and the other based on diffusion resistors (with positive TCs). The poly version achieved an inaccuracy of ±2800 ppm from −45 °C to 125 °C after a fixed TC trim and a one-point frequency

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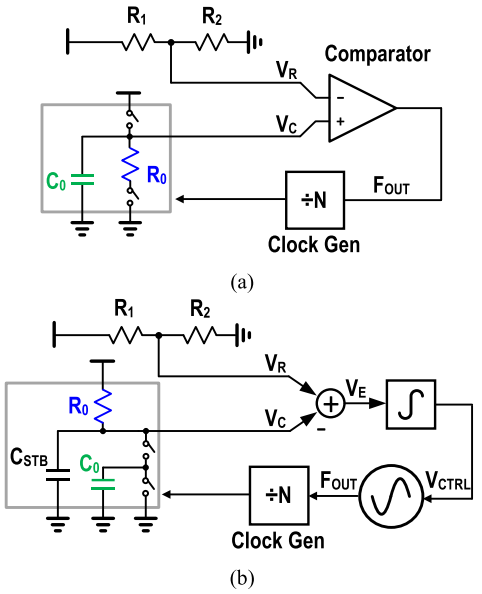


Fig. 1. Simplified schematics of (a) conventional *RC* relaxation oscillators and (b) conventional *RC*-based FLLs.

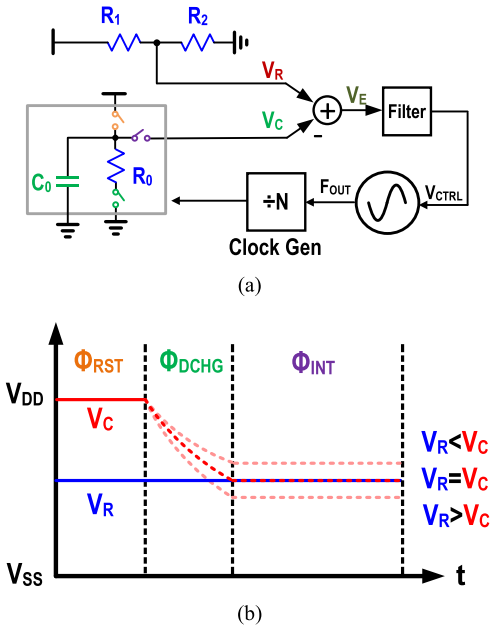


Fig. 2. (a) Simplified schematics of the adopted FLL and (b) its timing diagram.

trim. Although the diffusion version achieves worse inaccuracy (±14 400 ppm) over the same temperature range, its long-term drift (600 ppm), after one week of accelerated aging at 150 °C, is nearly 10× better than that of its poly counterpart.

The rest of this article is organized as follows. Section II discusses the architectural choices, while the circuits' nominal implementation details are briefly discussed in Section III. Measurement results of chips with different resistor combinations are presented in Section IV, and the frequency reference's performance is compared with the state of the art. Finally, conclusions are drawn in Section V.

II. Architecture and Design Considerations

A. FLL

Fig. 1(a) shows the simplified diagram of a traditional *RC* relaxation oscillator. Despite being a simple and compact design, comparator non-idealities, e.g., offset, noise, and delay, severely limit its inaccuracy and jitter. Although techniques have been proposed to address the offset and delay issues [3], [20], the overall inaccuracy of such oscillators is generally limited to ∼5000 ppm over a wide temperature (>100 °C) and supply (>20%) range.

Frequency references based on FLLs can achieve better inaccuracy. One typical structure [21] is shown in Fig. 1(b). The front end is a Wheatstone bridge (WhB), which consists of three resistors, a switched-capacitor resistor (C_0), and a stabilizing capacitor C_{STB}, which filters out the ripple on V_C. The WhB output is integrated and then applied to a VCO, whose output frequency, in turn, controls the equivalent resistance of C_0. At steady state, the large dc gain provided by the integrator will force a zero WhB output on average. Assuming $R_1 = R_2$, the resulting output frequency becomes

$$F_{OUT} \approx \frac{N}{R_0 C_0} \tag{1}$$

where N is the division ratio of the phase generation block.

One drawback of this FLL design is its large chip area. To ensure a stable WhB output and thus high accuracy, a large C_{STB} (typically $>50C_0$) is required. Also, an even larger integration capacitor ($\sim 1000C_0$ in [21]) may be required to ensure that the dominant pole is set by the integrator and to minimize low-frequency noise.

To circumvent the need for large stabilizing/integration capacitors, a sampling-based front end [22] is adopted in this work. As shown in Fig. 2, during the reset phase (Φ_{RST}), C_0 is charged to V_{DD}, while R_0 is disconnected. Then during the discharging phase (Φ_{DCHG}), C_0 is exponentially discharged via resistor R_0, so that its voltage at the end of this phase can be expressed as follows:

$$V_C = V_{DD} \cdot e^{-\frac{T_{DCHG}}{R_0 \cdot C_0}} \tag{2}$$

where T_{DCHG} is the phase duration. Finally, during the integration phase (Φ_{INT}), the error signal V_E, which is the difference between the resistive divider output [$V_R = V_{DD} \cdot R_2/(R_1 + R_2)$] and that of the capacitor (V_C), is integrated and then used to control the VCO frequency. Since V_C will ultimately approach V_R given a large loop gain, the steady-state frequency output can be derived as follows:

$$F_{OUT} = \frac{N}{R_0 C_0 \cdot \ln(1 + R_1/R_2)}. \tag{3}$$

Apart from eliminating the stabilizing capacitor C_{STB}, the circuit is also free from the error introduced by V_C ripple [13], [21].

B. Trimming Strategy

Since integrated resistors and capacitors both spread over process and temperature (>30%), the temperature dependence and the nominal frequency of the frequency reference should

be trimmed. In this work, this is done by simply trimming R_2 and C_0, respectively.

Nominal frequency trimming is achieved by adjusting the value of C_0. To achieve high resolution, a coarse-fine trimming strategy is adopted, which will be elaborated on in Section III-A. Since the TCs of resistors are much larger (thousands of ppm/°C) than that of capacitors (less than 50 ppm/°C), an analog technique for compensating for resistor TC is required.

Conventionally, the analog TC compensation of *RC* oscillators is done by combining resistors with complementary TCs to realize a "zero" TC resistor R_0 [15]. However, some processes do not have resistors with negative TCs. Furthermore, the switches needed to trim R_0 will create trim-code-dependent parasitic capacitances, which will alter the effective *RC* time constant, resulting in extra frequency inaccuracy.

In this work, R_0 and R_1 are fixed resistors made from the same material, while the TC trimming is performed on R_2 (Fig. 3). The resistive divider serves as a minimalist analog temperature sensor, which provides a reference voltage that tracks the temperature characteristics of the *RC* branch. As a result, the parasitic capacitance issue is mitigated. Moreover, the generated V_R is determined by the TC difference of R_1 and R_2 instead of by their absolute TCs. At room temperature (T_0), we assume that the resistance of both R_1 and R_2 is R_{1T0}, and that of R_0 is R_{0T0}. The linear TCs (TC1) of R_1 and R_2 are denoted by TC_{R1} and TC_{R2}, respectively. The resistance expressions of $R_0/R_1/R_2$then become

$$\begin{aligned} R_0(T) &= R_{0,T0} \cdot (1 + \Delta T \cdot \mathrm{TC}_{R1}) \\ R_1(T) &= R_{1,T0} \cdot (1 + \Delta T \cdot \mathrm{TC}_{R1}) \\ R_2(T) &= R_{2,T0} \cdot (1 + \Delta T \cdot \mathrm{TC}_{R2}) \end{aligned} \tag{4}$$

where ΔT is the temperature difference with respect to the room temperature. Equation (3) can then be approximated by applying the Taylor expansion, i.e.,

$$F_{\mathrm{OUT}} = \frac{N}{\tau_0 ln2}\left(1 - \Delta T\left(\left(\ln 2 + \frac{1}{2}\right) \cdot \mathrm{TC}_{R1} - \frac{1}{2}\mathrm{TC}_{R2}\right)\right) \tag{5}$$

where $\tau_0 = R_{0T0}C_0$ is the *RC* time constant at room temperature. To achieve a 1st-order temperature compensation, the relationship between the TCs should be

$$\mathrm{TC}_{R2} = (2\ln 2 + 1) \cdot \mathrm{TC}_{R1} \approx 2.39\mathrm{TC}_{R1} \tag{6}$$

which can be achieved by using resistors with the same TC1 polarity. It should be noted that the approximation above only holds for small resistance variations. Circuit simulations or numerical calculations are required to analyze the temperature characteristics of designs based on high-TC resistors (e.g., diffusion and silicided ones) over a wide temperature range.

In the first prototype chip, R_0 is realized as a p-type polysilicon (p-poly) resistor, since this has the lowest TC (Fig. 4) in the chosen 180-nm technology. R_1 is made from the same material, while R_2 is a series combination of p-type and n-type polysilicon (n-poly) resistors. After compensation,

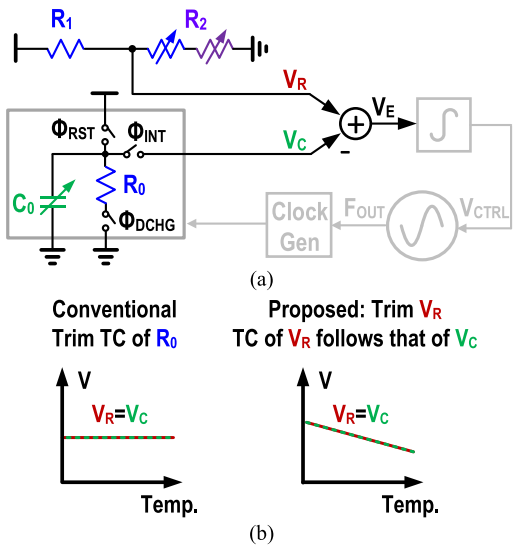


Fig. 3. (a) Trimmed devices. (b) Corresponding characteristics of voltage output signals.

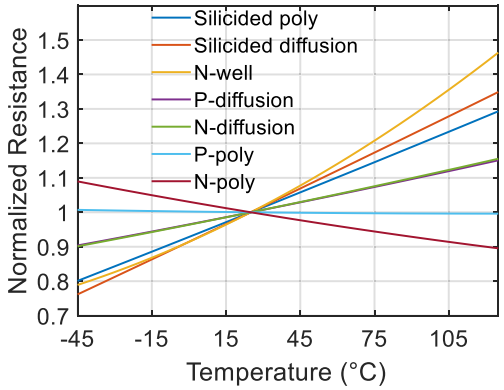


Fig. 4. Temperature characteristics of resistors in the chosen standard 180-nm technology.

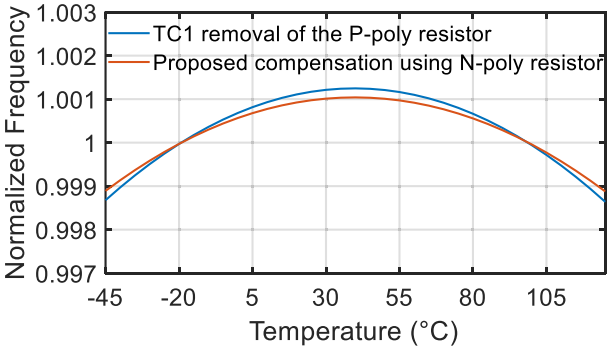


Fig. 5. Simulated frequency error over temperature with different resistors and TC compensation scenarios.

a negative 2nd-order TC (TC2) remains, resulting in a simulated frequency error of $\sim \pm 1100$ ppm over temperature, as shown in Fig. 5. Interestingly, compared with an ideal 1st-order TC compensation, the proposed trimming method introduces a small positive TC2 due to the $1/X$ and logarithmic terms in (3), resulting in slightly less error.

In the second prototype chip, R_0 and R_1 are made from p-diffusion (p-diff) resistors, which have a positive TC1

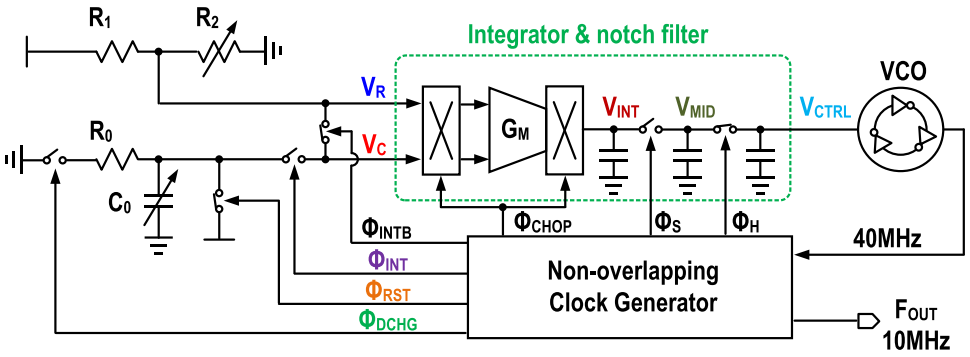


Fig. 6. Simplified circuit diagram of the proposed *RC* frequency reference.

(Fig. 4). Both the silicided diffusion (s-diff) and n-well resistors have a larger positive TC1, and so, in principle, could both be used to realize an R_2 that cancels the TC1 of R_0. However, since n-well resistors have a large minimum width and a large TC spread [23], s-diff resistors were chosen.

III. Circuit Implementation

A simplified circuit diagram of the proposed *RC* frequency reference is shown in Fig. 6. To achieve a good trade-off between chip area and output frequency, the *RC* discharging time is set to 25 ns, corresponding to a 40-MHz internal frequency. A standard 10-MHz output frequency is then generated by a clock divider.

A. Capacitor Trimming

To save area in the chosen 180-nm technology, all the capacitors are implemented as metal–insulation–metal (MIM) capacitors, whose density is about 2.4× larger than that of the available metal–oxide–metal (MOM) capacitors. To achieve high trimming resolution without dramatically increasing the overall capacitor value, a coarse-fine structure [Fig. 7(a)] is adopted. Introducing an offset of 40 fF allows the LSB of the capacitive digital-to-analog converter (DAC) to be set to 10 pF, instead of to a design-rule restricted 40 fF, which corresponds to ∼1% resolution of the coarse trimming capacitor bank (C_C). By connecting the fine-trimming capacitor bank (C_F) in series with a small 50-fF capacitor (C_S), the effect of changes in C_F on C_0 will be down scaled. Simulation results show that the worst-case capacitance trimming resolution is then 0.73 fF, which ensures that the frequency trimming resolution stays below 0.1% over corners [Fig. 7(b)]. To avoid creating a floating node, the junction of C_S and C_F is periodically connected to the virtual ground of the G_m–C integrator.

B. Resistor Trimming

To allow the TC1 and nominal frequency trims to be done orthogonally, the two types of resistors have been scaled to obtain the same nominal resistance per unit length, and then configured as shown in Fig. 8(a). Taking the poly version, for example, the TC1 of the frequency reference can be trimmed from −40 to 40 ppm/°C in 16 steps, which corresponds to a

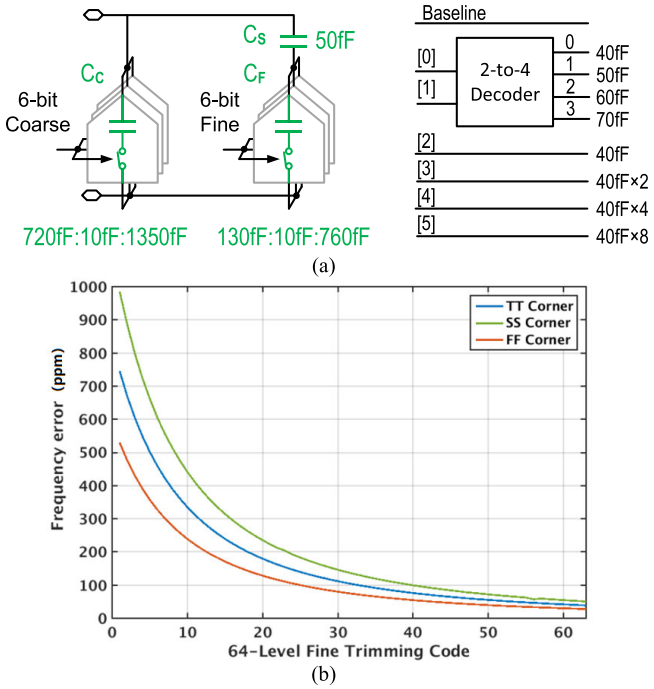


Fig. 7. (a) Coarse-fine capacitor trimming and its implementation. (b) Trimming resolution over corners and fine-trimming codes.

resistor spread of ±20%. Due to the TC contributions from the interface resistance and the contact resistance, the actual TC of the poly resistors is somewhat larger than the simulation results shown in Fig. 5. In this work, R_0 is set to 36 kΩ, while setting $R_1 = R_2 = 100$ kΩ results in an even power split between the *RC* and the resistive divider branches.

C. G_m–C Integrator, Notch Filter, and VCO

To improve the FLL's energy efficiency, Φ_{INT} is 2× longer than Φ_{RST} or Φ_{DCHG} [Fig. 9(b)], such that the signal amplitude of the *RC* front end is enlarged given the same G_m stage noise. To suppress the $1/f$ noise of the G_m stage and improve the oscillator's long-term stability, it is chopped at $F_{VCO}/32$ (1.25 MHz), with the chopping transitions occurring when the integrator is gated ($\Phi_{INT} = 0$). However, the resulting chopper ripple at the VCO input (V_{CTRL}) will increase its output jitter. Increasing the chopping frequency or lowering the G_m/C_{INT} ratio can solve this issue. However, the former leads to more

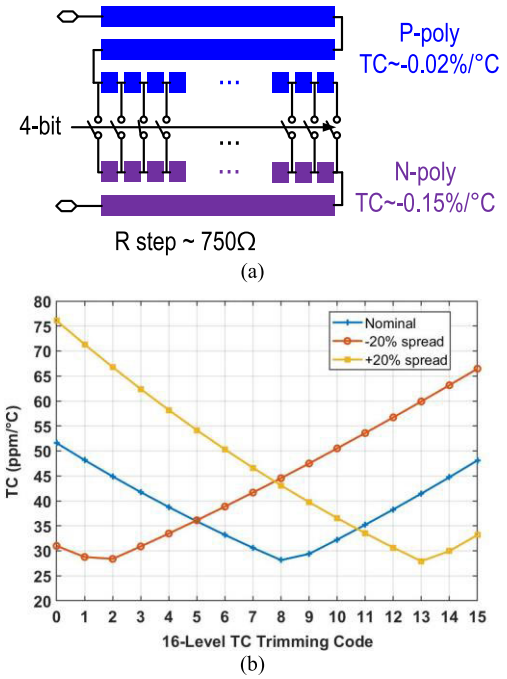


Fig. 8. (a) Implementation of the 4-bit resistor trimming in the first prototype using p-poly/n-poly resistors. (b) Simulated temperature coefficients (TCs) (box method) from −45 °C to 125 °C.

residual offset, and thus worse inaccuracy, while the latter results in a trade-off between jitter performance and capacitor area. In this work, a compact switched-capacitor notch filter is implemented to suppress the chopping ripple without a large C_{INT} (7 pF) [25]. By driving the filter with two capacitors C_{MID} (1.8 pF) and C_{HOLD} (2.7 pF) using CMOS non-overlapping switches, the voltage across C_{INT} is effectively sampled at $F_{VCO}/64$ (625 kHz), resulting in a ripple-free VCO input voltage (V_{CTRL}) and reduced jitter.

Fig. 9(a) shows the schematic of the chopped telescopic G_m. It has an 80-dB dc gain and a nominal transconductance of 5 μS. With self-biased cascodes based on medium-V_{th} (M-vt) transistors, no cascode bias-voltage generation is required, thus saving some chip area/power. The VCO consists of a PMOS current source that drives a three-stage current-starved ring oscillator, whose output is level-shifted to drive the non-overlapping clock generation circuit.

IV. Measurement Results and Discussion

Two prototype chips have been fabricated in a standard 180-nm CMOS technology. The first chip implements 16 identical frequency references based on p-/n-poly resistors (both with negative TCs) [Fig. 10 (top)]. All the transistors and resistors are placed below MIM capacitors for area saving. The second chip implements frequency references based on s-/p-diff resistors (both with positive TCs) [Fig. 10 (bottom)]. To achieve the same nominal resistance using the low-Ohmic silicided resistors and thus enable a fair comparison, the latter reference circuit is somewhat larger (0.0145 mm^2) than the first one (0.01 mm^2). At room temperature, a single frequency reference draws 56.7 μA (27.5-μA analog and 29.2-μA digital) from a 1.5-V supply, and about 2/3 of the digital power is used to drive the output buffer.

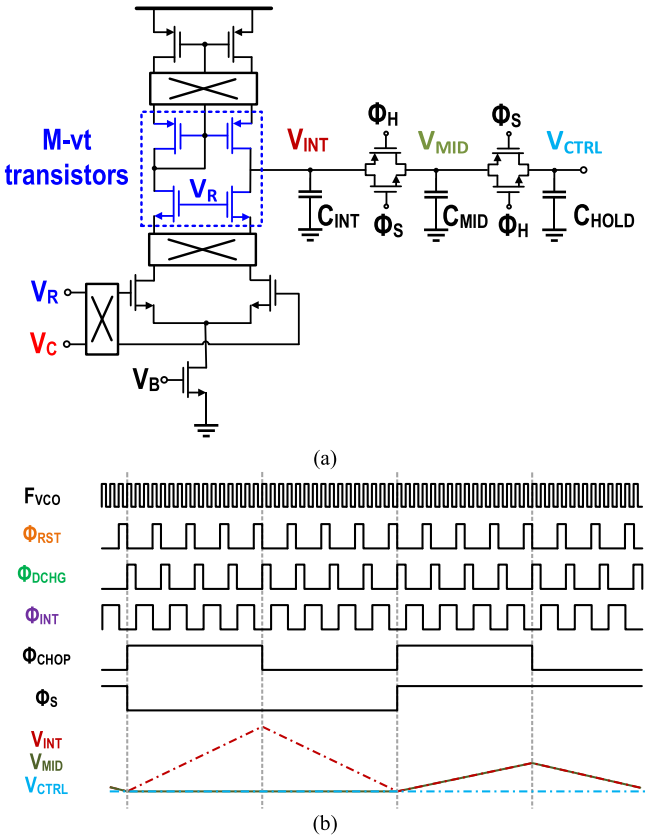


Fig. 9. (a) Implementation of the G_m–C integrator and the notch filter. (b) Timing diagram.

A. Startup and Stability

Although the use of a notch filter introduces an excess delay of roughly eight front-end cycles (∼800 ns at steady state), the dominant pole (∼110 kHz) of the proposed FLL is set by the G_m–C filter ($G_m \approx 5$ μS and $C \approx 7$ pF), resulting in an over 10× frequency margin and well-defined stability. As shown in Fig. 11, after resetting V_{CTRL} to ground, the output frequency settles within about 30 μs. A step-wise settling transient will appear after chopping and notch filtering are enabled, but the settling time remains unchanged.

B. Noise Performance

As shown in Fig. 12, the FLL achieves a closed loop period jitter of 45 ps, which is only slightly worse than the open loop jitter (∼40 ps) determined by the ring VCO and its following level shifter. After disabling the notch filter (fixing $\Phi_S = 1$ and $\Phi_H = 0$), however, the jitter will become significantly larger (∼79 ps). The frequency reference achieves an Allan deviation of 2.3 ppm for a 0.6-s stride, as shown in Fig. 13.

C. Trimming and Temperature Characteristics of the First Prototype

Seven ceramic packaged chips (112 samples) from one wafer were trimmed and then characterized in a temperature-controlled oven. As expected, the resistor TC spread from the same batch turned out to be quite small (±8 ppm/°C), allowing a fixed 4-bit TC trim code (corresponding to the TT corner

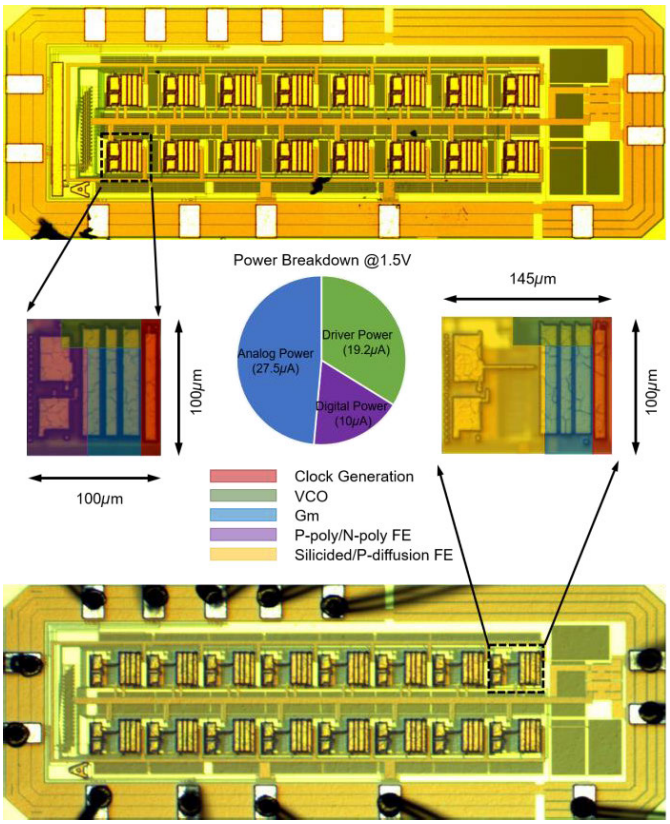


Fig. 10. Chip micrograph and power breakdown of the p-/n-poly based frequency reference (top). Chip micrograph of the second TO with the s-/p-diffusion-based frequency reference (bottom).

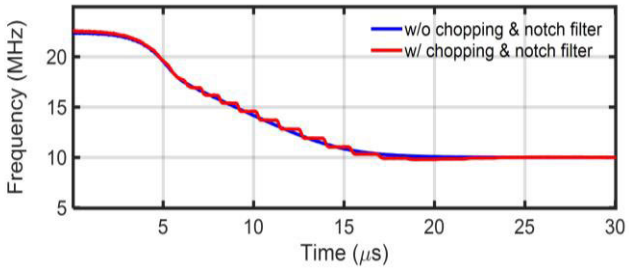


Fig. 11. Transient response after V_{CTRL} reset.

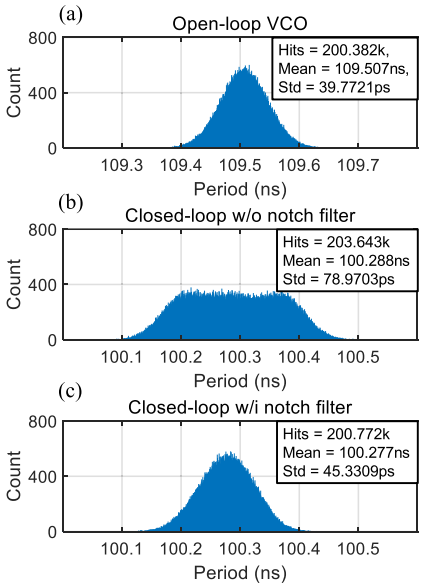


Fig. 12. Jitter performance of the frequency reference under different conditions. (a) Open-loop. (b) Closed-loop, notch filter disabled. (c) Closed-loop, notch filter enabled.

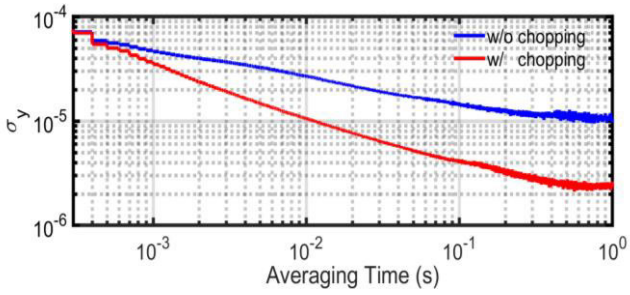


Fig. 13. Allan deviation of the frequency reference.

simulation) to be determined by characterizing one sample over temperature. After this, the nominal frequency spread (±1.9% within the tested batch) was individually trimmed at room temperature (RT, ∼25 °C) by adjusting the 12-bit coarse-fine capacitor bank.

As shown in Fig. 14(a), this first frequency reference prototype achieves an inaccuracy of ±0.28% from −45 °C to 125 °C, resulting in a frequency inaccuracy of ±2800 ppm and a residual TC of 31.5 ppm/°C (box method). Due to the instability of the poly resistors, however, significant hysteresis (worst case 1500 ppm) is observed as the samples are cycled from hot to cold, while the cycle-to-cycle variation is much smaller (±200 ppm).

To investigate the effect of stress, seven chips from the same batch were plastic-packaged and then characterized. Although the nominal frequency spread then becomes about 1.7× larger than that of the ceramic packaged chips, a fixed TC trimming code could still be used, but with a 3-LSB offset compared with the code used for the ceramic packaged chips. A similar frequency inaccuracy of ±3000 ppm was achieved after one-point calibration, as shown in Fig. 14(b), while the master curve and the hysteresis curve only changed slightly.

D. Resistor Aging and Other Prototype

To investigate the effect of resistor aging, an accelerated aging experiment was performed by storing the chips at 150 °C for one week while powered OFF. As shown in Fig. 15, the output of the p-/n-poly prototype then drifted by about 5000 and 2000 ppm when packaged in ceramic and plastic, respectively. The smaller drift of the plastic packaged chips may be due to the effective pre-aging caused by their high-temperature (>180 °C) packaging process. Since the frequency error due to TC drift is still less than that due to TC curvature, it may be concluded that the long-term inaccuracy of the frequency reference can be further improved by periodically trimming its output frequency against an external [27] or internal [18] reference.

In contrast, the diffusion resistor prototypes exhibits much better long-term stability. As shown in Fig. 16, they exhibit greater robustness to aging (600 ppm, almost 10× less than their poly counterparts) at the expense of somewhat more

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART WORKS

Reference	This work			Gurleyuk JSSC 2022	Jiang ISSCC 2021	Khashaba JSSC 2022	Wang TCAS-I 2016	Lee JSSC 2020	Park ISSCC 2023
Technology	0.18µm			0.18µm	0.18µm	65nm	0.18µm	0.18µm	65nm
Resistors	p-poly/ n-poly		p-diff/ silicided diff	p-poly/ silicided poly	p-poly/ silicided poly	p-poly/n-poly/ silicided poly	p-poly/ n-diffusion	Not clear	p-poly/n-poly/ VIA
Area [mm^2]	0.01		0.0145	0.3	0.06	0.18	0.012	0.015	0.22
Frequency [Hz]	10M			16M	16M	32M	12.77M	10.5M	100M
Power [µW]	85 [a]			220	158	34	56.2	219.8	142
Power efficiency [pJ/cycle]	8.5			13.8	9.9	1.1	4.4	21	1.42
Supply range [V]	1.5~1.8			1.6~2	1.6~2	1.1~2.3	0.6~1.1	1.4~2.2	1.1~1.3
Supply sensitivity [ppm/V]	3500		XXX	1200	2000	80 [d]	10000	44000	1400
Jitter [ppm]	414			638	196	713	983	104	510
Allan deviation [ppm]	2.3			0.32	0.35	2.5	-	2.8	8.1
Temp. range [°C]	-45~125			−45~85	−45~85	−40~85	−30~120	-45~125	-40~85
Packaging	Ceramic	Plastic	Ceramic	Ceramic	Ceramic	Plastic	-	-	Plastic
Max. Freq. error [ppm]	±2800	±3500	±14400	±90	±400	±400	±9000 [b]	-	±760
Temp. coefficient [ppm/°C]	31.5 [c]	35.3 [c]	169.2 [c]	1.3 [c]	6 [c]	8.4	31	137	12.2
Trimming points	1+batch			2+batch	1+batch	2	1	0	2
Number of samples	112			20	18	6	4	15	11
Max. aging error [ppm] [e]	5000	2000	600	-	-	-	-	-	410 [f]

[a] Including driver [b] Estimated from inaccuracy plots [c] Box method [d] LDO used [e] 150°C for 1 week [f] 125°C for 3 weeks, with compensation

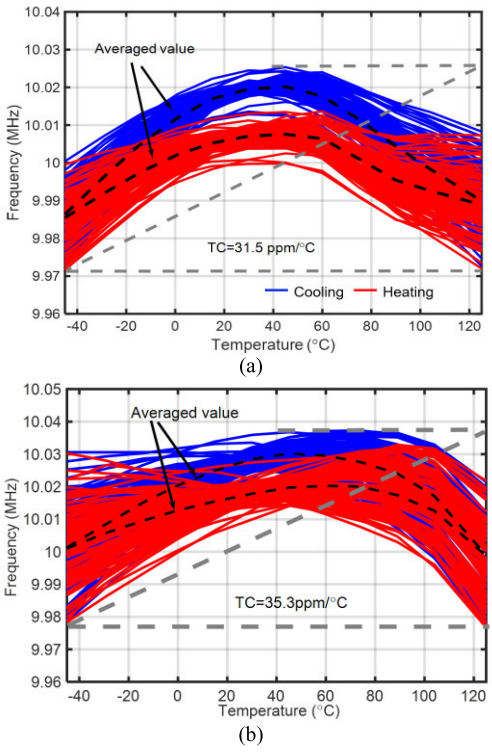


Fig. 14. Temperature sensitivity and hysteresis of the p-/n-poly frequency reference after a one-point calibration at RT of (a) ceramic packaged chips and (b) plastic packaged chips.

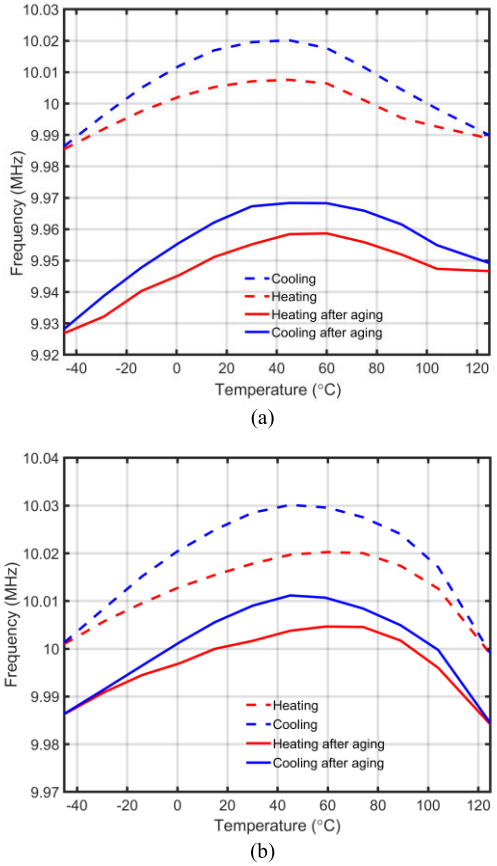
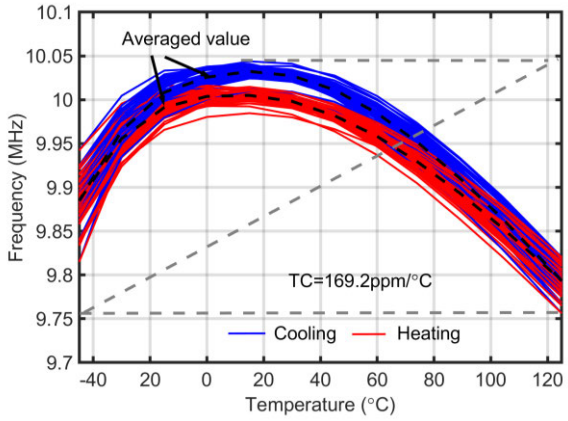


Fig. 15. Aging effect of the p-/n-poly frequency reference with (a) ceramic and (b) plastic packaging.

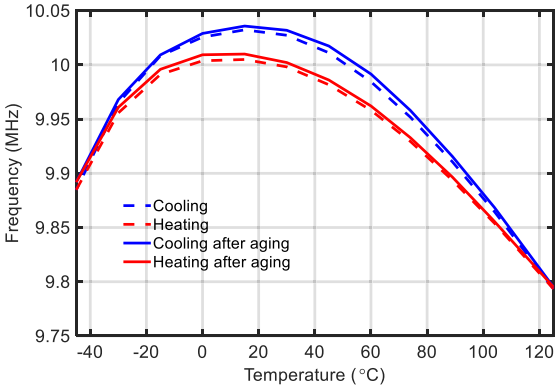
hysteresis (3000 ppm), a larger TC2, and thus worse inaccuracy (∼14 400 ppm). Compared with the simulation results [Fig. 5(b)], the degraded inaccuracy is probably due to the use of near-minimum-width resistors, whose temperature dependency then differs somewhat from the nominal model. This discrepancy also meant that the implemented TC1 trim did not have enough correction range.

E. Comparison to Previous Work

Table I summarizes the performance summary of the proposed *RC* frequency references, and compares them with the



(a)



(b)

Fig. 16. Characteristics of ceramic packaged *RC* frequency reference based on s-/p-diff resistors (a) frequency error after a one-point calibration and (b) aging effect.

state of the art. Despite being implemented in a relatively mature 0.18-μm technology, the p-/n-poly prototype achieves the best absolute inaccuracy among compact ($\sim$0.01 mm^2) frequency reference designs after a one-point calibration. In addition, the effect of packaging stress and aging of different types of resistors has been characterized.

V. Conclusion

This article presents a compact CMOS *RC* frequency reference with on-chip calibration. It employs an FLL, in which a resistive divider generates a temperature-compensating reference voltage for a switched *RC* branch, whose discharging time, in turn, determines the period of a VCO. The resistive divider can be implemented with resistors with TCs of the same polarity, making it suitable for use in most CMOS processes. Implemented in a standard 180-nm technology and using p-/n-polysilicon resistors, both with a positive TC, a prototype frequency reference occupies only 0.01 mm^2 and achieves an absolute inaccuracy of $\pm$2800 ppm from -45 °C to 125 °C after a fixed TC trim and a one-point frequency trim. After one week of accelerated aging at 150 °C, however, the prototype exhibited significant drift (5000 ppm). Under the same conditions, a prototype based on silicided/p-diffusion resistors exhibited much less drift (600 ppm), at the expense of worse inaccuracy, mainly due to a larger 2nd-order nonlinearity. Overall, this article presents a promising architecture for the realization of compact and stable *RC* frequency references in a wide variety of CMOS processes.

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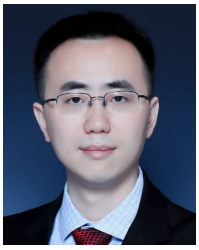

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