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23.2 A 40A Shunt-Based Current Sensor with ±0.2% Gain Error from -40°C to 125°C and Self-Calibration

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Low-cost metal (e.g., PCB trace) shunts can be used to make accurate current sensors (<1% gain error) [1-3]. However, their reported maximum operating temperature (85°C) is not high enough for automotive applications, and at higher temperatures, shunt resistance may exhibit increased drift, especially at high current levels. This paper presents a metal-shunt-based current sensor with a wide temperature range and a stable on-chip reference current (I_{REF}) source for shunt self-calibration. By employing a continuous-time (CT) front-end, it achieves an input noise density of 14nV/√Hz while consuming only 280μA, making it >10× more energy efficient than prior art [1,2], with comparable gain error (±0.2%) over a wider current (±40A) and temperature (-40°C to 125°C) range.

The proposed sensor employs an ADC to digitize the IR drop V_S across a copper shunt resistor R_S (Fig. 23.2.1), whose large temperature coefficient (TC, ~0.4%/°C) is compensated by using a near-PTAT ADC reference ($V_{REF}=V_{PTAT}+V_{CTAT}/\lambda$). By tuning λ, the TC of V_{REF} can be matched to that of the shunt [1,2], generating a temperature-independent digital output (I_S-mode). However, R_S may still drift over time [4]. In this work, by briefly disconnecting the shunt from the input current I_S, R_S can be calibrated with a known I_{REF} (I_{REF}-mode). Since R_S is quite small (<1mΩ), and I_{REF} is practically limited to a few tens of mA, a low-noise ADC is needed to achieve the required sub-μΩ resolution in a reasonable measurement time (seconds). ADC offset and I_{REF} drift will also cause residual errors. The former is mitigated by digital correlated-double-sampling (CDS). The latter requires a time and temperature stable I_{REF}, whose residual TC can be compensated by digitizing the ratio V_{CTAT}/V_{PTAT} to determine die temperature (T_{DIE}, T-mode).

Figure 23.2.2 shows the block diagram of the proposed current sensor. It consists of a 1-bit 2nd-order ΔΣ modulator with a sampling frequency (f_s) of 5.12MHz. The 1st stage is based on a CT capacitively-coupled Gm-C integrator, which blocks the input common-mode voltage and avoids the kT/C noise limitations of the switched-capacitor (SC) integrators used in [1,2]. However, Gm-C integrators typically suffer from poor linearity, which either requires the use of source degeneration or complex multi-bit DACs to reduce their input swing. In this work, since the maximum shunt voltage V_S and the required V_{REF} are quite small (~±50mV at room temperature, RT), the use of a simple 4-tap FIR-DAC is enough to reduce the input swing to less than 30mV over temperature, which is well within the linear range of a tail-resistor-linearized (TRL) current-reuse OTA [5] (Fig. 23.2.2 bottom-left). To allow its NMOS and PMOS input pairs to be independently biased, the input and feedback capacitors are split into two banks, which couple V_S and the FIR-DAC outputs, respectively, to both pairs. However, DAC transitions will then be coupled directly to the input pairs, overloading the OTA and causing quantization-noise (Q-noise) folding. To mitigate this, dead-band (DB) switches briefly (~25ns) isolate the OTA from the integration capacitor C_{INT} (40pF) during DAC transitions. Since its kT/C noise is suppressed by the gain (~70dB) of the CT 1st integrator, the 2nd stage is built around an SC integrator with a sampling capacitor of 50fF. As in [5], it also serves as the summing node of the feedforward and FIR-DAC compensation paths.

To sense DC inputs, the capacitively-coupled TRL OTA must be chopped. However, this also creates a gain notch at the chopping frequency f_{ch}. Since the 4-tap FIR-DAC creates notches at multiples of $f_s/4$, the TRL OTA can be chopped at $f_s/4$ without degrading the modulator's noise-transfer function. Switched resistors are used to realize the large DC bias resistances (~40MΩ) needed to ensure the highpass cut-off frequency (~1kHz) of the input network to well below f_{ch} (CHH=1.28MHz). To further mitigate offset and 1/*f* noise, low-frequency chopping (CHL=20kHz) is applied to both integrators.

As in [1-3], a tunable PTAT V_{REF} can be generated by diode-connected NPNs that provide ΔV_{BE} (V_{PTAT}) and V_{BE} (V_{CTAT}). However, due to their finite current gain β (~20), the base current of the NPNs will degrade the linearity of ΔV_{BE} over temperature. In [6], this error is mitigated by using a source follower (SF) to supply the base current. Its output impedance must then be low enough to ensure rapid settling after the DAC transients, which would otherwise cause DAC non-linearity and Q-noise folding. This work employs a flipped voltage follower (FVF), whose output impedance is reduced by a factor ($gm_2 \bullet ro_1$) compared to that of an SF [6] (Fig. 23.2.3 top-left). To improve the pull-up capability of the higher V_{BE} (V_{BEH}), an extra SF M_3 is added in parallel to achieve a Class-AB output. These measures reduce the settling time of V_{REF} transients to less than 25ns (13% of a sampling period) over PVT, allowing them to be blocked by the DB switches.

Since the TC of a copper shunt is nearly PTAT, the tuning factor λ needs to be quite large (|λ|>90) to cover the target TC tuning range (0.33±0.1%/°C). Thanks to the low output impedance of the FVF, part of this attenuation (<1/7) can be realized by a resistive divider (Fig. 23.2.3 top-right). The rest (1/14) is then realized by the CDAC ($C_{PTAT}=14C_{CTAT}=C_{IN}=4$pF, in Fig. 23.2.2). To achieve a step of <10ppm/°C, V_{CTAT}/λ should be tuned with 7-bit resolution. By taking advantage of the differential nature of the CDAC, this is achieved by combining a 4-bit coarse trim of V_{CTATP} and a 3-bit fine trim of V_{CTATN} with the resistive dividers.

To monitor R_S drift, I_{REF} is generated by forcing ΔV_{BE} (~54mV at RT) across a silicided diffusion resistor R_0 (~16kΩ) (Fig. 23.2.3 bottom). ΔV_{BE} and R_0 are both stable and have similar TCs (~0.3%/°C) [5], which are cancelled in the generated current. The residual TC (~60ppm/°C) can then be digitally compensated by sensing T_{DIE} in T-mode. Compared to the bandgap and SC-resistor-based I_{REF} generator used in [4], this approach avoids the need for an external zero-TC clock. As in [4], the resulting current is amplified by a current mirror (6×, ~20μA), and then boosted by an on-chip current driver with a programmable gain (from 500 to 2000). To mitigate errors due to transistor mismatch, chopping (at 625Hz) and DEM (at 1.25kHz) are applied to the amplifiers (A_1 and A_2) and current mirrors.

In T-mode, a fixed CTAT input ($V_{BE}/28$) is applied to the modulator by using half of C_{CTAT}, while the input capacitor C_{IN} is shorted by the shunt. Then the bitstream average will be proportional to $X=V_{BE}/\Delta V_{BE}$, which is a well-defined function of temperature. Due to the small residual TC of I_{REF}, an inaccuracy of 1°C is acceptable, which can be achieved even with the expected mismatch (~1%) of C_{PTAT} and C_{CTAT}, and the required conversion time (tens of μs) is negligible compared to that required in I_{REF}-mode (seconds).

The sensor is implemented in a 0.18μm CMOS process and occupies 0.38mm² (Fig. 23.2.7, top). The modulator and the V_{REF} generator draw 280μA from a 1.8V supply, while the I_{REF} generator can output currents ranging from 11mA to 45mA. Its performance was verified with a 0.83mΩ PCB trace shunt (Fig. 23.2.7, bottom). Good thermal coupling and galvanic isolation were achieved by bonding the chip to the shunt with non-conductive glue.

Figure 23.2.4 (top) shows the measured output spectra of the modulator. With DB disabled, its noise floor is limited to 23nV/√Hz by Q-noise folding, which improves to 14nV/√Hz after the DB is enabled. This results in a current-sensing resolution of 1.7mA_{rms} in a 10kHz bandwidth. In I_{REF}-mode, with CHL enabled, the noise floor is flat down to 10mHz (Fig. 23.2.4 bottom), which is limited by ambient temperature drift and residual 1/f noise. This can be further suppressed by applying digital CDS to pairs of short (e.g., 128ms) I_{REF} measurements (45mA and 11mA). Then it achieves a resolution of ~9nVrms in 5s, which corresponds to a gain error of less than 0.1% (3σ). Measurements on 10 samples show that the ADC's offset is less than 35μV without CHL and is below 4μV with CHL.

The sensor was characterized in a current range of ±40A from -40°C to 125°C. Figure 23.2.5 (left) shows the measured gain accuracy over temperature. With an optimal, but fixed, λ (~-200) obtained by batch calibration, it achieves a maximum gain error of ±0.2% after a single-current gain trim (at RT and 10A). Figure 23.2.5 (right) shows the measured I_{REF} from -40°C to 125°C. Its absolute value varies by ±3% due to resistor spread. After a 1-point correlated trim [5], both the nominal value and TC spread can be mitigated, resulting in a normalized spread of ±0.15% from -40°C to 125°C after digital TC compensation. To verify the stability of I_{REF}, 10 samples were subjected to accelerated aging at 150°C for one week. The resulting drift is less than 0.1% around RT, and less than 0.15% over temperature, allowing a gain error of <0.3% for current sensing with shunt-drift calibration.

The performance of the sensor is summarized and compared with the state-of-the-art in Fig. 23.2.6. Compared to prior metal-shunt-based sensors [1-3], it achieves the highest energy efficiency (+11dB) and a competitive gain error (±0.2%) over a wider current (±40A) and temperature (-40°C to 125°C) range. The proposed self-calibration scheme allows a gain error of 0.3% to be maintained even in the presence of shunt resistance drift.

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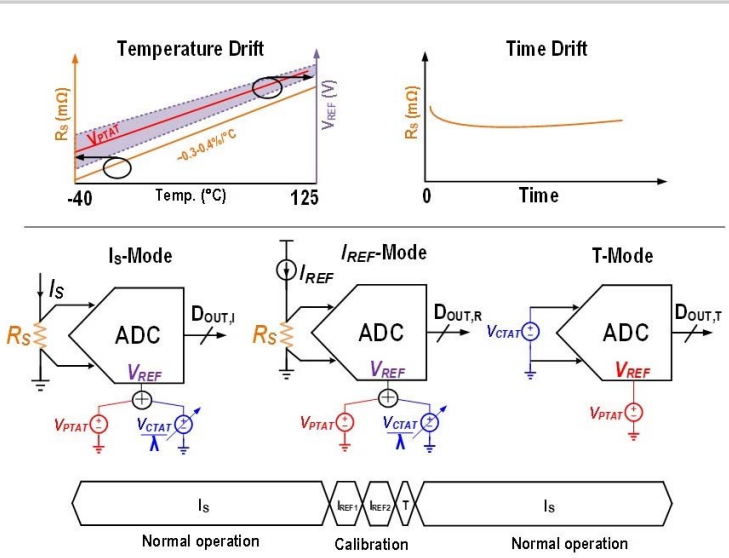

Figure 23.2.1: A versatile readout for low-cost metal-shunt-based current sensor with temperature and aging compensation.

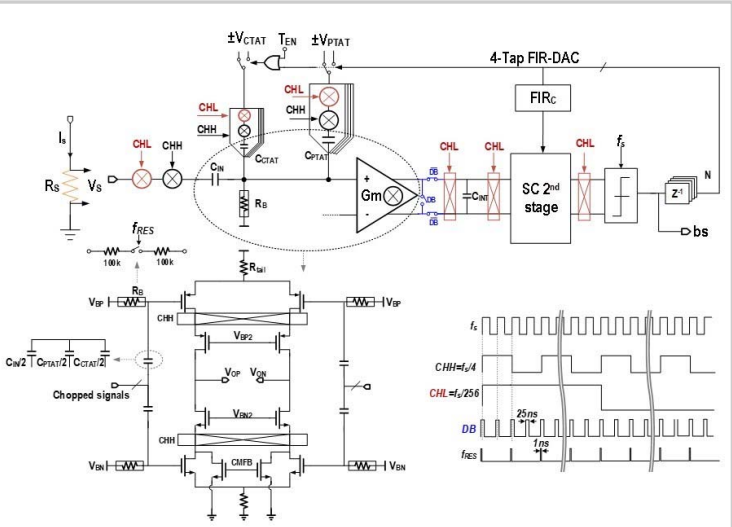

Figure 23.2.2: Simplified circuit diagram of the Gm-C-based ΔΣ modulator (top); The capacitively-coupled tail-resistor-linearized OTA (bottom-left); its timing diagram (bottom-right).

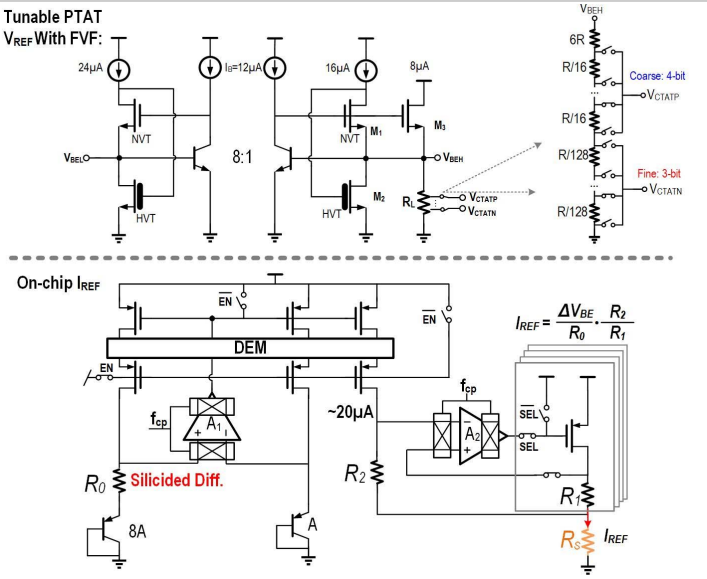

Figure 23.2.3: Simplified circuit diagram of the proposed tunable PTAT V_{REF} with FVF (top) and the on-chip current source (bottom).

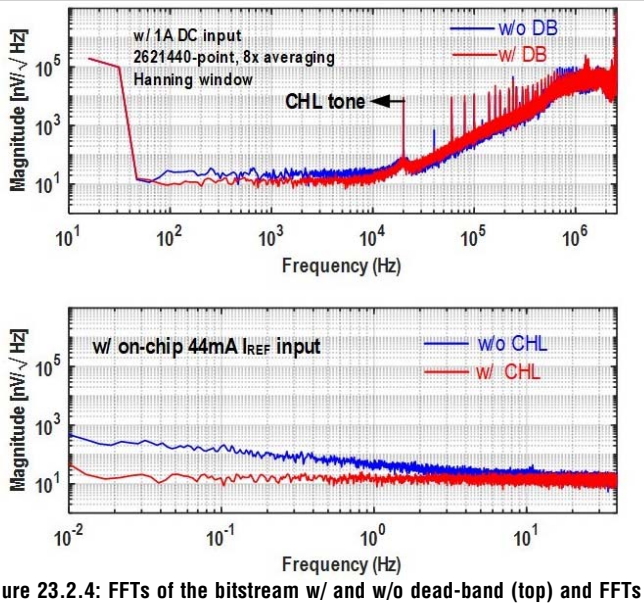

Figure 23.2.4: FFTs of the bitstream w/ and w/o dead-band (top) and FFTs of the decimated results in I_{REF}-mode w/ and w/o CHL (bottom).

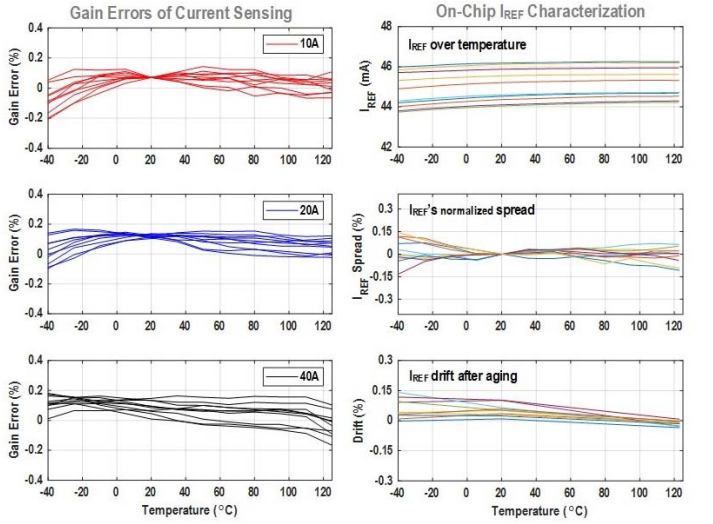

Figure 23.2.5: Gain errors of current sensing over temperature (left); I_{REF} over temperature (top-right); its spread after a 1-point correlated trim and TC compensation (middle-right) and the drift after accelerated aging at 150°C for one week (bottom-right).

	This work	Tang ISSCC'22 [1]	Zamparette VLSI' 21 [2]	Xu SSCL' 18 [3]	Danesh JSSC'19 [4]	INA236 [7]
Tech. (μm)	0.18	0.18	0.18	0.18 BCD	0.18	-
Area (mm²)	0.38	0.36	-	1.4	-	-
Shunt	0.83mΩ (PCB)	1.6mΩ (PCB)	3mΩ (PCB)	1mΩ (PCB)	0.14mΩ (low-TC)	- (low-TC)
I Range	±40A	±25A	±15A	±12A	±100 A	-
Gain Error	±0.2%	±0.25%	±0.6%	±0.35%	±0.1%	~±0.1% (ADC only)
Temp. Range	-40 to 125°C	-40 to 85°C	-40 to 85°C	-40 to 85°C	-40 to 85°C	-40 to 125°C
ADC Offset	<4μV	6μV	0.5μV	1μV	-	<5μV
Noise Density	14nV/√Hz	85nV/√Hz	955nV/√Hz	174nV/√Hz	7.8nV/√Hz	~300nV√Hz
Resolution and BW	1.7mA@10kHz	5.3mA@10kHz	1.8mA@32Hz	1.1mA@40Hz	-	-
Supply Voltage	1.8V	1.8V	1.8V	1.8V	3.3/1.8V	2.7-5.5V
Supply Current	280μA (ADC+V_{REF})	265μA (ADC+V_{REF})	1.4μA (ADC+V_{REF})	13.8μA (ADC+V_{REF})	1700μA (LNA+ADC)	300μA
Dynamic Range	87dB	73.5dB	78.4 dB	80.7dB	-	-
FoM$_1$*	160dB	147dB	149dB	143dB	-	-
FoM$_2$** (nV²/Hz·mA)	54.9	1915	1277	417.8	103.4***	27000
Shunt measurement (I_{REF} spread/drift)	Yes (0.15%/0.15%)	No	No	No	Yes (0.15%/-)	No

* FoM$_1$=Dynamic Range +10log (Bandwidth/Power), from [1]
**FoM$_2$=Noise Density² × Supply current, from [4]
*** Excluding V_{REF} generator

Figure 23.2.6: Performance summary and comparison with the state-of-the-art.

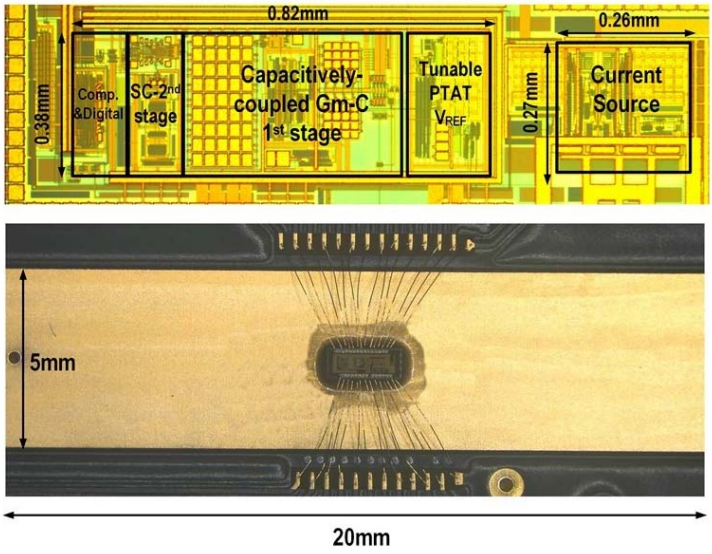

Figure 23.2.7: Die micrograph (top); chip on a PCB shunt (bottom).

Additional References:

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