Modelling and Analysis of the Single-Phase Operation of the Belgian PFC Rectifier

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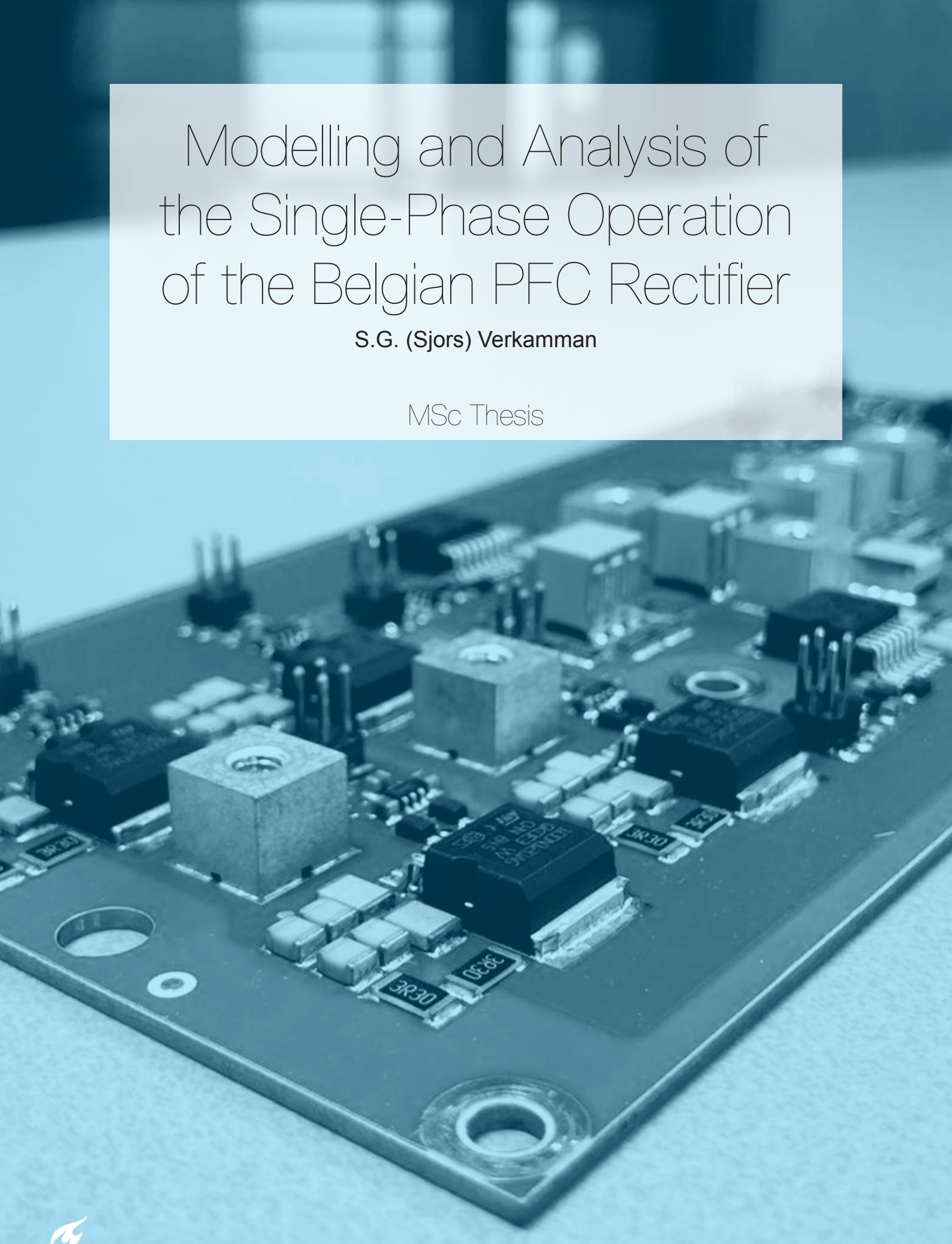
MSc Thesis



TU Delft

PRODRIVE TECHNOLOGIES

Modelling and Analysis of the Single-Phase Operation of the Belgian PFC Rectifier

by

Sjors Verkamman

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Wednesday October 7, 2020 at 11:00 AM.

Student number:	4294815			
Project duration:	December 16, 2019 – October 7, 2020			
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This thesis is confidential and cannot be made public until October 7, 2022.

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Abstract

Boost-type power factor correction (PFC) rectifiers can be used in, for example, battery charging systems for Electric Vehicles (EVs). Conventionally available three-phase PFC rectifiers are limited to output 1/3 of the rated power when connected to a single-phase mains. This work presents the research into the single-phase operation of the Belgian rectifier, a novel boost-type PFC rectifier which allows for full power operation in both single- and three-phase operation (relevant for the three-wire split-phase systems in the USA with a maximum power of 19.2 kW). The single-phase AC-to-DC power converter is operated by paralleling and interleaving the three-phase rectifier bridge legs. By using the analysed triangular current mode (TCM) modulation scheme complete zero-voltage switching is achieved over the entire mains period. The power converter is further analysed with respect to the steady-state operation and component-level modelling. The modelling techniques are used to generate the Pareto-front of efficiency versus power density. The optimal design is selected based on the multi-objective requirements, and is a design with 6× interleaving with a boost inductance of 30 µH that results in complete soft-switching transitions and achieves an efficiency of 98.42 % with a power density of 5.34 kW/dm^3. After that, the single-phase Belgian rectifier is compared to the conventional six-switch boost PFC rectifier to identify and quantify the benefits. Finally, a closed-loop control model is proposed and implemented on the 19.2 kW, 1.5 kW/dm^3 hardware demonstrator for the conversion of a 240 V AC input with a maximum rms current of 80 A into a 380 V DC output to verify the single-phase operation of the Belgian PFC rectifier. Experimental results show efficiencies higher than 98 % for power levels larger than 3 kW.

Acknowledgement

In December 2019 I started my master thesis project at Prodrive Technologies with the expectations to be working the entire project in Eindhoven. However, from March 2020 Covid-19 forced us all to work from home generating a totally different work environment to which I had to adapt. Tackling problems was not as easy as before, and personal meetings changed to online meetings. I would like to thank Prodrive Technologies for allowing me to do my laboratory tests in the last months of the project while considering social distancing. The continuing support from the people around me has helped me to get to the conclusion of this research. Therefore, I could like to thank a few people.

First of all, I would like to thank my supervisor of Delft University of Technology, Prof. Bauer, for supporting me throughout the project and allowing doing this project at a company. Secondly, I would like to express my sincerest gratitude to my supervisor at Prodrive Technologies, Jordi Everts, for all his valuable guidance, knowledge, support, and enthusiasm throughout my project.

Additionally, I would like to thank Thomas Gerrits, Nikolay Mihaylov, Noud Slaats, Bas van de Ven for helping me whenever I was stuck with my models, simulations, software, or hardware demonstrator testing.

Finally, I would like to thank my family and friends for all the support during my studies and for allowing me to follow my dreams.

Sjors Verkamman
Rotterdam, September 2020

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1 Introduction

The global adoption of Electric Vehicles (EVs), including Plug-in Hybrid Electric Vehicles (PHEVs) and full Battery Electric Vehicles (BEVs), increased over the last decade. In 2019, electric cars[1] sales reached a global peak of 2.1 million, 40% higher than 2018, making 2019 the new record year. The global stock of electric cars is now calculated to be 7.2 million. Increase of the EV sales is supported by environmental, health, and societal benefits [1] such as noise reduction and reduction of green house gas (GHG) emissions when the electricity is produced using a low-carbon electricity industry.

Even though the sales reached a peak in 2019 it is not even close to the goal of the EV30@30 campaign, which launched to accelerate the deployment of EVs. The goal for all EV30 members is to reach an electric car market share of 30% by the year of 2030. A good charging infrastructure is key to enable the electric mobility transition [2]. Following the increase of market shares of the EVs, electricity use is forcasted to increase by 50%, of which 4% is accounted by EVs to the global annual electricity demand (up from 0.3% today) [1]. A large part of the electricity will be converted by power electronic systems, such as electric vehicle chargers. The efficiency of a power electronic converter becomes important when the generation efficiency growth stays behind [3].

The DC batteries from EVs are charged from an AC mains grid. This requires the power converters to be AC-to-DC converters. The easiest way to charge the EV battery is by using the on-board charger, an isolated AC-to-DC charger. The on-board charger is usually power limited because of weight and space restrictions [2]. The other option is to charge the EV battery with an off-board (AC-to-)DC charger, which usually allows for higher power, faster, charging and is less restricted by size and weight. An illustration showing the difference between on- and off-board chargers is depicted in Figure 1.1.

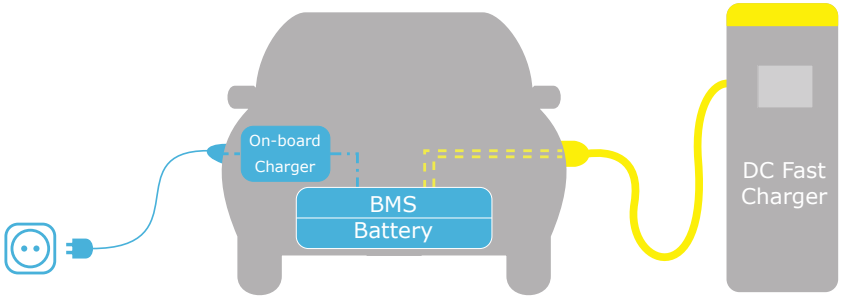

Figure 1.1: Illustration showing the difference between on- and off-board charging.

[1] 'Electric cars' refers to battery electric vehicles including plug-in hybrid electric vehicles in the light-duty vehicle segment. Hybrid electric vehicles that are not able to be plugged-in are excluded.

A typical block diagram of a battery charger is shown in Figure 1.2. The EMI filter is placed at the input of the AC-to-DC converter to reduce the high-frequency electric noise that may cause interference with other devices. Then the rectifier stage with power factor correcting (PFC) stage is visible to rectify the AC voltage and provide the correct grid power quality to comply with regulatory standards i.e. power factor (PF) and total harmonic distortion (THD). The isolated DC-to-DC converter placed after the PFC stage charges the EV battery at the correct voltage and current levels. The rectifier and PFC stage can be combined into a single active converter called a PFC rectifier, this allows for a more compact design.

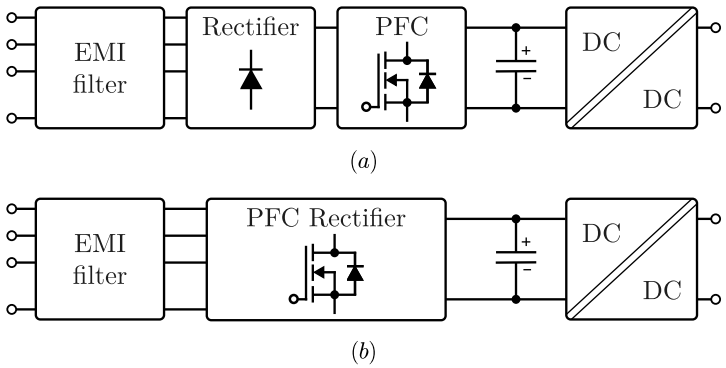

Figure 1.2: Typical block diagram of a battery charger consisting of (*a*) an EMI filter, rectifier stage, PFC stage and an isolated DC-to-DC converter. (*b*) The combined PFC and rectifier stage into a PFC rectifier.

The market for electric vehicle chargers is a global market. This means that these products can be used worldwide, and have to cope with different electricity grids. An example of such a difference is the single-phase 240 V/80 A mains (three-wire split-phase in the USA) with a maximum power of 19.2 kW compared to the three-phase 400 V/32 A mains with a maximum power of 22 kW (in Europe). EV-charger manufacturers would benefit from a universal front-end product with similar performance without having to over-dimension for the single-phase mains connection.

The main problem why this research is done is because a conventional three-phase battery charger can charge with only 1/3 of its rated power when connected to a single-phase or split-phase mains, resulting in the need to over-dimension the power stage. This research introduces, analyses and comparatively evaluates (as detailed further in section 1.1) a novel PFC rectifier topology, named the Belgian Rectifier, that allows for charging at rated power in case of a three-phase (400 V/32 A Europe) mains supply and comparable power with a single-phase (240 V/80 A USA/Japan) mains supply without having to over dimension for the single-phase operation.

1.1. Research Objectives

The *first* objective of this research is to proof that the Belgian PFC (BePFC) rectifier, which was invented to be used as a three-phase rectifier, is capable to operate in single-phase at a similar nominal power level with comparable component stress as in three-phase operation and thus without the need for over-dimensioning the power stage. This first objective is subdivided into three sub-objectives:

- *Mathematically describe and understand the operation principle of the single-phase BePFC rectifier and derive a suitable modulation scheme which facilitates low component stresses.*
- *Develop a controller, with converter simulation included, to verify the dynamic behaviour and operation principle of the single-phase BePFC rectifier.*
- *Model and design a* 19.2 kW *BePFC rectifier hardware demonstrator, that is used for the proof-of-concept of the BePFC rectifier.*

The *second* objective is to identify and quantify the benefits, in terms of efficiency and power density, compared to the conventional approach (in particular the Six-Switch Boost PFC rectifier) which yields significantly higher component stress in single-phase operation, thus leading to a need for over-dimensioning the system. This second objective is subdivided into two sub-objectives:

– *Model and (virtually) optimal design a 22* kW *Belgian PFC rectifier that is able to operate connected connected to a three-phase* 400 V 32 A *European and a split-phase* 240 V 80 A *USA grid.*

– *Comparatively evaluate the single-phase operated BePFC rectifier to a Six-switch boost PFC rectifier which must support multi-mode operation (i.e. three-phase, single-phase and split-phase).*

The rectifier is designed using the requirements listed in Table 1.1. The starting point for the optimal design and comparative evaluation is a three-phase system which is then tailored for single-phase operation. In other words, the designed and compared converter needs to be capable of covering both operating modes in order to make the comparison fair.

Table 1.1: Design requirements for the single-phase operation of the Belgian PFC rectifier.

Description	**Parameter**	**Value**
Single-phase mains voltage	$v_{s,\text{rms}}$	240 V
Single-phase mains current	$i_{s,\text{rms}}$	80 A
Mains frequency	f_s	60 Hz
Output voltage range	v_{out}	350 − 420 V
Nominal output voltage	$v_{out,nom}$	380 V
Output power	P_o	19.2 kW
Nominal full load eficiency	$\eta_{100\%}$	>98%
Power density	ρ_P	>5kW/L

Additional requirement:
- CISPR 22 Class A EMC standards

1.2. Research Methodology

The research into the single-phase operation of the BePFC rectifier is done using converter simulations in MATLAB. These simulations are based on analytical converter models, consisting of steady-state average models, Fourier-analysis models and component-specific models (e.g. loss and volume models). These models contribute to the overall system performance model. The modelling of the converter will be verified with time-domain simulations in Simulink/PLECS and verified by a hardware proof of concept.

With accurate and valid simulation models, an optimal virtual design can be generated without the need for hardware prototype iterations. This only holds if the models are close to reality. Therefore, the hardware demonstration that will be included in this research, is aimed at validating the simulation models and single-phase operation of the BePFC. Comparative evaluations of the BePFC rectifier with the Six-switch boost rectifier are done using the same modelling platform.

1.3. Thesis Outline

This thesis is divided into nine chapters:

The *first* chapter is an introduction to the main problem why this research is done into the single-phase operation of the BePFC rectifier. The objectives and methodology used in this research are also presented.

The *second* chapter presents a literature review on relevant topics to mains connected boost PFC rectifiers and the modelling of these converters. The power mismatch between three- and single-phase PFC rectifiers is explained, as well as the zero-voltage switching principle and power converter modelling procedure.

The *third* chapter introduces the Belgian PFC rectifier and the single-phase operation principle including the triangular current mode modulation scheme.

The *fourth* chapter elaborates on the converter component modelling, such as Fourier modelling, semiconductor modelling, inductor modelling and EMI modelling. The modelling routing is introduced and forms the basis of the design optimization.

The *fifth* chapter is dedicated to the closed-loop control structure of the Belgian rectifier. The interleaved control with variable switching frequency is explained together with the switch sequencing with each zero-crossing of the supply voltage.

The *sixth* chapter is about the design optimization of the single-phase Belgian rectifier. The proposed modelling techniques and virtual prototyping routine is used to generate the Pareto-front of power density versus efficiency. The optimal design is chosen based on multi-objective requirements.

The *seventh* chapter is a comparative evaluation of the single-phase Belgian rectifier and the six-switch rectifier that allows full power operation in single-phase. Both converters are compared on the semiconductor stresses, semiconductor losses and normalized required attenuation.

The *eight* chapter is dedicated to the design and experimental results of the BePFC rectifier hardware demonstrator.

The *ninth* chapter is the conclusion of this thesis with recommendations and ideas for future research.

2

Literature Review

This chapter presents a literature review on topics relevant to the research into the single-phase operation of a three-phase boost-type PFC rectifier, such as the principle of zero-voltage switching and the modelling of power converters. This research is focused on EV battery chargers. Power electronic supplies of high-power AC-mains-connected DC-electrical systems usually consist of two stages, i.e., an AC-to-DC PFC rectifier followed by an isolated DC-to-DC converter [4]. This research focusses on the AC-to-DC PFC rectifier stage of the charging system as was depicted in Figure 1.2.

2.1. The Basics of a Boost PFC Rectifier

The PFC rectifier is an active power converter that does the rectification of the AC grid voltage, power factor correction of the input currents and control of the DC output voltage. The behaviour of the power converter is defined by the power factor λ, the displacement angle ϕ_1 between the fundamental component of the voltage and current, and the total harmonic distortion (THD) of the input AC current [4]. These behavioural characteristics are related by

$$\lambda = \frac{1}{\sqrt{1+\text{THD}^2}} \cos(\phi_1) \tag{2.1}$$

The THD is a measure of the harmonic distortion present in a signal in relation to the fundamental component and is described as

$$\text{THD} = \frac{\sqrt{\Sigma_{h=2}^{\infty} I_h^2}}{I_1} \tag{2.2}$$

where I_1 is the fundamental component and I_h is the h-th harmonics.

Regulatory standards have been introduced to prevent grid pollution by power converters. Described in these standards are the maximum allowed THD and EMC limits. For example, the NEN-EN-IEC 61000-3-12 [5] details limits for harmonic current of systems with input current >16 A and <75 A per phase, and the NEN-EN 55022 [6] provides CISPR 22 EMC limits.

In order to avoid over-dimensioning components and grid pollution, the PFC rectifier shapes the input currents sinusoidal and in-phase with the grid voltage, resulting in a unity power factor and ohmic behaviour of the converter, as depicted in Figure 2.1*a*. The Figures 2.1*b* and 2.1*c* respectively show behaviour where the current is displaced or distorted. The corresponding power factor is non-equal to 1 and the power converter shows non-ohmic behaviour, resulting in power limitations of the converter and/or grid pollution.

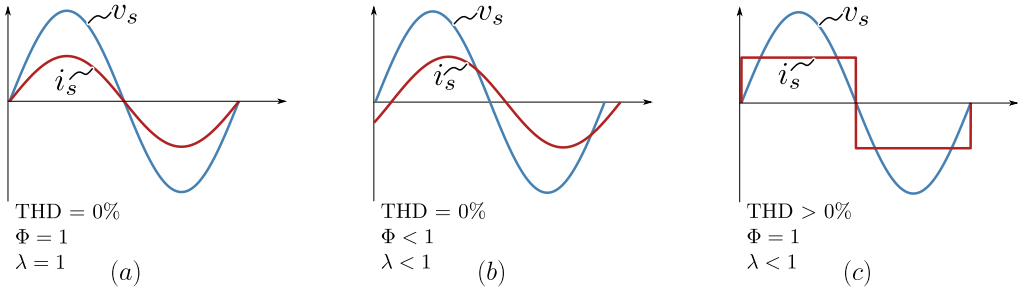

Figure 2.1: AC mains source voltage v_s and current i_s for different displacement factors and THD with corresponding power factor λ. Figure adapted from [7].

A single-phase boost PFC rectifier is a system that steps up the voltage with a lower output voltage limit specified as $U_{pn} > \sqrt{2}U_{ph,rms}$. Figure 2.2*a* shows the conventional single-phase boost PFC rectifier, a very simple boost topology where the rectification of the AC input voltage is done by the passive diode bridge, and the power factor correction of the input current and control of the output voltage is done by the boost circuit [8]. The converter operates at a high switching frequency to have a high power density and a fast transient response. However, when the boost converter is operated to have hard-switching transitions, the output diode will cause significant reverse-recovery losses. Other negative effects of the reverse-recovery are additional thermal management and electromagnetic interference (EMI). To overcome the problem of reverse-recovery, SiC Schottky diodes or SiC MOSFETs can be used instead of the output diode.

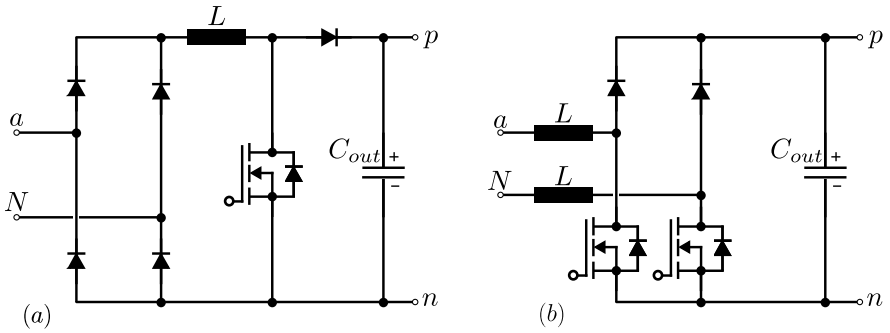

Figure 2.2: Single-phase PFC rectifier topologies with (*a*) the conventional boost PFC with rectifier stage and PFC stage separated and (*b*) the bridgeless (dual-boost) PFC rectifier.

An alternative boost PFC rectifier topology is the active bridgeless (dual-boost) PFC rectifier, as shown in Figure 2.2*b*. The rectifier and boost stage are combined into a hybrid rectification stage. Less semiconductor devices are conducting current, resulting in minimized conduction losses, thereby showing a higher efficiency compared to the conventional boost PFC rectifier.

The single-phase hybrid topology can be extended to a three-phase system, making it a half-controlled hybrid three-phase rectifier as depicted in Figure 2.3*a*. However, the problem with this converter is that it does not allow to for the impression of three sinusoidal AC input currents throughout the complete mains period [4]. This problem can be explained using Figure 2.4. In the 60° region where only phase voltage u_{aN} has a positive sign, switching-off $S_{\bar{a}n}$ result in the current i_a to flow through $D_{p\bar{a}}$. In the other phases, b and c, the body diodes $D_{n\bar{b}}$ and $D_{n\bar{c}}$ are conducting when switches $S_{\bar{b}n}$ and $S_{\bar{c}n}$ are switched-off. Sinusoidal input current can only be impressed for the 60° region where two phase voltage have a positive sign. The two phases voltages with a positive sign can be controlled to impress sinusoidal phase currents, the third phase follows to have a sinusoidal shaped current as a result of $i_a + i_b + i_c = 0$.

The six-switch boost converter, as depicted in Figure 2.3*b*, is an extension of the half-controlled hybrid three-phase rectifier where the diodes $D_{p(\bar{a},\bar{b},\bar{c})}$ are replaced with active switches. This converter allows for output voltage regulation, sinusoidal current impression over the full mains period, and bidirectional operation. Each rectifier bridge-leg is able to generate two voltages levels, a positive or negative voltage, referred to the virtual midpoint at the output. Hence, the converter allows to control the phase currents to

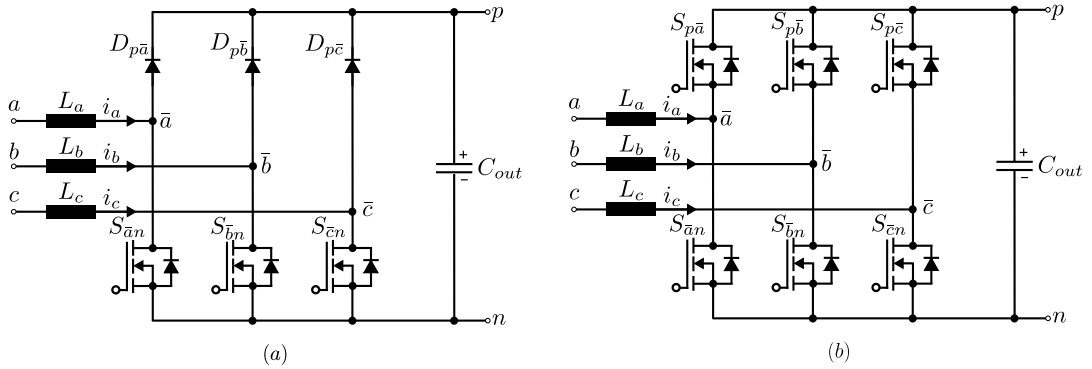

Figure 2.3: Three-phase PFC rectifier topologies with (*a*) the half-controlled hybrid three-phase rectifier and (*b*) full-controlled active rectifier also known as the six-switch boost rectifier.

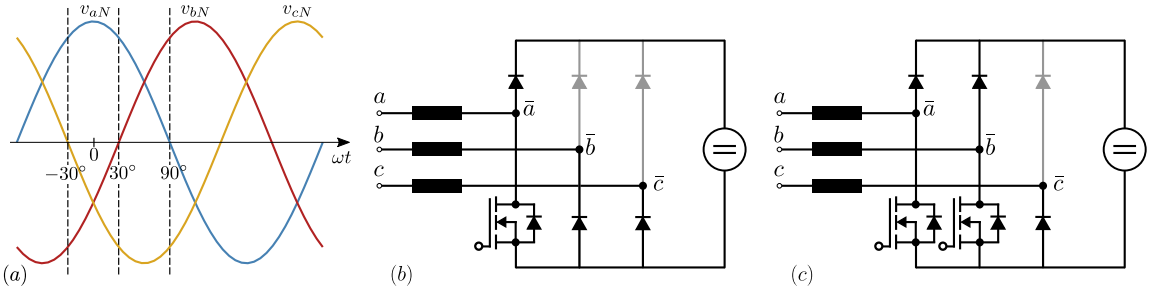

Figure 2.4: (*a*) Three-phase voltages within a mains period. (*b*) The half-controlled hybrid three-phase rectifier for the mains period between −30° and 30°. Only the current of one phase can be controlled. (*c*) The half-controlled hybrid three-phase rectifier for the mains period between 30° and 90° where phase a and b are controlling the corresponding phase currents.

be sinusoidal and with any phase displacement relative to the mains voltage, i.e., power can be fed back to the grid. This converter topology enables single-phase operation when connected as shown in Figure 2.5*b*. The downside is that the operation power is limited to 1/3 of the nominal three-phase power, since the power components of each phase are rated for nominal three-phase operation [9]. Single-phase operation with a total input current of 80 A would be feasible with the source connected as depicted in Figure 2.5*c*, thereby paralleling and interleaving phase a, b and c. However, in that configuration the magnetic core of the common mode (CM) choke will saturate because the return conductor, the neutral, is not added in the CM choke. Furthermore, each split DC-link capacitor would have high current stresses because these would need to buffer energy during a half mains cycle one after another. [9].

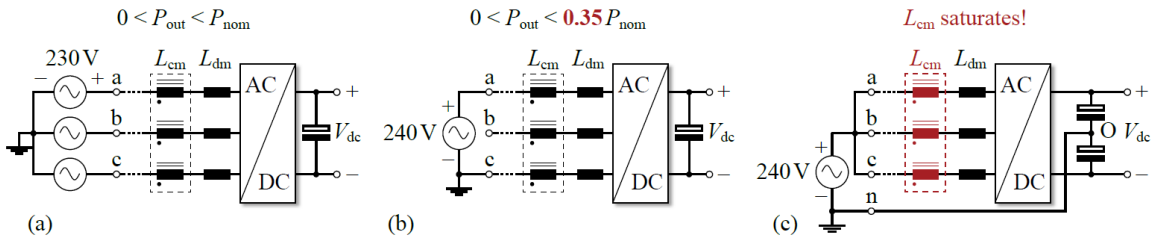

Figure 2.5: Examples of mains connections to a 3-ph power converter. Figure from [9]

Figure 2.6 shows the modifications to the six-switch boost rectifier to solve the single-phase power limitation, avoiding CM choke saturation and reducing the DC link rms currents. By using a 4-phase CM choke, the input phase and return currents are magnetically coupled, preventing magnetic core saturation both in 1-phase as well as 3-phase operation. The added passive diode bridge reduces the rms currents of the DC link capacitors. Finally, a relay contact is employed between the midpoints of the diode bridge-leg and the DC-link capacitors, which is needed to reduce CM noise in 1-phase operation [9]. These modifications can be applied to other boost PFC topologies, such as the Belgian PFC rectifier in this research.

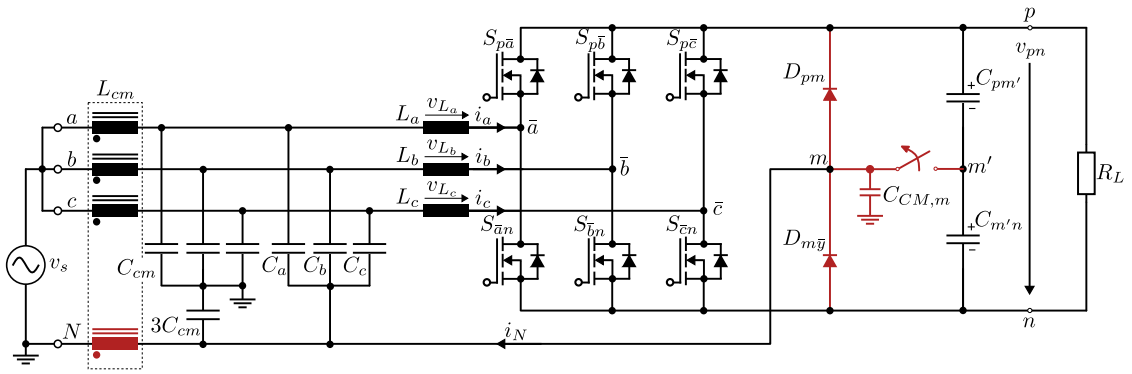

Figure 2.6: The modifications to the six-switch boost rectifier in red, to deliver full power in single-phase operation. Figure adapted from [9].

2.1.1. PFC Rectifier Efficiency and Power Density

The efficiency and power density of the PFC rectifier are important for EV battery chargers. The power density of a power converter can be improved by operating the active switches with a higher switching frequency. Moving to higher switching frequencies reduces the volume of the passive components by, for example, an increased cut-off frequency of the input filter, resulting in smaller inductor and capacitors required. The amount of current ripple in the boost inductor usually determines the inductor size. For higher switching frequency a smaller inductor can be used for the same amount of ripple current. However, a higher switching frequency goes at the costs of increased switching losses, since these scale proportional to the switching frequency. Soft-switching can be implemented to limit the increase of the semiconductor losses and have a reasonable combination of efficiency and power density. Higher losses result in needing more cooling effort which increases the volume, an optimum can be found for the power density and efficiency.

Table 2.1 gives an overview of realized boost PFC rectifier topologies, together with their performance indicators and used semiconductor technology. The BePFC rectifier of this research is competitive to these rectifier topologies, although not all topologies show performance indicators for combined single- and three-phase operation. Three single-phase PFC rectifiers can be connected in star(Y) or delta(Δ) to make it a three-phase rectifier, as explained in [4], while the conventional six-switch thee-phase rectifier is limited to 1/3 of its three-phase nominal power when connected to a single-phase mains.

Table 2.1: Realized boost-type PFC rectifiers.

Topology	Mains	Technology	Rated Power	Efficiency	Power Density
Modified Six-Switch Boost-	3-Ph	SiC MOSFET	22 kW	98.4 %	6.8 kW/dm^3
Type PFC Rectifier [9]	1-Ph	SiC MOSFET	19.2 kW	97.8 %	6.8 kW/dm^3
Totem-Pole PFC [10]	1-Ph	SiC MOSFET	6.6 kW	98.9 %	3.9 kW/dm^3
Belgian PFC Rectifier (BePFC)	3-Ph	SiC MOSFET	22 kW	-	-
Hardware Demonstrator	1-Ph	SiC MOSFET	19.2 kW	98.24 %	1.5 kW/dm^3
Virtual Prototype	1-Ph	SiC MOSFET	19.2 kW	98.4 %	5.34 kW/dm^3

The efficiency and power density of the three-phase BePFC is not given because the converter is modelled using a different converter model which is described in [11]. It is expected that the three-phase converter show comparable efficiency with the same power density.

2.2. Zero-Voltage Switching

The conduction losses in semiconductors are based on the drain-source resistance ($R_{DS,on}$) and the switching losses are based on the output capacitance (C_{oss}) and switching speed [12]. Zero voltage switching (ZVS) of semiconductors is used to reduce or eliminate the turn-on switching losses of a MOSFET. This allows the power converter to be operated at a higher switching frequency and improve the power density without significantly increasing the switching losses and decreasing the converter efficiency. To allow for ZVS transition, an inductive element is required that is connected to the midpoint of a MOSFET half-bridge [13].

With the single boost cell of Figure 2.8, the basic operation of a ZVS resonant transition, with turn-off of S_{11} and zero-voltage turn-on of $S12$, can be explained. Each power switch S_{xx} is made of a power transistor T_{xx}, a diode D_{xx}, and a non-linear parasitic capacitance C_{xx} (i.e., $C_{oss}(V_{DS})$) as depicted in Figure 2.7.

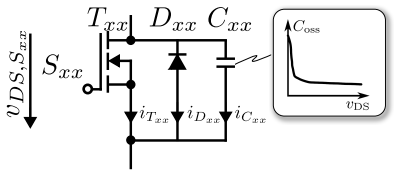

Figure 2.7: Representation of a switch S_{xx} with its transistors T_{xx}, diode D_{xx} and non linear capacitance C_{xx}. Figure adapted from [14].

Figure 2.8*a* depicts the first interval indicated in Figure 2.8*d*, where output capacitance C_{11} of switch S_{11} is charged to the voltage V_{DC}, switch S_{12} is in the ON-state, the voltage across the inductor is v_s and the inductor current is flowing through transistor T_{12} of switch S_{12}. The current i_L increases linearly. Switch S_{12} is turned OFF at t_1 and the channel resistance $R_{DS,S_{12}}$ of T_{12} starts to increase rapidly. Leading to the flow of inductor current through the total parasitic bridge leg capacitance. The turn-off of switch S_{12} is not completely lossless as there exists a voltage and current overlap in the MOSFET channel after t_1 [15]. A way to decrease the turn-off losses is to add an additional capacitor in parallel to the switch, lowering $\frac{dv}{dt}$ and thus reducing the voltage and current overlap. Additional advantages of adding parallel capacitance are easing the gate driver and lower EMC filtering requirements.

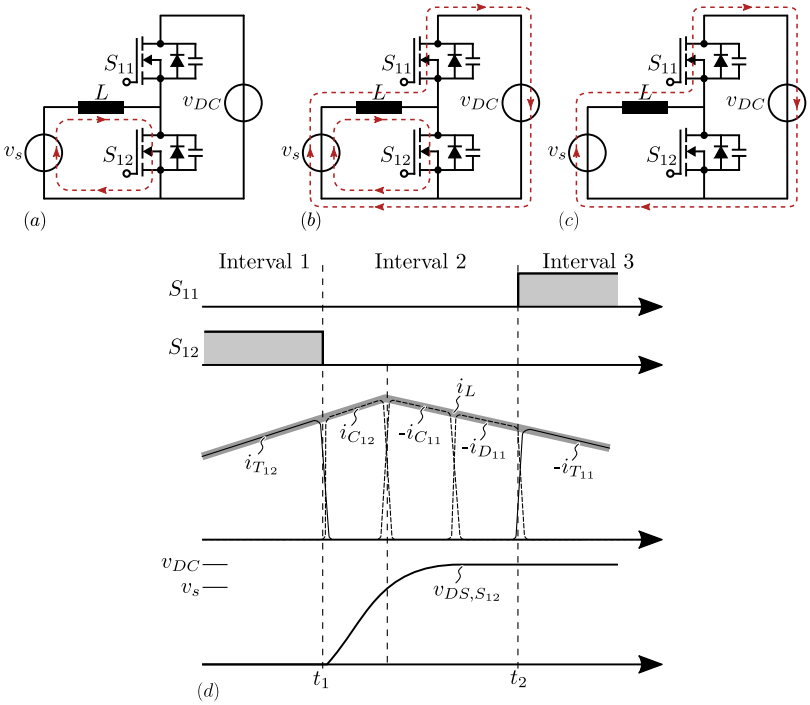

Figure 2.8: Example of a soft switching transition in a MOSFET half bridge from switch S_{12} to the top switch S_{11}. (*a*) Corresponds to the time interval before t_1 where switch S_{12} is ON; (*b*) Switch S_{12} turns OFF and the resonant transition starts charging and discharging the output capacitors of S_{12} and $S11$ respectively; (*c*) The body diode of switch S_{11} conducts the inductor current and switch T_{11} is turned ON with zero voltage; (*d*) the commutation currents of the switch transistor, switch capacitor and body diode corresponding to the three example circuits.

At the beginning of the second interval, which is shown in Figure 2.8*b*, the switch output capacitance C_{12} is discharged and forms a resonant circuit together with L and C_{11}. A resonant transition takes place where capacitor C_{12} is being charged and C_{11} discharged by the split inductor current i_L. The resulting increase of $v_{DS,S_{12}}$ causes the value of C_{12} to drop and that of C_{11} to rise leading to an inductor current transfer from C_{12} to C_{11}. These current commutations are shown in Figure 2.8*d*. The switching transition gets faster with a larger inductor current i_L.

When capacitor C_{11} is completely discharged, the body diode of S_{11} starts to conduct the inductor current and the third interval indicated in Figure 2.8d starts, corresponding to Figure 2.8c. After a deadtime, switch S_{11} is turned-on at zero drain-source voltage, achieving ZVS because the voltage drop across the body diode is negligible compared to V_{DC}.

Note that the same ZVS principle applies for a commutation from switch S_{11} to switch S_{12}. Also note that adding a capacitor in parallel with the switch, in order to reduce the $\frac{dv}{dt}$, increases the total charge Q_{oss} which needs to be removed or delivered by the inductor current to achieve a soft switching transition [15].

To conclude, in order to achieve ZVS it is required to have a large enough inductor current to remove charge Q_c to completely discharge the total equivalent output capacitance of the corresponding switch.

2.3. Modelling of Power Converters

There are multiple global trends in which optimization of power electronics is important as explained in [14] and [16]. The common objectives for these power electronics are improved efficiency, higher power density, minimized costs and high reliability. These objective are mutually coupled and can be translated into a set of 'performance indices'. Figure 2.9 show the performance indices including the fundamental trend in the design of power electronics. The design usually ends up having multiple design objectives for the optimal design.

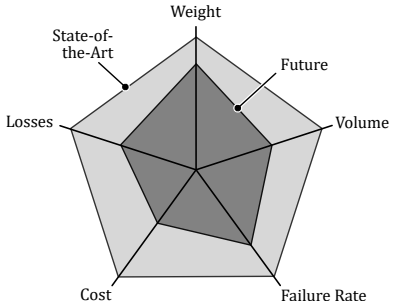

Figure 2.9: The representation of the state-of-the-art performance indices together with the fundamental trend (future) relevant in the design of power electronics. Adapted from [14].

The modelling and optimization of power converters can be done using mathematical multi-physics models of the converter and individual components. "The concept of optimization is the search for an optimal design with a set of alternatives with respect to performance measures" as stated by [17], such as efficiency and power density in this work. The performance measures for the optimization of power electronics are topically coupled. One example is a higher switching frequency implying smaller passive components and a higher power density. However, higher switching frequencies result in an increase in switching losses, making the converter less efficient [18].

The detailed mathematical modelling of the power converter can provide a complete estimate of the converter's performance aspects, such as losses, volume, EMI, and thermal stresses. Each coordinate in the design space, as depicted in Figure 2.10, represents a single converter design with performance aspects. These performance aspects can be combined into the total converter efficiency and volume, which can be mapped into a performance space [17]. The performance space is bounded by the Pareto Front. From the performance space, the best design with regard to multiple objectives can be chosen. The process of mapping the design space into the performance space and ultimately identifying the Pareto Front is also known as virtual prototyping [17]. The advantage of virtual prototyping is that there is no need to do multiple hardware design iterations to get to an optimal design. The optimization may feature up to a 1000 different converter designs since each design variable, such as semiconductor selection, inductor selection, switching frequency etc. adds possible converter designs. The main challenge with virtual prototyping is the minimization of the computation time.

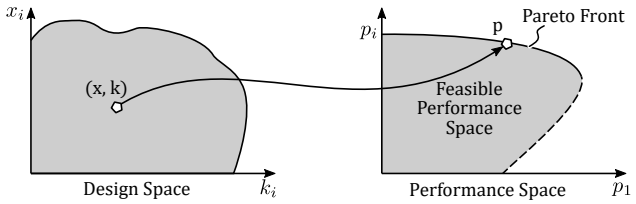

Figure 2.10: Representation of the design optimization where the multi dimensional design space is mapped onto the Performance Space. The feasible designs are bounded by the Pareto Front.

The modelling of a single converter design of the BPFC rectifier for this work is done using the flow diagram as depicted in Figure 2.11. This diagram is adapted from literature that have proven this modelling approach such as [14, 15, 18–20]. First the converter specification, such as input voltage v_i, output voltage v_o, output power P_o, grid frequency f_{gr} and EMC limits, have to specified to be able to evaluate the converter characteristics. For this research, these converter specifications (requirements) are listed in Table 1.1. Next, the system parameters have to be specified, including the component values, number of interleaved stages, number of switches placed in parallel, modulation scheme, switching frequency limits etc. The design space for the design optimization for this research is explained in section 6.2.

Based on the converter specifications and system parameters, the (converter specific) average model is used to calculate the duty cycles, average voltages, average currents and switching frequency as discussed in section 3.3 and 3.4.

With the information from the average model, the switching model calculates the Fourier coefficient to describe the switch-cycle waveforms. Examples are switch node voltage waveforms, inductor voltage and currents waveforms etc. These waveforms are analysed in the Fourier domain in order to increase the modelling possibilities, in particular with respect to the EMI model [15]. The Fourier modelling is explained in section 4.4

The modelling is then split into the component specific models, such as the semiconductor, inductor and EMI models. These models calculate the component specific losses, thermal stresses, and volume. The component volumes and losses are combined to calculate the total converter volume and efficiency.

The design optimization of the BePFC rectifier is done using the flow diagram as depicted in Figure 4.1. This flow diagram makes use of the single converter design model explained with Figure 2.11 and changes a system parameters, e.g. inductor value and switching frequency, in each virtual design iteration. The virtual designs are mapped into the performance space to find the Pareto Front and optimum design.

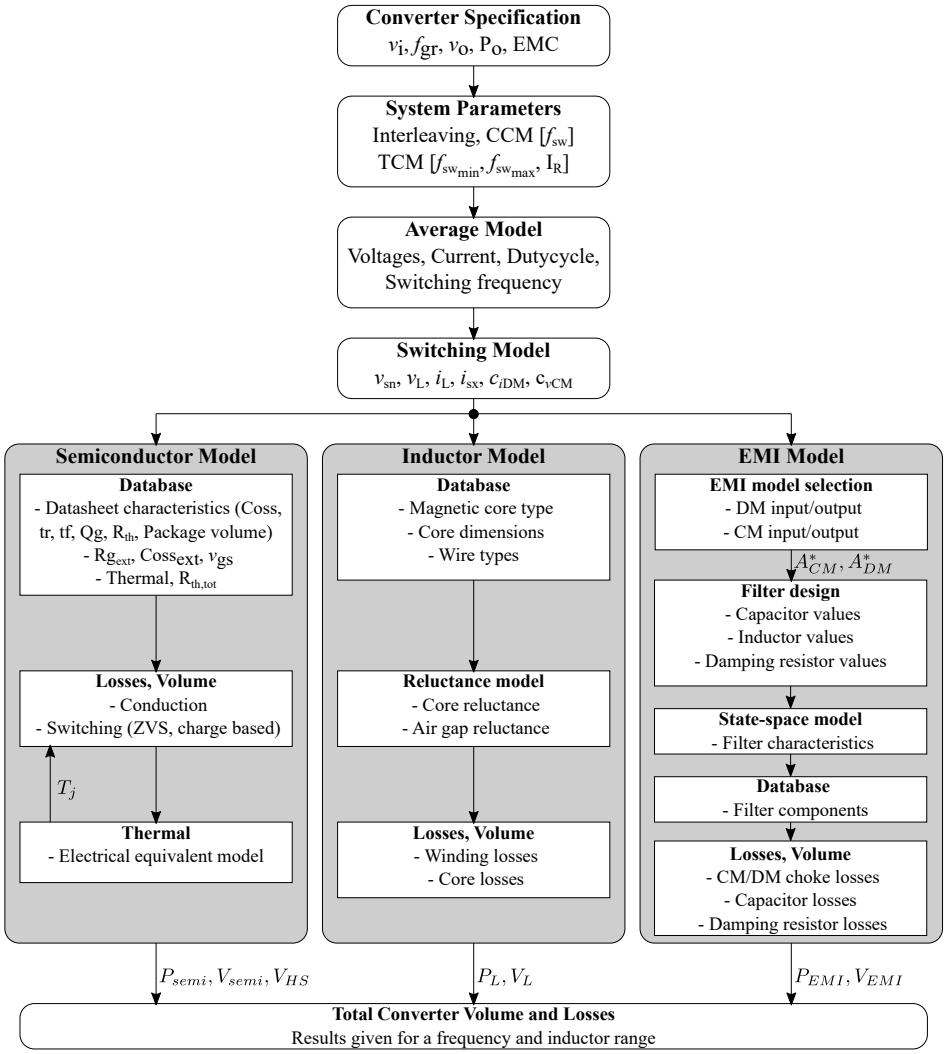

Figure 2.11: Modelling approach for single converter design.

3

Belgian Boost PFC Rectifier

3.1. Introduction

In this chapter, the single-phase operation of a novel three-phase boost PFC rectifier is explained. The single-phase Belgian PFC (BePFC) rectifier is derived from the three-phase BePFC rectifier [21] and is able to output comparable power in three-phase as well as single-phase operation without over-dimensioning the power stage. In single-phase operation this converter topology is able to be operated with complete ZVS conditions. The BePFC rectifier topology is explained in detail and the advantages of this topology are given. Furthermore, the operation principle, steady state analysis, conduction states, and modulation scheme to facilitate complete ZVS transition are outlined.

3.2. Belgian PFC Rectifier Topology

The BePFC rectifier, shown in Figure 3.1, is originally patented as a three-phase boost-type AC-to-DC converter that features a fully integrated top and bottom boost circuit together with a three-phase bridge rectifier to allow for a pulsed voltage at the rectifier output [21]. The semiconductor switches are controlled using pulse width modulated (PWM) control signals or are switched into the selection state. The top and bottom boost circuit control two out of three-phase current, i.e., the currents at the phase having the highest and the lowest voltage levels of the three-phase input voltages. The respective bridge legs of the rectifier that are connected to these phases are in a selection state (constant ON). The current of the remaining input phase, having an intermediate voltage level between the highest and lowest voltage levels, is controlled using PWM modulation of the corresponding bridge leg of the rectifier. This bridge leg is therefore in an active state (PWM state) instead of a selection state. The current control loop of the BePFC generates PWM signals to control the semiconductor switches of the rectifier bridge and boost circuit in order to control the current in each boost inductor/phase.

Advantages of the BePFC rectifier regarding the three-phase operation are:

- **Smaller phase inductors**; The top and bottom boost circuit generate a three-level voltage between the rectifier output nodes. As a result, the ripple of the inductor currents i_{abc} is smaller than for a conventional six-switch boost-type PFC rectifier. For the same ripple, smaller phase inductors can be used.
- **Reduced switching losses**; only one out of the three rectifier bridge legs are in an active switching state switching the three-level voltage between the rectifier output nodes. The top and bottom boost legs switch only half the DC bus voltage, resulting in an improved efficiency of the system due to lower switching losses.
- **Semiconductor switches with a lower voltage rating** of $V_{out}/2$, can be used in the top and bottom boost circuit. A lower breakdown voltage usually results in the reduction of switching losses. A reduction in conduction losses can also be obtained due to a lower $R_{DS,on}$ compared to higher voltage rating devices which are used in the rectifier bridge.

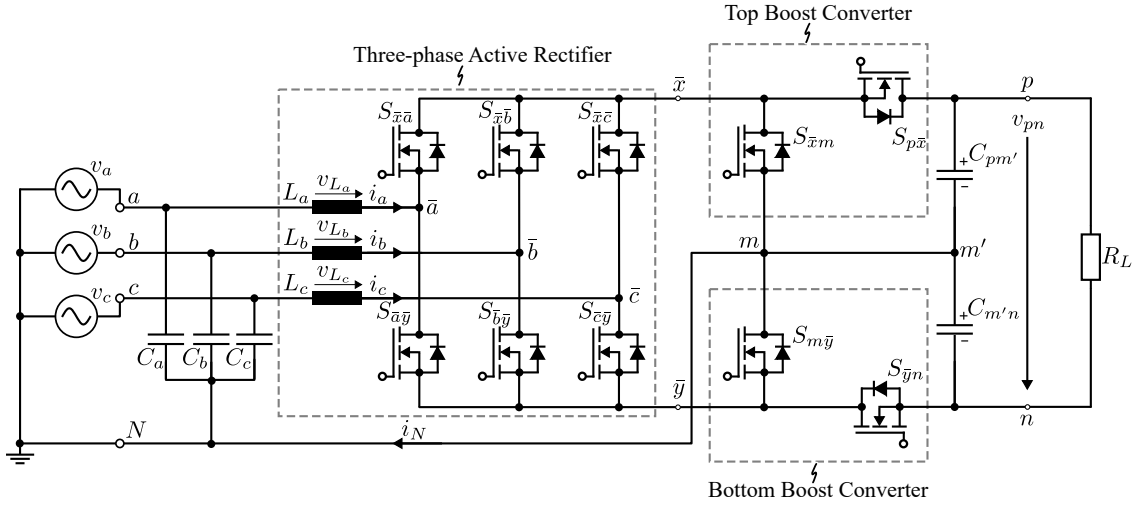

Figure 3.1: Circuit topology of the Belgian PFC rectifier connected to a three-phase grid and a resistive load.

3.2.1. Single-Phase Operation

The BePFC rectifier can be operated, with minor modifications, in single-phase at comparable nominal power levels without changing the three-phase operation. These modifications have been explained in section 2.1 with respect to the 6-switch boost rectifier. The modifications to the BePFC rectifier, depicted in Figure 3.2, are as follows:

- A relay contact is placed between the midpoint m of switches $S_{\bar{x}m}$ and $S_{m\bar{y}}$ and the midpoint m' of the DC-link capacitors $C_{pm'}$ and $C_{m'n}$.
- A 4-phase CM choke is used in the input EMI filter.

The bridge legs of the three-phase active rectifier act in parallel and interleaved for the single-phase operation, forming the interleaved boost circuit. The interleaved boost bridge legs, switching with high (variable) frequency (HF), shape the inductor current i_{L_a} i_{L_b} and i_{L_c} to be sinusoidal and proportional to the phase voltage v_s. Switches $S_{\bar{x}m}$ and $S_{m\bar{y}}$ form the low frequency (LF) switch leg, switching synchronously with the mains frequency, either connecting the output bus n to midpoint m or the output bus p to m based on the sign of the mains voltage. For a positive input voltage switch $S_{m\bar{y}}$ is in the ON-state and switch $S_{\bar{x}m}$ is in the OFF-state, and vise versa. The switches $S_{p\bar{x}}$ and $S_{\bar{y}n}$ are always in the ON-state. The external return path, from the midpoint m of the LF switch leg to N, in combination with the 4 phase CM choke allow the single-phase BePFC to be operated at comparable nominal power to the three-phase BePFC rectifier.

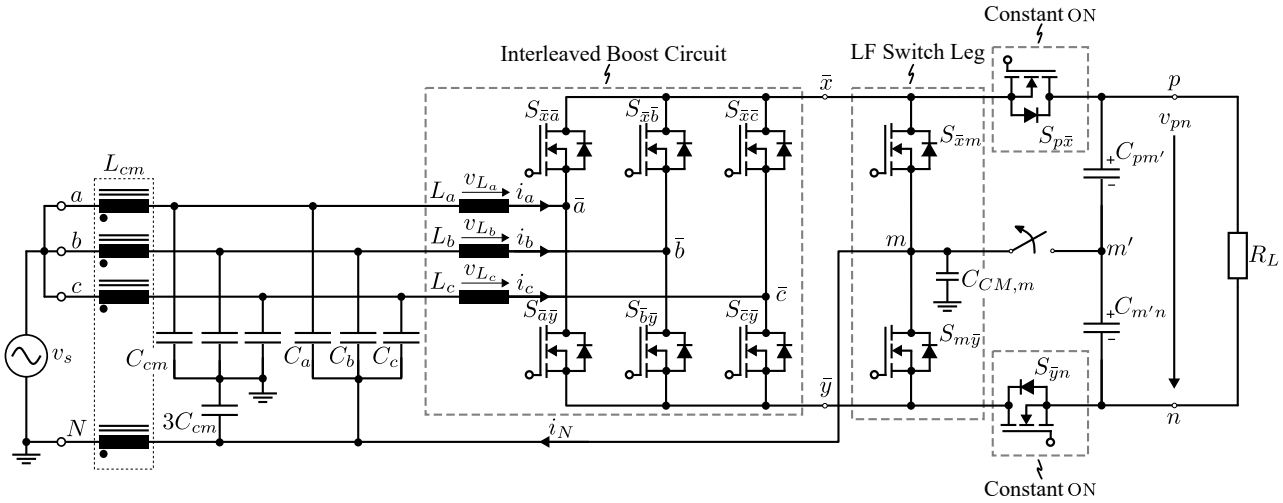

Figure 3.2: Circuit topology of the Belgian PFC rectifier connected to a single-phase grid and a resistive load with modifications, compared to Figure 3.1, to be able to operate at full power.

The single-phase BePFC rectifier allows for complete ZVS when a triangular current mode (TCM) is used. As explained in section 2.2, zero-voltage turn-on of switches $S_{\bar{x}\bar{a}}$, $S_{\bar{x}\bar{b}}$ and $S_{\bar{x}\bar{c}}$ is achieved with a large enough positive current in the inductor. To zero-voltage turn-ON the switches $S_{\bar{a}\bar{y}}$, $S_{\bar{b}\bar{y}}$ and $S_{\bar{c}\bar{y}}$, a large enough negative inductor current is required. So, in a switching cycle a zero-crossing of the inductor current is required, which can be facilitated with TCM. This type of modulation results in a variable switching frequency and is further explained in section 3.4. The inductor current ripple in TCM is high, but the interleaved operation of the boost bridge legs result in superposition of the inductor current ripple, reducing the input current ripple i_s, as depicted in Figure 3.3. The interleaving of the inductor current results in a lower required EMI filter attenuation.

The single-phase BePFC rectifier output voltage is lower than the output voltage in three-phase operation. This is a result of the decision going for lower voltage rating semiconductors in the top and bottom boost circuit for the three-phase BePFC rectifier due to only switching half the output voltage. The explanation how the DC/DC converter is connected after the BePFC rectifier is explained later using Figure 3.9.

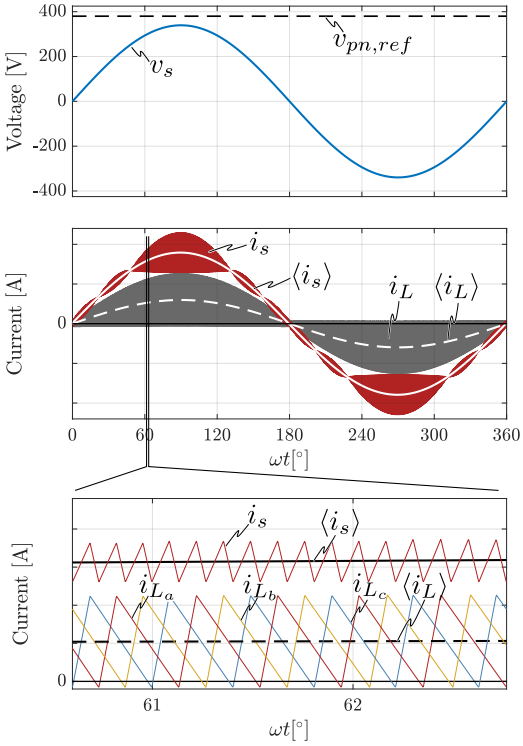

Figure 3.3: Belgian PFC rectifier input voltage and output voltage together with the input current i_s and inductor currents waveforms i_L for $v_{pn,ref} = 380$V in single-phase operation with three times interleaving.

The advantages of the single-phase BePFC rectifier are:

- No need to add additional passive diodes for the LF bridge, as is required for the six-switch boost (cf. Figure 2.5);
- The interleaving of the inductor currents result in low attenuation requirements;
- The topology allows for complete ZVS transitions over the full mains cycle;
- The single-phase operation benefit from the low inductance value (and volume) required in three-phase operation.

3.3. Steady-State Average Operation

The average input current i_s of the converter is defined by the input voltage v_s and the output power P_o of the converter. The HF semiconductor switches $S_{\bar{x}(\bar{a},\bar{b},\bar{c})}$ and $S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$ are switched in such way that the summed local average inductor currents follows the reference input current i_s. For the steady-state analysis it has been assumed that:

- The input and output voltages are constant within a switching cycle, $f_{sw} >> f_{mains}$
- $v_{pn} = \langle v_{pn} \rangle$ = constant
- The switching cycle averaged volt-sec across an inductor is zero, $\langle v_{L_a} \rangle = 0$
- $\langle i_L \rangle$ is the sum of the local average inductor currents $\langle i_{L_{(a,b,c)}} \rangle$

Where $\langle\rangle$ denotes the switch-cycle average value of the parameter.

The converter steady-state operation of the circuit from Figure 3.2, is analysed by solving equations describing the relation between the input and output voltages. The relation between input and output can be described using the duty cycle expression for this rectifier topology:

$$d_{(\bar{a},\bar{b},\bar{c})\bar{y}} = \begin{cases} 1 - \frac{v_s}{v_{pn}}, & \text{if } v_s > 0 \\ -\frac{v_s}{v_{pn}}, & \text{if } v_s < 0 \end{cases} \tag{3.1}$$

Where the duty cycles for the switches $S_{\bar{a}\bar{y}}$, $S_{\bar{b}\bar{y}}$ and $S_{\bar{c}\bar{y}}$ are equal but the bridge legs switch interleaved. The duty cycle d denotes the relative conduction interval of the corresponding switch.

By applying Kirchoff's voltage law to the converter, the following equations can be obtained:

$$v_{am} = \langle v_{\bar{a}m} \rangle = \begin{cases} (1 - d_{(\bar{a},\bar{b},\bar{c})\bar{y}}) \cdot v_{pn}, & \text{if } v_s > 0 \\ (-d_{(\bar{a},\bar{b},\bar{c})\bar{y}}) \cdot v_{pn}, & \text{if } v_s < 0 \end{cases} \tag{3.2}$$

$$v_{pn} = v_{pm} - v_{nm} \tag{3.3}$$

By applying Kirchoff's current law to the converter, as depicted in Figure 3.2, the following equations are derived:

$$\langle i_{pn} \rangle = \langle i_{\bar{x}} \rangle - \langle i_{C_{out}} \rangle \tag{3.4}$$

Where the currents $\langle i_{\bar{x}} \rangle$ and $\langle i_{\bar{y}} \rangle$ can be described using the following equation:

$$\begin{aligned} \langle i_{\bar{x}} \rangle &= (1 - d_{(\bar{a},\bar{b},\bar{c})\bar{y}}) \cdot \langle i_L \rangle \quad \text{if } v_s > 0 \\ \langle i_{\bar{y}} \rangle &= (-d_{(\bar{a},\bar{b},\bar{c})\bar{y}}) \cdot \langle i_L \rangle \quad \text{if } v_s < 0 \\ \langle i_{\bar{x}} \rangle &= -\langle i_{\bar{y}} \rangle \end{aligned} \tag{3.5}$$

The steady-state waveforms for the operation with nominal power $P_o = 19.2\,\text{kW}$ can be found in Figure 3.4. Figure 3.4*a* and *b* show the main converter voltage waveforms, including the average input current $\langle i_s \rangle$. Figure 3.4*c* shows the average inductor currents $\langle i_{L_{(a,b,c)}} \rangle$, output capacitor current $\langle i_{C_{out}} \rangle$ and average intermediate current $\langle i_{\bar{x}} \rangle$. Figure 3.4*d* shows the converter duty cycles of the boost bridge legs.

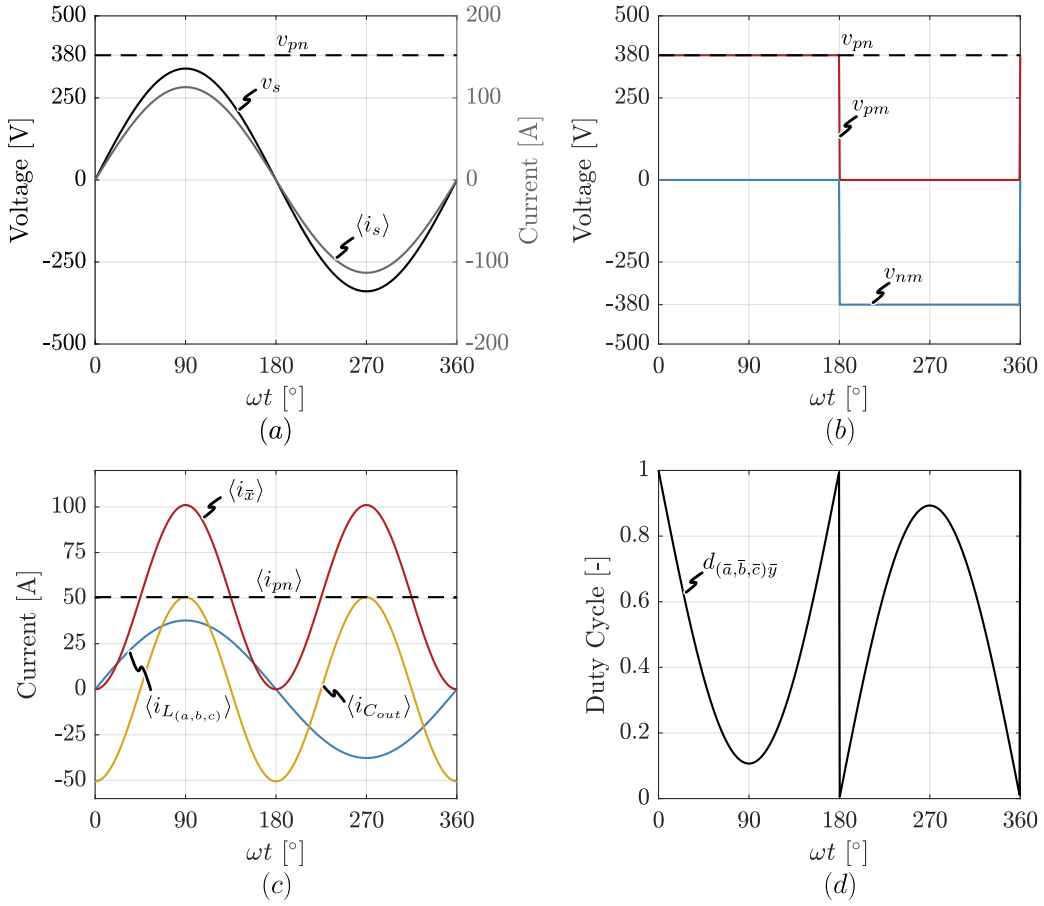

Figure 3.4: Single-phase steady-state average waveforms of (*a*) the input voltage v_s and current $\langle i_s \rangle$ together with the output voltage v_{pn} (*b*) the output voltages v_{pm}, v_{nm} and v_{pn} (*c*) the inductor current $\langle i_{L_{(a,b,c)}} \rangle$ with the intermediate current $\langle i_{\bar{x}} \rangle$ and average output current $\langle i_{C_{out}} \rangle$ and (*d*) the duty-cycle d of the HF interleaved boost bridge legs.

3.4. Basic Operation

Figure 3.5 shows a simplified single-phase BePFC rectifier where only a single boost half bridge of phase a is considered with corresponding conduction states. The output capacitors $C_{pm'}$ and $C_{m'n}$ are replaced by a single equivalent output capacitor C_{out}, and the constant ON switches ($S_{p\bar{x}}, S_{\bar{y}n}$) are replaced with a short circuit. The bridge leg formed by switches $S_{\bar{x}m}$ and $S_{m\bar{y}}$ switch synchronously with the mains frequency based on the sign of the input voltage v_s. For a positive input voltage v_s, $S_{m\bar{y}}$ is turned ON and $S_{\bar{x}m}$ is turned OFF.

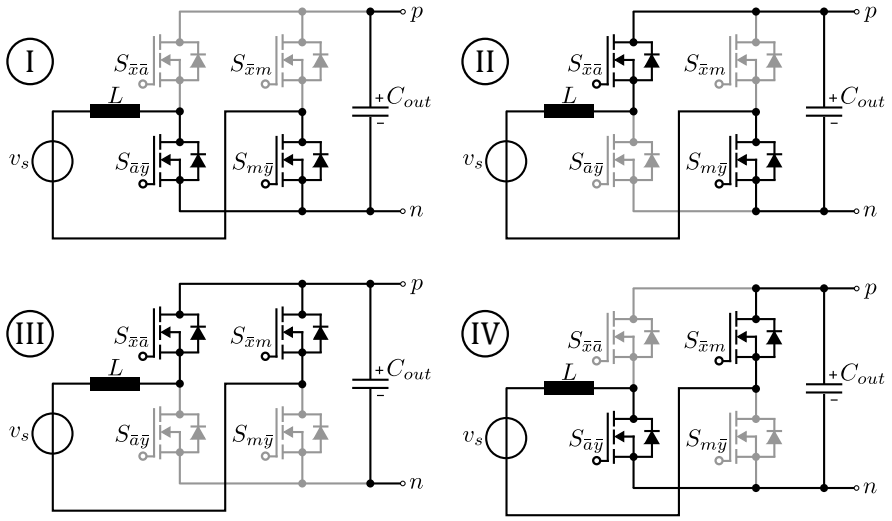

Figure 3.5: Conduction states of phase a of the BePFC rectifier. Conductions states I and II apply for a positive input voltage v_s, and III and IV for a negative input voltage.

Multiple modulation schemes are possible for this topology. Typical waveforms for boundary conduction mode (BCM) and triangular current mode (TCM) are shown in Figure 3.6. By using the BCM modulation technique proposed in [22] ZVS is can only be achieved when $|v_s| < v_{pn}/2$, for a larger input voltage valley switching is implemented to decrease switching losses. The use of TCM modulation allows for complete ZVS transitions over the entire mains period. A disadvantage of using TCM modulation is the large inductor ripple that will be imposed at the input, which initially results in the need for a larger differential mode (DM) EMI filter. The interleaving of the half bridges make it possible to reduce the EMI filter size, e.g., for a 3 times interleaved converter only the fundamental and multiples of the third harmonic have to be filtered since the other harmonics are cancelled. The variable switching frequency, due to the TCM modulation, has the additional advantage of a lower required EMI attenuation [23].

The basic principle of operation of the BePFC rectifier can be explained using Figure 3.6. The waveforms are based on the single boost leg equivalent circuit, as shown in Figure 3.5, with a positive input voltage. For a negative input voltage similar explanation follows, only the role of the switches $S_{\bar{x}\bar{a}}$ and $S_{\bar{a}\bar{y}}$ are interchanged.

Interval 1 $[t_0 ... t_1]$ The switch $S_{\bar{x}\bar{a}}$ is in the ON-state and the voltage v_s is applied to the boost inductor, the inductor current i_{L_a} rises linearly with a slope of v_s/L until $\hat{I}_S$. In case of BCM modulation in Figure 3.6*a* the value $\hat{I}_S = 2 \cdot \langle i_{L_a} \rangle$. For TCM modulation, as depicted in Figure 3.6*b*, the value $\hat{I}_S = 2 \cdot \langle i_{L_a} \rangle + \hat{I}_R$, where $\hat{I}_R$ is the reverse current in order to achieve ZVS, explained later with eq. (3.9). The additional reverse current $\hat{I}_R$ have to be compensated for with a higher peak current $\hat{I}_S$ to achieve the same average switch cycle inductor current. When the current $\hat{I}_S$ is reached, the switch $S_{\bar{x}\bar{a}}$ is turned OFF.

Interval 2 $[t_1 ... t_2]$ A resonant transition takes place between the inductor L and output capacitances C_{oss1} and C_{oss2} of switch $S_{\bar{x}\bar{a}}$ and $S_{\bar{a}\bar{y}}$ respectively, which charges the output capacitor C_{oss2} of switch $S_{\bar{a}\bar{y}}$ and discharges C_{oss1} of switch $S_{\bar{x}\bar{a}}$. A larger inductor current i_{L_a} results in a faster resonant transition.

Interval 3 $[t_2 ... t_3]$ After the resonant transition, C_{oss2} of switch $S_{\bar{a}\bar{y}}$ is fully charged to v_{pn} and the body diode of $S_{\bar{x}\bar{a}}$ starts conducting the inductor current. After a predefined deadtime the switch $S_{\bar{a}\bar{y}}$ can be turned ON with ZVS, as was already explained in section 2.2. During this interval the voltage applied to the inductor is $v_s - v_{pn}$ and the inductor current decreases linearly with a slope of $(v_s - v_{pn})/L$.

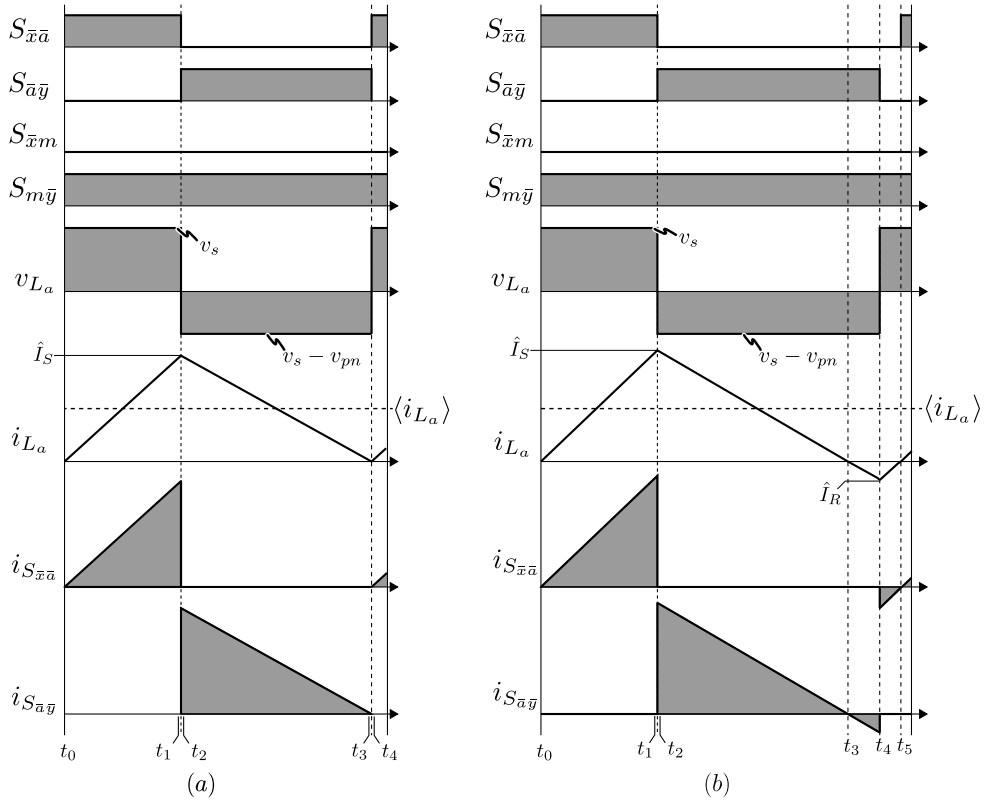

Figure 3.6: Typical waveforms of (*a*) BCM modulation and (*b*) TCM modulation with corresponding inductor and switch currents. The conduction states ($S_{\bar{x}\bar{a}} = 0, S_{\bar{a}\bar{y}} = 1$ & $S_{\bar{x}\bar{a}} = 1, S_{\bar{a}\bar{y}} = 0$) respectively correspond to I and II of Figure 3.5.

Interval 4 $[t_3 ... t_4]$ If BCM modulation is considered as depicted in Figure 3.6*a*, $S_{\bar{x}\bar{a}}$ is turned OFF when i_{L_a} reached zero. The boost inductor L, in combination with C_{oss1} of switch $S_{\bar{x}\bar{a}}$ and C_{oss2} of switch $S_{\bar{a}\bar{y}}$ become an oscillating resonant circuit. The oscillation behaviour depends on the input and output voltage ratio, for $|v_s| < v_{pn}/2$ the voltage over $S_{\bar{x}\bar{a}}$ rises to v_{pn} and the voltage of $S_{\bar{a}\bar{y}}$ declines to zero, thereby ZVS can be achieved [22]. If $|v_s| > v_{pn}/2$, ZVS can not be achieved and the $S_{\bar{a}\bar{y}}$ can be switched ON with valley switching to decrease the switching losses. To overcome the drawback of loosing ZVS, TCM modulation can be used. Switch $S_{\bar{x}\bar{a}}$ remains in the ON state after i_{L_a} reached zero, as depicted in Figure 3.6*b*. The inductor current keeps decreasing linearly with a slope of $(v_s - v_{pn})/L$, until a reverse current $\hat{I}_R$ is reached.

Interval 5 $[t_4 ... t_5]$ The switch $S_{\bar{x}\bar{a}}$ is turned OFF, the inductor current is large enough to have sufficient energy for the resonant transition which charges C_{oss1} of switch $S_{\bar{x}\bar{a}}$ and completely discharges C_{oss2} of switch $S_{\bar{a}\bar{y}}$. After C_{oss2} is completely discharged, the body diode of $S_{\bar{a}\bar{y}}$ starts conducting and after a specified deadtime the switch $S_{\bar{a}\bar{y}}$ can be turned ON with ZVS. At the time $t = t_5$ a new switching cycle starts.

The switch currents shown in Figure 3.6, are formed by segments of the inductor current. The average switch current can be calculated as:

$$\langle i_S \rangle = \frac{1}{T_{sw}} \int_{T_x} i_L(t) dt \tag{3.6}$$

where T_x denotes the conduction interval of the switch within a switching cycle period T_{sw} and $\langle i_S \rangle$ the average switch current. The average switch current can be simplified to:

$$\langle i_S \rangle = d \cdot \langle i_L \rangle \tag{3.7}$$

where d is the switch duty cycle, $\langle i_L \rangle$ the local average inductor current and $\langle i_S \rangle$ the average switch current.

The three boost bridge legs of a BePFC rectifier switch interleaved to limit the input current ripple of the power converter. The phase shift of each bridge leg is calculated as:

$$\phi_k = \phi_1 + \frac{k \cdot 2\pi}{3 \cdot n_i} \qquad \text{with } k \in \{1,2,3 \cdot n_i\} \tag{3.8}$$

where k the the bridge-leg count and n_i is the number of BePFC rectifiers in parallel. For example, two BePFC rectifiers in parallel result in six bridge legs that switch interleaved.

The inductor current is shaped by the interleaved bridge leg switches in such way that the sum of the local average inductor currents follows the reference current i_s which is proportional to the input voltage v_s and output power. There is an infinite set of combinations of $\hat{I}_S$ and $\hat{I}_R$ which result in the required average inductor current $\langle i_{L_a} \rangle$ since a larger reverse current $\hat{I}_R$ can be compensated for with a higher $\hat{I}_S$ and vise versa. However, a larger $\hat{I}_R$ and $\hat{I}_S$ result in a higher rms current i_{L_a} and flux density swing of the boost inductors, increasing the winding and core losses. Changing the combination of $\hat{I}_S$ and $\hat{I}_R$ results in different switching frequencies, imposing different switching losses.

The closed-form analytical model as proposed in [24] provides expressions to be able to calculate the switching instances and required reverse current $\hat{I}_R$ to achieve ZVS over the full mains period. The reverse current can be calculated using the following formula:

$$\hat{I}_R = \begin{cases} -\sqrt{\frac{2Q_c}{L}(2v_s - v_{pn})}, & \text{if } v_s > \frac{v_{pn}}{2} \\ 0, & \text{if } v_s < \frac{v_{pn}}{2} \end{cases} \tag{3.9}$$

The required reverse current depends on v_{pn}, v_s and semiconductor switch selection that defines Qc which is the charge required to be removed to discharge C_{oss} of the switch. If additional capacitors are placed in parallel with the switch to reduce the turn OFF losses, more charge has to be removed to discharge C_{oss} and achieve ZVS.

For the remainder of this thesis TCM modulation is used to facilitate ZVS over the entire mains cycle. However, the reverse current $\hat{I}_R$ is set to a fixed value, larger than the minimum required reverse current, over the entire mains period. This is done to simplify the analysis and make sure a safety factor is taken when ZVS need to be achieved.

The switching frequency of the BePFC can be calculated with

$$\begin{aligned} T_{sw} &= \frac{L_{boost} \cdot 2 \cdot (|\langle i_{L_a} \rangle| + \hat{I}_R)}{|v_s|} + \frac{L_{boost} \cdot 2 \cdot (|\langle i_{L_a} \rangle| + \hat{I}_R)}{|v_s| - v_{pn}} \\ f_{sw} &= \frac{1}{T_{sw}} \end{aligned} \tag{3.10}$$

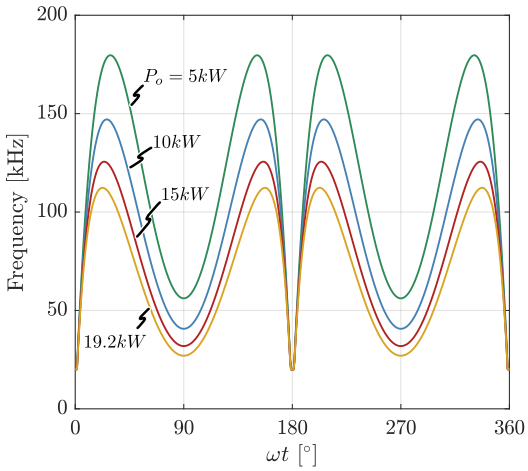

Figure 3.7: Resulting switching frequency of a bridge leg using TCM modulation, considering a twice interleaved BePFC rectifier (6 times effectively interleaving) with a boost inductor of L = 25.01µH for different power levels.

Figure 3.7 shows the switching frequency waveform for two BePFC rectifiers in parallel (effectively 6 times interleaving because of three parallel bridge legs per rectifier), with a boost inductor of L = 25.01µH for different output power levels. The switching frequency increases with a decreasing output power and vise versa. Choosing a smaller boost inductor also results in an increased switching frequency. The switching frequency should be limited in order to not enter the audible region (f_{sw}> 20 kHz) and should have an upper limit of $f_{sw,max}$ because switching losses become significant at higher switching frequencies increasing the converter cooling volume [25]. As an alternative, the switching frequency can be fixed in order to let the converter operate with continuous current mode (CCM) modulation within large regions of the mains cycle as explained in [19] for a PFC full-bridge topology.

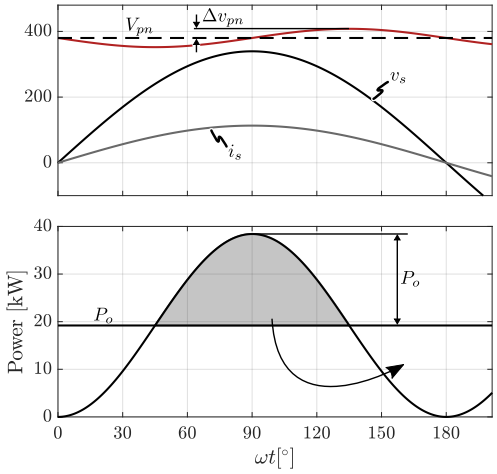

Figure 3.8: The single-phase grid connected power converter have a power variation with twice the mains frequency, an output capacitor is place to smooth out the energy variations resulting in an output voltage ripple Δv_{pn}. Adapted from [24]

In single-phase grid connected power converters, the energy flow from the input is not constant and has a power variation with twice the mains frequency. This phenomenon is shown in Figure 3.8 and can be explained using the following formula[24, 26]:

$$\begin{aligned} p_o(t) &= \eta v_s(t) i_s(t) = \eta \hat{V}_s |\sin \omega_{gr} t| \hat{I}_s |\sin \omega_{gr} t \\ &= \eta \hat{V}_s \hat{I}_s \cdot (1 - \cos(2\omega_{gr} t)) = P_o \cdot (1 - \cos(2\omega_{gr} t)) \end{aligned} \tag{3.11}$$

where η is the converter efficiency and $\omega_{gr} = 2\pi f_{gr}$ is the grid angular frequency. The output power has a constant component P_o and a varying component $\Delta p_o = -P_o \cdot \cos(2\omega_{gr} t)$. The output capacitor is used to smooth the energy variations. Initially the output capacitor was assumed to be large enough so the output voltage v_{pn} was stable. However, the capacitor is not infinity large and a ripple voltage can be estimated [26]. The output capacitor has to deliver energy to the load when $p_o(t) < P_o$. Equation (3.4) can be used to calculate the LF capacitor current. The inductor current ripple results in an output voltage ripple which can be calculated as:

$$\begin{aligned} v_{pn}(t) &\approx V_{pn} + \frac{1}{C_{out}} \int i_{C_{out}} dt \\ &= V_{pn} - \frac{P_o}{V_{pn}} \cdot \frac{1}{2\omega_{gr} C_{out}} \cdot \sin(2\omega_{gr} t) \end{aligned} \tag{3.12}$$

The maximum output voltage ripple can be calculated with

$$\Delta v_{pn} = \frac{P_o}{v_{pn}} \frac{1}{2\omega_{gr} C_{out}} \tag{3.13}$$

With a specified maximum allowed ripple, the minimum required capacitance can be calculated. For the BePFC rectifier with an output power of 19.2 kW and an output voltage $v_{pn} = 380$ V and maximum allowed voltage ripple of $\Delta v_{pn} = 10$ V, the minimum output capacitor is

$$C_{out,min} = \frac{P_o}{2\omega_{gr} \cdot \Delta v_{pn} \cdot v_{pn}} = 7.3\,\text{mF} \tag{3.14}$$

For the three-phase operated BePFC rectifier, the output capacitors are switched in series in order to withstand the full DC-link voltage of 750 V as shown in Figure 3.9*a*. In single-phase operation the output capacitors including DC-DC converters are switched in parallel, as shown in Figure 3.9*b*. The paralleling is possible due to the lower bus voltage of 380 V and is done in order to achieve a larger output capacitance.

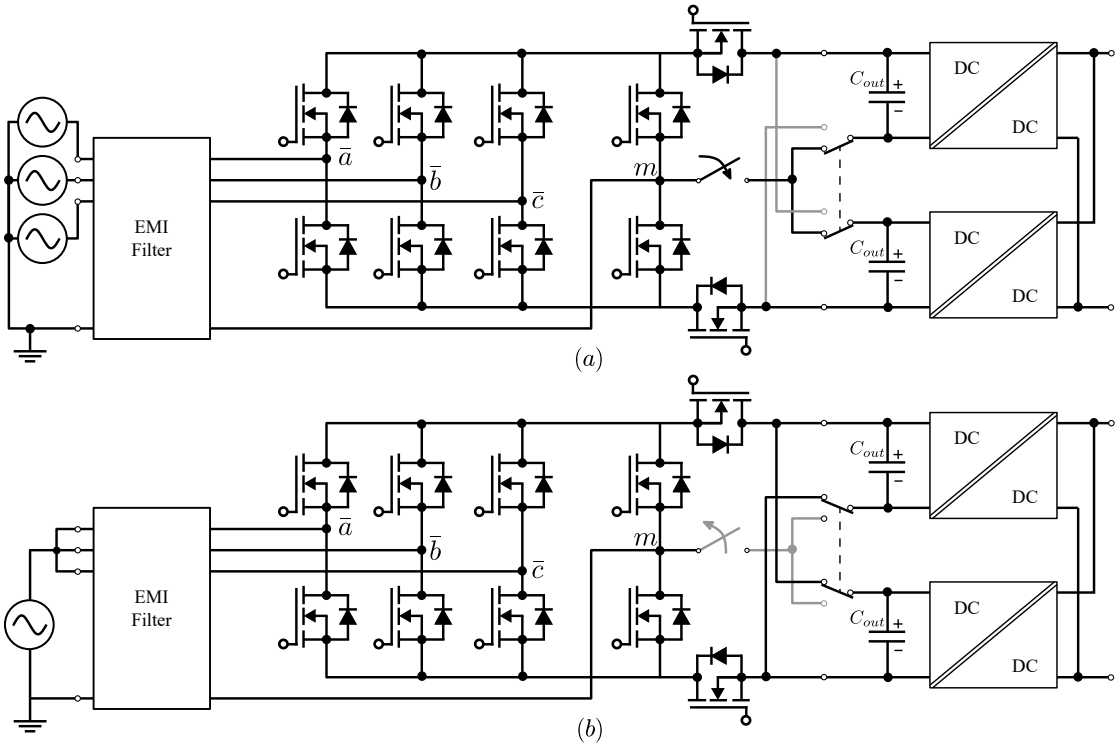

Figure 3.9: Block diagram of the proposed way of how the output capacitor and isolated DC-DC converters are switched for (*a*) three-phase operation and (*b*) single-phase operation. Adapted from [9] and applied for the BePFC rectifier.

3.5. Component Stresses

The component stresses determine the component selection for the BePFC rectifier. The stresses for the output capacitors consist of capacitor ripple current and the voltage it should be able to handle. The minimum required capacitance can be calculated using eq. (3.14). However, the current ripple in this output capacitor will also affect the choice of the capacitor. For output bulk capacitors, electrolyte capacitors are conventionally used. These capacitors are specified to withstand a maximum current ripple at a defined frequency. The minimum required capacity to handle the capacitor ripple can be calculated with

$$C_{out,min} = ceil(\frac{\hat{I}_{C_{out}}}{i_{AC,R}(2f_{gr})}) \cdot C_r \tag{3.15}$$

where $\hat{I}_{C_{out}}$ is the peak current in the output capacitors, $i_{AC,R}(2f_{gr})$ the recommended current ripple at $2f_{gr}$, and C_r is the capacity of a single capacitor.

For the converter with the steady-state waveform as shown in Figure 3.4*c*, a minimum required capacity based on ripple currents is 10.34 mF, considering the capacitor described in [27]. This capacitor value is larger than the minimum required capacity calculated with eq. (3.14) for the maximum allowed ripple voltage. A higher output bulk capacity results in a smaller voltage ripple at the output. For the voltage rating of the capacitor the peak output voltage of the power converter is considered. Electrolyte capacitors with a voltage rating of 450 V have been selected to function as output bulk. These capacitors are also suitable to be used for the three-phase operation, where the output bulk is switched in series to withstand the higher maximum output voltage of 860 V [11].

The maximum blocking voltages for the semiconductors can be calculated by considering the peak output voltage. These blocking voltages determine which class of semiconductor is suitable, i.e. Si, SiC or GaN. For a hard switching BePFC rectifier it is beneficial to use SiC or GaN semiconductors since the reverse recovery effect of SiC is negligible and even zero for GaN devices [28, 29]. Usually SiC devices are used in high power application, as the BePFC rectifier is. Higher blocking voltage of a semiconductor usually comes with increased switching and conduction losses, as the drain-source capacitance in increased as well as the drain-

source resistance when the switch is turned ON. The selection of the components for the BePFC rectifier not only depends on the single-phase, but also the three-phase operation of the power converter. An overview of the semiconductor blocking voltages is shown in Table 3.1.

Table 3.1: Maximum blocking voltages of the switches used in the BePFC rectifier for both 1-phase and 3-phase operation.

Semiconductor	**Blocking Voltage (1ph)**	**Blocking voltage (3ph)**
$S_{\bar{x}(\bar{a},\bar{b},\bar{c})}$	427.03 V	860 V
$S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$	427.03 V	860 V
$S_{\bar{x}m}$	427.03 V	430 V
$S_{m\bar{y}}$	427.03 V	430 V
$S_{p\bar{x}}$	427.03 V	430 V
$S_{\bar{y}n}$	427.03 V	430 V

Although the switches $S_{p\bar{x}}$ and $S_{\bar{y}n}$ are considered to be constantly ON in single-phase operation, the switches still have to block the output voltage if they are switches OFF. The maximum blocking voltage is dependent on the maximum output voltage of the converter. This output voltage has a small ripple Δv_{pn} which can be calculated with eq. (3.13) for the single-phase operation.

The rms currents of the semiconductors are dependent on the type of modulation, i.e. CCM BCM or TCM. In case of TCM, the reverse current will influence the rms currents of the semiconductors, these rms currents can be estimated with:

$$i_{S,rms} = \sqrt{\frac{1}{T}\int_T i_S^2 dt} \tag{3.16}$$

The **HF switches** consist of $S_{\bar{x}(\bar{a},\bar{b},\bar{c})}$ and $S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$. The maximum blocking voltage of these switches is 860 V for the three-phase operation. These switches are selected to be SiC switches with a blocking voltage of 1200 V, where a safety margin of >25% is considered in case of undesirable oscillations and a single-event burnout (SEB). Switches with a low $R_{DS,on}$ and small output capacity C_{oss} are recommended.

The **LF switches** consist of $S_{\bar{x}m}$ and $S_{m\bar{y}}$. The maximum blocking voltage is 430 V for the three-phase operation. These switches are selected to be SiC switches with a blocking voltage of 650 V, taking a margin of >30% into account. In single-phase operation, the switching losses are neglected for these switches, since the switches switch corresponding to the grid frequency. Switches with a low $R_{DS,on}$ are recommended to use.

The **constant ON** switches consist of $S_{p\bar{x}}$ and $S_{\bar{y}n}$. The maximum blocking voltage of these switches is 430 V for the three-phase operation. These switches are selected to be SiC switches with a blocking voltage of 650 V, taking a margin of >30% into account. The switching losses of these switches are also neglected. Switches with a low $R_{DS,on}$ are recommended to use.

The BePFC rectifier considered for the proof-of-concept has an output power of 19.2 kW in single-phase. The rectifier is implemented by interleaving two three-phase BePFC rectifiers resulting in 6 times interleaving in single-phase. This is done because 3.3 kW is considered to be the sweet spot for a bridge leg [10]. Higher powers for this rectifier topology can be achieved by placing more rectifiers in parallel. A more detailed multi objective optimization for the design of the BePFC is presented in chapter 6.

4

Modelling of the Main Converter Components

4.1. Introduction

Mathematical modelling of power converters and power converter components is a much studied topic [14, 15, 17, 30, 31]. The multi-physics modelling of power converter components forms an important part of the converter modelling. The component models provide estimations on performance indices such as losses, volume, EMI and thermal stresses, depending on the specified design variables. The use of the component models does not only allow to estimate the performance of a single power converter but also allows to run an optimization algorithm to select the optimal design variables of multiple virtually designed converters. The goal of the mathematical modelling and optimization is also to derive a performance trade-off on a set of design parameters, such as for example switching frequency, boost inductor value and the number of BePFC rectifiers in parallel.

In this chapter the mathematical modelling of the BePFC rectifier using Fourier analysis is explained, together with the component specific models of the semiconductors, inductors and filter components. The modelling explained in this chapter forms a basis for the design optimization in Chapter 6.

4.2. Modelling Approach

The modelling of the BePFC rectifier is adapted from the modelling of power converters explained in Section 2.3 (cf. Figure 2.11). The mathematical modelling of the power converter is done using MATLAB. For this work the modelling approach as depicted in Figure 4.1 is used. The modelling is subdivided into a *Global* Design Space, *Component* design space and Performance Space [15]. In the global design space the operating conditions, converter topology and design variables are specified. An example of the global design space for the BePFC rectifier can be found in Table 6.1. The component design space specifies component specific parameters, component material and component design variables. An example of the component design space for the BePFC rectifier of this research can be found in Table 6.2.

In this research two different modelling routines are used. *The first routine* is depicted with the solid arrows. This is the modelling routine for the design considerations of the hardware prototype, of which the design is explained in Chapter 8. The modelling routine estimates the converter performance of the hardware prototype without considering optimization. The component selection is done based on experience of previous PFC rectifier projects complemented with input from the modelling done throughout this research.

First, converter specification have to be specified, such as the input voltage v_i, grid frequency f_{gr}, output voltage v_o, output power P_o and the EMI limitations. With the converter specification, basic analysis of the BePFC rectifier is done and steady-state average waveforms of voltages and currents in the converter are generated as explained in Section 3.3.

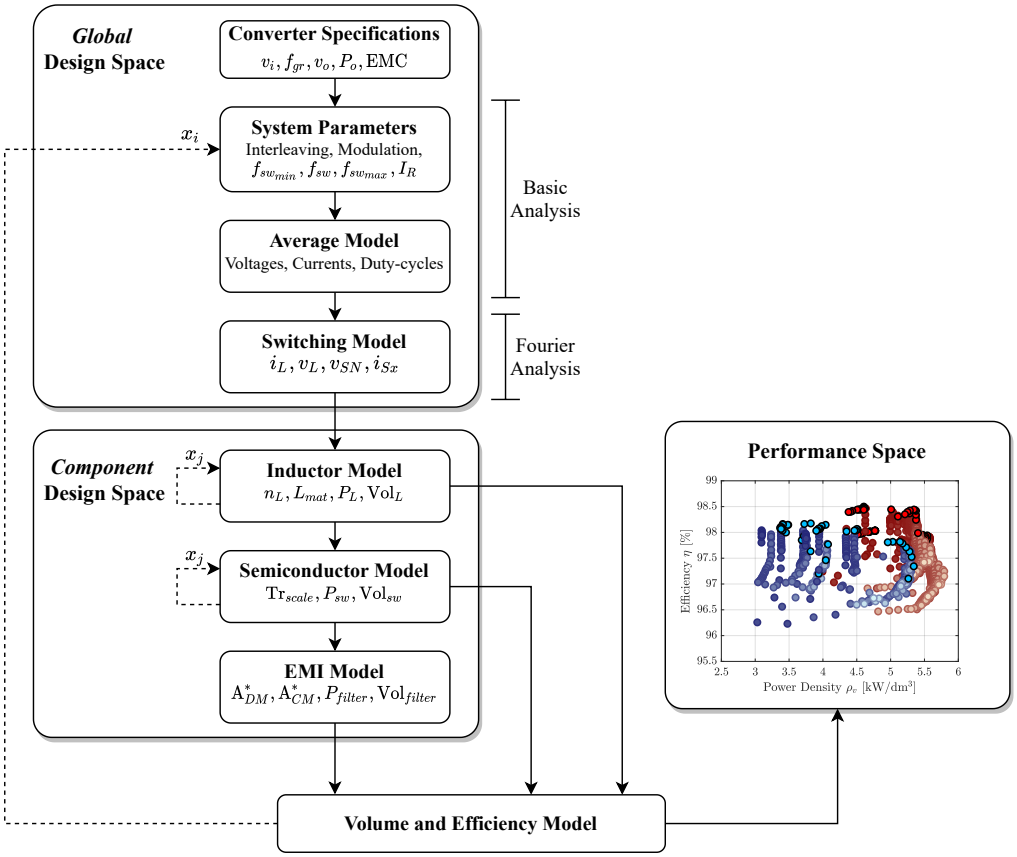

Figure 4.1: Proposed modelling routine adapted from Figure 2.11. The solid arrows correspond to the modelling routine of the hardware prototype. The dashed arrows correspond to the virtual prototyping routine. The global design space is defined by the user input and specifies the number converter design iteration x_i. The component design space defines the number of component design iteration x_j. The volume and efficiency model outputs the system volume and efficiency. Adapted from [15].

The switching model of the power converter is derived using the steady-state average waveforms and Fourier analysis. The Fourier coefficients are derived for the relevant converter components such as the inductor current i_L, switch node voltage v_{SN}, switch current i_{sw} and high frequency output capacitor current i_{C_o}. Describing the switch cycle waveforms in the Fourier domain makes the derivation of the voltages and currents easy, in particular with respect to the modelling of the EMI filters. By performing an inverse Fourier transform, the time domain waveforms can be reconstructed. The Fourier analysis is explained in Section 4.4.

The performance of the main converter components is estimated accordingly based on their switch cycle waveforms and a grid cycle average performance is calculated. The main converter components are the semiconductors, inductors, EMI filter and filter capacitors (e.g. output filter). Each component model gives an estimation of the losses and volume. Detailed component temperature and loss distribution of each component can be obtained within the component specific model. For example the amount of switching losses compared to conduction losses.

When combining the losses and volumes of the converter components in the Volume and Efficiency Model, an estimation of the power converter performance indices is generated.

The second modelling routine is referred to as the virtual prototyping routine, corresponding with the dashed arrows in combination with the solid arrows in Figure 4.1. This routine calls sequentially the Basic Analysis, Fourier Analysis, Inductor Model, Semiconductor Model, EMI Model and Volume and Efficiency Model for x_i iterations. Each iteration x_i is a new virtual BePFC rectifier prototype of which the losses and volume is estimated. Each iteration of x_j is an optimization of the local component loop. The output of the component model loop is a single design optimized for volume or losses. When all global design parameters have been looped, the performance space is filled with all possible virtual prototypes and their performance indices in order to estimate the Pareto trajectory and select and select an optimal design.

4.3. Basic Analysis

The basic analysis of the 1-phase operation of the BePFC rectifier is done in Section 3.3 and 3.4. The steady state average waveforms are derived using Kirchoff's current and voltage laws, together with the duty cycle derivation. The switching frequency f_{sw} is derived while considering TCM modulation for different output powers as shown in Figure 3.7. The basic analysis can already give a good estimate of the average currents and voltages of the converter. Components can be selected based on the estimated stresses as explained in Section 3.5.

4.4. Fourier Analysis

The Fourier analysis is used to derive the switch cycle waveforms of the currents and voltages in the power converter based on the basic analysis of the BePFC rectifier. From two voltage levels (U_1 and U_2), the duty cycle (d) and a phase-shift (ϕ), a Fourier description of a two level voltage square wave can be derived using the generalized complex Fourier equations [32]:

$$\begin{aligned} x(t) &= \sum_{n=-\infty}^{\infty} c_n e^{jn\omega_0 t} \\ c_n &= \frac{1}{T}\int_T x(t) e^{-jn\omega_0 t} dt, \end{aligned} \tag{4.1}$$

The complex Fourier coefficients c_n of a two level voltage square wave can be described as:

$$c_n = \frac{e^{-j\phi n}}{j2\pi n}[(U_1(1-e^{-j2\pi nd})) + (U_2(e^{-j2\pi nd}-1))] \tag{4.2}$$

where c_n are the complex Fourier coefficients of a double sided spectrum, U_1 and U_2 the two voltage levels, ϕ the phase-shift and d the duty cycle. The derivation of eq. (4.2) can be found in Appendix A.1. The Complex Fourier Series (CFS) requires only to calculate a single coefficient c rather than the conventional a and b coefficients [33].

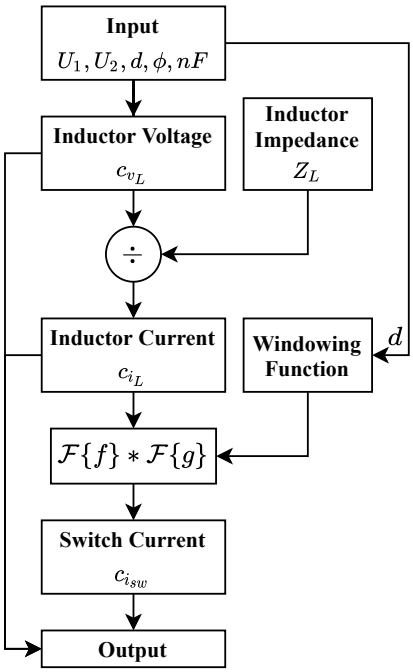

Figure 4.2: The proposed flow diagram for the Fourier analysis to determine the Fourier coefficients of the inductor voltage, inductor current and switch currents.

The Fourier analysis is done according to the proposed diagram shown in Figure 4.2. Equation 4.2 is used to generate the Fourier coefficients of a voltage waveform, i.e. inductor voltage (cf. Figure 4.3). Using the inverse Fourier transform, the time-domain switch-cycle waveform can be reconstructed for the purpose of visualization. Figure 4.3*a* shows an example of the inductor voltage waveform. The inductor current can be easily calculated by a division of the voltage Fourier coefficients by the complex impedance of the inductor, omitting the need for integration. The inductor current can be derived as:

$$c_{i_L} = \frac{c_{v_L}}{Z_L} \tag{4.3}$$

where c_{i_L} and c_{v_L} are the Fourier coefficients of the inductor current and voltage respectively, and Z_L is the complex inductor impedance for each multiple of the switching frequency. These inductor current coefficients can be used to generate a time-domain representation of the inductor current waveform as shown in 4.3*b*.

From the inductor-current Fourier coefficients, the Fourier coefficients of the semiconductor switches can be generated. This is done by representing the time when a switch is conducting by a, so called, windowing function which is one when the switch is conducting and zero otherwise. The convolution of the inductor current Fourier coefficients and the windowing function of the representative switch results in the switch-current Fourier coefficients. This can be described as:

$$\mathcal{F}\{f \cdot g\} = \mathcal{F}\{f\} * \mathcal{F}\{g\} \tag{4.4}$$

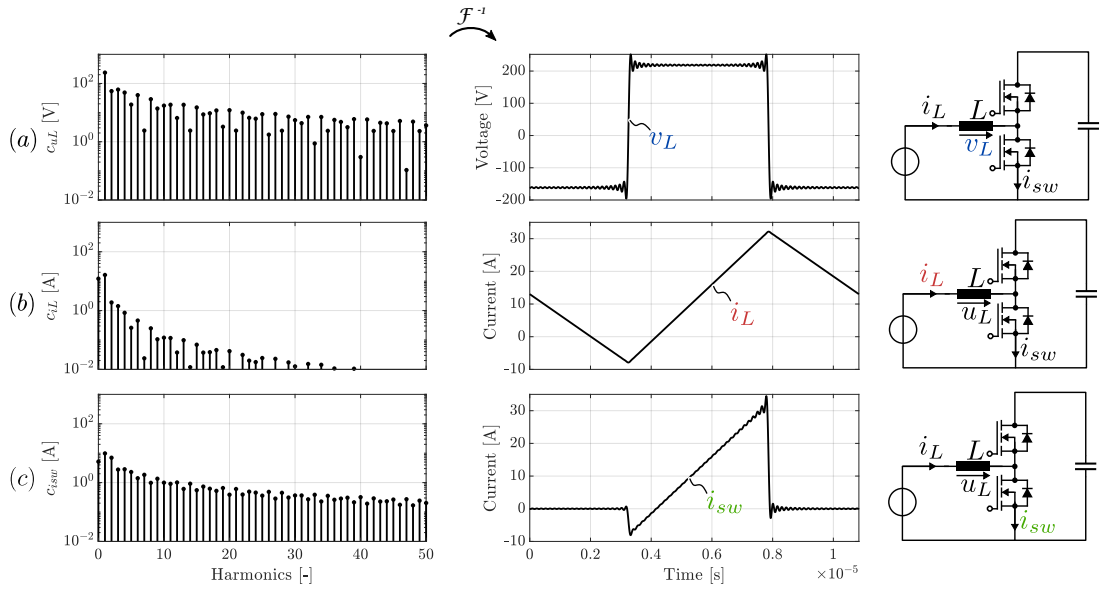

Figure 4.3: Example of the derived Fourier coefficients with corresponding restored time-domain waveforms with (*a*) the inductor voltage Fourier spectrum c_{v_L} and corresponding restored time-domain waveform v_L, (*b*) the inductor current Fourier spectrum C_{i_L} with corresponding restored time-domain waveform i_L and in (*c*) the switch current Fourier spectrum $c_{i_{S_{\bar{a}\bar{y}}}}$ with corresponding restored time-domain waveform $i_{S_{\bar{a}\bar{y}}}$.

From the resulting switch-current Fourier coefficients, the time-domain switch cycle current can be reconstructed as seen in Figure 4.3*c*. Other currents can be derived by summation and/or subtraction of the currents, e.g. output capacitor currents. The capacitor voltage can then be derived by multiplication of the Fourier coefficients with the complex impedance, similar to eq. (4.3)

The rms currents of a switch cycle can be calculated using the following formula in a single sided Fourier spectrum:

$$i_{rms} = \sqrt{c_{i_0}^2 + \sum_{n=1}^{nF} \frac{|c_{i_n}|^2}{2}} \tag{4.5}$$

where nF is the total number of harmonics and c_{i_n} is the Fourier coefficient of the nth harmonic. Similar relation holds for calculating the rms voltages of the switch cycle.

Advantage of using the CFS for the modelling of power converter can be:

- EMI performance can easily be calculated as this is in the frequency domain;
- Currents and voltages can be easily obtained by multiplication or division of the Fourier coefficients by the complex impedance;
- Switch currents can be obtained by a convolution with a windowing function representing the time when the switch is conducting;
- The switch cycle rms currents can be calculated with eq. (4.5) to calculate the HF switch cycle losses [34];
- Compact matrix-form calculations are enabled, gaining speed and memory.

4.5. Component Modelling

Multi-physics modelling is done for the converter semiconductors, inductors and EMI filter components. These component models output the performance indicators in terms of volume, losses and component temperatures. The combination of the component models and design variables defines the total converter performance in terms of efficiency and volume. In the following three sections the modelling of the semiconductors, inductors and EMI filter are discussed including the assumptions made.

4.5.1. Semiconductor Modelling

The modelling of semiconductors is done according to the diagram as shown in Figure 4.4. In the semiconductor losses are calculated until the junction temperate has converged. The size of the cooling area of the semiconductors is scaled in order to lower the junction temperature of the switching device until a pre-defined set-value. The losses in the semiconductors can be subdivided into conduction losses, switching losses and gate driver losses. Each will be discussed accordingly.

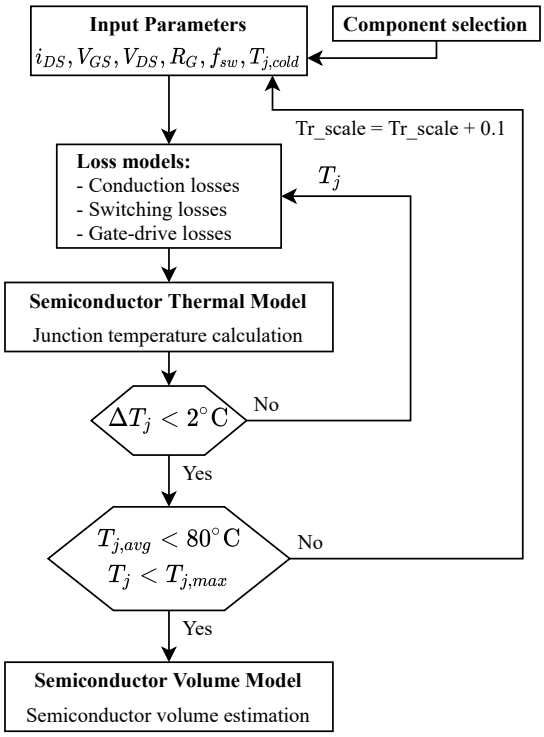

Figure 4.4: The proposed flow diagram for the modelling of the semiconductor devices to calculate the semiconductor losses and volume.

Conduction Losses The switch cycle and average grid cycle conduction losses $P_c(t)$ and $\langle P_c \rangle$ respectively, of the semiconductor can be computed with

$$\begin{aligned} P_c(t) &= R_{DS,on}(i_{DS,rms}(t), T_j(t), V_{GS}) \cdot i^2_{DS,rms}(t)dt \\ \langle P_c \rangle &= \frac{1}{T}\int_T P_c(t)dt \end{aligned} \tag{4.6}$$

where $R_{ds,on}$ is the MOSFETs drain-source on-resistance which depends on the switch cycle rms drain-source current $i_{DS,rms}(t)$, the switch-cycle average junction temperature $T_j(t)$ and the gate-source voltage V_{GS} applied to the switch. A second-order approximation from the MOSFETs datasheet information can be made in order to approximate a generalized fitted formula of the $R_{DS,on}$ with the following variables: $i_{DS,rms}, T_j$ and V_{GS} [14]. From the Fourier coefficients of the switch current, the switch cycle rms currents can be calculated using eq. (4.5).

The influence of the MOSFETs junction temperature and drain-source current on $R_{DS,on}$ is shown in Figure 4.5*a* for a 650 V SiC MOSFET. A higher junction temperature results in a higher $R_{DS,on}$. In Figure 4.5*b* the influence of the gate-source on-state voltage on $R_{DS,on}$ is shown. The gate-source voltage should be chosen as high as possible to lower $R_{DS,on}$ and thereby the conduction losses of the MOSFETs.

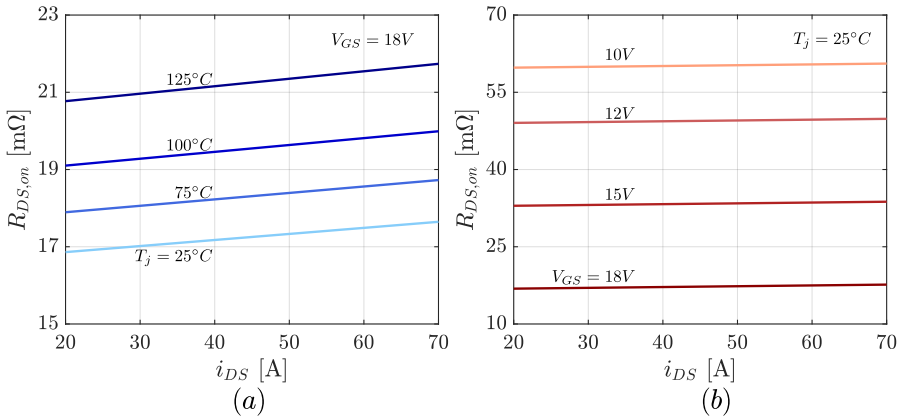

Figure 4.5: Fitted waveforms of the 650 V SiC MOSFET SCTH90N65G2V-7 [35] for (*a*) the drain-source on-state resistance $R_{DS,on}$ versus the drain-source current i_{DS} for different junction temperatures T_j with a gate-source voltage V_{GS} = 18 V and (*b*) the drain-source on-state resistance $R_{DS,on}$ versus the drain-source current i_{DS} for different gate-source voltages V_{GS} with a junction temperature T_j = 25 °C.

The outputs of the conduction losses calculation are the switch cycle average conduction losses and the grid cycle average conduction losses. The switch cycle losses will give an indication of the temperature swing of the junction temperature over a grid cycle, where the grid cycle average losses are used in the steady state efficiency calculation of the converter.

Switching Losses The switching losses of the LF and constant ON switches are neglected. The switching losses of the HF switches in the semiconductor model are calculated with

$$P_{sw}(t) = f_{sw}(t) \cdot [E_{on}(i_{DS,on}(t), T_j, v_{DS}, V_{GS,on}, R_{G,on}) + E_{off}(i_{DS,off}, T_j, V_{DS}, V_{GS,off} R_{G,off})] \tag{4.7}$$

where $E_{on/off}$ denotes the turn-on/off switching loss energies which depend on the switch currents $i_{DS,on/off}$, juction temperature T_j, corresponding operation voltage v_{DS}, gate turn-on/off voltage $V_{GS,on/off}$ and external gate resistor $R_{G,on/off}$.

The total losses for a switching cycle are a combination of the $E_{on/off}$ which also depend on the switching transition, i.e. ZVS turn-on will result in no turn on losses. From the semiconductor datastheet, $E_{on/off}$ functions can be fitted, similar as for fitting the $R_{DS,on}$. The fitted switching loss waveforms of a 1200 V SiC MOSFET are visible in Figure 4.6.

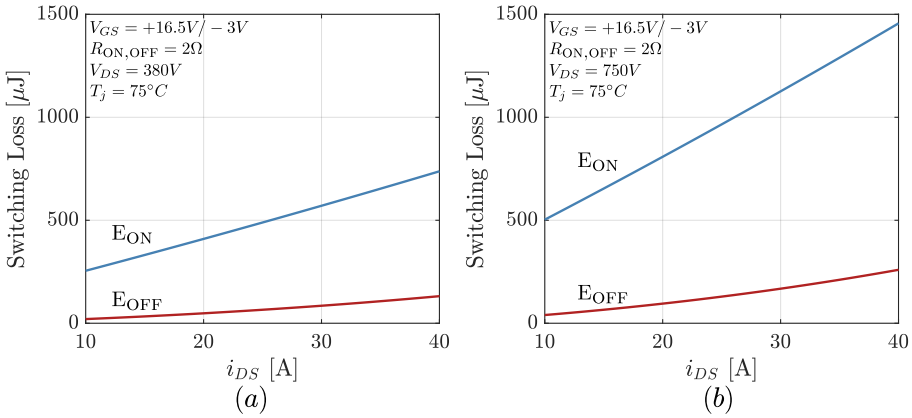

Figure 4.6: Fitted switching loss waveforms of the 1200 V SiC MOSFET SCTH100N120G2-AG [36] for (*a*) a drain-source voltage V_{DS} = 380 V and (*b*) a drain-source voltage V_{DS} = 750 V.

To examine the type of switching transition, two options are available in the semiconductor model:

The first option, the most easy option, requires the least computational power and time of the simulation software. This solution calculates the required reverse current of the complementary switch to be able to ZVS turn-on the switch. The required reverse current is calculated with eq. (3.9). Note that when an additional capacitor C_{par} is placed in parallel to the switch the required charge increases accordingly. This is shown in Figure 4.7*a*. Because there is more charge required, the reverse current increases. For partial ZVS turn-on, a linear approximation is made between the turn-on and turn-off energies of the semiconductor.

The second option, a more advanced option, requires more computational power and time of the simulation software which is undesired for the optimization of a power converter. This option makes use of the Fourier coefficients of the switch current, specified dead-times and varying inductor current and semiconductor output capacitor over time. From the Fourier coefficient, the time-domain waveforms are reconstructed for the period of the switching moment + dead-time. The total charge before and after the switch point is calculated by integration of the inductor current $i_L(t)$, $Q(t) = \int i_L(t)dt$. When the charge equivalent is large enough to discharge the output capacitor of the switch, ZVS is achieved. An example of a complete ZVS transition is visible in Figure 4.7*b*. When there is not enough charge, incomplete ZVS occurs. An example where the charge $Q < Q_{req}$ is shown in Figure 4.7*c*. The inductor current reaches zero before the required charge is reached. The semiconductor turns on at zero current but with a remaining drain-source voltage.

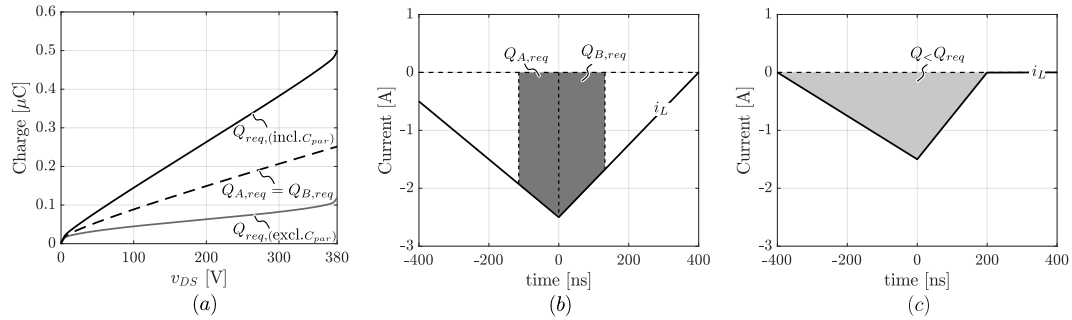

Figure 4.7: (*a*) The required commutation charges for both with and without considering an additional capacitor parallel to the semiconductor switch. (*b*) An example of a ZVS transition where there is enough charge before and after t = 0s for the resonant transition. (*C*) An example of an incomplete ZVS transition where the charge $Q_{B,req}$ is not large enough to completely discharge/charge $C_{oss} + C_{par}$. The dead-time considered is 800 ns.

The outputs of the switching losses calculations are the switch cycle losses together with grid cycle average losses. The average grid cycle losses are used to estimate the converter steady-state efficiency, while the switch cycle losses are used to calculate the grid-cycle temperature swing of the semiconductor junction temperature. The separately calculated turn-on and turn-off losses can be used to verify the soft-switching transitions over a grid cycle of the power converter.

Gate-Drive Losses The gate-drive losses are caused by the energy required to charge the MOSFET gate capacitance. Having a higher switching frequency results in non-negligible gate driver losses. The gate-drive losses of the LF and contant ON switch are neglected because of their low switching frequency. The switch cycle gate-drive losses are expressed in terms of gate charge Q_g, gate-source voltage difference ΔV_{GS} and the switching frequency as:

$$P_{gd}(t) = Q_g \cdot \Delta V_{GS} \cdot f_{sw}(t) \tag{4.8}$$

The gate voltage during during the off-state is −3 V. This is done to avoid unwanted turn-on due to coupling effects. The gate-voltage during the on-state chosen to be high e.g., 18 V, to keep the conduction losses low.

Semiconductor Thermal Model The semiconductor thermal equivalent model is used to estimate the junction temperatures T_j of the switches based on the total switch losses. The losses are calculated starting with a junction temperature of $T_{j,cold}$. T_j is iterated until a thermal equilibrium is reached. The semiconductor thermal model is based on the thermal equivalent model as shown in 4.8*a*. The semiconductor losses are modelled as a current source, the thermal interfaces are modelled as (thermal) resistances. The voltage over a thermal resistor is equivalent to the temperature difference over the thermal interface.

The assumptions made for the semiconductor thermal model are as follows:

- The semiconductor is a surface mount device (SMD) component which is placed on top of a metal core PCB (MCPCB).
- The semiconductor is surrounded by free cooling area which is scaled with the scaling factor Tr_{scale}, a visual explanation of the transistor scaling factor is visible in Figure 4.8*b* .
- The heat is distributed uniformly across the copper foil.
- The cold plate has a constant temperature of 50 °C due to the constant flow of coolant liquid in the cold plate.

The MCPCB consists of a copper foil, an insulation layer and the metal core. The MCPCB is connected to an aluminium heatsink block with thermal paste, having a contact thermal resistance $R_{th,contact}$. The aluminium block is placed on top of the cold plate that extracts the heat. The height of the stack, is defined by the height of the boost inductors because for both devices heat is extracted via the coldplate.

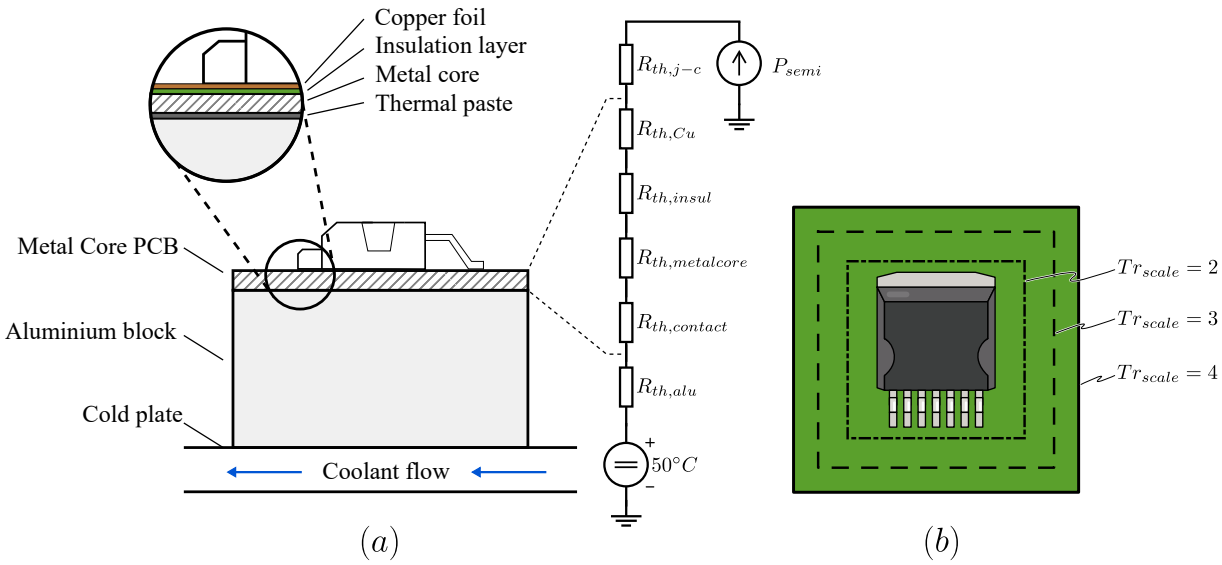

Figure 4.8: (*a*) The semiconductor thermal model with corresponding thermal equivalent model and (*b*) a sketch of the top view of a MOSFET on a metal core PCB with corresponding cooling area which is scaled with Tr_{scale}.

The thermal resistance of the semiconductor package can be derived from the datasheet, specified as the junction-to-case resistance $R_{th,j-c}$. The thermal resistances of the remaining parts depend on the cooling area A, thickness d and thermal conductivity of the material λ and can be calculated as

$$R_{th} = \frac{d}{\lambda \cdot A} \tag{4.9}$$

The thermal modelling of the semiconductors is done until a thermal equilibrium is reached, represented with the block $\Delta T_j < 2\,°C$ in Figure 4.4. When, after reqaching thermal equilibrium the average junction temperature $T_{j,avg}$ is above 80 °C the transistor scale factor is enlarged, as visually explained in Figure 4.8*b*. Enlarging this factor results in a larger MCPCB and alumium block cooling area, thereby lowering the corresponding thermal resistances, except the $R_{th,j-c}$ of the semiconductor. This iterative process is repeated until there is enough cooling for the semiconductor devices. A thermal runaway is detected in the semiconductor model if the scaling factors end up being too large or if the switch cycle junction temperature does not reach equilibrium.

Semiconductor Volume Model The volume model estimates the volume required for the semiconductors including cooling. This is estimated by calculating the boxed volumes of the MCPCB (with semiconductor components on top), the aluminium block and the semiconductor cold plate. The boxed volume can be calculated with

$$V = A \cdot h \tag{4.10}$$

where A is the required area and h is the required height. It is important to take margins in defining the required area and height. The area required is the initial semiconductor area, obtained from the datasheet, multiplied by the transistor scaling factor Tr_{scale}. This scaling factor starts with an offset of 2 because of the required space for routing. Additional height of 10 mm above the semiconductors is taken into account if other PCBs are placed on top.

4.5.2. Inductor Modelling

The modelling of the boost inductors is done following the diagram as shown in Figure 4.9. This flow diagram shows the calculation of the winding and core losses for each switch cycle in a grid cycle. The mathematical calculations used in the inductor model are based on [14, 17, 31, 37, 38] and are explained in this section. The Fourier modelling is an advantageous basis for the modelling of the inductors because the the inductor losses are frequency and waveform dependent. The Fourier coefficients can represent a current and/or flux in the frequency domain, enabling the direct calculation of frequency dependent losses.

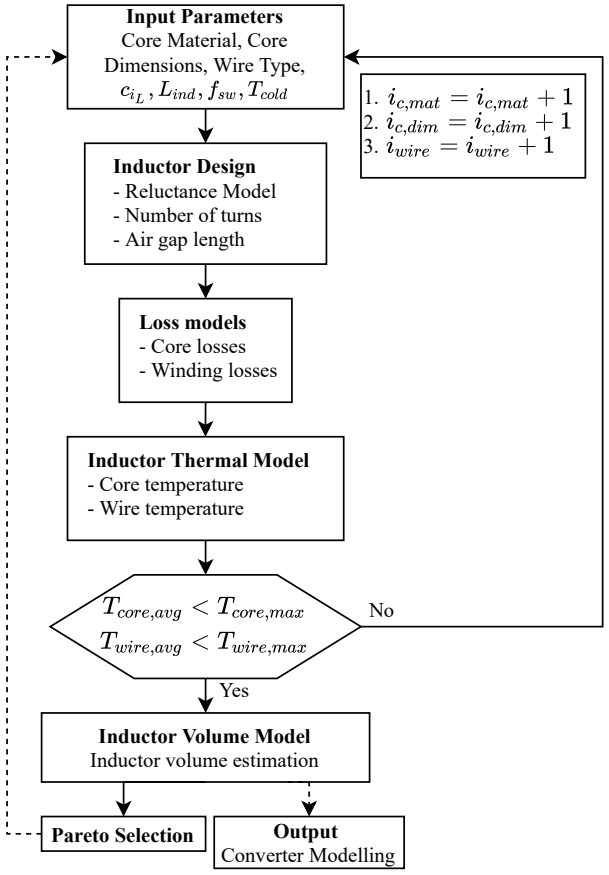

Figure 4.9: Flow chart of the inductor modelling with a design loop indicated with the solid line, the loop makes inductor designs by changing the core material with $i_{c,mat}$, the core dimensions with $i_{c,dim}$ and the wire type i_{wire}. At the end of the design loop the best design is selected. After the design loop the final evaluation loop starts with the designed inductor, indicated with the dashed line. This loop simulates each grid switch cycle to have the losses and volume as output for the converter modelling.

Inductor design When no boost inductor design is specified, an inductor will be designed based on the desired inductance. For the boost inductor design the worst case operation point in a grid cycle is selected as calculating the losses of a grid cycle requires too much computational power and time. After the optimized boost inductor design is selected, the full grid-cycle losses are calculated similar to the single point worst case losses for the inductor design.

The inductor is designed based on a design goal, which can be minimum (boxed) volume or minimum losses. The inductor design is done for a predefined inductor design space consisting of different wire types, core material and core dimensions. For each virtual inductor design, the first step is to generate the reluctance model. The inductance of an inductor with n windings and a total magnetic reluctance of $R_{m,tot}$ can be calculated as

$$L = \frac{n^2}{R_{m,tot}} \tag{4.11}$$

The total reluctance $R_{m,tot}$ is a combination of the core reluctance $R_{m,core}$ and airgap reluctance $R_{m,airg}$ and is calculated according to the methods proposed in [38]. The inductance value is controlled with the airgap length l_g, while the peak flux density $\hat{B}$ should not exceed the maximum flux density $\hat{B}_{max}$ specified in the core datasheet. The limits on the airgap length l_g and maximum flux denisity $\hat{B}_{max}$ result in a minimum and maximum number of turns for the inductor calculated as

$$\begin{aligned} n_{ind,min} &= ceil\left(\frac{L_{ind} i_{ind,max}}{\hat{B}_{max} A_c}\right) \\ n_{ind,max} &= floor\left(\sqrt{L_{ind}(R_{m,core} + R_{m,airg})|_{l_g = l_{g,max}}}\right) \end{aligned} \tag{4.12}$$

The range of possible number of turns $n_{ind,min} < n_{ind} < n_{ind,max}$ defines the number of possible inductor designs where for each design iteration the required airgap l_g for the desired inductance is calculated. The core volume and losses and winding losses calculations define the selection of the optimal inductor design.

Core Losses The core losses can be estimated by the Steimetz Equation (SE) $\overline{P_v} = k f^{\alpha} \hat{B}^{\beta}$ where $\hat{B}$ is the peak flux amplitude, $\overline{P_v}$ is the time-average power loss, f is the frequency of the sinusoidal excitation and k, α, and β the Steinmetz parameters [39]. However, this formula is only applies to sinusoidal exited waveforms. In the BePFC rectifier the boost inductors experience a piecewise-linear current excitation and thus a piecewise-linear flux-time function. The improved Generalized Steinmetz Equations (iGSE) [39], which is consistent with the Steinmetz equation for sinusoidal waveforms has been used in the inductor model for evaluating

the core losses on non-sinusoidal excited waveforms. With the iGSE the core losses, time averaged per unit volume, are calculated as

$$P_{core,v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{4.13}$$

with

$$k_i = \frac{k}{2\pi^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{4.14}$$

The Steinmetz parameters k, α and β are material parameters that are extracted out of data provided by the core manufactures.

Winding Losses It is assumed that the wire used for the inductor is a Litz wire. The winding losses in this Litz wire can be separated into LF and HF losses. The LF losses can be considered as DC losses while the HF losses originate from the higher strand resistance with increased frequency due to eddy currents. These eddy currents can be separated into three loss sources. The first source are self-induced eddy currents with skin-effect losses P_s as a result. The second source are due to an external alternating magnetic field, e.g. external magnetic field H_e from other neighbouring conductors leading to the external proximity effect losses $P_{p,e}$. And the third source are are due to an internal magnetic field H_i produced by the Litz bundle itself, leading to the internal proximity effect losses $P_{p,i}$ [14].

The skin-effect losses of a Litz bundle, per unit length L, can be calculated with [37]:

$$P_{s,L} = n_s \cdot R_{DC,s,L} \cdot F_R(f) \cdot \left(\frac{\hat{I}}{n_s}\right)^2 \tag{4.15}$$

where $\hat{I}$ are the Fourier coefficient amplitudes of the inductor current, $R_{DC,s,L}$ is the per unit length DC resistance of a single stand in the Litz bundle calculated with

$$R_{DC,s,L} = \frac{4}{\sigma\pi d_s^2} \tag{4.16}$$

where σ is the conductivity of the conductor material and d_s the strand diameter. F_R is the skin-effect factor describing the conductor resistance due to skin effect for the corresponding frequencies. This factor is calculated using the proposed formulas in [37].

The per unit length proximity-effect losses, both due to external and internal magnetic fields, can be calculated as shown in [31], with

$$\begin{aligned} P_{P,L} &= P_{P,L,e} + P_{P,L,i} \\ &= n \cdot R_{DC} \cdot G_R(f) \left(\hat{H}_e + \frac{\hat{I}^2}{2\pi^2 d_b^2}\right) \end{aligned} \tag{4.17}$$

where G_R is the proximity-effect factor [37], d_b is the Litz bundle diameter and $\hat{H}_e$ is the peak external magnetic field from the airgap fringing field and in neighbouring Litz bundles, calculated with the 2D analytical approach proposed in [37]. This uses the method of imaging (also known as mirroring) of conducting material in order to estimate the effect of a surrounding magnetic conducting material. The internal magnetic field originating from neighbouring strands in the same litz bundle is modelled as $H_i = \hat{I}^2/(2\pi^2 d_b^2)$. It is assumed that the current is equally distributed over the Litz wire bundle.

Inductor Thermal Model The input for the thermal model are the core and winding losses that are calculated previously in the inductor loss model. For modelling the inductor thermal behaviour, a simplified thermal model is adapted from [40]. For the simplification it is assumed that the inductor bobbin and the inductor core are thermally decoupled. It is also assumed that all cooling of the wires is done via the cold plate with a constant temperature, on which the inductor is placed, as depicted in 4.10*a*. Because of the thermal decoupling, the winding temperature (T_w) and core temperature (T_c) can be computed separately.

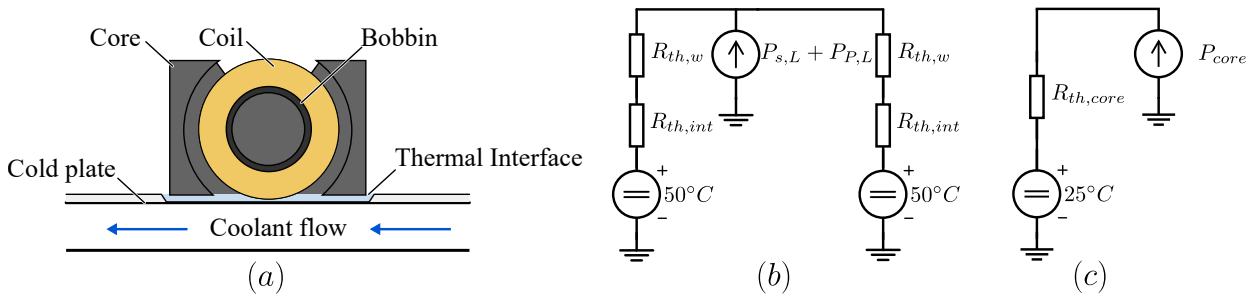

Figure 4.10: (*a*) side view sketch of the inductor with the core, bobbin, coil, thermal paste and the cold plate and (*b*) the electrical equivalent thermal model to calculate the inner winding temperature with cooling via the cold plate and (*c*) the thermal equivalent model of the core with cooling of the core surface via the ambient air.

For calculating the core temperate, the thermal equivalent model from 4.10*c* is used. The core temperature can be estimated by

$$T_c = P_{core} \cdot R_{th,core} + T_{amb} \tag{4.18}$$

where the thermal resistance of the core is given in the core datasheet. A smaller core will result in a higher $R_{th,core}$. For calculating the winding temperature, only the worst case wire temperature of the most inner winding is considered because the thermal resistance from the inner wire to the cold plate is the highest. It is assumed that the winding losses are equally distributed over the length of the inductor wire. The thermal resistance of the inner winding can be calculated as shown in [40]

$$R_{th,w} = \frac{l_w \cdot n_L}{\lambda_{cond} A_{cond}} \tag{4.19}$$

where l_w is the mean length of winding turn, n_L is the number of winding layers, and λ_{cond} and A_{cond} are the thermal conductivity and cross-sectional area of the conductor. For the simplification is assumed that there is only a heat flow along the wire length. It is assumed that the distance to the cold plate is equal for both sides of a winding turn. Litz wires are used for the windings, therefore the assumption of the effective cross-sectional area is scaled as

$$A_{cond} = \pi \cdot \frac{d_b \cdot {d_{fill}}^2}{2} \tag{4.20}$$

where d_b is the Litz bundle diameter and d_{fill} is the fill factor.

Inductor Volume Model The inductor volume is calculated based on the core dimensions. It is assumed that the windings of the inductor fit within the core and thus do not add to the inductor boxed volume. The core size is estimated from the datasheet parameters specified by the core manufacturers.

4.5.3. EMI Modelling

An Electromagnetic Interference (EMI) filter is designed in order to comply with regulatory standards, e.g. CISPR 22 Class A/B for conducted emission (CE). The design of this filter is based on a harmonic analysis, using the Fourier modelling approach, of the equivalent common mode (CM) and differential mode(DM) noise sources of the converter, in combination with the filter and line impedance stabilizing network (LISN). Inserting the input filter to the converter has influence on the displacement factor, resonances in the system and a significant influences on the converter volume [41]. Therefore the design and modelling of the EMI filter has to be accurate in to minimize the required converter volume. The design of the DM and CM filter is usually decoupled, i.e. the CM filter is designed after the DM filter. The design of the DM filter is typically more straightforward than the CM filter which is more based on a trial-and-error method [14] as the CM filter is designed based on parasitic assumptions which depend on the physical converter design.

The LISN is used to provide an stable connection between the converter and the test receiver. A simplified equivalent circuit of the LISN according to CISPR 16 is shown in 4.11, which is valid for the mid-to-high-frequency range (150 kHz - 30 MHz). The LISN provides a stable input resistance for this frequency range (R_{LISN} = 50 Ω). The voltage u_{meas} is used for the EMC test receiver. Attached to the LISN is a EMC test receiver to measure the Quasi-Peak (QP). The test receiver is modelled to have a bandwidth of 9 kHz as explained in [41]. In the remaining figures of this work, the LISN is simplified with R_{LISN}.

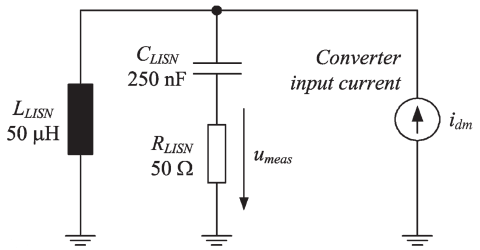

Figure 4.11: Simplified model of the LISN. Valid for the mid-to-high-frequency range (150 kHz - 30 MHz)[41].

Analytically describing the (multi-stage) filters can be complex. A simplification can be made when considering two asymptotes in the magnitude bode plot of a filter stage transfer function [30]. One asymptote corresponds withto low frequencies and a second asymptote corresponds with high frequencies, as depicted in Figure 4.12 for a single stage LC filter. The simplified HF asymptote can be describes as

$$\left| \frac{1}{A_{asymptote}(\omega)} \right| \cong \frac{1}{\omega^2 LC} \tag{4.21}$$

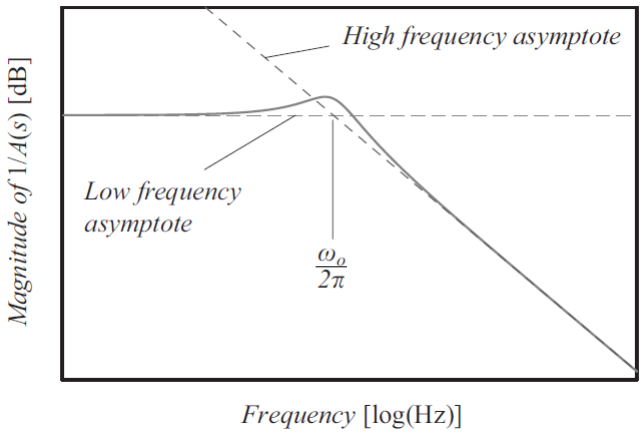

Figure 4.12: Attenuation characteristics of a single-stage LC filter where the high and low frequency asymptote are shown. From [30].

As explained in [30], the multi-stage filter can be considered decoupled from the surrounding ones for frequencies that are high enough. Because of these simplifications a generalized formula, adapted from 4.21, can be used to estimate the filter attenuation as

$$\frac{1}{A_{general}(f)} \cong \frac{1}{K_T} (2\pi f)^{N_L+N_C} \prod_{i=1}^{N_L} L_i \prod_{j=1}^{N_C} C_j \tag{4.22}$$

where the coefficient K_T depends on the filter structure as shown in table 4.1.

Table 4.1: Coefficients K_T for different filter structures.

Configuration	K_T
LC	1
LCL	R_o
CL	R_o/R_{in}
CLC	$1/R_{in}$

DM Filter Model

The interleaved modulation of the BePFC rectifier results in an equivalent DM circuit as depicted in Figure 4.13. The DM noise sources are described in the Fourier domain by the Fourier coefficients of the switch node voltages. Only the frequency multiples equal to $(n_{int}(3k+3)f_{sw})$ are common to all three phases and appear in the LISN, where n_{int} is the number of interleaved BePFC rectifiers placed in parallel. The remaining HF harmonics circulate between the three phases and, in case of an ideally symmetric filter, do not lead to significant voltages at the LISN [9].

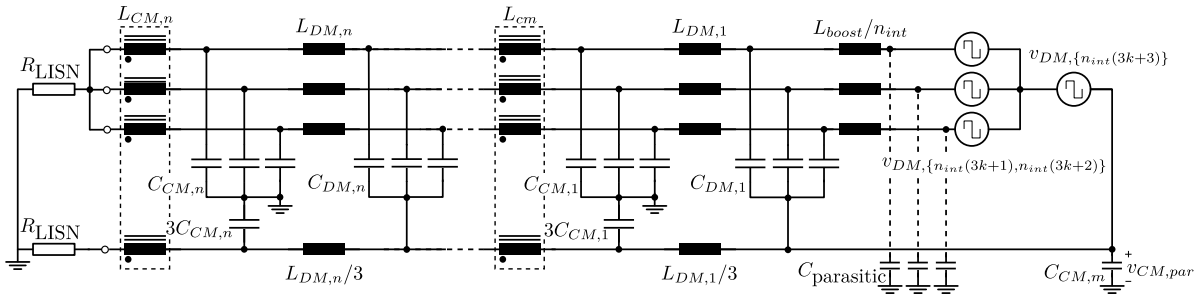

Figure 4.13: HF equivalent circuit with n DM and CM filter stages and the DM noise sources of the BePFC rectifier. Only the frequency multiples equal to $(n_{int}(3k+3)f_{sw})$ are relevant for the DM filter design. Filter damping is not considered for this figure.

The modelling and design of the DM is done according to the flow diagram as shown in Figure 4.15, this flow diagram is later also used for the CM filter design. First the required attenuation is calculated, considering the worst case single phase equivalent circuit as shown in Figure 4.14. The required attenuation is calculated by comparing the CISPR limits (including a margin) with the worst case QP estimation as:

$$\mathrm{A}^*_{DM}[\mathrm{dB}] = U_{QP,DM}(f_D)[\mathrm{dB\mu V}] - \mathrm{limit}_{\mathrm{CISPR}}(f_D)[\mathrm{dB\mu V}] + \mathrm{margin}[\mathrm{dB}] \tag{4.23}$$

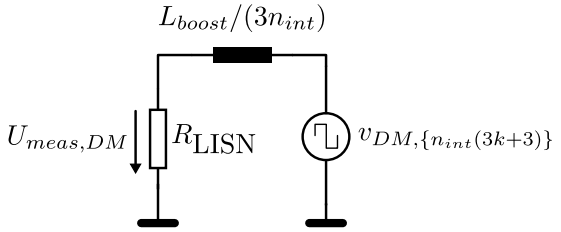

Figure 4.14: Single phase equivalent worst-case differential mode circuit to estimate the required attenuation. n_{int} refers to the number of BePFC rectifiers in parallel.

The frequency f_D is defined as the design frequency for the EMI filter at which the worst case QP occurs within the range of the CISPR limits. Figure 4.16 shows the measured voltage across R_{LISN} including the QP measurement of the DM noise at the design frequency f_D. The required attenuation A^*_{DM} is calculated with a margin of 6 dB. The regulatory limits for the CISPR 22 Class A in the range of 150 kHz - 500 kHz is 79 dBµV and for the range 500 kHz - 30 MHz the limit is 73 dBµV.

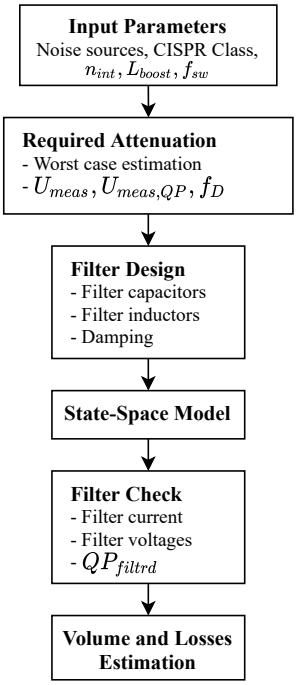

Figure 4.15: Flow chart of the differential-mode and common-mode EMI filter design.

DM Filter Design The DM filter is designed based on the required attenuation at the design frequency. A single stage filter will requires a low cut-off frequency resulting in large filter components, therefore the filter is built up with a two-stage LC filter. The inductor $L_{DM,2}$ of the second stage filter is omitted since the influence on the filter performance measured with the LISN is negligible, the last filter stage is formed by the second stage filter capacitors $C_{DM,2}$ and R_{LISN}. To optimize for volume it has been chosen to go for a multi-stage filter with equal components for each filter stage ($L_1 = ... = L_n$ and $C_1 = ... = C_n$) [42]. Optimizing the filter with respect to volume and using eq. (4.22) results in a minimization function of the DM capacitance C_{DM} as [42]:

$$C_{DM} = \sqrt[3]{\frac{2/3 \cdot k_{L,powder} \cdot I_{max}^2 \cdot 10^{\mathrm{A}^*_{DM}/20}}{3 \cdot k_{c,foil,X2} \cdot V_{max}^2 \cdot R_{\mathrm{LISN}} \cdot \omega_D^3}} \tag{4.24}$$

where $k_{L,powder} = 3.95 \times 10^{-3}\,[\mathrm{m}^3/\mathrm{HA}^2]$ and $k_{c,foil,X2} = 45 \times 10^{-6}\,[\mathrm{m}^3/\mathrm{FV}^2]$ are volumetric coefficients for powder inductors and X2 foil capacitors [43]. V_{max} and I_{max} are the maximum voltage and current ratings of the grid source and ω_D is the design frequency in [rad/sec]. The factor 2/3 and 3 come from the 4-phase filter structure, the derivation of 4.24 can be found in the Appendix A.2. It should be mentioned that in terms of control stability it is preferred to have attenuation of the first filter stage higher than the second filter stage. This suggests that the cutoff frequency of filter stage 1 should be chosen to be smaller than the cutoff of filter stage 2 [44, 45].

The DM capacitance C_{DM} has an upper limited because a large capacitance will lead to a lower initial power factor λ. The maximum capacitance can be calculated for a specified λ at a given minimal active power, as

$$C_{DM,tot,max} = \frac{Q_{max}}{\omega_{gr} \cdot |V|^2} = \frac{\sqrt{(P/\lambda)^2 - P^2}}{\omega_{gr} \cdot |V|^2} \tag{4.25}$$

where Q_{max} is the maximum allowed reactive power, P and λ are the minimum active power and power factor respectively, ω_{gr} is the grid frequency in [rad/sec] and $|V|$ is the maximum rms phase voltage. This total capacitance is evenly distributed over the filter stages. If the C_{DM} capacitance calculated with eq. (4.24) is larger than the limit, the maximum allowed capacitance is selected.

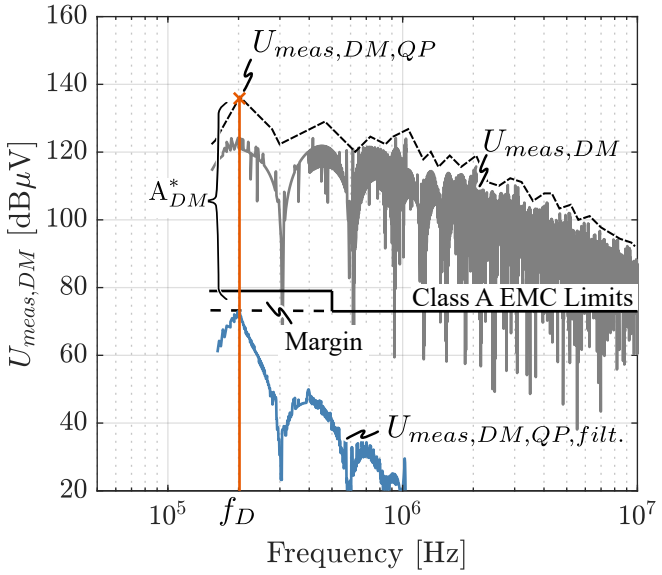

Figure 4.16: Worst case DM noise modelled with the LISN and EMC test receiver for a TCM modulated BePFC rectifier. The dashed line represents the estimated QP noise. The blue line represents the filtered QP noise.

With a known C_{DM}, the value of L_{DM} can be estimated using eq. (4.22) as

$$L_{DM} = \frac{10^{A^*_{DM}/20}}{\omega_D^3 \cdot R_{LISN} \cdot C_{DM}^2} \tag{4.26}$$

The damping of each filter stage is done using series RC damping. The optimal damping resistor for each filter stage can be estimated with the methodology used in [45] and [30] as

$$R_D = \sqrt{\frac{L_{DM_{eq}}}{C_{DM}}} \cdot \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \tag{4.27}$$

where n is the factor between the filtering capacitor C_{DM} and damping capacitor $C_{D,DM}$. In the case for the BePFC rectifier filter they are chosen equal so $n = 1$.

The filter values are put in the state-space model of the filter stages. The currents and voltage in the filter circuit and LISN are estimated in order to calculate if the resulting QPs are below the CISPR limits.

DM Filter Loss Model The losses in the DM inductors are dominated by the LF AC losses. For the DM inductors, a design is generated which uses a design space of a set of toroidal cores with solid copper windings to achieve the required inductance L_{DM}. The design with the lowest volume is chosen, resulting in a wire length and thickness which determine the LF AC resistance. The inductor LF losses can be estimated by

$$P_{L,DM} = 3 \cdot R_{L_{DM,phase}} \cdot i^2_{phase,rms} + R_{L_{DM,neutral}} \cdot i^2_{neutral,rms} \tag{4.28}$$

where $R_{L_{DM,phase}}$ and $R_{L_{DM,neutral}}$ are the winding resistances of the phase and neutral inductor respectively. And $i_{phase,rms}$ and $i_{grid,rms}$ are the phase and grid rms currents where the following relation holds, $i_{grid,rms} = 3 \cdot i_{neutral,rms}$.

High frequency currents lead to losses in the DM capacitor induced by the internal equivalent series resistance (ESR). The filter state space model is able to output the Fourier coefficients of the DM capacitor currents. The capacitors of the first filter stage experience the largest HF ripple and are implemented using X2 electric film capacitor that can handle up to 8 A rms. The ESR losses can be calculated as

$$P_{C,DM} = 3 \cdot R_{\mathrm{ESR}}(f) \cdot i^2_{DM,rms}(f) \tag{4.29}$$

where R_{ESR} is dependent on the noise frequency f and can be extracted from the capacitor datasheet, $i_{DM,rms}$ is the rms current at frequency f generated from the Fourier coefficients using eq. (4.5).

DM Filter Volume model The total volume of the DM filter can be estimate by their peak stored energy and volumetric coefficients as were previously used in eq. (4.24). It is assumed that the stored energy is directly related to the volume similar as explained in [43]. The volume estimation of the filter capacitor and inductor can be done as

$$\begin{aligned} \text{Vol}_C &= k_{F,foil,x2} \cdot C_{DM} \cdot V^2 \\ \text{Vol}_L &= k_{L,powder} \cdot L_{DM} \cdot I^2 \end{aligned} \tag{4.30}$$

For the DM inductor, an optimized design based on volume has been generated for the DM inductor loss calculation, the boxed volume of this design can replace the volume estimation done with the inductor volumetric coefficients. In order to have a good estimate of the filter volume, additional margins are taken for mounting, connections, PCB routing and airflow. A margin of 2.0 is taken to take the required extra space into account.

CM Filter Model

In 1-phase operation of the BePFC rectifier, the LF switching of $S_{\bar{x}m}$ ans $S_{m\bar{y}}$ and $v_{dm,n(3k+3)}$ cause CM noise. The CM noise of the LF switches is resolved by placing a capacitor $C_{CM,m}$. Thus, the CM noise relevant for the input CM filter is caused by $v_{DM,n(3k+3)}$ [9]. The HF equivalent circuit of the BePFC is show in Figure 4.13 where $C_{\text{paracitic}}$ is the parasitic capacitance through a heatsink of the MOSFET, estimated to be 90 pF for a single FET. Estimating the required attenuation for the CM filter is more complex because it considers parasitics which are difficult to estimate and depend on the physical design.

Similar to the DM filter model, the first step is to determine the required attenuation with a worst-case estimation. The equivalent circuit shown in Figure 4.17 is used to estimate the worst-case voltage across the LISN resistor $R_{\text{LISN}}/2$ with $C_{\text{pararasitic}}$ considered. The CM noise source $v_{CM,par}$ is estimated in according to the estimation done in [9] by first replacing the boost inductor by an open circuit and the capacitors of the first DM stage by a short circuit and the DM noise source by its Thevenin equivalent source as

$$v_{CM,par} = \frac{-v_{DM,n(3k+3)} \cdot 3 \cdot n \cdot C_{\text{paracitic}}}{3 \cdot n \cdot C_{parasitic} + C_{CM,m}} \tag{4.31}$$

where n refers to the number of BePFC rectifiers in parallel and $C_{\text{parasitic}}$ is due to the grounded heatsink of the semiconductors. Increasing the value of $C_{CM,m}$ would improve the attenuation, due to the voltage division, but it is limited by the ground leakage current as explained with eq. (4.33). The steps taken to get to the $v_{cm,par}$ noise source is further elaborated in Appendix A.2.1.

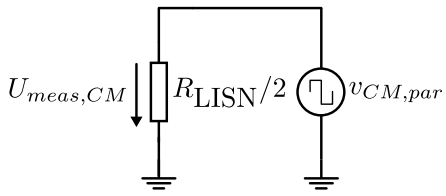

Figure 4.17: Worst-case common mode circuit to estimate the required attenuation.

The measured worst-case voltage $U_{meas,CM}$ across $R_{\text{LISN}}/2$, for a converter with 2 BePFCs in parallel, is shown in Figure 4.18 together with the CISPR 22 class A EMC limits. The required attenuation is calculated from the maximum QP estimation with the CISPR limit as:

$$\text{A}^*_{CM}[\text{dB}] = U_{QP,CM}(f_D)[\text{dB}\mu\text{V}] - \text{limit}_{\text{CISPR}}(f_D)[\text{dB}\mu\text{V}] + \text{margin}[\text{dB}] \tag{4.32}$$

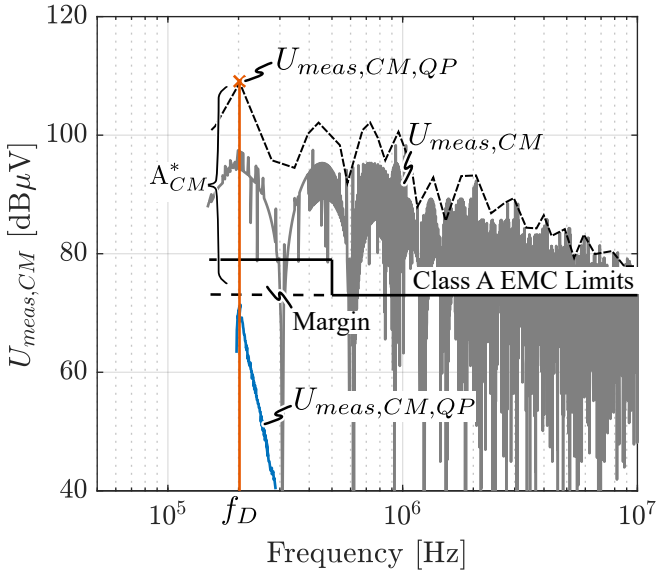

Figure 4.18: Worst case CM noise modelled with the LISN and EMC test receiver for a TCM modulated BePFC rectifier. The dashed line represents the estimated QP noise. The blue line represented the filtered QP noise.

CM Filter Design The CM filter design is restricted by the maximum allowed current to flow though the CM capacitances. The CM capacitance C_{CM} is limited to keep the leakage current towards PE below 3.5 mA at 110% of the input voltage. The limited CM capacitance can be calculated as

$$C_{CM,tot} \geq \frac{I_{PE}}{1.1 \cdot V_{gr,rms} \cdot \omega_{gr}} \tag{4.33}$$

where I_{PE} is the maximum allowed current towards PE, $V_{gr,rms}$ the grid rms voltage and ω_{gr} the grid frequency in [rad/s]. A safety margin is taken in case there are other sources of leakage current towards PE. The maximum total allowed CM capacitance is chosen to be 20 nF. The CM filter is designed to be a two-stage LCLC filter, thus the total CM capacity per filter is stage is 10 nF. The CM filter is designed to be symmetrical, therefore the CM capacitance from neutral to PE is $3 \cdot C_{CM,phase}$ as depicted in Figure 4.13. The capacitors use in the CM filter are referred to as Y1 capacitors to fulfil the safety standards. The CM filter capacitances are designed to have the maximum allowed capacity. Therefore the CM inductance, for a two stage LCLC filter, can be calculated with the HF approximation from 4.22 as

$$L_{DM} = \frac{\sqrt{10^{A^*_{CM}/20}}}{\omega_D^2 \cdot C_{DM,eq}} \tag{4.34}$$

where A^*_{CM} is the required CM attenuation, $C_{DM,eq}$ the equivalent phase capacity and ω_D the design frequency in [rad/s]. The filter component values are put in the state-space model of the CM filter. The currents and voltages in the CM filter can be estimates in order to calculate if the resulting QPs are below the CISPR limits.

CM Filter Loss Model The CM filter losses are dominated by the LF AC conduction losses of the 4-phase CM chokes. A 6-phase CM choke, paralleling 3 phases for the neutral connection, is designed using a design space of a set of high permeability Nanocrystalline toroidal cores with solid copper wire winding to achieve the required inductance. The output of the CM choke design is a wire length and wire thickness of a single phase. The losses of a CM choke can be calculated as

$$P_{L,CM} = 3 \cdot R_{L,phase} \cdot i^2_{ph,rms} + \frac{R_{L,phase}}{3} \cdot i^2_{neutral,rms} \tag{4.35}$$

where $R_{L,phase}$ is the phase resistance, $i_{ph,rms}$ the phase rms current and $i_{neutral,rms}$ the neutral rms current which is related to the phase rms current as $i_{neutral,rms} = 3 \cdot i_{ph,rms}$

CM Filter Volume Model The volume of the CM filter can be estimated using the volumetric coefficient, similar to as is done for estimating the DM filter volume with eq. (4.30). It is assumed that the stored energy is directly related to the component volume as:

$$\mathrm{Vol}_C = k_{F,foil,Y1} \cdot C_{CM} \cdot V^2 \tag{4.36}$$

The volume estimation of the CM choke is done using the CM choke design model. Using the core dimension and wire thickness, a CM inductor boxed volume can be estimated. A margin of 2.0 is taken in order to have enough space for PCB routing, air cooling and mounting, similar to the DM filter volume estimation.

4.6. Total Losses and Volume

The converter components models discussed in this chapter output each the component volume and losses. The component models for inductors, capacitors, semiconductors and EMI filters have the most impact on the total converter volume and efficiency. However, there are also other sub-circuits that have a minor influence on the total losses. Additional losses originate from auxiliary electronics (passive balancing circuits), control electronics (FPGA, microcontroller) and measurement, supply and protection circuits. These additional losses are estimated to be around 25 W. The total converter efficiency is estimated as:

$$\eta_{converter} = \frac{P_i - P_{loss}}{P_i} \cdot 100\,\% \tag{4.37}$$

The total converter volume can be estimated by summation of the converter component volumes and an additional volume required for the sub-circuits that also added the minor losses. Additional volume margins have to be taken above the component specific margins. The additional volume exists due to variables such as, electrical isolation restrictions, mounting restrictions, interconnection restrictions etc. An additional margin of +10 % is taken on the total converter volume. The total converter volume is estimated as:

$$\rho_{converter} = \frac{P_o}{V_{box}} \cdot 100\,\% \tag{4.38}$$

4.7. Summary

In this chapter the modelling routine were explained starting from the the converter specifications, basic analysis, Fourier analysis and component specific models into the full converter efficiency and power density. The proposed modelling routine is further used for the design optimization explained in Chapter 6.

The basic analysis of the BePFC rectifier is used from Chapter 3, and the Fourier analysis is explained using a flow diagram and an example. The main converter models are the semiconductor model, inductor model and EMI model. These multi-physics models of the converter components were explained in detail. Finally, the calculation of the total converter efficiency and volume were described with taking into account the additional losses and required volume when physically designing the power converter.

5

Closed-loop Control

5.1. Introduction

In this chapter the proposed closed loop current controller for the BePFC rectifier is explained together with the interleaving control of the boost rectifier stages. The relevant waveforms from the simulation results are shown together with two different interleaving start-up sequences at every zero-crossing of the source voltage. The relevant results for the simulation are the input current THD, interleaved inductor currents, the source power factor and the current control behaviour. The voltage control behaviour is not considered because the output of the rectifier is connected to a bi-directional supply with a stable output voltage. Table 5.1 lists the converter parameters of the performed simulations of the single-phase BePFC rectifier.

Table 5.1: Simulation parameters of the Belgian PFC rectifier.

Description	**Parameter**	**Value**
Single phase rms voltage	$v_{s,rms}$	240 V
Source frequency	f_s	60 Hz
Output voltage	v_{pn}	380 V
Output power	P_o	11 − 19.2 kW
Inductor current amplitude	i^*_{ampl}	10.80 − 18.86 A
Boost inductance	L_{boost}	25.01 µH
BePFCs in parallel	n_{int}	2
Switching frequency	f_{sw}	40 − 250 kHz
Input current THD	iTHD	< 8%
Input displacement factor	Φ	> 0.99
Input power factor	λ	> 0.99

5.2. Control Scheme

Figure 5.1 shows the proposed (closed-loop) control scheme of the Belgian PFC rectifier for the proof-of-concept tests explained in Chapter 8. This control scheme only considers a current controller as the output is connected to a voltage supply in order to only control the AC input current of the rectifier.

The measured input voltage v_s is an input of phase locked loop (PLL). The PLL locks onto the source frequency and outputs the source frequency f_s, source voltage amplitude $\bar{U}_s$, phase angle θ_s and a normalized input voltage reference REF_s. The REF_s is used to create signal relevant for the current controller, such as the reconstructed source voltage $v_{s,PLL}$ and set current i^*_{set}.

The average inductor current amplitude i^*_{ampl} is an input for the control structure and is chosen based on the desired output power P_o. The measured boost inductor currents i_L are compared with the set-value of the average inductor current i^*_{set} and fed into a (fast inner loop) current PI controller to generate the inductor voltage set-points v^*_L. The duty cycles for the HF switches are calculated based on the output voltage v_{pn} and

average switch-node voltage v_{sn} which is obtained from v_L^* and the measured grid voltage $v_{s,PLL}$.

The switching frequency of the HF bridge legs is calculated as

$$T_{sw}^* = \frac{L_{boost} \cdot 2 \cdot (|i_{set}^*| + \hat{I}_R^*)}{|v_{ctrl}|} + \frac{L_{boost} \cdot 2 \cdot (|i_{set}^*| + \hat{I}_R^*)}{|v_{ctrl}| - v_{pn}}$$
$$f_{sw}^* = \frac{1}{T_{sw}^*} \tag{5.1}$$

where $v_{s,PLL}$ is the measured source voltage, v_{pn} the measured output voltage, i_{set}^* the current set-value and $\hat{I}_R$ the reverse current required to achieve complete ZVS transition considering TCM modulation with a known boost inductor value L_{boost}. The switching frequency set-value f_{sw}^* is used for the interleaving control of the boost circuits.

The state of the LF bridge leg is defined by the sign of the input voltage $v_{s,PLL}$. A positive input voltage corresponds with $S_{m\bar{y}}$ being turned ON and $S_{\bar{x}m}$ turned OFF and vise versa. Another output of this block is the signal $enable_0$ to disable all the switches when the rectified input voltage is smaller than a certain threshold voltage. Any mismatch in the reconstructed voltage $v_{s,PLL}$ with the original voltage v_s result in current spikes. The disabling of the switches is used to prevent these current spikes.

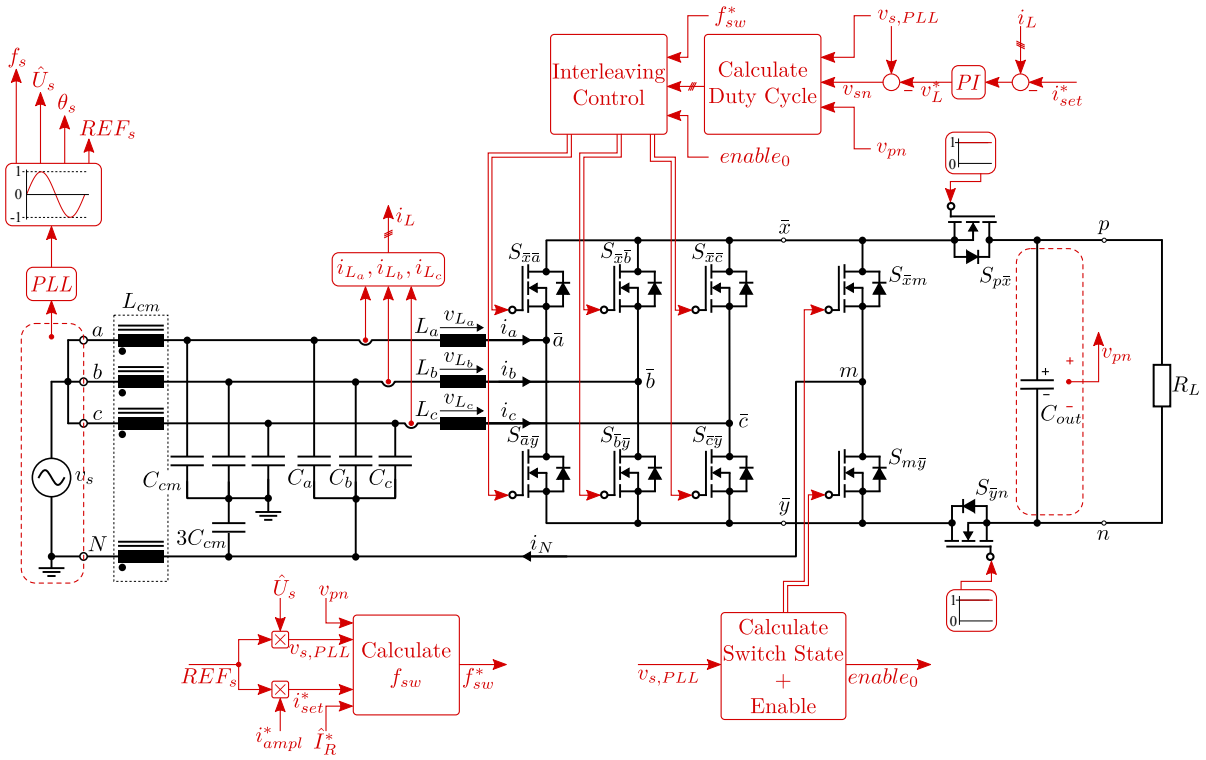

Figure 5.1: Proposed control scheme of the Belgian PFC rectifier. It is assumed that the load will be connected to a voltage supply, therefore no voltage control loop is visible in this figure.

The single-phase BePFC rectifier is controlled using a variable switching frequency, which is difficult to implement for an interleaved converter. This switching frequency is limited as explained in section 3.4. A variable switching frequency in combination with interleaved control results in the need for a correct timing when to update signals in order to keep the interleaved boost circuit synchronized. As explained in [46] and [47] it is important to update the phase shift of the interleaved branches together with the switching frequency. The per unit phase shift between the interleaved branches is calculated as:

$$\phi_{p.u.} = \frac{1}{n} \tag{5.2}$$

where n is the number of interleaved branches.

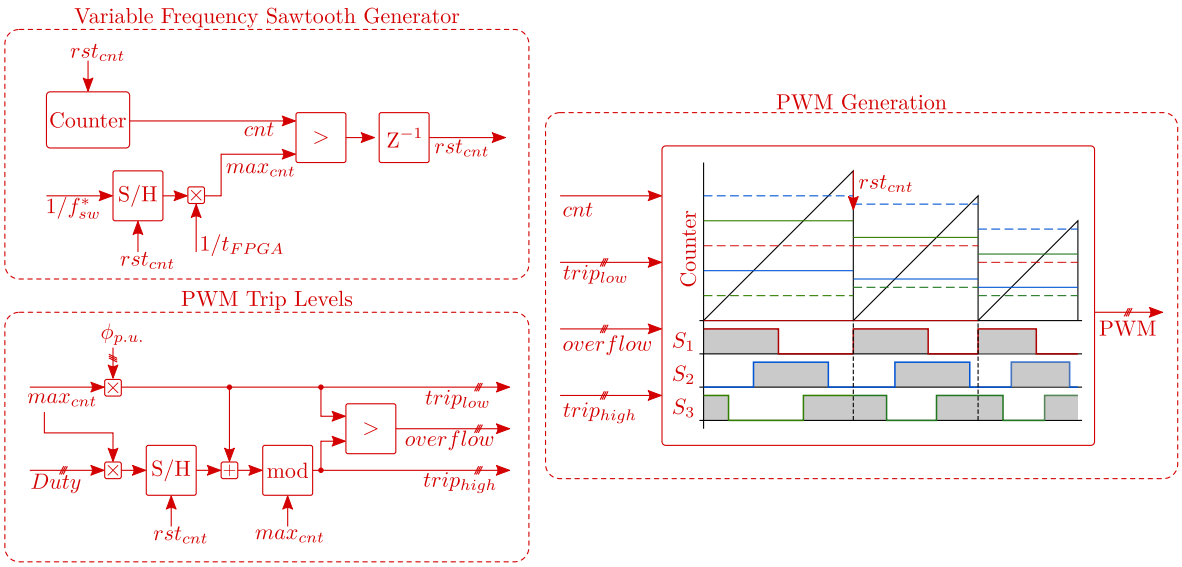

Figure 5.2: Interleaving control block of the proposed Belgian PFC rectifier control scheme as shown in Figure 5.1.

The interleaved control block is further explained using Figure 5.2. This figure consists of three blocks, of which the first one is the *'Variable Frequency Sawtooth Generator'* block. The counter counts with every controller clock cycle t_{FPGA} until it gets a reset from rst_{cnt}. The maximum value of the counter max_{cnt} depends on the set-value of the switching frequency f^*_{sw}. The delay Z^{-1} on the reset signal is to not make the input directly dependent on the output. It is important that the set-value of the switching frequency is processed via a sample and hold block.

The second block is the *'PWM Trip Levels'* block. In this block the trip levels for the PWM generation are calculated using the max_{cnt}, phase shift vector ϕ and duty cycles. If the $trip_{low}$ level is higher than the $trip_{high}$ level, an overflow will be detected and the low and high value are interchanged. Again it is important to process the scaled duty cycles using a sample and hold block. The switching frequency, phase shift and duty cycles are now updated simultaneously using rst_{cnt}.

The third block is the *'PWM Generation'*, in this block the PWM generation for three switches S_1, S_2 and S_3 is visually explained using the solid and dashed line trip levels. The rst_{cnt} is triggered together when the max_{cnt} is reached, corresponding to the period of S_1, making the PWM generation of S_1 the master. The slave synchronisation of the slaves S_2 and S_3 goes together with the update of the counter, possibly resulting in a slight change of the ON time, especially for the last slave. However, this mismatch is controlled with the current controller loop.

5.3. Simulation Results

The simulation of the BePFC rectifier is done using Simulink/PLECS. It is assumed that the output of the rectifier is connected to a voltage source with load, therefore no voltage control is performed. Figure 5.3 show the simulation results for the rectifier using the control scheme from Figure 5.1. The simulation parameters are listed in table 5.1. The average inductor current amplitude i^*_{ampl} is an input for the current controller which can be changed during the simulation. For the simulation results in Figure 5.3, i^*_{ampl} is switched at 50 ms from 10.80 A to 18.86 A corresponding to a jump from 11 kW to 19.2 kW considering an ideal converter where $P_{in} = P_o$. In Figure 5.3*a* a single $enable_0$ signal is considered to disable and enable all the switches around the zero-crossing of the AC grid voltage. It can be seen in the zoomed version of the inductor current that the switches are turned OFF prior to the simultaneous turn ON of all switches. This results in distorted out of sync inductor currents. This current distortion is solved by implementing a start-up sequence of the switches based on the $enable_0$ signal as visible in Figure 5.3*b*. The inductor currents start now in sync resulting in an improved THD at the AC input.

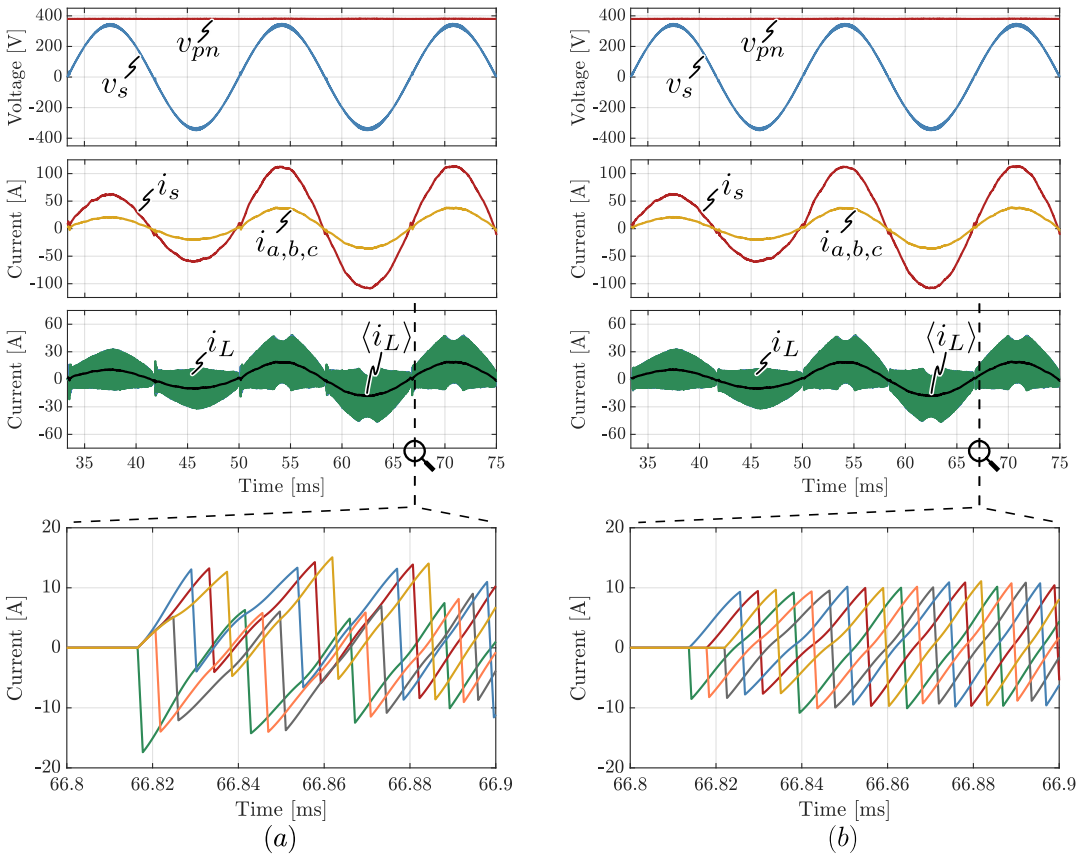

Figure 5.3: Simulation results of the Belgian PFC rectifier in simulink/PLECS using the proposed control scheme of Figure 5.1 and parameters as listed in Table 5.1. (*a*) shows the simulations where a single $enable_0$ signal is used based on the zero-crossings of the source voltage and (*b*) shows the improved simulation results where a start-up sequence for the interleaving boost control is used based on the $enable_0$.

The effect of limiting the switching frequency is visible in the simulation results corresponding to the 19.2 kW simulation t = 50 ms - 75 ms. The switching frequency for this simulation is limited to [40 kHz - 250 kHz]. It is visible that the reverse current of the inductor current i_L is limited resulting in a different current waveform than for the 11 kW simulation.

The fundamental of the current waveform of i_s and voltage waveform v_s are used when determining the displacement factor of the converter. The displacement factor for the simulations is $\Phi > 0.99$ with an output power of 19.2 kW. The THD is estimated based on the current waveform i_s and equals < 8% in both simulations. However the simulation with the 'start-up sequence' shows a 0.3 % lower THD. The THD in combination with the displacement factor Φ contribute to a power factor $\lambda > 0.99$ for the simulations.

5.4. Summary

This chapter proposed the control structure of the single-phase BePFC rectifier. The calculation of the switching frequency were explained including the interleaved control with a variable switching frequency. The control scheme contains only a fast current controller loop as it was assumed that the proof-of-concept hardware prototype is connected to a stable voltage supply and load at the output. Simulation results were provided in which the disabling of the switches, with every zero-crossing of the supply voltage, is showed together with switching frequency limiting and the enabling pattern of the switches. The improved switch enabling pattern showed better THD performance.

6

Design Optimization

6.1. Introduction

The proposed modelling techniques of chapter 4 and proposed modelling routine of Figure 4.1 are used to estimate the losses and volumes of multiple virtual BePFC rectifier designs in order to find an optimal design with respect to the converter efficiency and power density. The global and component design space, specified in this chapter, are chosen such that the the most optimal designs are expected to follow. Furthermore, the relevant parameters are discussed to explain the influence on the simulation results.

Each design iteration calculates the converter performance in order to come with a design that is valid for the full required operating range. A simulation optimization is implemented to not further simulate designs that already show a design failure during simulation, thereby improving the simulation time. The final design space is then mapped onto the performance space which visualizes the dependency on the global and component design spaces. The performance space results in a set of Pareto-optimal designs of which a Pareto-trajectory can be extracted. The most optimal design can be selected from the performance space based on the desired weighting factors of the efficiency and power density.

6.2. Methodology

The design optimization of the 22 kW Belgian PFC rectifier is done according to the proposed modelling routine of Figure 4.1 using the modelling techniques that are further explained in chapter 4. For the design optimization it is assumed that the converter is connected to a three-wire split-phase USA grid with a frequency of 60 Hz and a maximum rms current of 80 A resulting is a maximum output power of 19.2 kW. Furthermore, it is assumed that the nominal output voltage is 380 V or 750 V. The global design space, based on the requirement of table 1.1, is given in Table 6.1. Four design parameters that have a large influence on the performance space are left variable. The *first* parameter is the output voltage range which can either be 350 - 420 V with a nominal output voltage of 380 V, or 450 - 800 V with a nominal output voltage of 750 V. The voltage range defines the component selection based on its voltage levels and influences the switching frequency when TCM modulation is considered. The *second* parameter of influence is the switching frequency. The switching frequency can either be variable, using TCM modulation as explained in section 3.4, or it can have a constant switching frequency resulting in (possible) hard switching for higher frequencies but a smaller inductor current ripple. The *third* parameter of influence is the boost inductance value, which defines the peak-to-peak inductor current ripple. The *fourth* parameter is the number of interleaved BePFC rectifiers. All these four parameters have an influence on the EMI filter volume. The last three design parameter vectors are chosen as:

$$f_{sw} \in \{variable, 24, 30, 36, 42, 48, 54, 60, 66, 72, 78, 84, 90, 96, 102, 114, 126, 144, 160, 180\}\text{[kHz]}$$
$$L_{boost} \in \{5, 10, 15, 20, 25, 30, 35, ...120, 125, 130, 135, 140, 145, 150\}\text{[µH]}$$
$$n_i \in \{1, 2, 3\}$$

The indicator $variable$ in the switching frequency vector refers to the variable switching frequency which follows from using TCM modulation as shown in Figure 3.7. This variable frequency is limited with a lower and higher limit as $f_{sw,min}, f_{sw,max}$. In the global design the number of transistors in parallel is also specified and seems to be variable. However, this value is fixed at the start of the simulation based on output voltage and number of interleaved rectifiers. It can be selected to place transistors in parallel for all HF bridge legs, and/or the combination of the LF with the constant ON switches.

Table 6.1: Global requirements and design space for the optimization routine of a 22 kW BePFC rectifier.

Description	**Parameter**	**Value**
Single-phase mains voltage	$v_{s,rms}$	240 V
Mains frequency	f_s	60 Hz
Output power	P_o	19.2 kW
Power factor at full load	$\lambda_{100\%}$	0.99
Power factor at 20 % load	$\lambda_{20\%}$	0.95
Earth leakage current	$i_{PE,leak}$	3.5 mA
EMI compliance	-	Class A
Output voltage	v_{pn}	350 - 420 V
	v_{pn}	450 - 800 V
Nominal output voltage	$v_{pn,nom}$	380 V , 750 V
Switching frequency	f_{sw}	20 - 180 kHz
Switching frequency limits	$f_{sw,min}, f_{sw,max}$	20 kHz, 300 kHz
Boost inductance	L_{boost}	5 - 150 µH
Interleaved BePFC stages	n_i	1-3
Transistor parallel	$Tr_{par,HF}, Tr_{par,LF}$	1-3

Component specific design parameter such as the semiconductor selection, inductor core material, cooling design etc. are specified in the component design space. The component design space for the Belgian rectifier is listed in Table 6.2. The voltage rating of the semiconductors is dependent on the three-phase BePFC rectifier. It is required for the HF semiconductors to be implemented with 1200 V SiC MOSFET. The LF and constant ON semiconductors show the possibility of implementing with either 1200 V or 650 VMOSFETs depending on the single-phase nominal output voltage. SiC MOSFETs with lower voltage rating show in general a better results with respect to conduction and switching losses.

The inductor core dimensions contribute to a large portion of the total converter volume. The inductor can either be designed based on optimizing for power dissipation, usually resulting in the largest core size, or optimizing for volume. The inductor design optimized for volume results in a good compromise between the inductor volume and losses. The core geometry is chosen to be the PQ range because of the availability and to limit the design space. The wire type of the boost inductor ia s fixed to Litz wire because of the expected reduction in skin effect losses at the defined switching frequencies. The strand diameter for the boost inductor design is chosen based on the switching frequency of the global design loop.

Both the boost inductors and MOSFET board are cooled via the coldplate. The difference in height between both components is bridged with an aluminium block to thermally couple the MOSFET board with the coldplate. The cooling design for the power converter is defined to be scalable as explained in section 4.5.1. The size of the heatsink is iteratively increased until all semiconductor steady-state average junction temperature are below the specified 80 °C.

The DM input filter is designed based on an automated design as explained in section 4.5.3. This *CLC* filter design is an optimization based on volume of the filter components. The automated design of the CM filter is explained in section 4.5.3. The CM filter component values are calculated based on the required CM attenuation to meet the CISPR limits, starting from the limited capacitance to PE due to the leakage current constraint. The output DM filter is a fixed design. The output bulk capacitor is designed based on the voltage ripple requirements of the converter in combination with the current ripple and operation voltage rating. Capacitors rated for 450 V are considered, and placed in series when required.

Table 6.2: Component design space for the optimization routine of a 22 kW BePFC rectifier.

Component	**Selections**	**Note**
HF Semiconductors	SCTH100N120G2AG	1200 V SiC MOSFET
LF Semiconductors	SCTH90N65G2V-7	650 V SiC MOSFET
	SCTH100N120G2AG	1200 V SiC MOSFET
Constant ON Semiconductors	SCTH90N65G2V-7	650 V SiC MOSFET
	SCTH100N120G2AG	1200 V SiC MOSFET
Magnetics	∈{PQ50/50, PQ60/42, PQ60/52, PQ65/44, PQ65/54}	Core sizes
	∈{N87, N92, N97, N95}	Core material
	Litz Wire	Wire type
	∈{0.05, 0.071, 0.1, 0.2, 0.355} [mm]	Strand diameter
	Optimize for Power(P)/Volume(V)	Optimization
Heatsink	Aluminium thickness + Coldplate (50 °C)	Scalable design
Input EMI filter	DM: *CLC* filter	Automated design (sec. 4.5.3)
	CM: *LCLC* filter	Automated design (sec. 4.5.3)
Output EMI filter	DM: *LC* filter	Fixed design
	Bulk Capacitors	Scale with output voltage

The size of the global and component design space have influence on the simulation time of the virtual prototyping routine. Enlarging the global design space results in more virtual designs of the power converter. However, enlarging the component design space results only more design options for the component but only a single optimal design is chosen per global design iteration. The component design space is limited to be able to generate a good amount of power converter design within a reasonable simulation time.

Each virtual power converter design should be able to work for the full required operation range. Therefore, the modelling of each virtual prototype is done in three steps:

1. Simulate lowest output voltage
2. Simulate highest output voltage
3. Simulate nominal output voltage

The two extremes of the output voltage range are simulated in the first and second step order to obtain the scaling factors and component values for the output voltage range. At last the power converter is simulated for the nominal output voltage using the maximum of each scaling factor and component value of the first two simulations. The estimation of the converter efficiency and volume is calculated based on the final design at nominal output voltage and mapped onto the performance space.

The modelling of the three output voltage set points is optimized to limit the total simulation time. When in the first or second step of the simulation shows a thermal limit or invalid (component) design, the simulation loop is interrupted and moved to the next iteration starting again with step 1. This simulation optimization results in a lower total simulation.

The number of grid points, switching cycle points and number of Fourier harmonics have a large influence on the calculation time of a single design iteration, similar to size of the global and component design space. By using the following settings an average execution time per three simulations (for the voltage range) of 40 s is obtained. With a relative tolerance in total efficiency of 0.03 % compared to a simulation with high accuracy.

– Grid cycle points = 100
– Switch cycle point = 150
– Number of Fourier harmonics = 75

With an average of 90 iteration (30 virtual nominal designs) per hour a reasonable performance space can be generated within 8 hours. The design space then contains different design extremes ranging from

low switching frequency with high boost inductance value, to high switching frequency with low boost inductance value and every other possible design in between. Each performance space also contains a series of simulations where a variable switching frequency can be obtained using TCM modulation for different boost inductor values. The performance space should be able to show a good comparison based on the global and component design space to draw conclusions for more detailed design optimization with a limited design space. A more detailed simulation with higher accuracy can be done on this limited design space.

6.3. Optimization Results

The design optimization is done using the virtual prototyping routine of Figure 4.1 and the global and component design spaces specified in this chapter. In Figure 6.1 the performance space, with Pareto-trajectory line, is shown for different design iteration in the design space. The sub-figures show each the power density vs. efficiency for three different interleaved variants, $n_i = 1,2,3$, with two nominal output voltages. A Pareto-trajectory line is indicated for a group of designs with the same colour, which corresponds to the nominal output voltage. This is a line from the low power density - high efficiency towards high power density - lower efficiency designs. The Pareto-optimal design with a high efficiency and high power density could be found in the 'knee-point' of the Pareto-trajectory after which the trajectory goes to lower power density - lower efficiency designs. The trajectory follows this path because a lower efficiency usually requires more cooling and therefore the power density decreases. There are no design possible below this part of the Pareto-trajectory line because of the thermal limit.

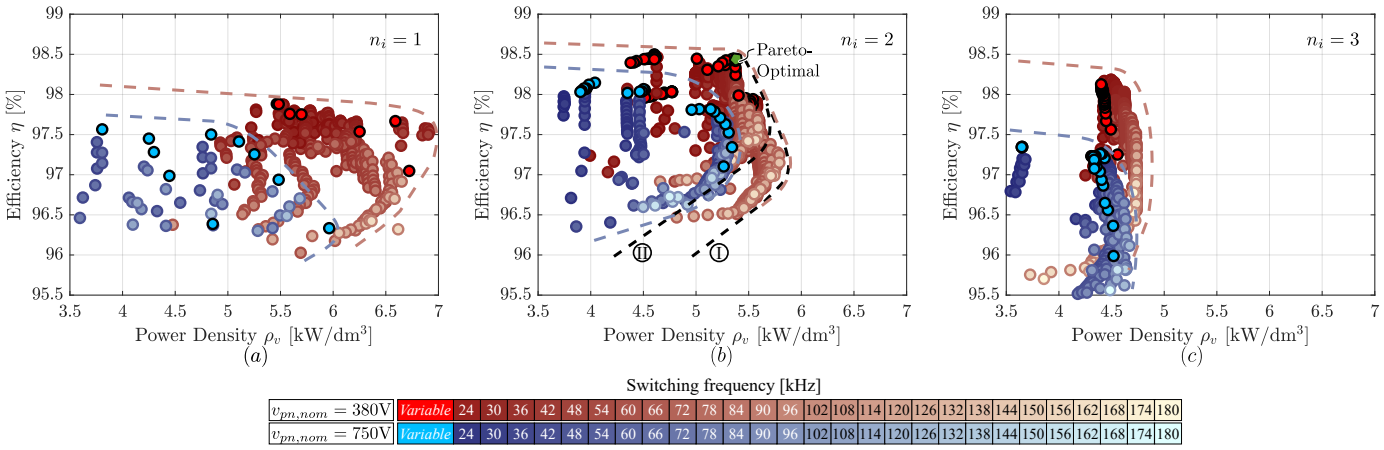

Figure 6.1: Power density vs. efficiency Pareto front for the single-phase BePFC rectifier with global design parameters as listed in Table 6.1. The Pareto-trajectory is shown for two different nominal output voltages, namely 380 V and 750 V. (*a*) Single parallel $n_i = 1$ BePFC rectifier implementation (3x interleaved), (*b*) double parallel $n_i = 2$ BePFC rectifier implementation (6x interleaved), (*c*) three parallel BePFC rectifier $n_i = 3$ implementation (9x interleaved).

When investigating the Pareto-trajectories for the three interleaved variants, one can observe that the designs with $v_{pn,nom} = 380\,\text{V}$ (in *red*) show an overall higher efficiency compared to the $v_{pn,nom} = 750\,\text{V}$ designs (in *blue*). This is mainly due to the fact that the lower voltage designs are implemented with lower voltage rated SiC MOSFETs (650 V SiC MOSFETs (SCTH90N65G2V-7 [35]). This semiconductor has a lower $R_{DS,on}$, as well as turn-on and -off losses, compared to the 1200 V MOSFET. Therefore, the power converters with a nominal output voltage of 380 V are selected as the preferred design.

The interleaved variant with $n_i = 1$ (Figure 6.1*a*) allows for the highest power density as there are only three boost inductors in the design. These designs show the highest power density when implemented with only a single transistor in parallel for the HF bridge legs. The efficiency is a little improved when implemented with 2 transistors in parallel for the HF bridge legs. The higher efficiency can be obtained because the load is shared over more semiconductor switches, resulting in lower losses.

The interleaved variant with $n_i = 2$ (Figure 6.1*b*) performs well in both power density and efficiency. There are six boost inductors in these designs. Compared to the single interleaved variants, these boost inductors are designed to be smaller, therefore the power density is just slightly decreased. The higher efficiency is achieved because of the ripple cancellation of boost inductor currents resulting in lower losses.

The interleaved variant with $n_i = 3$ (Figure 6.1*c*) performs worst in terms of power density as there are nine boost inductors in the design. It can be observed that the power density range is limited, this can be attributed to the limited component design space, in particular for the boost inductor cores. The boost inductors could be designed with smaller cores resulting in a higher power density. The current designs shown in Figure 6.1*c* would allow for a higher output power increasing the power density. However, all the designs are tested the same output power.

The preferred number of BePFC rectifiers in parallel is selected to be the interleaved variant with $n_i = 2$ showing also the best result for the three-phase BePFC rectifier detailed in [11].

When investigating the Pareto-front of the interleaved variant with $n_i = 2$ ((Figure 6.1*b*) one can observe two dashed black lines (I) and (II). The line corresponding to (I) are designs with a single transistor in parallel for the LF and constant ON switches. It is expected that these designs show a higher power density because there are only 4 LF semiconductor switches ($S_{\bar{x}m}, S_{m\bar{y}}, S_{p\bar{x}}, S_{\bar{y}n}$) required in the design. The line corresponding to (II) are design with a double transistor in parallel for the LF and constant ON switches, resulting in a higher efficiency due to the lower equivalent $R_{DS,on}$, however, also a lower power density because the design consists of 8 LF semiconductor switches. The requirements listed in Table 1.1 require an efficiency >98 % and a power density >5 kW/L, therefore it is preferred to design the BePFC rectifier with $n_i = 2$ with a double transistor in parallel for the LF and constant ON switches.

6.4. Pareto-Optimum Design

In Figure 6.2*a* the Pareto front of interest is shown. As mentioned in section 6.3 the Pareto-front of interest of the single-phase Belgian PFC rectifier has:

- A nominal output voltage $v_{pn,nom} = 380\,\text{V}$
- A design with $n_i = 2$ BePFC rectifiers in parallel (6x interleaving)
- Two transistors in parallel for the LF and constant ON switches

The designs around (II.a) are high efficiency - low power density designs with a low variable switching frequency and a high boost inductance value (100 - 150 µH). The results around (II.b) show a high power density - lower efficiency with a high constant switching frequency (126 – 180 kHz) and small boost inductance value (10 - 25 µH). The designs around (II.c) are designs with both a high efficiency and power density, these designs either have a variable switching frequency (TCM modulation) with low boost inductance value (20 - 40 µH), corresponding with the bright red dots, or a constant switching frequency with high boost value (100 - 150 µH). In particular 24 kHz because the effective frequency $f_{sw,eff} = 6 \times f_{sw}$ obtained in the EMI filter is just below the 150 kHz frequency of the CISPR limits resulting in little attenuation required and thus a smaller EMI filter. To understand the differences in the designs a detailed losses and volume breakdown is done and shown in Figure 6.2*b* and *d*.

The four stars in Figure 6.2*a* correspond to the selected designs for the detailed volume and losses breakdown. When observing the switching frequencies and boost inductor in Figure 6.2*c* one can observe that the green and blue designs both have a variable switching frequency which originates from the TCM modulation as explained in section 3.4. The switching frequency range of the green design is small because of the high inductance value, and is limited because of the lower switching frequency limit as explained in section 3.4.

With Figure 6.2*b* the origin of the losses for the chosen designs can be observed. Evident is that the switch on losses sw_{on} of the blue design are extremely low, this is because of the TCM modulation resulting in almost all ZVS transitions for the HF interleaved boost legs. However, an increase in the conduction losses can be observed because the TCM modulation results in a high peak-to-peak current waveform with increased rms currents. The switching losses of the grey design are high compared to the other designs, this is because the switching losses increase proportional to the switching frequency. The HF current ripple seen by the LF and constant ON switches is low because of the interleaved control, therefore the conduction losses in these switches are almost equal in all designs. The losses in the boost inductor are the highest for the red design, this originates from the boost inductor design with core and wire combination. The large boost inductance requires more number of turns to fit in the same core as the blue design, a thinner wire is used resulting in

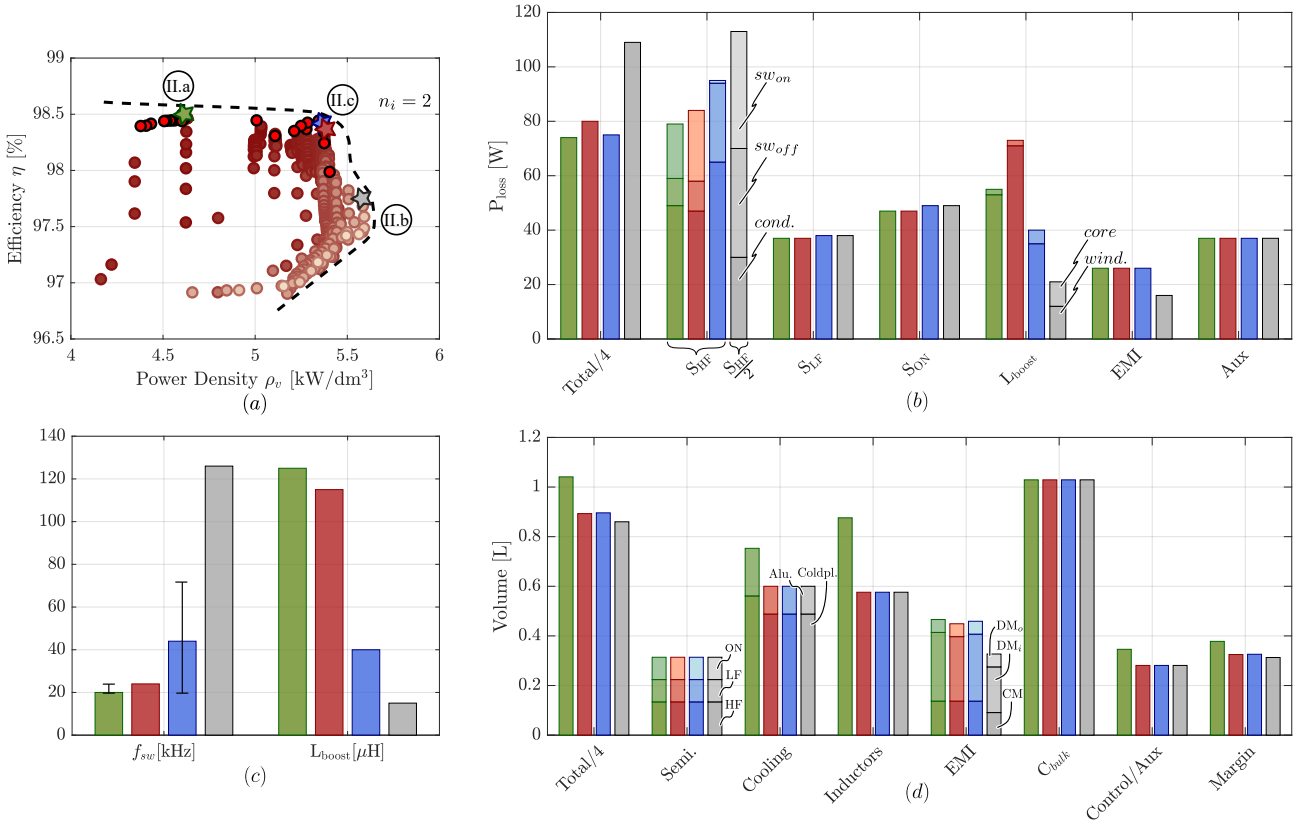

Figure 6.2: (*a*) Pareto front of interest for the 1-phase BePFC rectifier with a double parallel $n_i = 2$ BePFC rectifier implementation (6x interleaved) and two transistors in parallel for the LF and constant ON switches. (*b*) the losses breakdown of four selected designs. (*c*) the switching frequency and switching frequency range with the boost inductance values. (*d*) the volume breakdown of th four selected designs.

higher winding losses. The losses from the EMI filter are the lowest for the grey design as the high switching frequency results in smaller filter components and high frequency losses are obtained. The auxiliary losses are equal for all designs, these are the losses of balancing resistors, control supply circuits and the MPSoC.

With Figure 6.2*d* the volume distribution for the chosen design can be observed. The green design requires the largest inductance and therefore result in a design with a PQ60/52 core. The other boost inductor designs are generated with the smallest PQ50/50 core of the component design space. It is expected that the grey design could have been implemented with a smaller inductor core because the losses are low and only a small boost inductance value is required. A larger boost inductor core size results in a larger cooling volume because the inductor area to be cooling is larger. The filter volume is the lowest for the grey design, the required attenuation is lower because of the high switching frequency. Therefore, the filter can be implemented with smaller components. The volume required for the bulk capacitors is more than 25 % of the total volume, this is the main disadvantage of a high power single phase converter. The required capacitance is such large because of the current ripple limits of these capacitors as explained in section 3.5.

The designs with TCM modulation around the blue star in 6.2*a* are selected as the optimal choice. These designs give both a high efficiency and high power density. Although the current ripple is higher when using TCM, leading to an increase of the conduction losses, the total switching losses are still limited because there are no switch-on losses because of the soft switching transitions. Additionally, the losses in the boost inductors are kept low, the combination of the number of turns and wire thickness result in lower losses compared to the designs with low frequency and high boost inductance (corresponding to the red star). Shifting between hard and soft-switching during normal operation is undesired for the control stability as it is difficult to estimate the type of switching transition for the controller to be able to use deadtime compensation. The optimal boost inductance is selected as 30 µH as a result of the resulting switching frequency range (cf. eq. (3.10)). This range is not limited and therefore results in only soft switching

transitions. The Pareto-optimal design specification are listed in Table 6.3 with the corresponding losses and volume distribution in Figure 6.3 and schematics in Figure 6.4. The optimal design results in an efficiency of 98.42 % with a power density of 5.34 kW/dm^3. Evident is that the HF semiconductor contribute the most to the total converter losses and that the output bulk capacitors contribute the most to the total volume of the power converter. This volume of the output bulk could be reduced by utilizing an active pulsating power buffer which could be relevant for further research.

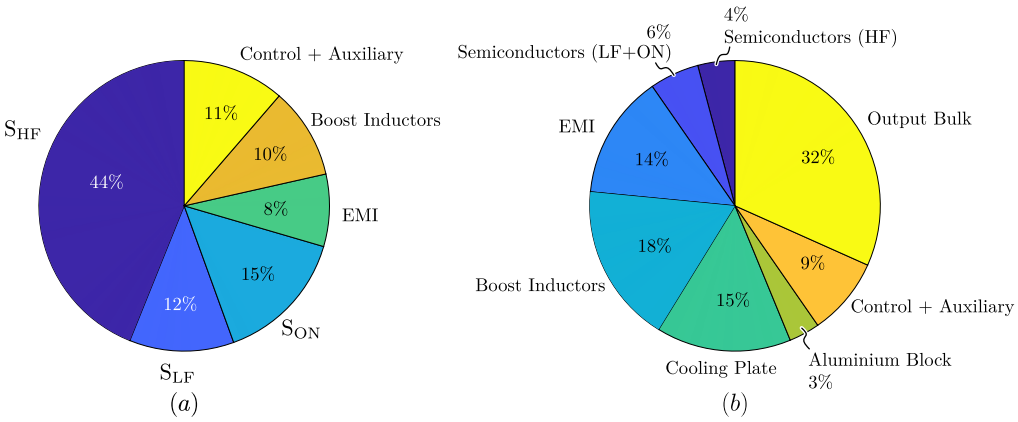

Figure 6.3: (*a*) Pie chart of the loss breakdown of the Pareto optimum design with L_{boost} = 30µH and (*b*) the volume breakdown. The HF semiconductors contribute the most to the losses and the output bulk capacitors take up the most of the volume.

Table 6.3: Single-phase Belgian PFC rectifier Pareto-optimal design specifications.

	Component	Designator	Value	Selection	Note
Electrical	Mains AC input	$v_{s,rms}$	240 V	-	-
	Nominal DC output	$v_{DC,nom}$	380 V	-	-
	Nominal output power	$P_{o,nom}$	19.2 kW	-	-
	Switching frequency	f_{sw}	20 −250 kHz	-	Variable frequency
	Interleaved BePFC stages	n_i	2	-	6× interl.
Semiconductor	HF boost switches	$S_{\bar{x}(\bar{a},\bar{b},\bar{c})}, S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$	-	SCTH100N120G2-AG	-
	LF selector switches	$S_{\bar{x}m}, S_{m\bar{y}}$	-	SCTH90N65G2V-7	2 parallel
	Constant ON switches	$S_{p\bar{x}}, S_{\bar{y}n}$	-	SCTH90N65G2V-7	2 parallel
Passives	Boost inductors	$L_{a,b,c}$	30 µH	PQ50/50, N97, 16 turns, 1.6 mm airgap, 986 × 0.071 mm Litz wire	-
	1st stage input DM filter	$C_{DM,1}, Cd_{DM,1}$	832 nF	-	-
		$L_{DM,ph,1}$	1.7 µH	-	-
		$L_{DM,N,1}$	576 nH	-	-
		$Rd_{DM,1}$	2 Ω	-	-
	2nd stage input DM filter	$C_{DM,2}, Cd_{DM,1}$	832 nF	-	-
		$L_{DM,ph,2}$	1.7 µH	-	-
		$L_{DM,N,2}$	576 nH	-	-
		$Rd_{DM,2}$	0.7 Ω	-	-
	1st stage input CM filter	$C_{CM,ph,1}$	1.7 nF	-	-
		$C_{CM,N,1}$	5.1 nF	-	-
		$L_{CM,1}$	234 µH	-	-
	2nd stage input CM filter	$C_{CM,ph,2}$	1.7 nF	-	-
		$C_{CM,N,2}$	5.1 nF	-	-
		$L_{CM,2}$	234 µH	-	-
	DM output filter	$C_{DM,o}, Cd_{DM,o}$	72 µF	-	-
		$L_{DM,o}$	2.2 µH	-	-
		$Rd_{DM,0}$	0.2 Ω	-	-
	Electrolytic bulk capacitors	C_{pn}	9.87 mF	-	-
	Midpoint CM capacitor	$C_{CM,m}$	4.7 nF	-	-

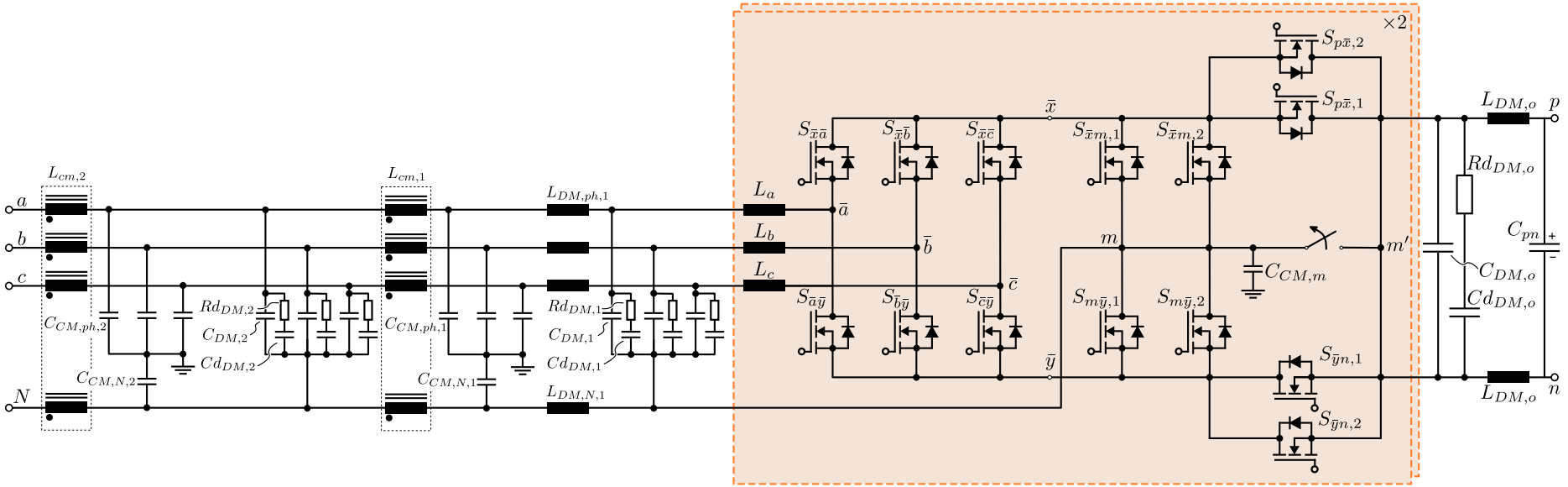

Figure 6.4: Schematic of the Pareto-optimal design with a *CLC* DM filter and a *LCLC* CM filter at the input and two BePFC rectifiers placed in parallel to achieve 6× interleaving for the HF bridge legs.

6.5. Summary

In this chapter the design optimization of the single-phase BePFC rectifier is described. The modelling routine of Figure 4.1 is used which sequentially uses the modelling techniques presented in Chapter 4 to generate different converter designs from the defined global and component design spaces, which are mapped onto the performance space. The global design space is explained consisting of a set of design variables such as the switching frequency, boost inductance value, number of BePFCs in parallel Together with a set of fixed parameters such as the the grid voltage, grid frequency output power, EMI compliance, and output voltage range for which each converter is designed. Also the component design space is explained that contains variables such as inductor core dimensions, Litz wires, core material, and different semiconductor devices.

The Pareto-front for a single, double and triple BePFC in parallel were shown after which a selection followed for the optimal nominal output voltage, number of BePFCs in parallel, and transistors in parallel. A detailed volume and losses breakdown on four different designs is presented to finally select the optimal design according to the multi-objective design requirements presented in 1.1. The optimal design featured a boost inductance of 30 µH and used TCM modulation with complete soft-switching transitions because the non-limited variable switching frequency. The power converter was estimated to have a 98.42 % efficiency with a 5.34 kW/dm^3 power density. The output bulk capacitors occupied 32 % of the total volume because of the high power variation resulting in large currents in the capacitors as explained in 3.5. Research into the implementation of an active pulsating power buffer could be relevant for this high power single-phase converter.

7

Comparative Evaluation

This chapter presents a comparison to see if the single-phase operation of the Belgian PFC rectifier is, potentially, a better alternative than the six-switch boost PFC rectifier which supports full-power delivery in single-phase operation. Both the converters are designed to also work in three-phase operation that specifies the boost inductance value. The topology comparison is done by using different performance indicator such as component stresses, semiconductor losses and required (normalized) attenuation for both the CM and DM filter. The performance indicators are calculated using the modelling techniques explained in chapter 4 and displayed to observe the influence of the boost inductance value in combination with the switching frequency.

7.1. Methodology

The single-phase Belgian PFC rectifier is compared in detail to the six-switch boost rectifier with modification to be able to operate at full power in single-phase operation (cf. Figure 2.5). The passive diode bridge of the modified six-switch PFC rectifier is replaced with active SiC MOSFET switches in order to create an equal basis of comparison. The converters are designed according to have a design space as specified in Table 7.1.

Table 7.1: Requirements and design space for the comparison of the Belgian PFC rectifier with the six-switch boost PFC rectifier.

Description	**Parameter**	**Value**
Single phase rms voltage	$v_{s,rms}$	240 V
Source frequency	f_s	60 Hz
Output voltage	$v_{pn,nom}$	380 V
Output power	P_o	19.2 kW
Input power factor	λ_{100}	> 0.99
EMI compliance	-	Class A
Boost inductance	L_{boost}	5 −150 µH
Switching frequency	f_{sw}	20 − 250 kHz
PFC rectifiers in parallel	n_i	2
Interleaving	n_{interl}	6
Transistor parallel	$Tr_{par,LF}$	2

The boost inductance value and switching frequency of the HF bridge legs are the two parameters that are kept variable for the comparison of the two topologies which are designed to have the semiconductors as listed in Table 7.2. Both converters are designed to be switching with either a constant switching frequency or a variable switching frequency (TCM modulation).

Table 7.2: Selected semiconductors for the comparison of the Belgian PFC rectifier with the six-switch boost PFC rectifier.

	Semiconductor	BePFC rectifier	Six-switch rectifier
Interleaved boost circuit	$S_{\bar{x}(\bar{a},\bar{b},\bar{c})}$	SCTH100N120G2AG	SCTH100N120G2AG
	$S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$	SCTH100N120G2AG	SCTH100N120G2AG
LF switch leg	$S_{\bar{x}\tilde{m}}$	SCTH90N65G2V-7	SCTH90N65G2V-7
	$S_{\tilde{m}\bar{y}}$	SCTH90N65G2V-7	SCTH90N65G2V-7
Constant ON switches	$S_{p\bar{x}}$	SCTH90N65G2V-7	-
	$S_{\bar{y}n}$	SCTH90N65G2V-7	-

The comparison is done with the assumption that both PFC rectifiers are designed for the three-phase operation. The result is that for the same inductor ripple a smaller boost inductor can be chosen for the BePFC rectifier as explained in Section 3.2. Therefore, the converters will be designed with the rough assumption that the boost inductance has a relation as $L_{boost,6switch} = 1.4 \cdot L_{boost,BPFC}$. The parameters of interest for the comparison are:

- Semiconductor stresses
- Semiconductor losses
- Required (normalized) attenuation

The semiconductor stresses are the voltage blocking capabilities of the semiconductor switches, this gives an indication of the required minimum breakdown voltage of the switch. Switches with a higher breakdown voltage usually result in having a larger $R_{DS,on}$ and higher switching losses. Both these consequences have a negative effect on the converter efficiency.

The semiconductor losses contribute for >40 % to the total losses in case of the BePFC rectifier making the semiconductor losses the second parameter of interest. The modelling of the semiconductor losses is done with a fixed transistor scaling factor (cf. 4.8*b*), so that the cooling design of both converter is the same, creating an equal basis of comparison.

The required attenuation gives an indication of the size of the EMI filters. A higher required normalized attenuation results is an EMI filter design with larger components. The required attenuation, as explained in 4.5.3, is specified at the design frequency f_D. For the comparison the attenuation is normalized to 150 kHz by using a high frequency asymptote of 60 dB/decade in case of the DM *CLC* filter and 80 dB/decade for the CM *LCLC* filter. The normalization is done because it could happen that the output of the EMI model results in similar attenuation, however a higher design frequency would result in a smaller EMI filter. The normalized attenuation will show a lower normalized attenuation for the design with a higher design frequency.

The volume of the boost inductor is assumed to be directly related to the peak stored energy as $v_L = k_L \cdot L \cdot \hat{I}^2$, where the peak stored energy in the inductor is $E = 1/2 \cdot L \cdot \hat{I}^2$. However, this is of less relevance for the comparison regarding the single-phase operation of both converters since the peak current scales linearly with the inductor value with the relationship $v = L \cdot di/dt$, so it is evident that the larger boost inductor of the six-switch rectifier, results in a lower peak stored energy when the same switching frequency is used. The peak stored energy becomes relevant for the comparison of the three-phase BePFC rectifier with the six-switch boost rectifier, as the three-level voltage obtained between the rectifier output nodes of the BePFC rectifier results in a smaller inductor ripple than for the six-switch boost rectifier with the same boost inductance. However, the comparison of the three-phase operation of the BePFC rectifier is out of the scope of this work.

7.2. Component Comparison

The basic operation principle is equal for both single-phase operated converters. The two main difference between both converters are that the BePFC rectifier is designed with a smaller boost inductor and that this converter is designed with the additional constant ON switches $S_{p\bar{x}}$ and $S_{\bar{y}n}$. The influence of both these differences is discussed in the following sections.

7.2.1. Semiconductor Stresses

The semiconductor voltage stresses for the BePFC rectifier are listed in Table 3.1 where the blocking voltages are dominated by the three-phase operation. The blocking voltages for the modified six-switch boost PFC rectifier are equal to the BePFC blocking voltages in single-phase as well as three-phase operation. With respect to the semiconductor stresses, there is no advantage of the single-phase operated BePFC rectifier over the modified six-switch boost PFC rectifier.

7.2.2. Semiconductor Losses

The semiconductor losses contribute to a large portion of the total losses for both topologies, therefore the high frequency semiconductor losses of the interleaved boost circuit and the conduction losses of the low frequency switch leg, (including the constant ON for the BePFC rectifier) are used for the semiconductor losses comparison of the two converter topologies. The only advantage is that the six-switch rectifier is implemented without the use of the constant ON switches.

High Frequency Switches The HF semiconductor losses imposed in the interleaved boost circuit are divided into the switching losses and conduction losses. The interleaved boost circuits in both converter topologies are similar but operate with a different size of boost inductance. The semiconductor loss model output the same results for both converter topologies, however for the comparison the two should thus be compared with a different size of boost inductance. In Figure 7.1 the constant switching frequency HF semiconductor losses are shown, where the white segments in the figure are the impossible designs due to thermal runaways in the semiconductors. Figure 7.1*a* show the switch-on losses of switches $S_{\bar{x}(\bar{a},\bar{b},\bar{c})}$ and $S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$. Zero switch-on losses are obtained below the ZVS-line, depicted with a dashed line. Above the ZVS-line partial, and further away full hard-switching occurs, this results in higher switch-on losses. In fig. 7.1*b* the total switching losses, a combination of the switch-on and -off losses, are shown. Higher switching losses occur when using a larger boost inductor with the same switching frequency as a result of hard-switching. It should be noted that the effect becomes noticeable when a small boost inductance ($20-40\,\mu$H) and a mid-range switching frequency ($80-160\,$kHz) is chosen for the BePFC rectifier.

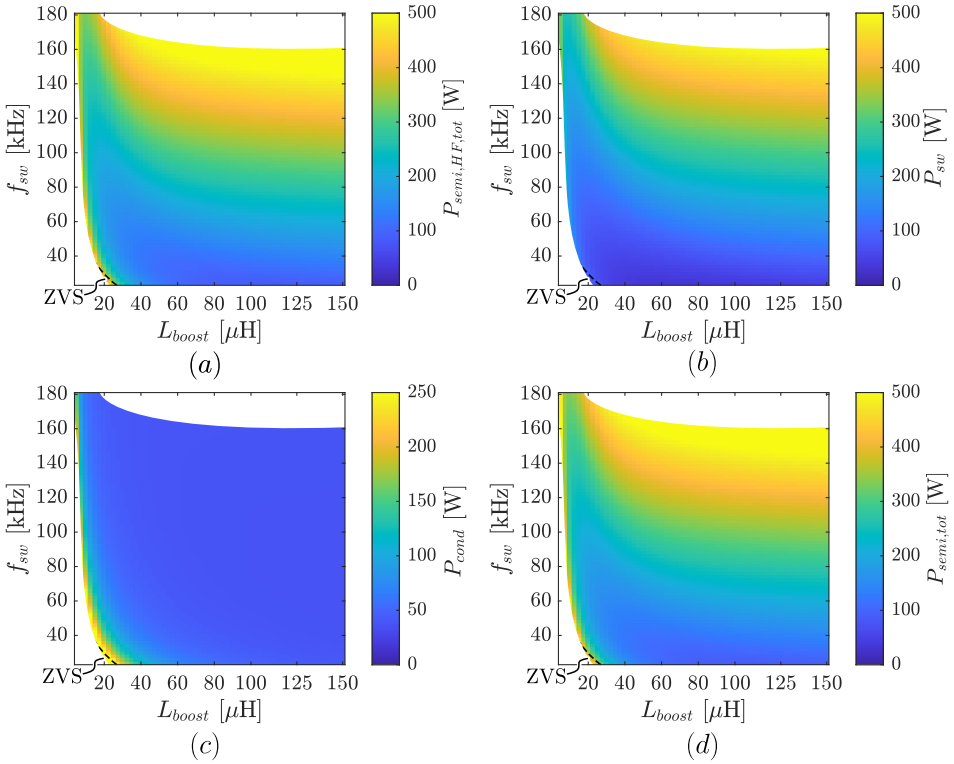

Figure 7.1: High frequency semiconductor (*a*) switch-on losses, (*b*) conduction losses, (*c*) switching losses and (*d*) total losses for different sizes of boost inductance with different constant switching frequencies at a nominal output voltage of $v_{pn,nom} = 380\,$V. These figures apply to both the single-phase Belgian PFC rectifier and six-switch boost rectifier.

The total conduction losses in the interleaved boost circuit (Figure 7.1*c*) shows a large increase when the boost inductance gets too low. The low boost inductance imposes in a high inductor current ripple with high rms currents that are the source of the higher conduction losses. A higher boost inductor results only in a slight decrease of the conduction losses. In fig. 7.1*d* the total losses in the interleaved boost circuit is shown. Two regions are visible that have high losses >400 W, the first one is the region when a low boost inductance is used, these losses mainly originate from the conduction losses. The second region is when a high switching frequency (>140 kHz) is used with a mid to high boost inductance (40 – 150 µH), these high losses originate mostly from the switching losses which scale proportional to the switching frequency.

The outcome of the design optimization in Chapter 6 was a design with a variable switching frequency as a result of the TCM modulation. The HF semiconductor losses for designs with different sizes of boost inductance using TCM modulation are depicted in Figure 7.2. The switch-on losses (fig. 7.2*a*) with this type of modulation should result in zero losses. However, the switching frequency limits [20 – 250 kHz] result in minor switch-on losses for designs with a boost inductance >32.5 µH. The total switching losses (fig. 7.2*b*) are high for designs with a small boost inductance, because the switching losses increase proportional to the increasing switching frequency with smaller boost inductor designs.

The conduction losses (fig. 7.2*c*) shows a large increase for designs with small boost inductance due to the increased rms current as a result of the the upper switching frequency limit. The conduction losses remain almost constant when the switching frequency is not limited (designs with L_{boost} = [10 - 32.5 µH]). The conduction losses decrease for designs with larger boost inductances due to the lower inductor current ripple as a result of the lower switching frequency limit. The total semiconductor losses of the interleaved boost interleaved boost circuit (fig. 7.2*d*) shows almost similar losses for designs with a boost inductance >75 µH.

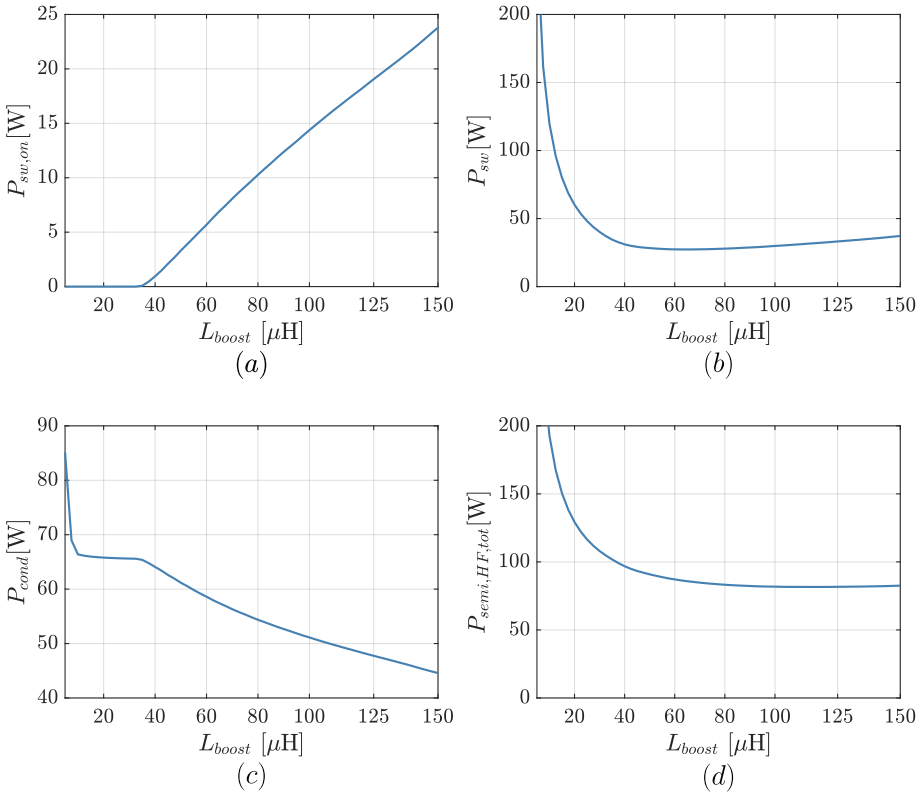

Figure 7.2: High frequency semiconductor (*a*) switch-on losses, (*b*) conduction losses, (*c*) switching losses and (*d*) total losses for different sizes of boost inductance with a variable frequency due to TCM modulation at a nominal output voltage of $v_{pn,nom}$ = 380 V. These figures apply to both the single-phase Belgian PFC rectifier and six-switch boost rectifier.

Solely on the HF semiconductor losses there is no advantage or disadvantage of using the single-phase BePFC rectifier (with a smaller boost inductance), compared to the six-switch rectifier (with a larger boost inductance). With constant switching frequency the six-switch rectifier can be operated with a lower switching frequency resulting in similar HF semiconductor losses. With TCM modulation the six-switch rectifier has only a slight advantage when the BePFC rectifier is implemented with a boost inductance <75 µH.

Low Frequency Switches The LF semiconductor losses are generated in the LF switch leg, in combination with the constant ON switches in case of the BePFC rectifier. These losses consist only of the conduction losses as the switching frequency is low. The total LF semiconductor losses for both converter topologies for constant switching frequency as well as variable frequency as a result of TCM modulation are shown in Figure 7.3.

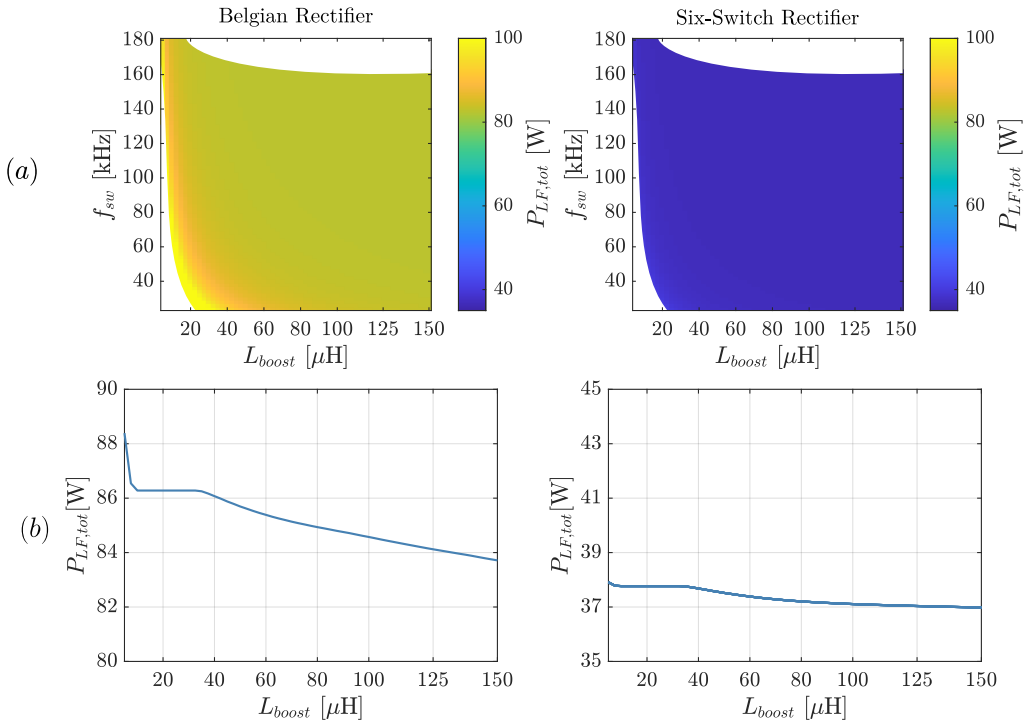

Figure 7.3: Low frequency semiconductor losses with (*a*) constant switching frequencies and (*b*) variable switching frequency with different sizes of boost inductance for the single-phase Belgian PFC rectifier and six-switch boost rectifier at a nominal output voltage of $v_{pn,nom} = 380\,\text{V}$.

The losses for the BePFC rectifier are higher because of the implementation with the additional constant ON switches. The boost inductance value and switching frequency have only a minor influence on these LF semiconductor losses because the boost circuit is operated using an interleaved pattern thereby cancelling the ripple. The single-phase BePFC rectifier is less favourable with respect to the total LF losses. The constant ON switching in the BePFC rectifier are useless in single-phase operation and only generate undesired conduction losses.

Total Semiconductor Losses The total semiconductor losses is, a combination of the HF and LF semiconductor losses, is shown in Figure 7.4 for both converter topologies. An advantage is evident to the single-phase six-switch rectifier in terms of the total semiconductor losses for designs with a constant switching frequency as well as with variable frequency. This advantage comes from the lower conduction losses due to the lower number of semiconductors. The lower number of switches also requires less boxed volume which is a additional advantage for the six-switch rectfier. There is no semiconductor losses advantage in the single-phase BePFC rectifier with smaller boost inductors. The only advantage that could arise is that the smaller boost inductance result in only ZVS switching transitions which is better for control stability as explained in Section 6.4.

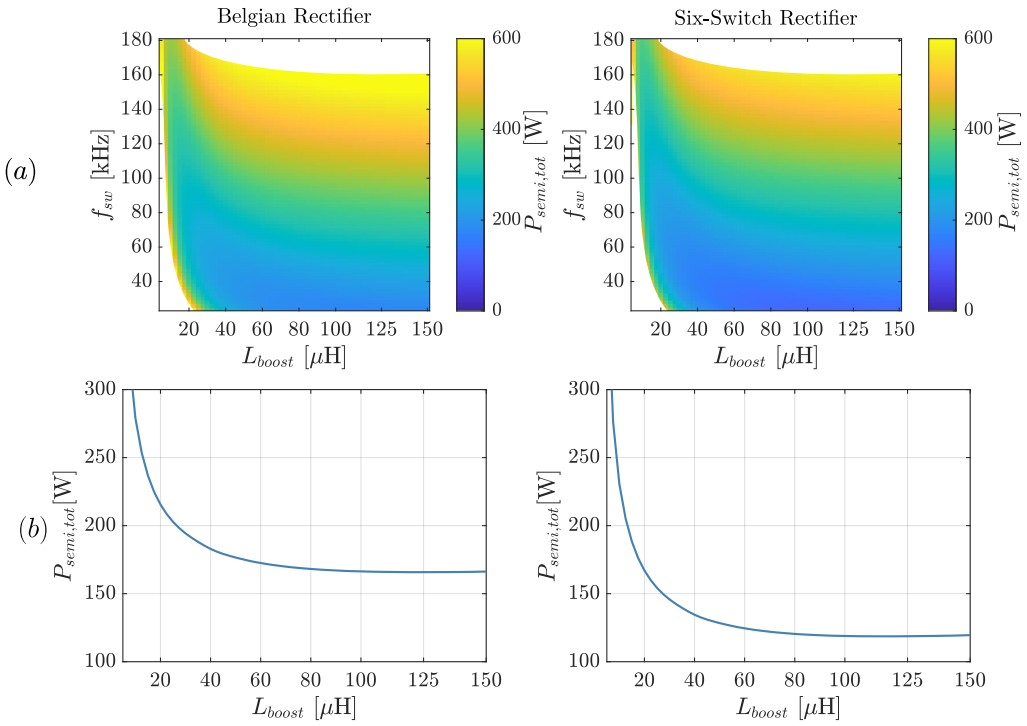

Figure 7.4: Total semiconductor losses with (*a*) constant switching frequencies and (*b*) variable frequency with different sizes of boost inductance for the single-phase Belgian PFC rectifier and six-switch boost rectifier at a nominal output voltage of $v_{pn,nom} = 380\,\text{V}$.

7.2.3. Required Attenuation

Figure 7.5 depicts the normalized required attenuation for both the single-phase BePFC rectifier and six-switch rectifier. The DM and CM sources originate from the HF interleaved boost circuit which is equal for both converters, therefore the same figures can be used for the comparison. Figure 7.5*a* refers to the designs with a constant switching frequency where two important jumps in required attenuation are evident. The first one is at a switching frequency of 24 kHz and the second one is at 82 kHz. Both these frequencies results in an effective frequency ($f_{sw,eff} = 6 \times f_{sw}$) just below the CISPR limits at 150 and 500 kHz and therefore result in lower required normalized attenuation. An almost not noticeable advantage results in the designs with a larger boost inductance of the six-switch rectifier, therefore this advantage is neglected. The filter designs will be similar in component values and thus also filter volumes when the same switching frequency is considered.

Figure 7.5*b* depicts the normalized required attenuation with variable frequency modulation. There is a low normalize attenuation required for low boost inductance design as a result of the high switching frequency. For designs with a boost inductance >115 µH a jump in the required attenuation is evident due to the resulting effective switching frequency below the CISPR limit.

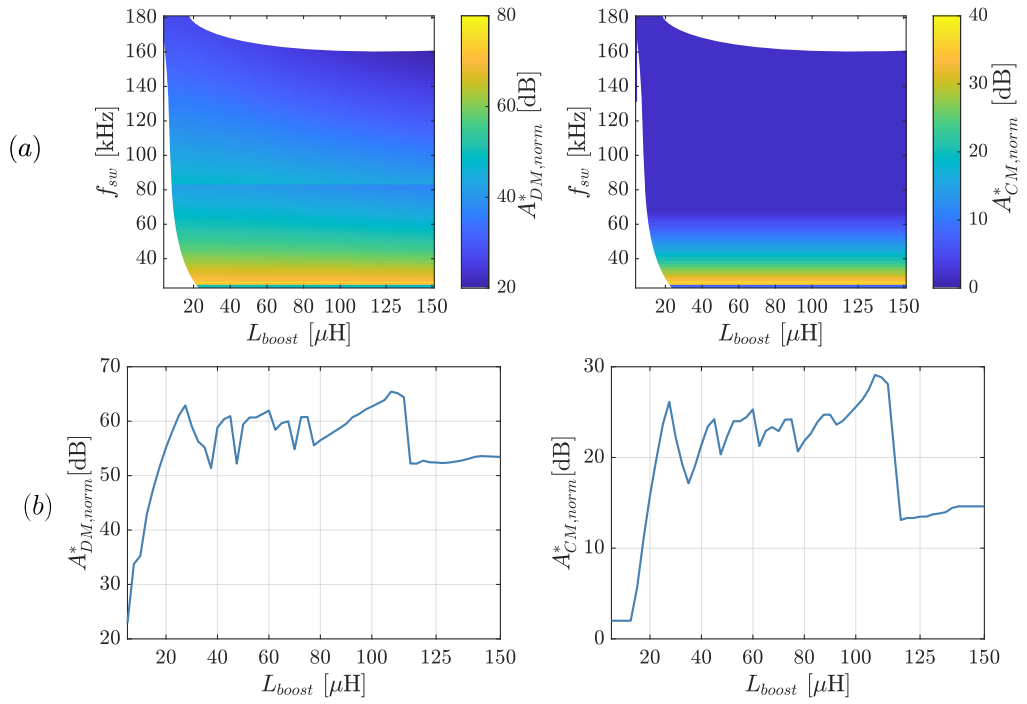

Figure 7.5: Normalized required DM and CM attenuation for the (*a*) constant switching frequency and (*b*) variable frequency designs for different sizes boost inductor These figures apply for both the single-phase Belgian PFC rectifier and six-switch boost rectifier.

7.3. Comparison Conclusion

It is difficult to conclude the comparison solely on the single-phase operation of the two converters because the designs depend on the three-phase operation. The main advantages are found in the three-phase BePFC rectifier as explained in Section 3.2. However, a slight disadvantage arises for the single-phase operation. The constant ON switches introduces additional losses independent on the boost inductor size giving the six-switch rectifier a slight advantage. Besides this, both the single-phase converters show very similar performance in the parameters of interest. With respect to the occupied volumes, the BePFC rectifier has the slight advantage of the smaller boost inductances but the advantage is nullified by the increased boxed volume due to the additional switches $S_{p\bar{x}}$ and $S_{\bar{y}n}$. The main advantage of the BePFC rectifier is the combination of the a high efficient three-phase rectifier which can be employed as single-phase converter without the need of additional switches to achieve full-power in both operations.

In [9], the modified six-switch PFC rectifier is compared to the conventional six-switch PFC rectifier, which which would be limited to 1/3 of the nominal three-phase power. It is concluded that only a slight increased converter volume, results in comparable out power levels as the three-phase modified six-switch rectifier. Because the BePFC rectifier and modified six-switch rectifier show very similar single-phase performance it can be concluded that there the advantage as specified in [9] also apply for the BePFC rectifier.

8

Hardware Demonstrator

8.1. Introduction

In this chapter the proof-of-concept hardware demonstrator of the single-phase BePFC rectifier is explained and measurement results are shown. The prototype converter design is described in detail by explaining the design of each converter component. The hardware demonstrator is tested with an input mains voltage of 240 V AC with a frequency of 60 Hz and a nominal 380 V DC output voltage. The hardware demonstrator is tested for a range of output power levels to obtain the THD, power factor, and efficiency curves. The interleaving of the six boost inductor current waveforms is verified with experimental results. Finally, a loss breakdown of the hardware demonstrator operating at 12 kW is presented and discussed.

8.2. Prototype Converter Design

The hardware prototype is designed to function as a proof-of-concept of the BePFC rectifier and is capable of supporting both the three- and single-phase operation. The 22 kW hardware demonstrator is designed as a twice interleaved three-phase BePFC rectifier, resulting in a 6 times interleaved single-phase BePFC rectifier similar to the Pareto optimal design explained in Section 6.4. The single-phase BePFC rectifier is controlled using the closed-loop control explained in Chapter 5. The TCM modulation in combination with a boost inductance of 25.01 µH results in a variable switching frequency and complete ZVS transitions in the bridge legs of the interleaved boost circuit. To limit the design effort, reduce design mistakes, and speed up the prototype design phase, most system peripherals and certain converter segments are reused from existing products within Prodrive Technologies. Figure 8.1 shows the single-phase BePFC rectifier hardware demonstrator and table 8.1 lists the relevant electrical parameters and component values.

EMI filter

The input EMI filter is a two-stage CM and DM filter adapted from an existing three-phase EMI filter within Prodrive Technologies, which is then tailored to a four-phase input EMI filter to be functional in case of single-phase operation. The modifications are the addition of a 4th phase winding in the CM-chokes and the additional DM inductor in the single-phase return path via the Neutral. The core and size of the 4-phase CM-choke is chosen to be able to easily hand-wind the inductor phases with 4 mm^2 solid copper wire. The reuse of the EMI filter and design of the CM-choke result in unnecessarily high attenuation and a non-optimized filter volume.

The output EMI filter is a single-stage DM filter formed by DM capacitors between p and n in combination with a filter inductor. An electrolytic bulk capacitor is placed parallel to the DC output with a value of 9.4 mF to cover the single-phase power pulsation as explained in Section 3.4.

Boost Inductors

The boost inductors are designed using a N87 PQ65/54 core with an airgap of 1.8 mm. The inductor is wound with 13 turns of Litz wire with a bundle diameter of 4.65 mm (1990 strands with a strand diameter of 0.071 mm) resulting in a boost inductance of 25.01 µH. The boost inductor design is reused from an existing product within Prodrive Technologies resulting in a larger inductor volume inductor than required. The Pareto optimum design, detailed in Section 6.4, makes use of a PQ50/50 core.

Semiconductors

The interleaved boost circuit is implemented with 1200 V SiC MOSFETs because the three-phase BePFC rectifier is operated with an output voltage of 750 V. The LF selector switch leg and constant ON switches are implemented with 650 V SiC MOSFETs. A capacitance of 0.5 nF and 0.75 nF is placed in parallel to each of 1200 V and 650 V MOSFET respectively in order to reduce the turn-on losses.

Prototype Mechanics

Figure 8.1 shows the BePFC rectifier hardware demonstrator. The prototype consists of a large PCB, also known as the 'Control & Power Board', with the input EMI filter, isolated gate supplies and MOSFET gate drivers. The boost inductors and metal core PCB, also know as 'MOSFET Board', are mounted and connected underneath the Control & Power Board with screw terminals. The metal core PCB is interfaced with the coldplate through the aluminium cooling block. An image of the hardware demonstrator without the coldplate is shown in Appendix A.3, Figure A.3. In the appendix Figure, the input EMI filter with DM inductors and CM chokes is better visible together with the boost inductors and FPGA board. The prototype mechanics is not optimized for volume, but explicitly to reach a (fast designed) operational proof-of-concept of the BePFC rectifier.

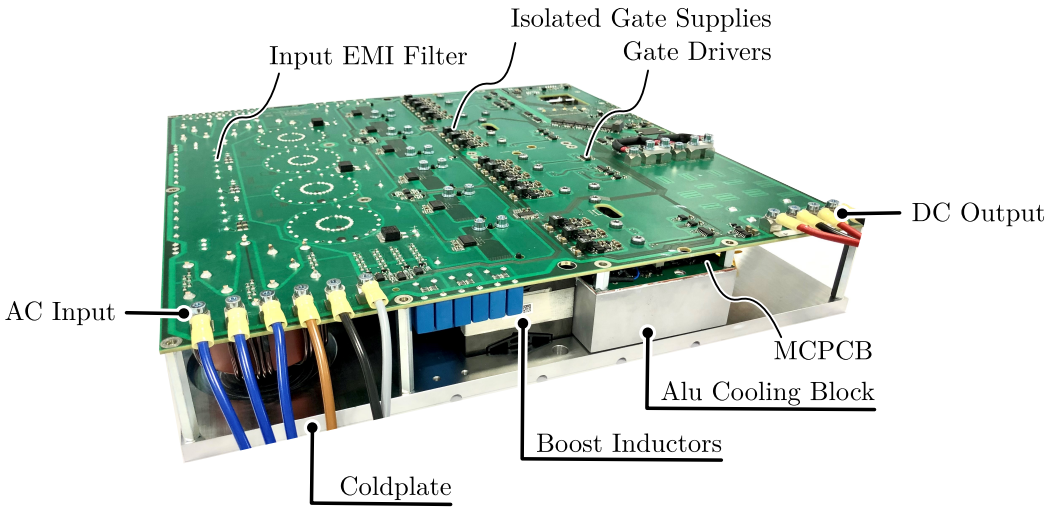

Figure 8.1: The single-phase BePFC hardware demonstrator with dimensions 400 x 400 x 73 (mm^3). The hardware demonstrator is tested up to an input power of 12 kW with a converter efficiency of >98 % and a power density of 1.5 kW/L.

Table 8.1: Single-phase Belgian PFC rectifier hardware demonstrator electrical parameters and component values.

	Component	Designator	Value	Selection	Note
Electrical	Mains AC Voltage	$v_{s,rms}$	240 V	-	-
	Mains Frequency	f_s	60 Hz	-	-
	Nominal DC Output	$v_{DC,nom}$	380 V	-	-
	Output Power	$P_{o,nom}$	19.2 kW	-	-
	Switching Frequency	f_{sw}	20 −250 kHz	-	Variable frequency
	Interleaved BePFC stages	n_i	2	-	6× interl.
Semiconductor	HF Boost Switches	$S_{\bar{x}(\bar{a},\bar{b},\bar{c})}, S_{(\bar{a},\bar{b},\bar{c})\bar{y}}$	-	SCTH100N120G2-AG	1 parallel
	LF Selector Switches	$S_{\bar{x}m}, S_{m\bar{y}}$	-	SCTH90N65G2V-7	1 parallel
	Constant ON Switches	$S_{p\bar{x}}, S_{\bar{y}n}$	-	SCTH90N65G2V-7	1 parallel
Passives	Boost Inductors	$L_{a,b,c}$	30 µH	PQ65/54, N87, 1990 × 0.071 mm Litz wire	13 Turns, 1.8 mm airgap
	DM Output Filter	$C_{DM,o}, Cd_{DM,o}$	72 µF	-	-
		$L_{DM,o}$	2.2 µH	-	-
		$Rd_{DM,0}$	0.2 Ω	-	-
	Electrolytic Bulk Capacitors	C_{pn}	9.4 mF	-	-

8.3. Volume Breakdown

Table 8.2 summarizes the estimated and actual occupied boxed volume of each individual converter component. The delta column in the table shows the difference between the estimated boxed volumes and the actual boxed volumes. The total column shows how much percent the converter component contributes to the total converter volume.

Table 8.2: Volume breakdown of the BePFC rectifier hardware demonstrator.

	Component	**Designator**	**Estimated**[cm^3]	**Actual** [cm^3]	**Delta** [%]	**Total** [%]
MCPCBs	Semiconductors	-	19.79	19.79	-	-
	Gate Drivers	-	-	24	-	-
	Snubbers	-	-	33	-	-
	Other	-	-	355	-	-
	Total	V_{MCPCB}	258	432	−40 %	4 %
EMI Filter	$DM_i + CM_i$	-	3004	3552	−15 %	-
	DM_o	-	53	100	−47 %	-
	Total	V_{EMI}	3276	3652	−30 %	28 %
Other	Boost Inductors	V_{boost}	1127	1254	−10 %	10 %
	Cooling Interface	$V_{Al,block}$	703	1332	−47 %	10 %
	Cooling Plate	V_{plate}	670	3200	−81 %	25 %
	Auxiliary	V_{aux}	376	843	−44 %	7 %
	Bulk Capacitors	V_{bulk}	1029	1029	-	8 %
	Surplus	$V_{surplus}$	1531	968	-	8 %
	Total volume	V_{total}	7941	12710	−38 %	-

The MCPCBs take up 4 % of the total converter boxed volume. A difference of −40 % can be obtained with the estimated boxed volume. The increased actual MCPCB volume comes mainly from the additional mounting points to connect a copper bus-bar that functions as the relay switch to switch between the single-phase and three-phase operation. The connection points are kept large to be able to conduct a large current which in turn increases the required area of the MCPCBs.

The EMI filter takes approximately 28 % of the total converter boxed volume, of which the largest portion is taken by the input EMI filter. The estimated input EMI filter volume shows a delta of −15 % which is attributed to the height of the CM-chokes that make the total boxed volume of the input filter larger than has been accounted for with the margin factors. The large delta of −47 % from the output EMI filter is due to the routing area that turned out larger than expected with the margin factors, therefore the filter volume is underestimated.

Other large contributors to the total converter volume are the boost inductors, cooling interface and the cooling plate. The estimated boost inductors volume is close to the actual value, a slightly larger margin factor could have been taken to come closer to the actual boost inductor volume. The volume of the cooling interface is underestimated with a delta −47 % of as a result of the underestimation of the MCPCB area. The actual cooling plate turned out to have significantly larger volume than estimated. In the estimation is was assumed that the cold plate was only located underneath the boost inductors and MCPCBs. However, the cold plate spanned the complete Control & Power Board area to make a rigid hardware demonstrator.

The bulk capacitor volume is estimated to be equal to the actual volume. The bulk capacitors are placed between the output of the BePFC rectifier and load. If this capacitor bank was placed on the PCB, margins had to be included for routing and bus clearances.

The actual auxiliary volume takes up 7 % of the total volume, the delta of −44 % can be attributed to the short design phase of the project. It has been decided to go for a larger size of PCB to make the routing-process of the Control & Power Board easier. The final volume contributor is named surplus, which is taken as a margin on the total estimated converter volume to take regions of air into account.

The final hardware demonstrator dimensions are 400 x 400 x 73 (mm^3) with an additional capacitor bank of 350 x 70 x 40 (mm^3), resulting in 12.7 L of boxed volume. The prototype power density is 1.5 kW/L when a nominal output power of 19.2 kW is considered. The prototype is designed with the purpose to function as a proof-of-concept. During the prototype design phase there has been chosen to not optimize the volume but deliver a working prototype before the end of this research project. Therefore, the occupied volume turned out to be larger than the results of the Pareto optimization, explained in chapter 6.

8.4. Measurement Results

The prototype measurements are done in order to prove the operation principle and proposed closed-loop control of the single-phase BePFC rectifier. A picture of the measurement set-up can be found in Appendix A.3, Figure A.4. Two *Chroma 61509* AC sources can be used in parallel to simulate the 240 V 60 Hz single-phase mains that can reach a maximum source power of 12 kVA. Two *EA-PSB-91500-30* bi-directional supplies are used as electric load to keep the output voltage at 380 V and sink the output current of the BePFC rectifier. The current, voltage, and power measurements are done with a *Tektronix MSO58* oscilloscope and *Yokogawa WT3000* power analyser. The measurements are done in the following two ways. The first way is with a single AC source connected and the power analyser measuring the in and output currents with the internal current sensor, where the input of the Yokogawa is limited to 30 A. The second way is with two AC sources parallel and the power analyser measuring the in and output currents with the use an external current sensor (current transformer) that is capable of measuring 600 A. The first test tests are done with a maximum power of 6 kW and the second tests allow maximum input power levels up to 12 kW. The presented measurement set-up does not allow to test with higher power levels.

Input AC Current THD and Power Factor To verify the power factor correction principle of the single-phase BePFC rectifier, the THD and power factor are measured. The THD, as explained in Section 2.1, is a measure of harmonic distortion present in a signal in relation to the fundamental component, and the power factor λ is defined by the displacement angle between the fundamental component of the voltage and current, and THD of the AC input current.

Figure 8.2*a* shows the THD and power factor measurement results of the single-phase BePFC rectifier. The measurements with the internal current sensor and external current transformer correspond to the results in red and blue respectively. Both measurements show a decreasing (improving) THD with increasing input power. The internal current sensor results show a better THD performance than the external current sensor results. This can be attributed to the single versus two Chroma AC sources in parallel, which lowers the source impedance resulting in higher current peaks with every zero crossing of the source voltage. The THD measured with the external current sensor shows a minimal THD of 6.3 % that increases at 10 kW input power. The THD jump is a result of the FPGA firmware that shows non-perfect interleaving of the six boost inductor currents resulting in higher inductor current peaks with a lower converter efficiency as a result. To improve the efficiency for input powers >9 kW, the current controller gain is lowered to keep the inductor current peaks within reasonable limits and achieve a higher efficiency, but a worse THD. When a dedicated single (higher power) source is used and the control is programmed without any issues, it is expected for the THD to reach below 5 %.

The BePFC rectifier shows a power factor <0.95 when operated at power levels <2.2 kW. This is due to DM capacitors drawing reactive power as explained with eq. (4.25). The measurement results show a power factor reaching >0.95 that keeps increasing until reaching close to 1 for input power levels >2.2 kW. Power factor limits typically require to have a power factor >0.95.

The combination of measurement results of the THD and power factor verify the power factor correction principle of the single-phase BePFC rectifier. The THD could be improved by further inspection of the control as it is not yet optimally implemented. Inductor current measurement are triggered with a constant instead of variable frequency. Wrong current measurements are then input to the current controller which results in an unstable controller. The required software changes have been noted but could not be implemented before the end of the project.

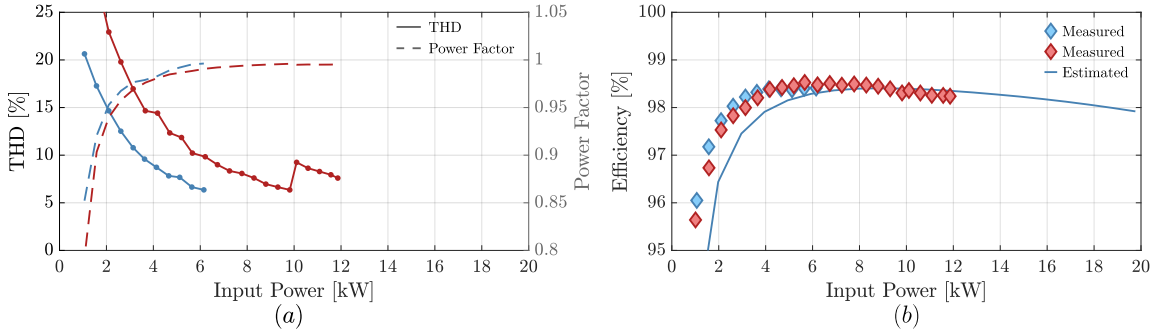

Figure 8.2: Measurement results of the single-phase BePFC hardware demonstrator with a boost inductance of 25.01 µH, 240 V single-phase input and 380 V DC output. The measurements in blue and red are done with the internal current sensor and external current sensor respectively. (*a*) The measured total harmonic distortion (THD) and power factor λ versus input power. (*b*) Estimated and measured converter efficiencies versus input power. Tests are performed with a maximum input power of 12 kW because of input AC source limitations.

Converter Efficiency Figure 8.2*b* shows the estimated and measured converter efficiencies of the single-phase BePFC rectifier. The blue and red diamonds correspond to the internal current sensor and external current transformer measurements respectively. The measured efficiency reaches >98 % for input power levels >3 kW, a peak efficiency of 98.53 % at 5.5 kW, and an efficiency of 98.24 % at 12 kW (the maximum test set-up power level). A delta of −0.11 % can be observed when comparing the measured with the estimated efficiencies at 12 kW, which amounts to a mismatch of 13 W. The mismatch can be attributed to the current status of the software implemented control that does not allow for perfect interleaving with higher current peaks in six boost inductor currents as a result. These higher current peaks lead to higher losses which is not accounted for in the model. Further mismatch can be attributed to the error margins in the implemented mathematical converter model and obtained datasheet information. In particular with datasheet information obtained from the HF 1200 V SiC MOSFET switch. The switching energy graphs, provided by the switch manufacturer, correspond to the E_{on} and E_{off} graphs of a totally different switch. Updated E_{on}/E_{off} graphs are provided by the manufacturer, however, have not yet been implemented in the converter model.

Interleaved Boost Inductor Currents Figure 8.3 shows the measured waveforms of the source voltage v_s, source current i_s and six boost inductor currents i_L. When investigating the input current i_s (cf. fig. 8.3*a*), current peaks can be observed with every zero crossing of the source voltage. This occurs due to the charging and discharging of the DM capacitors of the input EMI filter when the switches are disabled. These current spikes have a constant peak amplitude, which become less noticeable when the power converter is operated at higher power levels.

Figure 8.3*b* and *c* shows a closer look at the six boost inductor currents i_L similar to Figure 5.3 in Chapter 5. Although the interleaving control is not yet optimal over the entire mains period, Figure 8.3*b* identifies the switch-specific start sequence after the zero-crossing of the source voltage. There are regions where interleaving works perfect, as visible in Figure 8.3*c*. This happens to occur within regions where twice the switching frequency falls together with the (constant) trigger frequency of the current measurements which should have been programmed to be variable to show good control behaviour over the entire mains period.

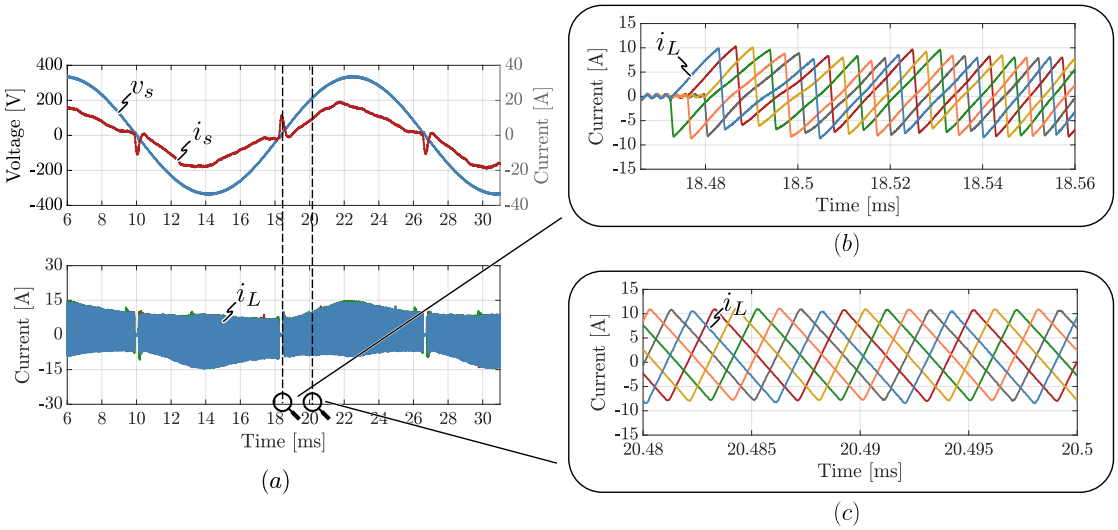

Figure 8.3: (*a*) Measurement waveforms of the hardware demonstrator with a 240 V 60 Hz AC input voltage and nominal 380 V DC output at 2.6 kW input power. Depicted are the input voltage v_s, input current i_s and boost inductor currents i_L. (*b*) The start-up sequence of the six interleaved boost inductor currents after the zero-crossing of the source voltage. (*c*) The perfect interleaving principle of the single-phase BePFC rectifier at regions where twice the switching frequency falls together with the inductor current sampling frequency.

8.5. Loss Breakdown

Figure 8.4 shows the estimated loss breakdown and pie-chart of the single-phase BePFC rectifier hardware demonstrator with L_{boost} = 25.01 µH, nominal 380 V DC output voltage at an input power level of 12 kW. The hardware demonstrator is operated with complete ZVS transitions of the HF semiconductor, as can be seen with the absence of sw_{on} in Figure 8.4*a*. The HF semiconductor losses, which amount to 34 %, contribute the most to the total converter losses.

Other large loss contributor are the EMI filter, S_{LF} and S_{ON} switches. The total EMI filter losses amount to 25 % of the total converter losses. The EMI filter losses mainly consist of conduction losses in the filter components. The losses of S_{LF} and S_{ON} contribute for 14 % and 19 % respectively. These losses only consists of the conduction losses as the switching losses are negligible. The remaining losses originate from the conduction and core losses in the boost inductor L_{boost}, that 8 % of the total converter losses.

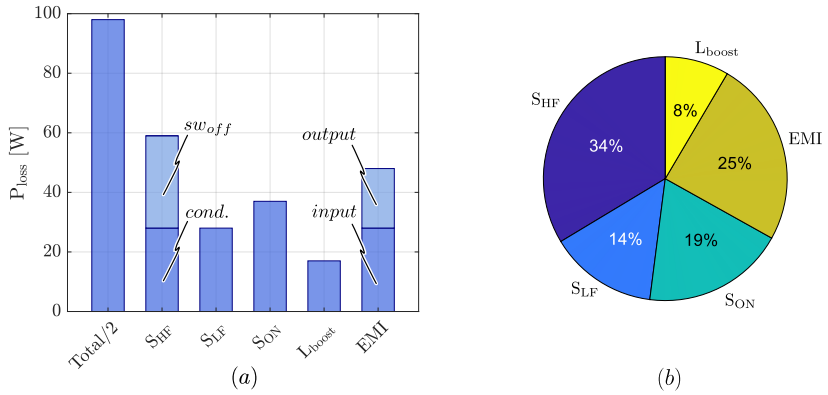

Figure 8.4: Estimated loss breakdown of the single-phase hardware demonstrator with a boost inductance of 25.01 µH, 240 V 60 Hz AC input voltage and 380 V nominal DC output voltage at an input power of 12 kW. (*a*) The loss bar chart with the HF switch losses divided into conduction and switch-off losses. The EMI filter is divided into in- and output EMI filter losses. (*b*) The corresponding loss distribution pie-chart.

8.6. Summary

This chapter served as the explanation of the BePFC rectifier hardware demonstrator design and experimental result verification. The design of the BePFC rectifier was discussed in detail with the hardware demonstrator shown in Figure 8.1. The decision to go for a working prototype instead of an optimally designed mechanical prototype has let to a power density of 1.5 kW when an output power of 19.2 kW is considered. A volume breakdown of the hardware demonstrator was provided and compared to the estimated component volumes.

THD and power factor measurements were performed on the hardware demonstrator. The hardware demonstrator already showed a THD below 7.5 % and is expected to show a THD below 5 % when operated at higher powers with a single AC source in combination with the improves firmware of the FPGA. The power factor of the hardware demonstrator reached >0.95 for input power levels >2.2 kW. The results of both the THD and power factor have proven the power factor correction principle of the single-phase BePFC rectifier.

Efficiency measurements on the hardware prototype were performed that show efficiencies >98 % when operated at input powers >3 kW, a peak efficiency of 98.53 % at 5.5 kW, and an efficiency of 98.24 % at the maximum test power level of 12 kW. The modelling techniques of Chapter 4, used to estimate the hardware demonstrate efficiency, showed a mismatch of 0.11 % at 12 kW compared to the measured efficiency. The main sources of model inaccuracy were discussed in detail and the six interleaved boost inductor currents were shown to prove interleaving principle together with the start-up sequence explained in 5. An explanation was given for the correct and incorrect interleaving of the boost inductor currents. Finally, a loss breakdown of the hardware demonstrator at 12 kW was discussed in detail.

9

Conclusion and Future Work

This work presented the research into the single-phase operation of the Belgian rectifier, a novel boost-type PFC rectifier which allows for full power operation in both single- and three-phase operation. This converter can be relevant for EV fast chargers in countries providing three-phase 400 V 32 A (22 kW), as for example in Europe, as well as single-phase 240 V 80 A (19.2 kW) in the USA. The *first objective* of this research was to proof that the Belgian PFC rectifier is capable of operating in single-phase at similar nominal power levels with comparable component stresses as in three-phase operation, thus without the need to over-dimension the power stage. This research objective included the description of the operating principle, the development of a closed-loop control, and the modelling and design of a 19.2 kW single-phase Belgian PFC rectifier hardware demonstrator that was used for the proof-of-concept.

Starting with the literature review, relevant background was provided to understand: (1) the topology modifications to operate a three-phase power converter at nominal power levels in single-phase operation, (2) the principle of zero-voltage switching of semiconductors in MOSFET half-bridges, and (3) the mathematical modelling of power converters.

The topology modifications, that include a 4th-phase winding in the CM chokes and additional relay contact, have been applied to the Belgian PFC rectifier and a steady-state analysis is performed to form a mathematical basis for the modelling and design. This section concluded to operate the three-phase rectifier bridge-legs using an interleaved pattern with a triangular current mode modulation scheme to allow for a reduced input current ripple and complete zero-voltage switching transitions over the entire mains period. However, the high current ripple in the output bulk capacitors, as a result of the single-phase power pulsation, required to over-dimension the output bulk with a negative effect on the total converter volume.

The introduced MATLAB power converter model is formed by: (1) the basic- (steady-state) analysis, (2) Fourier-analysis to obtain the switch-cycle Fourier coefficients, and (3) multi-physics component specific models, i.e. semiconductor model, inductor model, and EMI models. The component specific models output component losses and volume in order to estimate the system level efficiency and power density.

A description of the proposed single-phase closed-loop control scheme was provided containing the explanation of the current controller, switching frequency calculation, and variable frequency interleaving control. This section concluded to disable and enable the semiconductor switches using a switch-specific pattern with every zero-crossing of the mains voltage to prevent current spikes and allow for an improved THD at the AC input. The proposed closed-loop control is implemented on the hardware demonstrator.

The single-phase operation principle, closed-loop control, and modelling techniques have been verified with a 19.2 kW hardware demonstrator with a power density of 1.5 kW/L. Experimental results showed efficiencies >98 % for input power levels >3 kW and a peak efficiency of 98.53 % at 5.5 kW. The estimated system level efficiency, obtained using the proposed converter model, showed a mismatch of 0.11 % or 13 W at the maximum tested input power level of 12 kW.

The *second objective* of this research was to identify and quantify the benefits in terms of efficiency and power density of the Belgian PFC rectifier. This research objective included the optimal design of a 22 kW Belgian PFC rectifier and the comparison with the conventional six-switch boost PFC rectifier operating in single-phase mode.

A global and component design space were determined for the design optimization of a 22 kW single-phase Belgian PFC rectifier. Four variable design parameters that have a large influence on the performance were determined to be the nominal output voltage, switching frequency, boost inductor value, and number of interleaving boost stages. By execution of the virtual prototyping routine, the different virtual power converter designs were mapped onto the performance space to obtain the Pareto-fronts. This section concluded that low boost inductance, variable switching frequency designs ensure a high efficiency with complete zero-voltage switching in combination with a high power density. The Pareto-optimal design makes use of 30 µH boost inductance and achieves a full-power efficiency of 98.42 % with a power density of 5.43 kW/L.

The Belgian PFC rectifier was compared with the six-switch boost PFC rectifier. The starting point was a three-phase system which is tailored to be operated in single-phase. The comparison was done based on the semiconductor stresses, semiconductor losses, and required (normalized) EMI filter attenuation. This section concluded that the main advantages of the Belgian rectifier are to be found in the three-phase operation with (1) smaller boost inductors, (2) reduced switching losses, and (3) the use of semiconductor switches with a lower voltage rating. Compared to the single-phase operated conventional six-switch PFC rectifier, which is limited to 1/3 of the three-phase power, the Belgian rectifier showed a slight volume increase but can be operated at full three-phase power levels.

The two research objectives with sub-objectives, as specified in Section 1.1, have been completed and the design requirements of a nominal full load efficiency of >98 % with a power density of >5 kW/L, as specified in table 1.1, have been met by the Pareto-optimal design. The hardware demonstrator proved the operation principle of the single-phase Belgian rectifier with efficiencies >98 kW for input power levels >3 kW.

9.1. Future Work

The research objectives have been completed and a working hardware demonstrator has been provided. However, during the modelling and design of the Belgian PFC rectifier of this research, simplifications are done and non-ideal electrical components have not always been considered. To improve the modelling and design for future work, topics of interest are summarized below:

- The modelling and optimization of the three- and single-phase Belgian PFC rectifier were done using two separate power converter models. However, both operation principles are to be used on a single power converter. Therefore, the optimization algorithm would benefit from combining the modelling of both the three- and single-phase operation in a single power converter model to quantify the influence of design changes on both operation principles.
- The hardware demonstrator was implemented with matched boost inductor values. Any mismatch would lead to the non-perfect cancellation of the interleaved boost inductor currents. Modelling the single-phase Belgian PFC rectifier with tolerances on the boost inductors values could show the influence on the Belgian PFC rectifier design.
- The single-phase Belgian PFC rectifier suffers from high currents in the output bulk as a result of the single-phase power pulsation. The Pareto-optimal design showed that the output bulk capacitors contribute to approximately 32 % of the total converter volume. To lower this contribution, research can be done into an active power pulsation buffer.
- The hardware demonstrator showed to have problems with the interleaving control at higher powers. The required software change is to trigger the inductor current measurements with a variable sampling frequency corresponding to twice the switching frequency. Implementing these changes would make the full power testing of the hardware demonstrator possible.

A

Appendix A

A.1. Complex Fourier Analysis

The complex Fourier coefficients of a time domain signal $s(x)$ can be calculated with:

$$c_n = \frac{1}{T}\int_T s(x)e^{-j\frac{2\pi nx}{T}}dx \tag{A.1}$$

The two level square wave of Figure A.1 can be described as:

$$c_n = \frac{1}{T}\int_0^{\frac{\phi}{2\pi}T} U_2 e^{-j\frac{2\pi nx}{T}}dx + \frac{1}{T}\int_{\frac{\phi}{2\pi}T}^{dT+\frac{\phi}{2\pi}T} U_1 e^{-j\frac{2\pi nx}{T}}dx + \frac{1}{T}\int_{dt+\frac{\phi}{2\pi}T}^{T} U_2 e^{-j\frac{2\pi nx}{T}}dx \tag{A.2}$$

This equation can be simplified to

$$c_n = \frac{e^{-j\phi n}}{j2\pi n}[(U_1(1-e^{-j2\pi nd})) + (U_2(e^{-j2\pi nd}-1))] \tag{A.3}$$

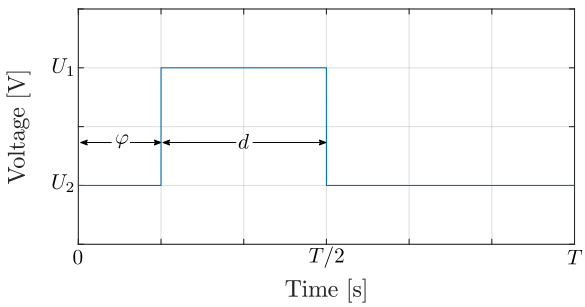

Figure A.1: A two level square wave with voltage levels U_1 and U_2 a phase-shift ϕ and duty cycle d.

A.2. EMI Filter Design Analysis

For the derivation of eq. (4.24), only the DM part of the filter depicted in Figure 4.13 is considered.

The attenuation provided by the CLC filter stages and R_{LISN} is given by:

$$Att_{LC} = \frac{1}{(2\pi f_D)^3 \cdot L_{DM} \cdot C_{DM}^2 \cdot R_{\text{LISN}}} \tag{A.4}$$

The volumes of the filter inductor and filter capacitors are given by

$$\begin{aligned} V_L &= k_L \cdot L_{DM} \cdot \hat{I}^2 \\ V_C &= K_c \cdot C_{DM} \cdot \hat{V}^2 \end{aligned} \tag{A.5}$$

where $\hat{I}$ and $\hat{V}$ are the peak current and voltage for the corresponding component.

The total DM filter volume is the sum of all the filter component volumes and is calculated as:

$$\begin{aligned} V_{DM} &= 3 \cdot V_{L,ph} + V_{L,N} + 2 \cdot V_C \\ &= 3 \cdot k_l \cdot L_{DM} \cdot \hat{I}_{ph}^2 + k_L \cdot \frac{L_{DM}}{3} \cdot (\hat{I}_{ph} \cdot 3)^2 + 2 \cdot k_c \cdot 3 C_{DM} \cdot \hat{V}^2 \\ &= \frac{2}{3} \cdot k_L \cdot \hat{I}_{ph}^2 \cdot L_{DM} + 6 \cdot k_c \cdot \hat{U}^2 \cdot C_{DM} \end{aligned} \tag{A.6}$$

The filter volume can be minimized by rewriting (A.4) and (A.6) to

$$L_{DM} = a \cdot \frac{1}{C_{DM}^2} \tag{A.7}$$

and

$$V_{DM} = b \cdot L_{DM} + c \cdot C_{DM} \tag{A.8}$$

with

$$\begin{aligned} a &= \frac{10^{\mathrm{A}_{DM}^*/20}}{(2\pi f_D)^3 \cdot R_{\mathrm{LISN}}} \\ b &= \frac{2}{3} \cdot k_L \cdot \hat{I}_{ph}^2 \\ c &= 6 \cdot k_c \cdot \hat{U}^2 \end{aligned} \tag{A.9}$$

Differentiating of A.8 with respect to C_{DM} and equating with zero

$$\begin{aligned} \frac{\delta V_{DM}}{\delta C_{DM}} &= 0 \\ b \cdot a \cdot -2 \cdot C_{DM}^{-3} + c &= 0 \end{aligned} \tag{A.10}$$

leads to the optimal C_{DM} filter values as

$$C_{DM} = \sqrt[3]{\frac{2 \cdot a \cdot b}{c}} \tag{A.11}$$

Rewriting and filling in leads to the final equation

$$C_{DM} = \sqrt[3]{\frac{2/3 \cdot k_{L,powder} \cdot I_{max}^2 \cdot 10^{\mathrm{A}_{DM}^*/20}}{3 \cdot k_{c,foil,X2} \cdot V_{max}^2 \cdot R_{\mathrm{LISN}} \cdot \omega_D^3}} \tag{A.12}$$

A.2.1. Equivalent CM Noise Source

To get to the equivalent CM noise source corresponding to eq. (4.31), the following steps are taken (cf. Figure A.2):

1. L_{boost}/n_{int} is replaced by an open circuit;
2. $C_{DM,1}$ is replaced by a short circuit;
3. The DM noise source is replaced by the Thevenin equivalent source and the equivalent circuit as Figure A.2*b* is generated;
4. The HF impedance of C_{eq} is found negligible compared to the other magnetic components and the circuit can be further simplified without C_{eq}.

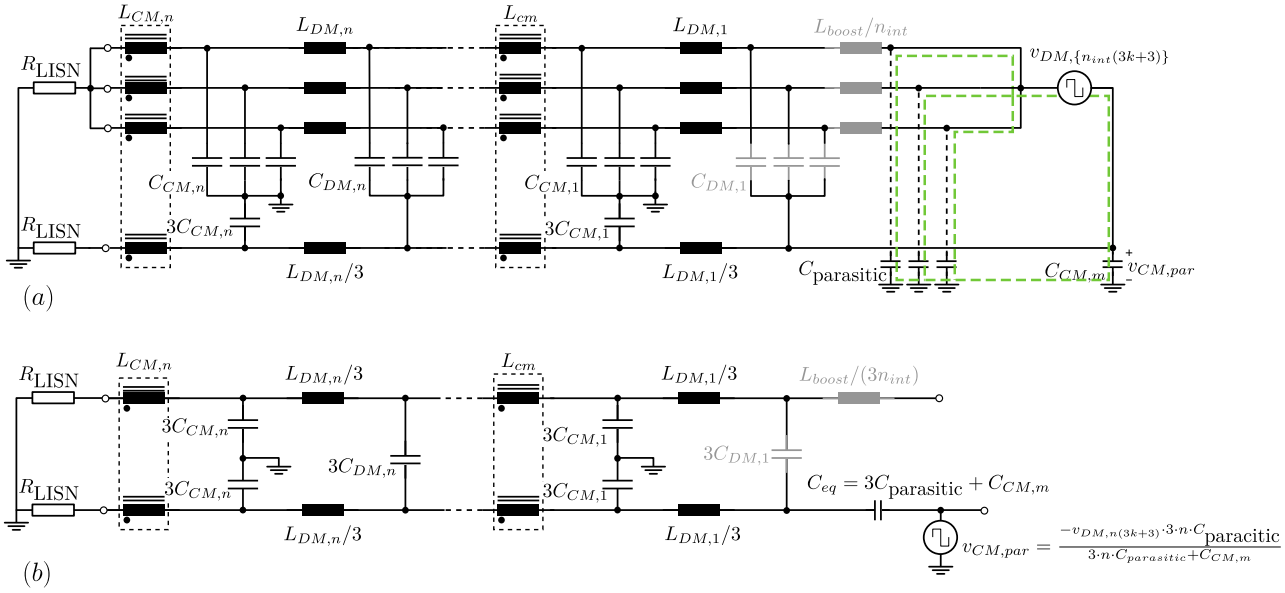

Figure A.2: CM equivalent noise source circuit.

A.3. Hardware Demonstrator Figures

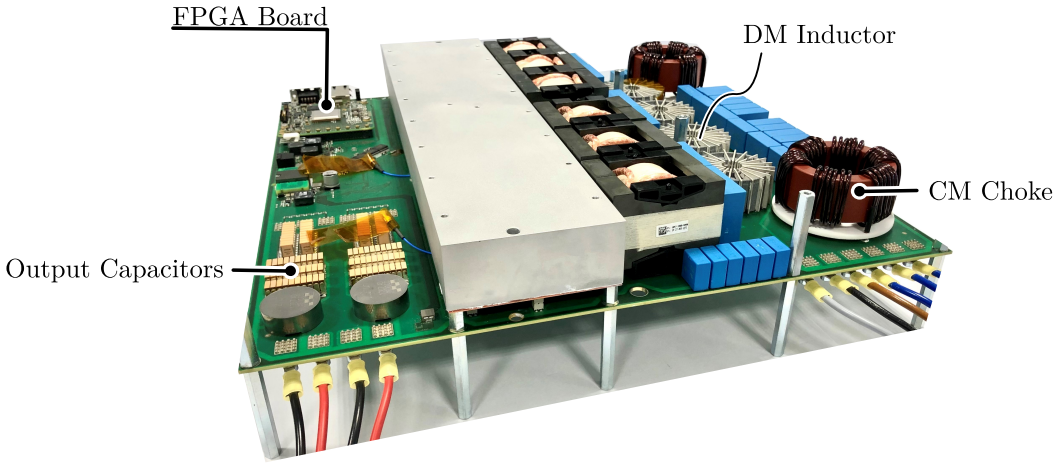

Figure A.3: The BePFC rectifier hardware demonstrator where the coldplate is removed to show the HF output capacitors, FPGA board, DM inductors and CM chokes.

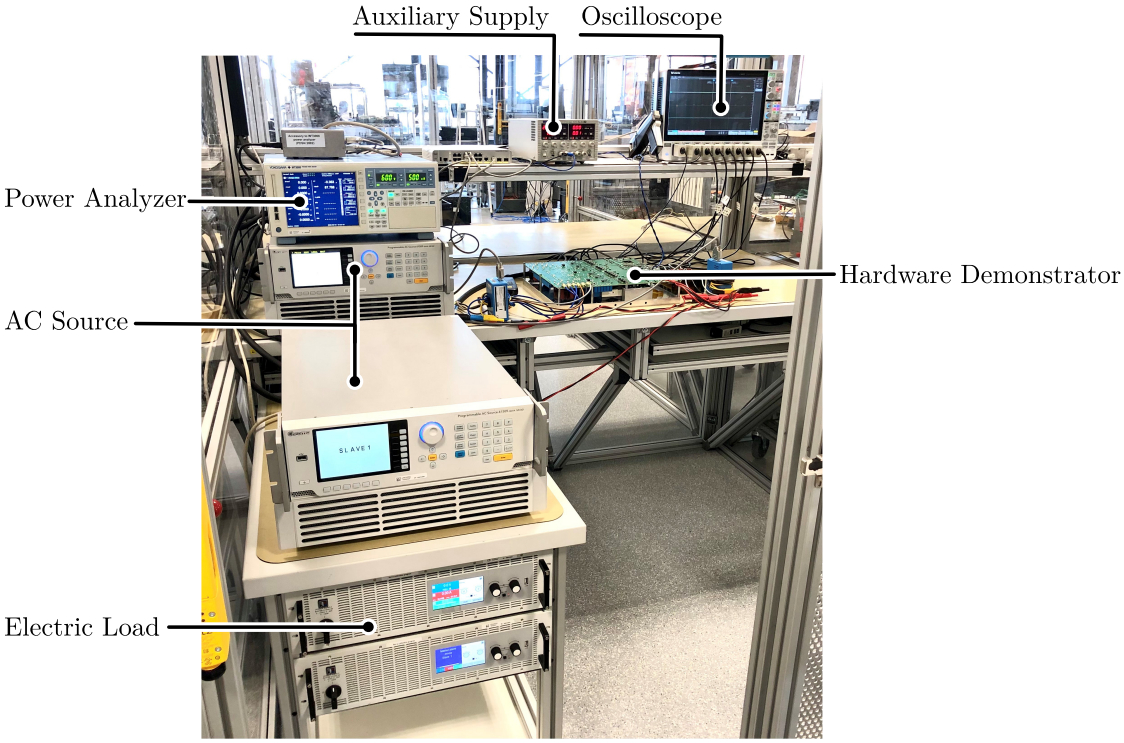

Figure A.4: Measurement set-up of the hardware demonstrator.

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