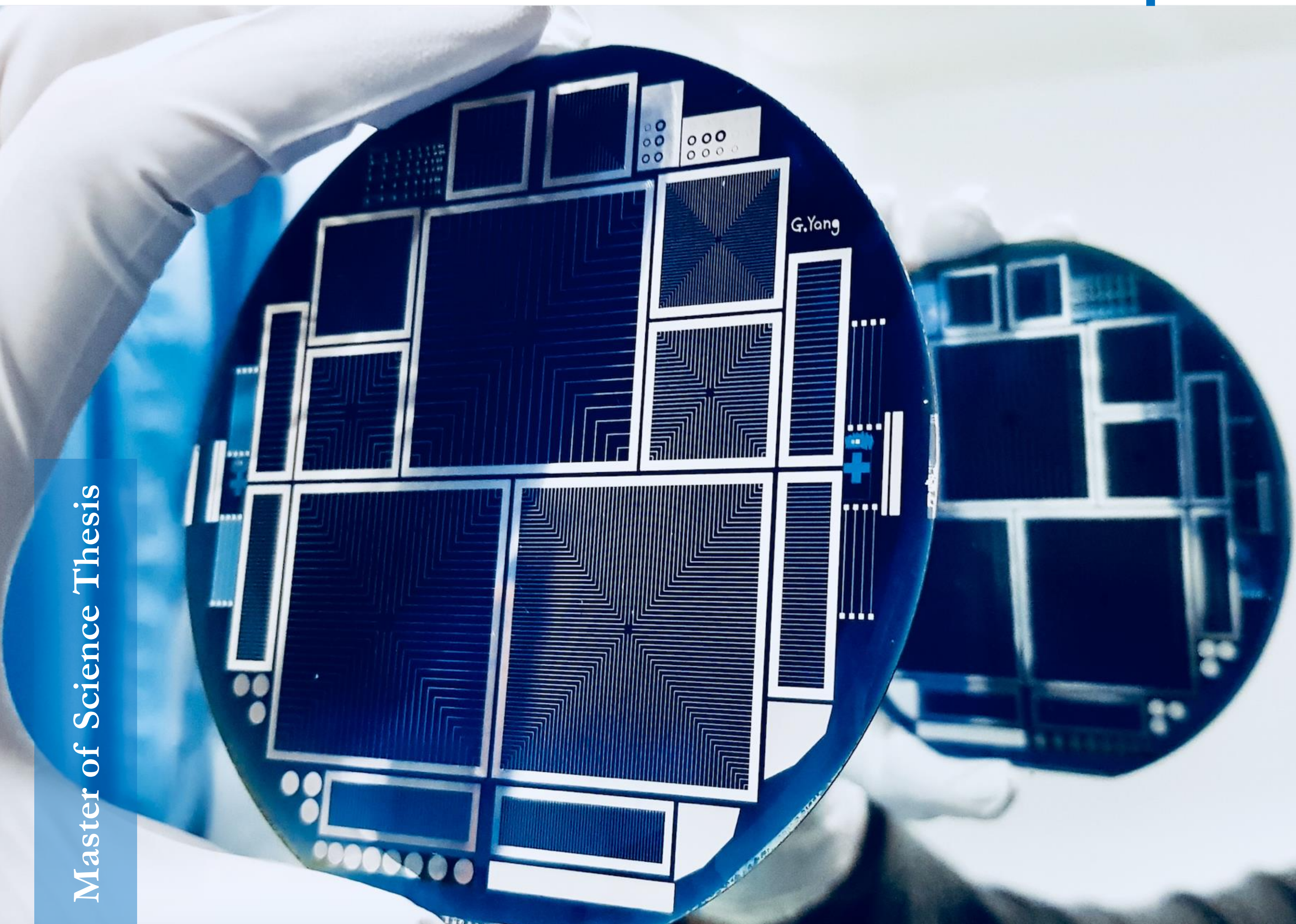
Advanced Bifacial Solar Cell with Poly-Si Passivating Contacts

Yiran Zhao



Master of Science Thesis

TUDelft Delft University of Technology

EKL Else Kooi Laboratory

PVMD Delft University of Technology

Advanced Bifacial Solar Cell with Poly-Si Passivating Contacts

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May 2018

In partial fulfilment of the requirements for the **Master of Science** in

Sustainable Energy Technology at Delft University of Technology

to be defended on Thursday May 31, 2018 at 11:00 AM.

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Abstract

As a new face of PV industry, bifacial technology offers the utmost utilization of reflected light while efforts are still required to further improve its cell efficiency. The objective of this thesis project is to fabricate bifacial solar cell with poly-Si passivating contacts only underneath metal grids. An advanced bifacial architecture is presented combining carrier-selective n/p+ doped poly-Si passivating contacts to quench recombination at c-Si/metal interface, and lightly doped n/p type c-Si surface to ensure high optical transparency on both sides.

LPCVD based doped poly-Si works together with wet-chemically grown ultrathin oxide, providing both field-effect and chemical passivation for metal contacts. By investigation into poly-Si thickness and thermal budget, symmetric test samples show a good passivation of 5.4fA/cm^2 J_0 for n doped poly-Si and 10.9fA/cm^2 J_0 for p doped poly-Si.

An optimal n+ c-Si surface passivation of 14.5 fA/cm^2 J_0 is achieved with PECVD deposited a-Si:H/SiN_X stack on textured wafers. For p+ c-Si surface passivation, the influence of thermal ALD Al_2O_3 film thickness and Forming Gas Annealing on Al_2O_3/SiN_X stack is studied. Also an optimal p+ surface with 123 Ω/sq sheet resistance is formed by boron ion implantation approach, which provides space to play with the trade-off between surface passivation and lateral carrier transport for emitter and front/back surface field.

Applying optimized results, bifacial solar cell fabrication enables only one-time high temperature annealing for both highly doped poly-Si and lightly doped c-Si activation. Following such flowchart, n/p bulk rear/front junction test PeRFeCT cells were fabricated, stressing the importance of FSF passivation on solar cell V_{OC} performance.

A good passivated bifacial cell precursor is also prepared with iV_{OC} of 714mV while BHF, poly-etch and TMAH developer in bifacial cell fabrication is proved to over-etch poly-Si passivaitng material, resulting in a poor performance. For further improvement with smooth processing and delicate control of etching steps, a good performed bifacial solar cell with poly-Si passivaing contacts is expected to be fabricated.

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1

Introduction

1.1 Bifacial Technology

Albedo, which is defined as the ratio of the reflectivity of a light from a surface to the incident light or radiation, is an important factor worth considering for PV modules installation in frequently snowy places or places with changeable weather conditions [1]. Installed with common monofacial PV modules, only light illuminated on front side can be utilized and converted into electrical energy. Distinguished from the conventional ones, bifacial technology is a good candidate under these conditions. As shown in figure 1.1, bifacial solar cell also has metal grid patterns presented on back side thus the fundamental value of this technology is the ability to give utmost utilization of reflected light and allow for increased power generation with same occupied area as monofacial panels [2]. Another benefit is that due to reduced infrared absorption in open-grid rear metallization, solar cell substrate working temperature can be reduced [3] ensuring a better inner performance i.e. power output of solar cell.

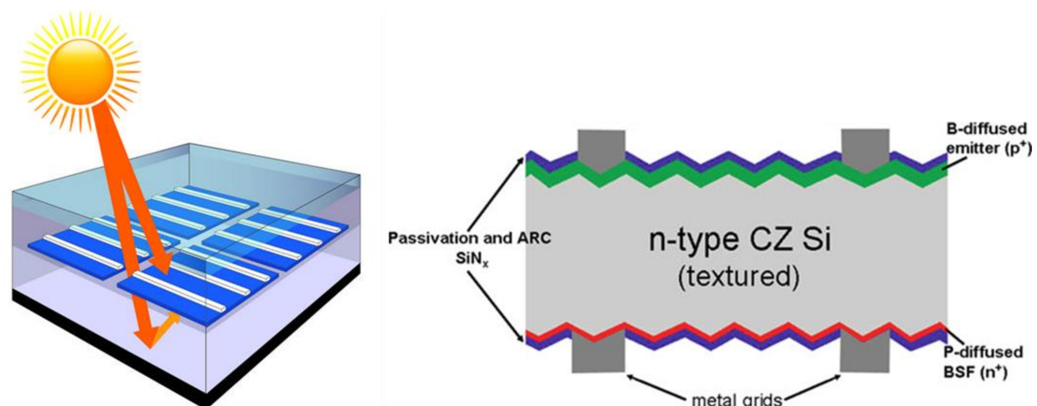


Figure1.1 Schematic illustration of bifacial module light capture from rear side (left); and Yingli PANDA Bifacial solar cell [4] (right).

As an early developer of high efficiency bifacial technology, ECN achieved over 20.0% efficiency on n-pasha cell, a bifacial solar cell with homogeneous diffusion and screen-printing metallization on 239 cm^2 CZ wafers as shown in Figure 1.1(right). This cell is currently produced on industry scale by Yingli Solar for its Bifacial PANDA modules, providing the highest efficiency via low-cost industry processing [5]. Rewarded with the Advanced Technology Product Certification of Top Runner Program in China, Yingli PANDA Bifacial technology continues to gain industry and market recognition [6]. It's worth mentioning that thanks to this innovative technology, Tempress Systems BV has opened Europe's largest bifacial PV plant in Vaasen, the Netherlands. 1428 PANDA Bifacial solar modules were installed enabling over 400kilowatt-peak capacity with up to 30% more energy production than monofacial implementation [7]. This projected was also granted with a SDE+ subsidy form Dutch ministry of Economic Affairs with the aim of encouraging renewable energy in the Netherlands.

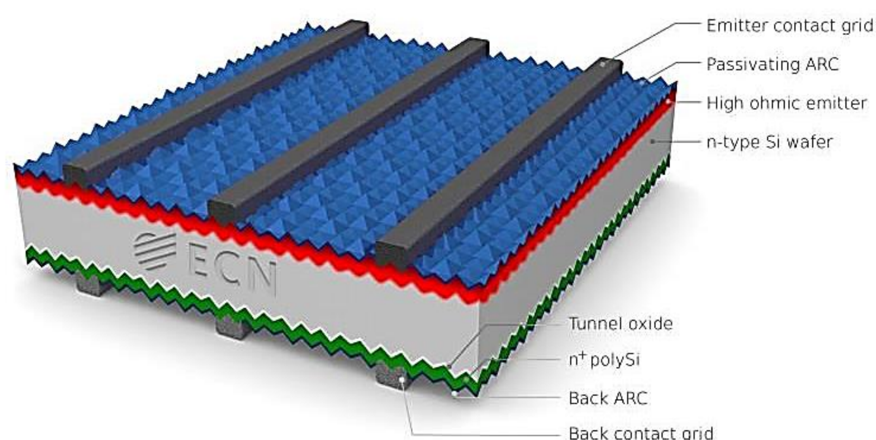


Figure1. 2 n doped poly-Si applied as rear contact in n type bifacial PERPoly solar cell [8]

With the appilication of $POCl_3$-diffused n type poly-Si passivating contacts, a bifacial PERPoly (Passivated Emitter Rear Poly-Si) solar cell has been manufactured with low-cost industrial process, achieving 676 to 683mV V_{OC} and J_{SC} above 39.4mA/cm^2 targeting efficiency potential above 23%[8]. This device reveals that not only lab-level, high efficiency bifacial solar cell can also be expected in industry mass production.

With the emphasis of albedo, bifacial photovoltaic technology stands head and shoulder above the rest and starts to call on its play. Based on the survey from ITRPV, worldwide market share for bifacial technology is in a tremendously increasing trend and will reach 40% by 2028, as shown in Figure 1.2 [9]. This statistic counts in 'non-standard' case that bifacial solar cell mounted in monofacial PV modules. While the expected ratio for 'true' bifacial would also increase to 35%.

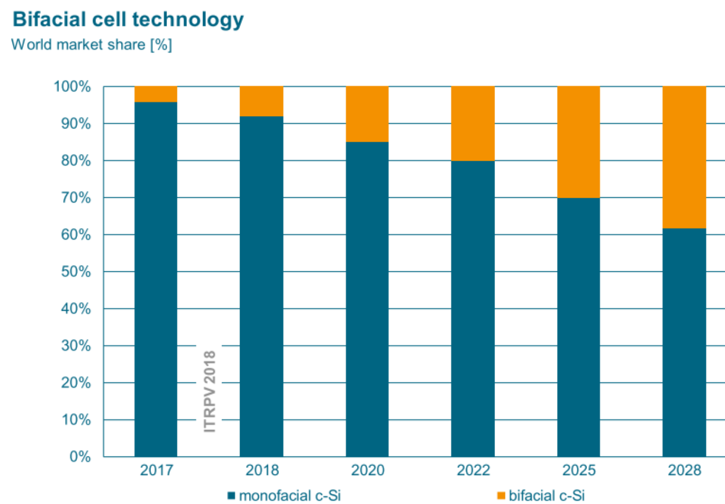


Figure1.3 Worldwide share of bifacial c-Si solar cell technology by ITRPV [9].

Taking an overview of the whole PV market, mono PERC technology will still maintain a mainstream in 2018-2019 but it can be a bridge to bifacial adoption in PV industry [10]. This transition can be really fast once the PERC become an industry standard. Because for mass production, among various routes for c-Si module to obtain bifacial performance, the easiest is to upgrade PERC process and manufacture rear side straightforward. Especially for bifacial PERC production, most PERC manufacturing techniques can be inherited, which illustrate the best approach to realize low LCOE.

As a new face of PV industry, bifacial technology is expected to be a good niche product entering semiconductor industry. Many leading companies including LG, LONGI, Prism Solar, Silfab, Trina Solar and Yingli Solar have started their bifacial business and fastened their step to advanced bifacial technology [11]. However, still efforts are required for research and development to further increase cell efficiency and module power production per unit area. In this project, poly silicon passivating contacts are applied to bifacial crystalline silicon solar cell only underneath metal grids. Compared to standard bifacial PERC configuration, in this advanced structure, poly-Si and tunneling oxide

significantly reduce contact recombination and lightly doped c-Si with high transparency is designed as FSF/BSF and emitter. Such architecture is expected to provide sufficient surface passivation, contact passivation and also less parasitic absorption for both front and rear side on c-Si solar cell.

1.2 Recombination and Passivation

1.2.1 Recombination Mechanisms

When solar cell devices illuminated with light source with equivalent or higher energy than its bandgap energy, the electrons with energy lower than valence band E_V will absorb photon and be excited to conduction band E_C. A vacancy is left behind in valence band called 'hole' [12]. Followed up by the generations of electron-hole pairs, they are separated and collected by certain semipermeable membranes adjacent to absorber, which is called p-n junction. For example for n bulk c-Si substrate, electrons are collected in BSF and holes are collected in emitter. They flow to the terminal of each junction and then pass through the external circuit to convert into electrical energy. While during this path, photon-generated carriers still have a chance to recombine either in bulk or surface (interface). This is detrimental for high efficiency solar cell because this recombination significantly lowers effective carrier transport and reduce carrier lifetime. To be specific, recombination can be divided by bulk recombination, which includes radiative recombination, Auger recombination and Shockley-Read-Hall (SRH) recombination; and also recombination on surface.

Opposite from radiative generation, which is the main generation mechanism of e-h pair, radiative recombination mostly happens in direct bandgap material [12], which is not the case for c-Si because photon energy and momentum are conserved simultaneously. Thus radiative recombination is not dominant in our crystalline silicon material.

Auger recombination is a three-particle involved process and is the main limit for theoretical efficiency of c-Si solar cell reaching maximum 29.43% [13]. The third particle absorbs energy and momentum, drives to higher level in E_C (or lower in E_V) and later returns to original energy state releasing what is absorbed and transfers into lattice vibration and heat.

Different from the former two mechanisms in defect-free semiconductor, SRH recombination happens with the existence of impurities or defects. Such as Fe, lattice

faults and dangling bonds at grain boundaries, all can present defects in bulk. They act as recombination center and induce trap states, an allowed energy level within the forbidden gap. Because of the unavoidable defects during solar cell fabrication, SRH also contributes to most of c-Si solar cell recombination. Surface recombination is a special case for SRH recombination.

By definition, the rate of surface recombination U_S with unit of $cm^{-2}s^{-1}$ can be expressed as a function of interface defect density N_{it}, with unit of cm^{-2}; hole and electron capture cross sections $\sigma_{p/n}$; and surface electron and hole density p_S and n_S [14]:

$$U_S = \frac{(n_S p_S - {n_i}^2)v_{th}N_{it}}{\frac{n_S + n_1}{\sigma_p} + \frac{p_S + p_1}{\sigma_n}} = \frac{n_S p_S - {n_i}^2}{\frac{n_S + n_1}{S_p} + \frac{p_S + p_1}{S_n}} \approx \frac{n_S p_S}{\frac{n_S}{S_p} + \frac{p_S}{S_n}} \quad (1\text{-}1)$$

Here v_{th} for thermal velocity of electron, $n_1 p_1$ statistical factors, n_i intrinsic carrier concentration and $S_{n/p} = \sigma_{p/n} v_{th} N_{it}$. By supposing a single defect at midgap, some parameters are neglected while normally surface defects are placed throughout the whole bandgap. Thus D_{it} [$eV^{-1}cm^{-2}$] is applied to replace N_{it} for an integral. As illustrated in equation (1-1), surface recombination can be reduced with decreased N_{it} or $n_S p_S$.

1.2.2 Surface Passivation

As introduced above, surface recombination can be suppressed by reducing surface defect density, a chemical passivation or by reducing surface electron/hole concentration with induced electric field thus called electric field passivation.

By growing ultrathin layers like SiO_2 or a-Si:H films, dangling bonds at c-Si surface can be saturated with the formation of Si-O or Si-H bonds. Typically these layers are deposited by Chemical Vapor Deposition with precursor gases reacting with substrate and growing high-quality thin layers to passivate dangling bonds. Nitric acid or hydrofluoric acid also forms Si-O or Si-H bonds to terminate defects on surface.

When electron and hole concentrations are equal at surface, recombination rate reaches its highest point [12] thus by reducing one of those values, U_S can be significant inhibited. Such a performance is normally induced by creating a highly doped n+/p+ region via thermal diffusion, ion implantation or CVD. p+-p or n+-n junction and various doped p-n junction show good field effect passivation. Beyond this, by applying a dielectric layer with high charges also induce an internal electric field inside this insulator,

preventing the accumulation of one specific carrier. This carrier selectivity is also one form of electric field passivation.

1.2.3 Passivating Contacts

For high efficiency homojunction solar cells, a certain limit has been reached and large recombination at metal/silicon interface weakens the device performance, remaining to be a huge obstacle all the time. This is because metal always has large number of states in forbidden c-Si bandgap [15], which becomes quite active when contacting silicon bulk thus efficient recombination occurs lowering device performance. With such high barrier height in bandgap, direct metal contacts show apparent resistivity and poor selectivity for either carrier. That's why compared with heterojunction, where metal does not contact silicon absorber directly, there's still long way to go for homojunction device to hit higher V_{OC}. Consequently a contact with less than $5fA/cm^2$ J_0 is needed enabling good majority carrier contacts [13]. As illustrated in figure 1.3, both hole-selective contacts and electron-selective contacts are in demand.

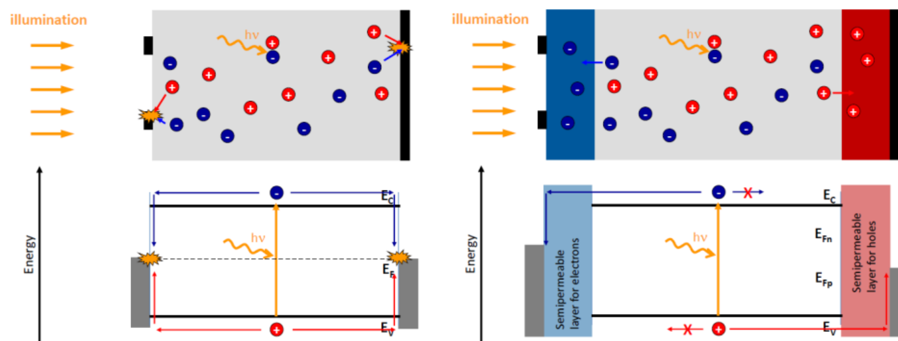


Figure1.4 Illustration for typical cell and with electron/hole passivating contacts [16].

Fundamental Concepts for Passivating Contacts

Equal carrier current under open-circuit condition results in an extremely high J_0 around several thousand magnitude. Origin from the low base, lower hole conductivity σ_h than electron σ_e (figure 1.5a) is achieved but it's not sufficient to annihilate high J_0.

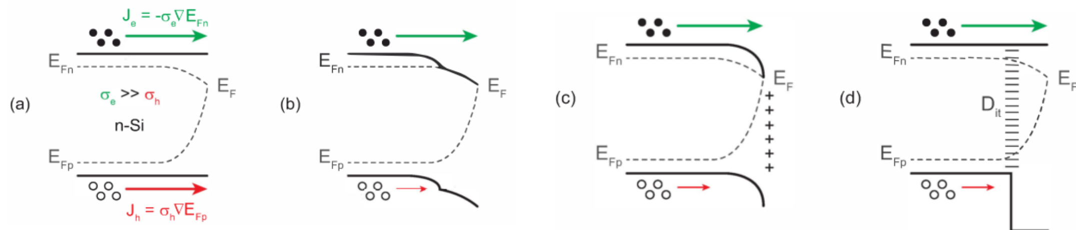


Figure1.5 Band diagram illustration for (a) n-Si wafer with metal contact, not showed but

at right side; electron selective and passivation induced by (b) an n+ doped c-Si layer as metal/ bulk interface; (c) an external introduced band bending; (d) a band offset by contact with a higher band-gap material [15].

Normally a classic way to make metal contact selective is to create a doped surface as figure 1.4b, i.e. emitter or BSF in PERL and PERC structure. In this way selectivity is ensured with higher doping and certain minority carrier conductivity correspondingly. Meanwhile shortcoming remains: additional inserted Auger recombination and energy expense on thermal diffusion processing for dopant driving. That's why a carrier selective passivating contact is in demand to play. They provide alternative solutions i.e. introduce an external band bending from a larger work function metal or a tunnel oxide layer with fixed charges. For case in fig 1.4c, hole current reduces and electron selectivity is achieved. Another method is to contact c-Si with a wider band-gap material while ensuring least conduction band offset. Mature application is the invention device IBC-SHJ, which achieved efficiency 26.7% by Keneka [17] with good care of interface chemical passivation.

Examples for Current Passivating Technology

Nowadays examples like hydrogenated amorphous silicon (a-Si:H), hydrogenated amorphous silicon nitride (a-SiN_x:H), dielectric silicon oxide (SiO_2) and aluminum oxide (Al_2O_3) layers have already been successfully applied to provide passivating function.

a-SiN_x:H or SiN_x for its simplify, is widely used as ARC for its optical properties. Considering passivation, its performance depends on film deposition [14]. If it's Si-rich with low nitrogen content, it provides high chemical passivation as a-Si layer. If it's N-rich, due to a large density of fixed charge, field-effect passivation is playing the role.

For thermal SiO_2, they exhibits a rather low surface recombination velocity (S_{eff}<10 cm/s) [14] because the induced hydrogen content during annealing passivates electronically active defects. Both n/p type c-Si with a great range of doping levels benefits from such a high extend chemical passivation.

These layers can provide good passivating performance to reduce recombination in surface but they cannot give either high conductivity for electrons or holes. This is due to the fact that neither conduction band nor valence band of two materials are not

good-aligned, as shown in figure 1.4(a) [15]. Instead, an electron-selective contact would have conduction band aligned and valence band offset (figure 1.4 b). It creates a far more long distance for hole quasi Fermi level with valence band. So reduction of hole concentration makes this inner layer electron-semipermeable.

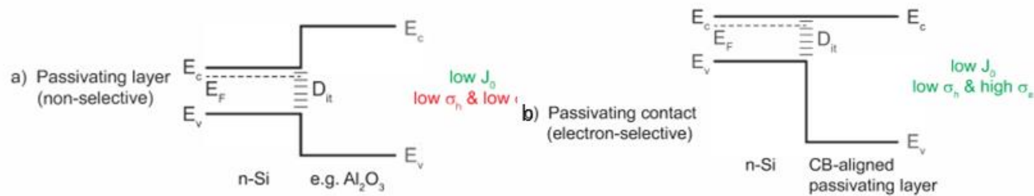


Figure1.6 Schematic band diagram of (a) passivating layer with little selectivity (b) electron selective passivating contacts [15].

Poly-Si Passivating Contacts

In this project, doped poly-Si working together with ultrathin tunneling oxide layer acts as passivating contacts underneath metal grids on both sides of solar cell. This combination provides both chemical passivation from dielectric oxide for its internal fixed charge and field effect passivation induced by highly doped poly-Si layer. This technology is called TOPCon, first implemented on a n type c-Si with boron diffused front and passivated contact at rear [18] (figure 1.7 left) and 25.8% efficiency is achieved as world record for a solar cell featuring top/rear contacts.

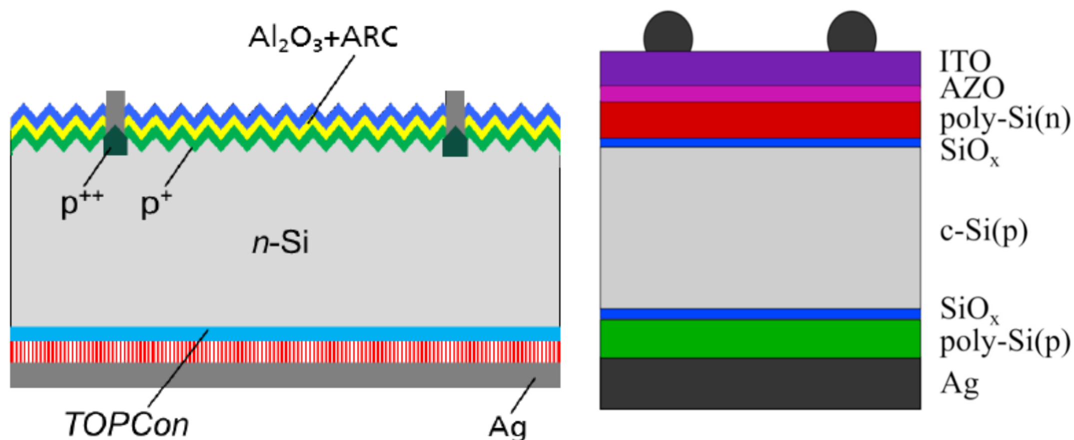


Figure1.7 TOPCon application of n type wafer with boron diffused front and passivated contact at rear[19] and solar cell with top/rear passivated contacts [20].

Also doped poly-Si(O_X) with integrated back contact (IBC) architecture has been implemented successfully within PVMD group, TUDelft. Solar cell performance of 23%

efficiency, 701 mV V_{OC} was achieved [21].

Typically dopants are annealed at high temperature and also as-deposited intrinsic amorphous silicon poly-crystallize through this high temperature activation. Previous results from G.Yang et al. [21] give good description of relation between implantation dose and dopants distribution as shown in figure 1.7.

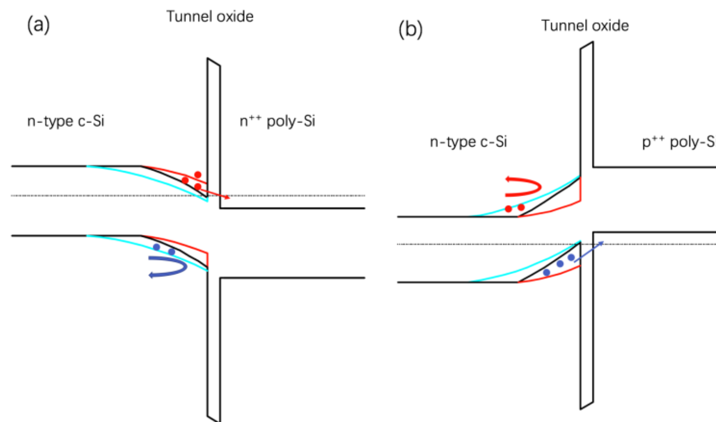


Figure1. 8 Schematic illustration for band diagram of (a) n doped poly-Si contact (b) p doped poly-Si contact, where blue lines for too deep diffused dopants; red lines for shallow doping and black lines for optimal cases [22].

A too high implantation dose gives too deep diffusion for dopants into c-Si. Though selectivity is formed by valence band offset (c-Si versus poly-Si, thus reduced hole conductivity and electron selectivity), the indistinct concentration step offers too weak band bending [22]. Also high dopant concentration at c-Si surface leads to high Auger recombination. However a too low dose means dopants limits in shallow doping profile, results in a too low electric field passivation. It's not sufficient to reduce minority carrier concentration and provide selectivity because minority still have chance to tunnel through oxide layer, diffuse into poly-Si and recombine with majority. Therefore only with optimal implantation energy, dose and annealing condition, dopants can be well-confined to provide carrier-selectivity for certain carrier and optimal passivation for solar cell performance.

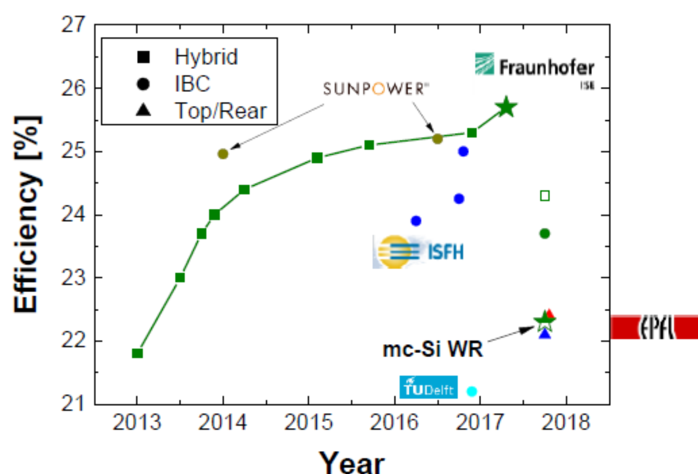


Figure1.9 Novel lab scale efficiency achievement for Poly Si Contacts[23].

However regarding poly-Si material, one disadvantage is the parasitic light absorption especially in long wavelength range, making the application of front poly-Si(O_X) potentially problematic. Also due to the high resistive character of this material, carrier mobility is limited, dramatically affecting FF. Recent approach is to suppress parasitic absorption induced by thick poly layer by reducing its thickness to 10-40 nm range [20]. Such a symmetric passivating layer enables solar cell (figure 1.7 right) parameter up to 709 mV V_{OC} and over 81% FF. As shown in figure 1.9, till now highest lab efficiency for poly-Si passivating contacts has reached up to 25.8% for hybrid configuration (passivated boron diffused c-Si surface on front side with full-area rear TOPCon contact) while there's space for further improvement for IBC and top/rear cell implementation [23].

1.3 Motivation for Developing Bifacial Solar Cell with Poly-Si Passivating Contacts

To suppress parasitic absorption induced by front poly-Si passivating layer, a novel concept comes up with Passivated Front and Rear Contacts (PeRFeCT) solar cell. As shown in figure 1.9, both high transparency and low recombination rate can be ensured by employing a carrier-selective n type poly-Si passivating contact to a standard homojunction front surface. Thanks to the optical transparent lightly-doped front side with poly-Si only underneath metal grid, high current density can be promised. At back side full area p doped poly-Si is deposited as rear passivating contact. Opto-electrical simulation[24] of this front/rear contacted architecture provides a potential efficiency over 26% and based on optimization of FSF, $2.8\ cm^2 \times 2.8\ cm^2$specificated solar cell reported 20.1% efficiency.

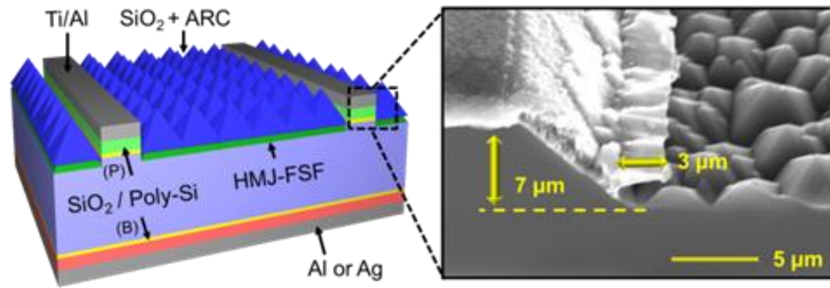


Figure1.10 Schematic structure for PeRFeCT cell and cross-sectional SEM depicting black-dashed detail on complete device [24].

In this project, a bifacial solar cell is to be fabricated with PeRFeCT concept on both sides as passivating contacts to enhance light absorption from both front and rear sides. As illustrated in figure 1.10, for a n bulk bifacial architecture, n doped poly-Si passivating contact with tunneling oxide under metal grid is expected to effectively reduce metal contact recombination and also passivating layer stack is capped to reduce surface recombination on front lightly doped c-Si. At the other side, p doped poly-Si together with tunneling oxide also acts as passivating contact underneath rear metal grid and passivating layers such as Al_2O_3/SiN_X stack are deposited for p+ c-Si surface passivation.

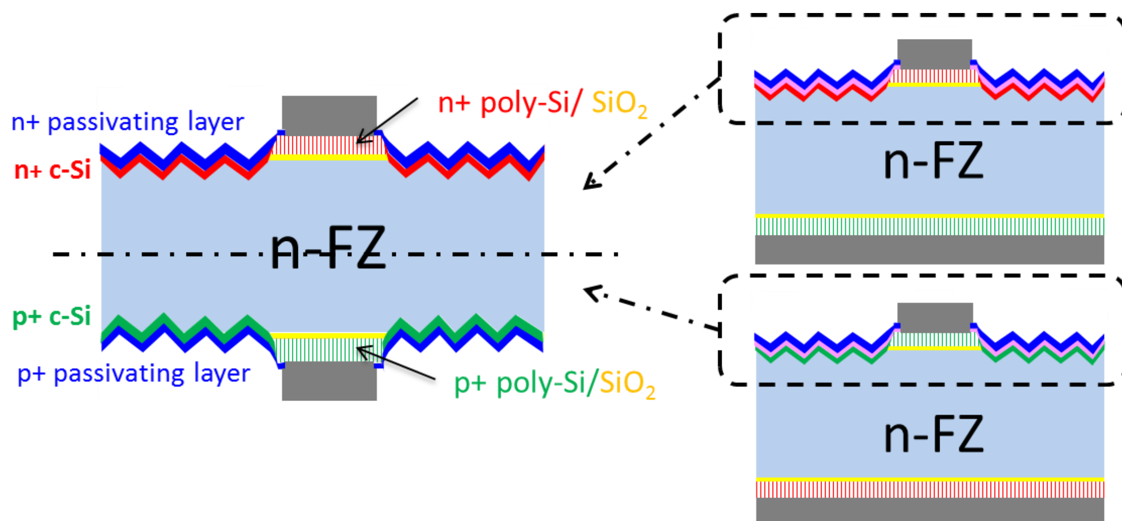


Figure1.11 Schematic structures of the proposed bifacial solar cell with poly-Si passivating contacts and its origin concept of n bulk rear/front junction PeRFeCT cell.

According to previous investigation within PVMD group, excellent passivation quality has been revealed on symmetric structure with n type flat wafer deposited with 250nm poly-Si passivating layer. Best effective lifetime of 15 ms and least J_0 of 4.5fA/cm^2 was achieved on phosphorous implanted poly-Si and 5.4 ms τ_{eff} with 11.5 fA/cm^2 J_0 was

obtained on boron implanted poly-Si [21]. This verifies its promising application on bifacial architecture as front and rear passivating contacts. The demand is driven to seek for an optimal emitter and front/back surface field which eventually give more space to play with their passivation properties and literal carrier transport or in other words, for solar cell V_{OC} and FF. Besides, the optimal annealing condition for passivated c-Si surface also has an influence on poly-Si performances, this correlated optimization should also be investigated for its integrated adjustment into a feasible bifacial solar cell flowchart.

The **main research question** of this project is:

Whether a bifacial solar cell with poly-Si passivaitng contacts can be fabricated with optimized doped poly-Si performance and reduced n/p+ c-Si surface recombination?

Considering the above requirements for poly-Si material and c-Si surface, **detailed scientific questions** are brought up:

1. What is the optimal thickness of poly-Si passivating contacts and how does the annealing condition influence its performance?

2. What is the optimal thickness of a-Si layer on textured phosphorous doped c-Si to improve n+ side front surface field passivation?

3. What is the optimal thickness for Al_2O_3 film to achieve a good passivation on textured p+ c-Si surface and how is the influence of Forming Gas Annealing to Al_2O_3/SiN_X passivating stack?

4. Aiming to play with the trade-off between carrier transport and passivation, what are the optimal implantation parameters and thermal budget for boron ion implantation approach with an optimal sheet resistance on p+ c-Si surface?

5. Whether a feasible flowchart can be designed for bifacial solar cell fabrication with different bulk material and optimal annealing condition adjustment?

1.4 Thesis Outline

Five chapters are included for the finalization of this thesis report. Brief introduction of bifacial solar cell in terms of its enhanced productivity and benefits is described in the first chapter. Theoretical concepts of solar cell recombination and passivation mechanisms are presented as well as state-of-art passivation technologies. Also the

motivation for applying poly-Si passivating contacts and novel PeRFeCT concept into our bifacial solar cell architecture is given followed by the scientific questions and outline of this project.

Chapter 2 is a detailed description of the main fabrication and characterization techniques implemented in this research.

Optimization of solar cell passivation is presented in Chapter 3. Firstly the thickness and annealing condition influence on flat surface n/p-implanted poly-Si material is investigated for the improvement of contact passivation. Then optimization was made for textured n+ c-Si surface passivation with varied a-Si film thicknesses followed by investigation into p+ c-Si surface. Influence of Al_2O_3 film thickness and FGA is studied in this section together with effort for an optimized sheet resistance for p+ c-Si surface formed by boron implantation with various implantation dose and annealing conditions.

Chapter 4 provides the performance analysis of PeRFeCT devices and bifacial solar cell with poly-Si passivating contacts. A flexible flowchart is first introduced as an overview of fabrication with all these optimized processes followed by n type rear junction PeRFeCT cell performance compared with reference configuration. Also J_{SC} performance regarding EQE is presented to distinguish front/rear junction solar cell and importance of FSF passivation is stressed by comparison among four PeRFeCT cell structures. In the final section, n/p bulk bifacial cell characterization is discussed.

Conclusions and outlooks for this thesis project are presented in Chapter 5.

2

Experimental Setup

2.1 Fabrication Techniques

In this section, techniques aiming for bifacial solar cell with poly-Si passivatng contacts are introduced. For doped poly-Si formation and activation, LPCVD, implantation and following high temperature annealing are used. Photo-lithography series are applied for poly-finger formation on both sides of wafers. TMAH texturing is implemented to create 'random pyramid' on surface, improving light trapping. To achieve surface passivation, thermal ALD is applied for Al_2O_3 deposition at 250 °C. a-Si and SiN_x deposition is achieved by PECVD at 250 °C, 400 °C respectively. Metal evaporation is used for solar cell front and rear metal contact formation followed by a lift-off process.

2.1.1 LPCVD

Regarding poly-Si passivating contacts, intrinsic poly-silicon layers are deposited in a high temperature LPCVD (low pressure chemical vapor deposition) furnace from Tempress. The typical reactor shown in figure 2.1 is horizontal, hot-wall, resistance-heated, fused-silica tube design. Equipped with quartz boats, vertically oriented slots are place for holding wafers. Principle for wafer placement is the close spacing, which ensures deposition process uniform across each wafer surface within a reaction-limited deposition regime [25]. Deposition rate has an exponential relation with substrate temperature which theoretically asks for a precise temperature control for such system.

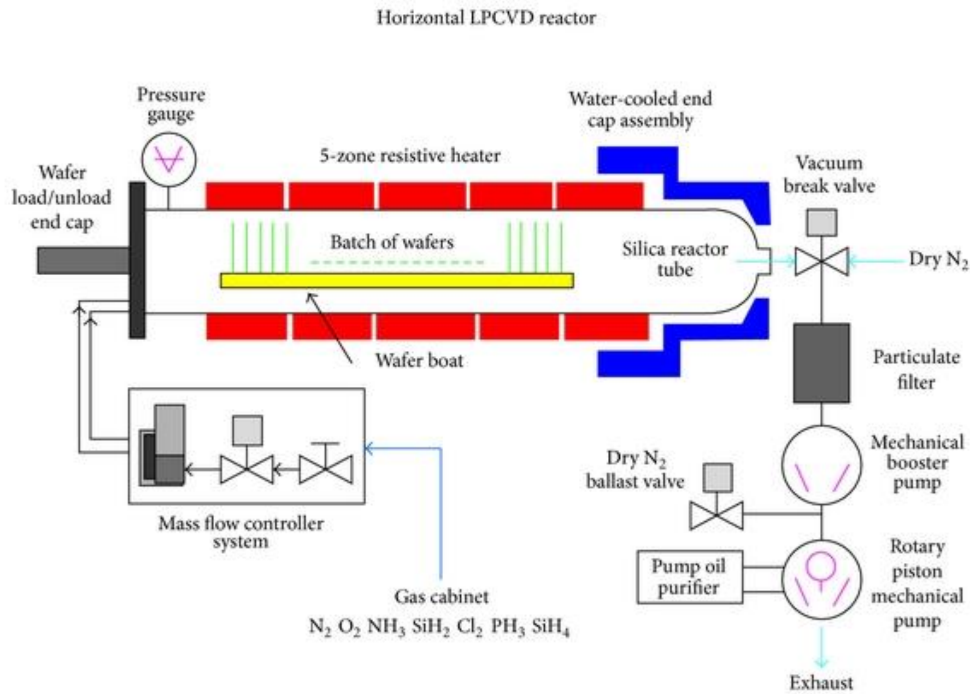


Figure 2.1 Schematic representation of LPCVD reactor for undoped Poly-Si deposition [26].

LPCVD is similar to other CVD process that it's a process where gaseous species reacts on solid surface and results in a solid phase material. What differs from other CVD is that LPCVD lowered pressure slows down diffusion by 1000 and velocity of mass transport also decrease, contributing to a closely approaching substrates and guaranteed uniformity & homogeneity [27].

LPCVD undoped poly-Si is deposited when silane is decomposed into silicon and hydrogen when temperature over 580 °C. Pressure range is within 150 mTorr and silane (SiH_4) – phosphine (PH_3) 1% mixed gas for doped or undoped poly-silicon. The desired deposition rate is 5nm/min depending on temperature and gas flow [28], while in EKL CR100, our measured rate is approximately 2nm/min. In our work, direct absolute thickness measurement is not available thus spectroscopic ellipsometry is implemented for estimation.

Generally LPCVD process is a promising technique for its repeatability and pinhole-free characteristics. To be specific, both annealing and doping parameters together with LPCVD deposition all contribute to poly silicon properties optically, structurally and

electrically [8]. Technically in a research by ECN, above 595 °C morphology for poly-Si would be fine-grained, 'columnar and pinhole-free' (roughness$\sigma_{RMS} \approx 3\%$) while below this, crystalline precipitates can be visible and amorphous-like poly layers (roughness$\sigma_{RMS} \approx 1.8\%$) are deposited. Deposition temperature at which amorphous structure transits into columnar is defined but variables like deposition rate, pressure also matters. Besides, silane flow has an influence: lower flow or concentration results in a much thinner layer with void formation observed [8]. In this project intrinsic a-Si like layers are deposited both sides of wafers at a temperature of 580 °C followed by an annealing step at 600 °C for an hour to release the stress [21].

2.1.2 Implantation

Ion implantation is a low-temperature physical and/or chemical modification of surface material by bombarding materials with a beam of very high energy ions [29]. Historically the first ion implanter is helium based and one of the first references for ion implantation application in solar cell dates back to 1964. At that time, King and Burrill used a Van de Graaff electrostatic accelerator to accelerate boron or phosphorous ions, which were generated by microwave ion source [30]. Till the end of 1970s, in-line, wafer-to-wafer, high throughout commercialized ion-implanter has been widely used. It was firstly applied to dope semiconductor material and then years after also used for metal properties improvement.

Generally three parts are included: ion source, accelerator and target chamber. Ions of desired element are generated and electrostatically accelerated to high energy finally strike on a target, which is wafer in our case. Actual amount of material implanted in the target is the integral over time of the ion current [31].

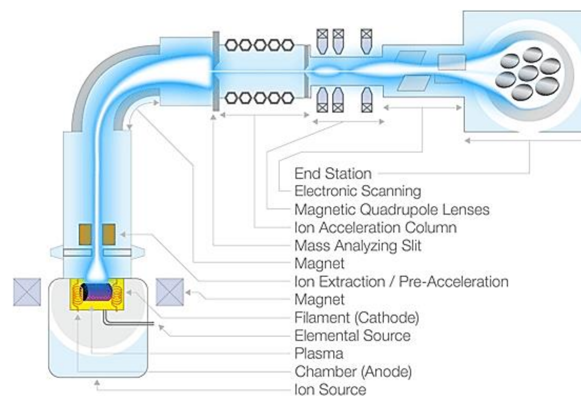


Figure 2.2 Schematic illustration for ion implanter [32].

Owing to its unique characteristic, both beneficial to current cell designs and extendible to future cell architectures, ion implantation has become important role-player for high-productivity solar cell commerciality [30]. Two main techniques being applied are mass-analysis and non-mass-analysis. For the former, ion beam are bended by a large magnet into an aperture. Only ions with desired mass and energy can pass through thus significantly smaller current than initial. For non-mass-analyzed equipment, as its name gives there's no filtering so higher beam currents and lower capital costs are characterized. However this drives to another problem of such a wide range of ion energies would co-implant other precursor species [30].

To obtain a doped amorphous Si like poly layer, Varian implanter E500HP is applied to implant Boron and Phosphorous dose within EKL CR100.

For such technique, one benefit is that only one side is processed so not necessary to etch back the other side. This eliminates the need for removing phosphosilicate glass (PSG) also edge isolation neither [33]. Normally after implantation, to decrease damage on surface, an annealing at 900 °C for 30 min is required to restore silicon crystallinity also driving B/P dopants into silicon for electrical activating. This can be carried out together with surface passivation by a single co-annealing, which largely simplified many cell designs. Beyond these, one reason for choosing ion-implantation is that there's no other way to dope selected areas with an accurately defined amount of dopant atoms and controlled concentration profile. This is extremely important considering our advanced solar cell with poly-Si passivating contacts.

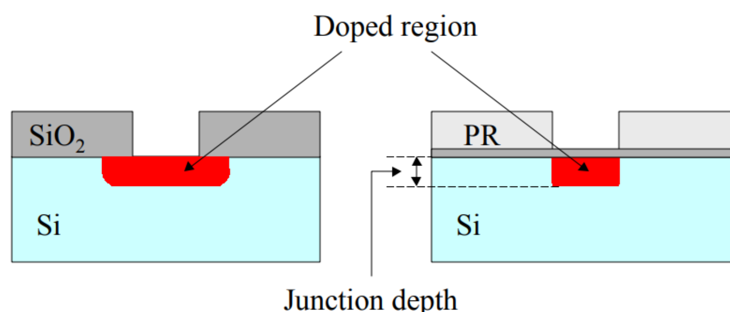


Figure 2.3 Schematic comparison for diffusion (left) and ion-implantation (right) method to form dope region, which illustrate a well-control of both junction depth and desired area by implantation [34].

While it's worth mentioning based on research by Fraunhofer ISE [35] passivation quality

of BF_2 implanted samples annealed at 800 °C exhibits a strong dependence on ion dose, which is not observed with n implantation. Annealed at 900 °C, samples show poor interface passivation irrespective of applied ion dose due to a shallow doping profile and low surface concentration due to short annealing time. They conclude it with high recombination within semi-crystalline silicon or c-Si/SiO_2 interface. Owing to the clustering of boron atoms, this raise up the importance of boron dose optimization. Besides many research explain higher J_0 for boron implanted than phosphorous ones by the fact that P segregates to grain boundaries while B does not. Also boron's solubility limit is much lower than that of phosphorous, which results in higher number of implanted boron atoms not electrically active [35].

It's worth mentioning typically lower implantation energy results in less damage to lattice and correspondingly higher lifetime can be expected [24].

2.1.3 Photolithography

In our daily life, phone, phablet and all popular electronic devices are powered by integrated circuits. Each chip inside is the end product of semiconductor lithography process.

Literal origin of the word 'lithography' comes from Greek, litho meaning stones and graphia meaning to write. Optical lithography is based on the mechanism that light-sensitive polymer (photo-resist) is exposed and developed to form desired feature or image on substrate.

As illustrated below, general series of photolithography steps include:

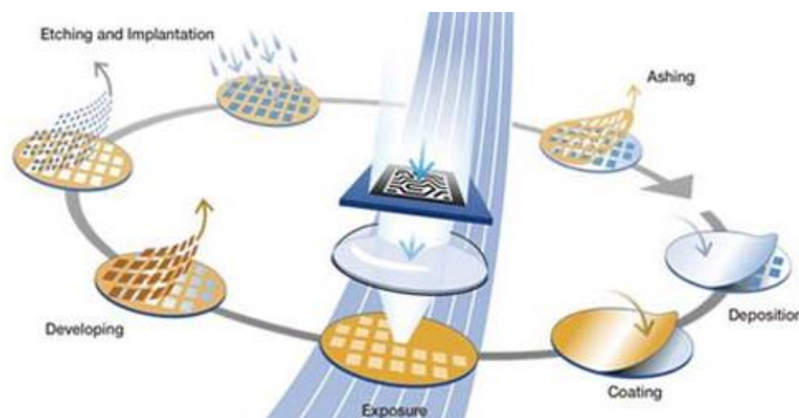


Figure 2.4 Schematic demonstration for photolithography process from ASML [36].

1) Substrate preparation, material deposition or modification

This preparation is intended to improve adhesion of photoresist material to substrate. For example, substrate cleaning to remove contamination, dehydration baking to remove water and additional adhesion promoting. HMDS (hexamethyldisilazane) is commonly applied to dehydrated wafers for achieving the surface hydrophobicity required to prevent photoresist delamination. Thus it improves resist wetting and adhesion [37]. On water-free surfaces, HMDS chemically bonds its Si atom to oxygen of oxidized surfaces releasing ammonia at same time.

2) Photoresist coating and prebake

A uniform, well-controlled specific thickness of PR is applied to a spinning wafer. Temperature and humidity of coating atmosphere, also spinner cleanliness is critical for resist film quality. Basically PR consists of two categories: positive PR which is soluble when exposed; negative photoresist which is soluble in unexposed region. If there's extra PR by edge, it influences the uniformity or even stick to destroy pattern, an edge beam removal is to be implemented. In EKL CR100, coating is automatically processed by EVG120 coater-developer.

Prebake drives out excess solvent within resist film leaving 30-40% weight solvent inside. They evaporate and change resist film properties with time. By prebake and stabilization, films thickness is reduced which makes development easier; adhesion is improved; photoresist becomes less sticky thus less possible to be contaminated [38].

3) Alignment and exposure

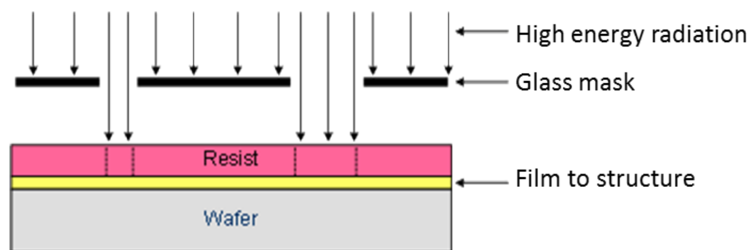


Figure 2.5 Schematic illustration for exposure [39].

Exposure activates photo-sensitive components of photoresist. Before this, a glass mask with fractional covered with chrome is loaded on EVG 420 contact aligner. As illustrated in figure 2.5, desired pattern is defined by mask where light can pass through certain region. Marker on mask is for alignment to wafer. Modern steppers use automatic pattern recognition which takes several seconds to complete align and

expose process. On EVG 420 this step is manually achieved and exposure time depends on thickness of photoresist and light intensity, which is essential to be checked for correct dimension. Bad focus or not optimized exposure will result in improper feature. The longer exposing time, the larger radiated area on wafer. Thus an under-expose is not sufficient to open and conductors may still in contact with each other leading to short-circuit condition. In contrast, over-expose results in small pattern beneath or even disconnected.

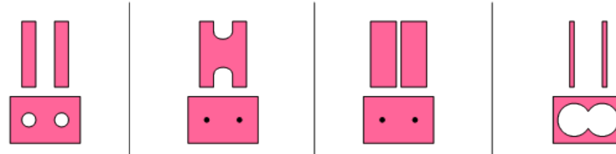


Figure 2.6 Schematic illustration for exposure cases [39]: (1) correct exposure; (2) bad focus, resist remains between line and holes are not opened; (3) under-exposure, lines too wide or connected, holes not opened; (4) over-exposure, lines too thin or disappear, holes too big.

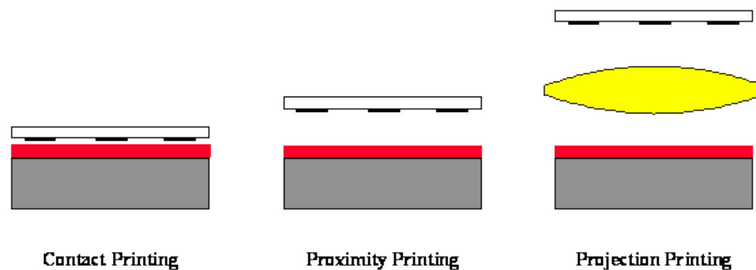


Figure 2.7 Schematic illustration for lithography exposure methods involving contact printing (in the early 1960s), proximity printing and projection printing (mid 1970s to today) [38].

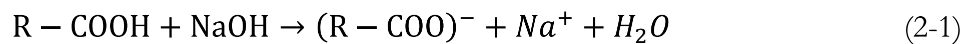
Regarding exposure method, the oldest way is contact printing, which offers high resolution but may cause scratch to mask or damage on resist layer because of too close contact. If particles exist between, optical imaging would be degraded [40]. Thus this method is available only for moderate feature size. While proximity lithography enables mask a distance from wafer (i.e. 20 µm). This provide safety insurance to good photoresist and mask condition but lower resolution. To promise productivity and good imaging at same time, current technology is projection printing. Normally condenser lens and projection lens are implemented thus structures on reticle are enlarged 4 fold or 10 fold. Such an alignment is enabled by step-and-repeat technique which means wafer stage and reticle stage move and align correspondingly. Thereby

only a few dies are projected onto wafer same time. As introduced by ASML product manager Paul Derks [41], the best lithography technology enables good imaging, overlay and productivity, which are also called ' lithography triangle'.

Regarding illumination subsystem, such a step is enabled by light sources i.e. deep ultraviolet (DUV) and extreme ultraviolet (EUV). The main difference between two light sources are the wavelength: the former DUV ranges 248 nm or 193 nm while the latter EUV deliver wavelength of 13.5 nm [42]. EUV lithography is much closer to the size of final features to be printed. With it, manufacturers can turn three or four lithography steps into one [43]. This innovation is critical transition to fulfill Moore's Law, which states price and feature for chips halves every two years. Main technology obstacles for EUV is that exposure has to be processed in vacuum chamber and 13.5nm light absorb by all materials thus no lens could be made for it [36].

4) Development and inspection

In EKL CR100, auto spray development is executed one wafer by one by EVG120 coater-developer. Different recipes can be selected for positive or negative photoresist. Mechanism for develop is that sensitizer formed acid during exposure is neutralized by developer as follows:



$$\mathrm{R-COOH+NaOH\rightarrow(R-COO)^-}+Na^+ + H_2O \quad (2\text{-}1)$$

The advantages for spray development are that chemical is renewed steadily and involved developer is much less. However, manual developing can be carried out with corresponding developer in wet bench when auto developing time is not sufficient to remove soluble photoresist.

The alignment and opening have to be inspected after development. Normally several terms are covered:

- Uniformity of resist layer: it's worth mentioning that resist layer can only be checked with white light or moved to natural light when exposure finished otherwise all area will be exposed. Thus lithography is always carried out in a yellow light house.
- Pattern structure alignment: resist pattern has to be adjusted precisely as desired, not twisted or too shifted. Otherwise resist should be removed and repeat lithography again to ensure good layout.

- Line width: exposure time, developing time and focusing all contribute to this. Certain deviation is allowed as long as i.e. metal contact opening is within poly-Si finger region, not touching silicon region.

5) Pattern transfer

Normally three methods are applied to achieve this: subtractive transfer, basically etching; additive transfer, selective deposition; and impurity doping through ion implantation [38].

For this bifacial solar cell flowchart, pattern transfer is achieved by acid etching. Normally before lithography a uniform layer of silicon nitride or silicon dioxide is deposited above bulk for protection. Within area still with photoresist, etching is not going so layers underneath are protected. While for regions without resist protection, BHF (1:7) or other wet chemical solution i.e. 0.55% HF is applied to etch away SiN_X (or SiO_2) sacrificing layer. A hydrophobic surface is shown indicating opened areas are without SiN_X (or SiO_2) thus leaving poly-Si layer or silicon bulk stay. In EKL CR100, etching line, desired etching time can be calculated based on provided etching rate (indicated below in table 2.1 but only as a reference).

Table 2.1 Etching rates regarding different layers in EKL CR100 etching line.

Layer	BHF 1:7	0.55% HF	Poly-Si etch
Thermal oxide	60-90nm/min	2 nm/min	8-8.5 nm/min
Novellus oxide	220-300nm/min	19-22 nm/min	55 nm/min
PCVD nitride	23-28 nm/min	8.5-9 nm/min	N/A

Normally to ensure the quality of lithography, inspection on etched pattern is to be carried out. If substrate under uncovered region is not etched completely or over-etched that acid etched through the edge of opening though the protected area, feature is not appropriately transferred.

6) Strip, photoresist removal

To finish lithography process, remained photoresist should be removed. This can be done by wet stripping in organic or inorganic solution and dry (plasma) stripping. One commonly used organic stripper is acetone. In EKL CR100, acetone bath is for photoresist removal (only positive PR) at 40 °C. However, acetone tends to leave

residues on wafer. A following St. Cleaning is essential to be processed. Besides, to reduce scum formation, most commercial organic strippers are phenol based or inorganic acid based stripping system at elevated temperature for positive photoresist removal [38].

As the other standard method, both positive and negative photoresist can be removed by plasma stripping. PVA Tepla 300 is applied in EKL CR100 for wafer stripping. Batch of wafers are placed by order with certain space between to allow plasma pass through. Pyrex holder with faraday grid is applied and oxygen plasma also O_2/CF_4 plasma is used. The mechanism behind this operation is that oxygen plasma present highly reactive character towards organic polymers thus leaving inorganic materials under photoresist untouched. This equipment is self-program controlled and an endpoint detection for inspecting whether photoresist is stripped throughout or not. Be careful with wafer picking when recipe stopped for the reason that slightly heated substrate makes wafer fragile compared with normal condition.

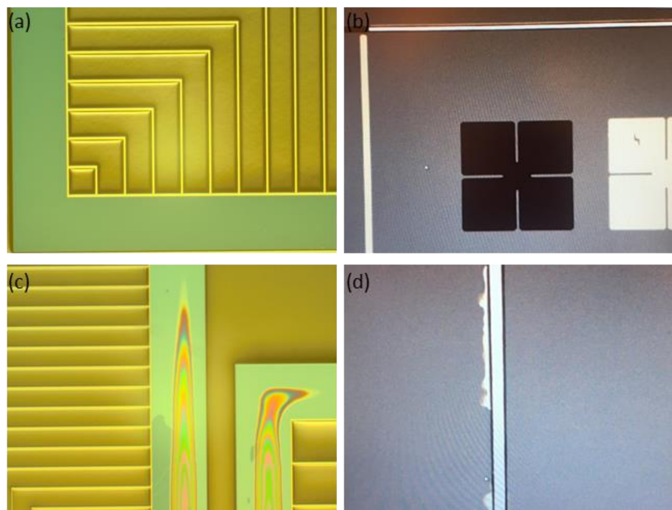


Figure 2.8 Images during wafer lithography processing for (a). good alignment and lithography; (b). misalignment (c). under-exposure, photoresist still remain in opening region; (d). over-etch during BHF contact opening.

During solar cell fabrication in this project, four series counting for eight times lithography are involved to achieve the final architecture. Firstly alignment markers are printed on both sides of wafer to locate the following pattern. Secondly poly-Si finger is created by poly-Si mask design with a width of 6μm. Afterwards, a narrower opening is achieved on both sides of wafer to limit metal and lastly metal contact opening

lithography to define area where metal evaporation processed afterwards. Various situations happened during lithography processing as shown in figure 2.9.

2.1.4 TMAH Texturing Etch

In order to improve light trapping and correspondingly obtain higher current, the state-of-art technique is to induce random pyramids on solar cell front surface.

Alkaline texturing is used to etch the poly silicon between the desired front contact patterns and then to form micro-pyramid. The mechanism behind is that alkaline etchants can texture silicon at lower concentration by selective crystalline orientation. With our commonly used <100> wafer, the <100> and <110> panels are etched while leaving random four-sided pyramids with <111> orientation (which means <111> has lower etching rate). With such structure, light incident onto front surface will be reflected to closing pyramid surface and then couple with those light transmitted into inner structure [44]. So light trapping can be improved also light path length into silicon bulk can be extended in optical aspect.

Texture solution consists of 4L deionized water, 1L 25%TMAH (tetramethylammonium hydroxide) and 120mL ALKA-TEX.8, which is employed to accelerate texture process and extend effective time for solution. A desired temperature at 80°C and rotating speed of 120 rpm with a magnetic stirrer is set for texture solution. Normally with 4 minutes texturing, crystalline silicon wafer would have sufficient micro-size random pyramid and roughly 7μm etch back of bulk material [24]. As shown in figure 2.10 below, the morphology of c-Si surface shows a textured surface with random sized (0.5μm to 2μm) up-right pyramids. Poly-Si finger is protected with SiNx capping while the other open surface area is etched by texturing solution. To ensure the uniformity, a test wafer is processed before starting every batch for the reason that etching rate of TMAH solution varies after use.

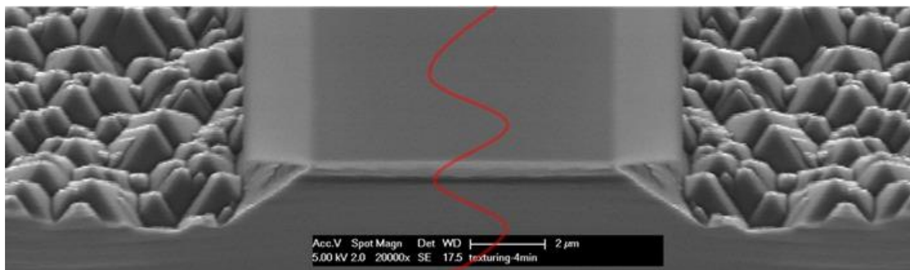


Figure 2.9 SEM image for IBC solar cell front surface with 4min texturing.

2.1.4 Atomic Layer Deposition

To achieve a reduced recombination on p type c-Si surface Al_2O_3 is applied for its extraordinary passivation by negative fixed charge, adequate stability processing and ability to use ultrathin films down to nanometer in thickness [14]. In this project the Al_2O_3 layer deposition is synthesized on Atomic Layer Deposition (ALD) machine Ultratech Fuji G2 in Kavli Nanolab.

As a new technology in the field of c-Si nanolayer manufacturing, ALD technique is based on sequential use of gas phase chemical and is generally considered as a subclass of chemical vapor deposition. Self-limiting surface reactions are achieved by ALD. Typically two precursors are used. Each period substrate surface is exposed to one precursor when gas-phase reactant reacts with the surface functional group. It ends automatically when all available surface groups are consumed then process alternate to the other precursor. Remaining former precursor and reaction products are pumped away in 'purge' step as indicated in figure 2.10, at same time latter precursor is introduced. The film grows by changing in precursor ABAB pattern. This strict separation between precursor behaviors contributes to 'self-limiting' character. During each cycle, one or less than one atomic layer is deposited and ALD cycles end when determined thickness is reached. Differ from PECVD, film growth rate on ALD is not related to precursor flux on surface. Thus designed with sufficient precursor exposure time, same amount of atomic layer is formed everywhere on surface.

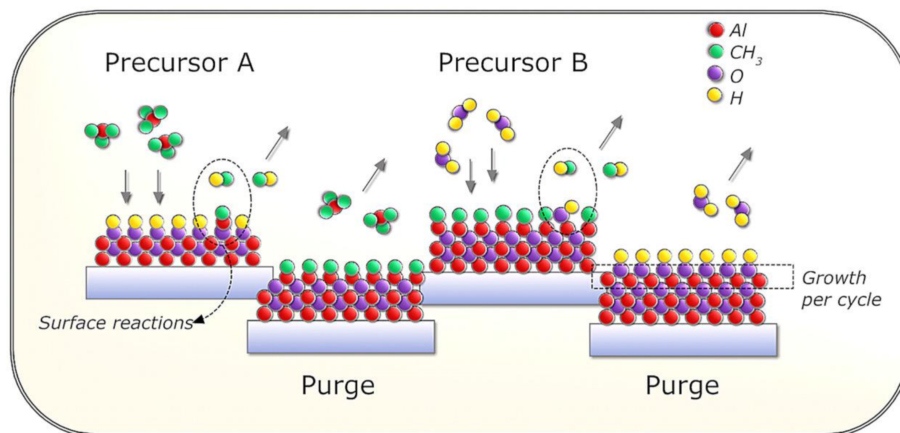


Figure 2.10 Schematic illustration for two precursor reacting steps and two purge steps during ALD cycle [14].

As stated above, the precise thickness control and uniform deposition make ALD a

promising technique for the passivation of c-Si surface as required for high efficiency c-Si solar cells.

TMA ($Al(CH_3)_3$ or trimethylaluminum) is often used as ALD deposited aluminum oxide precursor. Normally water, ozone or oxygen radicals from plasma can play the role as the other oxidants. Water and ozone involved are classified as thermal ALD and plasma assisted is named plasma ALD. Based on application different choice can be made [45].

2.1.5 Plasma Enhanced Chemical Vapor Deposition

PECVD, short for plasma enhanced chemical vapor deposition, is a widely used deposition equipment and in this project, SiN_X or SiO_2 as protection for photolithography and a-Si:H and SiN_X passivating layers for doped c-Si surface passivation, is achieved by Noellus Concept one in EKL CR100 or PECVD in Kavli Nanolab. It consists of radio frequency power generator, gas supply, heater, pump system, reaction chamber with substrate holder. With plasma between electrodes created by RF power, electrons are accelerated and highly energetic to collide with gas precursor. Reactive radicals are formed and deposited on substrate surface. While PECVD is a rather sensitive process, temperature, pressure, gas flow and other parameters all contributes to the deposition quality of final layer.

2.1.6 Thermal and Electron Beam Evaporation

After deposition of solar cell layers, front and back contacts are evaporated onto the substrate. As illustrated below, thermal evaporation and electron beam (e-beam) evaporation are two standard processes within PVMD group. Pumping down to 2.5×10^{-5}Torr, chamber is available to provide a low pressure for electrons passing through electron gun to evaporation material. Metal vapor particles are spread within the inside of chamber and condense back to solid state touching substrate. Samples are placed in a holder with the deposited side facing metal and are rotated at a low speed of 20 rpm to ensure homogeneity. With Provac PRO500S in EKL, an average depositing rate of 1 nm/min can be achieved.

E-beam evaporation is to use a high energy electron beam to heat the target material up to its melting point and then evaporate. Metallic material is loaded in water cooled pocket and electron beam is emitter by filament through a strong electric field. E-beam evaporation is aimed for high melting-point temperature metals like chromium (1860 °C),

titanium (1670 °C) and nickel (1453 °C) [46]. Thermal evaporation differs for the way metal is heated. Source metal is held in a tungsten evaporation boat and high current fed through the boat. Aluminum with 660 °C is suitable with thermal method while an alloy can be forms with tungsten thus for Provac only silver is evaporated by this method. As indicated in figure 2.11, a rotatable pocket containing each four metal material (Al/Cr/Ti), filled within independent ceramic crucibles.

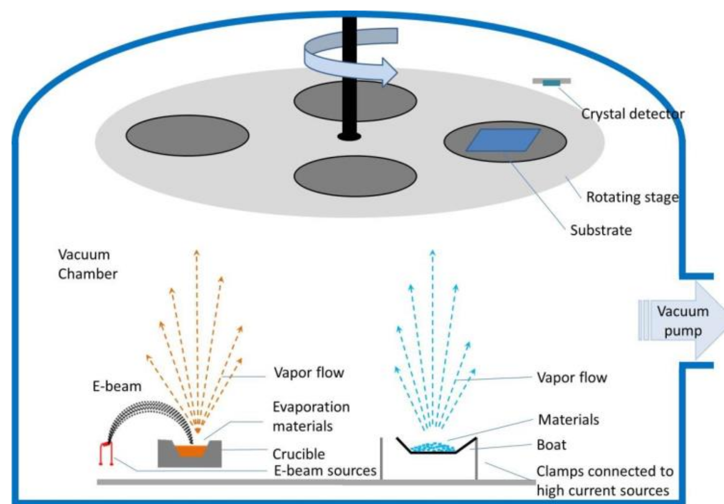


Figure 2.11 Schematic representation of metal evaporation deposition system, PROVAC with two energy sources (a) e-beam evaporation in left side and (b) thermal evaporation in right side [47].

While it's worth mentioning that some drawbacks remain for e-beam evaporation:

1) Electron beam irradiation causes damage on the degradation of semiconductor device due to the induced interface traps. Lifetime is observed to decrease with increasing e-beam irradiation dose [48].
2) Another problem is this process is not available to be implemented for coating inner surface of complex geometries.
3) Certain metal materials illustrate poor e-beam evaporation performance. This can be checked [49] into details.

2.1.7 Metal Lift-off

For solar cell front side or bifacial architectures which have metal patterning on both sides of wafers, a lift-off process is desired as shown in figure 2.13. Substrate is prepared with sacrificial stencil layer i.e. photo-resist. This is achieved by lithography and an inverse pattern is formed so target material can touch the etched openings. While the

latter material covers patterning layer as well so when PR is dissolved by acetone, metal upon will also be washed out. In this way only target material in desired opening (metal finger and bus-bar) with the underlying layer stays[50]. Literally photo-resist thickness should be twice thicker than the thickness of deposited metal. Otherwise it will be not easy to lift-off. Based on measured results, auto coated PR is 8 μm and the other side with manual spinner coating is 4.5 μm at minium level. To guarantee a successful lift-off, 2.5 μm Aluminum is decided.

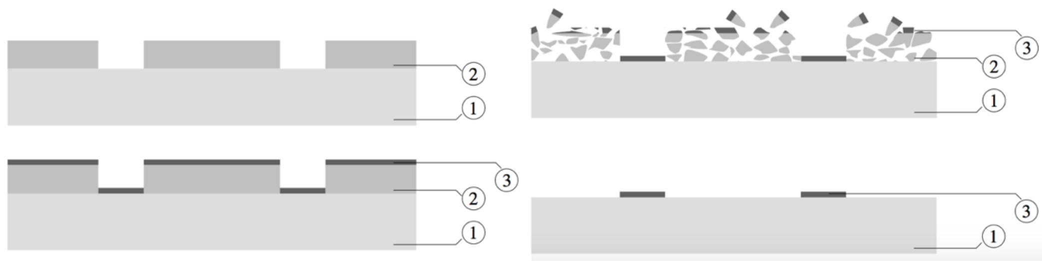


Figure 2.12 Illustration for lift-off steps with (1) substrate (2) sacrificial layer (3) target material [50].

However such a direct process may also lead to problems such as retention, which means unwanted part of metal layer still remain on substrate. This results from non-sufficiently dissolved photo-resist underneath or possibly too adhered metal that makes the lift-off not available. The other disadvantage occurs when metal covers sidewalls of resist and an 'ear' forms [50]which has the possibility to fall over on undesired surface and cause unwanted connections.

2.2 Characterization Techniques

In this section, the methods and equipment for both solar cell and test samples' characterization are introduced into details. Photoconductance decay lifetime tester offers effective lifetime and implied V_{oc} results thus applied for passivation quality evaluation. Illuminate J-V and external quantum efficiency measurement are applied for solar cell device characterization. To investigate an optimal sheet resistance, four-point probe measurement is carried out. SEM is conducted for closer look into surface morphology.

2.2.1. Photoconductance Decay Lifetime Tester

Photoconductance decay measurement is a widely used technique for wafer minority carrier lifetime, which demonstrates passivation quality for poly-Si, boron diffused

surface field and annealing performance etc. An infrared flash will give samples a photoexcitation and excess photons and holes are generated then recombine afterwards to reach thermal equilibrium. But the minority carrier density changes gradually which will give a decay of photonconductance:

$$\sigma_L = q\left(\Delta n\mu_n + \Delta p\mu_p\right)W = q\Delta p\left(\mu_n + \mu_p\right)W \tag{2-2}$$

given $\Delta n = \Delta p$ for n type substrate and Δp for excess carrier density, μ_n μ_p for electron and hole mobility respectively and W for wafer width[51].

The decay of excess charge carrier or absence of trapping is expressed as:

$$\frac{\partial \Delta p}{\partial \mathrm{t}} = -U(\Delta p, n_0, p_0) \tag{2-3}$$

where n_0, p_0 for thermal equilibrium electron/hole concentration, U for net recombination rate, which depends on overall recombination mechanisms inside bulk and on surface.

In our group, here the step-by-step monitoring of passivation performance is conducted by Sinton WCT-120 Lifetime Tester which provides lifetime measurements within 100ns to over 10ms range[52]. As illustrated in figure 2.13, programmable flash lamp with bypass filter is included in setup. Samples are arranged on a temperature-stable (within 22-25 °C) stage and the coil beneath connects samples to an RF bridge. The conductance and incident light density can be measured by calibration instruments and reference cell.

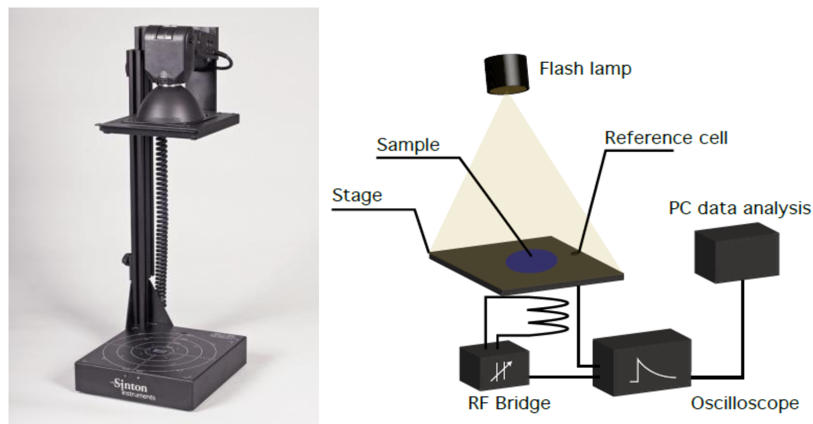


Figure 2.13 Photoconductance decay lifetime tester (left) used in PVMD group [52] and schematic illustration for its measurement mechanism (right) [53].

Upon photonexcitation, following change of conductance, excess carrier density Δp is

obtained and the minority carrier lifetime can be derived according to different analysis modes. For this Sinton WCT-120, quasi-steady-state photonconductance (QSSPC, preferable for $\tau_{eff} < 100\mu s$), transient photonconductance ($\tau_{eff} > 200\mu s$) and generalized lifetime analysis modes are available.

$$\tau_{eff} = \frac{\Delta p}{G - \frac{\partial \Delta p}{\partial \mathrm{t}}} \tag{2-4}$$

where G for carrier generation rate and is acquired through reference cell. In equation 2-4, effective lifetime can be obtained with $\partial\Delta p/\partial\mathrm{t} \equiv 0$ for QSS and $G \equiv 0$ for transient mode.

Also implied open-circuit voltage $\mathrm{i}V_{OC}$ and dark saturation current density J_0 can be deduced. The excess carrier density suggests an $\mathrm{i}V_{OC}$ at which quasi-Fermi level splits. For a n bulk sample:

$$\mathrm{i}V_{OC} = \frac{K_B T}{q} ln(\Delta p)\left(\frac{N_D + \Delta p}{n_i^2}\right) \tag{2-5}$$

where K_B for Boltzmann constant, T for temperature, N_D for donor concentration and n_i for intrinsic carrier concentration. This equation is applicable for any doping level or minority carrier injection level [51]. Normally an implied V_{OC} versus illumination curve is demonstrated and the $\mathrm{i}V_{OC}$ value for passivation measurement is read at one sun illumination.

2.2.2 Illuminated J-V

Wacom WXS-156S-L2 super solar simulator is applied in PVMD group to evaluate the illuminated performance for bifacial and PEReCT solar cells. This simulator involves xenon lamp and halogen lamp combinations to improve artificial spectral distribution and produce standard test condition (AM 1.5 solar spectrum, 1000 W/cm^2). To give stable and reliable measurement results, a cooling system is integrated in stage to maintain 25 °C test condition. Also to verify, two mono-crystalline silicon reference cells from ISE (filtered and unfiltered) are used for calibration.

During the measurement, bias voltage from -1V to +1V is applied so the photo-generated current of illuminated solar cell varies accordingly. External parameters including V_{OC}, J_{SC}, FF and η are determined also V_{MPP}, I_{MPP}, R_{sh}, R_s can be derived. While it's worth mentioning that to reduce the impact of parasitic resistance from probe and metal contacts, a four-probe method is used. Also to indicate measurement uncertainties, hard mask and black paper blocks are used to limit the determined solar cell and isolate it from the others.

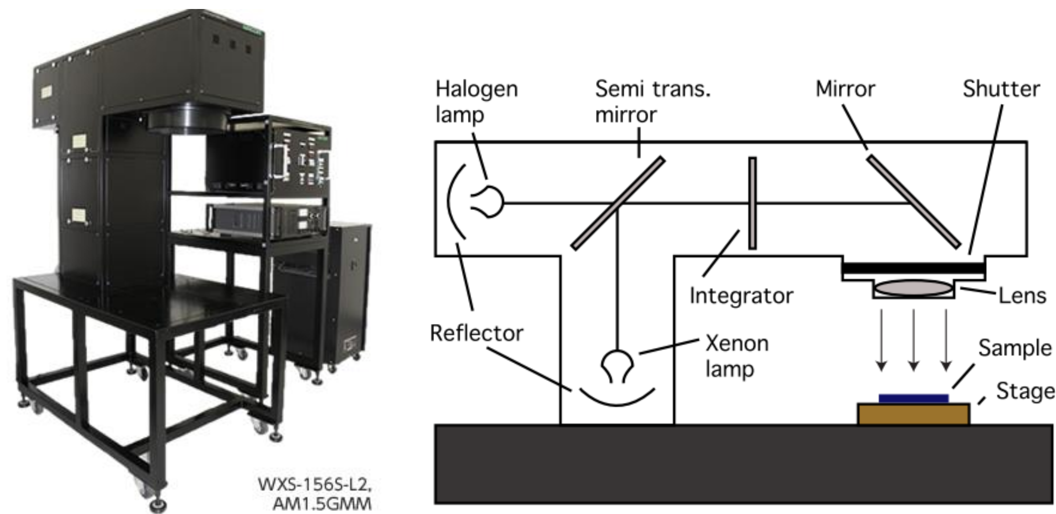


Figure 2.14 Schematic illustration of illuminated J-V measurement.

2.2.3. EQE

External quantum efficiency is defined as the ratio between the number of charge carriers successfully collected and the initial number of photons that incident on solar cell surface. Ideally photons with energy larger than bandgap energy can be absorbed but actually considering parasitic absorption i.e. by passivating layer in this case, reflectance, recombination loss etc., EQE term is determined to evaluate optical and electrical losses for specific solar cell. As a function of wavelength, EQE of determined solar cell is defined as [12]:

$$\mathrm{EQE}(\lambda) = \frac{I_{ph}(\lambda)}{q\phi_{ph}(\lambda)} \tag{2-6}$$

where $\phi_{ph}(\lambda)$ is the photon flux of certain wavelength, specific equal to [12]

$$\phi_{ph}(\lambda) = P(\lambda)\frac{\lambda}{hc} \quad (2\text{-}7)$$

In equation (2-7) $P(\lambda)$ is spectral power density for AM1.5 spectrum, h for Planck constant and c for light speed. Thus compared with Wacom J-V measurement, here standard data from AM1.5 is more accurate than integrated spectrum of halogen and xenon lamps because for the latter, there can be spectral mismatch.

EQE measurement is carried out in an in-house setup within PVMD group. 300W Xenon lamp generates light with wavelength from 200 to 2500nm range, while for silicon based solar cell 300 nm to 1200 nm is sufficient for characterization because above this limit, rare photons are absorbed by c-Si. Before measurement, intensity is checked by silicon and germanium calibration diodes. Light from xenon lamp is chopped at 123 Hz (with aid of chopper controller) afterwards through filters and Oriel monochromator, certain output beam is focus onto solar cell with $3mm^2$ defined area. Lock-in amplifier is used to receive periodic signal modulated from chopper and filter out unchopped noise. The computer compares time-delay induced by generated signal and actual measured value, analyzes spectral response of cell and finally shows as a plot of EQE curve. Illuminated J_{SC} can be calculated as:

$$J_{SC} = q\int_{\lambda_1}^{\lambda_2} EQE(\lambda)\,\phi_{ph}^{AM1.5}(\lambda)d\lambda \quad (2\text{-}7)$$

2.2.4 Four-Point Probe Resistivity

To identify sheet resistance of B-doped c-Si after different annealing conditions, four-point probe technique (Figure 2.15) is applied to evaluate the impurity and passivation performance for ion-implantation. Current goes through two outer probes and voltage is measured across the inner ones. Typically probe spacing s is close to 1mm. In our case, for thin sheet (thickness t<<s), differential resistance is defined as

$\Delta R = \rho\left(\frac{dx}{A}\right)$ where $A = 2\pi xt$ and by integration between inner probes:

$$R = \int_{x_1}^{x_2} \rho\frac{dx}{2\pi xt} = \int_{s}^{2s} \frac{\rho}{2\pi t}\frac{dx}{x} = \frac{\rho}{2\pi t}ln\left(\frac{2s}{s}\right) = \frac{\rho}{2\pi t}ln2 \quad (2\text{-}8)$$

Thus for desired thin sheet $\rho = \frac{\pi t}{ln2}\left(\frac{V}{I}\right)$ with unit of $\Omega.cm$ and sheet resistance can be

derived as: $R_{sh} = {}^{\rho}/_{t} = \frac{\pi}{ln2}\left(\frac{V}{I}\right)$ with the unit of Ω/sq.

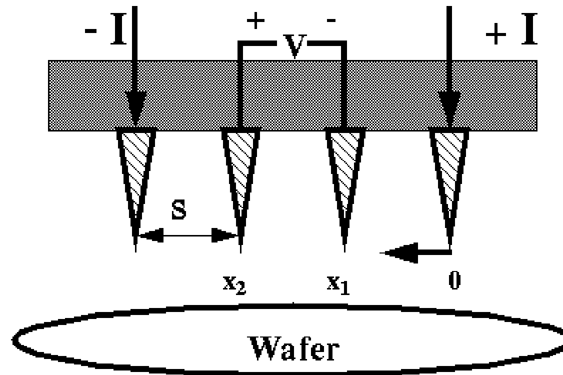


Figure 2.15 Schematic structure for four-point probe sheet resistance measurement setup.

It's worth mentioning that after oxide-atmosphere annealing, a thin layer of SiO_2 is induced at front of diffused samples. BHF solution etching is necessary to remove oxide or it can impede ohmic contact.

2.2.5 Scanning Electron Microscope

Short for Scanning Electron Microscope, SEM is used for detecting surface topology in this project. It consists of electron gun, condenser lens, scanning coil, objective lens, secondary electron detector and a display unit in final stage. Electron beam produced by electron gun is accelerated by lens and throw on samples where tons of secondary electrons are emitted depending on the topology of sample surface. By analyzing the changes of electron numbers detected, surface topology is mapped on final display unit.

3

Optimization of Solar Cell Passivation

To suppress recombination at metal and c-Si interface, in our bifacial solar cell fabrication, poly-Si passivating contacts are implemented. The combination of ultrathin tunneling oxide layer and n/p doped poly-Si layers provide both field-effect passivation and chemical passivation for c-Si surface. In this chapter, influence of LPCVD deposition time, which correlates to poly-Si film thickness together with influence of annealing time and temperature are studied respectively in section 3.1.1 and 3.1.2.

Besides poly-Si passivation contacts, resembling from PeRFeCT (Passivated Rear and Front Contacts) solar cell, highly transparent n+/p+ c-Si surface also contributes to the overall solar cell passivation performance. The objective of section 3.2 is to find optimized solution for the trade-off between good passivation and good conductivity. Compared with n+ c-Si surface passivation (section 3.2.1), p type stays to be a bottleneck thus most efforts are made regarding the optimization of boron diffused c-Si passivation. Influences of forming gas annealing, as-deposited Al_2O_3 film thickness and sheet resistance of p+ c-Si by boron implantation approach are studied individually in section 3.2.2.

3.1 Optimization of poly-Si Passivation

Passivation from doped poly-Si passivating contacts for c-Si consists of two parts: chemical passivation from ultra-thin tunneling SiO_2 layer and field-effect passivation at poly-Si/c-Si interface due to dopants within poly-Si layer induced strong band-bending preventing minority carrier to diffuse toward the interface. Previous investigation showed passivation mainly contributes from field effect passivation and poly-Si thickness,

implantation dose, annealing temperature and time all influence its performance. In this thesis, owing to the unstable performance of LPCVD poly-Si quality and annealing influence both on poly-Si and boron doped c-Si surface, main focus is the optimization of LPCVD deposition time and annealing condition, which will be discussed in section 3.1.1 and 3.1.2 separately.

3.1.1 Influence of LPCVD Deposition Time

To investigate the influence of poly-Si deposition time on n/p doped poly-Si passivation properties, a symmetric structure is fabricated as indicated in figure 3.1. Double side polished n bulk FZ c-Si wafers are wet-chemical cleaned and then Marangoni HF dip to remove native oxide. Then samples are immersed in 69.5% HNO_3 solution to form tunneling SiO_2 layer on both sides. Afterwards, intrinsic amorphous silicon is deposited also on both sides of wafer by low-pressure chemical vapor deposition (LPCVD) with an average deposition rate of 2 nm/min. Implantation is then used to ex-situ dope boron or phosphorous atoms into former a-Si layer. The implantation dose and energy are set at same level for different samples: 5 keV, 5×10^{15} ions/cm^2 dose for n type phosphorous implantation on both sides and 20 keV, 6×10^{15} ions/cm^2 dose for p type boron implantation. To finalize, a high temperature annealing step is carried out in N_2 atmosphere at 950 °C for 5 minutes to drive in and activate dopants. Also this annealing process functions for poly-crystalizing a-Si. It's worth mentioning that for poly-Si passivation, optimized performances were all carried out on flat surface. Therefore in this project, deposition time optimization and its application on bifacial solar cell are both implemented with flat structure.

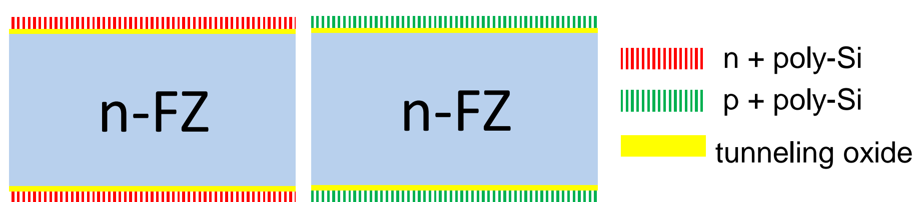


Figure 3.1 Schematic structures for n/p doped poly-Si passivation symmetric test samples.

To qualify poly-Si passivation performance, both injection-level dependent minority carrier lifetime (τ) and implied open-circuit voltage (iV_{OC}) are measured with Photo-conductance Decay Lifetime Tester. As shown in figure 3.2, these two parameters are plotted with various deposition times ranging from 113 mins, 150 mins, 180 mins and 210 mins(corresponding to approximately 226 nm, 300 nm, 360 nm and 420 nm film) separately.

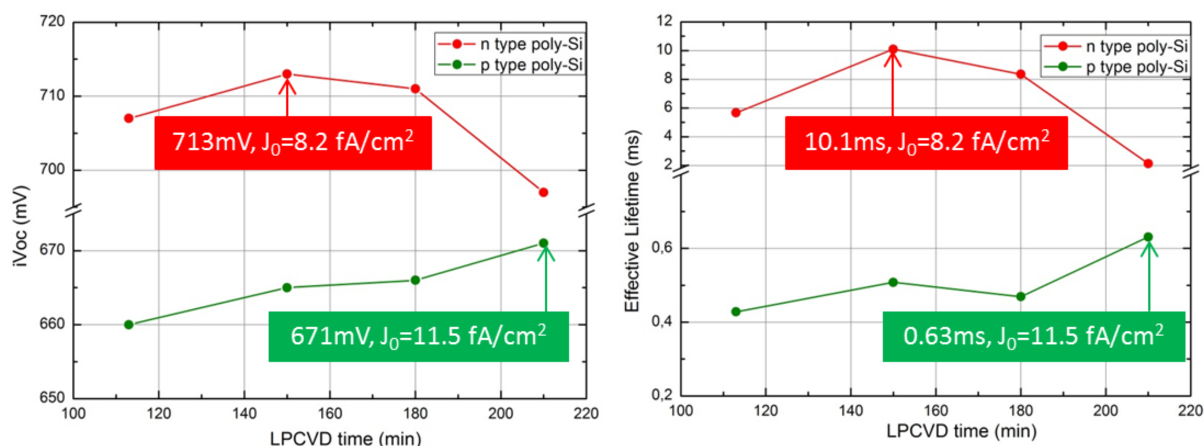


Figure 3.2 Implied Voc and effective lifetime performance for n type and p type poly-Si as a function of their LPCVD deposition time.

For n type poly-Si, both iVoc and lifetime increase when extending deposition time from 1 hr 53 min to 2.5 hr. Considering an approximate growing rate of 2nm/min, n type poly-Si with thickness of 300 nm achieves passivation of 10.1 ms lifetime and 713 mV implied Voc. Saturated current density is calculated to 8.2 fA/cm^2 by dividing overall J_0 value into half for symmetric structure. While passivation decreases with iV_{OC} dropping to 697 mV and lifetime dropping to 2.1 ms for sample with 3hr deposition. This can be explained by poly-Si doping profile at the interface. Suppose the same density and crystallinity fraction for all the poly-Si samples, which ensures the same quality for various thickness poly-Si layers. Good field-effect passivation occurs when P-dopants are well confined within poly-Si material region [21]. If poly-Si layer is too thin, dopants diffuse too deep into c-Si bulk thus there will be no or less band-bending at poly-Si/c-Si interface to provide carrier selectivity. Also this happens when poly-Si layer is too thick when deposition time is prolonged. The thermal budget (annealing 950 °C for 5 min) is not sufficient to drive in dopants to the interfaces and only a too shallow doping profile within poly-Si layer is achieved, which also leads to a low field-effect passivation. It's not

sufficient for minority carrier selectivity because holes still have chance to diffuse to the interfaces or through the tunneling layer into poly-Si (where there are much high D_{it}) and recombine with the majority electrons. Such large recombination will lead to a much lower effective lifetime, as indicated for 180min and 210min deposition samples.

Considering p type poly-Si performance with varying deposition time (or thickness), best passivation can be observed at 210 min, which is much longer than the optimized n type deposition 150min. Under this condition, 671 mV iV_{OC} and 0.63 ms effective lifetime is achieved with a minimal J_0 value of 11.5 fA/cm^2, which is 1.5 times larger than n type. Such an inferior passivation can be revealed by the difference of phosphorous and boron atom diffusion into poly-Si layer. Largely increased recombination velocity is pronounced at boron doped poly-Si and c-Si interface and in p type poly-Si itself [20]. Lighter boron atoms are easier to diffuse through tunnel oxide layer and may actively penetrate a thinner poly-Si layer (shorter deposition time) which leads to a higher defect density created by SiO_2/c-Si interface damaging. Also larger diffusivity leads to fewer boron atoms, which have already ionized segregated in the grain boundaries [54]. Both count for higher recombination and poor passivation.

3.1.2 Influence of Annealing Condition

As previously introduced architecture in figure 1.11, to fabricate a bifacial solar cell with poly-Si passivatng contacts which locates only underneath metal, we still need boron doping for p type c-Si formation in the area between the metal fingers. Normally even for conventional solar cell fabrication, boron diffusion is a most decisive step either to create back surface field when dealing with p type bulk or create an emitter for n type substrate. Higher diffusion temperature or longer processing time is often applied for boron diffusion [55] then the thermal budget used for preparing the above poly-Si passivating contacts. While the investigation for an optimized p type c-Si surface passivation regarding varying annealing condition with film sheet resistance will be introduced into details in chapter 3.2.2. To adjust for a balance between optimized poly-Si and optimized p c-Si surface after anneal, here it’s essential to minimize high temperature degradation on poly-Si passivation to the least. In this section, influence of high temperature annealing ranging from 900 °C to 1050 °C (which is the commonly used highest temperature available in EKL CR100) on n/p doped poly-Si material is analyzed into details.

Applying same symmetric structure as indicated in figure 3.1, after NAOS-tunneling oxide formation and LPCVD deposition time of 150 min, samples were implanted with the same Phosphorous or Boron implantation parameters as in section 3.1.1. A following high temperature annealing is carried out in oxygen atmosphere with a ramping rate of cooling or heating at 10 °C/min. After varied annealing temperature and time, passivation properties of different samples are plotted below in figure 3.3.

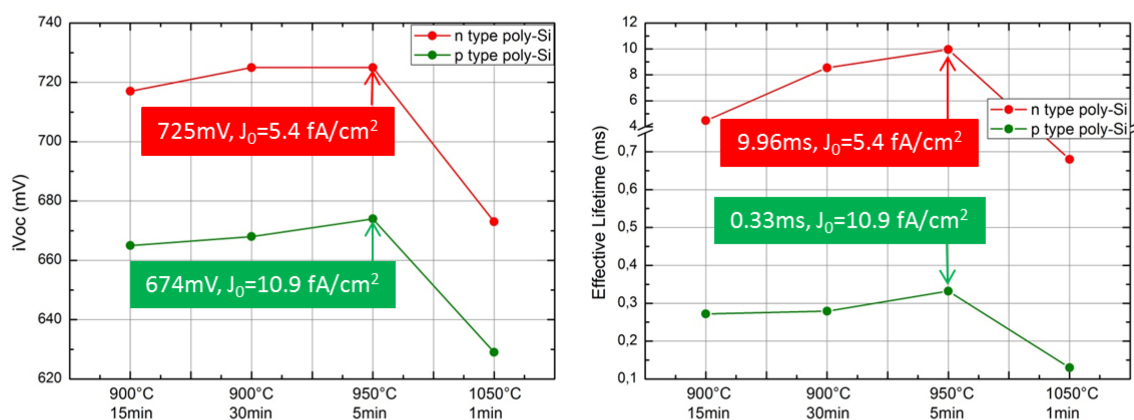


Figure 3.3 Implied V_{OC} and effective lifetime performance for n type and p type poly-Si regarding various annealing temperature and time. Lines are just used to guide sights.

It can be observed for n type poly-Si, higher τ_{eff} of 8.5 ms is achieved with 900 °C annealing when extending annealing time from 15min to 30min. Further better performance is also observed when increasing annealing temperature to 950 °C for only 5min, an optimized τ_{eff} of 9.96 ms is reached. Also implied V_{OC} keeps rising up from 718 mV to 725 mV with the change of annealing temperature from 900 °C to 950 °C. It corresponds to varied crystallization phase in Si layer [56]. At 900 °C temperature LPCVD deposited amorphous silicon become semi-crystalline while increasing temperature to 950 °C, a stronger crystallization will be achieved with more than 90% Raman crystallinity fraction [21] also dopants are driven sufficiently deep within poly-Si and to be confined in poly-Si with a shallow profile in c-Si. This is of great benefit because compared with amorphous, crystalized Si material has a superior optical and electrical property. However, rising temperature to 1050 °C with a duration time of 1min annealing, passivation worsens greatly. Effective lifetime decreased to 0.68 ms with implied V_{OC} dropping to 673 mV. This can be explained by the fact that higher temperature may not only enable crystallization of Si layer but also induce a localized

disruption in tunneling SiO_2 layer. Its stoichiometry changes and barrier quality weaken. As suggested by NREL [57], this tunneling SiO_2 degradation or even break-up contributes to hydrogen blistering and pinhole formation on oxide/c-Si interface with higher temperature annealing. Thus it's important that high temperature annealing would not exceed a certain point that maintaining tunneling oxide integrity.

Taking a look into passivation performance of p-type poly-Si with varied annealing temperature, similar trend also can be observed. When increasing temperature from 900 °C to 950 °C, effective lifetime of p type poly-Si improves slightly from 0.27 ms to 0.33 ms with an iV_{OC} increase by 10mV. However, continuing temperature rising to 1050 °C with annealing time of 1 min, passivation performance undermined sharply to 0.13 ms τ_{eff} and 629 mV implied V_{OC}. This also suffers from same high temperature induced damage to tunneling oxide quality and inferior performance of boron diffused poly-Si properties.

Therefore, taking into account both n and p type poly-Si passivation with varied annealing condition, 950 °C temperature and 5 minutes duration is determined as an optimal recipe. Under this condition, with 300 nm thickness poly-Si material, n type layer results in a minimized J_0 of 5.4 fA/cm^2 and p type with a J_0 value of 10.9 fA/cm^2. Compared with previously optimized passivation under same condition, the slightly improved performance (2.8 fA/cm^2 and 0.6 fA/cm^2 less J_0 for n and p type respectively) also indicated the unstable performance for LPCVD deposition or wet chemical ultrathin tunneling oxide quality.

3.2 Optimization of c-Si Surface Field Passivation

Conventional c-Si solar cell with the application of a passivated rear contact used to be limited by its front side contact recombination. With the employment of TOPCon technology on top and rear, both sides are equipped with wider bandgap poly-Si above tunneling oxide to create both hole-selective and electron-selective contacts. Such a structure has been proved to achieve a good passivation quality on solar cell device of 709 mV V_{OC} and FF above 81% [20]. While the limitation of top/rear poly-Si(O_x) approach is still the parasitic absorption of poly-Si in blue response, making its application potentially problematic with severely degraded J_{SC} [58]. Recent effort is made to provide good passivation performance with much thinner poly-Si layer but research

has been made reporting that the upper bound for parasitic absorption losses in 10-40 nm thick poly-Si layer counts for 0.5 mA/cm^2 per 10 nm poly-Si film[20].

While to solve this problem, as introduced above in Chapter 1, the concept of PeRFeCT cell combines the advantage of highly transparent lightly doped homojunction as front surface field and highly doped low metal contact recombination rate TOPCon layer only under front metal grid [24]. Resembling from this approach, the advanced bifacial solar cell design in this project, also employs with n type and p type lightly doped c-Si surface to ensure reduced light absorption losses. As a trade-off, the low quality passivation of such homojunction surface field and emitter becomes a bottleneck, owing to its greatly larger coverage than metal grid area. Therefore, to fabricate such an advanced bifacial solar cell with poly-Si passivating contacts, optimized surface passivation for both n type c-Si and p type c-Si are brought into emphasis. In this section, investigation for improved n/p c-Si surface passivation is carried out separately aiming for a lower contribution of total J_0 in final solar cell device.

3.2.1 Optimization of n type c-Si Surface Passivation

In this section, the objective is to improve passivation of lightly doped n type c-Si surface. Considering the mature application for intrinsic hydrogenated amorphous silicon passivation on SHJ solar cell, which enables the highest V_{OC} of 750 mV and 26.7% efficiency by Keneka [17], a-Si:H is implemented above lightly phosphorous-doped c-Si for surface passivation.

The mechanism of a-Si:H passivation on c-Si is that this film can effectively passivate the dangling bonds on c-Si interface by forming Si-Si bonds. While some dangling bonds are not able to be bonded with Si, then it is the atomic hydrogen in a-Si:H bulk that play a role of terminating dangling bonds. Thus sufficient atomic hydrogen is critical for decreasing a-Si:H/c-Si interface defect density and improving surface passivation [44]. Regarding the performance for phosphorus doped c-Si with intrinsic a-Si: H passivating layer, implantation dose, a-Si:H deposition temperature and thickness all correlate and contribute. With a too low deposition temperature (below 200 °C), hydrogen mobility is lowered hence cannot provide a sufficient passivation to dangling bonds on c-Si surface. While if a-Si: H is deposited at a temperature exceeding 300 °C, hydrogen atom is much fastened and could accumulate in defects, which in return undermine the passivation.

Owing to the atomic structure and energy states of a-Si:H, holes and electron mobility in this film is one hundred times lower than that of c-Si [44]. Also as a wide bandgap material (1.6 eV to 1.8 eV depending on hydrogen amount in amorphous network), amorphous silicon show an extremely high absorption coefficient in the wavelength range from 390 nm to 700 nm. This draws its disadvantage of great parasitic absorption if applied at front side surface. The desired P implantation dose and a-Si:H deposition temperature is decided based on previous research [22] within PVMD group, which also functions as a reference for optimal deposition time.

In this project, influence of a-Si thickness is investigated with the assist of PECVD, which is a typical equipment to form uniform and high-quality a-Si film. A symmetric structure is fabricated as indicated below in figure 3.4.

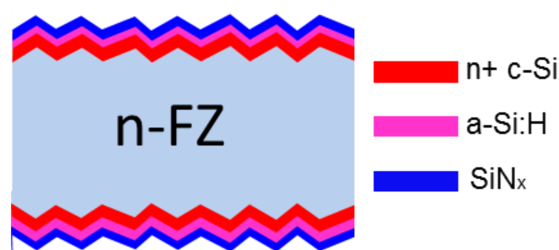


Figure 3.4 Schematic structure for a-Si:H passivated n type c-Si surface test samples.

To achieve a textured surface, double side polished n bulk FZ wafers are immersed into TMAH solution for 'random pyramid' formation. Then 10 keV energy, 1×10^{14} ions/cm^2 dose of phosphorous atoms are implanted on both sides of wafer with a followed annealing step at 950 °C for 5 mins to activate and drive in dopants into c-Si bulk. Reason for this choice is based on [21], which indicate a low J_0 of 6.5fA/cm^2 for 1×10^{14} ions/cm^2 phosphorous dose on n+ FSF with 5nm a-Si passivation layer, but when increasing doping level to 5×10^{14} ions/cm^2, recombination increase to a J_0 of 19fA/cm^2. So a lower implantation dose is chosen for n+ c-Si surface formation to ensure better passivation, in other words higher V_{OC} for solar cell.

To remove thermally formed oxide and also remove native oxide, BHF after annealing and HF dip before a-Si deposition is essential. Then with such an n-doped surface field, a-Si is deposited by PECVD in Kavli Nanolab at 250 °C with different deposition time. The gas ratio during deposition is 25 sccm for SiH_4 and 475 sccm for Argon. To finalize, a capping layer of SiN_x is also grown with a thickness of 75 nm at 400 °C. The passivation performance of varied a-Si thickness samples are measured with Sinton Lifetime Tester and results are plotted below (figure 3.5) in terms of minority carrier density versus lifetime.

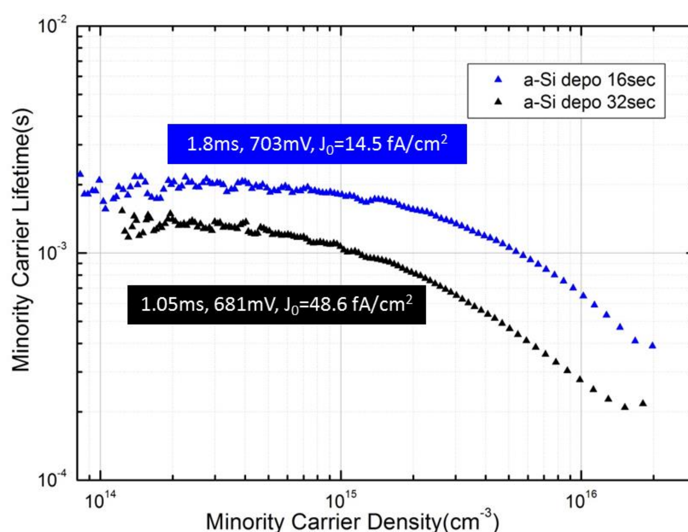


Figure 3.5 Minority carrier lifetime plots of 16sec and 32sec deposited a-Si by Kavli PECVD capped with 75nm SiN_X ARC.

By SE measurement of same processed flat samples, 16sec deposition results in a thickness of 24nm a-Si and 48nm for 32sec sample. This means approximately a deposition rate of 1.5 nm/sec on flat surface thus 0.87 nm/sec on textured surface can be calculated. Obviously as shown in figure 3.5, a much higher lifetime of 13.87 nm (16sec deposited) a-Si is achieved with varying minority carrier density from low injection level to high injection. It provides an optimized lifetime of 1.8 ms and a optimal J_0 value of 14.5 fA/cm^2, which can be applied in solar cell fabrication.

It's worth mentioning that two half wafer samples are from the same original wafer processing together only with changed deposition time. In spite of the thickness influence, blistering on 32sec-deposited samples might also lead to the inferior

passivation performance. Blistering is caused by hydrogen diffusing from deposited film while forming gas bubbles on wafer interface when a barrier exists, preventing its diffusion [59]. Normally to avoid such problem, a careful and throughout wet-chemical cleaning is critical for keeping wafer surface cleanliness.

3.2.2 Optimization of p-type c-Si Surface Passivation

For $2\Omega \cdot cm$ p type c-Si, successful implementation of Aluminum oxide (Al_2O_3) has been revealed with an effective surface recombination velocity close to 10cm/s[45]. Different from the widely industrial hydrogenated silicon nitride, which provides field-effect passivation by high positive charge density, Al_2O_3 with negative charge density is beneficial for p doped c-Si because minority carriers (electron) are effectively repelled from c-Si surface. Another benefit of Al_2O_3 is that it acts as an effective hydrogenation reservoir. During the post annealing or firing treatment, this film can provide hydrogen to terminate dangling bonds on silicon interface and passivate surface defects. As introduced previously in Chapter 2, by approach of self-limiting process in ALD, an accurate thickness control down to a few nanometers can be achieved. Previous research also revealed that Al_2O_3 is compatible for a Al_2O_3 a-SiN_x:H and an improved thermal stability is observed compared to single layer performance[14]. All this advantages enable Al_2O_3 as a suitable candidate for p type c-Si passivation.

In this section, the performance of Al_2O_3 (in the form of Al_2O_3/a-SiN_x:H stack) is studied. Optimizations were carried out mainly in two aspects: (1) the influence of post-annealing (FGA atmosphere) with p bulk wafer and (2) various Al_2O_3 film thicknesses influence on the passivation of p+ emitter on n type wafer. For the latter, an average sheet resistivity of $60\Omega/sq$ is achieved by boron deposition and diffusion in furnace.

Furthermore, optimal boron implantation parameters and annealing conditions are also investigated in section 3.2.2.3 aiming for a R_{SH} value around $120\Omega/sq$. Because over the years, tremendous amount of research has revealed that a suitable passivation scheme depends on doping type, Si resistivity and various aspects i.e. thermal/ UV/ long-time stability and other correlated parameters [60]. A low doping concentration underneath the passivation layer is necessary to minimize recombination but high doping concentration under metal contact is necessary to reach minimized series resistance [33].

By changing the implantation dose and annealing condition, in this section, efforts were made aiming for an optimized boron doping profile, which can provide both good passivation but also good conductivity in solar cell performance, in order to enable a good trade-off between the final solar cell V_{OC} and FF.

3.2.2.1 Influence of Forming Gas Annealing

Forming gas is a mixture of hydrogen and nitrogen, which often provides the atmosphere for annealing. The well-known effect of forming gas annealing is to provide hydrogen passivation to electrically active dangling bonds and reduce interface trapping density.

To be specific, the high adsorption of hydrogen content in forming gas provides hydrogen atoms to silicon surface, which closes the voids formed by hydrogen abstraction [61]. Its application has already been proved to be great enhancement for surface electron mobility in NMOSFETs with polysilicon gate electrode [62]. Meanwhile considering low temperature (below 600 °C) surface morphology won't be changed after annealing. Its application on p type silicon surface for both no-diffused or boron diffuses cases also proved to show an excellent level of surface passivation and enhanced thermal stability even through 825 °C firing step.

In this case, the influence of forming gas annealing is studied by carrying out experiments at 400 °C by Tempress furnace with a gas ratio of 10% H_2 and 90% N_2 for 30 min. Symmetric structure of samples for the passivation test is scratched in figure 3.6.

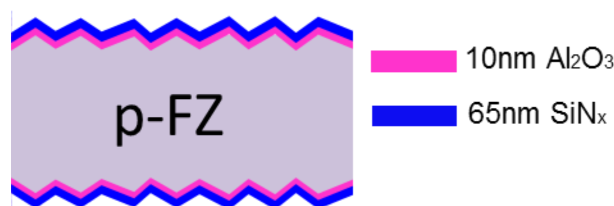


Figure 3.6 Schematic structure for passivation test samples with Al_2O_3/SiN_X as passivating layers.

After standard cleaning to remove organic and inorganic contamination, double side textured p type samples are ready for ALD aluminum oxide deposition at 250 °C with a thickness of 10 nm. Thermal process is chosen for its superior performance and it's not necessary to remove native oxide on top of surface because this thermal recipe with H_2O

precursor also form thermally grown SiO_2 during process. Then samples are divided into groups, for later direct processing of FGA or another capping layer of 65 nm SiN_x, which is necessary in our bifacial solar cell structure to function as a 75 nm anti-reflection coating stack. The passivation performances are shown in figure 3.7.

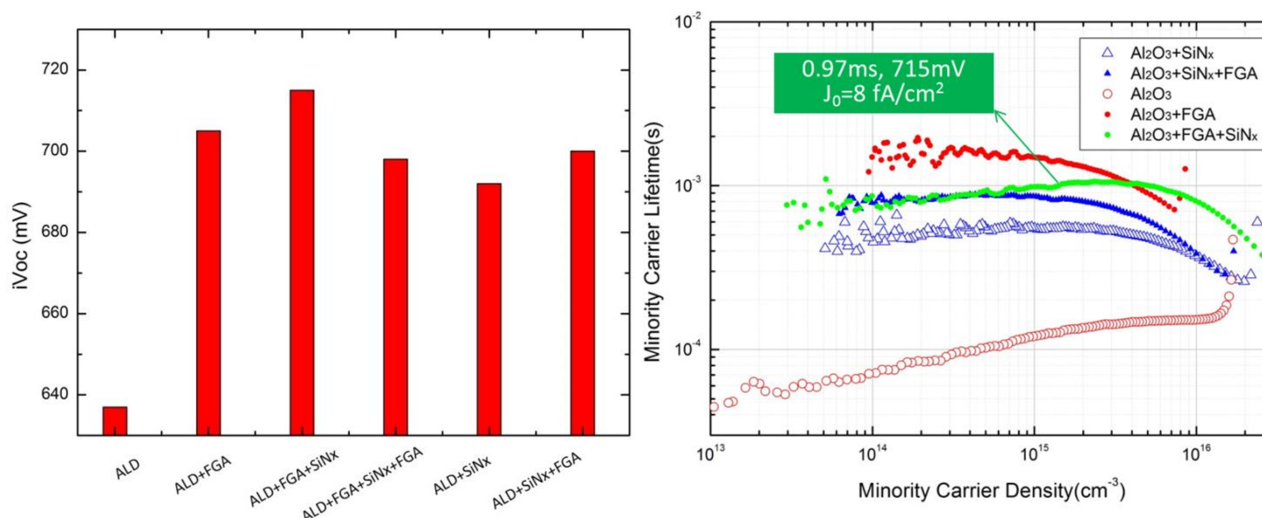


Figure 3.7 Implied Voc (left) and minority carrier lifetime (right) plots with various processed Al_2O_3/ SiN_x stack after or before Forming Gas Annealing.

After single process of ALD deposited Al_2O_3 on textured p type surface only 640mV implied V_{OC} achieved, which illustrates the essentiality of further annealing or nitride deposition step to enhance passivation. Following FGA or SiN_x deposition contribute to an iV_{OC} increase of 68 mV and 55 mV respectively. This is because SiN_X deposition at 400 °C is already an annealing that enhance hydrogen bonding to Si at the interface, which contributes to the passivation. The highest iV_{OC} performance can be observed by thermal ALD deposition and FGA followed by PECVD deposited SiN_x counting for 715 mV. Similar results can be found regarding the minority carrier lifetime plots versus Minority carrier density in figure 3.7 (right). Comparing lifetime performance for single Al_2O_3 (red opening) with post-annealed Al_2O_3 sample (red closed dots) and Al_2O_3/SiN_x:H stack (blue opening) with same stack after FGA (blue closed triangle), significant lifetime improvement can be observed. While for best iV_{OC} performed sample, Al_2O_3/FGA/SiN_x stack offers a slightly lowered lifetime than single Al_2O_3. This is mainly due to by attaching SiN_x as ARC, injection level also increased. The higher τ_{eff} at high injection level indicates a better passivation for Al_2O_3/FGA/SiN_x stack with only 8

fA/cm^2 $J_{0.}$

Forming Gas Annealing is proved to activate and improve p type silicon wafer passivation after Al_2O_3 deposition. Hence, with J_0 value of 8 fA/cm^2, this optimized process series of Al_2O_3/FGA/SiN_x stack can be applied for bifacial solar cell textured p type c-Si surface.

3.2.2.2 Influence of Al_2O_3 Thickness

In this section, the influence of thermal Atomic Layer Deposited Al_2O_3 film thickness on the passivation of Al_2O_3/SiN_x stack to p type c-Si passivation is studied.

Previously correlation between thickness and as-deposited (before annealing or capping layer) surface passivation was revealed, for example, by TU/e research group[14]. They found that regarding thermal process, a constant passivation level can be maintained with above 10 nm Al_2O_3 film. A significant deterioration below 5 nm is mainly due to the degradation of chemical passivation when decreasing to ultrathin layers while field-effect passivation shows independence of thickness change. Because the induced negative charge mainly stays on Al_2O_3/c-Si interface and keeps as a constant value even Al_2O_3 dropping to 2 nm film thick. However, based on large scale of data set, some statistic also showed field-effect passivation undermined inactively after certain compensation point.

In this section for our experiment, double side textured n bulk wafers are prepared. p+ diffusion on both sides is created by boron deposition furnace in EKL CR10000 with a duration of 30 minutes which is followed by 950 °C annealing in oxidation atmosphere for 5 minutes to drive in and activate boron diffusion. BHF etch is carried out for thermal oxide removal. Afterwards, **one wafer was cut into four pieces**, each of them were then passivated with Al_2O_3 film by thermal ALD at 250 °C. Al_2O_3 film thickness was varied ranging from 6 nm to 30. Then samples were capped with 65 nm SiN_x deposited together by PECVD at 400 °C. Figure 3.8 show the symmetric structure for this optimization test and passivation quality is evaluated by photo-conductance decay lifetime tester, shown in figure 3.9.

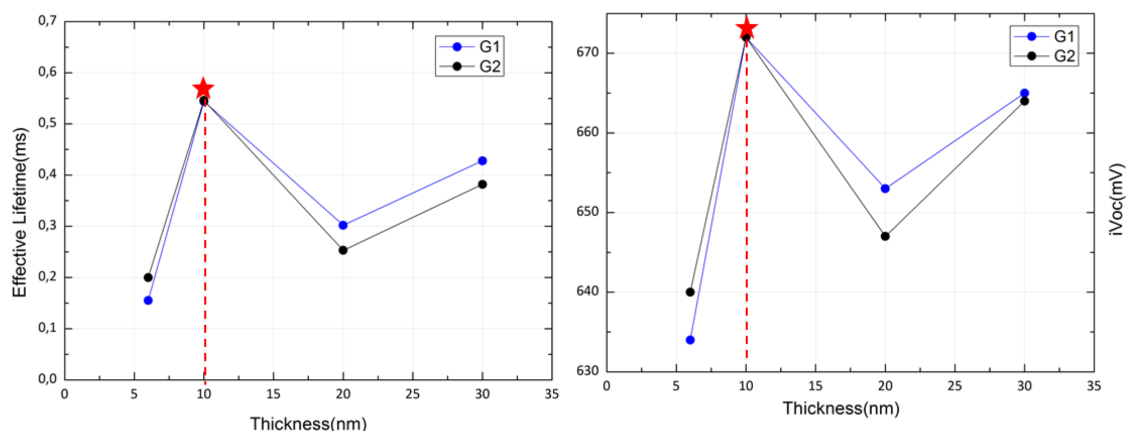


Figure 3.8 Schematic structure of the symmetrical passivation test samples for p+ c-Si surface prepared on textured n bulk, Al_2O_3/SiN_X films are used as passivation layers.

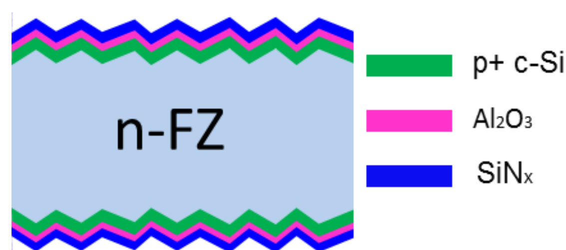


Figure 3.9 Effective lifetime and iV_{OC} plots of two groups of samples with various Al_2O_3 film thickness with average sheet resistivity of $R_{sh_{G1}} = 69 \pm 6\Omega/\text{sq}$, $R_{sh_{G2}} = 74 \pm 9\Omega/\text{sq}$ separately.

Two groups of samples revealed similar trends for the passivation changes with thickness. The highest value is achieved with 10nm Al_2O_3 film with 672mV implied V_{OC} and τ_{eff} around 0.55 ms. By fitting lifetime curve versus MCD, a J_0 value of 46 fA/cm^2 can be calculated, which is quite high for solar cell application.

Furthermore, it can be observed from figure 3.9 that the performance of 6nm passivated sample shows degradable passivation, which is in line with previous research [14]. They reported a deteriorate passivation with thermal ALD deposited Al_2O_3 film thickness below 10nm on 3.5 Ω•cm n-type wafer followed by 400°C annealing in N_2 atmosphere for ten minutes. This is mainly due to significantly decreased chemical passivation of the ultrathin Al_2O_3 layers. However, weakened performance was also founded at 20 nm thickness level. Figure 3.9 showed an implied V_{OC} drop of 20 mV with only 0.25 ms and 0.3 ms respectively for samples in two groups. Theoretically with constant negative fixed

charge, as-deposited Al_2O_3 passivation performance normally reaches a saturated point at certain thickness and then maintains compatible level of τ_{eff} [63]. Speculations can be established regarding our experiments that this degradation is resulted from variation in samples' sheet resistivity. By boron deposition in furnace, it's difficult to control the thickness uniformity because B_2H_6 gas flow enters and touches wafer by top half. And B_2H_6 flow may already exhausted too much when reaching the bottom of processed wafers. Thus the bottom of the wafer may not obtain sufficient access to B deposit with the same thickness as the top, leading to a larger R_{SH}. As already known, it is more difficult to passivate heavily doped p+ c-Si, therefore the passivation of the top part of wafer may undermine passivation. This is verified by the variation of R_{SH} on different samples. However, still a better performance was noticed for 20 nm/30 nm Al_2O_3 film than 6nm.

3.2.2.3 Influence of Boron Implantation Parameters

The above discussed p+ c-Si prepared with boron layer deposition and diffusion is obtained on both sides of wafer without any surface selectivity. A masking layer and etching steps are necessary to pattern such p+ c-Si surface for our solar cell structure.

In this section, the p+ c-Si is prepared by boron implantation approach, which can be locally obtained by using lithography masking. The investigation was then made mainly aiming for an optimized sheet resistivity for p+ c-Si surface which can offer sufficient lateral conductivity to support the carrier collection for maintaining sufficient high solar cell FF. And on the other hand, the doping should be kept low enough for a high enough passivation, which enables high solar cell V_{OC}.

1) Introduction to boron diffusion

For industrialized p+ emitter formation, boron diffused region is normally created by first depositing precursors (i.e. BBr_3) on wafer surface and then high temperature annealing to step up diffusion, which can be done in in-line(belt) furnace or tube furnace [55]. A a sheet resistance of $65\Omega/\text{sq}$ can be obtained [55]. While during this process, a boron rich layer (BRL) can be formed, which is too detrimental for achieving a high passivation for solar cell fabrication.

BRL is a surface layer with high concentration of boron formed during diffuse process.

Normally after boron deposition, a drive-in process is essential for temperature activation and such a reaction below happens on c-Si surface[55]:

$$\mathrm{Si} + 6\mathrm{B} \rightarrow SiB_6 \tag{3-1}$$

The minority carrier recombination is relatively high in this supersaturated layer because of inactive boron, segregated metal impurity and structural defects [64]. Thus it's necessary to remove BRL to ensure good quality of surface passivation. While even with acid like HF, this BRL is difficult to remove. So normally after deposition, an in-situ oxidation is performed, to exhaust the BRL and form boron silicide glass (BSG, a SiO_2 layer) which can be removed by HF or BHF. We can achieve this in our annealing process with oxygen atmosphere included.

The mechanism behind this operation is because of the higher solubility of boron in silicon oxide than in silicon, which would assist the diffusion from primary silicon surface to newly formed oxide surface. Consequently with less boron concentration, minority carrier concentration also reduced. Wet chemical etching can easily remove this BSG. Thus in EKL CR100, after BHF etching, a hydrophobic surface is obtained with very low surface states density [55].

2) Approach by Boron Ion Implantation

Instead of boron deposition and diffusion by open-tube furnace, to enable a uniform R_{SH} and ensure homogeneity on wafer surface, we also tested the approach of ion implantation for forming p+ surface region. As introduced in section 2.2, ion implantation is only one-side process so no need to etch back or protect the n+ side for our bifacial cells. Also the desired implantation dose and energy can achieved a well-controlled boron doping level.

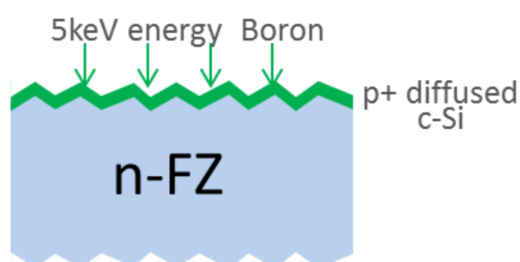


Figure 3.10 Schematic structure for Rsh optimization of p+ c-Si.

Based on simulation results, a R_{SH} value around $120\,\Omega/\mathrm{sq}$ enables both good

passivation and conductivity which enables a fill factor reaching 80% with around 1 mm metal finger gap. To achieve such R_{SH} value, structure in figure 3.10 on double side textured n type wafer is implanted with varied boron dose and annealing temperature and time. It's worth mentioning that annealing is processed in O_2/N_2 atmosphere and BHF immersion is followed to remove the defective BSG.

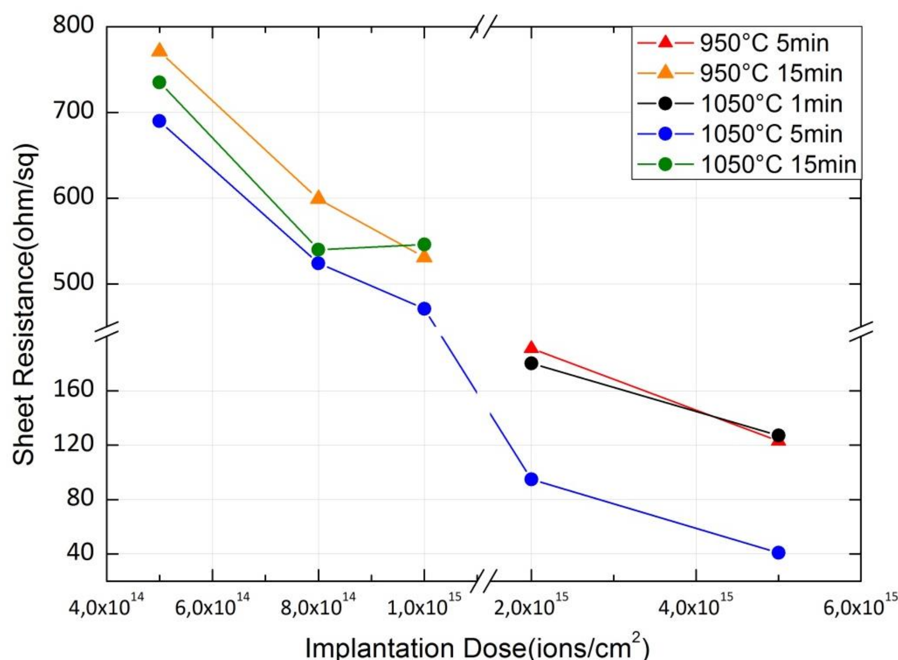


Figure 3.11 Sheet resistance plot versus boron implantation dose ranging from 5E14 to 5E15 ions/cm^2 with the annealing temperature under 950°C and 1050°C.

By four-point probe measurement, R_{SH} values for different samples can be revealed and are plotted in figure 3.11 with an increasing implantation dose. A general trend can be observed that with higher implantation dose, sheet resistance of doped materials decrease. First trial of 5E14 magnitude dose with 950 °C annealing for 15 mins provides sheet resistance around 500 to 800 Ω/sq. For boron diffusion, a higher temperature is required[55]. Hence annealing temperature rises up to 1050 °C but still no significant improvement. Further by increasing implantation dose to 1E15 magnitude, R_{SH} can be effectively dropped to within 500 Ω/sq region. Adjusting boron dose to 2E15 and 5E15, we can easily obtain a R_{SH} of 190 Ω/sq and 123 Ω/sq respectively when annealing at 1050 °C for 1 min. However to adjust this annealing step into our bifacial solar cell fabrication flowchart without degrading poly-Si passivation, 950°C annealing is tested. Results showing that a boron doped p+ c-Si with 123 Ω/sq can be created by

boron implantation with 5 keV energy and 5E15 ions/cm^2 dose, followed by 5 minutes annealing at 950 °C. This condition perfectly matches the optimized annealing condition for n/p type poly-Si thus will be further applied in solar cell flowchart.

4

Solar Cell Fabrication and Results

In this chapter, based on previous process optimization, flowchart for fabrication of bifacial solar cell with poly-Si passivating contacts and corresponding PeRFeCT cells with four different cell architectures, different bulk or junction combinations are established. Adjusting annealing condition for both poly-Si and boron implanted c-Si surface, this flowchart is available for flexible structures to be processed in same batch. The objective for this chapter is to first introduce this flowchart with schematic illustrations and process descriptions in section 4.1. Then optimized n type rear junction PeRFeCT cell parameters are compared with previous reference device in section 4.2, followed by a brief comparison between n type rear junction and front junction PeRFeCT solar cell performance. Section 4.3 presents the results of four test PeRFeCT cells, discussion on recombination analysis and the importance of FSF passivation. Finally in section 4.4, performance of n/p bulk bifacial solar cell will be discussed into details.

4.1 Solar Cell Flowchart

As illustrated below in figure 4.1, complete fabrication process for both bifacial solar cell and PeRFeCT solar cell (here n bulk rear junction solar cell is listed as an example) are proved to be implementable and will be described step by step:

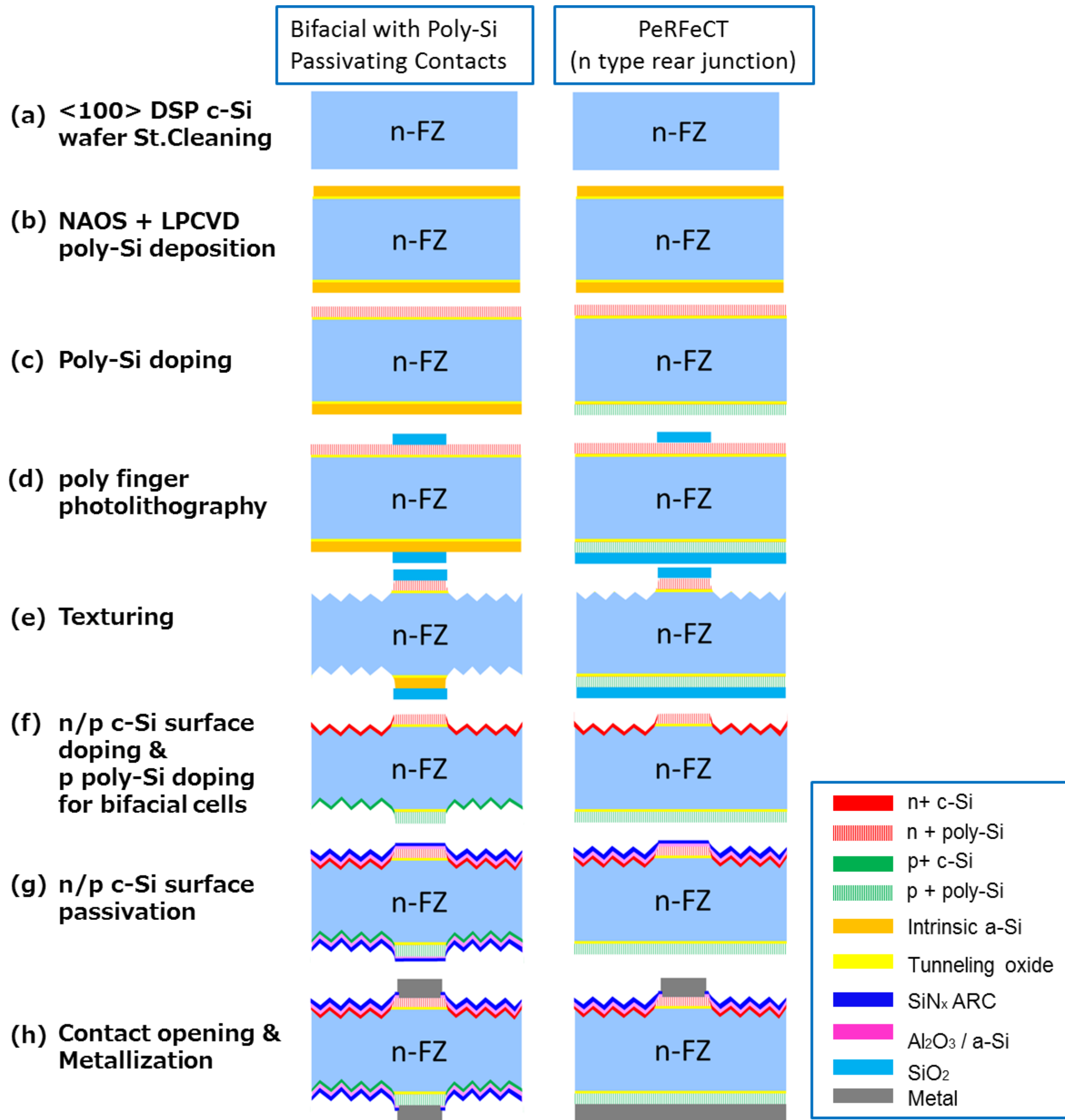


Figure 4.1 Schematic illustration of complete fabrication steps for both bifacial and PeRFeCT solar cell structures.

1) Wafer Preparation

Topsil or Siegert manufactured n bulk double side polished FZ c-Si wafer with <100> orientation is applied for solar cell fabrication. The resistivity ranges for $3 \pm 2\Omega \cdot \mathrm{cm}$ with $280 \pm 20\mu\mathrm{m}$ thickness. First to begin with processing in EKL CR100, a wet-chemical cleaning is essential. Nitric acid oxidation cycle (NAOC) is the standard cleaning process inside cleanroom. To be specific, during NAOC, brand-new polished wafers are first immersed in 99% concentrated nitric acid HNO_3 at room temperature for

10 minutes to remove organic contaminations. Then rinse in the next bath DI water with standard program until resistivity reaches 5MΩ or duration of 5. After this, wafers are cleaned in 69.5% concentrated nitric acid at 110°C for 10 minutes to remove metal contaminations, also followed by a DI water rinse. Next step after cleaning is to remove native oxide and acid induced silicon oxide on c-Si surface by Marangoni. That is to rinse wafer in 0.55% HF for 5 minutes then rinse in DI water for approximately 5 minutes to clean up remaining acid and dry up with IPA.

2) LPCVD poly-Si Deposition

With oxide removal, wafers are ready for high-quality tunneling oxide forming. Because if there's pinhole inside tunneling oxide, it gives direct touching for poly-Si and c-Si, which will lose chemical passivation for this structure and dramatically increase recombination. Immersed in 69.5% room temperature HNO_3 for 60 minutes, wafers are grown with a 1.5nm tunneling oxide. This process is called nitric acid oxidation of silicon (NAOS). As indicated in step (b), a stable SiO_2 layer provides perfect chemical passivation and also good lattice match with c-Si. Regarding the immersion time, previous investigation [22]in our group suggests NAOS is a self-limiting process. Immersion time may change the stoichiometry of SiO_2 also the density, which influence a lot for dopants diffusion into poly-Si. Optimal passivation occurs with one hour (a deviation of 5 minutes) immersion and TLM measurement also proved no additional increase in contact resistance for this NAOS step.

Following this is the deposition of intrinsic amorphous silicon on both sides of polished wafer by low pressure chemical vapor deposition (LPCVD). E3 furnace from Tempress is used with 'Lpolybin' desired recipe. Because intrinsic a-Si is deposited together on both sides of wafers, which means same deposition time and same thickness is determined for both sides of poly-Si. Therefore as discussed in section 3.1.1, the deposition duration of 150 min is chosen for an optimized n type poly-Si passivation and a comparable p type performance.

3) Poly-Si Doping

Implantation is applied to form both phosphorous and boron doped poly-Si. Here marking the correct side is extremely important both for implantation operator and solar

cell fabrication people. 5keV energy with 5×10^{15} ions/cm^2 dose is implemented for boron and 20keV energy, 6×10^{15} ions/cm^2 dose for phosphorous (step b).

While only n+ side will be implanted for bifacial solar cell because sharing the same energy and dose for p type poly-Si and p type c-Si, this step will be carried out afterwards together with p c-Si formation. Similarly, to drive in and activate the dopants, the 950°C annealing for 5 minutes (as optimized in section 3.1.2) will also postpone and process together with n/p c-Si surface annealing. A standard cleaning step is necessary for wafers coming out of implantation chamber.

4) Alignment Marker Formation

For mask alignment, before any lithography, alignment markers should be formed. First SiO_2 is deposited at 400°C by Novellus Concept 1, PECVD equipment in CR100. Depending on individual function of this sacrificing layer on both sides, different deposition thickness for front side and rear side are determined. Then by front side photolithography and PR removal, alignment markers are formed on front side. Back-alignment is applied to achieve same marker pattern on rear side. Then poly-etch (69.5% HNO_3/ 40%HF) to etch into silicon is for preventing texture eliminate markers on poly-Si.

5) Poly-finger Formation and Texturing

Another 500nm SiO_2 layer is deposited on front side functions as sacrificing layer for poly-finger photolithography. Negative photoresist is applied here so after exposure and development, only photoresist above poly-finger pattern remains. Other regions are only covered with oxide which also will be removed in BHF etching step.

For PeRFeCT cell, only n side poly-finger pattern is created and back side full area p type poly-Si is protected by SiO_2 (as shown in figure step e). Wafers are immersed in self-prepared TMAH solution for texture etching. As indicated in chapter 2.1.4, this step is to form random pyramid on illuminated side and improve light scattering for solar cell current collection. After about 8 minutes texturing is sufficient with DI water rinse and dry-up, a dark grey unreflective surface can be observed on wafer.

6) n+/p+ c-Si surface doping and passivating

After transported from MEMS lab, a standard cleaning step is carried out to remove contamination and then wafers are able to continue processing inside CR100. Sacrificing layer SiO_2 on both sides are removed by BHF (1:7). Then 10keV energy, 1×10^{14} ions/cm^2 dose is implanted for n + diffused c-Si surface and 5keV energy with 5×10^{15}ions/cm^2 dose for p+ poly-Si and p+ c-Si implantation. To activate dopants, a high temperature annealing at 950°C in N_2/O_2 atmosphere is carried out for 5 minutes. As illustrated in step (f), former doped amorphous silicon is poly-crystallized at the same time surface field also forms. Then we use BHF to remove thermally grown oxide on c-Si surface. Normally for a-Si deposition, it's essential to first passivate dangling bonds by Marangoni otherwise native oxide will decrease the passivation performance.

For n+ surface passivation, PECVD deposited hydrogenated amorphous silicon is applied. The thickness in our batch is optimized and following previous reference, 13.87nm a-Si:H is grown at 250°C. Then another 75nm SiN_x is deposited at 400°C to decrease front side reflection. This thickness is chosen based on destructive interference and characteristic of AM1.5.

For p+ surface (referring to bifacial cell), 10nm Al_2O_3 /65nm SiN_x is deposited to provide sufficient passivation and hydrogenation. Such a complete structure is illustrated in figure 4.1(g).

7) Contact opening

As introduced previously, to avoid metal touching c-Si, before metal deposition, a photolithography step is processed to confine limited region for contact opening. Three times of positive PR coating (3μm per time) is applied for textured side. After BHF etching to remove nitride and acetone stripping of photoresist, the architecture is finished with narrower opening width than poly-finger width. For bifacial ones, photolithography is carried out on both sides while for PeRFeCT cells, rear side is protected with either PECVD deposited SiN_x sacrificing layer or manual coated PR. A follow-up 5sec poly-etch is implemented to remove a-Si under opened contact region.

8) Metallization

Based on previous study within PVMD group [46], copper-electroplating can increase fill factor of a poly device with non-conductive ARC because of the decreasing series

resistance. However Aluminum still stands out for its easy processing, cheap price, acceptable conductivity, low work function and good adhesion onto silicon.

Hence for PeRFeCT cell test structure, front side 3000nm aluminum is used to collect charge carriers transporting through poly-Si passivating contacts. On rear side, Ag/Cr/Al stack with thickness of 400/30/2000nm respectively is used as back contact with a hard mask to define separate solar cell. Silver layer is thermally evaporated, which act as a back contact for its good conductivity. To increase adhesion of silver and aluminum, chromium is sandwiched between by E-beam evaporation. Silver is not good enough to survive from lift-off thus 2000nm Al is evaporated afterwards.

For bifacial cell, only Al is evaporated on both sides for its availability in metal lift-off.

9) Firing/Post-Annealing

Performance of c-Si solar cell with a-Si surface passivation improves after step annealing in N_2 atmosphere at 600°C. To effectively reduce ohmic-resistance, firing is identical for high efficiency solar cell because metal layers fire through the dielectric to define good contacts with semiconductor [65].

To finalize the device, external parameters i.e. V_{OC}, J_{SC}, FF and η can be measured by Wacom. Also EQE, transmittance and reflectance performance can be obtained. These results will be discussed in the following-up sections.

4.2 n-type Rear Junction PeRFeCT Cell

Previous optimization results for n/p poly-Si and n+ surface passivation were first implemented on PeRFeCT test cell. In this section, performance of two batches n type rear junction PeRFeCT solar cell is given in detailed description. Owing to an amorphous silicon (deposited as passivation layer in step-g in figure 4.1) barrier underlying metal contact, device is completed with 652mV V_{OC} and 17.5% efficiency. By removing this barrier by poly-etch, solar cell in Run 2 exhibits a performance of 687mV V_{OC} and 18.9% efficiency. Comparisons were made with reference PeRFeCT cell By the end of this section, n type rear junction and front junction PeRFeCT cell performance is studied, revealing an enhanced J_{SC} induced by less parasitic absorption on p+ side than n+ side.

Run 1

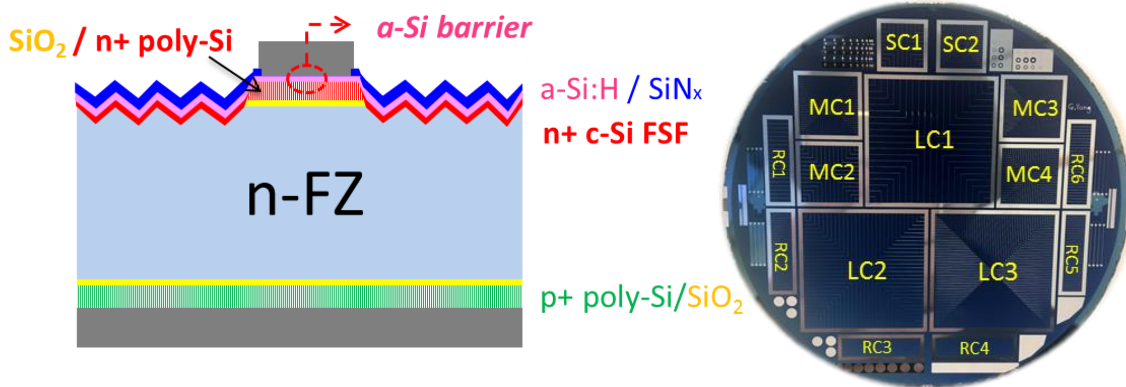


Figure 4.2 Schematic structure for n type rear junction PeRFeCT cell fabricated in Run 1 with a-Si barrier underneath metal contact (left) and real image token after solar cells fabrication (right).

As indicated in figure 4.2, n type rear junction PeRFeCT cell is fabricated with n+ poly-Si at front side as passivating contacts(J_0=5.4 fA/cm^2) and lightly doped n+ c-Si front surface field with a-Si:H/SiNx stack as passivating layers (J_0=14.5 fA/cm^2). Back side full area p type poly-Si (J_0=10.9 fA/cm^2) with tunneling oxide is implemented as contact passivation. While performance right after metallization is relatively low, which is 664mV V_{OC}, 60.8% FF and 14.99% η for 9cm^2 LC1 with 1.927% metal coverage and 633mV V_{OC}, 45.9% FF and 10.23% η for 2cm^2 MC2 with 2.755% metal coverage. A followed-up step annealing in N_2 environment at 600°C (as introduced in section 4.1 firing step) exhibit great enhancement for solar cell performance. FF and efficiency variation of #LC1 and #MC2 with annealing time are plotted below in figure 4.3. FF performance after 40sec treatment rises up to 66.5% for #LC1 and 66% for #MC2 with efficiency increase to 16.9% and 17.6% respectively.

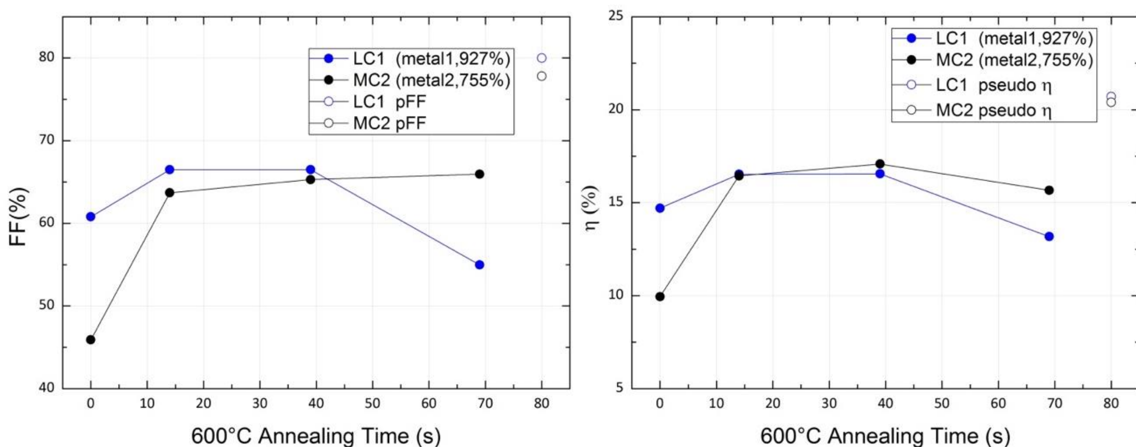


Figure 4.3 Fill factor and efficiency variation of Run 1 PeRFeCT cells with firing treatment at 600°C.

The accurate mechanism behind this increase is still unclear but some speculations can be made [21]:

Firstly, this high temperature provides hydrogen atoms inside a-Si:H passivating layers with energy to travel to certain right place. They passivate silicon dangling bonds on n+ c-Si surface and enhance the original passivation performance;

Secondly by 600°C annealing, Al reacts with a-Si:H on n+ side and Al:Si alloy is formed which means the low conductivity amorphous silicon layer is consumed as much as possible and the high conductive Al:Si is formed which induces lower contact resistance. With lower barrier between metal contact and FSF/ emitter, contact resistance decreases. But it's worth mentioning that V_{OC} improvement saturates or even deteriorates after long-time annealing which means passivation might destroy [66]. This is in line with our experiments that after another 30sec firing step, both fill factor and efficiency show a general trend of degradation.

Though enhancement was made by 600°C post-annealing treatment, such a-Si layer (deposited as passivation for n+ c-Si) barrier with 13.87 nm thickness cannot be consumed completely. This barrier under front metal grids show extremely low conductivity remains to be a poor contact contributing to the poor performance of solar cells. This layer has to be removed in next run.

Run 2

By poly-etch step after contact opening on front side, the a-Si barrier is removed in this run, which enabled a better performance than Run2. The schematic structure for Run 2 n type rear junction PeRFeCT cell is illustrated in figure 4.4 and overall performance listed below in table 4.1.

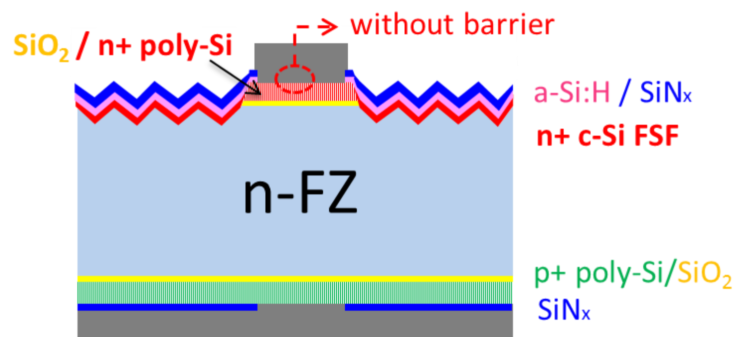


Figure 4.4 Schematic structure for Run 2 n type rear junction PeRFeCT cell.

Table 4.1 Overall performance of Run 2 n type rear junction PeRFeCT cell and reference solar cell [24].

	V_{OC} (mV)	$J_{SC\text{-}aperture}$ (mA/cm^2)	FF (%)	pFF(%)	η (%)
Reference	656	40.7	75.2	82.7	20.0
Run2_#LC3	687	40.4	68.2	83.5	18.9

Large-scale data set are collected from two wafers processed in same batch (each with 15 cells) and the best performance after 15sec firing treatment comes from 9cm^2 #LC3 with 6.021% metal coverage. Thanks to the low J_0 from enhanced FSF passivation, recombination is largely decreased and leads to 687mV V_{OC}, counting for 31mV increased compared with reference PeRFeCT performance [24]. This also benefits from the novel design of contact opening mask that an opening much narrower than poly-Si contact is created beforehand. So metal contact can be confine in this region at metal/poly-Si interface This design efficiently reduces tremendous contact recombination when metal directly touching c-Si surface, as happened during metal evaporation in reference PeRFeCT cell fabrication (SEM image in figure 4.5).

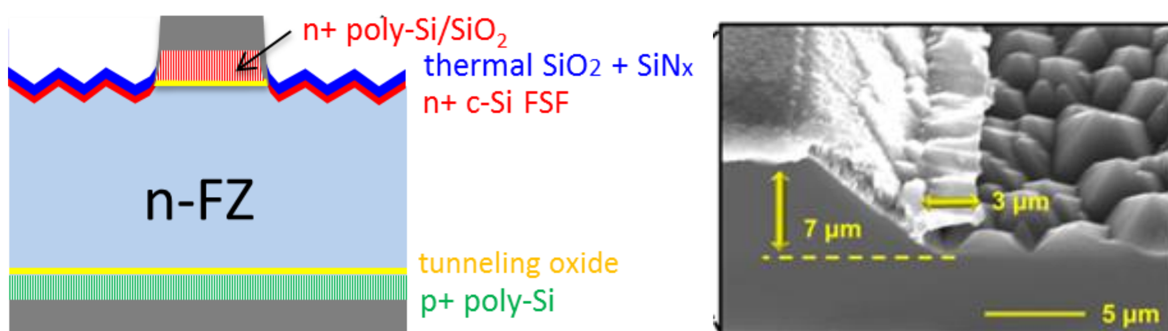


Figure 4.5 Schematic structure of reference n type rear junction PeRFeCT cell with thermal SiO_2/SiNx double ARC at front side (left) and SEM image illustrating metal contact touching c-Si (right) [24].

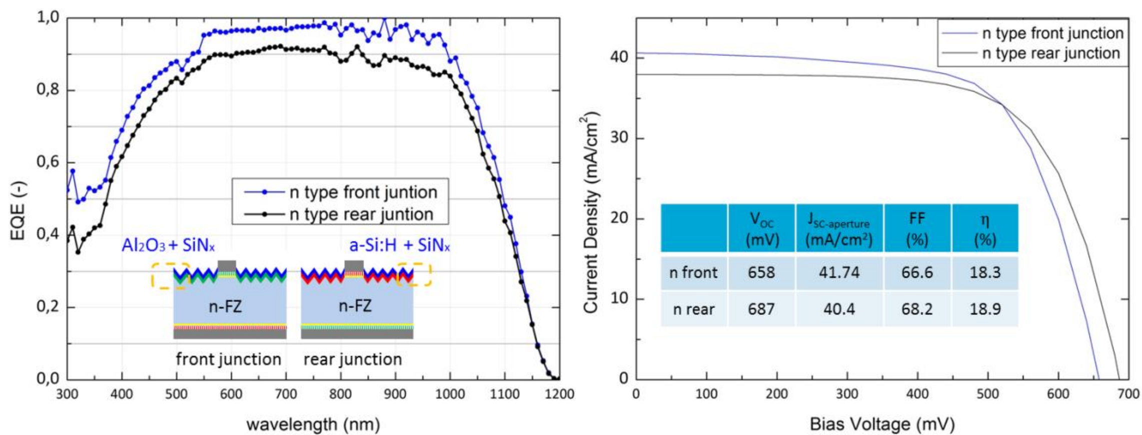
Considering the slightly lower aperture J_{SC}, which were both calculated with respectively metal coverage, 0.3 mA/cm^2 origins from the a-Si layer as n+ c-Si passivation on front side induces parasitic absorption compared with reference SiO_2/SiN_x stack. Taking a look at pFF, obtained through sunsV_{OC} measurement, 83.5% pFF is achieved in this optimized n bulk rear junction PeRFeCT cell, higher than reference structure which

illustrates a better carrier transport under the condition without series resistance. However, for actual solar cell performance, a lowered fill factor can be explained by local contact of SiN_x at rear side of PeRFeCT in this run (see figure 4.4). Such a structure was intended for etching back full area metal layer and turning this cell into n bulk Bifacial-PeRFeCT solar cell by metal etch back on p+ side. However, due to this structure, higher series resistance ($2.403\Omega \cdot cm^2$) is resulted by longer current flow path at rear poly-Si contact.

This n type rear junction PeRFeCT cell results the availability of our optimized n/p poly-Si and n+ c-Si surface passivation with an increase of 31mV ΔV_{OC} despite its inferior FF and efficiency, which is less significant for determined bifacial cell.

n type front junction PeRFeCT cell

To implement and investigate passivation performance of p+ c-Si surface, n bulk front junction PeRFeCT cell is also fabricated. As illustrated before in section 1.3, p type poly-Si with ultrathin tunneling oxide is deposited at front side, functioning as passivating contacts. Lightly doped p+ c-Si created by boron diffusion in tube furnace is used as FSF, which is passivated with 10nm Al_2O_3/65nm SiN_x ARC. At rear side, n type poly-Si with TOPCon structure is deposited full area to reduce rear side metal recombination. Such a structure provide excellent optical perfromance as illustrated in the EQE curves shown in figure 4.6.



	V_{OC} (mV)	$J_{SC\text{-aperture}}$ (mA/cm²)	FF (%)	η (%)
n front	658	41.74	66.6	18.3
n rear	687	40.4	68.2	18.9

Figure 4.6 EQE and J-V curves for n type rear junction and front junction PeRFeCT solar cells.

By comparising to n type rear junction perfromance, a better carrier collection is observed in front junction structured cell and this accounts for $J_{SC\text{-}aperture}$ of 41.74mA/cm^2. The noticeable difference for EQE in short wavelength is mainly contributes to less parasitic absorption of Al_2O_3/SiN_x other than a-Si/SiN_x stack in rear junction PeRFeCT for FSF passivation. Recombination loss contributes to the rest of EQE curve difference between front and rear junction structured cells.

V_{OC} performance for both front junction and rear junction solar cells can also be discussed as plotted in figure 4.6. Hints can be given that although a high J_{SC} is obtained, not optimal p+ c-Si for front junction cell results a weaken passivation. In all, it leads to lower solar cell efficiency than rear junction PeRFeCT cell. This result is also confirmed by effective tunneling mass simulation[24]. Both front junction and rear junction PeRFeCT configurations show current crowding between the edge of homojunction region and carrier-selective contact. However rear junction stands out with higher potential efficiency over 26% (front junction >24%) because of more favorable lower-tunneling-mass hole transport.

4.3 Performance Comparison for Four PeRFeCT Cell Architectures

In order to test and verify the influence of solar cell performance due to performance of n/p poly-Si passivating contacts and n/p homojunction passivation on both n bulk and p bulk c-Si wafer, four different PeRFeCT cell configurations are fabricated. Each performance will be investigated in this section. As illustrated in figure 4.7, it's clear to notice that n type rear junction and p type front junction share same recipe of 13.87nm a-Si/75nm SiN_x as FSF passivation while n type front junction and p type rear junction cells are passivated by 10nm Al_2O_3/65nm SiN_x stack for p+ c-Si homojunction.

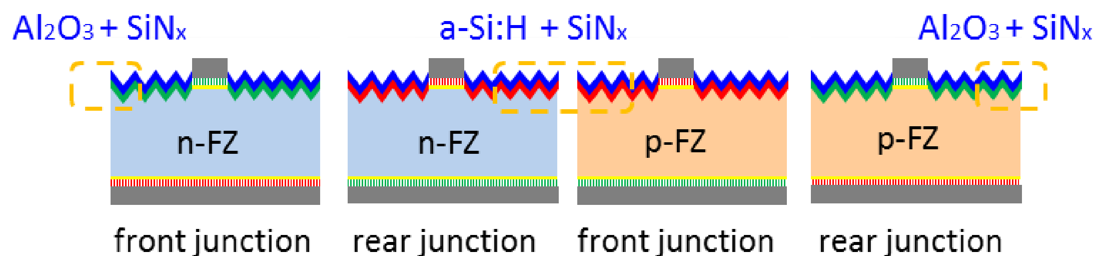


Figure 4.7 Schematic structures for n/p bulk front/rear junction PeRFeCT cells, which are test cell structures for the aiming bifacial solar cells.

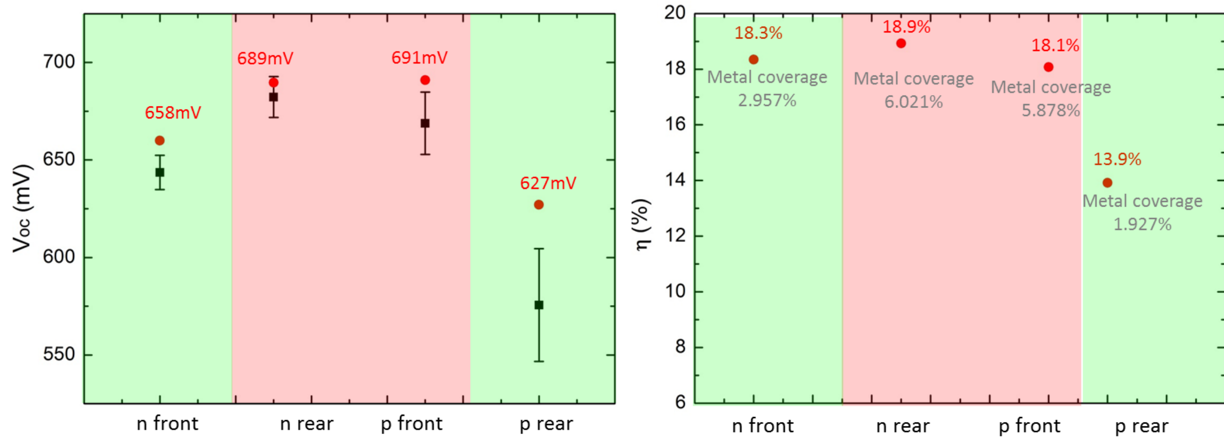


Figure 4.8 V_{OC} and η performances for n/p bulk front/rear junction PeRFeCT cells.

These cell structures are used as test cells for our bifacial solar cells. Therefore we are mainly focusing on the analysis of cell V_{OC}, cell efficiencies are also listed to make this discussion more clear. Figure 4.8 is a data collection based on overall 15 solar cells on each type of wafer. Average value and standard deviation for V_{OC} are calculated and marked with the highest performance in red. It can be revealed that both n bulk rear junction and p bulk front junction exhibit an open-circuit voltage around 690mV, which is superior to the highest V_{OC} point in n bulk front junction (658mV) and p bulk rear junction (627mV). This stresses the highly correlated solar cell performance with FSF passivation for PeRFeCT-like architecture.

Throw back the previously mentioned the definition formula for V_{OC} calculation:

$$V_{OC} = \frac{K_B T}{q}\left(\frac{J_{sc}}{J_0} + 1\right) \tag{4-1}$$

In spite of J_{SC} influence on solar cell V_{OC}, total J_0 is a critical parameter and if we look into the recombination in a solar cell:

$$J_{0,tot} = J_{0,bulk} + f \cdot J_{0,front\ contact} + (1 - f) \cdot J_{0,FSF} + J_{0,rear\ contact} \tag{4-2}$$

It mainly comes from recombination in bulk material, front contact, rear contact and FSF. Here the 'f' factor is poly-Si finger coverage ratio on front side. Poly-Si material area varies with metal/poly finger width, gap and finger numbers designs on mask. Typically for the poly mask applied in our project, 'f' factor ranges from 3% to 10%. If we take an

average value of 5%, 10fA/cm^2 J_0 in bulk, still recombination in FSF accounts for the most of solar cell total saturated current density. That means, FSF passivation is critical for performance of the final device and it confirms the necessity of previous optimization for n/p+ c-Si surface in section 3.2.

Regarding solar cell efficiency, best performance of each structure comes from different solar cell with varied metal coverage rate, which are 9cm^2 LC2, 9cm^2 LC3, 2cm^2 MC4 and 9cm^2 LC1. All efficiency values have already taken metal coverage into account. This distribution mainly contributes to the non-uniformity of passivation layers deposition and metal pattern design, which will not be looked into details in this project.

4.4 Bifacial Solar Cell with poly-Si Passivation Contacts

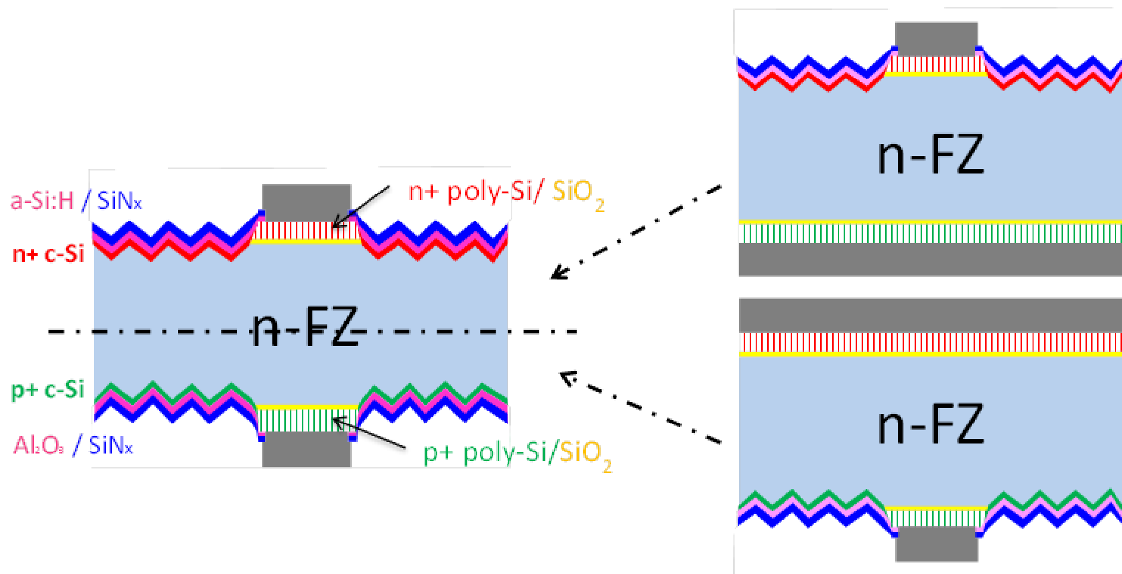


Figure 4.9 Schematic structure for n bulk bifacial solar cell with poly-Si passivation contacts (left) and its test structure on n type rear/front junction PeRFeCT cells (right).

In this section, performance of bifacial solar cell with poly-Si passivation contacts are studied with the assist of SEM for high resolution investigation of surface topology.

Based on previous optimization and trial fabrication and characterization of PeRFeCT configurations, an optimized n/p doped poly-Si passivation is obtained with 5.4fA/cm^2 and 10.9fA/cm^2 respectively. In terms of n type c-Si surface, 14.5 fA/cm^2 J_0 is observed with 13.87nm a-Si/75nm SiN_x stack as passivation layer. This poor-conductive a-Si under metal contact will be removed by poly-etch before metallization. Also new approach of

5keV boron implantation with 5E15 ions/cm^2 dose is chosen to obtain an optimal 120 Ω/sq sheet resistance after 950°C annealing in N_2/O_2 atmosphere for 5mins. By adjusting all these optimization into a bifacial solar cell flowchart, architecture as suggested in figure 4.9 is fabricated in EKL CR100. In the same batch, both n bulk and p bulk wafers are processed and the best performance for n bulk solar cell is listed as below in Table 4.2.

Table 4.2 Best performance of n bulk bifacial solar cell with poly-Si passivating contacts.

LC3 6.021%m	V_{OC} (mV)	$J_{SC\text{-}aperture}$ (mA/cm^2)	FF (%)	η(%)
n+ side	546	35.4	45.9	8.34
p+ side	585	40.2	55.1	12.96

For 9cm^2 LC3 with 6.021% metal coverage, on n side 546mV open-circuit voltage is obtained with $J_{SC\text{-}aperture}$ of 35.4mA/cm^2 and contributes to an efficiency of 8.34% after 10sec firing treatment at 600°C. This performance is unexpected and pretty low regarding the previous PeRFeCT test cell performance. On p side, a relatively enhanced passivation is obtained with 585mV V_{OC}, 40.2 mA/cm^2 $J_{SC\text{-}aperture}$, 55.1% FF and 12.96% efficiency.

While during illuminated J-V measurement for p bulk bifacial solar cell, only S-shape is obtained. The device functions as a resistor under dark J-V measurement, which reveals the fact that this solar cell is not acting as a diode. However precursor performance measured after c-Si surface passivation on both sides exhibits a iV_{OC} of 714mV and 1.038ms τ_{eff}. Speculation was made that metal evaporation induced great defect on wafer surface, which results in much recombination, detrimental for cell performance. Thus samples were immersed in 40% HCl to remove Aluminum on both sides and lifetime measurement regarding one complete p bulk wafer was made, given a degraded iV_{OC} to 617mV with 0.054ms τ_{eff}. The minority carrier lifetime versus MCD curve is plotted below in figure 4.10.

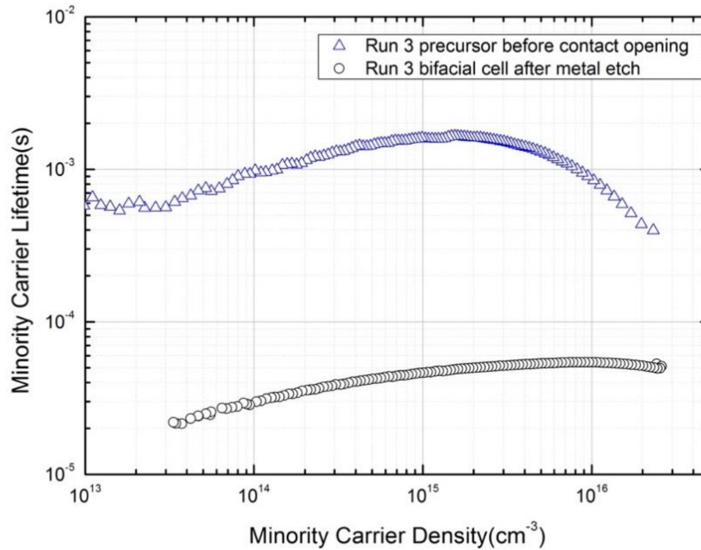


Figure 4.10 Minority carrier lifetime performance under varied MCD for p bulk bifacial cell precursor and cell after metal removal.

This significant degradation illustrates the problem not only from e-beam induced surface defects but also the possibility that poly-Si passivating layer might be partially damaged so solar cell passivation damaged. To have a clear idea of the surface topology of all these films, SEM is implemented and cross-section of p side surface in p bulk bifacial sample is detected as shown in figure 4.11 (1).

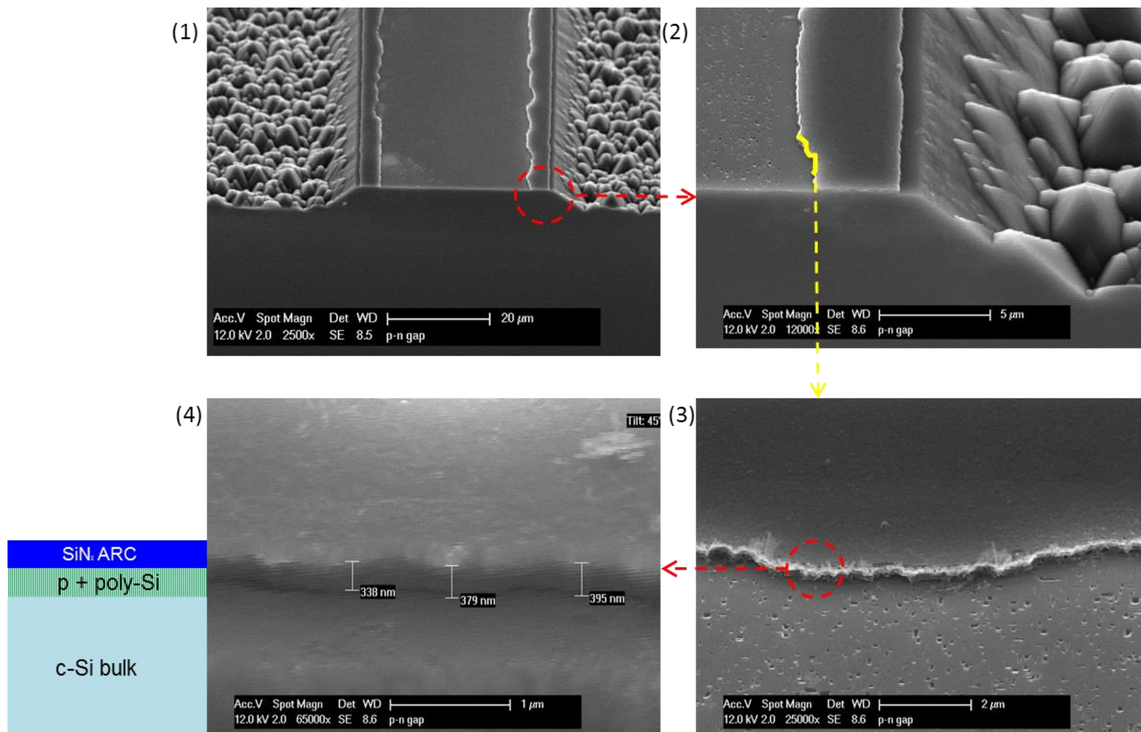


Figure 4.11 SEM images taken after metal etching away, showing partially removed poly-Si contact opening region on p+ side of bifacial solar cell.

In the middle is one finger of flat surface patterning. Because SEM is detected after metal removal, there's no Aluminum on top. The region beside finger pattern is textured c-Si surface with random pyramid structure. By higher resolution of 12000x in figure 4.11(2), a layer only lying on top of the finger pattern edge can be noticed and for the middle region on finger, obviously film material was etched away only left with some pinholes on surface. This deepens the speculation that partial ploy-Si film is removed. A 25000x cross-section image in figure (3) with 45° tilt angle gives a better view of the remaining layer by the edge (highlighted in yellow color in figure 4.11(2)) and the thickness of this outstanding edge is detected as 338nm, 379nm and 395nm with an average thickness of 371nm as shown in figure 4.11 (4).

Theoretically 300nm poly-Si was deposited on flat surface with SiN_x capping of 129nm thickness (75nm SiN_x deposited on textured surface for p+ c-Si passivation, corresponding to a thickness of 129nm with 1.73 times PECVD depositing rate on flat surface than on textured surface). A thickness of 429nm material should be expected by whole region of this flat finger. However, now only 371nm was detected by both edges of this finger. It means that besides the unavoidable poly-etch and developer in lithography step (TMAH based), which has isotropic etching into Si material, some etching steps, for example BHF, used during processing is not highly poly-Si selective.

For this $9cm^2$ solar cell, width of poly-finger is 50μm (considering after texturing approximately 40μm stays on the flat finger surface) and metal opening is 26μm. This reminds the fact that the largely removed poly-Si layer results from over-etch after contact opening step, supported by the SEM image that by poly-finger edges still a 371nm thick material stack remains. This is in line with previous experiment revealing BHF also etches n type poly-Si material if immersed for too long time. Also precursor measurement results convince us that poly-Si layer was still able to provide sufficient passivation after all surface passivation steps complete. Thus the overall BHF etching, poly-etch and TMAH developer immersing time within this batch of bifacial solar cell fabrication (classified by before contact opening stage and from contact opening till metal evaporation stage), are summarized below in Table 4.3.

Table 4.3 Summarized BHF, poly-etch and TMAH developer immersing time for bifacial solar cell fabrication.

Stage	Step	BHF time (min)	Poly-etch time (sec)	Developing (min)
Before contact opening	Alignment marker lithography	3+3	30	1
	SiO_2 protection removal	3	/	
	Poly-finger lithography	3+3	/	1
	SiO_2 protection removal	3	/	
	Removal of poor passivation	**15**	**8**	
Sub-total		33	38	2
Contact opening till metallization	Contact opening lithography	10+10	8	2.5+2.5
	2nd contact opening lithography	**10+10**	**8**	**2.5+2.5**
	Metal lithograhy			3
Sub-total		40	16	13
Total		73	54	15

Typically BHF is applied to etch the sacrificing SiO_2/SiN_X layer after photolithography or texturing. Wafers are poly-etched 30sec to create alignment marker into silicon bulk. Also poly-etch is applied after contact opening to remove 13.87nm a-Si passivation layer beneath metal contact for good conduct. It has to be pointed out that due to poor performance of first time c-Si surface passivation (mainly ALD deposited Al_2O_3/SiN_x stack), all the passivating layers on both sides were removed by 15min BHF and following 8 sec poly-etch to remove the a-Si layer. Also during contact opening, exposure on one side was not sufficient due to non-properly calibrated UV light intensity on contact aligner. Thus photoresist was removed and another series of contact opening lithography was processed. Totally 35min BHF, 16sec poly-etch and 5min developer immersion (bold in table 4.3) can be avoided if following standard processing in the bifacial flowchart as introduced in section 4.1.

Regarding the SEM image and summarized etching time, it's reasonable to speculate that before contact opening step, approximately 50nm poly-Si material is removed by BHF/poly-etch/TMAH based developing. Among them, 15min BHF and 8sec poly-etch to remove poor surface passivation are the main reason because poly-Si layer was not completely protected during that step.

For the over-etched poly-Si within middle region on finger pattern surface, 40min BHF,

16sec poly-etch and 13min rinsing in TMAH developer are responsible for its removal. Though during these etching steps, poly-Si material are initially covered with protecting layer but if immersed for too long time poly-Si are etched directly, which is a large loss regarding passivation performance. Without (or partially weakened) this highly doped poly-Si passivating contact, there's not sufficient band bending between c-Si/tunneling oxide/poly-Si interface, carrier selectivity also deteriorate. This explains the dramatically decreased passivation for bifacial solar cell compared to our PeRFeCT test cells and bifacial precursor.

However, based on all optimization, the PeRFeCT cell performance and the high passivation of bifacial cell precursor, we reasonably believe by smooth processing and avoiding any unnecessary etching step, the established flowchart is available to provide a good performed bifacial solar cell with poly-Si passivating contacts.

5

Conclusions and Outlook

5.1 Conclusions

The objective of this project is to fabricate bifacial solar cell with poly-Si passivating contacts which locates only underneath the metal fingers and to improve passivation of n/p doped poly-Si and n/p diffused c-Si front surface field aiming for its successful application in this advanced bifacial solar cell architecture.

For n/p highly doped poly-Si passivation, by dedicated optimization of film thickness (via LPCVD deposition time), annealing condition, dopants are well-confined within poly-Si doping profile and the created band-bending is sufficient to provide carrier-selectivity for good passivation. Optimized symmetric samples show a passivation result of $J_{0,n\,poly}$=5.4fA/cm^2 and $J_{0,p\,poly}$=10.9fA/cm^2 respectively with a film thickness of 300nm annealed at 950°C for 5min on flat surface.

For phosphorous diffused n+ c-Si, hydrogenated amorphous silicon is confirmed to provide good surface passivation. With 10keV energy and 1×10^{14}ions/cm^2 dose, ion implantation created n+ c-Si FSF, influence of a-Si:H thickness (via PECVD deposition time) is investigated. The optimized result shows that on textured surface, 13.87nm a-Si:H with 75nm SiN_X combined passivation layers are able to provide a J_0=14.5 fA/cm^2.

For boron diffused p+ c-Si, boron implantation approach is applied instead of previously implemented boron deposition via furnace. This enables uniformity on wafer, also a good control of boron doping profile. By ion implantation with 5keV energy and 5×10^{15}ions/cm^2 dose, annealed at 950°C for 5min, an average sheet resistance of 123Ω/sq is obtained. This enables the possibility to play with the trade-off between passivation and conductivity. To provide sufficient passivation for this p+ c-Si surface,

thermal ALD formed Al_2O_3 is used for its induced negative charge density efficiently repel minority carrier (electron) from p+ c-Si surface thus recombination reduced. The influence of film thickness and Forming Gas Annealing is studied and optimization results shows a greatly enhanced passivation after FGA and best performance of 10nm Al_2O_3/65nm SiN_X stack on textured p+ c-Si surface.

These optimizations are implemented on n/p bulk front/rear junction PeRFeCT (Passivated Front and Rear ConTacts) cells, which outstand for its combination of highly transparent doped c-Si surface on front side and highly doped poly-Si as passivating contacts. Such a structure enables both high V_{OC} and high J_{SC}. With the application of a-Si:H/SiN_X stack for n+ c-Si passivation, a V_{OC} increase of 31mV is achieved compared with reference. Also the other three PeRFeCT cell architectures were fabricated successfully, revealing the correlated solar cell V_{OC} performance with FSF passivation.

For the bifacial solar cell, a very high passivated **cell precursor with iV_{OC} of 714mV** was prepared. However, during bifacial solar cell fabrication, BHF, poly-etch and the TMAH developer in lithography step were proved to over-etch solar cell poly-Si passivating contacts. This results in a poor performance of 585mV V_{OC}, 40.2mA/cm^2 J_{SC}, 55.1% FF and 12.96% efficiency on n bulk p side and 546mV V_{OC}, 35.4mA/cm^2 J_{SC}, 45.9% FF and 8.34% efficiency on n bulk n side. Investigation via SEM confirmed the partial removal of poly-Si passivating material within contact opening region.

From the fabrication process point of view, the established flowchart is proved to be applicable for both bifacial solar cell with poly-Si passivating contacts and n/p bulk front/rear junction PeRFeCT cells. Optimization of p+ c-Si surface enables only one-time high temperature annealing to activate both implantation dopants for doped poly-Si and lightly doped c-Si. This simplified fabrication achieved the goal of energy-efficient for its industrialized implementation.

5.2 Outlooks

Based on the measured external parameters of bifacial cell, there's still large space for improvement in terms of V_{OC}, J_{SC} and FF. Also regarding solar cell fabrication, issues can come up with four series of photolithography or etching steps. Some recommendations will be made to reduce any avoidable experimental damage and further improve solar cell performance.

To enhance solar cell V_{OC}:

1) p+ c-Si surface passivation

There's still space to play with the trade-off between passivation and lateral carrier transport on p+ c-Si surface. Symmetric structures are supposed to be prepared for testing whether a good passivated surface can be obtained by 10nm Al_2O_3/65nm SiN_X with forming gas annealing treatment, on the optimized boron implanted c-Si surface with 123Ω/sq sheet resistance.

To enhance solar cell J_{SC}:

2) Reducing thickness of a-Si:H layer on n+ c-Si surface

Considering the high absorption coefficient of a-Si material in short wavelength, a thinner layer is expected for reducing current loss in this region on spectrum. Since typically a better passivation is obtained with thicker intrinsic a-Si layer, it's worth a trial to find solution for the trade-off between parasitic absorption and passivation quality. Also a sheet resistance around 550Ω/sq is reached for such 10keV, 1×10^{14} ions/cm^2 P implanted n+ c-Si surface, which is apparently not optimal for lateral carrier transport. By increasing implantation dose to 5×10^{14}ions/cm^2, R_{SH} reduces to 250Ω/sq [33] but more defects will be induced leading to higher recombination on surface. Thus the influence of implantation parameter with a-Si thickness on n+ c-Si surface should be studied to find a saturated point where good passivation can be achieved with thinner a-Si layer on a more conductive c-Si surface.

3) Reducing poly-Si thickness to improve optical performance

Poly-Si material exhibits a large absorption coefficient in long wavelength region (over 700nm) due to its high doping, which contributes to optical loss in EQE in the same wavelength region. To decrease the parasitic absorption, state-of-art researches are dedicated to adjusting the passivation performance for a thinner poly-Si up to 10-40nm [20] or PECVD in-situ doped poly-Si [67]. Also oxygen content can be alloyed with poly-Si film forming the wider-bandgap poly-SiO_X material. It shows much reduced free carrier absorption than poly-Si also reported with no absorption above 880nm [21], which enables poly-SiO_X a good candidate as passivating contacts in this bifacial solar cell structure.

To enhance FF:

4) New approach for metallization

Comparing typical high efficiency solar cell of over 80% fill factor, large difference can be observed for our 55% bifacial solar cell. By removing a-Si layer under n+ side metal contact opening and firing after metallization, a good contact is realized while there's still space for reducing series resistance. Besides, e-beam induced defects degrade surface passivation. Screen-printing with silver-paste and copper plating [46] are two potential approaches to replace Aluminum evaporation. Owing to the high conductivity and high height-to-width aspect ratio, these two methods are expected to achieve higher FF. A J_0 value around 350~400 fA/cm^2 was revealed for fire through screen-printed metal contacted poly-Si with 200nm thickness [68]. This also confirms the availability of industrialized metallization on our bifacial solar cell structure. However, considering the advanced design of our bifacial cell, probably new mask has to be designed for poly-finger lithography based on a more delicate printing metallization.

To improve fabrication:

5) Mask for back side alignment

For fabrication of bifacial solar cell, patterns are created by photolithography and normally both a front side mask and a back side mask are necessary. Currently we first create alignment markers on front side and then use back alignment on contact aligner to create makers on the other side. However, the designed mask is not symmetrical. If we follow the desired alignment marker, there will be a pattern-shift on rear side. Besides, non-symmetrical mask leads to metal patterning mismatch and varied metal coverage rates on front and rear cells in the same position on wafer. This makes it impossible to compare FF and J_{SC} performance of corresponding front junction and rear junction cell at same level. Considering lithography steps are most time-consuming process within bifacial cell fabrication, with a back alignment mask, the accuracy of lithography steps will be much enhanced also it makes alignment step time-efficient.

6) Accurate control of etching time

As illustrated in section 4.2, BHF, poly-etch and TMAH based developer are responsible for the partial removal of poly-Si passivation layer. It's highly recommended to give good

control of each etching step and have a test wafer for etching rate investigation. Also the choice of SiO_2 as protection layer for lithography and texturing can be widely applied instead of SiN_X, which accounts for five-fold lower etching rate in BHF. Thus with SiO_2 protection layer, much etching time can be reduced, enable it less possible to over-etch poly-Si material.

Regarding lithography, to avoid too much immersion in TMAH based developer, front and back exposure can be carried out successively followed by one-time developing of both sides. This avoids the over-developing of front side when processing development on rear side. But be sure to use edge chuck for contact alignment otherwise the coated photoresist can be scratched while processing the other side.

Acknowledgement

Firstly, I would like to thank my supervisor Olindo Isabella, daily supervisor Guangtao and also Gianluca, Paul for offering me great help during this thesis project. They guided me into this fantasy PV track, provided me with both theoretical and experimental knowledge related to semiconductor and solar cell fabrication. They showed their great patience and valuable suggestions whenever I went into bottleneck during experiments or couldn't find a reasonable explanation regarding my results. They taught me how to be more scientific, how to play with trade-off between V_{OC} and FF but also how to balance time between work and leisure life. I would also express my appreciation to technicians within PVMD and EKL for every specific issue during this ten-month thesis. Ten months is not long enough for such a novel project but also too short to work together with all these awesome big bosses in this amazing group.

In addition, I would like to extend my gratitude to all my friends. Yifeng, Zhimin, Peiqing, Hao, Yue, Yuan and all SET Chinese families, you are always the closest and lovely friends during my two-year life in Delft. Thanks for all the time you listening to my feelings, sharing happiness and celebrating important moments together. I also feel lucky to meet Bhavya, Anjali and Rosa. These wonderful girls are thoughtful, considerate and the most important is that they cook delicious Indian or Indonesian dishes! Thanks to you all, I lived a really full and interesting life during my master program here in the Netherlands.

Last but not least, hopefully these greetings can fly thousand miles away back to China, to my hometown Harbin. Words are limited but I really appreciate my parents for supporting me with every decision in my life. Always love you and miss you.

'For you, this special you, a thousand times.'

Yiran

EWI LB02.480, TU Delft

May 20, 2018

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