Powering Electronics worn by Group-Housed Rodents: A Control Loop Design for a Rodent's Headstage

From Exploration of a Potential Power Link to the Implementation of the Control Loop for a Power Converter

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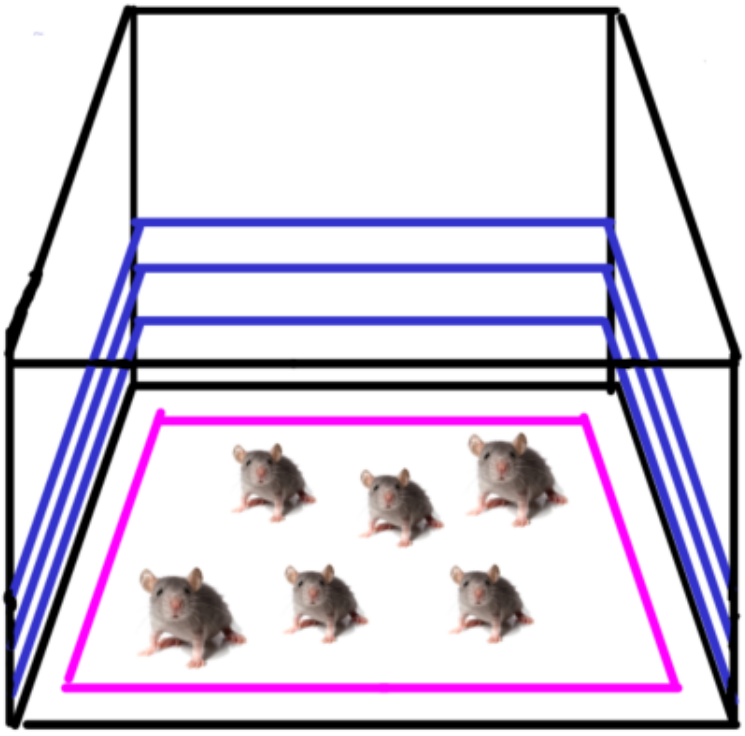
MSc. Electrical Engineering



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Powering Electronics worn by Group-Housed Rodents: A Control Loop Design for a Rodent's Headstage

From Exploration of a Potential Power Link to the Implementation of the Control Loop for a Power Converter

by

Kwok Hang Luo

Master's Thesis

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Abstract

This study aims to systematically design and implement a voltage regulation control loop (VRCL) for an unspecified power management unit (PMU) to maintain the desired load voltage for electronics worn by group-housed rodents. This is crucial for analyzing the spontaneous behaviour of group-housed rodents, focusing on social interactions and environmental exploration in a simulated natural environment.

The study explores a potential high-level design of a power link, selecting resonant inductive coupling for wireless power transfer (WPT), enabling continuous power supply over larger areas (for instance, 5 by 5 meters). A literature review reveals a research gap in integrating encircling and underneath configurations for sufficient uniform power distribution. A block diagram of the WPT system is provided, outlining the transmitter and headstage receiver components. Subsequently, a hybrid layout is suggested and significant challenges like optimizing driving current and minimizing angular and vertical misalignments are addressed.

Next, a control loop is systematically designed and implemented. Potential loads and a PMU are selected, followed by the development and verification of an ideal power converter and its derived and proposed plant model. Control specifications derived from this model suggest the tuning of the controller parameters using a tailored model-based control-system approach. MATLAB simulations confirm that the control specifications are met. A non-ideal power converter is then integrated with the control loop, including ideal gate drivers, a voltage-controlled oscillator, a bandgap reference, and a PI controller. Simulation results show that the control loop meets the specifications. Despite limitations in robustness, particularly regarding load and input voltage transient response, the study also highlights the need for verification of the power converter model for load capacitors in the pF-nF range, and identifies discrepancies in overshoot behaviour. Future work includes an analysis of the system's robustness during controller tuning and the incorporation of a transient controller. The combination of the suggested plant model and model-based tuning approach offer an alternative option for the power converter's control loop design.

Acknowledgements

This report contains the thesis work I have been engaged in for a year to obtain my Master of Science in Electrical Engineering at the Technical University of Delft, marking the end of my graduate program in Microelectronics. My thesis involves energy harvesting, control system design, and CMOS design. This experience has been invaluable, as complex projects will require systematically approaching problems to achieve first-time-right and first-time-best solutions, as my supervisor would say.

I would like to express my gratitude to PhD students Kimia Ahmadi and Arash Akhoundi and the technician of the BE group, Tarique Mohd. Kimia provided relevant sources for wireless power transfer and also discusses my progress, and Arash was helpful in discussing potential loads and offering tips during my project. Moreover, Tarique assisted me with Cadence and took the time to discuss the encountered problems and offered tips what to look for. I also want to thank the entire BE group for providing the necessary tools for the project and for holding group meetings relevant to my work.

While the project was challenging at times, I am grateful to my supervisor, Wouter Serdijn, for his encouragement and excellent feedback during discussions and supervision. Without his input, my thesis report would not have reached its current quality, which is potentially the best thesis report I have written during my entire life at college and university. I also want to thank Dr. Ir. C.J.M. Verhoeven and Dr. Ir. M. Jafarian for their willingness to serve as thesis committee members and provide feedback on my work.

Lastly, I would like to thank my family for their support during tough times.

Kwok Hang Luo
Delft, August 2024

Contents

Reading Guide

The thesis report consists of two parts: a potential power link approach (Part I) and the design of a voltage regulation control loop for a mouse's headstage (Part II).

If you prefer to read the following:

1. **A specific part:** please refer to Table 1 for the specific subject or the topic that closely aligns with your interests.
2. **Control design and the implementation of the control loop only:** before delving into Part II, start with Section 6.1 to gain an understanding of the block diagram of the WPT system.
3. **Power link approach only:** please refer to Part I.
4. **Both the power link approach and the design of the control loop:** please read Part I and II from the start to the end.

Table 1: A guide for reading based on specific topics categorized into relevant chapters and appendices.

Specific subject	Chapter	Part	Appendix/Appendices
Selection of the energy harvesters for the targeted application.	2.3	I	-
Potential specifications for the Nat-B lab.	3.2	I	-
Selected energy harvester mechanism.	4.4	I	-
Overview of the existing continuous power supply systems for homecages.	5.1	I	A.1
A suggested power link approach for the Nat-B lab.	6.2	I	-
The working principle of the selected power converter type.	10.1.1	II	-
Overview of the existing control loops for the selected power converter type and its limitations.	10.2.2	II	-
Sizing of the selected ideal power converter.	11.1	II	B.2.1, B.2.2 B.2.3, C.3.1 and C.3.2
Sizing of the selected non-ideal power converter.	12.2.4	II	C.3.2 and D.4.5
The plant model of the power converter.	11.2.1	II	D.4.1
The tailored control-system approach for controller tuning.	11.2.3	II	C.3.3, D.4.4 and D.4.6
The implementation of the control loop.	12	II	D.4.3, D.4.5, B.2.4
Control specifications.	11.2.2	II	-
Simulation results of the control loop.	12.3	II	D.4.7
Selected load and PMU for the control loop assessment.	9	II	-

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Nomenclature

Abbreviations

Abbreviation	Definition
AFE	Analog front-end
BGR	Bandgap reference
CLPC	Closed-loop power control
CPT	Capacitive power transfer
DUT	Device Under Test
EH	Energy harvesting
EMI	Electromagnetic Interference
GSM	Global system for mobile communications
ICNRP	International Commission on Non-ionizing Radiation Protection
IMD	Implantable medical device
IMN	Impedance matching network
IPT	Inductive power transfer
IR	Infrared
ISM	Industrial, Scientific, and Medical
MEMS	Micro-electromechanical Systems
MPPT	Maximum power point tracking
NIR	Near-infrared region
NOV	Non-overlapping clock generator
PDL	Power delivered to load
PM	Permanent magnet
PTE	Power transfer efficiency
RF	Radio frequency
RIPT	Resonant inductive power transfer
SAR	Specific absorption rate
SIMD	Semi-implantable medical device
SRF	Self-resonance frequency
UPT	Ultrasonic power transfer
VCO	Voltage-Controlled Oscillator
VCR	Voltage conversation ratio
VRCL	Voltage regulation control loop
WPT	Wireless power transfer

I

Potential power link approach

1

Introduction

1.1. Background

Animal studies in neuroscientific and behavioral research often use rodents to observe spontaneous behavior without external stimulation, providing insights into brain activity. Data is collected from rodents' natural actions in small cages due to their behavioral and physiological similarities to humans. For example, a small homecage was used in [1] to treat chronic neural diseases.

The research project DBI^2 aims to expand spontaneous behavior analysis to group-housed rodents, focusing on their social interactions and environmental exploration. Small cages can lead to poor ecological validity and abnormal behaviors due to stress. Therefore, simulating a natural environment in the lab room, which is called the Nat-B lab, is needed. This presents challenges in powering electronic devices used for neural recording, neuromodulation, biosensing, signal processing, edge computing, control and data exchange that are worn by group-housed rodents due to varying environmental factors.

In previous studies such as [1] and [2], wireless power transfer (WPT) systems have been proposed for utilization in homecages, which are commonly designed for housing one or two animals. In these studies, the receiver in the WPT system is the headstage of the rodents. The headstage refers to a device that is attached to the head of an animal, typically a rodent, and is used to interface the animal's brain in order to monitor and stimulate neural signals for various purposes, such as studying the brain function. This requires the headstage to have a continuous power supply. WPT is commonly used in biomedical devices to reduce infection risks and weight, as seen in [2], However, it is not the only method available. To study group dynamics effectively, a Nat-B lab with sufficient space is necessary.

The overarching research question that is at the base of Part I of this thesis becomes: **how can a high-level WPT system potentially be designed to provide power to group-housed rodents in the Nat-B lab, simulating a naturalistic environment?**

1.2. Organization of Part I

Chapter 2 provides a comprehensive exploration of various energy-harvesting methods, evaluating their respective merits and drawbacks.

Chapter 3 presents specifications for the designated application, accompanied by brief explanations of the selected criteria.

Chapter 4 reviews prevalent WPT mechanisms employed in biomedical contexts and the most suitable approach is chosen for the intended application.

Chapter 5 briefly discusses state-of-the-art WPT systems, offering a brief overview of their pivotal limitations and identifying a key research gap in the field.

Chapter 6 elaborates on a potential high-level design approach, encompassing a description of the laboratory environment alongside a schematic depiction of the envisaged WPT system's components.

Chapter 7 concludes Part I by addressing the research question, introduced in Chapter 1.

2

Energy harvesters

2.1. Energy harvesting in biomedical devices

Conventional implants are typically powered by batteries, but this method has several drawbacks:

1. **Size and weight:** batteries add significant size and weight to the rodent's headstage.
2. **Battery replacement:** limited battery life requires frequent replacements, often involving surgical procedures, which undermines device reliability.
3. **Power dissipation:** batteries have internal resistance that causes power dissipation, posing risks to rodents.
4. **Leakage and energy density:** batteries suffer from leakage and reduced energy densities during discharge, particularly when idle, leading to decreased longevity.

To address these issues, battery-less (semi-)implantable medical devices ((S)IMDs) have been developed, harnessing ambient energy sources to power wearable electronics and biomedical devices.

2.2. Types of energy harvesters

Energy harvesting (EH) is categorized into two types: ambient EH and human EH. Human EH uses the human or animal body as a power source, while ambient EH utilizes environmental sources such as light, wind, vibration, and RF radiation. These types of energy harvesters are commonly used in biomedical devices, shown in Figure 2.1.

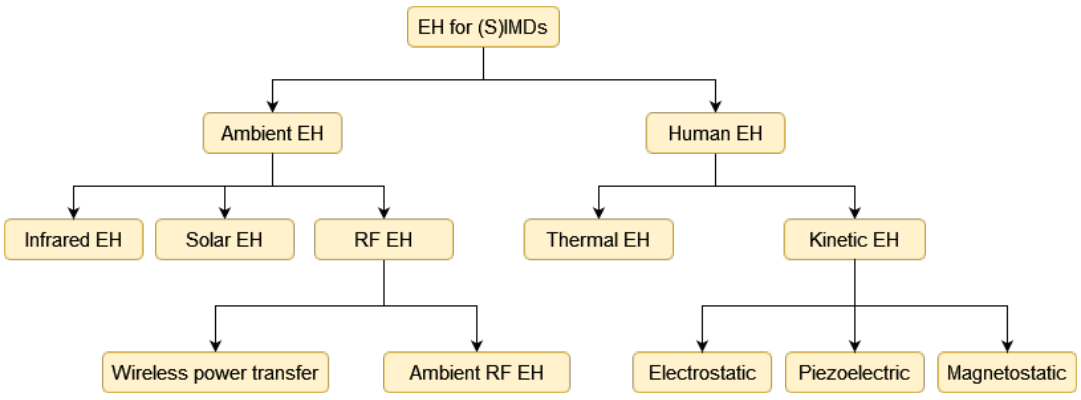


Figure 2.1: Types of energy harvesters for biomedical devices.

2.2.1. Solar energy harvesting

Solar EH involves converting sunlight or other light sources into electrical energy, typically achieved through photovoltaic cells or solar panels. In biomedical applications, photovoltaic cells are frequently used. Figure 2.2 illustrates a simple model of a solar cell.

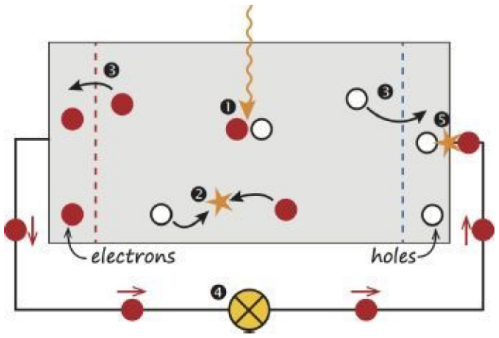


Figure 2.2: A simple solar cell model [3].

The working principle of a solar cell involves capturing light to generate excess electrons, creating electron-hole pairs. These pairs are separated by semipermeable membranes [3], resulting in electrons flowing to the anode terminal, generating a current flowing through the LED. However, recombination of electrons and holes occur, which degrades the efficiency of the solar cell.

Common solar cell materials include amorphous, monocrystalline, and polycrystalline silicon, with varying efficiencies [4]. Despite limitations such as size dependency of the solar cell and reduced energy generation in low-light conditions, solar energy harvesters offer advantages like sustainability, long-term cost savings, and high power density. However, challenges include the need for battery storage during low-light conditions, such as seasonal variations, and increased power dissipation due to the additional components like maximum power point tracking (MPPT) mechanisms. Despite drawbacks, solar energy harvesters find applications in various fields, including biomedical applications, such as in study [5].

2.2.2. Thermal energy harvesting

Thermal EH utilizes the Seebeck effect in a thermocouple or thermoelectric module to convert heat from a human or warm-blooded animal body into electrical energy. The process involves three steps: generating a temperature difference, generating voltage, and managing the load and power.

A temperature gradient is created across the thermoelectric material by exposing one side to a heat source (such as an animal body) and the other side to a heat sink (the surrounding environment). This temperature difference leads to the generation of a voltage across the material due to the Seebeck effect, as described by Equation 2.1 [4].

$$V_{thermal} = N \int_{T1}^{T2} \alpha \, dT = \alpha N \Delta T \tag{2.1}$$

N represents the number of thermocouples connected in series, α is the Seebeck coefficient of a thermoelectric material and ΔT is the temperature difference. This voltage can be scavenged and used as electrical energy. The harvester can be modeled as a voltage source in series with an internal resistance. For biomedical devices utilizing thermal energy harvesting, a power management circuit is typically incorporated to optimize energy transfer and regulate the electrical output, given the small voltage output ranging from 0 mV to 25 mV [6].

Thermal EH presents several advantages for biomedical applications. Firstly, thermoelectric harvesters offer reliability and longevity due to their solid-state nature, requiring minimal maintenance and ensuring high reliability. Secondly, their compact size enables efficient design, with advancements like organic thermoelectric nanomaterials allowing for self-powering without adding significant bulk [7]. Additionally,

utilizing heat from human or animal bodies eliminates the need for external power sources and frequent battery replacements. Finally, the wide temperature range they can operate in allows for harvesting from various heat sources encountered in different biomedical settings, enhancing flexibility and applicability.

However, thermal energy harvesters also have limitations. Their conversion efficiency is constrained by the Carnot efficiency, limiting the maximum energy that can be collected from heat [8]. This limitation is described by Equation 2.2.

$$\eta_c = \frac{T_{body} - T_{ambient}}{T_{body}} \tag{2.2}$$

In practice, the conversion efficiency (η_c) of thermal energy harvesters is lower than the theoretical Carnot efficiency due to the various factors, as this only contains the thermoelectric module efficiency . For example, assuming a room temperature of 20 °C ($T_{ambient}$ in kelvin) and a typical body temperature of 37 °C (T_{body} in kelvin), the Carnot efficiency would be 5.5%. Increasing the environmental temperature decreases this efficiency.

Using wires to connect thermoelectric modules to a load or device, raises concerns in biomedical applications for rodents when not integrated into MEMS technology. These wires may be perceived as threats, leading to behavioral changes like chewing, and can introduce noise during data collection, affecting accuracy. Additionally, excess heat dissipation may cause tissue damage.

The power extractable from the human or animal body is limited by the temperature gradient. To maximize the temperature gradient, thermoelectric energy harvesters are often placed under or on the skin, enhancing gradient and power generation capabilities [6].

2.2.3. Kinetic energy harvesting

Kinetic EH involves the conversion of mechanical energy into electrical energy, which is accomplished by three common techniques: piezoelectric conversion, electrostatic and magnetostatic conversion.

1. Piezoelectric conversion

Piezoelectric energy harvesters utilize materials like quartz, lead zirconate titanate (PZT), and polyvinylidenefluoride (PVDF), generating charge when mechanical stress is applied, known as the direct piezoelectric effect [9]. They offer advantages such as high output power (2-8 mW) in wearable electronics and flexibility in design, crucial for implantable devices due to the size and weight constraints [7].
Their scalability allows adjustment for optimal energy conversion efficiency by matching vibration frequencies, thereby maximizing energy conversion efficiency.

However, limitations exist. Matching device resonance to mechanical frequencies, typically low (for instance, 2 Hz) in human motion increases size and weight, posing challenges for IMDs. Balancing size and efficiency are crucial. Additionally, output power (<10 μW) in implantable devices may be insufficient for certain applications, like neurostimulators requiring 50 μW [6].

2. Electrostatic conversion

Electrostatic energy conversion uses capacitive devices to convert mechanical energy into electrical energy in two stages. First, vibrations are converted into motion between two elements via a mass-spring system. Second, a variable capacitor adjusts its distance or area between plates in response to mechanical stress, altering the capacitance.
Electrostatic energy harvesters have three types of variable capacitors: variable area, variable gap, and, rarely, variable dielectric capacitors. One capacitor plate remains fixed while motion changes the capacitance on the other plate. Mechanical-to-electrical energy conversion is achieved through fixed charge cycle and voltage cycle. The fixed charge cycle process is illustrated in Figure 2.3.

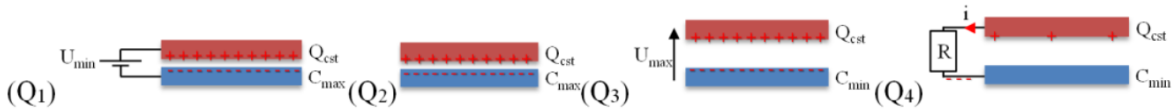


Figure 2.3: Fixed charge cycle process [10].

To elucidate this process, Equation 2.3 is used for a brief explanation of the process.

$$Q = CV_{cap} \tag{2.3}$$

In Figure 2.3, the fixed charge cycle process involves four steps: (Q1) the variable capacitor is pre-charged with a constant charge, Q_{cst}, at minimum voltage, V_{min}; (Q2) the system is open-circuited; (Q3) mechanical motion alters the capacitor's geometry, decreasing capacitance until it reaches C_{min}; (Q4) as Q_{cst} remains constant, voltage increases to V_{max}, driving current through the load. The fixed voltage cycle approach, shown in Figure 2.4, keeps the voltage fixed throughout the process.

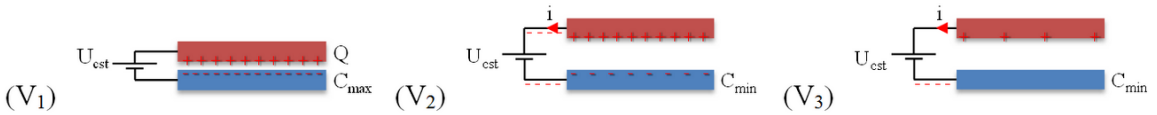


Figure 2.4: Fixed voltage cycle process [10].

As illustrated in Figure 2.4, the fixed voltage cycle process also involves four steps, which are the following: (V1) the variable capacitor connects to a constant voltage, V_{cst}; (V2) the spacing between elements increases, hence capacitance decreases; (Q3) with voltage fixed, charges (Q) rise, generating current. This leads to charge accumulation, which is stored when capacitance reaches C_{min}.

Electrostatic energy harvesters are advantageous for biomedical applications due to their integration into MEMS technology, enabling compact designs suitable for internal use [6]. Additionally, they excel in ultra-low power scenarios, with output ranging from 24 µW to 80 µW, meeting requirements for devices like neurostimulators [6]. Their high efficiency, achieved by minimizing plate spacing, increases capacitance and improves power generation, further enhancing their appeal.

However, challenges exist. Pre-charging of electret-free devices adds complexity and is sensitive to parasitic capacitance, especially in MEMS integration, leads to power losses and efficiency reductions due to the additional pathways for the current flow.

3. Magnetostatic conversion

The magnetostatic energy harvester is composed of a mass spring system, a coil, and a permanent magnet, operates based on the oscillation frequency of vibrations. In contrast, rotational harvesters use rotational power from machines like wind turbines, and hybrid harvesters convert linear motion into rotational motion, which are less commonly used in biomedical applications [11]. A generic resonant generator is shown in Figure 2.5.

The resonant generator operates on the magnetostatic principle, described by Lenz's and Faraday's laws, as shown in Equation 2.4.

$$\mathrm{EMF} = -\mathrm{N}\frac{d\Phi}{dt} \tag{2.4}$$

In this equation, EMF represents the induced voltage, N is the number of turns around the coil, and $\frac{d\Phi}{dt}$ is the time-varying magnetic flux. In a magnetostatic energy harvester, either the coil or the permanent magnet (PM) is fixed, while the other moves, causing a varying magnetic flux and inducing a voltage in the coil. When connected to a load, this induced voltage leads to the generation of current. The amount of voltage generated depends on the number of coil turns, the magnetic field strength, and the motion velocity of the coil or PM [9]. Maximum induced voltage, due to the greatest swing of vibration

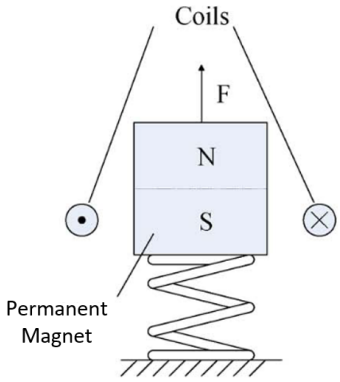


Figure 2.5: A schematic overview of how the main components are connected [11].

and hence maximum flux variation, occurs when the harvester operates at its resonance frequency, matching the mechanical resonance frequency.

Magnetostatic energy harvesters can generate both high and low power outputs, depending on their design. For example, a rotational structure generated 3.4 mW using blood flow and pressure, with a device weight of 24 g [12]. Another study demonstrated a mass imbalance oscillation generator producing 16.7 μW and 30 μW in *in vivo* and *in vitro* experiments, respectively, with a device weight of 16.7 g [13]. These harvesters are scalable and can be adapted for various applications, from biomedical devices like pacemakers to large-scale machines like wind turbines.

However, there are drawbacks, especially for (S)IMDs. The addition of a permanent magnet and a coil makes these harvesters relatively large and heavy, often exceeding 10 g, for instance, in studies [12] and [13], which may be too heavy for some (S)IMDs. Additionally, the output voltage is typically below 0.1 V due to the limitations in the number of coil turns achievable with MEMS technology [11], [14]. This low-voltage output requires rectification and/or power management. Moreover, integrating a magnetostatic energy harvester in MEMS technology is challenging due to the miniaturized nature of MEMS systems and the incompatibility of fabrication techniques like photolithography and etching with the creation of coils and permanent magnets [14].

2.2.4. Infrared energy harvesting

All warm objects emit infrared (IR) energy, a special kind of electromagnetic wave. These waves can be utilized to harvest energy. A specific example of this approach, implemented in a mm-scale system, is described in [15]. The general principle of harvesting energy from infrared waves is depicted in Figure 2.6.

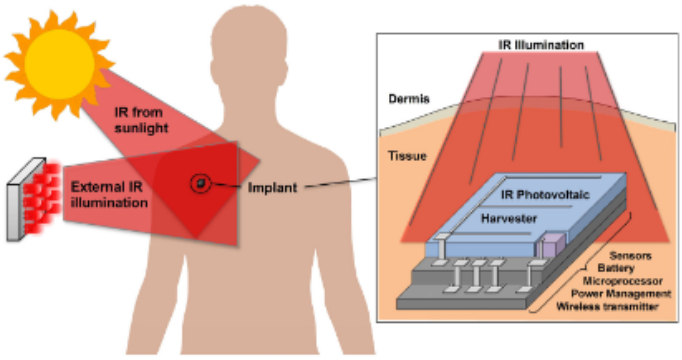


Figure 2.6: General principle of infrared energy harvesting [15].

The figure illustrates two main components: the IR provider and the IR receiver. The IR provider can be

an external source or sunlight-derived IR radiation, including laser diodes emitting near-infrared (NIR) radiation. The NIR wavelength range (650 nm - 1350 nm) is advantageous for its effective penetration of biological tissues, enabling power transfer through them [15]. The IR receiver comprises photovoltaic cells or an integrated photodiode, positioned just below the skin surface to maximize transfer efficiency. These cells, made from materials like silicon or InGaAs, offer power efficiencies exceeding 17% and 31%, respectively [15]. However, achieving high efficiency for small-area photovoltaic cells under low irradiance conditions poses a challenge due to the increased susceptibility to recombination losses, leading to reduced power efficiency.

IR EH offers advantages such as safety for humans and animals due to its non-ionizing nature, unlike X-rays used in medical imaging. IR frequencies are also less susceptible to noise interference and can effectively penetrate biological tissues, depending on their wavelength [7]. These characteristics make IR EH suitable for various biomedical applications where safety, noise immunity, and tissue penetration are crucial.

However, IR EH faces limitations. The size of the energy harvester, particularly the large photovoltaic cells, can be bulky, potentially generating excess heat and consuming more power. This may not be suitable for compact and low-power biomedical applications. Moreover, IR radiation can cause tissue damage due to heat generation, posing a concern that requires careful consideration. Additionally, the transfer efficiency decreases rapidly with increasing distance between the IR source and the target device, which is a critical factor to address in IR EH system design.

2.2.5. RF energy harvesting

RF EH involves capturing electromagnetic waves, like Wi-Fi signals, and converting them into electrical energy using a rectenna (rectifying antenna), which can be classified into ambient RF EH and wireless power transfer categories.

Ambient RF energy harvesting

Ambient RF EH aims to harness electromagnetic energy from the environment, predominantly in the form of RF waves emitted by various sources, such as radio broadcasting stations and GSM networks [16], which involves the use of rectennas. The RF spectrum encompasses frequencies ranging from 3 kHz to 300 GHz, depending on the sources.

This EH method presents several advantages. Firstly, it offers continuous energy harvesting as RF waves are omnipresent, ensuring uninterrupted power for devices like IMDs, crucial for operations in challenging environments, such as aircraft or chemical plants. Another advantage is the lightweight nature of RF energy harvesters, typically weighing only 2 to 3 grams, making them suitable for applications like IMDs in animal studies [17]. Integration with other EH technologies is also feasible, as demonstrated in study [18] where antennas were integrated with photovoltaic cells, enabling simultaneous DC power provision for electronic circuitry and RF antennas for wireless communications, thereby reducing costs and space requirements. Moreover, ambient RF EH eliminates the need for wired connections, relying on RF waves for power transfer, which is advantageous for (S)IMDs, considering animal welfare concerns. Lastly, ambient RF EH offers a broad coverage area, leveraging high-output power RF signals from sources like TV towers, with potential power outputs reaching up to 1 MW [18].

However, ambient RF EH faces several limitations. One challenge is the low RF power density, sometimes as low as 0.2 nW/cm^2, which complicates antenna design [17]. To address this, antennas need to be placed in areas with denser RF sources, like urban environments. Another limitation is the variability in RF power levels due to environmental factors like location and signal strength. Designing antennas must consider this variability, requiring a balance between power level range, frequency, and size constraints. Lastly, the distance between the transmitter and receiver affects the power received by the RF energy harvester.

Wireless power transfer

Wireless power transfer (WPT) and ambient RF EH differ in control over power levels and power sources. Ambient RF EH harnesses energy from existing RF sources, leading to unpredictable power

fluctuations. In contrast, WPT systems have dedicated transmitters, offering control over power levels, which must comply with regulatory standards like FCC or ETSI [19]. Two different types of WPT systems are near-field and far-field, with near-field often using inductive coupling for high efficiency but limited distance. Far-field WPT, on the other hand, operates at greater distances using radiative coupling, transmitting electromagnetic waves through the air. It enables power transmission over longer ranges but may have lower efficiency compared to near-field techniques.

WPT shares some advantages with ambient RF EH, including integration with other energy harvesting technologies and contactless power provision to electronics. However, WPT offers advantages over ambient RF EH by providing control over power levels and signal strength, ensuring a more consistent and reliable energy source. Nevertheless, WPT has limitations, such as the critical distance between the source and target, increased complexity, and the cost of the system with the addition of the power transmitter(s).

2.3. Energy harvester for the targeted application

In the specific case of the targeted application, the welfare of the rodents must be taken into account. Mice and rats are highly sentient animals and can experience suffering in certain situations [20]. For example, a large headstage restricts the mobility of the rodent. Minimizing the size and weight of the headstage reduces the burden on the rodent, allowing them to move more freely and naturally. Considering the high sentience of rodents, their response to tissue damage can lead to significant pain, similar to humans. Therefore, the criteria chosen for eliminating certain types of energy harvesters include size and weight, elimination of wires, MEMS integration, and potential power levels.

When looking at MEMS integration and elimination of wires, thermal energy harvesting and magnetostatic conversion are ignored due to the potential use of wires and the addition of permanent magnets and coils, respectively. Considering size and weight, solar, infrared, and electrostatic energy harvesting are neglected due to the potential size of solar cells in solar and infrared energy harvesting, seasonal variations affecting solar availability, and the pre-charging requirements of electret-free devices in electrostatic energy harvesting.

Regarding potential power levels required, an estimation of the required load power of 13 mW is made, which may differ depending on the load design. Piezoelectric and ambient RF energy harvesting are insufficient for this application: piezoelectric energy harvesting might not provide sufficient power if a higher load power is expected than the estimated value (13 mW), and ambient RF energy harvesting relies on unpredictable power levels and low RF power density (nW/cm^2 to μW/cm^2), which may not meet the power requirements for the targeted application [17]. Wireless power transfer (common coupling mechanisms of WPT being discussed in Chapter 4), on the other hand, allows for controlled power levels, making it the preferred choice for the targeted application.

3

High-level system specifications

3.1. Rodents in a laboratory environment

The study of spontaneous behavior in laboratory mice and rats reveals differences in behavior under identical conditions, including cage size and the number of rodents. These differences encompass social interaction, cognition, addictive behavior, and impulsivity. In the DBI^2 project, the emphasis is on investigating social behavior.

The main differences in social behaviour between mice and rats are summarised in Table 3.1.

Table 3.1: Summary of the main differences in social behaviour between mice and rats [21].

Rodent species	Social behaviour
Rats	Less territorial and open to friendships with male rats.
	Higher social interaction with each other.
	Lower aggression than mice.
	Prefer areas where they had social interaction.
Mice	More aggressive than rats.
	More territorial against other male mice.
	Mice avoid areas where they have met other mice.
	Social interaction is considerably less.

Understanding the high-level system specifications may seem disconnected from the differences observed in social behavior. However, from the standpoint of neuroscientists, comprehending neuronal collaboration and responses are crucial. For instance, variations in responses among rodents of the same species are of interest to researchers studying social behavior. Once a specific rodent is chosen, the WPT system needs adaptation to suit it, potentially necessitating adjustments in the high-level system specifications.

The size and weight of the headstage are crucial specifications that depend on the chosen rodent model. Table 3.2 serves as a guideline for establishing these specifications.

Table 3.2: Summary of weights of adult mice and rats [22].

Species	Size	Weight (g)
Male mouse	Small	22
	Medium	38
	Large	52
Female mouse	Small	20
	Medium	33
	Large	45
Male rat	Small	232
	Medium	424
	Large	597
Female rat	Small	140
	Medium	354
	Large	486

The weight constraint for the headstage is less strict when using a rat compared to mice. Adult mice typically weigh between 20 g and 52 g, while adult rats weigh between 140 g and 597 g, as shown in Table 3.2. It is suggested that the overall weight of the system should be less than 10% of the body weight of the rodent [23]. For adult mice, the headstage weight ranges from 2 g to 5.2 g, and for adult rats, it ranges from 14 g to 59.7 g. These figures are based on adult rodents, and for weanling mice and rats, with weights around 10 g and 45 g, respectively, the headstage weight should not exceed 4.5 g for rats and 1 g for mice [24], [25].

Additionally, the size of the headstage should be designed to fit the rat or mouse head, with considerations for differences in head size. While size matters, weight is prioritized as it affects rodent movement and stress. Based on the meeting with a colleague from the DBI^2 project, the mouse has been chosen for initial experiments on spontaneous behavior analysis.

3.2. Specifications

A list of the mandatory specifications for the Nat-B lab and the WPT system are given in this section. Assumptions were made and listed below.

1. At least three mice are used.
2. An area with small trees, sand and grass to simulate the naturalistic environment is used.
3. The lab experiment takes place in the Nat-B lab for conducting animal studies.
4. The load of the WPT system is a system that enables data recording and stimulation.

Tables 3.3 and 3.4 list the specifications for the Nat-B lab and WPT system, respectively.

Table 3.3: The mandatory specifications of the Nat-B lab for research experiments.

Nat-B lab specifications	
Functional specifications	
1	The Nat-B lab shall have an area size of at least 5 by 5 meters to accommodate three or more mice.
2	The Nat-B lab shall contain mice, from weanling to adult's mice depending on the preference of the researchers.
3	The Nat-B lab shall contain at least a method to track the mouse.
4	The Nat-B lab shall contain temperature control, ventilation, lighting and veterinary care to imitate naturalistic environment.
Non-functional specifications	
1	The amount of WPT system components, for example a TX pole, shall be reduced as much as possible to keep the room area unobstructed.

The Nat-B lab shall have an area size of at least 5 by 5 meters to accommodate three or more mice.
The Nat-B lab in the DBI^2 project aims to replicate a natural setting for observing mouse behavior. Collaborators suggest a room size of at least 5 by 5 meters or larger. Considering typical rectangular room shapes, a size of 5 by 6 meters is chosen as an initial standard.

The compulsory specifications of the WPT system are given in Table 3.4.

Table 3.4: The mandatory specifications of the WPT system.

WPT system specifications	
Functional specifications	
1	The transmitter shall provide a minimum power level of 16 dBm to power the receiver.
2	The receiver shall harvest power while the receiver is at any orientation from 0° to 90° with respect to the cage surface plane.
3	The receiver shall have a size of less than or equal to 1.1 cm^3, obtained from [26], for the mouse depending on the mouse age.
4	The receiver shall have a weight of less than 5.2 g for an adult's mouse or less than 1 g for a weanling mouse to prevent induced stress and decrease of mobility.
5	The receiver shall provide a stable output voltage of 1.1 V for the recording and digital signal processing (DSP) and 3.3 V for the stimulation load.
6	The receiver shall include a power management block responsible for regulating and converting voltages to the required output voltage(s) for the load.
7	The WPT system shall provide support of continuous operation in the 'dead zones' as the received power varies due to the movement of the mouse.
8	The WPT system shall operate at a frequency of 13.56 MHz in accordance with the ISM standard, which is approved by the ICNRP.
9	The WPT system shall include an impedance matching block to match the source with the load to minimize power losses and prevent a portion of the transmitted power being reflected back to the source.
10	The WPT system shall have a built-in mechanism for detecting any faults or malfunctions, ensuring the safety and well-being of the animals.

Continued on next page

Table 3.4: The mandatory specifications of the WPT system. (Continued)

11	The WPT system shall support multiple headstages of the mice in the Nat-B lab.
12	The WPT system shall include mechanisms for power regulation and control to prevent over- and undercharging of the receiver.
Non-functional specifications	
1	The receiver shall have a small form factor to minimize discomfort, induced stress and decrease of mobility of the mice.
2	The WPT system shall have an extra power source in case of power outages or system failures of the Nat-B lab.
3	The WPT system shall contain safety measures of excessive power levels or electromagnetic fields to reduce the risk of the mice's health.
4	The WPT system shall follow the Directive 2010/63/EU standards for animal welfare.
5	The WPT system shall aim to minimize system complexity in order to mitigate the risk of device failure, particularly on the receiver side.
6	The WPT system shall not hinder mice's natural behaviour or mobility in the Nat-B lab.
7	The WPT system shall be robust to environmental factors such as electromagnetic interference and temperature variations within the Nat-B lab.
8	The WPT system shall have proper grounding and insulation to ensure electrical safety for lab experiments.
9	The WPT system shall allow for smooth integration with other tracking and data collection systems used in the Nat-B lab.
10	The WPT system shall have a low failure rate, minimizing the need for frequent maintenance or repairs.
11	The WPT system shall provide efficient power transfer with high power transfer efficiency to minimize energy losses.
12	The WPT system shall operate in a large and unobstructed Nat-B lab.
13	The WPT system shall not block the view of the cameras around the Nat-B lab.

The WPT system shall provide support of continuous operation in the 'dead zones' as the received power varies due to the movement of the mouse.
From the rodent's perspective, as it moves within the Nat-B lab, there may be areas where the magnetic field is weak, potentially resulting in a significant decrease in received power. These areas, commonly referred to as 'dead zones' or 'blank spots' can pose a problem as they may result in a lack of power supply to the electronics worn by the mice.

The transmitter side of the WPT system shall provide a minimum power level of 16 dBm to power the receiver.
The WPT system for mice comprises three main components: digital signal processing (DSP), stimulation, and recording. The initial estimated power specification, power delivered to load (PDL), is set to 13 mW, in collaboration with the designer of the WPT system's load, accounting for potential additional circuits and aiming to minimize power consumption due to wireless data transmission. However, actual power consumption may vary once the load is designed and implemented.

The power transfer efficiency (PTE) is around 10% at a 20 cm distance between coils [27], though some systems have achieved up to 35% PTE [28]. The required transmitting power can be calculated using Equation 3.1.

$$P_{t,dBm} = 10log\left(\frac{P_L}{\eta_{rec}\eta_{pow}\eta_{link} \cdot 1\ \mathrm{mW}}\right) \tag{3.1}$$

To power the load of the WPT system, the minimum transmitting power required is 16 dBm (40 mW). This calculation assumes an estimated 80% efficiency, which is a typical and estimated value for both the rectifier (η_{rec}) and the power management block (η_{pow}), and a starting point of 50% power transfer efficiency (PTE, η_{link}) due to the highest reported value in [28] being approximately 35% and the potential improvement of the PTE to 50% in the future. $P_{t,dBm}$ represents the estimated total transmitted power needed to deliver adequate power to the receiver, not the input power set at the transmission side of the WPT system in dBm.

The receiver shall provide a stable output voltage of 1.1 V for the recording and digital signal processing (DSP) and 3.3 V for the stimulation load.
In collaboration with the DSP designer of the load of the WPT system, it is determined that an output voltage of 1.1 V is required for the DSP and the recording part, while 3.3 V is required for the stimulation part.

In Table 3.5, a short list of recommended and desired specifications are listed.

Table 3.5: Some additional specifications for the WPT system.

Additional specifications	
Recommended specifications	
1	The WPT system should provide real-time measurement of the received power of each receiver to monitor its power transfer efficiency to ensure optimal operation.
2	The WPT system should have an adaptive impedance matching when impedance changes.
3	The WPT system should have a monitoring system that measures power outages and system failures in the Nat-B lab and can autonomously activate the backup power source to prevent interruptions in lab experiments.
4	The WPT system should be designed for long-term cost saving.
Desired specifications	
1	The WPT system could be scalable to different room sizes due to the increase of the number of group-housed mice.
2	The WPT system could be compatible with different mice and rat models in terms of sizes and weights, allowing for versatility and flexibility in analysis of spontaneous behaviour.
3	The WPT system could be designed modularly, allowing for an easy replacement or upgrade of components.
4	The WPT system could contain a communication module to be able to transmit and receive.
5	The WPT system could have a secure and reliable communication protocol for data transmission between the headstage and the external device.

In investigating the PTE of headstages in various scenarios, particularly those involving close proximity between mice, using a larger number of mice is crucial. This is because more mice increase the likelihood of interactions within the environment, which can help identify areas of insufficient power, or ”dead zones” for the headstage.

4

Wireless power transfer mechanisms

Wireless power transfer (WPT) is used in applications like mobile device charging, biomedical implants, and electric vehicles, with power needs ranging from microwatts to kilowatts. A typical WPT system includes a power source, transmitter, receiver, and load. The transmitter converts power into an electric or magnetic field, which the receiver converts back to direct current (DC) for the load.

WPT methods are classified into near-field and far-field systems. Near-field WPT, for short distances (millimeters to meters), uses non-radiative methods like capacitive, inductive, or acoustic coupling. Far-field WPT, for longer distances, uses radiative methods like microwaves. Near-field WPT is more efficient for short ranges, while far-field WPT covers longer distances with lower efficiency. Safety in WPT systems is evaluated using Specific Absorption Rate (SAR), measuring RF energy absorbed by tissue in watts per kilogram (W/kg). SAR values for mice in small cages range from 0.01 to 4.2 W/kg, as per the International Commission on Non-ionizing Radiation Protection (ICNRP) [29]. SAR assesses potential health effects of electromagnetic radiation, with concerns about long-term tissue heating and damage. Hence, WPT systems must adhere to SAR limits for safety.

Near-field WPT is preferred for its high efficiency over short distances and relative safety. Far-field WPT can produce high electromagnetic interference (EMI) and exceed SAR limits due to higher tissue absorption at gigahertz frequencies. Optical WPT, while free from EMI issues, require solar cells, which may have size and weight constraints for a mouse.

4.1. Capacitive coupling

Capacitive coupling, also known as capacitive power transfer (CPT), uses capacitors to transfer electrical power wirelessly. It involves four conductive plates separated by a dielectric material on both the primary and secondary sides of the WPT system, essential for completing the current loop [30]. CPT is commonly used in subcutaneous implants, as shown in Figure 4.1.

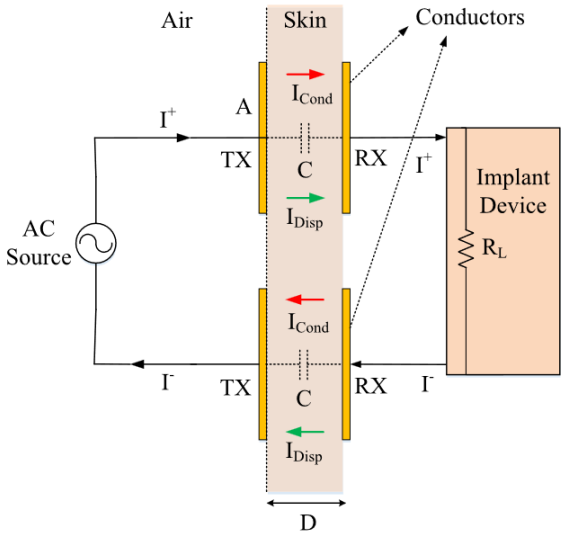


Figure 4.1: Capacitive coupling for subcutaneous implants [30].

In a CPT system, conductors are positioned on both sides of the skin. When a time-varying voltage is applied, displacement current occurs, changing the electric field between the capacitor plates and inducing a varying electric flux. To optimize PTE in CPT systems, the displacement current can be increased by enhancing the area of the capacitive plates or increasing the operating frequency. However, larger plate areas and higher voltages also increase conduction currents in tissues, leading to tissue losses. Strategies to minimize tissue losses include increasing the distance between conductors, decreasing the plate area, and adjusting the source voltage amplitude. Each approach involves trade-offs between improving displacement current and minimizing conduction current, requiring careful optimization to maximize PTE while minimizing tissue losses.

CPT in WPT systems offers several advantages listed below.

1. **Simple structure:** CPT utilizes only four thin plates, resulting in a lightweight and compact design, ideal for applications requiring small form factors, like IMDs.
2. **Localized electric fields:** the electric fields are confined to the capacitor plates, improving EMI performance by reducing potential interference with nearby electronics.
3. **Minimal Eddy current losses:** CPT uses electric fields instead of magnetic fields, avoiding energy losses from eddy currents typical in inductive coupling systems.

Disadvantages are listed as follows:

1. **Limited coupling capacitance:** the coupling capacitance dependents on the size and the distance between the plates. Increasing the distance or reducing the plate size decreases coupling capacitance, hence, decreased PTE.
2. **Increased voltage/frequency requirements:** greater distances may require higher voltage or frequency to compensate for the weaker electric field, imposing strict requirements on power management components and adherence to safety guidelines.
3. **Tissue heating:** balancing plate area, distance, and source voltage is crucial to maximize displacement current and minimize conduction current, avoiding tissue heating.

4.2. Ultrasonic power transfer

Ultrasonic power transfer (UPT) uses ultrasonic waves to transmit power, making it particularly suited for biomedical implants. The system includes two piezoelectric transducers: an external transmitter attached to the skin or tissue and an implanted receiver, shown in Figure 4.2.

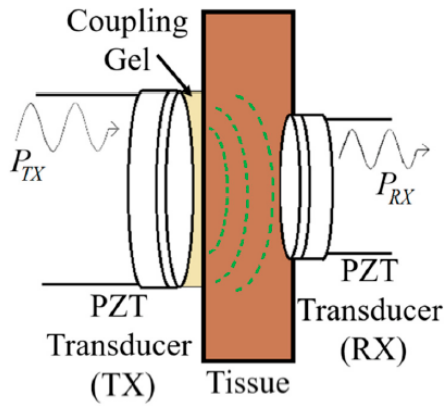


Figure 4.2: Ultrasonic power transfer for subcutaneous implants [31].

The transmitter generates an AC-signal that causes the piezoelectric crystal of the transmitter to vibrate, resulting from the inverse piezoelectric effect, creating ultrasonic waves that travel through tissue to the receiver. The receiver then converts these waves back into electrical energy to power the implant. UPT operates within a frequency range of 200 kHz to 2.1 MHz and benefits from high PTE due to the focused directionality of the ultrasonic waves [31]. The design of the transducers and their resonance frequencies take into account the concept of the Rayleigh distance, which is further explained in [31].

UPT in WPT systems offers several advantages listed below.

1. **Enhanced PTE with direct line of sight:** decreasing the distance between the source and the target reduces the number of obstacles that can interfere the ultrasonic waves, minimizing the reflections and diffractions, thereby reducing power losses.
2. **Minimized EMI compared to electromagnetic field:** electromagnetic fields are not used as energy carrier, ensuring safety for humans and animals.
3. **Versatility:** ultrasonic waves are versatile, able to travel through solids, liquids, and gases, making them compatible with various materials and suitable for diverse environments and applications.

Limitations are listed as follows:

1. **Distance limitation:** ultrasonic waves experience reduced PTE due to the inverse-square law and significant attenuation when encountering obstacles, as they propagate in a straight line, when in the far-field [31].
2. **Impedance mismatch:** impedance matching between the transducer material and the acoustic impedance of the medium is crucial. When UPT uses air as the medium, its low acoustic impedance (0.0004 MRayl) results in reflections and diffractions at the air-transducer interface, reducing PTE. The air's acoustic impedance is considerably lower than that of soft tissues (1.3-1.7 MRayl) [32].
3. **Energy losses due to absorption and environmental sensitivity:** the absorption coefficient of ultrasonic waves in air varies depending on the frequency range and environmental conditions such as humidity, pressure, and temperature [33].
4. **High PTE limited to one direction:** areas outside the direct line of sight of the receiver will have lower PTE, causing a non-uniform distribution of ultrasonic energy coverage.

4.3. Inductive coupling

Inductive Power Transfer (IPT) uses Faraday's and Ampere's laws, represented by Equations 2.4 and 4.1, respectively.

$$\oint_{loop} \vec{B} \cdot d\vec{r} = \mu_0 I_{enclosed} \tag{4.1}$$

$\oint_{loop}$ denotes the line integral around the closed loop, $\vec{B} \cdot d\vec{r}$ represents the inner product of the magnetic field and an infinitesimal element of the loop path, μ_0 is the permeability of free space, which is $4\pi \cdot 10^{-7}$ $\frac{N}{A^2}$ and $I_{enclosed}$ is the total current flowing through any surface bounded by the given loop. Ampere's law states that a conductor carrying a current generates a magnetic field around it. The direction of the magnetic field can be determined using the right-hand rule based on the direction of the current.

IPT employs TX and RX coils to transfer power through magnetic fields, illustrated in Figure 4.3.

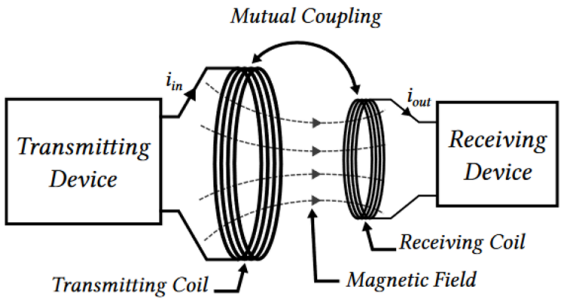


Figure 4.3: Generalized IPT link [34].

The TX coil generates a changing magnetic field when a time-varying current passes through it, inducing a voltage in the RX coil aligned with it. Efficiency is affected by the distance between the source and the target and increases complexity with multiple coils. Traditional IPT operates over short distances, while resonant IPT improves performance over longer distances [34], [35]. Resonant IPT, or RIPT, employs capacitors to enhance efficiency and can transmit over several meters. Different configurations optimize for different load requirements, illustrated in Figures 4.4 to 4.7.

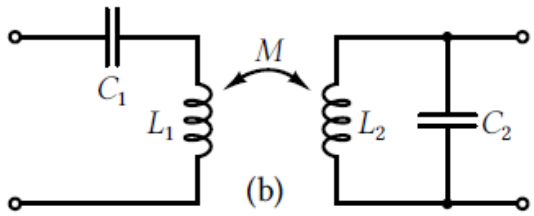


Figure 4.4: Series-parallel (SP) structure [34].

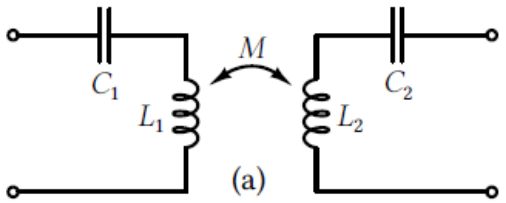


Figure 4.5: Series-series (SS) structure [34].

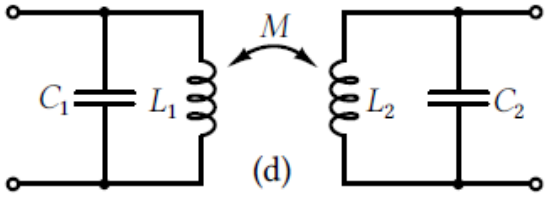


Figure 4.6: Parallel-Parallel (PP) structure [34].

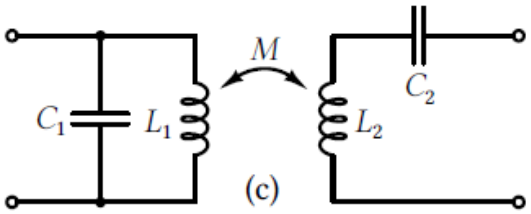


Figure 4.7: Parallel-series (PS) structure [34].

Each coil in the system is paired with a capacitor to form a resonant tank on both the primary and secondary sides of the link. The choice of the configuration determines whether a voltage source or a

current source is connected to the primary side of the link, depending on the desired input matching. For instance, in the SS and SP configurations, a voltage source is utilized, whereas the PP and PS configurations employ a current source for well-established input matching [34].

To optimize PTE, capacitors are used in different ways depending on the load requirements. A capacitor in series with the RX coil is used for loads that require high current, while a capacitor in parallel with the RX coil is preferred for low-power loads [34]. In RIPT, both coils are tuned to the same resonance frequency, unlike traditional IPT where mutual induction is the main factor. This tuning ensures maximum PTE in RIPT.

RIPT achieves maximum efficiency when coils are tuned to the same resonance frequency. Adding capacitors on both sides of an IPT system maximizes PTE, reducing energy losses during transfer.

The advantages are listed below.

1. **Implementation with various coil configurations:** using multiple coils and configurations can extend the transmission distance while keeping the PTE constant.
2. **Safety for humans and animals:** IPT typically operates within the kHz to MHz frequency ranges, adhering to safety guidelines outlined by the ICNRP.
3. **Operational in various conditions:** IPT is resilient to environmental factors like temperature changes, moisture, and dust, making it suitable for diverse operating conditions.

The challenges are listed below.

1. **High PTE limited to a few centimeters:** increasing the transmission distance decreases PTE, because the magnetic field may not reach the receiving coil, requiring a stronger magnetic field to reach it.
2. **Sensitivity to misalignments:** IPT necessitates aligned TX and RX coils to maintain optimal performance. Misalignment, such as horizontal misalignment, results in decreased PTE.
3. **Susceptible to EMI** inductive links may suffer from EMI caused by nearby metal objects or electronic devices. This interference can distort or divert the magnetic field, leading to a decrease in the coupling coefficient and, thus, a reduction in PTE.

4.4. The link selection for the targeted application

The appropriate WPT method is chosen based on factors like transfer distance, safety, and PTE. IPT and UPT are generally considered safe for humans and animals. However, for longer distances (in the meter range) and wider energy coverage, IPT becomes the preferred choice. This is because IPT can utilize resonant structures like RIPT to extend the WPT range to larger areas, potentially covering areas of 5 by 5 meters or even bigger.

While UPT and CPT offer the advantage of minimized EMI, careful design considerations can mitigate this issue in IPT and RIPT systems. Therefore, RIPT emerges as the preferred WPT mechanism for the targeted application.

5

State-of-the-art of WPT systems

Exploring and analyzing state-of-the-art WPT systems tailored to homecages will provide insights and guidance for the high-level design approach applicable to the Nat-B lab for freely moving animals.

5.1. WPT system developments and issues

To assess the limitations of different WPT system designs, a qualitative table (5.1) is provided. Appendix A.1 details the symbols and their corresponding assessments. This literature review focuses on research papers investigating transmitter (TX) and receiver (RX) coil placements, categorized as underneath or encircling configurations. Seven papers published between 2012 and 2023 explore the underneath configuration, while a single recent paper examines the encircling configuration. This selection allows for comparative analysis.

Table 5.1: Qualitative comparison with different research papers.

	Selected research papers							
Parameters	[36]	[37]	[38]	[23]	[39]	[40]	[41]	[42]
Year	2012	2014	2014	2015	2016	2022	2023	2023
Cage size (3 rodents)	- -	+ +	- -	- -	- -	-	- -	- -
PTE at 3 cm	+ +	+	+	+	+ +	+	+ +	+
Transmission range	- -	+	+ +	- -	+ +	- -	+	+
Angular robustness	- -	- -	-	- -	+	+	+	+
Lateral robustness	-	+	+	+	+	+	+	+ +
Vertical robustness	- -	-	+ +	- -	+ +	- -	+	+ +
Complexity	-	- -	+ +	-	+ +	+	+	+ +
Safety features	- -	- -	- -	- -	- -	- -	- -	- -

5.1.1. WPT systems based on power control loop with complex circuitry

Early WPT systems used large TX coils under homecages, leading to a reduced self-resonance frequency (SRF) and lower system efficiency. To address this, a novel configuration with four TX coils and Hall-effect sensors in study [36] was proposed to track the mouse movement, as depicted in Figure 5.1.

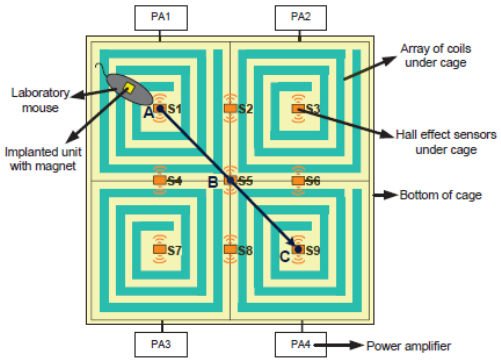


Figure 5.1: The TX-RX placement shown in [36].

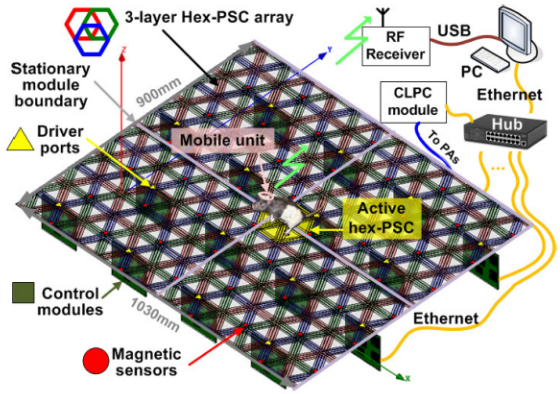


Figure 5.2: The TX-RX placement shown in [37].

However, this setup had power delivery issues in the form of blank spots at the edges and boundaries between the TX coils. Modifications were made to the closed-loop power control (CLPC) to eliminate these blank spots, which was adopted in studies [23] and [37].

The latter study used sixteen control modules driving three power amplifiers for hexagonal power coupling surfaces (hex-PCS), eliminating blank spots but adding complexity due to numerous components for covering a large area (0.9 by 1 meters). Despite improvements, issues with power levels persisted due to strong coupling between TX and RX coils. When a mouse moves to a specific hex-PCS, a 3-coil or 4-coil link is established for high PTE. However, operational issues were identified: at minimum power amplifier (PA) levels, the rectified voltage V_{rec}, should decrease but remains higher than expected due to strong coupling between TX and RX coils. At maximum PA levels, V_{rec} is lower than expected, indicating insufficient power for the headstage and suggesting the presence of blank spots. Angular and vertical misalignments were not considered, and a supercapacitor was used to account for these misalignments temporarily, which might not provide sufficient power for the mouse's electronics.

An alternative configuration in study [23] uses X and Y rails with a small powering coil, offering a simpler solution for mouse localization, shown in Figure 5.3 .

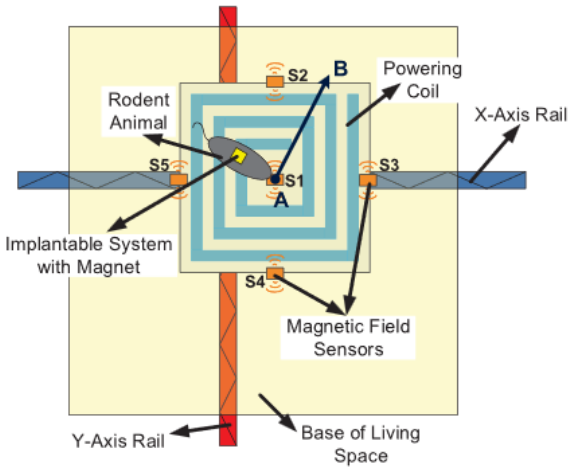


Figure 5.3: Top-view servo-controlled WPT system from [43] used in [23].

It faced delays in initial localization and challenges in expanding the coverage area. To counteract this delay, the time required to detect the highest magnetic field strength using magnetic sensors needs to be minimized. One potential solution is to increase the size of the permanent magnet (PM), although this is not desired for the targeted application. Moreover, The design was less robust against angular and vertical misalignments. However, the research papers mentioned earlier propose CLPC that

incorporate control circuits to maintain constant power levels and achieve uniform power distribution. Nonetheless, these efforts enhance the design's complexity, particularly in study [37].

5.1.2. WPT systems based on natural automatic power localization

A potential solution to overcome challenges with complex circuitry in CLPC systems is natural automatic power localization. This approach, explored in studies [38], [39], and [41], eliminates the need for intricate detection and control mechanisms, making it suitable for extending homecage spaces to support multiple receivers.

In [38] and [39], the conceptual representations of the configurations are similar. The study in [39] focuses on enhancing uniform power distribution, while the other study, [38], places more emphasis on the potential to support multiple receivers. The conceptual representation of this configuration is depicted in Figure 5.4.

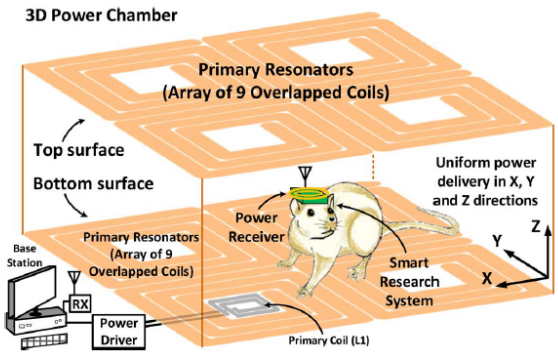


Figure 5.4: The TX-RX placement shown in [39].

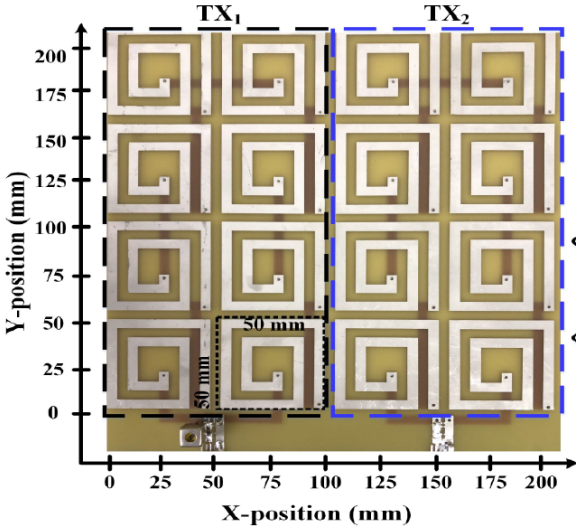


Figure 5.5: The TX-RX placement shown in [41].

Both of these research papers feature a conceptual TX configuration that involves a multicoil array, with the primary resonators arranged in parallel. The setup, illustrated in Figure 5.4, enhances uniform power distribution in X-, Y- and Z-directions and can power electronics even when a mouse stands up, improving over previous designs.

While [36] has mentioned that the mouse is usually on their four feet, measurement results from [37] demonstrated that there was a drop in V_{rec} at the maximum PA level, which could be that the mouse stood up or orientated the headstage at an angle of 90°. In addition to angular misalignment, [38] from 2014 claims robustness against this type of misalignments, although the specific TX placement's simulation and measurement results do not validate the claim. In contrast, [39] from 2016 presented the simulation and measurement results that account for angular misalignments, showing that the power can be transferred up to 80°, a significant advancement over research papers employing CLPC with active detection and control mechanisms.

The study described in [41] uses a unique magnetic field concept with two parallel TX coils carrying opposing currents. This setup enhances magnetic field strength and boosts PTE. The system features two multicoil arrays powered by separate transmitters, differing from the single transmitter configurations of other setups.

Simulation results indicate a consistent PTE above 50%, significantly improving the overall WPT system efficiency. Real-time measurements confirm this PTE, though the actual maximum PTE is slightly lower than expected. The study also includes the SAR analysis, crucial for the WPT system design in animal studies, which is often absent in previous research, such as in studies [38] and [39]. This

detailed analysis highlights the potential of the TX-RX placement for optimizing PTE.

Despite its advantage of boosting the PTE, the TX-RX placement presented in [41] exhibits a decline in PTE with increased angular misalignment, reaching an angle of 90°. This aligns with observations in configurations such as [23] and [36], [37], where angular misalignment up to 90° fail to deliver power. Similarly, while [38] and [39] manage to supply power with angular misalignment up to 80°, they experience a power cutoff at 90°.

To address this, study [42] proposes an encircling configuration with outer coils generating magnetic fields at the homecage edges and inner coils covering the central area, illustrated in Figure 5.6. This design maintains power regardless of receiver position and orientation, even at 90° misalignment.

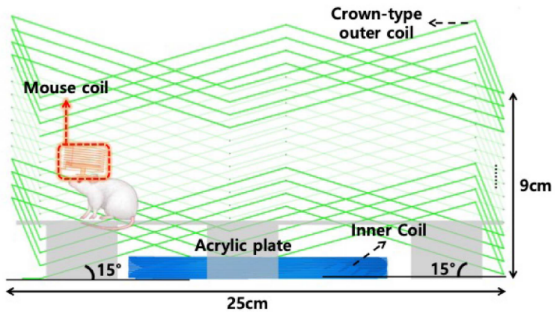


Figure 5.6: The TX-RX placement shown in [42].

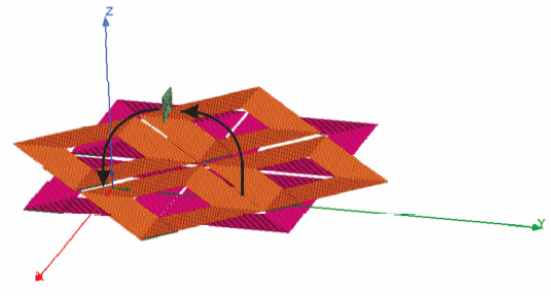


Figure 5.7: The TX-RX placement shown in [40].

The encircling configuration offers insensitivity to both the positioning and orientation of the receiver. For positioning insensitivity, the outer coil encircles the homecage, generating a magnetic field at the edges. In contrast, the inner coil generates a magnetic field within the central area of the homecage. These two coils are connected in parallel, allowing for uniform magnetic field coverage. This TX-RX placement ensures that the receiver can maintain power regardless of its position within the homecage.

The encircling configuration, featuring a crown-type outer coil as shown in Figure 5.6, addresses angular misalignments by maintaining power delivery even at 90° deviations. While the PTE might be slightly lower within the 0° to 80° range compared to some configurations, the key achievement is consistent power provision at 90°. Simulation results from [42] verify this capability.

Angular misalignment is also tackled by other encircling configurations like those in [44]. Additionally, study [40] proposes an underneath configuration with dynamically controlled current flow in star-shaped TX arrays, ensuring power delivery under varying receiver orientations. This method, applied through time multiplexing, has shown success in single receiver scenarios, achieving higher PTE at 90° orientations compared to traditional setups. Despite these advancements, comprehensive exploration of multiple-receiver scenarios is still needed.

5.1.3. Contribution to the targeted application

The existing WPT systems for homecages, with a focus on coil design placements, have been reviewed and compared. Table 5.1 assesses various parameters across selected studies. Most studies have focused on homecages with dimensions from 10 to 50 cm in terms of length, width and height, except for [37], which explored a 0.9 by 1 meter design. The intended application requires a minimum room size of 5 by 5 meters, posing significant design complexity and operational challenges. Upscaling the TX configuration of [37] for Nat-B lab coverage significantly increases design complexity, requiring intricate control mechanisms and active detection methods, which elevates the potential for operational failures.

The approach in [23] using X and Y rails is less viable for larger areas due to localization delays and lack of support for multiple receivers. Configurations with natural automatic power localization could facilitate multi-receiver support and larger area coverage without increasing design complexity. Studies like [38] and [39] show potential but face challenges with power distribution when applied to many re-

ceivers. The power supplied to each mouse's headstage diminishes as the number of mice increases. Increasing transmission power might address this, but it could lead to overcharging issues.

Using multiple receivers in an underneath CLPC configuration, as proposed in [37], can lead to uneven power distribution, requiring increased transmitted power and risking overcharging some receivers. This issue worsens as the number of receivers grows, potentially causing undercharging due to diminishing power delivery. This overcharging and undercharging are problematic since many research papers lack safety features, as indicated in Table 5.1. Furthermore, due to the large size of the Nat-B lab, not all the areas can supply sufficient power for mice moving in the X-, Y- and Z-directions, even with a potential suggested high-level design.

When placing TX units in the Nat-B lab for sufficient uniform magnetic field distribution, various factors like complexity and multi-receiver challenges must be considered. While increasing parallel primary resonators can extend coverage, it may lead to higher power losses [38], [39]. Encircling configurations can mitigate angular misalignments, and vertical misalignments can be addressed by adding a second TX placement on top. However, these solutions must not obstruct cameras' view. Hybrid configurations merging encircling and underneath setups could effectively cover large areas, maximizing PTE. Researching collaboration between these configurations can address issues like angular misalignments to achieve desired power distribution and efficiency across the Nat-B lab.

5.2. Conclusion

An overview of eight research papers was provided, highlighting their relationships and problem-solving approaches. The distinction between research papers utilizing CLPC with active detection and control mechanisms and those employing natural automatic power localization were made apparent. The latter approach was observed to simplify designs and reduce the risk of operational failures in WPT systems. Successful solutions to issues like angular misalignments, elimination of blank spots, and PTE enhancement were achieved with the natural automatic power localization approach, which outperformed conventional CLPC usage.

The qualitative table was used to identify a potential research gap, particularly within the context of the targeted application. The hybrid configuration, combining underneath and encircling high-level designs emerged as a promising approach to power the Nat-B lab while addressing design complexity. However, uniform power distribution, especially in the central area, remains a challenge in the Nat-B lab. A research gap involves investigating approaches to combine underneath and encircling configurations to create a sufficiently uniform power distribution in the Nat-B lab while overcoming issues like angular and vertical misalignments, and maximizing PTE close to edges and walls.

6

Potential high-level design approach

This chapter outlines a typical WPT system block diagram and the potential high-level design of the TX placement.

6.1. Block diagram of the WPT system

The block diagram of the targeted WPT system is shown in Figure 6.1.

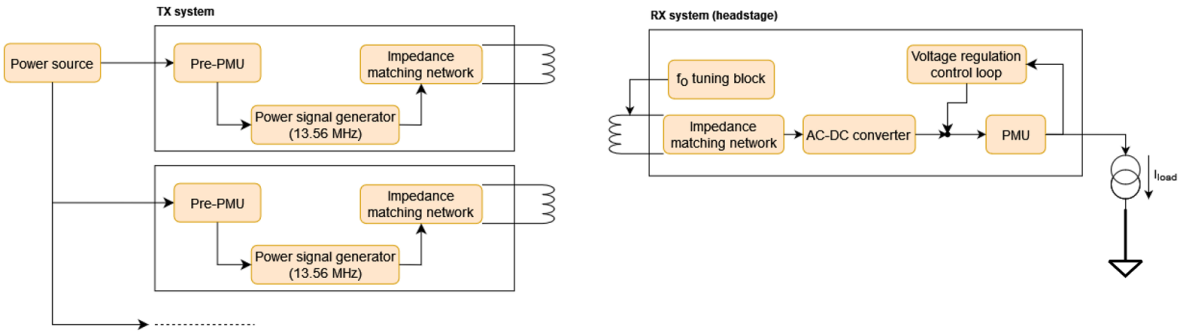


Figure 6.1: The WPT system block diagram for the Nat-B lab for multiple transmitters and one receiver.

Figure 6.1 illustrates two transmitters and a receiver within the TX and RX systems. However, the Nat-B lab requires more than two transmitters for sufficient uniform power distribution, connecting additional transmitters in parallel. TX coils transfer power to the RX coil through magnetic fields. Key components include:

pre-PMU: the pre-PMU (prior power management unit) protects against spikes and adjusts electrical parameters for the subsequent stages. It accommodates various voltage and current requirements for different transmitters. When using the mains (AC) as the power source, it might include an AC-DC converter and protective elements. The pre-PMU handles components specific to the power source, such as solar panels, batteries, grid power, energy storage systems, or dedicated DC power supply units. Given that multiple transmitters share a common power source, the exact type of power source for the Nat-B lab remains unknown.

Power signal generator: the power signal generator produces an alternating current (AC) to generate the magnetic field needed to excite the TX coil for power transfer with a resonance frequency, f_0 of 13.56 MHz, using a power oscillator or similar techniques.

Impedance matching network (IMN): the impedance matching network, IMN, minimizes energy losses and ensures high power transfer efficiency between the pre-PMU and the TX coil, and between the RX coil and the AC-DC converter. By minimizing the impedance mismatch between the source and the load, maximum power transfer is achieved in accordance with the maximum power transfer theorem, thereby mitigating energy reflections back to the source.

AC-DC converter: this component converts AC-signal from the impedance matching network into a DC-signal for further processing in the PMU for powering the load of the WPT system.

PMU: the PMU (power management unit) handles voltage conversion, possibly including LDOs and protection and monitoring functions for system robustness. A supercapacitor can be added as an energy reservoir to ensure continuous power supply during brief interruptions, such as when a mouse stands up.

Voltage regulation control loop (VRCL): the VRCL maintains PDL under variations in input voltage and load current. It measures a parameter related to the received power, compares it with the desired parameter, and adjusts the system to maintain constant output voltage, also known as post-regulation.

f_0 tuning block: the f_0 tuning block aligns the RX resonance frequency with that of the TX system to maintain PTE. This frequency match is vital, as highlighted by findings in [45], which demonstrate that a shift in resonance frequency, especially in strong coupling scenarios (for instance, at a distance of approximately 1 cm), can diminish PTE.

6.2. Potential hybrid configuration

A TX placement strategy was developed for the potential hybrid configuration.

6.2.1. Considerations

The pivotal considerations are listed below.

1. Minimization of X, Y and Z misalignment (lateral and vertical misalignments) is prioritized.
2. Adequate power should be supplied to blank spots.
3. Adequate power distribution is necessary along the walls and edges.
4. When mice stand up, the distance between the TX coils beneath the Nat-B lab and the headstage increases, as the nominal height of the mouse with respect to the ground is typically 4-6 cm.
5. Avoid switching off and on of certain areas to be able to save power in the TX system.
6. Take into account the interference between the receivers.

Natural automatic power localization and CLPC with active detection and control mechanisms are two techniques for ensuring continuous power throughout the Nat-B lab. The former technique aligns with the multi-receiver compatibility requirements and reduces design complexity, making it preferable for a room size of 5 by 6 meters, mentioned as the initial point in Section 3.2. CLPC's complexity, especially with active detection and control, could become overly intricate for such dimensions.

Key parameters for a robust WPT system include PTE, PDL, and misalignments (angular, lateral, and vertical), crucial for ensuring an uninterrupted power supply due to mice's behavior. Moreover, adequate power distribution along the edges, walls, and the midpoint of the Nat-B lab is vital. Initially, mice tend to explore at the edges and along the walls in an open-field environment, then gradually move to the central area, highlighting the importance of power distribution along walls and edges [46].

While mice typically move on all four feet [36], their head-to-ground distance ranges from 4 to 6 cm [39], [41]. When they stand on their hind legs, this distance increases, although a precise maximum distance has not been documented. However, based on a nominal range of 4 to 6 cm and insights from [37], an estimated maximum distance of around 12 cm can be inferred. This information is crucial

for determining the necessary height to encircle the entire lab room effectively.

To conserve power in the underneath configuration, selectively activating TX areas when mice are present can be effective, but it becomes complex with multiple receivers, like in scenarios with multiple mice. Precise tracking and decision-making for each mouse's TX area activation would lead to a complicated design. Therefore, it is advisable to keep all TX areas activated for continuous power distribution. Additionally, interference between receivers should be addressed as it degrades PTE, as seen in [38].

6.2.2. Mouse's headstage

Previous homecage designs have not directly tackled interference between mice and their receivers, but solutions exist. One method adjusts resonance frequencies to prevent overlap when receivers are close to each other. Sensors like ultrasonic sensors detect proximity and trigger frequency adjustments, temporarily altering a receiver's frequency until the other mouse moves away. However, this may complicate the design as it requires a decision sub-block for scenario detection within the existing WPT block diagram, illustrated in Figure 6.1.

An alternative solution to reduce interference between receivers is altering the 3D design of the headstage. Using a spherical 3D headstage, as illustrated in Figures 6.2 and 6.3, aims to minimize interference through its shape and structure, presenting an alternative to frequency tuning.

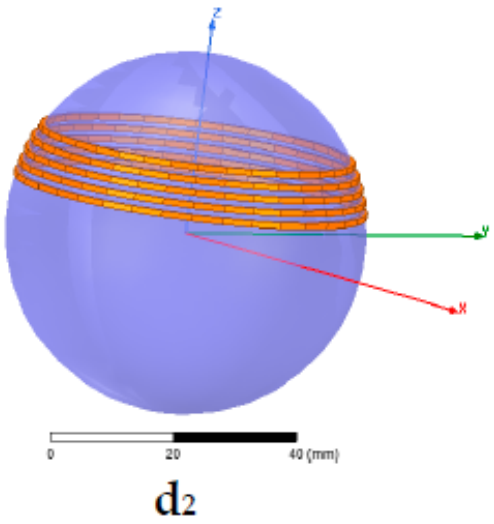


Figure 6.2: RX coil above the spherical design [47].

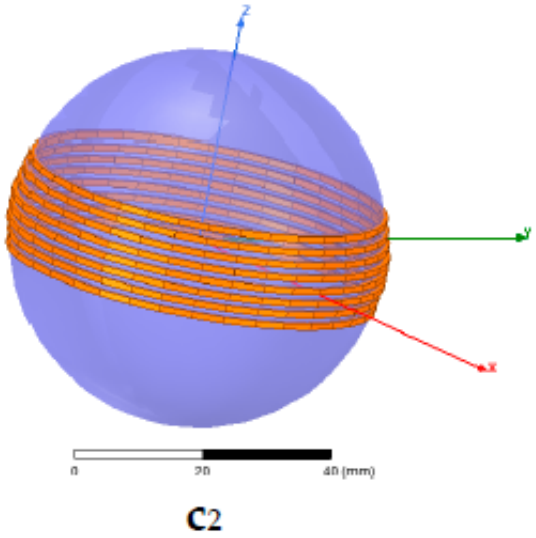


Figure 6.3: RX coil in the middle of the spherical design [47].

Incorporating designs from Figures 6.2 and 6.3 helps mitigate interference. For instance, using Figure 6.2 for 5 mice and Figure 6.3 for 6 mice minimizes interference by varying magnetic field orientations. However, the size and weight of the 3D design should be carefully considered to minimize stress on the mice. A cylinder shape is chosen for the headstage due to its simplicity, and the design in [41], as shown in Figure 6.4, serves as a high PTE reference, as demonstrated in that study.
To enhance interference avoidance, a slab-shaped object below the encircling 'wires' of the headstage can be utilized. Additionally, layers emitting high-pitched sounds upon collision can be added to each side of this shape. Mice are sensitive to such sounds, prompting them to move apart, maintaining a safe distance between headstages. While promising, the effectiveness of these methods in minimizing interference remains to be fully determined.

6.2.3. The TX Placement of the hybrid configuration

To aid our examination of how the magnetic field might behave in the Nat-B lab, a schematic depiction of the lab room is provided in Figure 6.5.

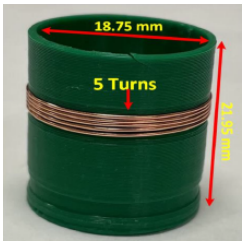


Figure 6.4: Headstage used in [41].

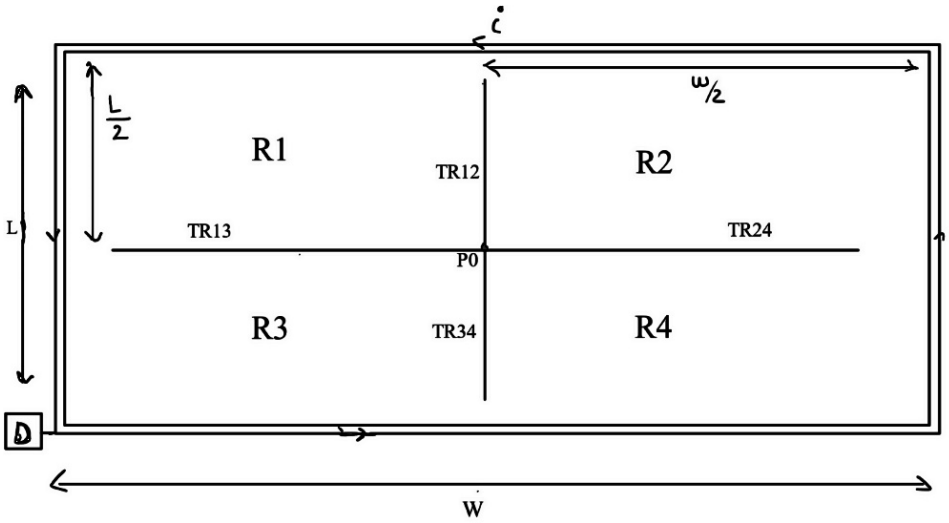


Figure 6.5: Top view of the lab room with global layout with W = 6 m and L = 5 m (Not scaled).

In this figure, the Nat-B lab is segmented into four regions (R1, R2, R3, R4) for effective transmitter placement. Boundaries between regions are labeled TRx, for example, TR12 between regions 1 and 2. P0 is the midpoint, and D represents the AC-current driver block. An outer rectangular loop with N turns encircles the room, and an inner rectangular loop represents the room's dimensions. A potential hybrid configuration is suggested, illustrated in Figure 6.6.

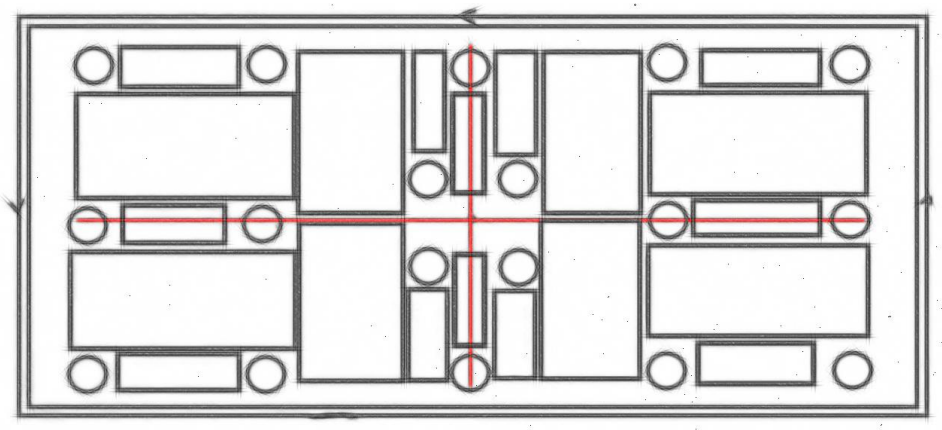


Figure 6.6: Suggested hybrid configuration.

Two common pole shapes, square and circular, are considered. Study [48] shows that square poles transmit more power under significant misalignment, whereas circular poles are better for well-aligned headstage receivers, yielding higher power compared to well-aligned receivers with a square pole. Since minimizing X and Y misalignments are crucial, the circular pole is chosen, represented by circles in Figure 6.6.

To minimize vertical misalignment and reduce the number of transmitters needed, circular TX poles were positioned in areas where mice are likely to stand up based on their behavior. Mice frequently stand on their hind legs during exploration for a better view of their surroundings or in response to dominant mice. These areas often include walls, edges, and central areas. Informed by these tendencies and study [46], a predictive approach was employed to identify these placement zones. This method necessitates iterative testing to refine the TX placement within the hybrid configuration.

This hybrid configuration consists of multiple rectangular areas and TX circular poles, each of which has specific magnetic field interactions. To facilitate effective description, the rectangular areas are assigned distinct names, as illustrated in Figure 6.7.

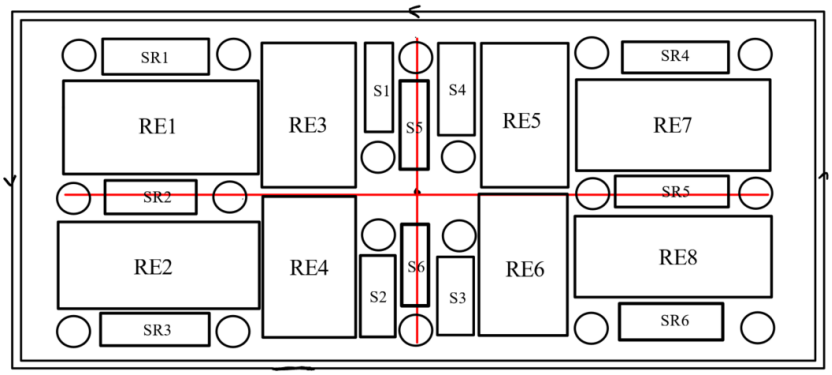


Figure 6.7: Suggested hybrid configuration with annotation for description.

In this figure, five different sizes of rectangular areas with equal area size are shown:

1. SR1 to SR6
2. RE1, RE2, RE7 and RE8
3. RE3, RE4, RE5 and RE6
4. S1 to S4
5. S5 and S6

While the initial sketch, shown in Figure 6.7, may suggest that for example, areas SR2 and SR3 have unequal sizes due to imperfect rendering of other elements, it is important to note that in reality, the intention is for both SR2 and SR3 to have equal area sizes. The inconsistency in the sketch arises from inaccuracies in representing certain components, particularly the placement of TX circular poles, causing the inconsistency of certain elements. This principle also applies to other areas such as S1 and S4, where equal area sizes are intended for implementation. The primary aim of the sketch is to provide a potential layout for the placement of transmitters.

6.2.4. Magnetic field interactions

The magnetic field interactions between the encircling and underneath configurations, between two rectangular areas, and between the TX circular poles and the rectangular area are depicted in Figure 6.8.

Only half of the hybrid configuration is shown as the other half is symmetrically similar. The design ensures sufficient power for the receiver by employing the magnetic concept of two conductors with currents flowing in opposite directions, resulting in additive magnetic fields. This principle, illustrated in Figure 6.9, is fundamental to the hybrid configuration. Additionally, the right-hand rule is used to establish current direction and prevent magnetic field cancellation, as shown in Figure 6.10. The coil design for the TX circular poles and rectangular areas must align with the indicated current direction for each component.

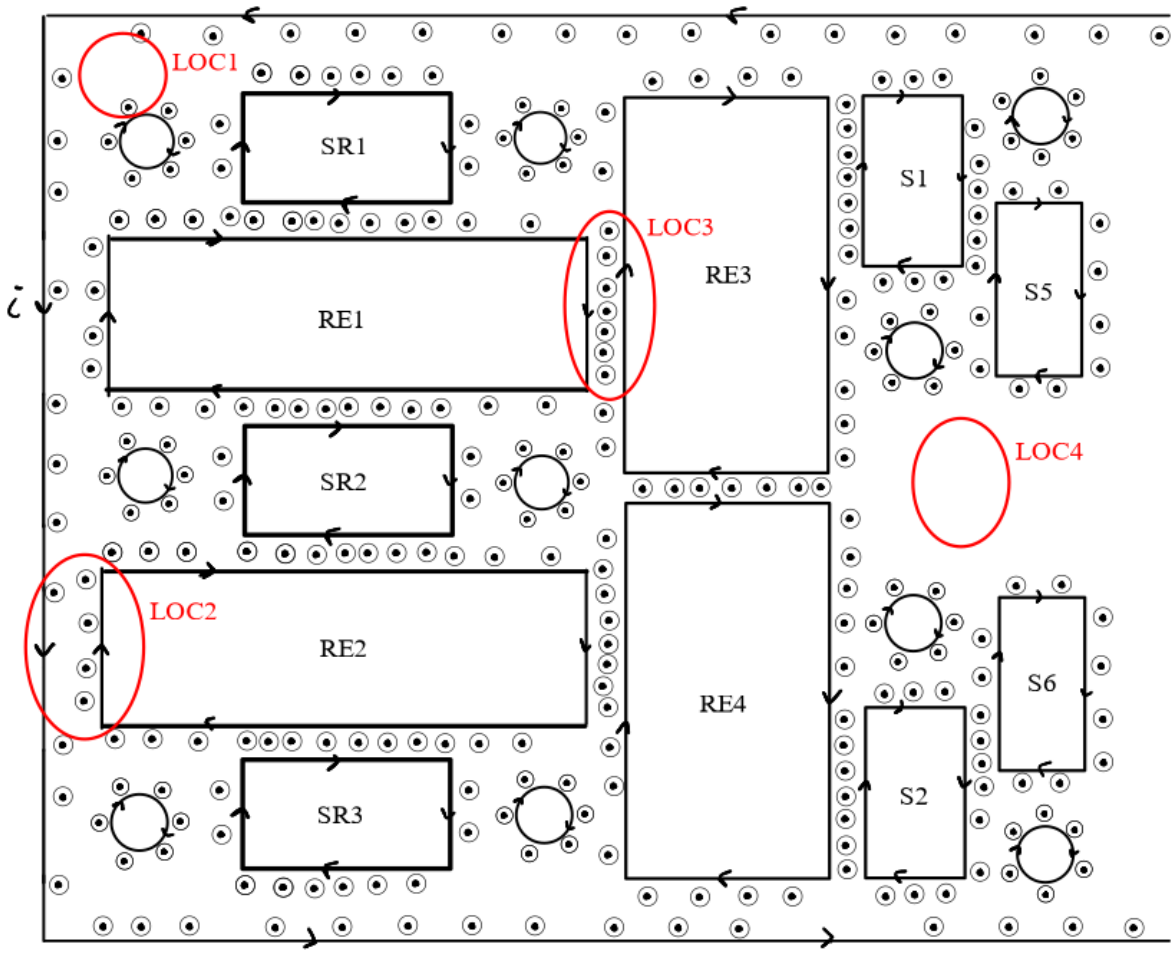


Figure 6.8: The left part of the hybrid configuration with magnetic fields coming out of the page.

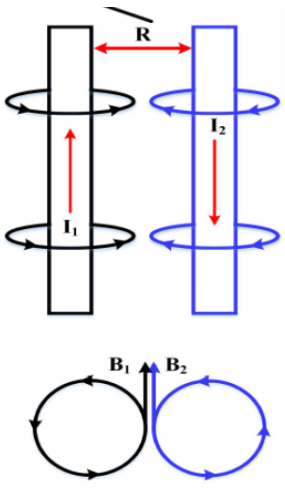


Figure 6.9: Magnetic field of two conductors with current in opposite direction [41].

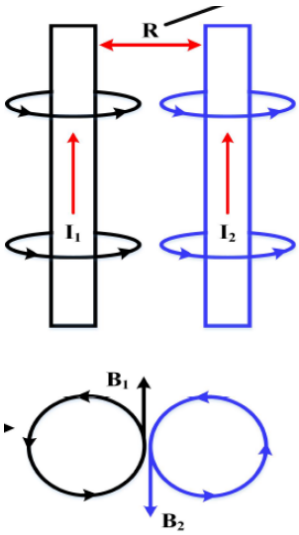


Figure 6.10: Magnetic field of two conductors with current in same direction [41].

Four specific locations, denoted as LOC1, LOC2, LOC3, and LOC4, require special attention in the Nat-B lab design, as shown in Figure 6.8.

LOC1: This location is the space between the encircling configuration and the TX circular pole. The TX circular pole is positioned at a certain distance to prevent overlapping magnetic fields that could increase stress levels in mice [49], because mice are sensitive to magnetic fields, impacting their natural activities. High current in the encircling configuration could magnify the overall magnetic field, hence the separation. If the magnetic field created through encircling is substantial, an overlap could potentially magnify the overall magnetic field in that specific region.

LOC2: The rectangular area is also positioned with a gap from the encircling configuration for similar reasons to LOC1, preventing magnetic field interference.

LOC3: This location involves the placement of rectangular areas RE1 and RE3 close together to minimize horizontal misalignments (X and Y). This arrangement ensures sufficient power delivery as mice move around, with the added magnetic field, illustrated by a row of circles with black points inside, directed out of the page according to the right-hand rule.

LOC4: LOC4 is located near the middle point of the Nat-B lab. Even though it might seem that no power can be delivered here, increasing the current of the TX circular poles in nearby areas (S1, S2, S5, and S6) could generate sufficient magnetic field to induce voltage at the receiver. Connecting S5 and S6 is not recommended as it might decrease PTE, thus simulations and tests are advised to ensure sufficient power supply at LOC4 without such connections.

The magnetic field interactions with the headstage receiver and the TX circular pole, as well as a cross-section view of the encircling configuration, are illustrated in Figures 6.11 and 6.12, respectively.

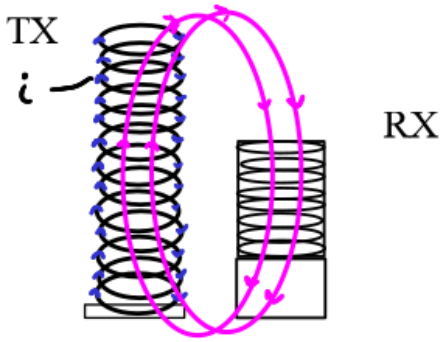


Figure 6.11: Interaction between the TX pole and the receiver.

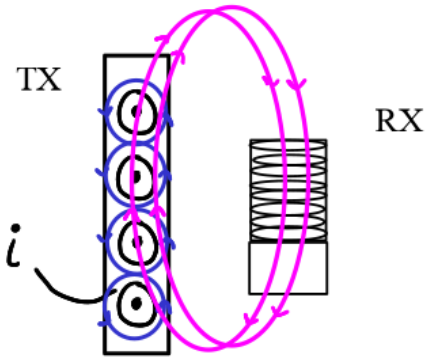


Figure 6.12: Left part of the cross-section view at LOC2 together with the receiver.

Both figures demonstrate that the generated magnetic field induces a voltage in the receiver. Figure 6.12 shows four turns of the encircling coils for illustration purposes. Additionally, even when the receiver moves up, it remains within the reach of the field lines, minimizing the impact of vertical misalignments. The magnetic field between the underneath configuration and the receiver, such as at the upper boundary of RE1, is shown in Figure 6.13.

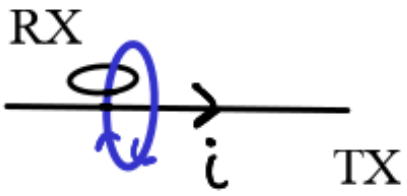


Figure 6.13: Magnetic field interaction between a part of the underneath configuration and the receiver.

Figure 6.13 shows the magnetic field (blue circular loop) directed towards the receiver (black circular loop) from beneath, providing power to the receiver's electronics. However, unlike Figures 6.11 and 6.12, this configuration does not effectively address vertical misalignments if the receiver moves up.

6.3. Main challenges

The hybrid configuration offers a potential solution for uniform power distribution in the Nat-B lab but presents several challenges. Key issues include determining the optimal current for the encircling wires, which is more complex in a larger setting compared to a homecage. Iterative testing across a range of currents is necessary to find the optimum magnetic field strength while avoiding overlaps with fields from TX circular poles and rectangular areas. Additionally, detailed mathematical analysis might be needed to estimate the required current and optimal distance between the encircling and underneath configurations to avoid excessive magnetic fields that could stress the mice.

A second challenge poses minimizing angular misalignments, particularly in the underneath and encircling configurations. While time multiplexing, as demonstrated in study [40], offers a solution for the underneath configuration, it decreases PTE at a receiver orientation of 90°. However, the suitability of this technique for the encircling configuration remains unproven. Further research is needed to explore alternative strategies that can enhance PTE at 90° orientations, suitable for both configurations.

Lastly, addressing vertical misalignments remains a challenge, particularly in areas like LOC3, as highlighted in Figure 6.8. While adding more TX circular poles could help, excessive numbers might lead to obstruction and inconvenience within the Nat-B lab. Hence, further research is needed to find effective solutions for vertical misalignments without significantly increasing the number of TX circular poles or exploring alternative approaches.

7

Conclusion

The research aimed to establish a potential blueprint for the high-level design of a WPT system intended for the Nat-B lab, simulating a naturalistic environment for group-housed rodents. The initial stage involved the selection of an energy harvester type, wherein wireless power transfer was chosen due to its adaptability in controlled power levels, its minimal disruption to the mice, and the elimination of physical contact (wires). Among WPT techniques, capacitive coupling, ultrasonic power transfer, and inductive coupling were considered. Resonant inductive coupling was eventually selected, thanks to its advantages in PTE at greater distances and its ability.

Following this, an extensive literature review was conducted on eight research papers on WPT systems for animal studies in homecages. Natural power automatic localization was favored over CLPC due to its simplicity and support for multiple receivers. A main research gap was identified: the integration of encircling and underneath configurations for sufficient uniform power distribution in the Nat-B lab.

Based on the research gap and literature review, a WPT system block diagram was given for the Nat-B lab. The preliminary layout design includes strategically positioned TX circular poles to address vertical misalignment where mice are likely to stand. Rectangular areas of various sizes supplement coverage where the magnetic field is lacking. The layout is completed by encircling the lab with 'wires' to generate magnetic fields along the walls and edges.

The suggested high-level design for wirelessly powering headstage electronics in the Nat-B lab marks an initial step but faces significant challenges. These include determining the optimal current for encircling wires, minimization of angular misalignments, enhancement of the PTE at 90° for both encircling and underneath configurations, and reducing vertical misalignments without increasing the number of TX circular poles.

II

Design of a voltage regulation control loop for a mouse's headstage

8

Introduction

8.1. Background

In Section 6.1, a high-level design of the potential wireless power transfer (WPT) system for the Nat-B lab was explained. This design incorporates the voltage regulation control loop (VRCL) block, which serves the purpose of maintaining a constant power delivered to the load (PDL) in the mouse's headstage, even when multiple headstages are added to the system, in the presence of potential horizontal misalignments within the Nat-B lab.

However, it is important to note that, due to the size of the Nat-B lab, at least 5 by 5 meters, achieving sufficient uniform power distribution across the entire space necessitates a significant number of transmitters. Consequently, the addition of more headstages might not drastically impact the reduction of received power per individual headstage as it still largely depends on the specific locations of the mice in the Nat-B lab. However, when a certain number of mice are in the same transmitter area, the receiver power per headstage would decrease.

Additionally, even with multiple transmitters, horizontal misalignments can persist, especially in regions where the magnetic fields do not overlap, creating dead zones. Figure 8.1 illustrates this scenario. Consequently, the received power, and thus the received voltage, is temporarily reduced. Therefore, post-regulation for the power management unit (PMU) is required to maintain the output voltage at the desired load voltage.

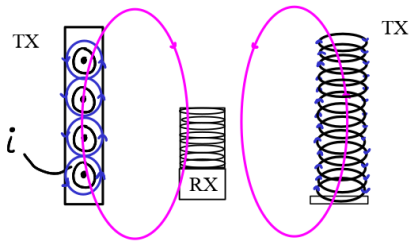


Figure 8.1: Mouse's headstage located between two non-overlapping magnetic fields potentially receiving insufficient power.

Given that the power link and the load have not been designed yet and a VRCL must be designed for post-regulation, the main research question arises: **how can a voltage regulation control loop (VRCL) be systematically designed and implemented for an unspecified PMU to achieve the desired load voltage?**

8.2. Thesis objectives

The goal of this part of the project is to design the VRCL block. The main objectives for this part of the project are listed below.

1. Conduct a literature review of the VRCL block.
2. Derive the relevant control specifications for the VRCL design.
3. Derive a plant model and use a control system technique to design the VRCL block.
4. Design the circuits for the VRCL block.
5. Design the non-ideal power converter to assess the performance of the VRCL block.
6. Acquire findings from the simulated VRCL block.

8.3. Organization of Part II

Part II of this report is organized as follows:

Chapter 9 provides the performed load analysis and the choices that have been made to be able to design the VRCL block without knowing the implementation of the PMU.

Chapter 10 provides a brief overview of the fundamentals of the switched-capacitor (SC) DC-DC converter, along with common regulation methods for SC-based DC-DC converters and potential limitations of the control loops, identified in the literature.

Chapter 11 introduces the design of an ideal SC-based DC-DC converter, a suggested mathematical model, drawing from the theory presented in Chapter 10 and a tailored control-system approach. It covers simulation results for the verification of the mathematical model.

Chapter 12 presents the implemented control loop and the non-ideal power converter with the design choices. Moreover, relevant simulation results are shown to evaluate the performance and compare them with the specifications, outlined in Chapter 11.

Chapter 13 concludes Part II by addressing the research question, mentioned in Section 8.1. It emphasizes the contribution of the thesis and outlines the future improvement possibilities.

9

Preliminary analysis

9.1. Load analysis

A load analysis has been conducted to comprehend the required specific load that should be connected to the PMU. The load components are indicated by the blue rectangles, illustrated in Figure 9.1.

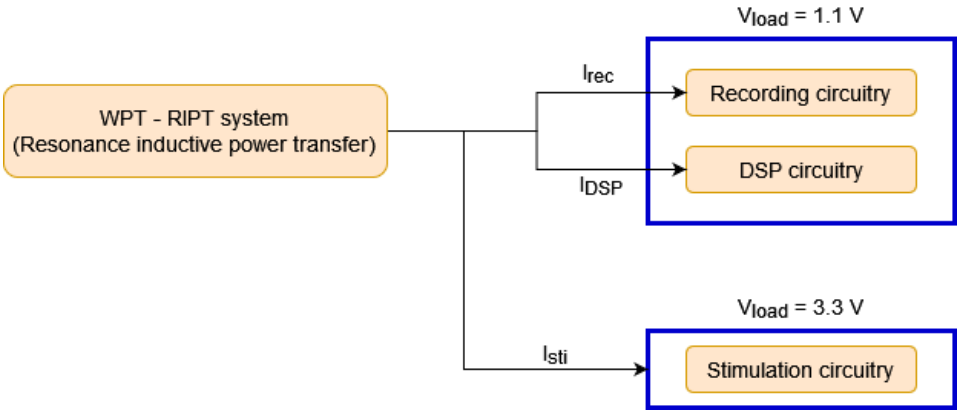


Figure 9.1: WPT system connected to the load components.

The load comprises three components: the recording, digital signal processing (DSP), and stimulation circuitry, which require output voltages (V_{load}) of 1.1 V for the former two components and 3.3 V for the latter, with output voltage tolerances of ±10%. The recording circuitry's load current is set to 5 mA, based on the retina project within the research department. The DSP's load current is fixed at 0.9 mA, determined in collaboration with the DSP designer. For the stimulation circuitry, referencing [50], the load current is set to 520 μA to better align with the targeted application, rather than using the retina project's 5 μA.

These components do not operate simultaneously, leading to varying load conditions as they switch between idle and active modes. While the magnitude of leakage current during idle mode is unknown, it is assumed to be 10 μA. Tables 9.1 and 9.2 summarize the load currents of the components in idle and active modes.

Table 9.1: General overview of the load currents in Recording and DSP with idle and/or active mode.

Load (V_{load} = +1.1 V)		Current per load		I_{rec} + I_{DSP}
DSP circuitry	**Recording circuitry**	**I_{DSP}**	**I_{rec}**	**I_{supply}**
Idle	Idle	10 μA	10 μA	20 μA
Idle	Active	10 μA	5 mA	5.01 mA
Active	Idle	0.9 mA	10 μA	0.91 mA
Active	Active	0.9 mA	5 mA	5.9 mA

Table 9.2: General overview of the load current of the programmable stimulation with processing circuit in idle and/or active mode.

Load (V_{load} = +3.3 V)	Current per load		$I_{stimulus}$ + $I_{circuit}$
Stimulation circuitry	**$I_{stimulus}$**	**$I_{circuit}$**	**I_{sti}**
Idle	0 μA	10 μA	10 μA
Active	1-500 μA	20 μA	21-520 μA

Table 9.1 shows the load current ranging from 20 μA to 5.9 mA. In Table 9.2, $I_{stimulus}$ is the programmable stimulation current (0 to 500 μA) applied to the mouse's brain [50], and $I_{circuit}$ is the current used by the stimulation driver. The load current ranges from 10 μA to 520 μA. Load conditions can vary with stimulus current adjustments and mouse movements in the Nat-B lab, necessitating a constant output voltage despite these changes.

9.2. PMU selection

9.2.1. Estimation of the input voltage of the PMU

The PMU, as the Device Under Test (DUT) for assessing control loop performance, faces design challenges due to the unknown input voltage from the undetermined power link. Estimating this input voltage can be guided by the literature on WPT systems for mice in homecages. While current resonance inductive power transfer (RIPT) systems are used in homecages, the intended application will be operated in the Nat-B lab. Table 9.3 summarizes the comparison of seven relevant research papers.

Table 9.3: General overview of 7 research paper to determine the input voltage of the PMU.

Parameters	**[44]**	**[37]**	**[27]**	**[40]**	**[51]**	**[52]**	**[53]**
Type of link	4-coil	3-coil/4-coil	4-coil	4-coil	4-coil	4-coil	4-coil
Operating frequency (MHz)	13.56	13.56	13.56	10	13.56	13.56	13.56
V_{rec} (V)	4.1	4	5	8	5	5	5
Homecage size (Length x Width)	46x24 cm^2	100x90 cm^2	46x24 cm^2	32x32 cm^2	46x24 cm^2	46x24 cm^2	40x20 cm^2
Powering distance (cm)	7	12	8 cm / 20 cm	4	7	8	7
PTE (%)	14%	6.2% / 5.6%	23.6% / 6.7%	18.20	14.9	20.6	2.4 - 3.4
CLPC	Yes	Yes	Yes	No	Yes	Yes	Yes

Seven research papers, aligned with the targeted application, except for the area size, indicate that the rectified voltage (V_{rec}) after the AC-DC converter is around 4 V or 5 V at 13.56 MHz. With output voltages of 1.1 V and 3.3 V, a step-down PMU topology is required. Considering the Nat-B lab's configuration, with mats covering the lab area (estimated at 100x90 cm^2), 4 V is chosen as the PMU input voltage.

Due to the mouse's constant movement and power variation, a multi-ratio PMU could be necessary. A multi-ratio PMU is a PMU that comprises multiple voltage conversation ratios (VCRs). However, if the closed-loop system ensures sufficient uniform power distribution, voltage variation may be minimal, a multi-ratio PMU might not be required. Since predecessor blocks are yet to be designed, a single-ratio PMU with a static input voltage of 4 V was initially selected.

9.2.2. Selection of the potential component(s) in the PMU

From the literature study, a DC-DC converter is typically required for voltage conversion in a power link. Some designs incorporate Low-Dropout voltage regulators (LDOs) to reduce ripple at the expense of increased PCB area and a reduced power efficiency.

While certain research papers employ a voltage regulator or a DC-DC converter solely for providing required output voltages to the load on PCB, the generation of these voltages must be integrated into 180 nm CMOS technology in the targeted application. The DC-DC converter can be designed to significantly reduce ripple at the output voltage. Consequently, an LDO might not be necessary. Besides, four types of step-down voltage converters are considered: transformer, LDO, inductive DC-DC converter, and SC-based DC-DC converter.

Due to the assessment of the control loop performance, a transformer might not be suitable, because the output voltage is regulated by adjusting the number of windings, which complicates the circuit design and is less straightforward.

An LDO saves area and space but is only efficient if $V_{out,LDO}$ is close to $V_{in,LDO}$, assuming equal input and output currents. However, in the targeted application, the use of an LDO would result in low efficiency due to the conversion of the 4 V input voltage to 3.3 V and 1.1 V output voltages, which the theoretically maximum efficiencies are 3.3/4 = 82.5% and 1.1/4 = 27.5%, respectively. Thus, the selection is narrowed down to an SC-based DC-DC converter and an inductive DC-DC converter.

Based on Chapter 3, the receiver will be integrated into CMOS technology, and its weight should be under 1 g when used with weanling mice in a Nat-B lab. While an inductive DC-DC converter might be suitable, the required inductor value is unknown. High inductor values often necessitate off-chip components, potentially exceeding the weight limit. Conversely, the SC-based DC-DC converter is fully integrable in CMOS technology, meeting size and weight constraints, thus becoming the preferred choice for the targeted application.

9.2.3. Selection of the potential high-level PMU arrangement

While the SC-based DC-DC converter with an input voltage of 4 V was selected, it is crucial to determine how the output voltages of 1.1 V and 3.3 V can be generated. Eight different potential high-level approaches are illustrated in Figures 9.2 through 9.9.

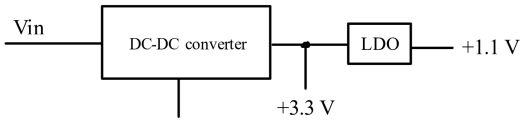


Figure 9.2: High-level PMU arrangement Option 1.

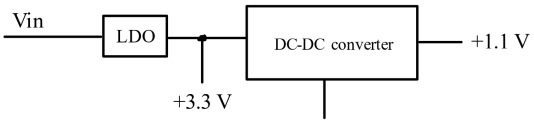


Figure 9.3: High-level PMU arrangement Option 2.

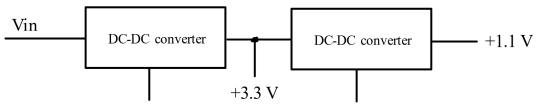


Figure 9.4: High-level PMU arrangement Option 3.

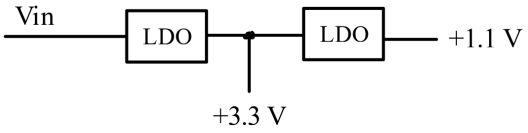


Figure 9.5: High-level PMU arrangement Option 4.

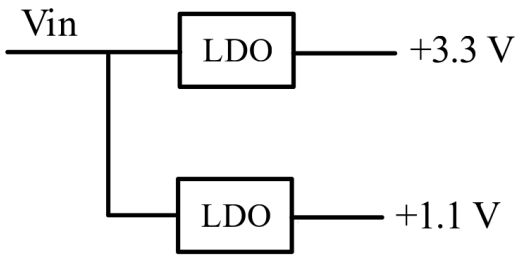


Figure 9.6: High-level PMU arrangement Option 5.

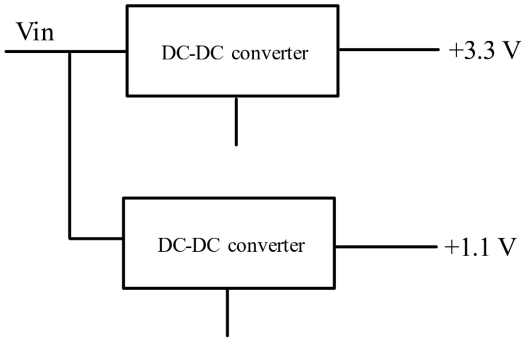


Figure 9.7: High-level PMU arrangement Option 6.

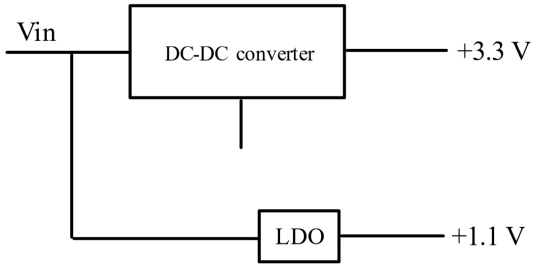


Figure 9.8: High-level PMU arrangement Option 7.

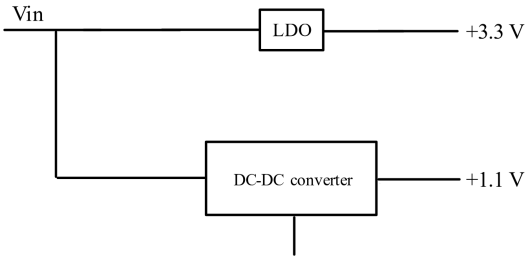


Figure 9.9: High-level PMU arrangement Option 8.

Ensuring a high overall efficiency of the WPT system, Options 1, 2, 4, 5, 7, and 8 using an LDO are insufficient due to the high power losses in the step-down voltage conversion. In contrast, Options 3 and 6, employing a DC-DC converter, exhibit higher efficiency for a V_{load} of 1.1 V and 3.3 V compared to the combination of a power converter and an LDO.

Option 6 independently generates V_{load}, whereas in Option 3, the second DC-DC converter depends on the first DC-DC converter, acting as an additional load. Another advantage of Option 6 is that the isolation of both outputs is better. This is recommended as the 1.1 V is used for neural recording and thus crosstalk might be mitigated. Therefore, Option 6 is preferred.

10

Literature study

10.1. Fundamentals of switched-capacitor DC-DC converters

10.1.1. Basic principle

The SC-based DC-DC converter is a switch-mode DC-DC converter that operates without using inductors, instead employing a specific number of flying capacitors and switches. During operation, these flying capacitors are charged and discharged between the input and output, forming a topology representing a discrete voltage conversion ratio (VCR). Common SC-based DC-DC converter topologies include Series-Parallel, Fibonacci, doubler, Dickson, and ladder topologies, as outlined in [54]. An example of a doubler topology is illustrated in Figure 10.1, and the switching phases are shown in Figure 10.2.

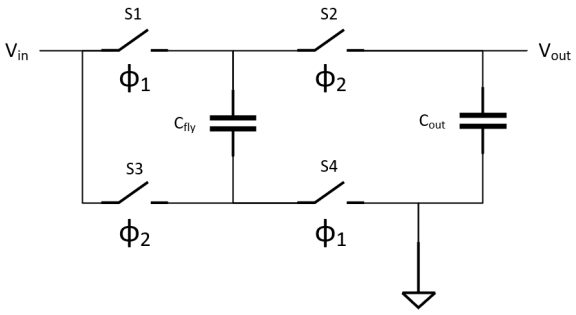


Figure 10.1: Doubler topology with M = 2.

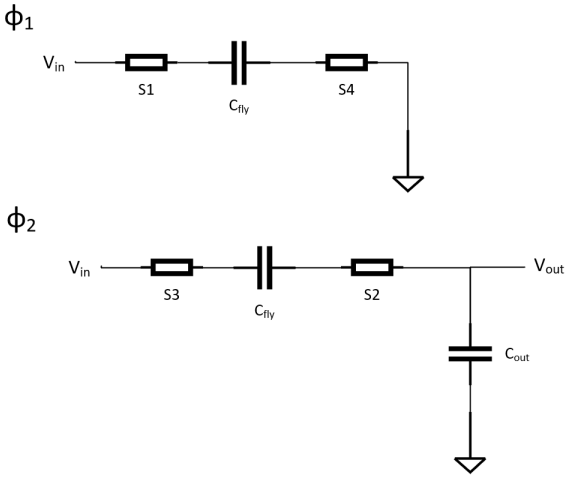


Figure 10.2: Doubler topology with two phases.

The basic principle of the doubler topology operates as follows: during clock phase ϕ_1, the flying capacitor (C_{fly}) is charged until it reaches V_{in}, when Switches S1 and S4 are closed. Subsequently, Switches S1 and S4 open, and Switches S2 and S3 close to discharge C_{fly} to the output capacitor. This process continues until the desired output voltage is achieved. While this configuration inherently represents a VCR of 2, it can be converted to a VCR of $\frac{1}{2}$ by swapping V_{in} and V_{out}, thereby reversing the working principle. Generally, this principle of swapping holds for all SC-based DC-DC converter topologies. A SC-based power converter is typically represented as an average model, as shown in Figure 10.3.

In this figure, M represents the VCR, $V_{out,nl}$ is the no-load output voltage, V_{out} is the output voltage after accounting for the output resistance, and R_{out} represents the average equivalent output resistance. This resistance is a result of the charging and discharging of the flying capacitors and the conduction

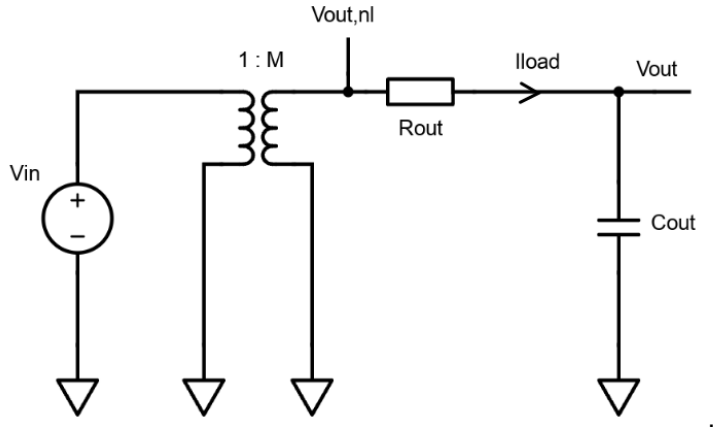


Figure 10.3: SC-based DC-DC converter average model [55].

losses of the switches. R_{out} can be further divided into the slow-switching limit (SSL) and fast-switching limit (FSL) regimes, as given by Equation 10.1 [55].

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{10.1}$$

In this equation, R_{SSL} represents the output resistance in the SSL regime, where the switches have sufficient time to charge and discharge the flying capacitors, and the on-resistances of the switches are neglected. On the other hand, R_{FSL} is the output resistance in the FSL regime, where flying capacitors do not have sufficient time to charge and discharge, and the on-resistances of the switches dominate. These output resistances can be described by Equations 10.2 and 10.3 along with Equations 10.4 and 10.5.

$$R_{SSL} = \frac{K_{SSL}}{f_{sw} C_{fly}} \tag{10.2}$$

$$R_{FSL} = K_{FSL} R_{\text{on}} \tag{10.3}$$

$$K_{SSL} = \sum_{i=1}^{n_c} \frac{a_{C,i}^2}{k_{C,i}} \tag{10.4}$$

$$K_{FSL} = \sum_{i=1}^{n_{swi}} \frac{a_{R,i}^2}{D_i} k_{R,i} \tag{10.5}$$

In the above equations, K_{SSL} and K_{FSL} are topology-dependent factors, n_c and n_{swi} represent the numbers of flying capacitors and switches, respectively. R_{on} is the on-resistance of all the switches in the ideal case. $k_{C,i}$ and $k_{R,i}$ are the proportionality factors of the flying capacitors and switches, respectively, used for calculating the on-resistance for each switch and capacitor value, which these values are proportional to the total on-resistance of the switch and flying capacitance, respectively. C_{fly} is the total flying capacitance, and D_i is the duty cycle of the i^{th} switch, typically 0.5. Additionally, $a_{R,i}$ and $a_{C,i}$ are the fractions of the output charge that flow through the i^{th} switch and flying capacitor, respectively, depending on the topology [55].

Equation 10.1 can be utilized for the design. However, it is crucial to note that this is an approximation, and the switching frequency should be optimized in the simulation. In addition to R_{out}, it can be plotted against the switching frequency, as shown in Figures 10.4 and 10.5.
With the help of Figure 10.4, it can be demonstrated that the minimum R_{out} occurs when the output resistances in the SSL and FSL regimes are equal, resulting in the maximum achievable power efficiency. From Figure 10.3, this maximum efficiency, η_{max}, can be calculated using Equation 10.6.

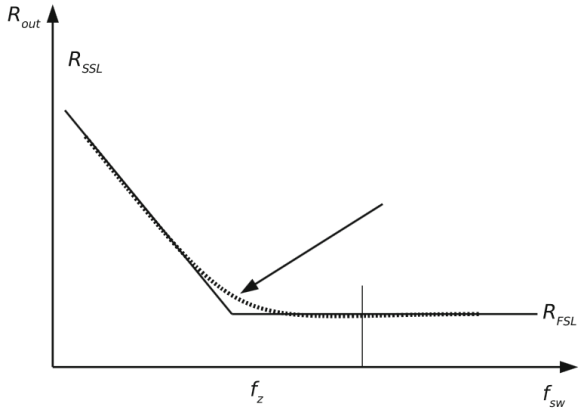


Figure 10.4: General plot of R_{out} vs. f_{sw} [56].

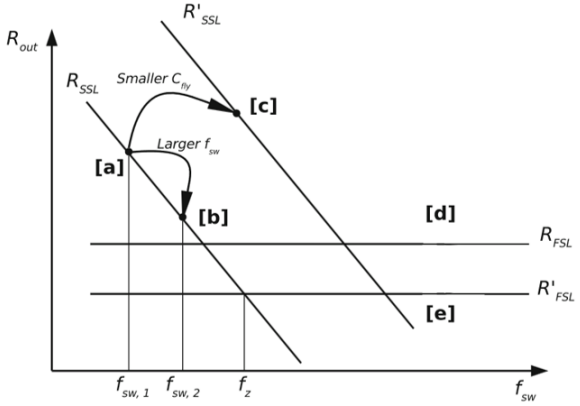


Figure 10.5: plot of R_{out} vs. f_{sw} with changing parameters [56].

$$\eta_{max} = \frac{V_{out}}{V_{out,nl}} = \frac{V_{out}}{MV_{\text{in}}} \tag{10.6}$$

Moreover, the output voltage in Figure 10.3, is determined by Equation 10.7.

$$V_{out} = MV_{\text{in}} - I_{out}R_{out}(D, K_{SSL}, K_{FSL}, f_{sw}, C_{fly}, R_{on}) \tag{10.7}$$

In addition to Figure 10.5, it shows how the curve changes when the parameters are modified.

10.1.2. Power losses of the SC-based DC-DC converter

The SC-based DC-DC converter experiences power losses due to the dynamics of the switches and the presence of parasitic capacitance. These losses include conduction losses, bottom-plate losses, gate driving losses, and control losses [57].

Conduction losses

The efficiency loss in the topology structure stems from the charging and discharging of flying capacitors by power switches and the finite on-resistance of the power switch. Represented as R_{out} in Figure 10.3, these effects result in conduction losses, $P_{cond.}$, calculated by Equation 10.8.

$$P_{cond.} = R_{out}I_{out}^2 \tag{10.8}$$

To enhance power efficiency by minimizing R_{out}, reducing voltage drop $V_{R_{out}}$ is essential. This can be achieved by increasing switching frequency and/or total flying capacitance, or decreasing the on-resistance of switches. However, higher switching frequency may result in increased switching losses. Additionally, increasing capacitance necessitates a larger chip area due to the inverse relationship with R_{SSL}. Decreasing on-resistance entails a larger switch width (as per Equation 10.9 assuming square-law model), which raises gate capacitance and switching losses. Similarly, increasing total flying capacitance increases switching losses through higher parasitic capacitance, thereby establishing a trade-off between switching and conduction losses.

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})} \tag{10.9}$$

Bottom-plate losses

Bottom-plate losses arise from the switching of internal nodes during phase changes, leading to the charging and discharging of parasitic capacitance associated with the flying capacitor. In CMOS technology, Metal-Insulator-Metal (MIM) capacitors are commonly utilized, introducing parasitic capacitance at both the top plate and the bottom plate. Typically, in MIM capacitors, the bottom plate is situated close to the substrate, resulting in the bottom plate capacitance being larger than the top plate capacitance [58]. Hence, the term ”bottom-plate losses”.

Gate driving losses
Flying capacitors are not the only components with parasitic capacitance. Power switches also exhibit this characteristic due to the gate capacitance, which is proportional to the width of the power switch. In CMOS power switches, the on-off transitions occur in each phase, necessitating gate drivers. This leads to the charging and discharging of the gate capacitance of the large power switches and the buffer chain. The buffer chain comprises cascaded inverters that amplify the control signal to effectively drive the gates of the power switches. The power dissipation attributed to the gate capacitance of the power switches and the switches in the buffer chain is calculated using Equation 10.10.

$$P_{drive} = f_{sw} V_{sw}^2 \sum_{i=1}^{n_{sw}} \left(C_{gate,i} + C_{eqbuffer,i} \right) \tag{10.10}$$

In this equation, V_{sw} is the voltage swing of the power switches and the drivers for the buffer chain, typically V_{in}. $C_{gate,i}$ is the gate capacitance of the i^{th} power switch, and $C_{eqbuffer,i}$ is the total capacitance of the i^{th} buffer chain to drive the i^{th} power switch.

Control losses
Control losses, denoted as $P_{control}$, stem from circuits controlling switches and parameters in the SC-based DC-DC converter for varying load conditions, ripple, and voltage regulation.

10.2. Regulation methods

10.2.1. Modulation techniques

There are several control schemes applicable to the SC-based DC-DC converter. As demonstrated in Section 10.1.1, the average model of the SC-based DC-DC converter includes R_{out} and M, with R_{out} further divided into R_{SSL} and R_{FSL}. This illustrates that various parameters can be modified, as summarized in Figure 10.6.

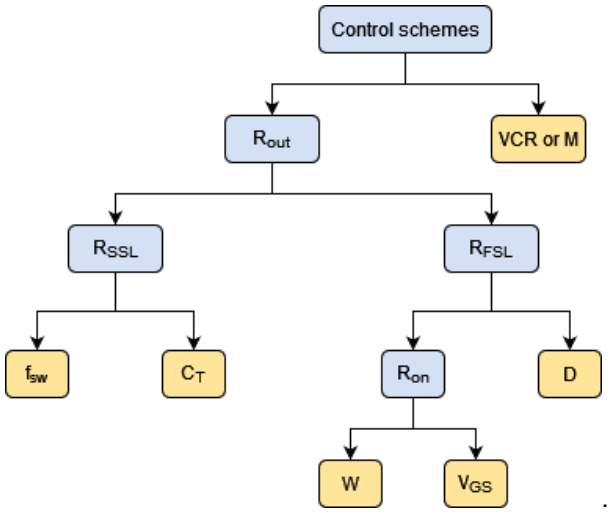


Figure 10.6: General overview of the parameters that can be modified in accordance to the average model of the SC-based DC-DC converter.

In this figure, VCR or M represents the voltage conversation ratio, f_{sw} is the switching frequency, C_T is the total flying capacitance, W is the width and V_{GS} is the gate-source voltage of the transistors that are used for implementing the switches and D is the duty cycle.

Regulation through VCR
This control scheme adjusts the VCR (or M), for the desired output voltage, reducing conduction losses with more switching cycles. Challenges arise as M can only take discrete values, like $\frac{1}{2}$ and $\frac{1}{3}$, leading to coarse regulation.

Regulation through R_{SSL}

R_{SSL} can be influenced by modulating f_{sw} and/or C_T. Pulse Frequency Modulation (PFM) is commonly used for f_{sw} modulation, employing pulse skipping mode or hysteretic control to minimize switching losses during light-load conditions. PFM achieves high efficiency by reducing switching power proportional to load current. However, this control scheme may result in high output ripple in the SSL region, which can be mitigated by using a large output capacitor.

Alternatively, capacitance modulation focuses on adjusting C_T. Flying capacitors are dynamically varied in size without affecting f_{sw}. This technique, using smaller flying capacitors of the big flying capacitor, controlled by digital codes, optimizes charge transfer in light-load conditions, reducing switching losses. However, the discrete nature of selectable values limits regulation, often requiring a combination with other control methods to meet specific specifications.

Regulation through R_{FSL}

An alternative regulation method involves modulating parameters through R_{FSL}. This is achieved by adjusting R_{on}, which can be divided into switch width modulation (SWM), gate-source voltage modulation, and pulse-width modulation (PWM).

In PWM mode, the pulse width is varied while keeping the switching frequency constant, controlling the output voltage in response to load current changes. Despite the 50% duty cycle preference for minimum R_{out} and R_{FSL}, varying duty cycle does not effectively enhance power efficiency, remaining unrelated to load current or power and resulting in constant switching losses. Duty cycle adjustments are limited from 0.1 to 0.5.

Modifying ON-resistance of MOSFETs via SWM alters R_{FSL} by adjusting the width of the CMOS switch, managing switching losses by varying gate capacitance. However, like capacitance modulation, SWM operates with discrete values for regulation, often employed with other control strategies. Another option is gate-source voltage modulation, determining the complete ON duration of the switch. Precise control of V_{GS} for each power switch is challenging due to non-linearity between drain-source current and gate-source voltage, requiring additional complex circuitry. Thus, controlling V_{GS} is less common in control loop designs.

10.2.2. Control loops in the literature

Output voltage regulation is commonly achieved using PFM alone or in combination with other control strategies, particularly SWM. While alternative control strategy combinations with PFM exist, we focus on five recent research papers that emphasize PFM, as shown in Table 10.1.

Table 10.1: Five selected research papers in the literature study.

	Selected research papers				
Parameters	**[59]**	**[60]**	**[61]**	**[62]**	**[63]**
Year	2023	2021	2021	2020	2017
Output voltage ripple (mV)	+ +	N.A.	N.A.	-	+ +
Response time	-	+ +	+	N.A.	-
Modulation scheme(s)	PFM	PFM	PFM, SWM	SWM	PFM, SWM
Gain Ratio	3:2	2:1	2:1, 3:1	3:1, 2:1	2:1, 3:1, 3:2

The analysis of Table 10.1 reveals a common focus among recent research papers on load transient response simulations, emphasizing response time and ripple values in their control loop architectures. Studies such as [59]–[62], and [63] primarily verify and validate their control loops' functionality, emphasizing meeting specified performance criteria.

For instance, in [59], achieving a ripple of 0.97 mV involves the use of an 800-nF output capacitor without explicit reasoning for its selection or intended purpose. However, this approach necessitates

integrating five high-speed comparators and five reference voltages, potentially increasing power consumption. In contrast, [60] utilizes a simpler control strategy with only three comparators, enabling independent load regulation and frequency control. However, scaling this approach for interleaving techniques may increase power consumption.

In [61], a PFM controller and SWM is proposed with two comparators, but it lacks explicit ripple reduction. Conversely, [62] outlines a strategy combining SWM with voltage ripple modulation control, though questions arise regarding voltage ripple modulation control (VRMC) operation during load-induced switching frequency scaling. Lastly, [63] employs a combination of PFM and SWM for regulating output voltage and enhancing power efficiency, involving activating or deactivating interleaving modules based on switching frequency and comparing with a reference voltage.

10.2.3. Limitation(s)

Each research paper proposes different control loops for voltage regulation, but they typically lack explicit demonstration of the control system design process. For example, in [59], although five comparators with an adaptive charge pump are utilized, the reason for choosing this configuration over others is unclear. Similarly, in [60], the use of three comparators lacks explanation regarding its contribution to achieving a fast transient response.

While the first four papers rely on voltage-controlled oscillators (VCO), comparators, and charge pumps, [63] uses a frequency divider and an up/down counter without elaboration on this choice. Generally, the control loop components would include a voltage-to-frequency converter and an accumulator/integrator, but a systematic approach for control loop design is missing in these research papers.

Designing control systems with control theory for SC-based DC-DC converters in CMOS is less common compared to power converters with inductors. However, [64] presents an approach using a sampled-data model to design a PI controller meeting specifications. This approach's complexity arises from manipulating matrices involving symbolic algebra despite using tools like Python and MATLAB.

Moreover, while the study employs a PI controller for voltage regulation, it does not justify this choice or address adapting to larger matrices for advanced topologies like Series-Parallel. Hence, highlighting a simplified mathematical model coupled with a systematic control-system approach tailored to a specific application would be beneficial. This would efficiently achieve the desired performance specifications while minimizing complexity and potential errors inherent in more elaborate methodologies.

11

Control design of the power converter

11.1. Design of the ideal SC-based DC-DC converter

In Chapter 10, an average model of the SC-based DC-DC converter was introduced. A power converter with sub-loads (V_{out} = 1.1 V) with V_{in} of 4 V has been chosen. This selection allows us to assess the control loop's performance with practical load currents, which are mentioned in Chapter 9.1, particularly its ability to handle load transient responses in practice.

11.1.1. VCR and topology selection

Several common VCRs were chosen for the comparison based on the output resistance, calculated using Equation 11.1.

$$R_{out} = \frac{MV_{in} - V_{out}}{I_{out}} \tag{11.1}$$

The chosen VCRs, along with the no-load voltage and the R_{out} values, are shown in Table 11.1.

Table 11.1: General overview of $V_{out,nl}$ and R_{out} for a few VCRs.

VCR	$V_{out,nl}$	R_{out} (Ω)
1/4	1	< 0
1/3	1.3	39.5
1/2	2	152.5
2/3	2.67	265.5
3/4	3	322

This table indicates that a VCR of 1/4 is not feasible since the no-load voltage is 1 V, while the required output voltage is 1.1 V. On the other hand, VCRs of 1/2, 2/3, and 3/4 are suitable candidates to provide the required supply voltage. However, increasing the no-load voltage with a constant V_{out} of 1.1 V would result in an increased voltage drop across R_{out} (V_{Rout}), thereby decreasing the power efficiency as stated in Equation 10.6. Selecting a VCR of 1/3 would be the preferred choice, as $V_{out,nl}$ is sufficient to provide 1.1 V while minimizing V_{Rout}.

Common topologies for SC-based DC-DC converters include Series-Parallel, Fibonacci, doubler, Dickson, and ladder. Another topology found in the literature is the recursive topology, commonly used for specific VCRs such as 1/8 and 1/16. An example of the recursive topology is shown in study [65]. The doubler topology is employed for VCR values of 2 and 1/2. However, neither of these topologies is typically used for VCR of 1/3, leaving four topologies for consideration. The selection of the topology is based on choosing the K_{SSL} and K_{FSL} to reduce the R_{out}, as described mathematically with the help of Equations 10.1 to 10.3, 10.9, and Figure 10.4:

$$R_{out,min} \longrightarrow R_{SSL} = R_{FSL} = R_{min} \longrightarrow R_{out,min} = \sqrt{2R_{min}^2} = \sqrt{2}R_{min}$$

$$R_{out,min} = \sqrt{2}R_{min} = \frac{\sqrt{2}K_{SSL}}{f_{sw}C_{fly}} = \sqrt{2}K_{FSL}R_{on}$$

$$R_{out,min} \propto \frac{\sqrt{2}K_{FSL}}{\left(\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\right)}$$

$$R_{out,min} \propto \frac{\sqrt{2}K_{SSL}}{f_{sw}C_{fly}}$$

It is observed here that reducing K_{FSL} and K_{SSL} would decrease $R_{out,min}$. The values of K_{SSL} and K_{FSL} for each topology are derived in Appendix B.2.1, and they are summarized in Table 11.2.

Table 11.2: Topology dependent factors in accordance to Appendix B.2.1.

Topology	K_{SSL}	K_{FSL}
Series-Parallel	0.222	1.56
Ladder	0.667	2.67
Dickson	0.222	1.78
Fibonacci	0.222	2.22

Based on this table, Series-Parallel topology is selected as it has the minimum K_{SSL} and K_{FSL}.

11.1.2. Selection of the transistor types and voltage rating

The sizing of the ideal SC-based DC-DC converter starts with Figures 11.1 and 11.2. Subsequently, Tables 11.3 and 11.4 are used for determination of the transistor type, of which the blocking voltages, the voltage across the power switches in the 'off' state, are derived in Appendix B.2.2.

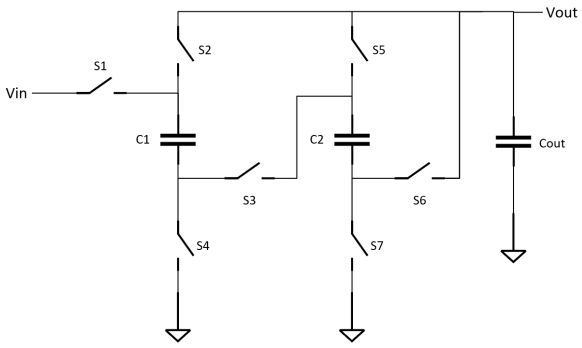


Figure 11.1: Series-Parallel topology.

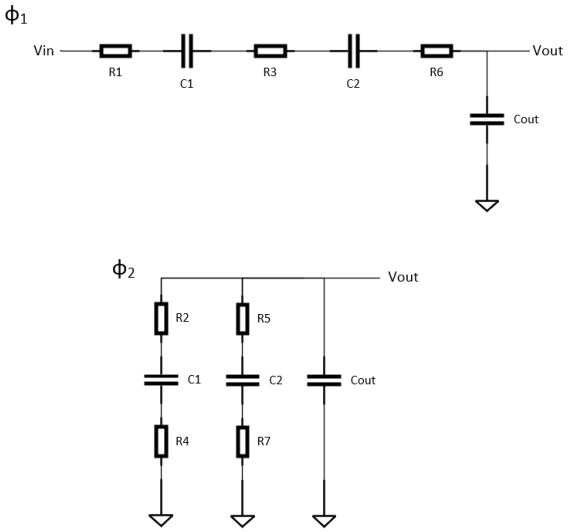


Figure 11.2: Phase 1 and 2 of the Series-Parallel topology.

Table 11.3: A general overview of voltage terminals, blocking voltages and NMOS and PMOS types for Switches S1-S4.

Switches	S1				S2				S3				S4			
ϕ_{phase}	ϕ_1		ϕ_2		ϕ_1		ϕ_2		ϕ_1		ϕ_2		ϕ_1		ϕ_2	
Terminals	V_{in}	V_{C1+}	V_{in}	V_{C1+}	V_{out}	V_{C1+}	V_{out}	V_{C1+}	V_{C1-}	V_{C2+}	V_{C1-}	V_{C2+}	V_{C1-}	GND	V_{C1-}	GND
V	1	1	1	1/3	1/3	1	1/3	1/3	2/3	2/3	0	1/3	2/3	0	0	0
|ΔV|	0		2/3		2/3		0		0		1/3		2/3		0	
$\mathbf{V_{rating}}$	5 V				5 V				5 V / 2 V				5 V			
$\mathbf{V_s}$ **(switch on)**	4 V				1.33 V				2.67 V				0 V			
xmos5v	PMOS				NMOS				PMOS				NMOS			
xmos2v	PMOS				PMOS				PMOS				NMOS			

Table 11.4: A general overview of voltage terminals, blocking voltages and NMOS and PMOS types for Switches S5-S7.

Switches	S5				S6				S7			
ϕ_{phase}	ϕ_1		ϕ_2		ϕ_1		ϕ_2		ϕ_1		ϕ_2	
Terminals	V_{out}	V_{C2+}	V_{out}	V_{C2+}	V_{C2-}	V_{out}	V_{C2-}	V_{out}	V_{C2-}	GND	V_{C2-}	GND
V	1/3	2/3	1/3	1/3	1/3	1/3	0	1/3	1/3	0	0	0
|ΔV|	1/3		0		0		1/3		1/3		0	
$\mathbf{V_{rating}}$	5 V / 2 V				5 V / 2 V				5 V / 2 V			
$\mathbf{V_s}$ **(switch on)**	1.33 V				1.33 V				0 V			
xmos5v	NMOS				NMOS				NMOS			
xmos2v	PMOS				PMOS				NMOS			

The interpretation of Tables 11.3 and 11.4 can be understood as follows: take, for instance, Switch S5. With two clock phases (ϕ_1 and ϕ_2) and each voltage terminal having a fraction of V_{in} (4 V), the blocking voltage $|\Delta V|$ of Switch S5 is one-third of V_{in} (1.33 V). This implies that the NMOS and PMOS voltage rating must be either 5 V or 2 V. Using Cadence Virtuoso, the source voltage (V_s) when the switch is conducting can be determined, aiding in selecting the appropriate transistor type (xmos5v or xmos2v).

To make the selection between xmos5v and xmos2v, minimizing R_{on} requires maximizing the gate-source voltages. Input signals of 4 V and 1.8 V are utilized for MOSFETs rated at 5 V and 2 V, respectively, with V_{in} of the power converter. For power switches S3 and S5-S7, where both MOSFETs rated at 5 V and 2 V can be used, subtracting V_s from the input signals maximizes V_{GS} when MOSFETs with a rated voltage of 5 V are selected. Hence, the transistor types in xmos5v are chosen.

11.1.3. Sizing of the flying capacitors

The chip area for the PMU remains undetermined, but Chapter 3 specifies that the headstage volume must be smaller than 1.1x1.1x1.1 cm^3, equating to a maximum area of 1.1x1.1 cm^2 (= 11x11 mm^2). Assuming an equally divided chip area for various blocks, including the AC-DC converter, PMU, f_0 tuning block, DSP, stimulation, recording, IMN, and other potential circuitry, the area for each block can be calculated using Equation 11.2.

$$A_{PMU} = \frac{11x11\ \mathrm{mm}^2}{8} = 1.9\ \mathrm{mm}^2 \tag{11.2}$$

Assuming that the area is predominantly occupied by the flying capacitors, MIM (Metal-Insulator-Metal) capacitors are chosen as the capacitor density of these capacitors are known while other capacitor types are unknown. The total flying capacitance is computed using Equation 11.3.

$$C_{fly} = C_{density} \cdot A_{PMU} \tag{11.3}$$

Since the MIM capacitor's density, $C_{density}$, is 2 nF/mm^2 for TSMC 180 nm CMOS technology, referenced from [66], and A_{PMU} is 1.9 mm^2, the total flying capacitance, $C_{fly,}$ is 3.8 nF. Accounting for other circuits within the PMU, C_{fly} is set to 2 nF. The optimized flying capacitor is given by Equation 11.4 [54].

$$C_i = k_{C,i} C_{fly} = \frac{|a_{C,i}|}{\sum_{i=1}^{n_c} a_{C,i}} C_{fly} \tag{11.4}$$

Using the charge multipliers ($a_{C1} = a_{C2} = \frac{1}{3}$) from the Series-Parallel topology, as derived in Appendix B.2.1, and Equation 11.4, each flying capacitor is set to 1 nF.

11.1.4. On-resistance and switching frequency

The on-resistance and switching frequency are determined using the relevant technology parameters obtained from Cadence Virtuoso. These parameters are outlined in Table 11.5.

Table 11.5: Relevant technology parameters for nmos and pmos.

Switch type	$C_{gate,density}$ (fF / μm)	ρ (Ω · μm)	Tested with $V_{sw} = V_{in}$
nmos5v	1.71	2137	4 V
pmos5v	1.63	5751	4 V
nmos2v	1.77	654	1.8 V
pmos2v	1.73	2142	1.8 V

It is important to note that the initial value of K_{SSL} was 0.222, derived for $C_1 = C_2 = C_{fly}$ in Appendix B.2.1 with $K_{c,i} = 1$. However, since the optimized flying capacitor is now 1 nF (C_{fly} = 2 nF), $K_{c,i}$ is 1/2 as per Equation 11.4. Substituting this value into Equation 10.4, the new value of K_{SSL} is 0.444.

In Chapter 10, various power losses were introduced. Since power switch sizing is essential when using a non-ideal power converter, minimizing power losses should be considered during sizing, which consists of gate driving losses and conduction losses. Assuming that all the power switches have the same width, on-resistance, and gate capacitance, and without considering the gate drivers of the power switches, Equation 11.5 is formulated.

$$P_{loss} = nC_g f_{sw} V_{in}^2 + I_{load}^2 R_{\text{out}} \tag{11.5}$$

In this equation, n is the number of power switches in the topology, C_g is the gate capacitance, and V_{in} is the voltage swing. P_{loss} is minimized when R_{out} and f_{sw} are optimized. R_{out} is optimized when R_{FSL} is equal to R_{SSL}. Hence, Equations 11.6 and 11.7 are derived.

$$f_{sw,opt} = \frac{K_{SSL}}{\sqrt{2} K_{FSL} C_{fly} R_{on}} \tag{11.6}$$

$$R_{\text{out,min}} = \sqrt{2} R_{\text{FSL}} = \sqrt{2} K_{FSL} R_{on} \tag{11.7}$$

Furthermore, the width of the power switches is proportional to the electrical resistivity and the gate capacitance, represented as ρ and $C_{g,unit}$, respectively.

Based on Equations 11.6 and 11.7, ρ and $C_{g,unit}$, The minimized power loss is shown in Equation 11.8.

$$P_{loss,min} = nC_{g,unit} V_{in}^2 \frac{K_{SSL} W^2}{C_{fly} K_{FSL} \rho} + \frac{\sqrt{2} K_{FSL} \rho}{W} I_{load}^2 \tag{11.8}$$

Taking the derivative with respect to the width and solving for width, W, the optimum width is derived, as shown in Equation 11.9.

$$W_{opt} = \left(\frac{\sqrt{2} C_{fly} K_{FSL}^2 \rho^2 I_{load}^2}{2nV_{in}^2 C_{g,unit} K_{SSL}} \right)^{\frac{1}{3}} \tag{11.9}$$

Equation 11.9 was used in the Python code, as shown in Appendices C.3.1 and C.3.2, to determine W_{opt}. Using the technology parameters of pmos5v, selected due to the highest electrical resistivity in Table 11.5, I_{load} = 5.9 mA, C_{fly} = 2 nF, n = 7 switches, K_{SSL} = 0.444, K_{FSL} = 1.56 and V_{in} = 4 V, W_{opt} is calculated to be 290 μm. The output voltage of 1.1 V is achieved with $R_{on,opt}$ of 19.883 Ω and f_{sw} of 9.048 MHz.

The schematic and transient response, with output capacitor, C_{out} (C_{out} » C_{fly}), are shown in Figures 11.3 and 11.4, respectively.

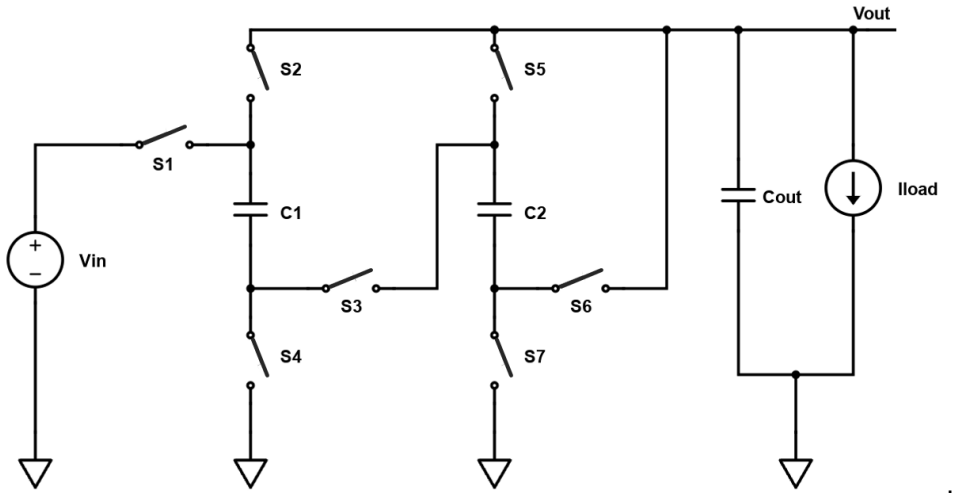


Figure 11.3: Schematic of the power converter with ideal switches.

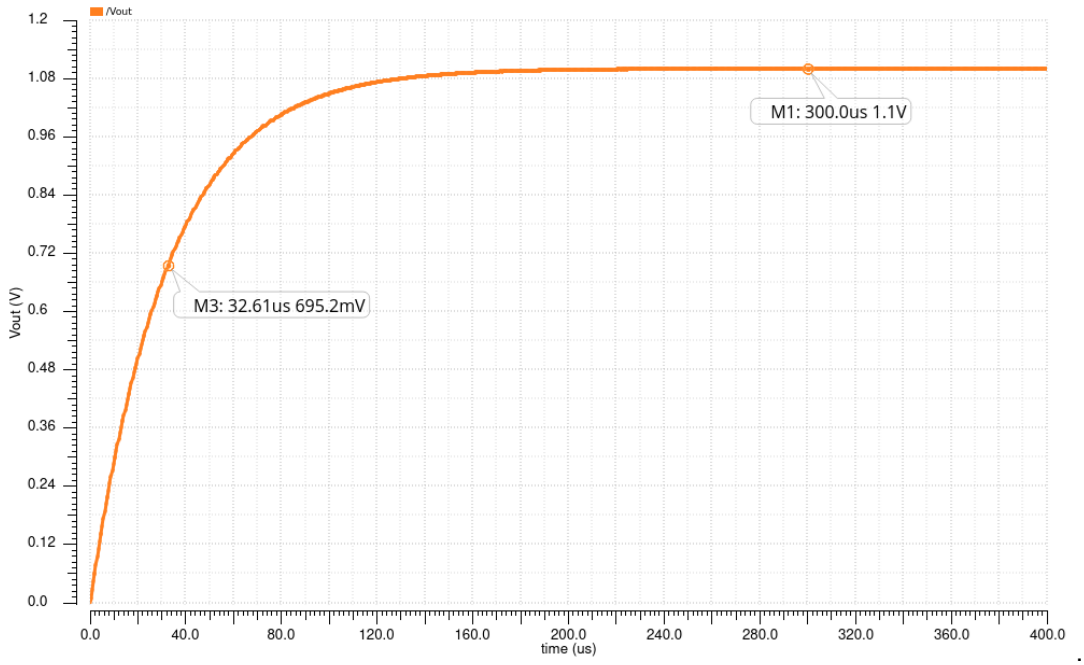


Figure 11.4: Verification of the output voltage using a transient response simulation.

Figure 11.4 displays the transient response of the ideal power converter, achieving an output voltage of 1.1 V with a time constant of 32.61 µs and f_{sw} was modified to 7.789 MHz, because the f_{sw} (9.048 MHz) is calculated with Equation 10.1, which approximates the simulated power converter curve, R_{out} vs. f_{sw}, similar to Figure 10.4. The comparison between the simulated and approximated R_{out} vs. f_{sw} is shown in Appendix B.2.3. It is worth noting that a 1 µF output capacitor has been utilized, consistent with the assumptions made in the calculations of K_{SSL} and K_{FSL}. The verification of K_{SSL} and K_{FSL} is detailed in Appendix B.2.3. It was demonstrated that K_{SSL} and K_{FSL} are 0.4356 and 1.51, respectively, which aligns well with the above-mentioned theoretical values of K_{SSL} and K_{FSL} of 0.444 and 1.56, respectively.

11.2. Control system design

This chapter introduces a proposed mathematical model of the power converter and a control-system approach tailored to the specific application.

11.2.1. Modeling of the power converter

Since each power converter can be represented by an equivalent average model for its static behavior, we can derive an approximate dynamic continuous model using Figure 11.5.

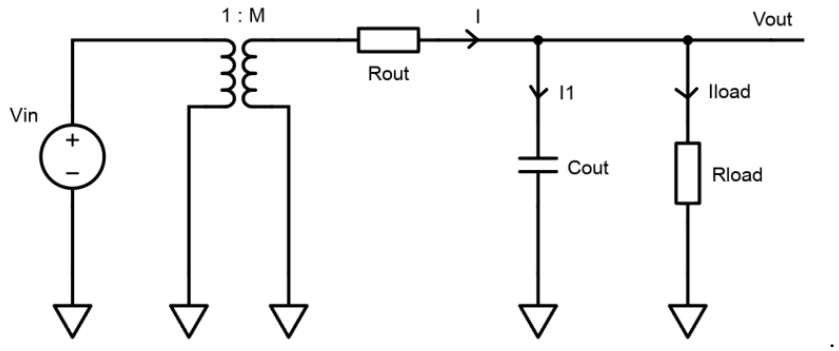


Figure 11.5: SC-based DC-DC converter average model with R_{load}.

For the voltage regulation control loop design, the switching frequency, f_{sw}, is related to the load current. The control-to-output transfer function becomes V_{out} over f_{sw}, where V_{out} represents the measured variable and f_{sw} the manipulated variable. Equation 11.10 may be relevant if readers are interested in the small change of input voltage affecting the output voltage, while Equations 11.11, 11.12, and 11.13 are necessary for the control loop design.

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)} = \frac{M}{C_{out}R_{out}} \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)} \tag{11.10}$$

$$\frac{\hat{V}_{out}(s)}{\hat{f}_{sw}(s)} = -\frac{K1}{\sqrt{\frac{K1}{(f_{sw})^2} + K2} \cdot (f_{sw})^3} \left(\frac{V_{out} - MV_{in}}{C_{out}(R_{out})^2}\right) \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)} \tag{11.11}$$

$$K1 = \left(\frac{K_{SSL}}{C_{fly}}\right)^2 \tag{11.12}$$

$$K2 = (K_{FSL}R_{on})^2 \tag{11.13}$$

Those equations are derived in Appendix D.4.1.

To verify the model's suitability for subsequent steps, we establish the operating point of the SC-based DC-DC converter under full load conditions (I_{load} = 5.9 mA), requiring a switching frequency f_{sw} of 7.789 MHz, as discussed in Section 11.1.4. Obtaining the control-to-output transfer function directly from simulation is challenging. To address this, a Verilog-A based voltage-controlled oscillator (VCO) and a non-overlapping clock generator (NOV) circuit was added to the power converter. This setup enables us to determine the transfer function from the VCO input, V_{ctrl}, to V_{out}, as depicted in Figures 11.6, 11.7 and 11.8.

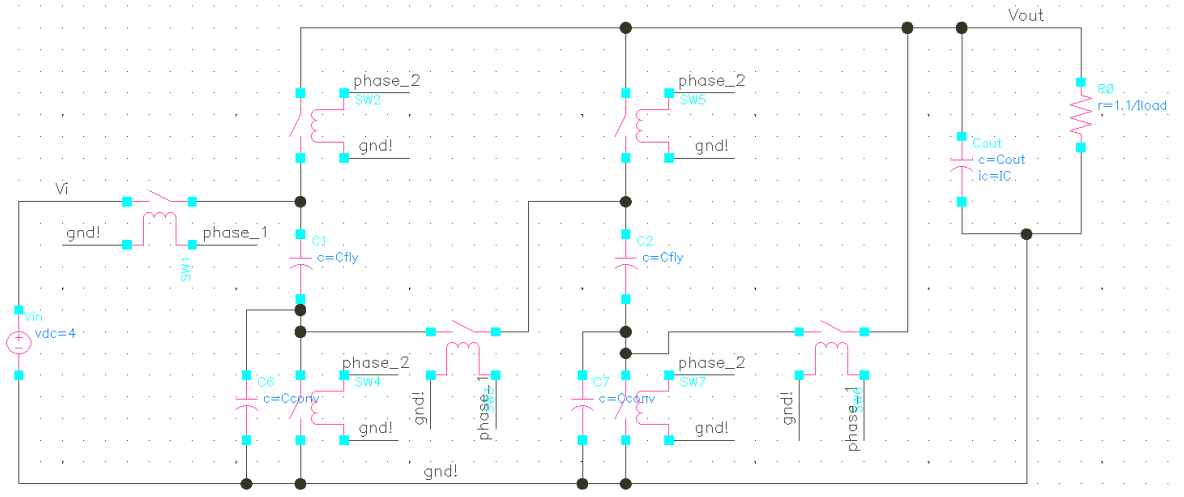


Figure 11.6: SC-based DC-DC converter with R_{load}.

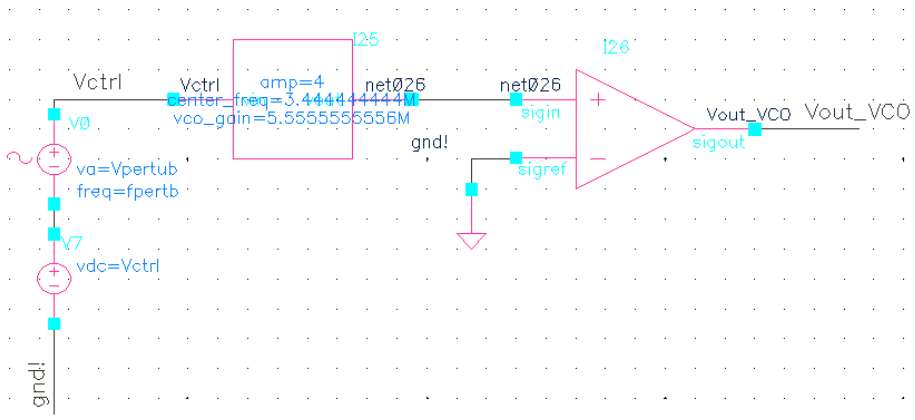


Figure 11.7: A Verilog-A based VCO with a comparator for sine wave to square wave conversion.

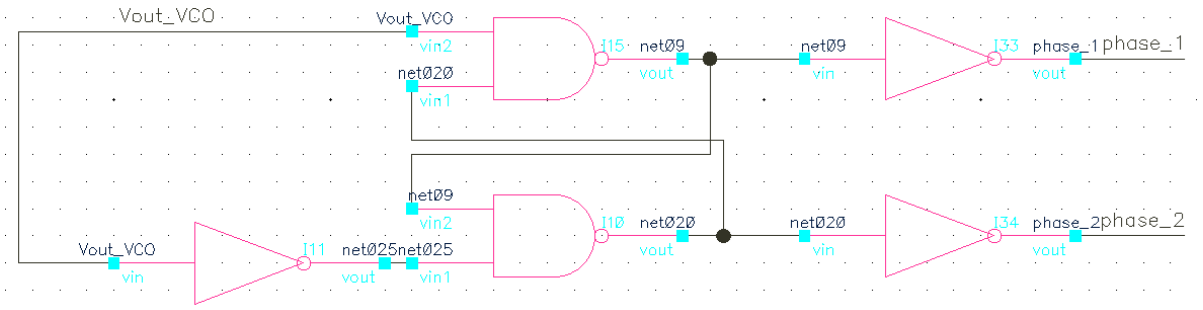


Figure 11.8: NOV circuit.

The 'phase_1' and 'phase_2' labels in Figure 11.6 are connected to the output nodes of the NOV circuit, shown in Figure 11.8. Moreover, the 'Vout_VCO' in Figure 11.7 is connected to the input of the NOV circuit.

The K_{VCO} and the center frequency, f_0, are calculated by using Equation 11.14 and 11.15, respectively.

$$K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \tag{11.14}$$

$$f_{sw} = K_{VCO} V_{CTRL} + f_0 \tag{11.15}$$

To regulate the output voltage within a specified range of load currents around 5.9 mA, f_{max} and f_{min} are set to 9 MHz and 4 MHz, respectively. However, the potential input voltage range of the VCO remains unknown. Initially, V_{max} = 1 V and V_{min} = 0.1 V are chosen as starting point. This yields a K_{VCO} of 5.56 MHz/V with an f_0 of 3.44 MHz.

Unfortunately, Cadence Virtuoso does not support PAC-analysis for Verilog-A written VCOs. Therefore, a perturbation voltage source with an amplitude of 100 mV is added to V_{in} to verify Equation 11.10. This verification process is similar to Equation 11.11, albeit the equation must be multiplied by K_{VCO} and the perturbation voltage source is added to V_{ctrl}, at the input of the VCO. Furthermore, during the model refinement, the average time delay and the dead time are incorporated into the model as power converters require time to respond to external disturbances such as input voltage. Consequently, Equations 11.16 and 11.17 are formulated.

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)} = \frac{M}{C_{out}R_{out}} \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)} \cdot e^{-\left(\frac{T_{sw}}{2} + t_{dead}\right)s} \tag{11.16}$$

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{ctrl}(s)} = -\frac{K_{VCO}K1}{\sqrt{\frac{K1}{(f_{sw})^2} + K2} \cdot (f_{sw})^3} \left(\frac{V_{out} - MV_{in}}{C_{out}(R_{out})^2}\right) \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)} \cdot e^{-\left(\frac{T_{sw}}{2} + t_{dead}\right)s} \tag{11.17}$$

Figures 11.9 and 11.10 depict the calculated (solid blue line) and manually simulated (red asterisk points) Bode plots of both transfer functions.

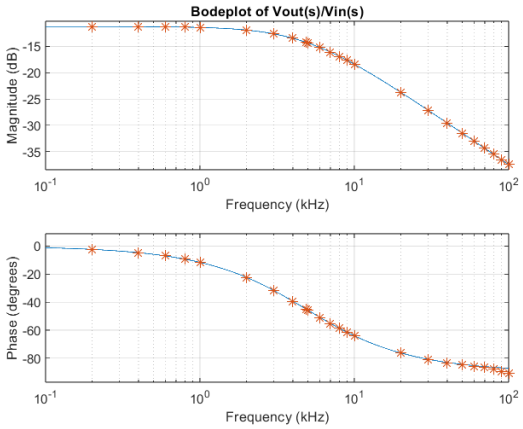


Figure 11.9: $\hat{V}_{out}$ vs. $\hat{V}_{in}$ at operating point I_{load} = 5.9 mA.

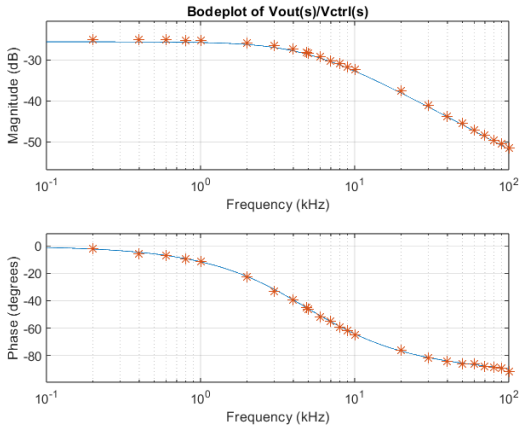


Figure 11.10: $\hat{V}_{out}$ vs. $\hat{V}_{ctrl}$ at operating point I_{load} = 5.9 mA.

The results illustrate that the Bode plots of the model align well with the simulation results, thus confirming the verification of the model for controller design.

11.2.2. Control objectives and specifications

The control objectives of the VRCL block are listed below.

1. The VRCL must maintain stability under load current and input voltage disturbances.
2. The VRCL must ensure the output voltage of the SC-based DC-DC converter remains constant despite small disturbances.
3. The VRCL is designed to measure the output voltage and track the reference setpoint, which is the desired output voltage.
4. The VRCL must be fast enough to react on the load change.

Considering that the loads (DSP and recording) have not been designed yet, the maximum allowable ripple voltage for the total load is currently unknown. With the help of an expertise from the Bioelectronics (BE) group, involving recording IC design in a different project, an initial value of 100 mV_{pp} has been chosen for the ripple voltage, V_{ripple}. Additionally, accounting for an output voltage tolerance of $\pm 10\%$, we have the following considerations:

$$V_{out,max} = \left(V_{out} \cdot \frac{110\%}{100\%}\right) - \frac{V_{ripple}}{2} = 1.16\ V \tag{11.18}$$

$$V_{out,min} = \left(V_{out} \cdot \frac{90\%}{100\%}\right) + \frac{V_{ripple}}{2} = 1.04\ V \tag{11.19}$$

$$V_{out,max} - V_{out} = +0.06\ V \text{ and } V_{out,min} - V_{out} = -0.06\ V \tag{11.20}$$

$$\text{Tolerance} = \frac{|\pm 0.06\ V|}{1.1\ V} = 5.46\% \tag{11.21}$$

Based on the tolerance, the maximum overshoot should not exceed 1.16 V, and the output voltage must be regulated within the bounds of $V_{out,max}$ and $V_{out,min}$. This specification also determines the portion of the steady-state output voltage at which the settling time is measured.

Since we have four operating points as shown in Table 9.1 in Chapter 9, all the operating points with the required f_{sw} and R_{out} for the corresponding load current have been summarised in Table 11.6 using R_{on} = 19.883 Ω, C_{fly} = 2 nF, V_{in} = 4 V, V_{out} = 1.1 V, M = 1/3 and C_{out} = 1 µF.

Table 11.6: General overview of f_{sw} and R_{out} for different operating points.

I_{load}	f_{sw}	R_{out} (Ω)
20 µA	19.1 kHz	11.642k
910 µA	870 kHz	255.41
5.01 mA	5.62 MHz	46.455
5.9 mA	7.789 MHz	39.548

Using this table, t_{dead} = 500 ps, Equation 11.17 and a frequency divider, required for operating points with I_{load} that need less than f_{min} = 4 MHz of the VCO as f_{sw}, four equations for each operating point are shown below.

$$\mathrm{H_{tot,5.9mA}(s)} = \frac{0.05285}{3.2626 \cdot 10^{-5}s + 1} e^{-(6.47 \cdot 10^{-8})s} \tag{11.22}$$

$$\mathrm{H_{tot,5.01mA}(s)} = \frac{0.1055}{3.834 \cdot 10^{-5}s + 1} e^{-(8.95 \cdot 10^{-8})s} \tag{11.23}$$

$$\mathrm{H_{tot,910uA}(s)} = \frac{0.2636}{0.0002109s + 1} e^{-(5.75 \cdot 10^{-7})s} \tag{11.24}$$

$$\mathrm{H_{tot,20uA}(s)} = \frac{0.2675}{0.009608s + 1} e^{-(2.62 \cdot 10^{-5})s} \tag{11.25}$$

Based on these equations, it is observed that when the load draws I_{load} of 5.9 mA from the power converter, the time constant is approximately 32.63 μs, which is also the smallest time constant among all the operating points. This indicates that for the worst-case scenario, the time constant at I_{load} = 5.9 mA is selected to obtain the smallest rise and settling time. These can be estimated by Equations 11.26 and 11.27, derived in Appendix D.4.2.

$$t_r = 2.1972\tau \tag{11.26}$$

$$t_s = 2.9077\tau \tag{11.27}$$

With these equations, τ represents the system's time constant and t_r and t_s denote the rise time and settling time, respectively. The calculated results are t_s = 94.6 μs and t_r = 71.28 μs.

The specifications are listed below.

1. The output voltage of the power converter is maintained at 1.1 ± 0.06 V (tolerances of $\pm 5.46\%$).
2. The reference setpoint (desired output voltage) is set to 1.1 V.
3. The tracking error, e_{ss}, should ideally be 0 mV. In non-ideal case, an acceptable e_{ss} of 20 mV is selected as starting point.
4. The settling time $t_s(5.46\%)$ must be less than 94.6 μs.
5. The rise time $t_r(10\% \text{ to } 90\%)$ must be less than 71.28 μs.
6. The maximum overshoot (OS) is 5.46%.

11.2.3. Controller design

The general feedback control system in our application is shown in Figure 11.11.

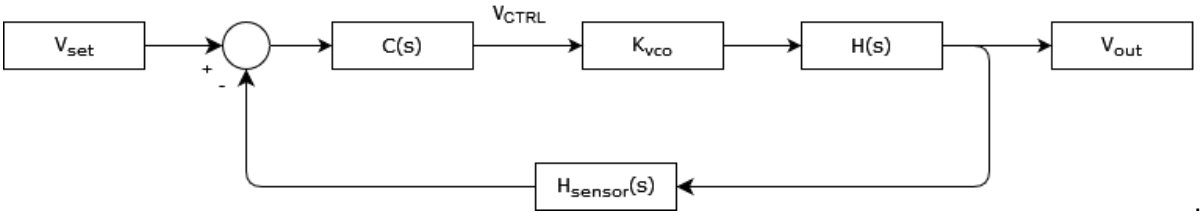


Figure 11.11: General feedback control system of our application.

In this figure, $H_{sensor}(s)$ is set to 1 since the measured variable (i.e., the output voltage) is close to 1.1 V, and the voltage rating of the transistors exceeds 1.1 V. The control voltage, V_{ctrl}, is converted to a switching frequency, making only the VCO gain relevant. H(s) represents the power converter transfer function (process), while C(s) is the transfer function of the controller. Conventionally, a control loop would be designed based on the process model, selecting a controller to tune to the desired response using tuning rules such as the Ziegler-Nichols method. However, this approach could be time-consuming if the controller is not chosen properly. Additionally, there is a wide range of controller choices, meaning that one can select any controller that provides the desired response. Nevertheless, some controllers may be unsuitable based on implementation constraints in software or hardware. In our application, instead of selecting a controller directly, we define the desired response and then determine which controller is needed to achieve it.

Let G(s) represent the multiplication of K_{vco} and H(s), where the transfer function of G(s) is given by Equation 11.17. By applying the feedback reduction rule in Figure 11.11 and obtaining the transfer function in the form of C(s) = f(V_{out}, V_{set}, G), Equation 11.28 can be formulated.

$$C(s) = \frac{1}{G(s)} \left(\frac{\left(\frac{V_{out}(s)}{V_{set}(s)}\right)}{1 - \left(\frac{V_{out}(s)}{V_{set}(s)}\right)} \right) \tag{11.28}$$

In this equation, $\frac{V_{out}(s)}{V_{set}(s)}$ is chosen as the desired response transfer function, and G(s) is generalized to be a first-order model with time delay and total gain, K_{tot}, represented by Equations 11.29 and 11.30, respectively.

$$H_{desired}(s) = \frac{1}{\tau_{des} s + 1} e^{-\left(\frac{T_{sw}}{2} + t_{dead}\right)s} \tag{11.29}$$

$$G(s) = \frac{K_{tot}}{\tau s + 1} e^{-\left(\frac{T_{sw}}{2} + t_{dead}\right)s} \tag{11.30}$$

In Equations 11.29 and 11.30, $H_{desired}(s)$ is the desired transfer function, τ_{des} is the desired time constant determined by the settling time and rise time specifications, T_{sw} is the switching period, t_{dead} is the delay between the two clock phases (charging and discharging phases) of a power converter where power switches are off, τ is the system's time constant, and K_{tot} is the total DC gain of the power converter transfer function plus the VCO gain.

Since Equations 11.22 to 11.25 are represented as first-order models with time delay, of which the delay is close to 0 s, the desired response is also a first-order model with time delay, with the desired time constant τ_{des} selected to be smaller than the time constant of the open-loop system. Subsequently, Equations 11.29 and 11.30 are substituted into Equation 11.28, and using 1st order Taylor series to approximate the time delay exponential expression, Equation 11.31 is formulated.

$$C(s) = \frac{\tau}{K_{tot}\left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right)} + \frac{1}{K_{tot}\left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right)s} \tag{11.31}$$

This equation indicates that a controller must incorporate both proportional and integral functions, equivalent to a PI controller. Hence, a PI controller is chosen to attain the desired response. The general equation of a PI controller is represented by Equation 11.32.

$$H_{PI}(s) = K_P + \frac{K_I}{s} \tag{11.32}$$

Matching Equation 11.31 with Equation 11.32, we obtain the equations for tuning the controller.

$$K_P = \frac{\tau}{K_{tot}\left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right)} \tag{11.33}$$

$$K_I = \frac{1}{K_{tot}\left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right)} \tag{11.34}$$

If we rewrite Equation 11.17 in the form of Equation 11.30, we obtain the following:

$$K_{tot} = -K_{vco} \cdot \frac{K1}{\sqrt{\frac{K1}{(f_{sw})^2} + K2 \cdot (f_{sw})^3}} \left(\frac{V_{out} - MV_{in}}{C_{out}(R_{out})^2}\right) \cdot \frac{1}{\left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)}$$

$$\tau = \frac{1}{\left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}R_{out}}\right)}$$

With this control-system approach and the corresponding equations, tuning the PI controller can be straightforwardly accomplished using a MATLAB script. The tuning script is provided in Appendix C.3.3.

11.2.4. Results

Using the MATLAB script to tune the PI controller to obtain the desired response for each operating point, the required values to achieve the specifications are summarized in Table 11.7.

Table 11.7: Tuned parameters for PI-controller for each operating point.

Operating point	K_P	K_I
I_{load} = 5.9 mA	20	610106
I_{load} = 5.01 mA	12	305337
I_{load} = 910 uA	26	120329
I_{load} = 20 uA	670	65445

Then, each operating point was simulated in Simulink to verify that the specifications are achieved. Figure 11.12 illustrates the simulation setup for the operating point with I_{load} = 5.9 mA. Additional simulation results for other operating points can be found in Appendix D.4.6.

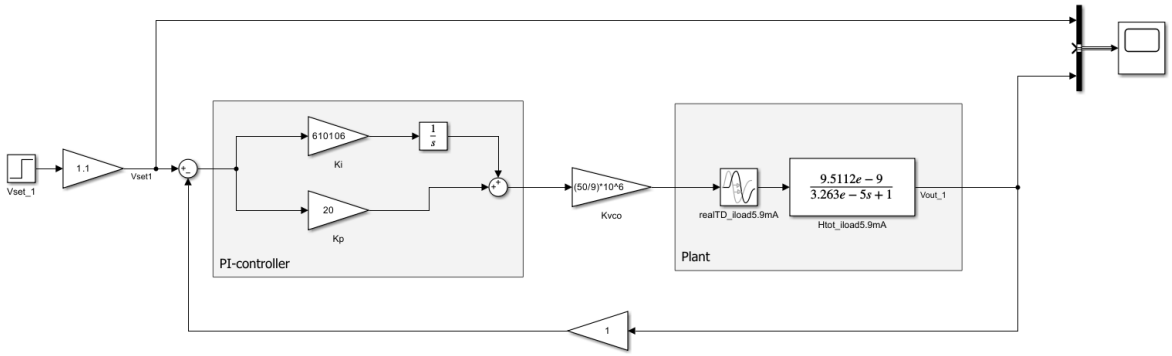


Figure 11.12: Simulink block diagram for verification for I_{load} = 5.9 mA.

The simulation results when the loads are in active mode, are shown in Figures 11.13 and 11.14.

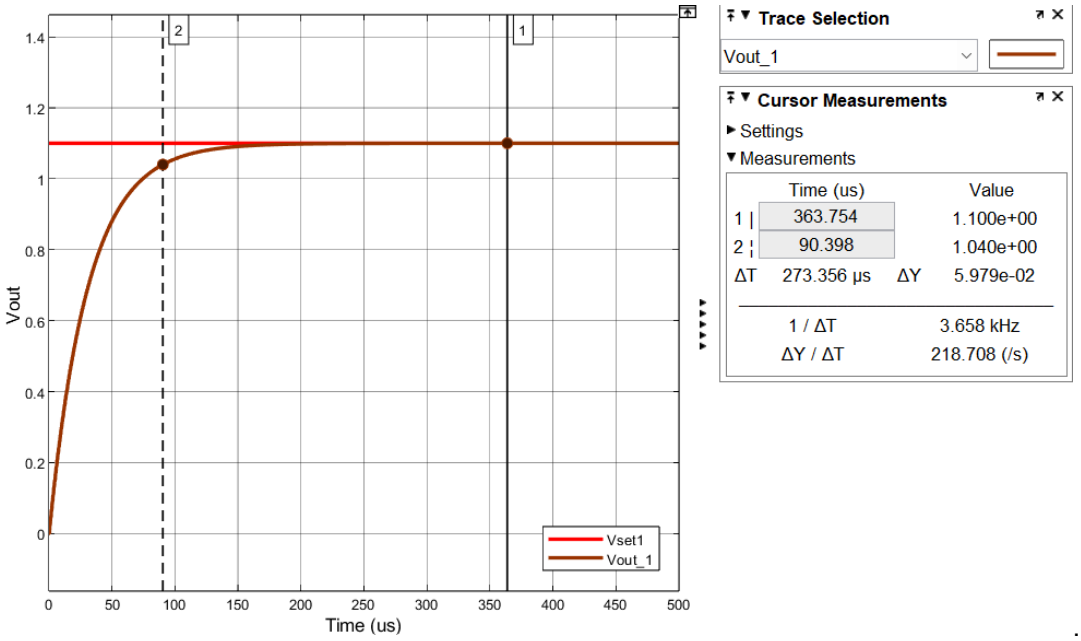


Figure 11.13: Verification of settling time and overshoot at operating point I_{load} = 5.9 mA.

Figure 11.13 illustrates that the control loop has a settling time of 90.4 µs. Moreover, the tracking error, e_{ss}, in this figure is 0 mV as the output voltage converges to 1.1 V in steady state.

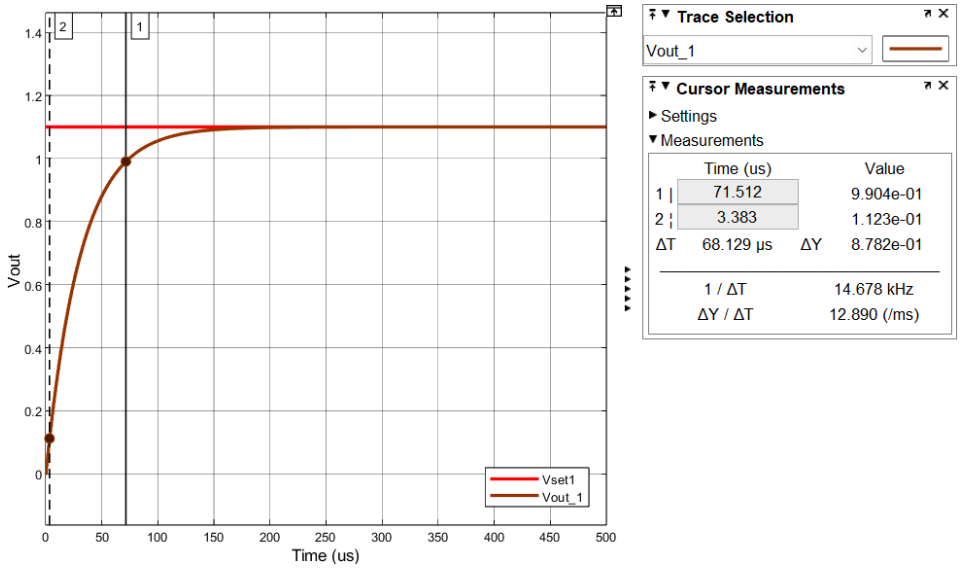


Figure 11.14: Verification of rise time at operating point I_{load} = 5.9 mA.

Figure 11.14 shows a rise time of 68.13 µs. An additional verification was conducted by applying a small input voltage to observe the recovery time and behavior, as depicted in Figure 11.15. More elaboration on how the small input voltage disturbance was generated can be found in Appendix D.4.4.

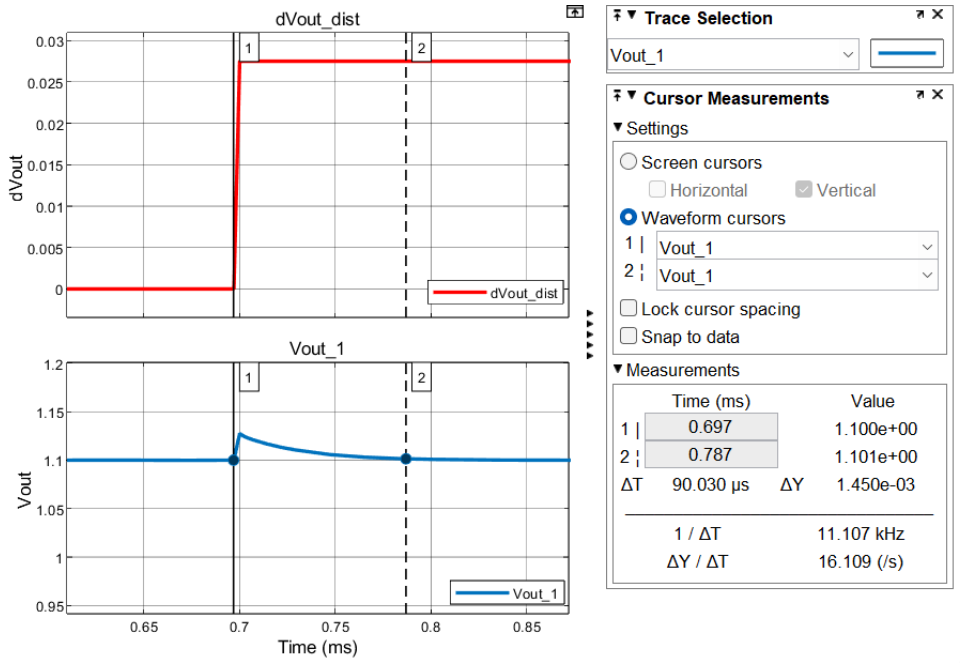


Figure 11.15: Verification of settling time under small input voltage disturbance at operating point I_{load} = 5.9 mA.

The simulation results show that the rise time, settling time and the overshoot meet the control specifications as listed in Section 11.2.2. Furthermore, the output voltage of the power converter model follows the V_{set} with e_{ss} of 0 mV as shown in Figures 11.13 to 11.15.

In the next chapter, the control strategy will be implemented in 180nm CMOS technology to verify the simulation results.

12

Implementation

In this chapter, the control system is implemented in Cadence Virtuoso. The sizes of the transistors for each component are found in Appendix D.4.5.

12.1. System-level design

The system-level design is depicted in Figure 12.1.

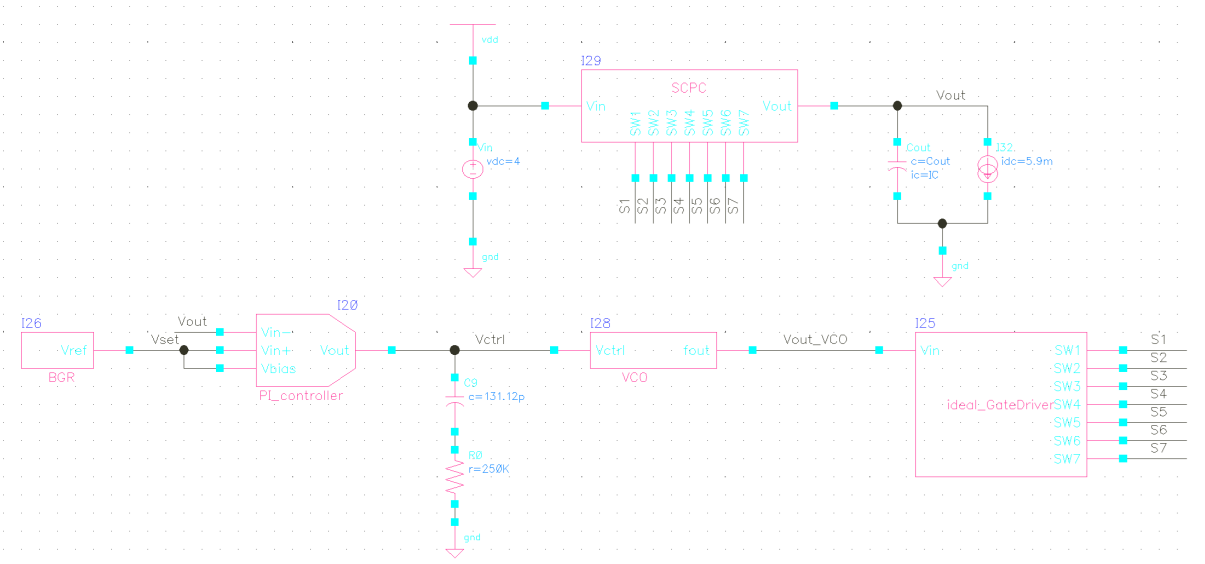


Figure 12.1: High-level design of the control loop with non-ideal SCPC.

This figure illustrates the main components: a non-ideal SC-based DC-DC converter with V_{in} of 4 V, a VCO, a PI controller, a bandgap reference (BGR) and an ideal gate driver block. The connection between V_{set} and V_{bias} supplies a voltage to the current source of the PI controller, while the other connection to V_{in+} sets the desired output voltage of the power converter to 1.1 V. The link between V_{out} of the power converter and V_{in-} provides the output voltage measurement. The PI controller computes the discrepancy between the setpoint and V_{in-} and generates a control voltage, V_{CTRL}. This voltage adjusts the oscillation frequency in the VCO, based on the VCO gain, to maintain and converge V_{out} to 1.1 V. After modifying the oscillation frequency, the ideal gate driver block divides the $V_{out,VCO}$ into two phases, which are out-of-phase and non-overlapping to prevent the shoot-through current flowing through the power switches.

12.2. Main components

12.2.1. Bandgap reference

The design of the BGR commenced with the selection between a BGR using an op-amp and a current mirror. A current-mirror BGR was selected due to the simpler design and potential lower power consumption. Subsequently, a voltage-mode BGR was chosen due to its straightforward design and the minimum required components. The bandgap reference circuit is shown in Figure 12.2 [67], [68].

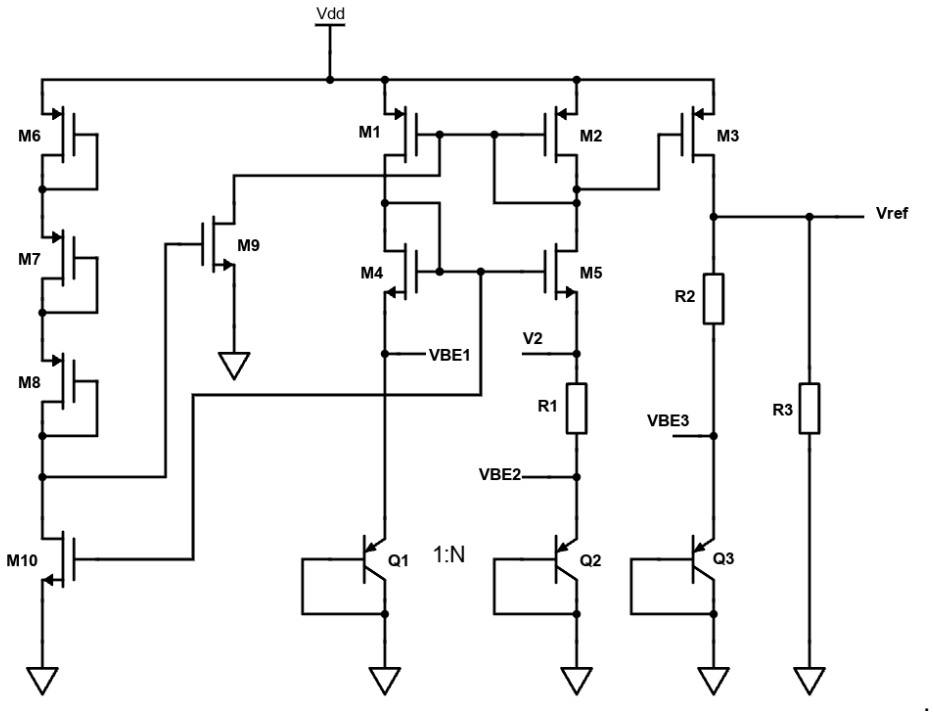


Figure 12.2: Schematic of a voltage-mode BGR.

In this schematic, MOSFETs M6 to M10 form the start-up circuit. The core is formed by Q1-Q3, R1 and R2, and R3 scales the reference voltage (V_{ref}) to 1.1 V. The V_{ref} is maintained within a temperature range between 10 °C and 50 °C. This specific temperature range is selected based on the thermoneutral zone temperature of mice, which is between 30 °C and 31 °C, different compared to humans [69], and the potential temperature in the research experiment that could affect the behavior of group-housed mice. Then Equations 12.1 to 12.3 are used, which are derived in Appendix D.4.3.

$$R_1 = \frac{V_T ln(N)}{|I_{D2}|} \tag{12.1}$$

$$R_2 = \frac{18.81 R_1}{ln(N)} \tag{12.2}$$

$$R_3 = \frac{R_2}{V_{BE3} + \left(\frac{R_2}{R_1}\right) ln(N) V_T - V_{ref}} V_{ref} \tag{12.3}$$

Initially, the power budget was set to 100 μW, assuming four current branches for the BGR: the startup-circuit current branch, two current branches for PTAT generation and one current branch for the CTAT generation. With V_{DD} at 4 V, the current branch was in the μA range. Additionally, a ratio of 1:8 (N = 8) between Q1 and Q2 was chosen for layout matching of the PNP transistors and Q3 to be the same area as Q1. The temperature coefficient (TC) of Q3 and V_{BE3} were simulated at room temperature, with values of -1.62 mV/°C and 0.753222 V, respectively, shown in Figure 12.3. Note, however, that R2, which has not yet been calculated, was neglected, and an ideal current source was used to obtain the TC of Q3 and V_{BE3}.

The TC of the thermal voltage and the thermal voltage itself were 86.14 µV/°C and 26 mV, respectively. Using these values, R_1 = 8.65 kΩ, R_2 = 78.245 kΩ, and R_3 = 604.93 kΩ. The BGR was then sized with I_d/W and g_m/I_d charts and further optimized to maintain 1.1 V within the temperature range of 10 °C and 50 °C. The optimized resistor values were found to be R_1 = 8.7 kΩ, R_2 = 69.57 kΩ, and R_3 = 786.5 kΩ. The final result is shown in Figure 12.4.

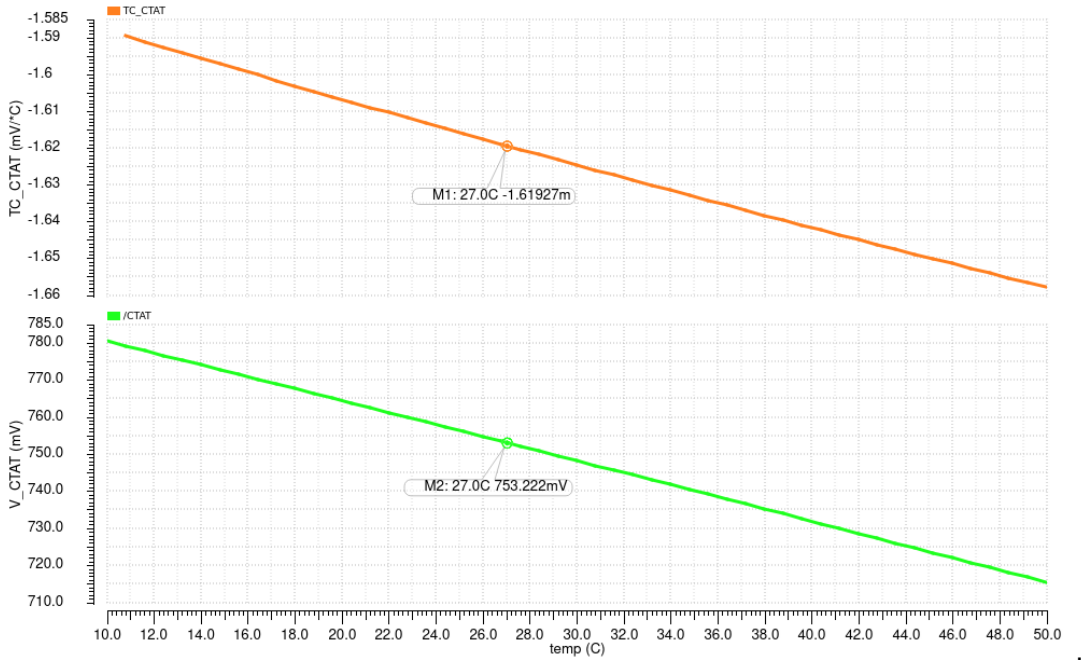


Figure 12.3: Plot for determination of V_{BE3} and temperature coefficient of CTAT.

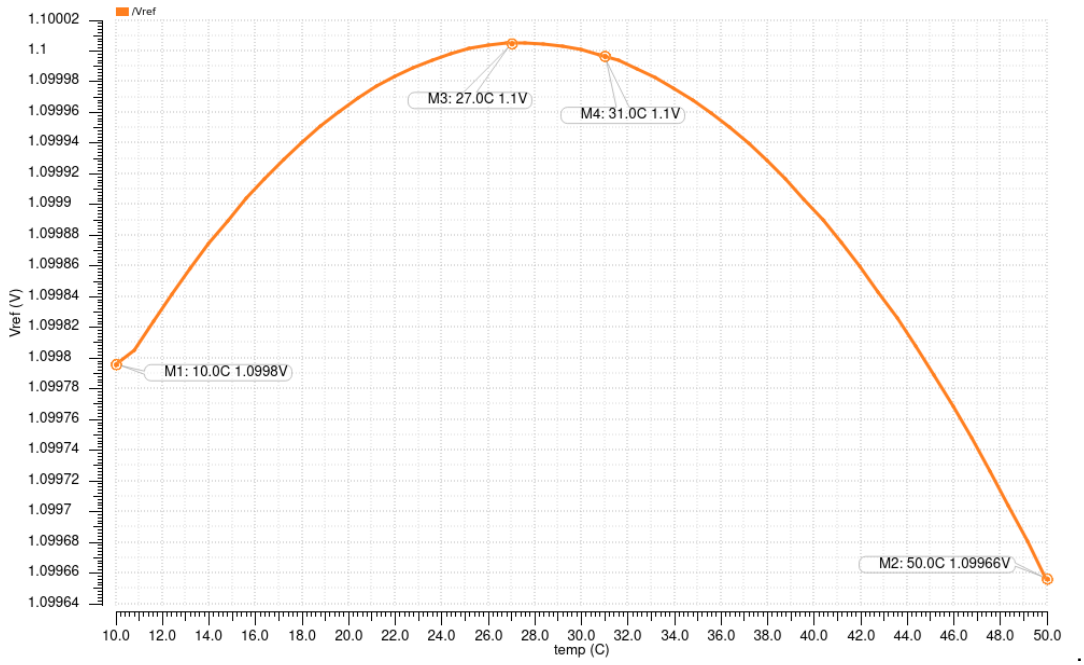
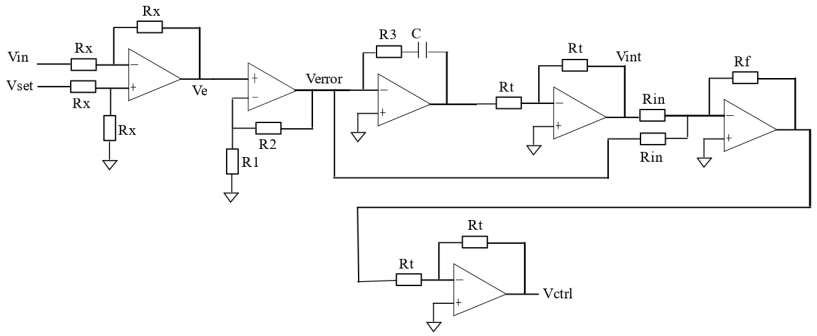


Figure 12.4: V_{ref} vs. temperature.

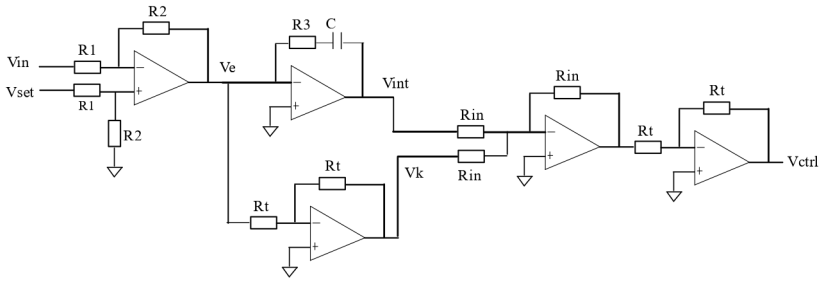
Figure 12.4 indicates that V_{ref} is 1.0998 V at 10 °C and 1.09966 V at 50 °C. Moreover, at 27 °C and 31 °C, the V_{ref} is 1.1 V.

12.2.2. Controller

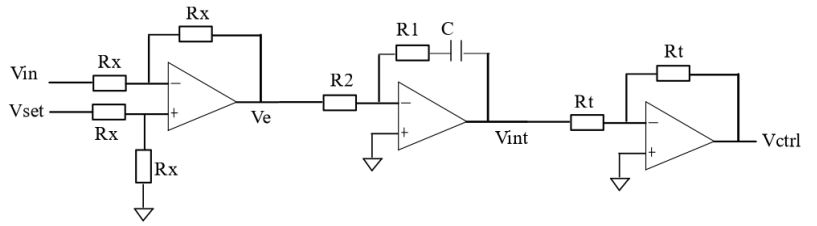
To implement the PI controller, a circuit should be designed that matches Equation 11.32. The potential solutions are shown in Figures 12.5 and 12.6.



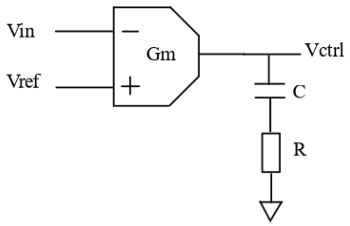
(a) Option 1 using six op-amps.



(b) Option 2 using five op-amps.

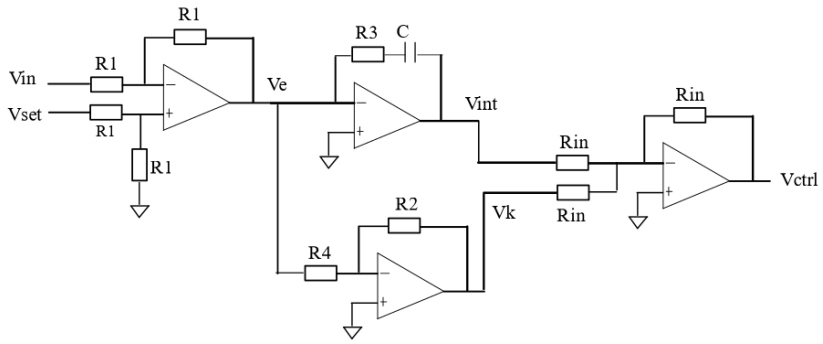


(c) Option 3 using three op-amps.

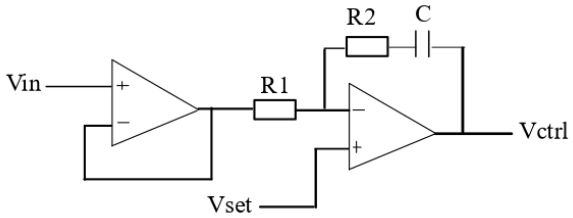


(d) Option 4 using one OTA.

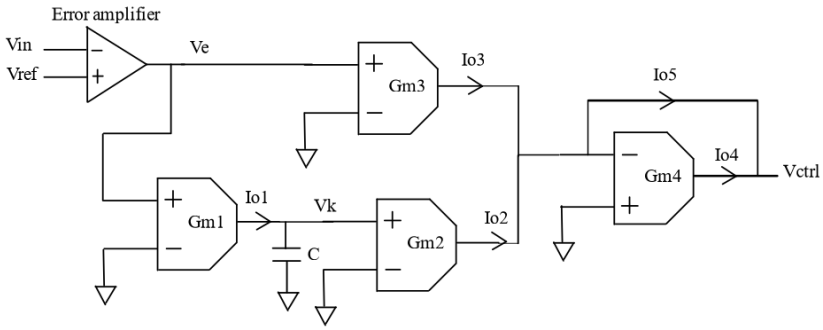
Figure 12.5: The first four potential solutions for matching the transfer function of the PI controller.



(a) Option 5 using three op-amps.



(b) Option 6 using two op-amps.



(c) Option 7 using one op-amp and four OTAs.

Figure 12.6: The last three potential solutions for matching the transfer function of the PI controller.

For selecting potential solutions, criteria were set based on the controller chip area, the potential to independently tune PI parameters (K_p and K_i or integral time constant τ_i), and the integration of the error amplifier to simplify the controller implementation. Options 1, 2, and 5 involve more than four op-amps, complicating the design and increasing chip area. Conversely, Options 3 and 6, which use op-amps, require a smaller chip area. However, they pose a challenge for potential adaptive tuning since one resistor determines both PI parameters instead of allowing independent tuning. This leaves Options 4 and 7. Option 7 requires an error amplifier and four OTAs, whereas Option 4 integrates the error amplifier using just one OTA. Additionally, Option 4 does not require input buffers, unlike Options 1, 2, 3, 5, and 7. Therefore, Option 4 is selected.

In the next step, an OTA architecture was selected based on known parameters, such as the setpoint and the supply voltage. The relevant information for the OTA design is listed below.

1. V_{DD} = 4 V (Supply available from the input of the power converter.)
2. Expected input common-mode range = 0.4 V to 2 V of the controller.
3. Output swing = 0.1 V to 2 V ⟶ based on simulation with ideal VCO and NOV circuit.
4. Power consumption of 100 μW as a starting point.
5. I_{load} = 5.9 mA with K_p = 20 and K_i = 610106.

Considering the input common-mode range and output swing restrictions posed by cascode MOSFETs in telescopic and folded-cascode OTAs, options like the 5-transistor OTA and current mirror OTA might be more suitable. These options can potentially achieve similar speeds to multi-stage OTAs without the complexity. However, for flexibility in increasing speed, a current mirror OTA is chosen as a starting point.

The current mirror OTA is shown in Figure 12.7.

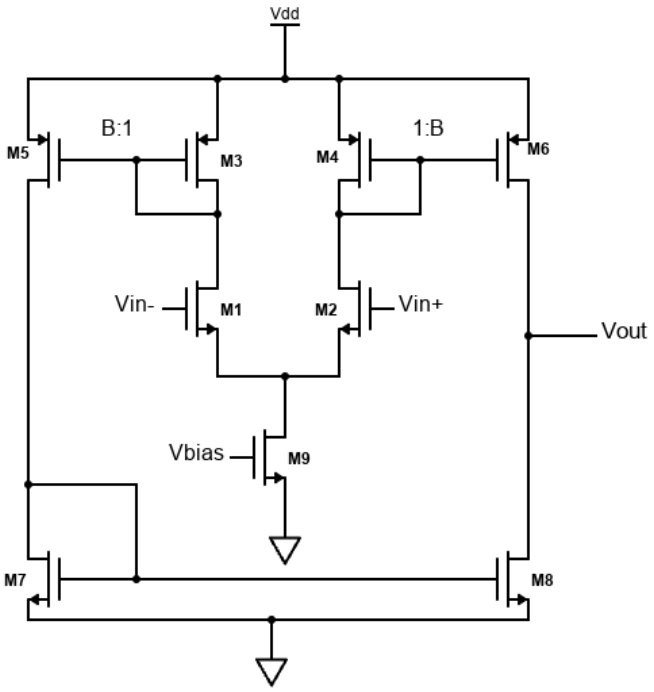


Figure 12.7: Current mirror OTA schematic.

In this schematic, B is a factor that determines the multiplication of drain current of M3 (I_{D3}) that will be copied to M5, which sets I_{D5} (similar principle applied to I_{D4} copying to I_{D6}). Initially, B = 2 was selected as a trade-off between power consumption and speed. A higher B would increase speed, but at the expense of the power consumption. V_{bias} is biased by the BGR with V_{ref} of 1.1 V to provide a tail current. The designed equations were derived by conducting circuit analysis using Figure 12.5d, which leads to Equation 12.4.

$$H_{PI,OTA}(s) = G_m R + \frac{G_m}{Cs} \tag{12.4}$$

With the aid of Equations 12.5 to 12.7, a PI controller can be designed. Equations 12.5 and 12.6 were derived from Equations 11.32 to 11.34 and 12.4.

$$G_m = \frac{K_p}{R} = \frac{\tau}{K_{tot} R \left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right)} \tag{12.5}$$

$$C = \frac{G_m}{K_i} = G_m K_{tot} \left(\tau_{des} + \frac{T_{sw}}{2} + t_{dead}\right) \tag{12.6}$$

$$G_M = B g_{m1,2} \tag{12.7}$$

In Equation 12.7, $g_{m1,2}$ denotes the transconductance of MOSFETs M1 and M2 in Figure 12.7. Since the PI parameters are already known, assuming that I_{load} = 5.9 mA, selecting R = 250 kΩ and employing the design equations, we obtain G_m = 80 µS, C = 131.12 pF, and $g_{m1,2}$ = 40 µS. Subsequently, the

current mirror OTA has been sized using g_m/I_d vs I_d/W charts. The final results are shown in Figures 12.8 and 12.9.

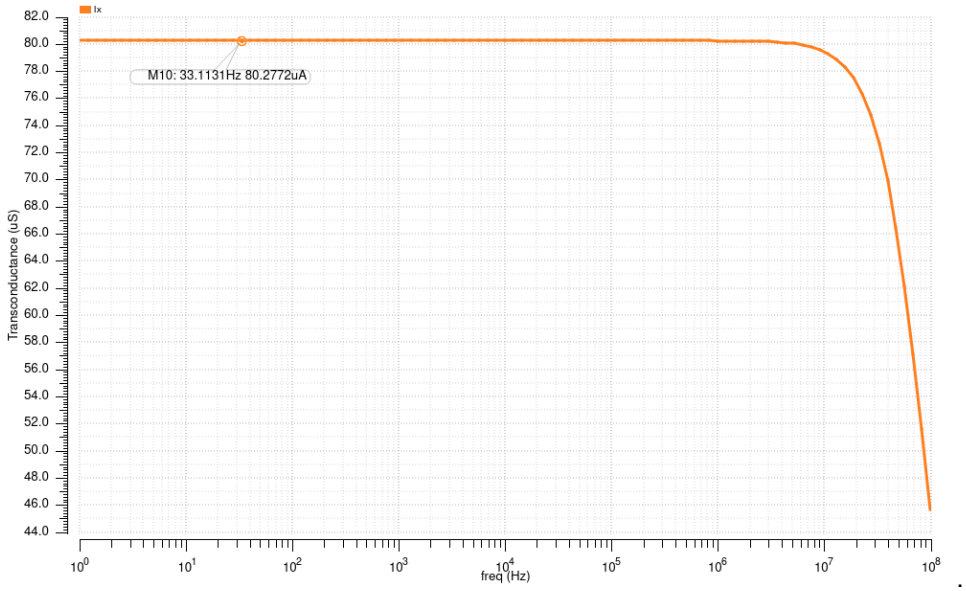


Figure 12.8: Verification of G_m of the current mirror OTA.

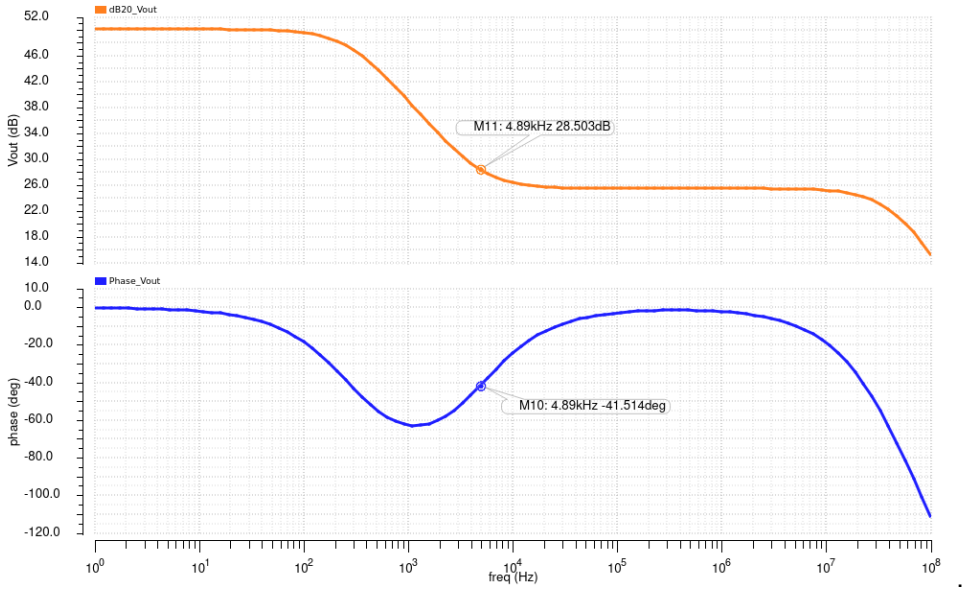


Figure 12.9: Observation of the PI controller in frequency domain.

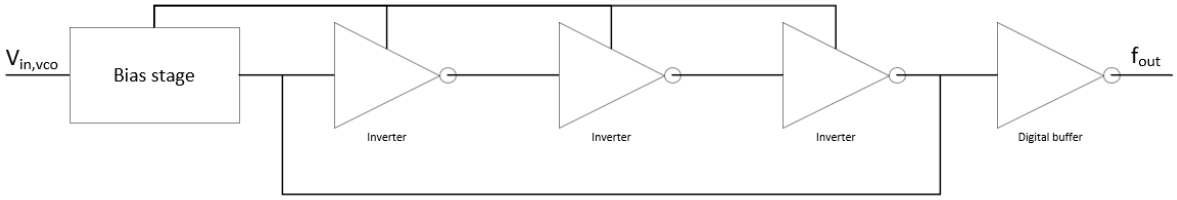
Figure 12.8 illustrates that G_m is approximately 80.2772 µS in the Bode plot of the PI controller. This value closely matches the calculated G_m of 80 µS. Furthermore, Figure 12.9 presents the Bode plot of the PI controller, which reveals a zero at a frequency slightly above 4.85 kHz. However, it also exhibits two additional poles introduced by the current mirror OTA.

12.2.3. Voltage-controlled oscillator

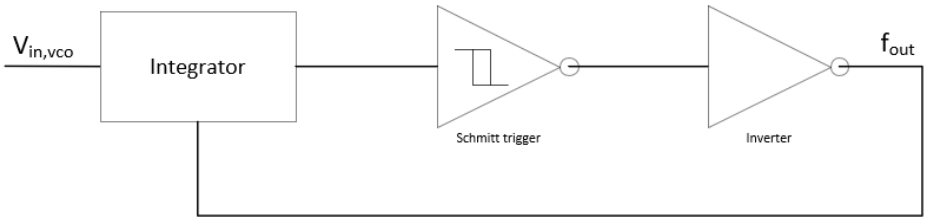
The relevant information for the VCO design was summarized, which is shown below.

1. V_{DD} = 4 V (Input voltage of the power converter)
2. V_{ref} = 1.1 V
3. Output signal of a VCO is a square wave signal (50% duty cycle).
4. Frequency range = 4 MHz to 9 MHz as a starting point, as stated in Section 11.2.1.

VCO implementation options include relaxation and ring oscillators, LC and RC oscillators, and crystal oscillators. For voltage regulation, simple control of the oscillation frequency (f_{osc}) is preferred. Crystal oscillators offer a fixed f_{osc}, while RC oscillators present control complexities due to the increased number of RC networks and feedback stages. Additionally, LC oscillators make f_{osc} control difficult because of their complex poles. In contrast, relaxation and ring oscillators have real poles, which are simpler to control. Thus, relaxation and ring oscillators are selected. A block diagram for each of the selected VCO types is shown in Figure 12.10.



(a) Block diagram of a 3-stage ring oscillator with a bias-stage, controlled by $V_{in,VCO}$.



(b) Block diagram of a relaxation oscillator, controlled by $V_{in,VCO}$.

Figure 12.10: Two different high-level implementations of a VCO.

A ring oscillator requires multiple inverter stages, leading to increased current branches, as each inverter stage needs its own current branch, resulting in higher power consumption. Furthermore, two additional current branches are required: one for the bias stage and one for the digital buffer, as shown in Figure 12.10a. In contrast, a relaxation oscillator needs three current branches to supply current to the integrator, the Schmitt trigger, and the inverter. The frequency range of the relaxation oscillator is determined by the Schmitt trigger's hysteresis, the integrator time constant, and the capacitor value. Given the required frequency range of 1 to 10 MHz, and the potential need for operation in the kHz range for the target application in the future, a relaxation oscillator is selected for its potentially reduced power consumption.

Figure 12.10b illustrates a relaxation oscillator-based VCO design. This design utilizes an integrator, Schmitt trigger, and an inverter. Another option is to replace the latter two components with two comparators and an SR-latch in cascade. However, this option would require more transistors and potentially additional bias voltages, increasing the chip area. Therefore, the VCO design was based on the block diagram, shown in Figure 12.10b.

The schematic of the VCO is shown in Figure 12.11 [70].

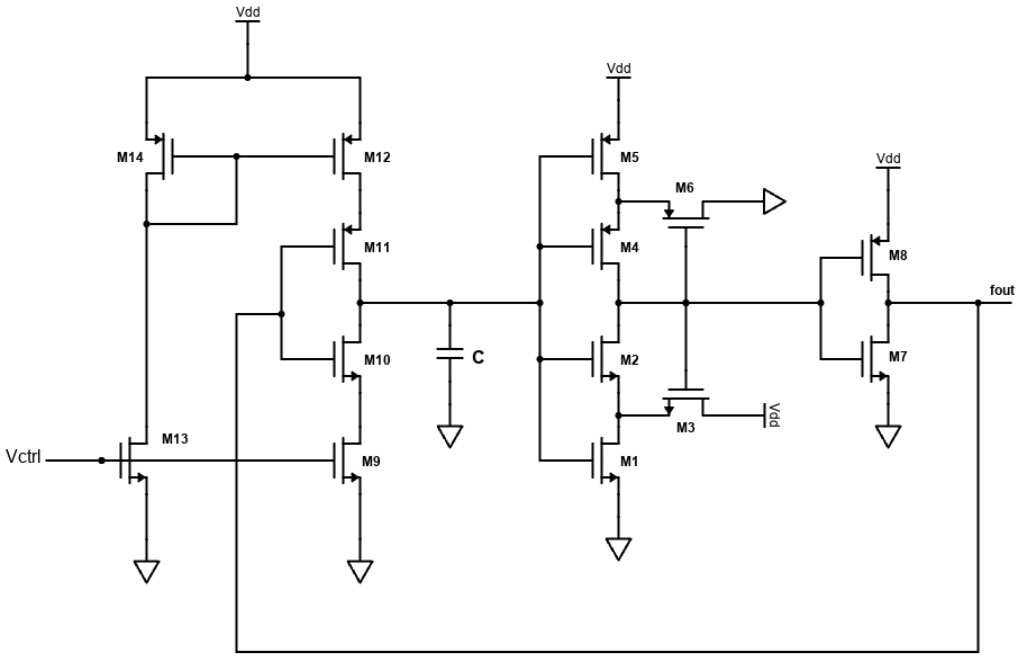


Figure 12.11: Schematic of the VCO based relaxation oscillator.

In this schematic, the integrator is formed by transistors M9-M14 and capacitor 'C'. The Schmitt trigger is implemented with transistors M1-M6, while transistors M7 and M8 function as the inverter. Initially, the inverter was sized to achieve approximately equal rise and fall times ensuring symmetrical switching behaviour and signal integrity. Next, the Schmitt trigger was sized by first selecting the upper threshold voltage V_H and the lower threshold voltage V_L to be 3 V and 1 V, respectively, as starting point. Consequently, Equations 12.8 to 12.11 were used to determine the sizes of transistors M1-M6. Equations 12.8 and 12.9 are derived in Appendix D.4.3.

$$\left(\frac{W}{L}\right)_1 = \left(\frac{V_{DD} - V_H}{V_H - V_{TH1}}\right)^2 \left(\frac{W}{L}\right)_3 \tag{12.8}$$

$$\left(\frac{W}{L}\right)_5 = \left(\frac{V_L}{V_{DD} - V_L - |V_{TH5}|}\right)^2 \left(\frac{W}{L}\right)_6 \tag{12.9}$$

$$\left(\frac{W}{L}\right)_2 \geq \max\left(\left(\frac{W}{L}\right)_1, \left(\frac{W}{L}\right)_3\right) \tag{12.10}$$

$$\left(\frac{W}{L}\right)_4 \geq \max\left(\left(\frac{W}{L}\right)_5, \left(\frac{W}{L}\right)_6\right) \tag{12.11}$$

The threshold voltages of M1 and M5, V_{TH1} and $|V_{TH5}|$, were simulated as 833 mV and 771 mV, respectively. The integrator was then sized in a similar fashion to the inverter. Each part of the VCO design was independently tested and then combined to size capacitor 'C' for a linear relationship between 4 MHz and 9 MHz in the f_{out} vs. $V_{in,VCO}$ plot. This capacitor was sized to 1.4 pF. The relevant final results are shown in Figures 12.12 and 12.13.

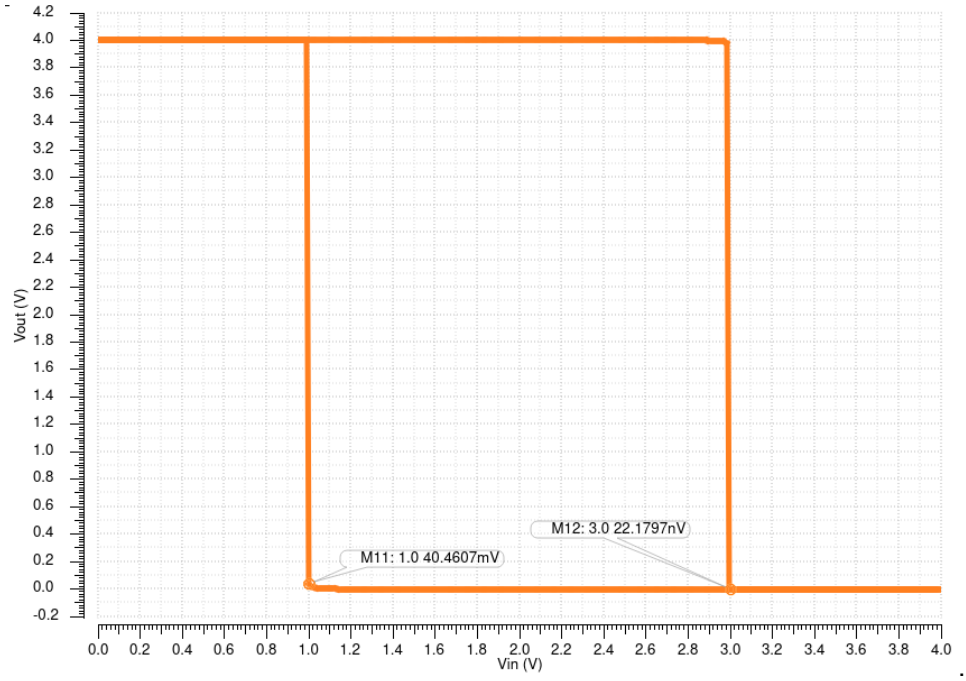


Figure 12.12: Hysteresis plot of the designed Schmitt trigger.

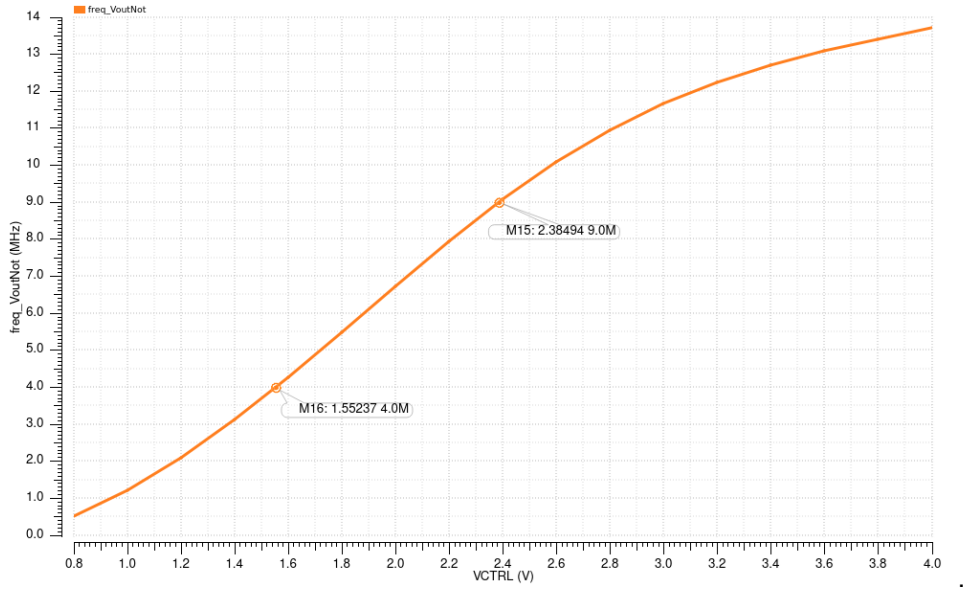


Figure 12.13: f_{out} Vs. V_{ctrl} plot.

Figure 12.12 illustrates that V_H and V_L are 3 V and 1 V, respectively, as selected earlier. Moreover, K_{VCO} was calculated to be 6 MHz/V based on Figure 12.13, which is close to the VCO gain of 5.56 MHz/V, mentioned in Section 11.2.1. The observed difference in K_{VCO} originates from the selection of the VCO's input voltage range as a starting point during the control design process, which V_{max} and V_{min} were selected as 1 V and 0.1 V, respectively, as mentioned in Section 11.2.1, while in Figure 12.13, V_{max} = 2.39 V and V_{min} = 1.55 V.

12.2.4. Non-ideal power converter and ideal gate drivers

To assess the designed and implemented control loop, a non-ideal power converter was designed, while the gate drivers were kept ideal. The ideal block of the gate driver and the power converter are illustrated in Figures 12.14 and 12.15, respectively. The gate driver consists of a NOV circuit with level shifters. In fact, level shifters are not required since we only use the input voltage of the SC-based power converter as the supply voltage. Therefore, the gain (LS_gain in Figure 12.14) of the voltage-controlled voltage source (VCVS) was set to 1 for each power switch.

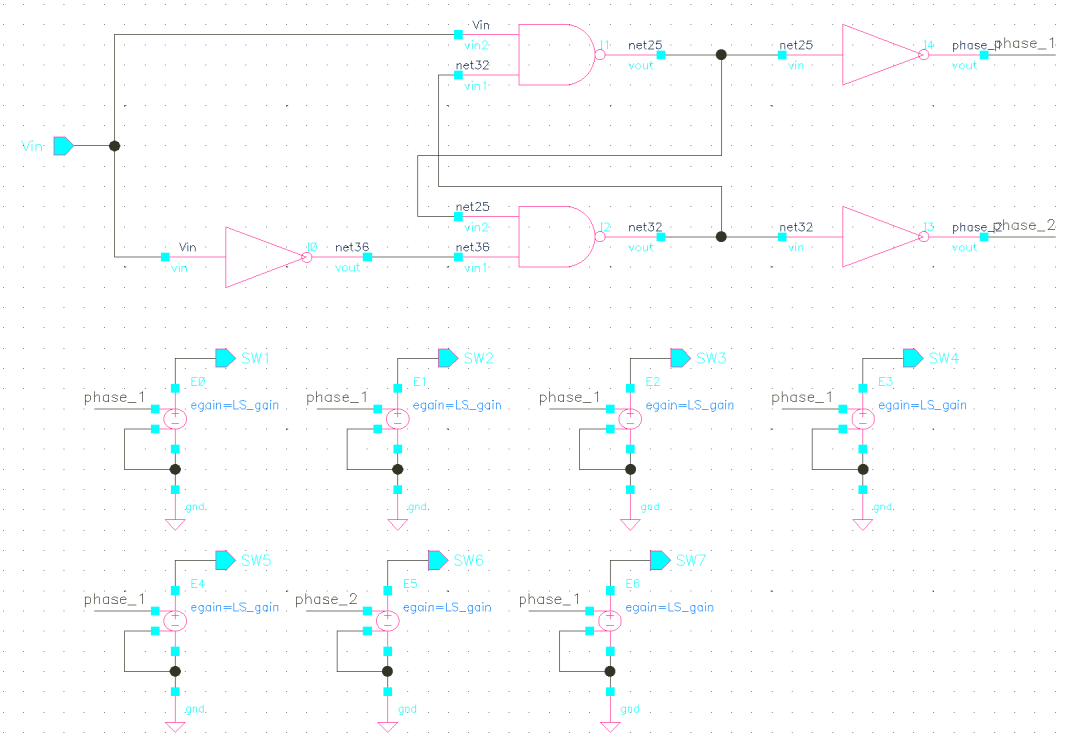


Figure 12.14: Schematic of the ideal gate driver.

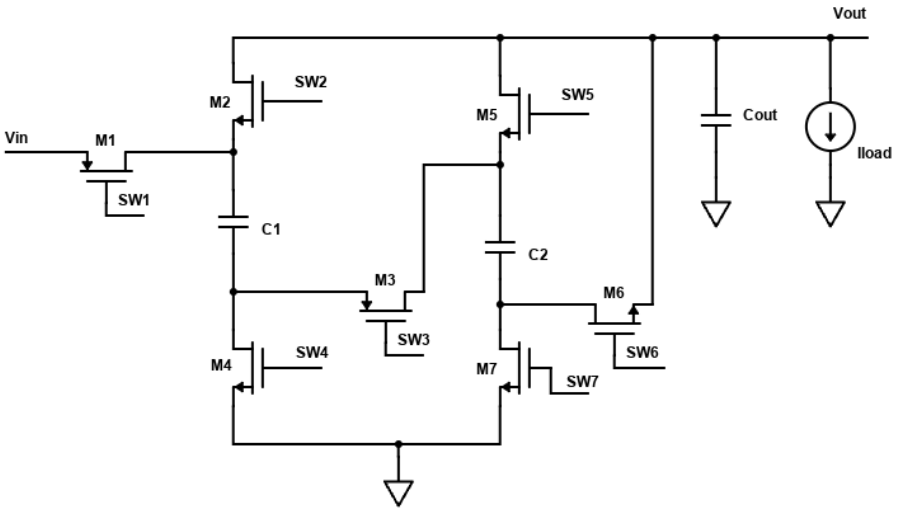


Figure 12.15: Schematic of the non-ideal SC-based power converter.

For the sizing of the power switches of the power converter, the selection of NMOS and PMOS types was explained in Section 11.1.4, along with the calculation of the optimum width for each of the power switches using the Python code, as can be found in Appendix C.3.2. The optimum width was calculated to be 290 µm. The non-ideal power converter was then simulated, and the on-resistance of M6 ($R_{on,SW6}$) was found to be 412.48 Ω, as shown in Figure 12.16. Consequently, M6 was replaced by a NMOS transistor instead of a PMOS transistor, which the PMOS transistor was suggested in Section 11.1.2. $R_{on,SW6}$ was decreased to 10.52 Ω, as illustrated in Figure 12.17.

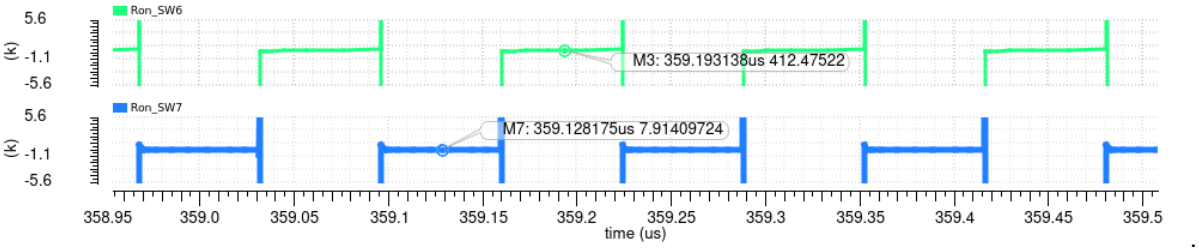


Figure 12.16: On-resistance value of MOSFET M6 as a PMOS type.

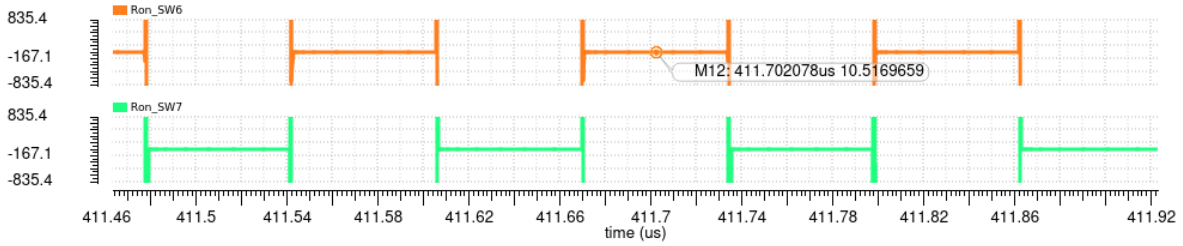


Figure 12.17: On-resistance value of MOSFET M6 as a NMOS type.

12.3. Simulation results

Along with the non-ideal power converter and the designed and implemented control loop, a transient response simulation, as well as robustness against input and load current variations, and the line and load regulation results, were generated. The transient response simulation is shown in Figure 12.18.

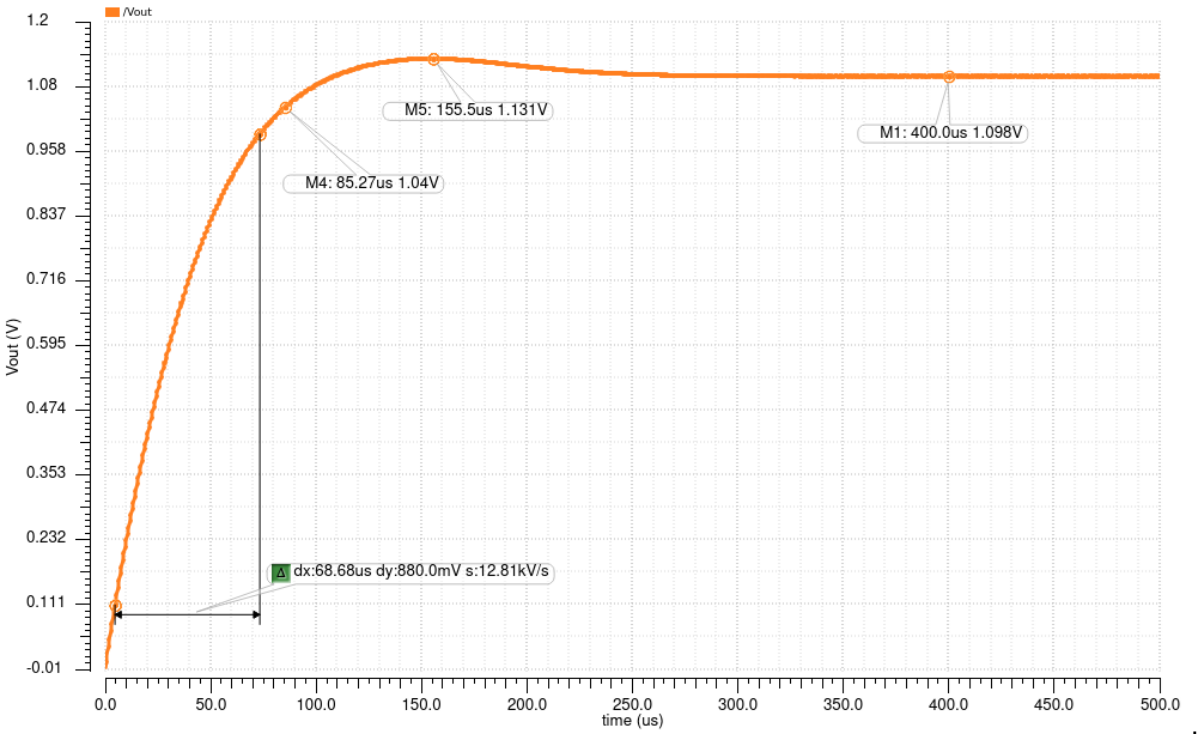


Figure 12.18: The transient response simulation plot at the output of the SC-based power converter, which V_{set} of the BGR was set to 1.1 V.

In this transient simulation plot, the V_{out} was regulated to 1.098 V. Moreover, the settling time (5.46%) was simulated to be 85.27 µs at 1.04 V (1.1 V ·(1 - 0.0546)) and the rise time is given by 68.68 µs. Furthermore, it is observed that V_{out} of the power converter has an overshoot of 3%, which is calculated by using the 'overshoot' voltage (1.131 V) and the $V_{out,nominal}$ (1.098 V).

In order to evaluate the robustness of the system with respect to load current variations, the load current was subjected to two distinct transient steps: a slow step from 5.9 mA to 5.01 mA and a fast step from 5.9 mA to 5.01 mA, as shown in Figures 12.19 and 12.20, respectively.

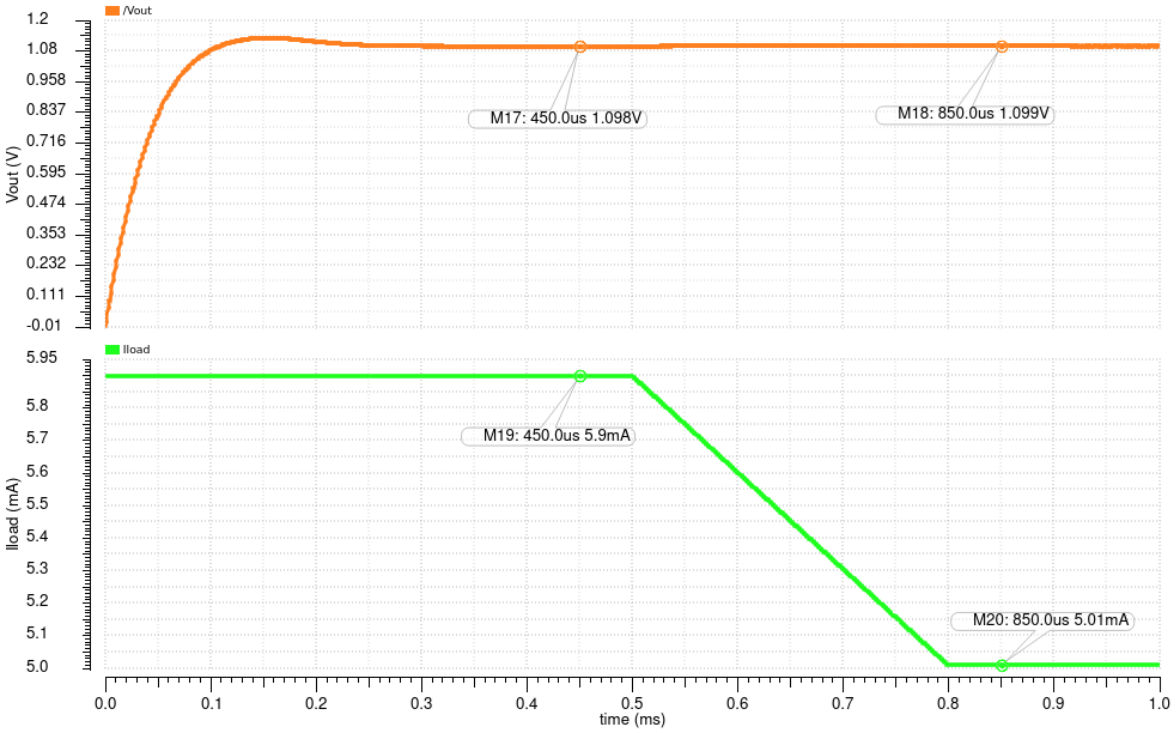


Figure 12.19: Slow step from I_{load} = 5.9 mA to I_{load} = 5.01 mA.

Figure 12.20: Fast step from I_{load} = 5.9 mA to I_{load} = 5.01 mA.

Figure 12.21 illustrates the load current step from 5.9 mA to 910 µA.

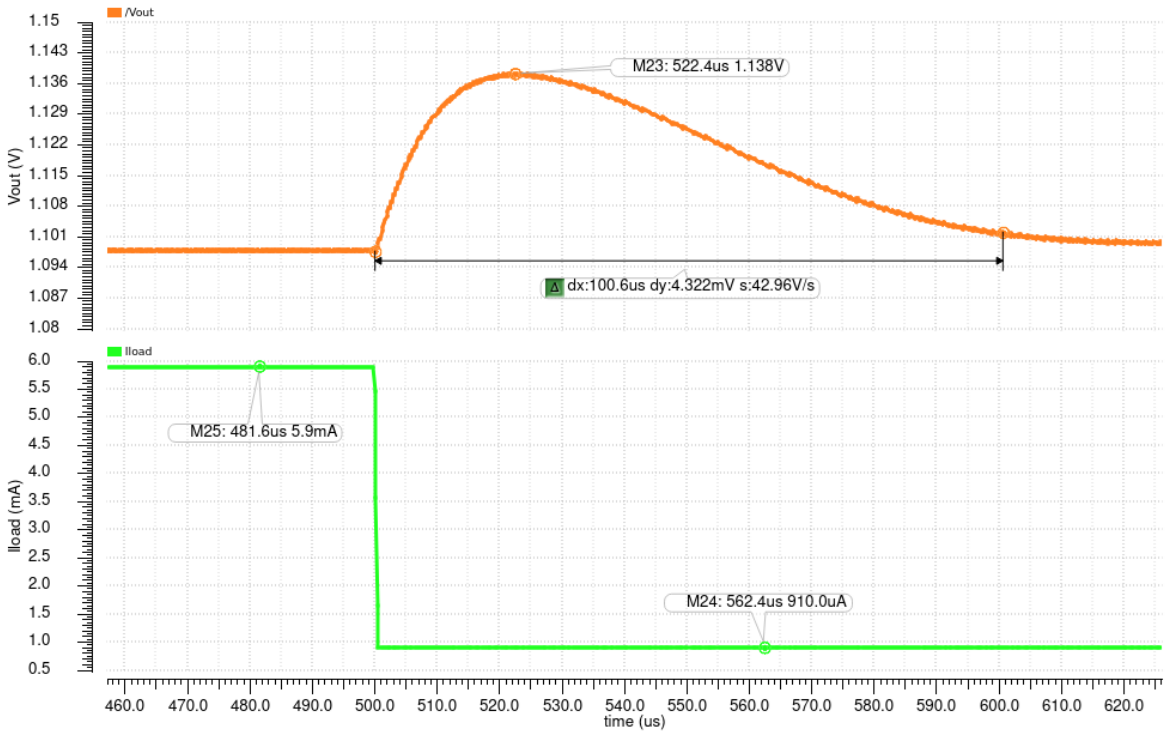


Figure 12.21: Fast step from I_{load} = 5.9 mA to I_{load} = 910 µA.

The results presented in Figures 12.19 and 12.20 demonstrate that the output voltage (V_{out}) successfully converges to its nominal value of 1.1 V for both slow and fast step changes in load current from 5.9 mA to 5.01 mA. Furthermore, as illustrated in Figure 12.21, a fast step change in load current from 5.9 mA to 910 µA leads to an initial overshoot in V_{out}, reaching a peak value of 1.138 V. However, this value remains within the acceptable tolerance of 5.46% relative to the nominal output voltage. Subsequently, V_{out} stabilizes at its desired V_{out} of 1.1 V. It is important to note that while the load recovery time, defined as the time required for V_{out} to return and remain within the 5.46% error band following a load current step change, is approximately 100.6 µs in this case, this value may vary depending on the magnitude of the load current step.

To evaluate the robustness of the power converter against input voltage variations, the input voltage was increased from 4 V to 0.1 V, as shown in Figure 12.22. Subsequently, a transient pulse, transitioning from the nominal input voltage (4 V) to 5 V and then back to 4 V, was applied to the converter, presented in Figure 12.23.

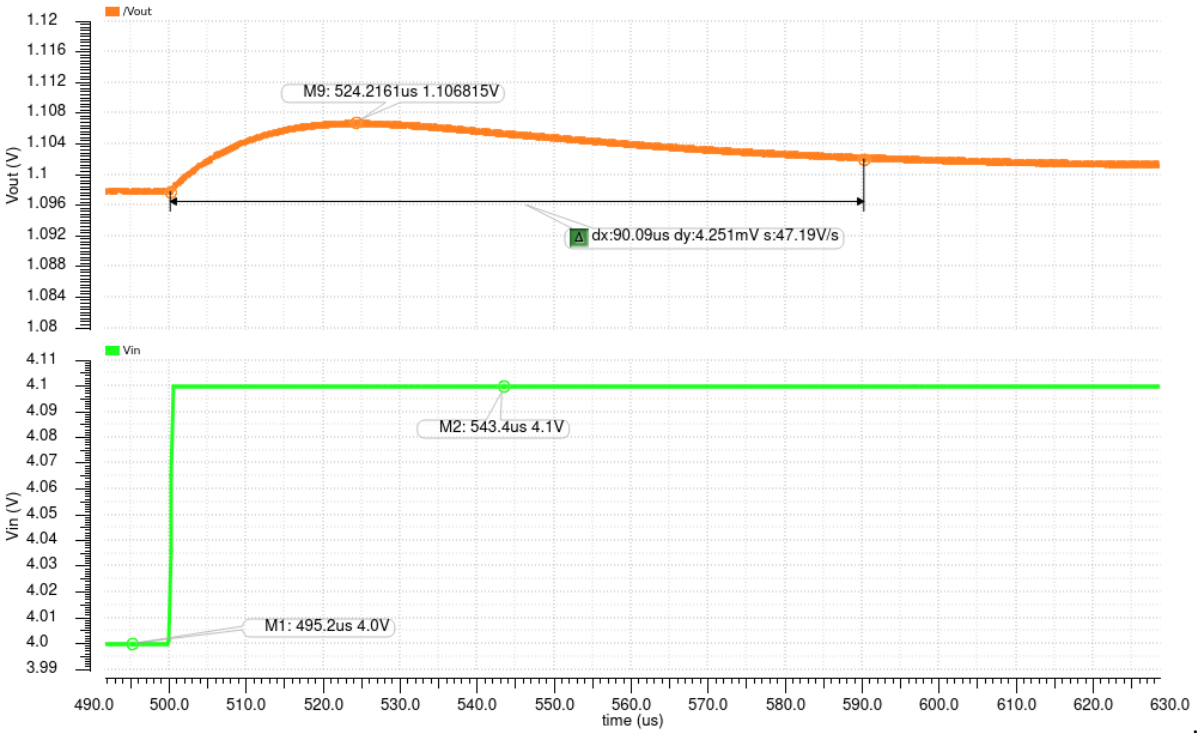


Figure 12.22: Small input voltage step from V_{in} = 4 V to V_{in} = 4.1 V.

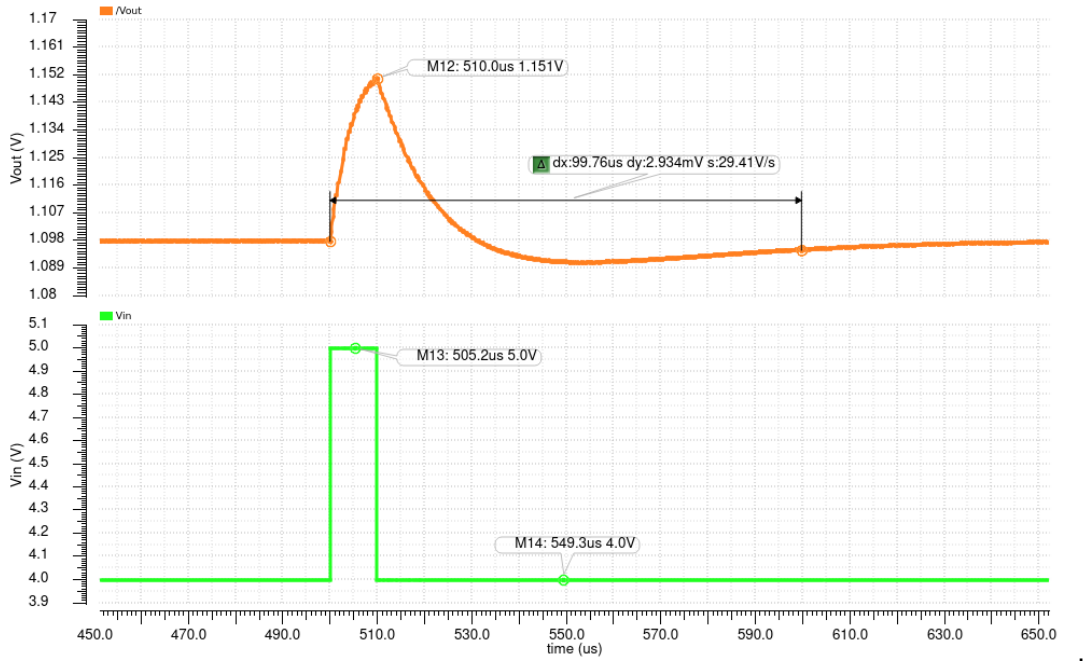


Figure 12.23: Large variation of the input voltage from step from V_{in} = 4 V to V_{in} = 5 V and back.

In a similar manner, a small input voltage step from 4 V to 4.1 V results in the output voltage remaining within the established error band. The recovery time for this scenario is approximately 90.1 µs. Conversely, when a larger input voltage variation is applied, as illustrated in Figure 12.23, both the recovery time and the peak output voltage increase. However, the latter remains below the upper limit of the error band, which is 1.16 V. Additional simulation results pertaining to the non-ideal power converter and the control loop are presented in Appendix D.4.7.

To assess the ability to maintain a 1.1 V output voltage despite variations in input voltage and load current in steady state, the line and load regulation graphs are plotted in Figures 12.24 and 12.25, respectively.

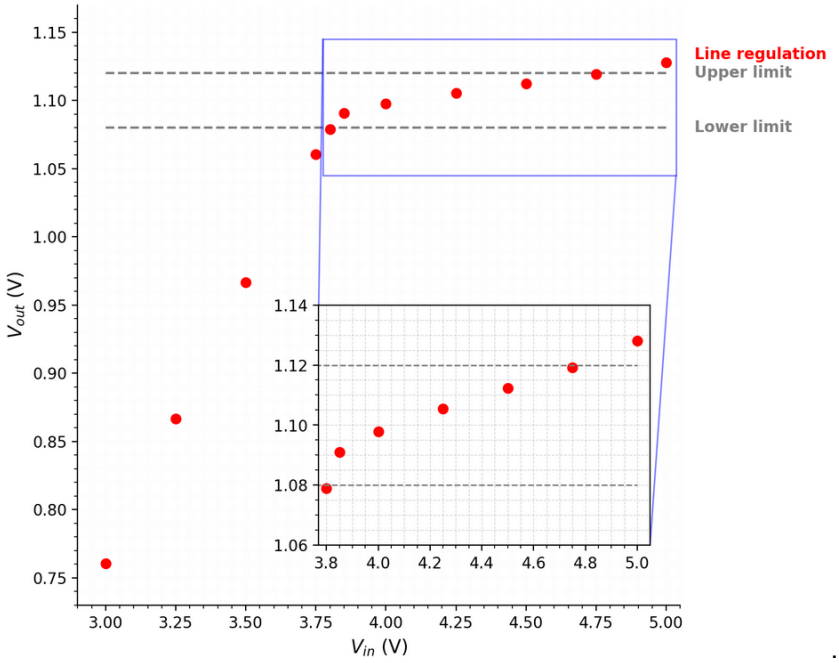


Figure 12.24: Line regulation: V_{out} vs. V_{in} plot.

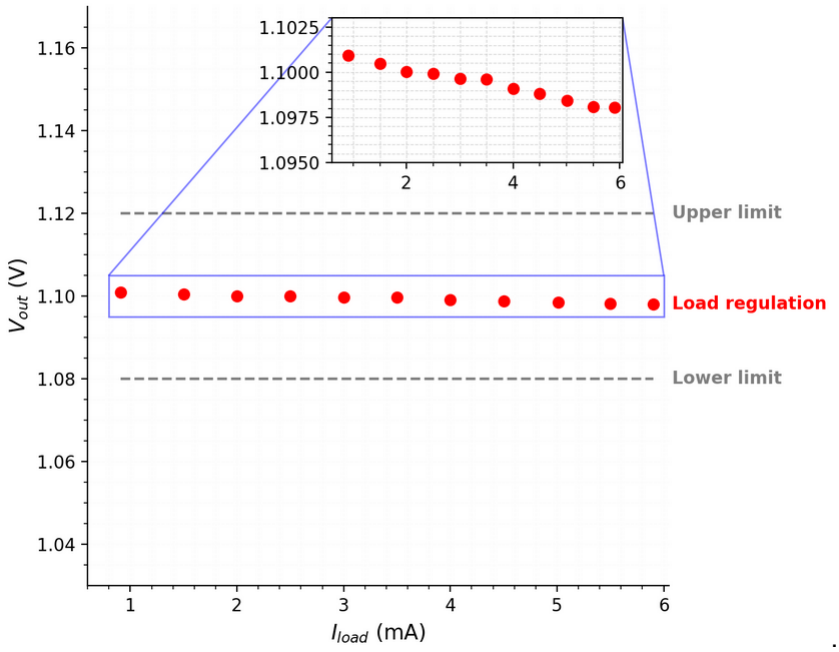


Figure 12.25: Load regulation: V_{out} vs. I_{load} plot.

Figure 12.24 depicts the variation of the output voltage (V_{out}) as the input voltage (V_{in}) is swept across a range of 3 V to 5 V, with selected data points from Appendix D.4.7. The 'upper limit' ($V_{lim,up}$ = 1.12 V) and 'lower limit' ($V_{lim,low}$ = 1.08 V) represent the boundaries established by the steady-state error specification ($e_{ss} \leq 20$ mV) as detailed in Section 11.2.2.

It is observed that V_{out} remains within the specified limits ($V_{lim,up}$ and $V_{lim,low}$) for input voltages between 3.8 V and 4.75 V. However, for input voltages below 3.8 V, the steady-state error specification is not met.

Figure 12.25 presents the load regulation characteristics, where the load current (I_{load}) is swept from 910 μA to 5.9 mA with selected measured data points, shown in Appendix D.4.7. As shown in the inset plot, V_{out} ranges between 1.0975 V and 1.1025 V for the swept load current range and stays within the voltage range of 1.08 V to 1.12 V.

12.4. Discussion of the simulation results

The verification of control specifications is summarized in Table 12.1 when I_{load} is 5.9 mA.

Table 12.1: Comparison performance between control design approach and implementation.

Specification	Given/Derived values	Control design	Implementation
Settling time (5.46%)	< 94.6 μs	90.4 μs	85.3 μs
Rise time (10% - 90%)	< 71.28 μs	68.13 μs	68.68 μs
Overshoot (OS)	≤ 5.46%	0%	3%
V_{out}	1.1 ± 0.06 V	1.1 V	1.098 V
e_{ss}	≤ 20 mV	0 mV	2 mV
V_{set} (= V_{ref})	1.1 V	1.1 V	1.1 V

This table demonstrates that both the control design utilizing the proposed power converter model and the implementation fulfill the control specifications. While the specifications of the implementation match those of the control design, the overshoot is observed to be 3% instead of the desired 0%, as seen in Figure 12.18. This deviation stems from the practical PI controller's additional low-frequency pole, which deviates from the ideal assumption of an integrator with zero frequency, as depicted in Figure 12.9. Hence, iterative tuning may be necessary if the initial design fails to meet the specifications.

Regarding robustness for input voltage and load current variations, the output voltage effectively returns to 1.1 V for both small and large input voltage steps, albeit with differing recovery times and peak voltages. However, larger input voltage variations may momentarily exceed the 5.46% error band (1.16 V) and increased recovery time, necessitating a faster control. Load current variations, particularly fast steps and for even lower load currents than I_{load} = 910 μA, increase the recovery time and the peak voltage, indicating a need for a transient controller for swift adaptation. Moreover, as shown in the control-system approach, different PI parameters are required for each I_{load}. However, the simulation results illustrate that using the PI parameters (K_p = 20 and K_i = 610106), tuned for I_{load} = 5.9 mA, the system still functions for other load currents, hence adaptive control is not required in our application.

Furthermore, while the control loop exhibits robustness in fast transient responses near input voltages of 4 V and load currents close to 5.9 mA, transient controller integration is vital for larger input voltage variations and lower load currents. Notably, the applied model-based approach lacks explicit consideration of robustness, suggesting the inclusion of an additional step in future iterations.

In addition to the line regulation, input voltages between 3.8 V and 4.75 V remain within the steady-state error voltage range (1.1 V ± 0.02 V), while input voltages lower than 3.8 V suggests the need for a multi-ratio power converter (power converter with multiple VCRs) covering this specific input voltage range, to retain close to 1.1 V. However, if the power link is well-designed such that the input voltage varies between 3.8 V and 4.75 V, as shown in Figure 12.24, a multi-ratio power converter is not required. Conversely, imposing a more stringent specification on the steady-state error (e_{ss}), such as ≤ 10 mV, then the inclusion of additional VCRs become necessary to ensure adequate coverage across the entire input voltage range of 3 V to 5 V.

Regarding the load regulation, as shown in Figure 12.25, the control loop maintains the output voltage within the steady-state error voltage range (1.1 V $\pm$ 0.02 V) across the swept load currents, making load transient response more critical.

Compared to the study in [64], the proposed power converter model in this report offers simplicity and clarity. The control-system approach used in [64] was derived based on the standard second-order system, resulting in PI parameters expressed in terms of zeta and angular frequency. Conversely, the approach in our application is written in terms of variables from the derived power converter model, of which the tuning parameters can be adapted when a variable of the power converter model changes, for example, a different flying capacitor value.

In the calculations of the power converter design, the output capacitor was assumed to be 1 μF, effectively making the ripple negligible. However, in practical SC-based DC-DC converters, ripple at the output is inevitable. Therefore, it is essential to conduct additional verification of the proposed power converter model when employing load capacitors in the range of pF to several nF before applying the control-system approach outlined in this report. Conversely, SC-based power converters with load capacitors in the μF range, typical range in power electronics for high voltages and power applications, are well-suited for the control-system approach. Notably, the sampled-data model in [64] was successfully simulated for a load capacitor of 10 nF without implementation.

The findings of our study are summarized below.

1. The control-system approach with the proposed model and practical implementation meets the derived control specifications.
2. The tailored approach assumes an ideal integrator of the PI controller, while practical PI controllers have additional poles where the dominant pole is not in the origin, thus nonzero steady-state error remains and overshoot is visible in the implemented control loop.
3. The tailored approach used in this study mainly focuses on achieving the desired time constant but does not account for robustness.
4. The PI controller in our study is tuned using variables from the power converter model, whereas the PI controller in the referenced study is tuned using zeta and angular frequency. The tuning process of the controller in our study is straightforward, intuitive, and can be adapted when a variable of the power converter model is modified.
5. The control loop functions adequately across different load currents using the tuned PI parameters of a specified load current, suggesting adaptive control is not required.
6. The control loop is robust near input voltages around 4 V and load currents close to 5.9 mA. However, for lower load currents in the range of micro-amperes, a transient controller is necessary to reduce the recovery time.

13

Conclusions and recommendations

This chapter concludes our thesis work on the design and implementation of the control loop for the targeted application. The key steps and findings are summarized, followed by the main contributions of this thesis report. Finally, potential future research directions are provided to build upon this work.

13.1. Conclusion

This report details the systematic design and implementation of a voltage regulation control loop (VRCL) for an unspecified power management unit (PMU), aimed at achieving the desired load voltage. It begins with the analysis of the PMU and load, selecting a SC-based power converter with an input voltage of 4 V, and the loads comprising the communication and control, stimulation, and recording circuitry. An ideal SC-based power converter was designed, followed by the development and verification of the plant model, which was aligned with the circuit simulations. Subsequently, control specifications were derived based on the plant model, and a tailored model-based control-system approach was formulated, with controller parameters adjusted according to the plant model variables. MATLAB results demonstrated the fulfillment of control specifications. A non-ideal SC-based power converter was then sized and integrated with the implemented control loop, consisting of a PI controller, BGR, ideal gate drivers, and a VCO, with careful selection and independent testing of the components within the control loop. Simulation results from the implementation indicated adherence to the control specifications. However, limitations include addressing robustness concerns in load and input-voltage transient responses, additional verification of load capacitors in the pF-nF range required for the derived power converter model, and discrepancies in overshoot due to the non-ideal controller behaviour.

13.2. Contributions

The main contributions of this thesis include the development of a simplified power converter model and a tailored control-system approach compared to study [64]. While similar control approach has been applied in chemical engineering, such as in studies [71] and [72], this study explores their application in SC-based power converters, particularly using an approximated continuous model. This provides an alternative approach to derive and tune the controller based on the plant-model variables rather than using zeta and angular frequency, which is less intuitive, shown in [64], offering another option for designing controllers for mouse headstage applications. The findings also suggest potential extensions to address identified limitations, contributing to the field of power electronics.

Moreover, during the design of the control loop, which relies solely on the tailored control-system approach with the derived plant model, this specific combination was verified in this study. Such a combination has not been found in the literature, as research papers on SC-based power converters with a systematic control approach are limited, while buck converters involving inductors with model-based approaches have been extensively researched. Additionally, the simulation results of the implemented control loop, provide insights into the potential use of multi-ratio power converter, transient controller, and the limitations that were not accounted for during the control design process.

13.3. Recommendations

Based on the limitations of the proposed power-converter model and the tailored control-system approach, a list for recommendations is listed below:

1. **Verification for load capacitors in the pF-nF range:** in this study, a 1 μF load capacitor was utilized for the verification of the derived power converter model. However, to ensure broader applicability, the model's validity should be further evaluated using load capacitors ranging from picofarads to several nanofarads. This broader verification would establish the extent to which the model's validity can be used for tuning of PI parameters (K_P and K_I) for a wider range of load capacitor values.

2. **Tuning process accounting for robustness:** in this study, the desired response was determined based on the expected transfer function. However, robustness was not considered. Hence, an additional step should be incorporated into the control-system approach, potentially involving a graph illustrating the relationship between the (desired) time constant and robustness. Moreover, given the involvement of a not-yet-designed power link, input voltage variation is expected to have a greater impact than the load condition. This assumption stems from the scenario where all electronics worn by group-housed mice are presumed to be active during the research experiment.

3. **Addition of the transient controller:** to reduce the recovery time for larger input voltage variations and potential load conditions, a transient controller is essential. This controller can be deployed by detecting when the input and/or output voltage surpasses the upper or lower limits of the error band. Subsequently, temporary adjustments can be made to the switching frequency to address these deviations.

4. **Plant model using charge balance analysis:** although the derived plant model is an approximation, it may be possible to refine its accuracy by employing the discrete-time charge balance method. This method was utilized in [56] to derive the transfer function, expressed as $\frac{\hat{V}_{out}(z)}{\hat{V}_{in}(z)}$. The power converter model can potentially be derived by examining the charging phase (Φ_1) and the discharging phase (Φ_2) of the SC-based power converter independently. This analysis would then be conducted under the assumption of steady-state operation, where charge conservation applies (i.e., $Q^{\Phi_1} = Q^{\Phi_2}$). Next, the fundamental relationships are utilized, which are the following: $Q = C \cdot V$ (charge, capacitance, voltage) and $Q = I \cdot t_{sw}$ (current, charge, switching period). Since this approach yields a transfer function in the z-domain, it can be converted into the s-domain before tuning the controllers.

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Appendices

A.1. Qualitative assessment

In this appendix, the symbols double plus (++), double minus (–), minus (-), and plus (+) used for the assessment of different WPT systems, as shown in Table 5.1, are briefly described for each of the parameters.

The parameters were carefully selected to ensure the ability to distinguish the selected research papers from each other, facilitating comparison and the identification of patterns and relationships. These parameters are crucial in guiding future research directions. To assess each selected research paper, the abstract, simulation, and real-time measurement results, as well as the working principle and pictures related to the coil configuration and/or block diagram of the WPT system, were thoroughly analyzed. Based on this analysis, the parameters were evaluated using the symbols to indicate the performance of each WPT system. The parameters are shown below with tables consisting of the symbols and the corresponding description.

Parameter: Cage size

Table 1: The meaning of symbols of cage size.

Symbol	Meaning
++	The cage size is large enough to put more than three rodents without restrictions of animal's movements.
- -	The space per rodent is too small with no space for animal's movement.
+	The cage size is appropriate for the specific animal species and allows for adequate movement and exploration.
-	The cage size may be small for three rodents, restricting the animals' movements and causing discomfort.

The assessment of the 'cage size' parameter is based on the housing of at least three rodents. This decision was made because the cage dimensions vary across different research papers, making it challenging to directly compare them. By selecting three rodents as the minimum housing requirement, it becomes possible to assess whether the cage size provides enough space for the rodents to move freely.

Common research papers for freely moving animals in homecages, only one or two rodents are used to obtain real-time measurements for testing their designed WPT system for wireless power supply in homecages. However, by increasing the number of rodents to three, it allows for a more realistic evaluation of the system's performance in a multi-rodent environment.

Parameter: Lateral Robustness

Table 2: The meaning of symbols of lateral robustness.

Symbol	Meaning
++	The coil configuration provides sufficient power, including the edges of the cage, to guarantee continuous power supply in the entire cage.
- -	The coil configuration does not provide enough power for the entire cage, only for a particular area.
+	The coil configuration provides minimum power during animal's movements, even where blank spots are located.
-	The coil configuration cannot provide minimum power during animal's movements in a specific area for a certain period of time.

The 'Lateral Robustness' parameter (X and Y directions) tells us how sufficient power is supplied to the electronics worn by the rodents during movement, for instance, when they move from the middle to the left of the homecage.

Parameter: Vertical Robustness

Table 3: The meaning of symbols of vertical robustness.

Symbol	Meaning
++	The coil configuration provides enough power when an animal is not on their feet even with increasing distance up to 16 cm.
- -	The coil configuration cannot provide enough power when an animal is not on their four feet.
+	The coil configuration provides enough power when an animal is not on their feet up to 8 cm.
-	The coil configuration can provide enough power when an animal is not on their four feet, but with a low PTE.

The 'Vertical Robustness' parameter (Z direction) tells us how sufficient power is supplied to the electronics worn by the rodents when the rodents stand up, which increases the distance between the source and target in the WPT system and, in turn, decreases the PTE. To assess the WPT system, the maximum distance between the source and target is set to 16 cm as this is the maximum distance that has been found in the literature study related to WPT system for homecages. Furthermore, 8 cm is selected for the intermediate distance to distinguish the boundaries between + and ++.

Parameter: Angular Robustness

Table 4: The meaning of symbols of angular robustness.

Symbol	Meaning
++	The WPT system demonstrates immunity to angular misalignments without large misalignments.
- -	The WPT system's performance is affected by major angular misalignments, leading to a significant decrease in PTE.
+	The WPT system demonstrates immunity to angular misalignments, meaning it can maintain efficient power transfer even when the transmitter and receiver coils are slightly misaligned.
-	The WPT system's performance is affected by minor angular misalignments, leading to a decrease in PTE.

The 'Angular Robustness' parameter tells us how sufficient the power can be transferred to the receiver when it is rotated up to 90°.

Parameter: Transmission range

Table 5: The meaning of symbols of transmission range.

Symbol	Meaning
++	Excellent transmission range, covers a wide distance with stable and reliable PTE.
- -	Poor transmission range, PTE degrades rapidly with even minor increases in distance.

Continued on next page

Table 5: The meaning of symbols of transmission range. (Continued)

+	Good transmission range, moderate drop-off in efficiency over longer distances, but still reliable.
-	Limited transmission range, significant drop-off in efficiency beyond a certain distance.

This parameter describes how far the source can transmit power to the receiver with a degree of reduction in PTE. For instance, a good transmission range with a moderate drop-off of PTE over a longer distance is considered as '+'. On the contrary, a limited transmission range with a significant drop-off of PTE at a certain distance is considered as '-'.

Parameter: Power transfer efficiency

Table 6: The meaning of symbols of power transmission efficiency.

Symbol	Meaning
++	The WPT system demonstrates exceptionally high PTE. It efficiently transfers power from the transmitter to the receiver coils, resulting in minimal energy loss, which is near-optimal.
- -	The WPT system shows poor PTE. It experiences significant energy loss during power transfer and is not suitable for practical use and requires substantial improvements.
+	The WPT system exhibits good PTE. It effectively transfers power from the transmitter to the receiver coils, with relatively low energy loss and is considered satisfactory for the targeted application.
-	The WPT system has suboptimal PTE. It experiences notable energy loss during power transfer. Improvements should be made to enhance the link efficiency.

This parameter describes how well the PTE can be achieved in a certain coil configuration by examining whether improvements should be made or if it is satisfactory for the intended application. For the assessment, a distance of 3 cm is selected as the research papers commonly provide results for this specific distance. Some research papers provide a figure sweeping the height (distance between the source and target) against the PTE to analyze the performance of the WPT system. Furthermore, for this assessment, it is assumed that the receiver is located at a place where the receiver and transmitter are aligned for the maximum achieved PTE.

Parameter: Complexity

Table 7: The meaning of symbols of system complexity.

Symbol	Meaning
++	The WPT system is exceptionally simple and straightforward, with minimal components and requirements. Maintenance is seldom.
- -	The WPT system has a high level of complexity, which could lead to potential challenges in implementation and maintenance.
+	The WPT system is straightforward, easy to implement, and requires minimal additional components or adjustments. Maintenance may be needed, but not necessary.
-	The WPT system has some level of complexity, involving multiple components or intricate designs.

The 'Complexity' parameter describes how intricate the designed WPT system is in terms of implementation. A complex design involving a significant number of components, such as fourteen control modules, may require frequent maintenance and increase the space needed for the WPT system.

Parameter: Safety features

Table 8: The meaning of symbols of safety features.

Symbol	Meaning
++	The WPT system demonstrates an exceptional level of safety features, ensuring the well-being of animals and minimizing potential health risks.
- -	The WPT system lacks essential safety measures, posing significant risks to the animals or users.
+	The WPT system incorporates robust safety features to prevent risks such as overheating, over- and undercharging or EMI.
-	The WPT system has some safety features but lacks comprehensive protection against potential risks.

This parameter is used to assess to what extent the WPT system guarantees safety such as electromagnetic interference and under- and overcharging of the receiver.

B.2. Ideal SC-based DC-DC converter

B.2.1. Derivation topology dependent factors in SSL and FSL

A derivation of K_{SSL} and K_{FSL} are derived for the following topologies: Series-Parallel, Dickson, Fibonacci and Ladder. This is done following the procedure of [54]. The following bullet points are assumed and considered before the derivation:

1. The charge that flows in one phase, ϕ_1 or ϕ_2, must be equal and opposite to the charge flow in the other phase.
2. I_{out} = 0 A.
3. Steady-state operation.
4. The charge flowing through each component, switch or capacitor, is taken as the absolute value.
5. Duty cycle is 50%.
6. C_{out} » C_{fly}.
7. The input charge is q_{in} starting from V_{in}.
8. Let q_{Cout} be the charge of the output capacitor and q_{out} the charge to the load.
9. $C_i = C_{i+1} = C_{i+N} = C_{fly} \longrightarrow C_i = k_{C,i}C_{fly} \longrightarrow k_{C,i} = 1$.
10. $R_i = R_{i+1} = R_{i+N} = R_{on} \longrightarrow R_i = k_{R,i}R_{on} \longrightarrow k_{R,i} = 1$.

We use the following equations to calculate K_{SSL} and K_{FSL} taking into account the listed assumptions and considerations.

$$K_{SSL} = \sum_{i=1}^{n_c} \frac{a_{C,i}^2}{k_{C,i}} = \sum_{i=1}^{n_c} a_{C,i}^2$$

$$K_{FSL} = \sum_{i=1}^{n_{swi}} \frac{a_{R,i}^2}{D_i} k_{R,i} = 2 \sum_{i=1}^{n_{swi}} a_{R,i}^2$$

$$q_{out} = q_{out}^1 + q_{out}^2$$

$$a_{c,i} = a_{S,i} = \frac{q_i}{q_{out}}$$

q^1_{out} denotes the output charge in phase 1 and q^2_{out} in phase 2. Moreover, the switch and capacitor multiplier ($a_{R,i}$ and $a_{C,i}$) is the fraction of the output charge that flows through the switch and flying capacitor, respectively, which is the ratio between the charge of capacitor or switch i and the output charge.

Series-Parallel topology

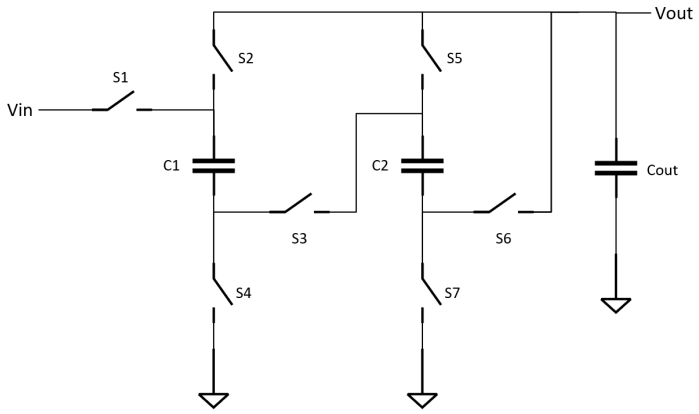

Figure 1: 3:1 Series-Parallel Topology.

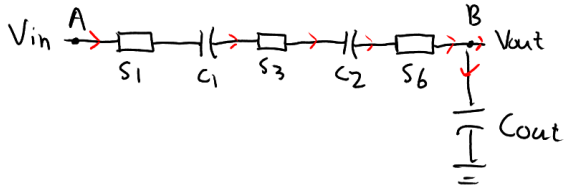

Figure 2: Phase 1 of Series-Parallel topology.

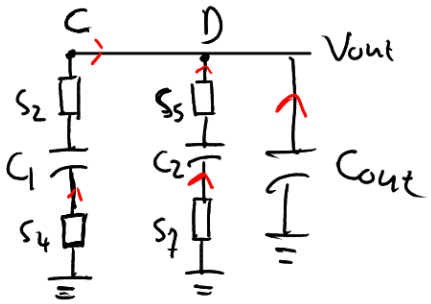

Figure 3: Phase 2 of Series-Parallel topology.

$$\text{node A } (\phi_1) : q^1_{C1} = q_{in}$$
$$\text{node C } (\phi_2) : |-q^2_{C1}| = q_{in}$$
$$\text{node B } (\phi_1) : q^1_{C1} = q^1_{C2} = q_{in} \text{ and } q^1_{out} = q_{in} - q_{Cout}$$
$$\text{node D } (\phi_2) : |-q^2_{C1}| + |-q^2_{C2}| = 2q_{in} \text{ and } q^2_{out} = 2q_{in} + |-q_{Cout}|$$
$$q_{out} = q^1_{out} + q^2_{out} = q_{in} - q_{Cout} + 2q_{in} + q_{Cout}$$
$$q_{out} = 3q_{in} \longrightarrow q_{in} = \frac{1}{3} q_{out}$$

$$q_{C1} = \frac{1}{3}q_{out},\ q_{C2} = \frac{1}{3}q_{out},\ q_{out}^{1} = \frac{1}{3}q_{out},\ q_{out}^{2} = \frac{2}{3}q_{out}$$

$$a_C = [a_{C1}\ a_{C2}] = \left[\frac{1}{3}\ \frac{1}{3}\right]$$

$$a_S = [a_{S1}\ a_{S2}\ a_{S3}\ a_{S4}\ a_{S5}\ a_{S6}\ a_{S7}] = \left[\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\right]$$

$$K_{SSL} = \sum_{i=1}^{n_c} a_{C,i}^2 = \left(\frac{1}{3}\right)^2 + \left(\frac{1}{3}\right)^2 = 0.222$$

$$K_{FSL} = 2\sum_{i=1}^{n_{swi}} a_{S,i}^2 = 2 \cdot 7\left(\frac{1}{3}\right)^2 = 1.56$$

Dickson topology

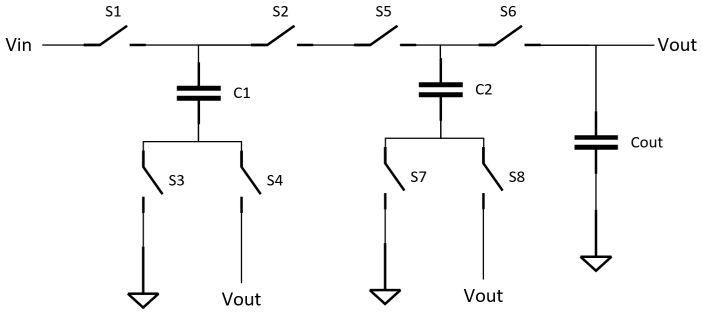

Figure 4: 3:1 Dickson Topology.

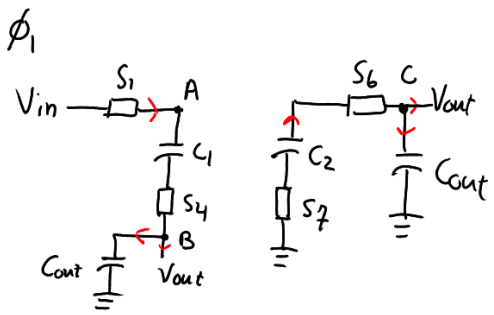

Figure 5: Phase 1 of Dickson topology.

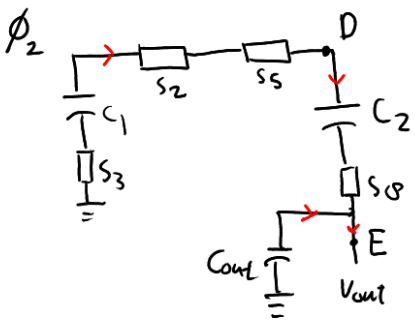

Figure 6: Phase 2 of Dickson topology.

$$\text{node A } (\phi_1): q_{C1}^1 = q_{in}$$
$$\text{node D } (\phi_2): |-q_{C1}^2| = q_{C2}^2 = q_{in}$$
$$\text{node B } (\phi_1): q_{out}^1 = q_{C1}^1 - q_{Cout} = q_{in} - q_{Cout}$$
$$\text{node C } (\phi_1): q_{out}^1 = |-q_{C2}^1| - q_{Cout} = q_{in} - q_{Cout} \rightarrow q_{out}^1 = 2q_{in} - 2q_{Cout}$$
$$\text{node D and E } (\phi_2): |-q_{C1}^2| = q_{C2}^2 \rightarrow q_{out}^2 = q_{C2}^2 + |-2q_{Cout}| = q_{in} + |-2q_{Cout}|$$
$$q_{out} = q_{out}^1 + q_{out}^2 = 2q_{in} - 2q_{Cout} + q_{in} + |-2q_{Cout}|$$
$$q_{out} = 3q_{in} \rightarrow q_{in} = \frac{1}{3}q_{out}$$

$$q_{C1} = \frac{1}{3}q_{out},\ q_{C2} = \frac{1}{3}q_{out},\ q_{out}^1 = \frac{2}{3}q_{out},\ q_{out}^2 = \frac{1}{3}q_{out}$$
$$a_C = [a_{C1}\ a_{C2}] = \left[\frac{1}{3}\ \frac{1}{3}\right]$$
$$a_S = [a_{S1}\ a_{S2}\ a_{S3}\ a_{S4}\ a_{S5}\ a_{S6}\ a_{S7}\ a_{S8}] = \left[\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\right]$$

$$K_{SSL} = \sum_{i=1}^{n_c} a_{C,i}^2 = \left(\frac{1}{3}\right)^2 + \left(\frac{1}{3}\right)^2 = 0.222$$
$$K_{FSL} = 2\sum_{i=1}^{n_{swi}} a_{S,i}^2 = 2 \cdot 8\left(\frac{1}{3}\right)^2 = 1.78$$

Fibonacci topology

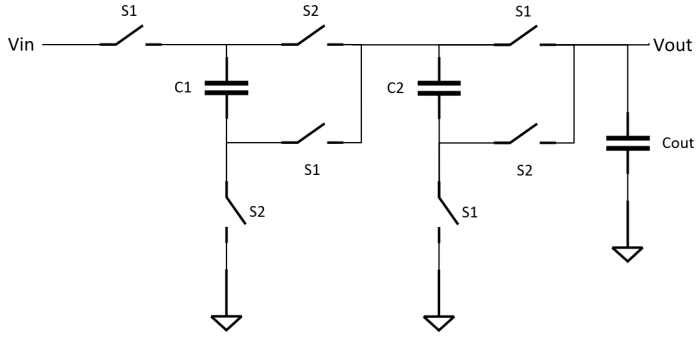

Figure 7: 3:1 Fibonacci Topology.

$$\text{node A } (\phi_1): q_{C2}^1 = q_{in}$$
$$\text{node C } (\phi_2): |-q_{C2}^2| = q_{C1}^2 = q_{in}$$
$$\text{node B } (\phi_1): q_B{}^1 = q_{C2}^1 + |-q_{C1}^1| = 2q_{in}$$
$$\text{node E } (\phi_1): q_{out}^1 = q_B^1 - q_{Cout} = q_{C2}^1 + |-q_{C1}^1| - q_{Cout} = 2q_{in} - q_{Cout}$$
$$\text{node D } (\phi_2): q_{out}^2 = q_{C1}^2 + |-q_{Cout}| = q_{in} + |-q_{Cout}|$$
$$q_{out} = q_{out}^1 + q_{out}^2 = 2q_{in} - q_{Cout} + q_{in} + |-q_{Cout}|$$
$$q_{out} = 3q_{in} \rightarrow q_{in} = \frac{1}{3}q_{out}$$

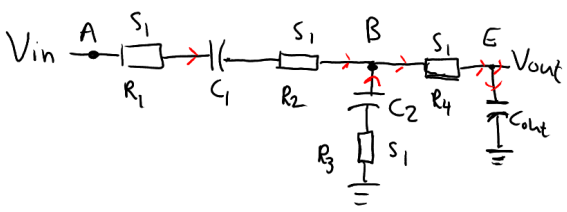

Figure 8: Phase 1 of Fibonacci topology.

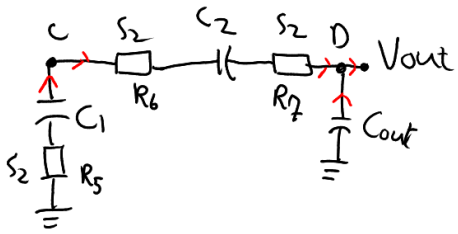

Figure 9: Phase 2 of Fibonacci topology.

$$q_{C1} = \frac{1}{3}q_{out},\ q_{C2} = \frac{1}{3}q_{out},\ q_{out}^{1} = \frac{2}{3}q_{out},\ q_{out}^{2} = \frac{1}{3}q_{out}$$

$$a_C = [a_{C1}\ a_{C2}] = \left[\frac{1}{3}\ \frac{1}{3}\right]$$

$$a_S = [a_{S1}\ a_{S2}\ a_{S3}\ a_{S4}\ a_{S5}\ a_{S6}\ a_{S7}] = [a_{R1}\ a_{R2}\ a_{R3}\ a_{R4}\ a_{R5}\ a_{R6}\ a_{R7}] = \left[\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\right]$$

$$K_{SSL} = \sum_{i=1}^{n_c} a_{C,i}^2 = \left(\frac{1}{3}\right)^2 + \left(\frac{1}{3}\right)^2 = 0.222$$

$$K_{FSL} = 2\sum_{i=1}^{n_{swi}} a_{S,i}^2 = 2 \cdot \left(6\left(\frac{1}{3}\right)^2 + \left(\frac{2}{3}\right)^2\right) = 2.22$$

Ladder topology

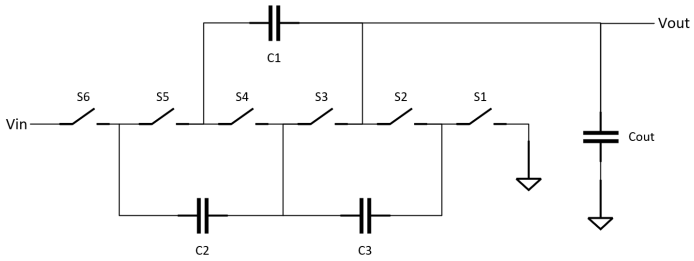

Figure 10: 3:1 Ladder Topology.

$$\text{node A } (\phi_1) : q_{C2}^{1} = q_{in}$$

$$\text{node D } (\phi_2) : |-q_{C2}^{2}| = q_{C1}^{2} = q_{in}$$

$$\text{node B } (\phi_1) : q_{C3}^{1} = q_{C2}^{1} + |-q_{C1}^{1}| = 2q_{in}$$

$$\text{node E } (\phi_2) : q_{E}^{2} = q_{C1}^{2} + (|-q_{C3}^{2}| - |-q_{C2}^{2}|) = q_{in} + (2q_{in} - q_{in}) = 2q_{in}$$

$$\text{node C } (\phi_1) : q_{out}^{1} = (q_{C3}^{1} - |-q_{C1}^{1}|) - q_{Cout} = q_{in} - q_{Cout}$$

$$\text{node F } (\phi_2) : q_{out}^{2} = q_{E}^{2} + |-q_{Cout}| = 2q_{in} + |-q_{Cout}|$$

$$q_{out} = q_{out}^{1} + q_{out}^{2} = q_{in} - q_{Cout} + 2q_{in} + |-q_{Cout}|$$

$$q_{out} = 3q_{in} \longrightarrow q_{in} = \frac{1}{3}q_{out}$$

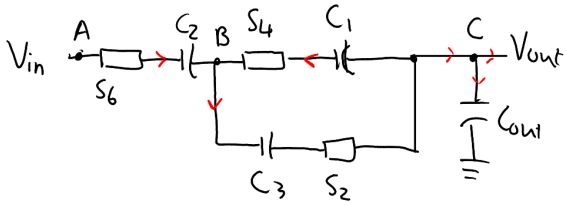

Figure 11: Phase 1 of Ladder topology.

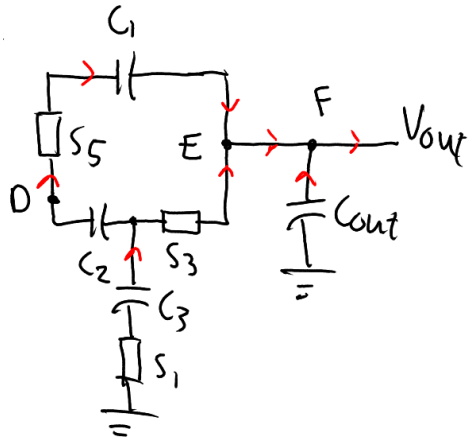

Figure 12: Phase 2 of Ladder topology.

$$q_{C1} = \frac{1}{3}q_{out},\ q_{C2} = \frac{1}{3}q_{out},\ q_{C3} = \frac{2}{3}q_{out},\ q^1_{out} = \frac{1}{3}q_{out},\ q^2_{out} = \frac{2}{3}q_{out}$$

$$a_C = [a_{C1}\ a_{C2}\ a_{C3}] = \left[\frac{1}{3}\ \frac{1}{3}\ \frac{2}{3}\right]$$

$$a_S = [a_{S1}\ a_{S2}\ a_{S3}\ a_{S4}\ a_{S5}\ a_{S6}] = \left[\frac{2}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\right]$$

$$K_{SSL} = \sum_{i=1}^{n_c} a_{C,i}^2 = \left(\frac{1}{3}\right)^2 + \left(\frac{1}{3}\right)^2 + \left(\frac{2}{3}\right)^2 = 0.667$$

$$K_{FSL} = 2\sum_{i=1}^{n_{swi}} a_{S,i}^2 = 2 \cdot \left(4\left(\frac{1}{3}\right)^2 + 2\left(\frac{2}{3}\right)^2\right) = 2.67$$

B.2.2. Derivation voltage terminals and blocking voltages

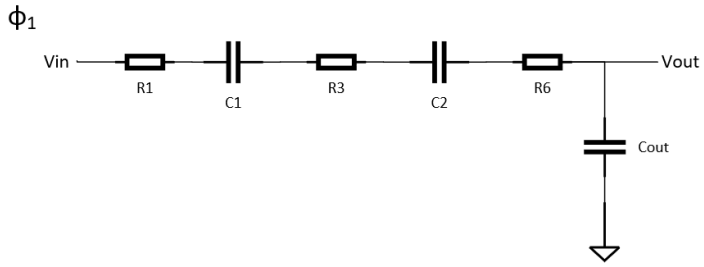

Figure 13: Phase 1 of the Series-Parallel topology.

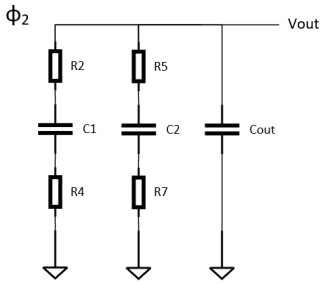

Figure 14: Phase 2 of the Series-Parallel topology.

Based on Figures 13 and 14, the required formulas are:

$$V_{in} = V_{C1} + V_{C2} + V_{out}$$

$$V_{C1} = V_{C2} = V_{out} \longrightarrow V_{in} = 3V_{out} \longrightarrow V_{out} = \frac{1}{3}V_{in}$$

Obtain the voltage across each capacitor and determine for each of the capacitor terminals (V+ and V-) the voltage in vector form, normalized to V_{in} (input voltage is 4 V based on Chapter 9).

$$V_{cap} = [V_{C1}\ V_{C2}]V_{in} = \left[\frac{1}{3}\ \frac{1}{3}\right]V_{in} = [1.33V\ 1.33V]$$

Determine V_{nodes1} and V_{nodes2}.

$$\text{In phase 1 :}$$

$$V_{C1+} = V_{in} \longrightarrow V_{C1-} = V_{C1+} - V_{C1} = V_{in} - \frac{1}{3}V_{in} = \frac{2}{3}V_{in}$$

$$V_{C2+} = V_{C1-} = \frac{2}{3}V_{in} \longrightarrow V_{C2-} = V_{C2+} - V_{C2} = \frac{1}{3}V_{in}$$

$$\text{In phase 2 :}$$

$$V_{C1+} = V_{out} = \frac{1}{3}V_{in} \longrightarrow V_{C1-} = V_{C1+} - V_{C1} = 0$$

$$V_{C2+} = V_{out} = \frac{1}{3}V_{in} \longrightarrow V_{C2-} = V_{C2+} - V_{C2} = 0$$

$$V_{nodes1} \text{ and } V_{nodes2} :$$

$$V_{nodes1} = [V_{C1+}\ V_{C1-}\ V_{C2+}\ V_{C2-}]V_{in} = \left[1\ \frac{2}{3}\ \frac{2}{3}\frac{1}{3}\right]V_{in}$$

$$V_{nodes2} = \left[\frac{1}{3}\ 0\ \frac{1}{3}\ 0\right]V_{in}$$

A table has been generated by looking at each switch per phase. Using V_{nodes1}, nodes in ϕ_1, and V_{nodes2}, nodes in ϕ_2, the voltage terminals is determined, which the blocking voltages, ΔV, are found when the switches are not conducting.

Table 9: Blocking voltages and voltages at the terminals in switches S1-S4.

Switches	S1 (R1)				S2 (R2)				S3 (R3)				S4 (R4)			
ϕ_{phase}	ϕ_1		$\phi 2$		ϕ_1		$\phi 2$		ϕ_1		$\phi 2$		ϕ_1		$\phi 2$	
Terminals	V_{in}	V_{C1+}	V_{in}	V_{C1+}	V_{out}	V_{C1+}	V_{out}	V_{C1+}	V_{C1-}	V_{C2+}	V_{C1-}	V_{C2+}	V_{C1-}	GND	V_{C1-}	GND
V	1	1	1	1/3	1/3	1	1/3	1/3	2/3	2/3	0	1/3	2/3	0	0	0
|ΔV|	0		2/3		2/3		0		0		1/3		2/3		0	

Table 10: Blocking voltages and voltages at the terminals in switches S5-S7.

Switches	S5 (R5)				S6 (R6)				S7 (R7)			
ϕ_{phase}	ϕ_1		$\phi 2$		ϕ_1		$\phi 2$		ϕ_1		$\phi 2$	
Terminals	V_{out}	V_{C2+}	V_{out}	V_{C2+}	V_{C2-}	V_{out}	V_{C2-}	V_{out}	V_{C2-}	GND	V_{C2-}	GND
V	1/3	2/3	1/3	1/3	1/3	1/3	0	1/3	1/3	0	0	0
|ΔV|	1/3		0		0		1/3		1/3		0	

The blocking voltage vector can be found now.

$$V_{block} = [V_{S1}\ V_{S2}\ V_{S3}\ V_{S4}\ V_{S5}\ V_{S6}\ V_{S7}]V_{in} = \left[\frac{2}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\right]V_{in}$$

$$V_{block} = [2.67V\ 2.67V\ 1.33V\ 2.67V\ 1.33V\ 1.33V\ 1.33V]$$

B.2.3. Rout verification and fine-tuning

The schematic used for fine tuning of the switching frequency and the R_{out} is shown in Figure 15.

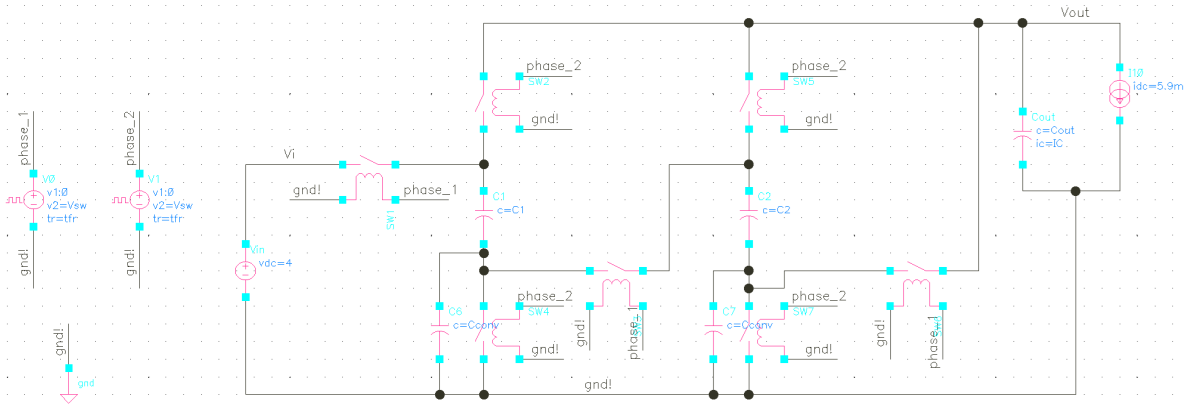

Figure 15: SP-topology with ideal switches to check R_{out} and fine-tune the switching frequency.

In this figure, C_{conv} capacitors are introduced to prevent convergence issues in simulations, with a value set to 0.1 fF to minimize its impact on the power converter. The R_{on} for each switch is set to 19.883 Ω, calculated in Chapter 11. I_{load} is set to 5.9 mA and the input voltage is 4 V. Before simulation, Equations 1 and 2 are used to determine the K_{SSL} and K_{FSL} from the graph of the simulation. These equations are derived from Equation 10.1 in Chapter 10 assuming $R_{SSL} = R_{FSL}$.

$$R_{on} = \frac{R_{\text{out}}}{\sqrt{2}K_{\text{FSL}}} \tag{1}$$

$$f_{sw} = \frac{\sqrt{2}K_{\text{SSL}}}{R_{\text{out}}C_{\text{fly}}} \tag{2}$$

The corresponding results are presented in Figures 16 and 17.

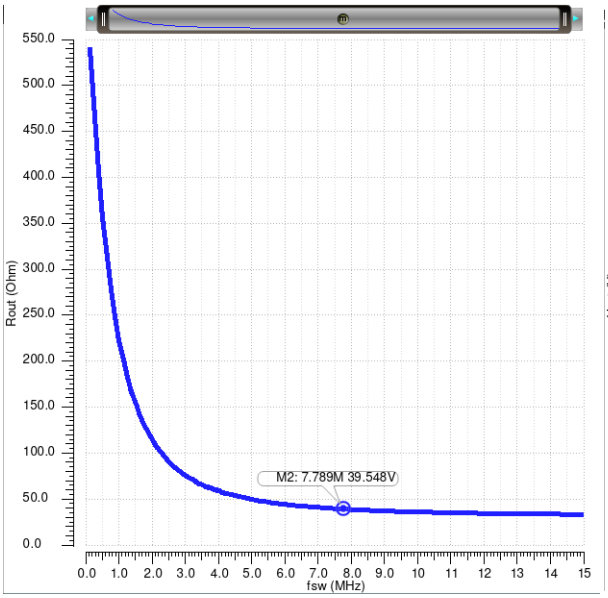

Figure 16: R_{out} vs f_{sw} for I_{load} = 5.9 mA.

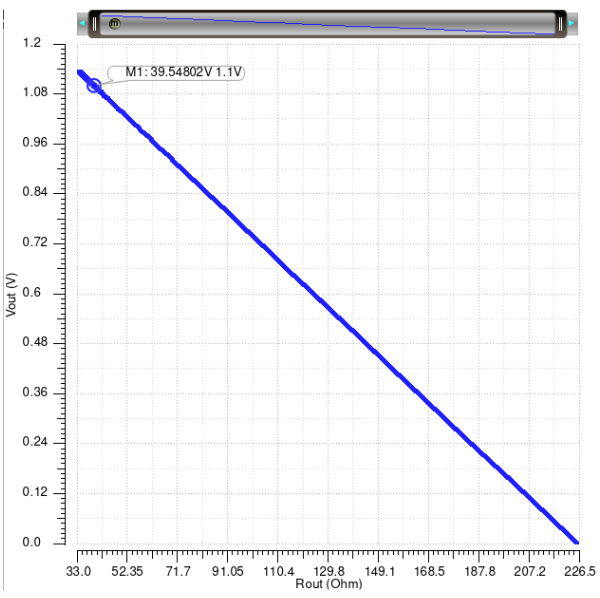

Figure 17: V_{out} vs R_{out} plot for I_{load} = 5.9 mA.

Figure 17 indicates that for V_{out} of 1.1 V, a R_{out} of 39.548 Ω is required, consistent with the calculated value (39.5 Ω). This corresponds to 7.789 MHz, differing from the initially calculated value (9.048 MHz). If we were to recalculate K_{SSL} and K_{FSL} with R_{on} of 19.883 Ω, C_{fly} of 2 nF, and the determined R_{out} and f_{sw} of 7.789 MHz, the results would be as follows:

$$K_{FSL} = \frac{R_{out}}{\sqrt{2}R_{on}} = 1.51$$

$$K_{SSL} = \frac{R_{out}C_{fly}f_{sw}}{\sqrt{2}} = 0.4356$$

Since the calculated values for K_{SSL} and K_{FSL} are known to be 0.444 and 1.56 when I_{load} = 5.9 mA as operating point, respectively, a comparison is made with the simulated values. This reveals that the simulated K-values align with the calculated values, although the SSL regime in the average model is slightly less accurate compared to the simulation. This is plotted in MATLAB for a more detailed comparison, as shown in Figure 18.

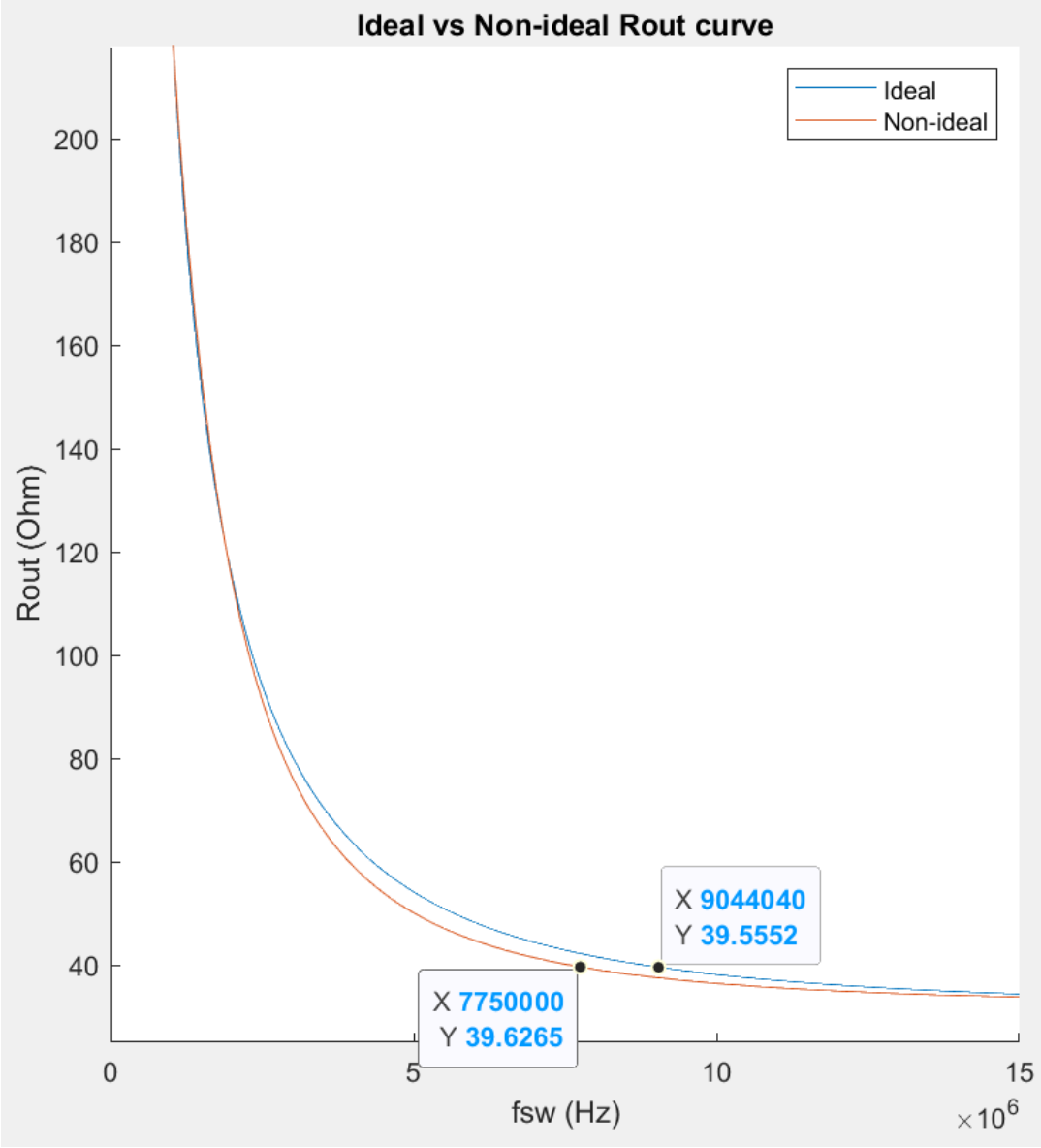

Figure 18: Calculated and simulated R_{out} plots, plotted in MATLAB.

This figure clearly indicates that the R_{out} formula corresponds to the non-ideal curve of the ideal power converter, extracted from Cadence Virtuoso. Utilizing this approximation formula allows for estimating and optimizing the switching frequency to achieve the desired V_{out} in the simulation.

B.2.4. Simulation results for the determination of NMOS and PMOS type switches

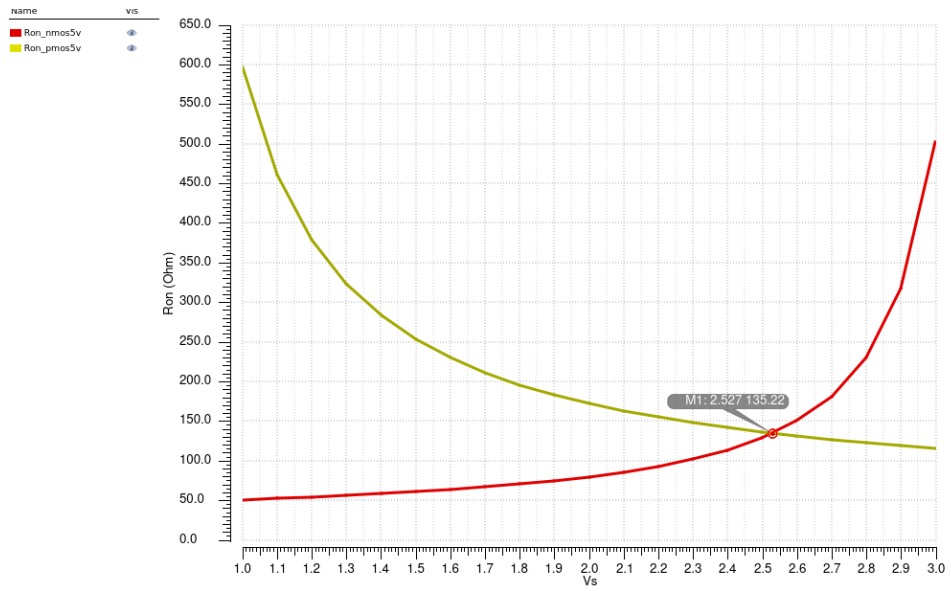

Figure 19: R_{on} Vs V_s (source voltage) with V_{trip} = 2.527 V.

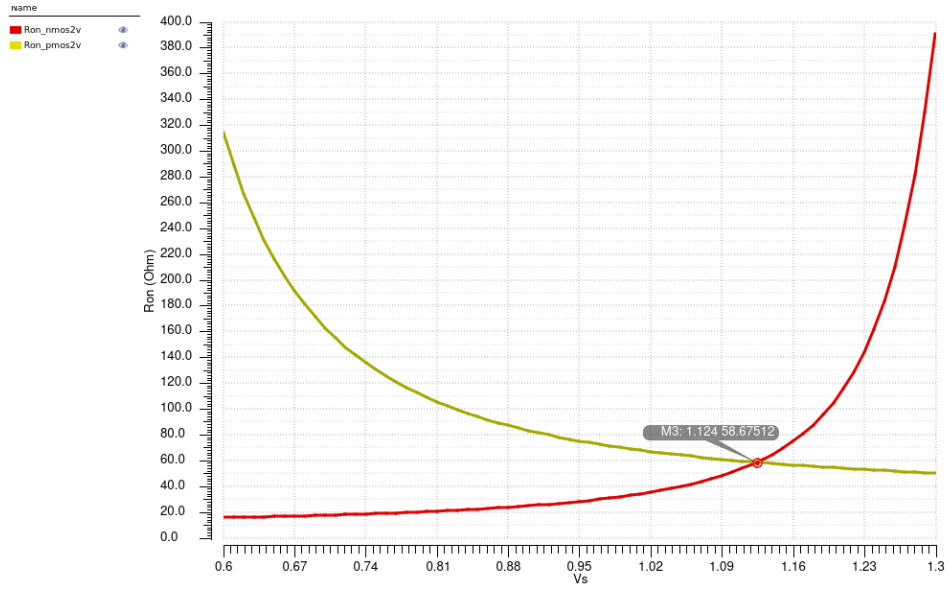

Figure 20: R_{on} Vs V_s (source voltage) with V_{trip} = 1.124 V.

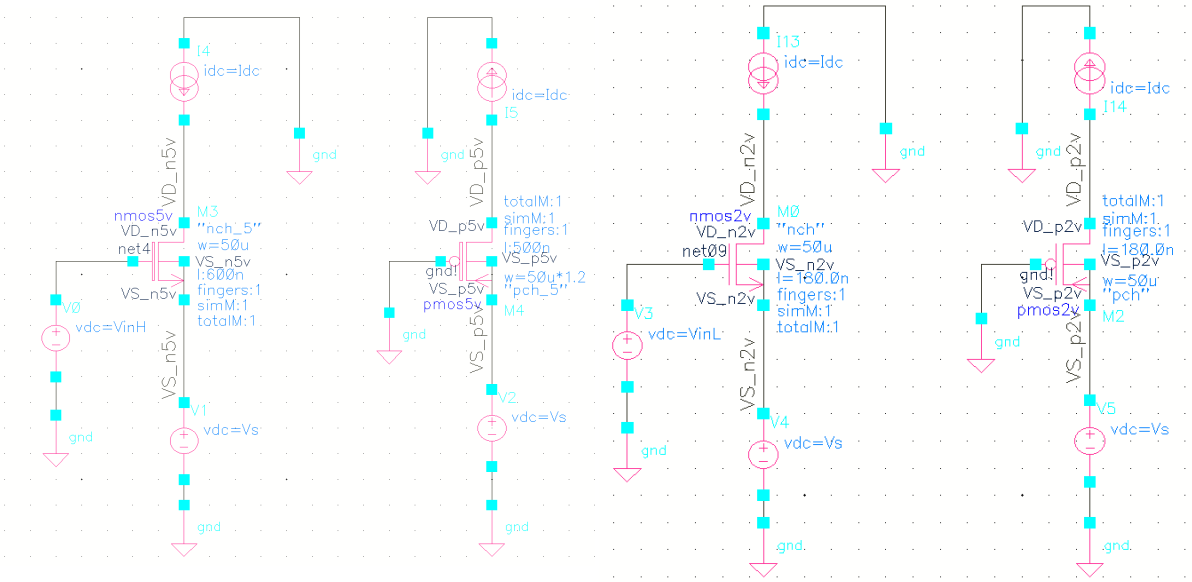

Figure 21: Schematic with nmos5v and pmos5v for V_s (source voltage) to obtain R_{on} with V_{in} = 4 V and 0 V, respectively.

Figure 22: Schematic with nmos2v and pmos2v for V_s (source voltage) to obtain R_{on} with V_{in} = 1.8 V and 0 V, respectively.

C.3. Python and MATLAB codes

C.3.1. Calculation of Wopt and fsw

```python
# CalculateVout.py
import numpy as np

# Technology Parameters of PMOS5v
cg_dens = 1.63e-15;
ron_dens = 5751;

# Constants
Vsw = 4; # Swing voltage at the switches
KSSL = 0.444; # KSSL = 0.444 for C1 = C2
KFSL = 1.56;
Vin = 4; # Input voltage
M = 1/3; # VCR = 1/3
Iload = 5.9e-3; # Iload = 5.9 mA
Cfly = 2e-9; # Cfly = 2 nF
n_sw = 7; # 7 switches

# Determine Optimum width and others

# Wopt with the derived equation
num = np.sqrt(2)*Cfly*pow(KFSL*ron_dens*Iload,2);
den = 2*n_sw*cg_dens*pow(Vsw,2)*KSSL;
Wopt = pow(num/den,1/3)
Ron = ron_dens/Wopt; # Ron = Ohm*um / um
fsw = KSSL/(KFSL*Cfly*Ron);

# Rout approximation formula
Rout = np.sqrt(pow(KSSL/(fsw*Cfly),2) + pow(KFSL*Ron,2));

# Determine Vout
Vout = M*Vin - Iload*Rout;

print(f"Wopt = {Wopt} (um)");
print(f"fsw = {fsw*1e-6} MHz");
print(f"Ron = {Ron} Ohm")
print(f"Rout = {Rout} Ohm");
print(f"Vout = {Vout} V");

# fsw = 9.048 MHz, Vout = 1.1286 V, Wopt = 366 um --> Need to optimize Vout to 1.1 V
```

Listing 1: Code for calculating W_{opt} and f_{sw}

C.3.2. Optimization for targeted Vout

```python
# CalculateOptimizedVout.py
import numpy as np

# Parameters
cg_dens = 1.63e-15;
ron_dens = 5751;

# Constants
Vsw = 4;
KSSL = 0.444;
KFSL = 1.56;
Vin = 4;
M = 1/3;
Iload = 5.9e-3;
Cfly = 2e-9;
n_sw = 7;
Vout_targeted = 1.1;

# Determined by CalculateVout.py
Rout_calculated = 34.69984316118019; # Calculated Rout
fsw_calculated = 9.048e6; # Calculated fsw (= 9.048 MHz)

```

```
Rout = (M*Vin - Vout_targeted)/Iload; # Ideal Rout
print(f"Required Rout = {Rout} Ohm");

RSSL = KSSL/(Cfly*fsw_calculated)

# Calculate RFSL from known Rout and RSSL
RFSL = np.sqrt( pow(Rout,2) - pow( RSSL,2));

Ron_new = RFSL/KFSL # Use RFSL = KFSL*Ron
Wopt_new = ron_dens/Ron_new;
Vout_new = M*Vin - Iload*np.sqrt(pow(RSSL,2) + pow(KFSL*Ron_new,2))

print(f"Wopt_new = {Wopt_new} (um)");
print(f"Ron_new = {Ron_new} Ohm"); # Use this Ron to optimize power switches size
print(f"Vout_new = {Vout_new} V");

# Vout = 1.1 V, Wopt = 290 um, Ron = 19.883 Ohm
```

Listing 2: Code for optimization W_{opt} for $V_{out,targeted}$

C.3.3. Controller tuning

```
% ========================================================================
% This script is used to calculate the required PI-controller gains.
% Formulas and specifications are derived in the report.
% Rise/Settling time and overshoot can be displayed.
% ========================================================================

clear;
clc;
close all;

s = tf('s');

% Relevant specification
tsettle_OL = 94.6e-6; % settling time open-loop = 94.6 us

%{ settling time (5.46 %) in CL-system must be slightly faster
  % than in OL-system
  %}
tsettle_CL = tsettle_OL - 4.6e-6; % for example 90 us.
tau_des = tsettle_CL/2.9077; % desired time constant of CL-system

% General settings
Vin = 4; % Input voltage
Vout = 1.1; % Output voltage
M = 1/3; % VCR
Cout = 1e-6; % Output capacitor
Cfly = 2e-9; % Total value of flying capacitors
Ron = 19.883; % ON-resistance
KFSL = 1.56;
tdead = 500e-12; % Deadtime of the NOV to avoid shoot-through current
%% Operating point selection

%{========================================================================
  % Select the required operating point based on Iload
  % Note however, we included the frequency divider as lower Iload would
  % yield lower switching frequency.
  % Assuming that Kvco of (50/9) MHz/V also holds for 19.1 kHz (Iload = 20 uA)
  % and 870 kHz (Iload = 910 uA), however, theoretically is possible, but
  % practically not feasible due to the negative control voltage of the VCO.
  % Hence, for Iload = 20 uA and 910 uA, the fmin = 4 MHz when Vmin = 0.1 V
  % To be able to use the VCO gain, we use frequency divider N = fmin/fsw
  % Then transfer function of frequency divider = 1/N.
  % Also note that the fsw of Iload = 5.9 mA and 5.01 mA are
  % within the VCO tuning range. Hence, no frequency divider is required.
  %}========================================================================
Iload = 5.9e-3;  % Select the desired load current to tune PI parameters

if Iload == 5.9e-3 % Iload = 5.9 mA
```

```
fsw = 7.789e6;
Rout = 39.548;
N = 1;
K_div = 1/N;
elseif Iload == 5.01e-3 % Iload = 5.01 mA
fsw = 5.62e6;
Rout = 46.455;
N = 1;
K_div = 1/N;
elseif Iload == 910e-6 % Iload = 910 uA
fsw = 870e3;
Rout = 255.41;
N = 4e6/fsw; % fmin = 4 MHz, fsw = 870 kHz
K_div = 1/N;  % transfer function of frequency divider
elseif Iload == 20e-6 % Iload = 20 uA
fsw = 19.1e3;
Rout = 11.642e3;
N = 4e6/fsw; % fmin = 4 MHz, fsw = 19.1 kHz
K_div = 1/N; % transfer function of frequency divider
else
fprintf("Please determine fsw, Rout and N first!");
end
%% Pre-calculations

%{=========================================================================
  % The required values are calculated before determing Htot(s) (G(s))
  %}=========================================================================

% Calculations
Tsw = 1/fsw;
td = 0.5*Tsw; % Average time delay of the SC-based DC-DC converter
td_tot = tdead + td; % Deadtime + the average time delay
Rload = Vout/Iload;
KSSL = fsw*Cfly*sqrt((Rout)^2 - (KFSL*Ron)^2);

k1 = (KSSL/Cfly)^2;
k2 = (KFSL*Ron)^2;
w = 1/(Cout*Rload);

kdc_p1 = (Vout-M*Vin)/(Cout*(Rout^2));
kdc_p2 = -k1/(sqrt((k1/((fsw)^2)) + k2)*fsw^3);

%% Calculations of the OL-transfer function Htot(s)
tau = 1/(w + 1/(Cout*Rout));
K = kdc_p1*kdc_p2;

% Transfer function of VCO
K_vco = (50/9)*10^6; % Change VCO gain if required

% Determine Ktot
Ktot = K_vco*K_div*K*tau;
Htot = (Ktot/(tau*s + 1))*exp(-td_tot*s); % with ideal delay
%% Kp and Ki calculations (PI-controller)
Kp = tau/(Ktot*(tau_des + td_tot));
Ki = 1/(Ktot*(tau_des + td_tot));
%% Print the OL-transfer function and the required Kp and Ki
fprintf("\nKp = %0.3f\n", Kp);
fprintf("Ki = %0.3f\n", Ki)
%% Check and obtain the step plot/data for the CL-system

% Obtain the CL-transfer function including PI-controller
H_c = Kp + Ki/s; % Controller transfer function
G = H_c*Htot; % Controller + Htot(s) transfer function
G_f = G/(1+G); % CL-transfer function

% Obtain step info from G_f (CL-transfer function)
% Set info with ts (5.46%) and Tr (10% to 90%) and obtain OS, Ts and Tr
StepInfo = stepinfo(Vout*G_f,'SettlingTimeThreshold',0.0546,'RiseTimeThreshold',[0.1 0.9]);
Iload_RT = StepInfo.RiseTime*10^6; % Convert to us
Iload_ST = StepInfo.SettlingTime*10^6; % Convert to us
Iload_OS = StepInfo.Overshoot;
```

```
120
121 % Print the results
122 fprintf("Ts(5.46%%) = %0.2f us\n", Iload_ST);
123 fprintf("Tr(10%% to 90%%) = %0.2f us\n",Iload_RT);
124 fprintf("OS = %0.2f %%\n",Iload_OS);
```

Listing 3: Code for tuning PI-controller for four operating points

D.4. Control loop

D.4.1. Derivation of the mathematical model

The dynamics of the power converter is derived from Figure 23.

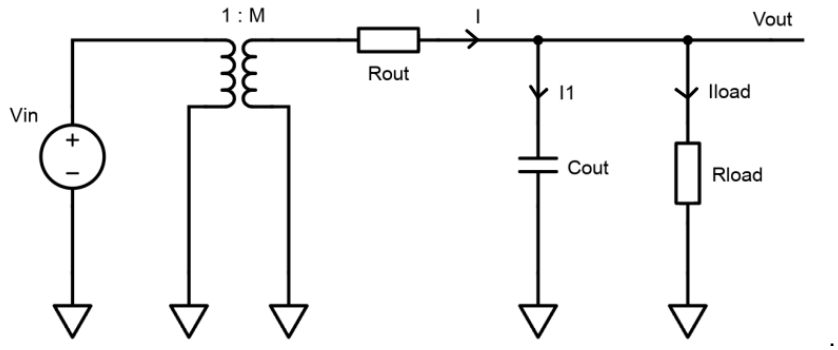

Figure 23: SC-based DC-DC converter average model with R_{load}.

For the derivation we make the following assumptions:

1. C_{out} » C_1 and C_2, which the capacitors are shown in Figure 15. These flying capacitors are the capacitors in the 3:1 SP-topology of the SC-based DC-DC converter.

2. Ripple at the output is negligible.

3. V_{in} is static.

4. Linearization around one commonly used operating point. (Our common operating point is when I_{load} = 5.9 mA.)

5. Duty cycle is fixed at 0.5.

6. A first-order model.

The derivations are divided in steps.
Step 1 - Obtain the differential equation of the average model.

$$R_{out} = \sqrt{\left(\frac{K_{SSL}}{f_{sw}C_{fly}}\right)^2 + (K_{FSL}R_{on})^2}$$

$$Let\ K1 = \left(\frac{K_{SSL}}{C_{fly}}\right)^2\ and\ K2 = (K_{FSL}R_{on})^2$$

$$I = I_1 + I_{load}$$

$$\frac{MV_{in} - V_{out}}{R_{out}} = C_{out}\frac{dV_{out}}{dt} + \frac{V_{out}}{R_{load}}$$

$$\frac{dV_{out}}{dt} = \frac{MV_{in} - V_{out}}{C_{out}R_{out}} - \frac{V_{out}}{C_{out}R_{load}}$$

Step 2 - Linearize R_{out} in terms of f_{sw} and linearize around the point P($\overline{f_{sw}}$).

$$R_{out} = \sqrt{\frac{K1}{f_{sw}^2} + K2}$$

$$\hat{R}_{out} = \frac{dR_{out}}{df_{sw}}\hat{f}_{sw} = -\frac{K1}{\sqrt{\frac{K1}{(\overline{f_{sw}})^2} + K2} \cdot (\overline{f_{sw}})^3}\hat{f}_{sw}$$

Step 3 - Let $\omega = \frac{1}{C_{out}R_{load}}$ and linearize $\frac{dV_{out}}{dt}$ around P($\overline{V_{in}}$, $\overline{V_{out}}$, $\overline{R_{out}}$).

$$\frac{dV_{out}}{dt} = k = \frac{MV_{in}}{C_{out}} \cdot \frac{1}{R_{out}} - \frac{V_{out}}{C_{out}R_{out}} - \omega V_{out}$$

$$\frac{d\hat{V}_{out}}{dt} = \frac{dk}{dV_{in}}\hat{V}_{in} + \frac{dk}{dV_{out}}\hat{V}_{out} + \frac{dk}{dR_{out}}\hat{R}_{out}$$

$$\frac{dk}{dV_{in}}\hat{V}_{in} = \frac{M}{C_{out}\overline{R_{out}}}\hat{V}_{in}$$

$$\frac{dk}{dV_{out}}\hat{V}_{out} = -\left(\frac{1}{C_{out}\overline{R_{out}}} + \omega\right)\hat{V}_{out}$$

$$\frac{dk}{dR_{out}}\hat{R}_{out} = \left(-\frac{M\overline{V_{in}}}{C_{out}(\overline{R_{out}})^2} + \frac{\overline{V_{out}}}{C_{out}(\overline{R_{out}})^2}\right)\hat{R}_{out}$$

$$\frac{dk}{dR_{out}}\hat{R}_{out} = \left(-\frac{M\overline{V_{in}}}{C_{out}(\overline{R_{out}})^2} + \frac{\overline{V_{out}}}{C_{out}(\overline{R_{out}})^2}\right) \cdot -\frac{K1}{\sqrt{\frac{K1}{(\overline{f_{sw}})^2} + K2} \cdot (\overline{f_{sw}})^3}\hat{f}_{sw}$$

Step 4 - Let $\hat{R}_{out}$ = 0 and determine $\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)}$.

$$\frac{d\hat{V}_{out}}{dt} = \frac{M}{C_{out}\overline{R_{out}}}\hat{V}_{in} - \left(\frac{1}{C_{out}\overline{R_{out}}} + \omega\right)\hat{V}_{out}$$

Use La place transform

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)} = \frac{M}{C_{out}\overline{R_{out}}} \cdot \frac{1}{s + \omega + \frac{1}{C_{out}\overline{R_{out}}}}$$

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)} = \frac{M}{C_{out}\overline{R_{out}}} \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}\overline{R_{out}}}\right)}$$

Step 5 - Let $\hat{V}_{in}$ = 0 and determine the control-to-output transfer function $\frac{\hat{V}_{out}(s)}{\hat{f}_{sw}(s)}$.

$$\frac{d\hat{V}_{out}}{dt} = -\left(\frac{1}{C_{out}\overline{R_{out}}} + \omega\right)\hat{V}_{out} + \left(-\frac{M\overline{V_{in}}}{C_{out}(\overline{R_{out}})^2} + \frac{\overline{V_{out}}}{C_{out}(\overline{R_{out}})^2}\right) \cdot -\frac{K1}{\sqrt{\frac{K1}{(\overline{f_{sw}})^2} + K2 \cdot (\overline{f_{sw}})^3}}\hat{f}_{sw}$$

Use La place transform

$$\frac{\hat{V}_{out}(s)}{\hat{f}_{sw}(s)} = -\frac{K1}{\sqrt{\frac{K1}{(\overline{f_{sw}})^2} + K2 \cdot (\overline{f_{sw}})^3}}\left(\frac{\overline{V_{out}} - M\overline{V_{in}}}{C_{out}(\overline{R_{out}})^2}\right) \cdot \frac{1}{s + \omega + \frac{1}{C_{out}\overline{R_{out}}}}$$

$$\frac{\hat{V}_{out}(s)}{\hat{f}_{sw}(s)} = -\frac{K1}{\sqrt{\frac{K1}{(\overline{f_{sw}})^2} + K2 \cdot (\overline{f_{sw}})^3}}\left(\frac{\overline{V_{out}} - M\overline{V_{in}}}{C_{out}(\overline{R_{out}})^2}\right) \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}\overline{R_{out}}}\right)}$$

D.4.2. Derivation of the rise and settling time

The average model of the power converter is a first-order model with a time delay of T_{sw} and t_{dead} in the range of ns to ms. Because the time delay is close to 0 s, it can be considered as a first-order model.

Settling time (5.46%) from the standard first-order model:

$$H_{plant}(s) = \frac{b}{s+a} = \frac{b}{a} \cdot \frac{1}{\frac{1}{a}s + 1} = \frac{K_{DC}}{\tau s + 1}$$

Determine step response in time – domain :

$$y_{plant}(t) = \frac{b}{a}\left(1 - e^{-a \cdot t}\right)$$

Error band is 5.46% and let t be $\frac{X}{a}$

$$\left(1 - \frac{5.46\%}{100\%}\right)\frac{b}{a} = \frac{b}{a}\left(1 - e^{-a \cdot \frac{X}{a}}\right)$$

$$0.9454 = 1 - e^{-X} \Longrightarrow X \approx 2.9077$$

$$t_s(5.46\%) = \frac{X}{a} = 2.9077 \cdot \frac{1}{a} = 2.9077\tau$$

Rise time(10% to 90%) from the standard first-order model:

$$H_{plant}(s) = \frac{b}{s+a} = \frac{b}{a} \cdot \frac{1}{\frac{1}{a}s+1} = \frac{K_{DC}}{\tau s+1}$$

$$y_{plant}(t) = \frac{b}{a}\left(1 - e^{-a \cdot t}\right)$$

Let t = t_{90} and t_{10} and take 10% and 90% of the final value

$$0.9\frac{b}{a} = \frac{b}{a}\left(1 - e^{-a \cdot t_{90}}\right)$$

$$t_{90} = -\frac{ln(0.1)}{a}$$

$$0.1\frac{b}{a} = \frac{b}{a}\left(1 - e^{-a \cdot t_{10}}\right)$$

$$t_{10} = -\frac{ln(0.9)}{a}$$

$$t_r = t_{90} - t_{10} \approx \frac{2.1972}{a} = 2.1972\tau$$

D.4.3. Derivation of the design formulas for BGR and VCO

The derivation is based on Figure 24.

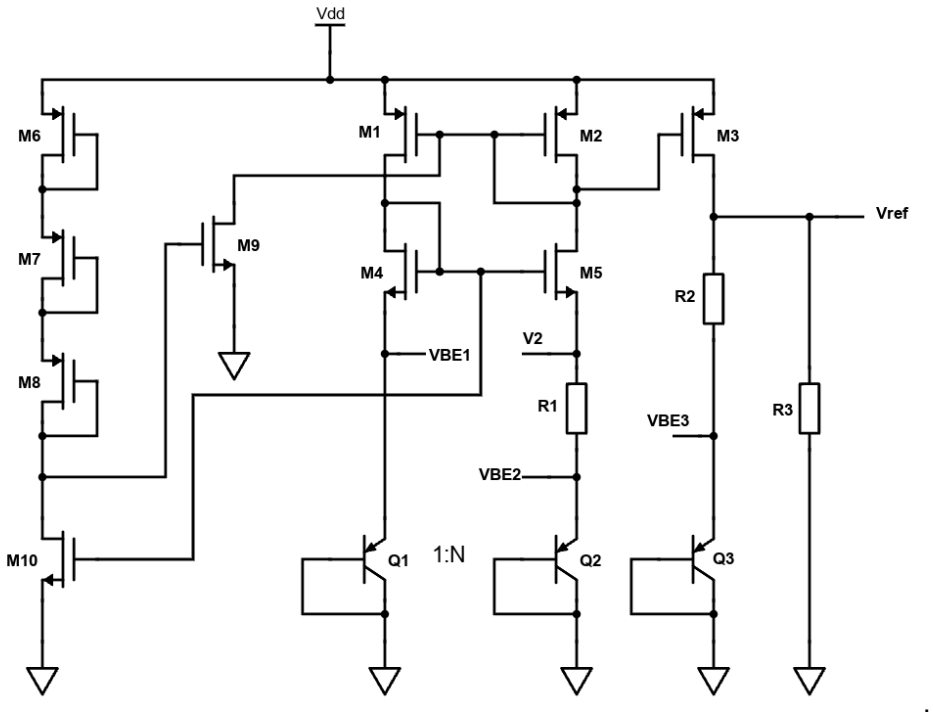

Figure 24: Schematic of a conventional voltage-mode BGR.

Let I_{Dx} be the drain current of transistor x, N is the number of PNP-transistors of Q2, I_x be the current flowing through resistor R_x and V_T be the thermal voltage, which is approximately 26 mV. Assume M1 = M2 = M3, M4 = M5 and VBE1 = V2.

$$V_{ref} = \alpha_1 V_{BE} + \alpha_2 ln(N) V_t$$

$$|I_{D2}| = \frac{V_2 - V_{BE2}}{R_1} = \frac{V_T ln(N)}{R_1}$$

$$R_1 = \frac{V_T ln(N)}{|I_{D2}|}$$

$$|I_{D3}| = I_{R2} + I_{R3} = \frac{V_{ref} - V_{BE3}}{R_2} + \frac{V_{ref}}{R_3}$$

$$|I_{D3}| = \frac{V_{ref}}{R_2} - \frac{V_{BE3}}{R_2 + \frac{V_{ref}}{R_3}}$$

$$|I_{D3}| = |I_{D2}|$$

$$\frac{V_T ln(N)}{R_1} = \frac{V_{ref}}{R_2} - \frac{V_{BE3}}{R_2 + \frac{V_{ref}}{R_3}}$$

$$\frac{V_T ln(N)}{R_1} = V_{ref}\left(\frac{1}{R_2} + \frac{1}{R_3}\right) - \frac{V_{BE3}}{R_3}$$

$$V_{ref} = \frac{1}{\left(\frac{1}{R_2} + \frac{1}{R_3}\right)} \frac{1}{R_2}\left(V_{BE3} + \frac{R_2}{R_1} ln(N) V_T\right)$$

$$V_{ref} = \frac{R_3}{R_2 + R_3}\left(V_{BE3} + \frac{R_2}{R_1} ln(N) V_T\right)$$

$$V_x = \frac{V_{ref}}{\left(\frac{R_3}{R_2 + R_3}\right)}$$

$$V_x = V_{BE3} + \frac{R_2}{R_1} ln(N) V_T$$

Derivation of R_2:

$$V_x = V_{BE3} + \frac{R_2}{R_1} ln(N) V_T \Longrightarrow V_{ref} = \alpha_1 V_{BE} + \alpha_2 ln(N) V_t$$

$$\alpha_1 = 1 \text{ and } \alpha_2 = \frac{R_2}{R_1}$$

$$\frac{\partial V_x}{\partial T} = \alpha_1 \frac{\partial V_{BE3}}{\partial T} + \alpha_2 \frac{\partial V_T}{\partial T} = 0$$

$$\frac{\partial V_x}{\partial T} = \alpha_1 \frac{\partial V_{BE3}}{\partial T} + \alpha_2 \frac{k}{q}$$

$$\alpha_2 ln(N) = -\frac{\frac{\partial V_{BE3}}{\partial T}}{\frac{k}{q}}$$

$$\alpha_2 = -\frac{\frac{\partial V_{BE3}}{\partial T}}{ln(N)\frac{k}{q}}$$

$$\alpha_2 ln(N) = 18.81 \Longrightarrow \alpha_2 = \frac{R_2}{R_1} \Longrightarrow R_2 = \frac{18.81 R_1}{ln(N)}$$

Derivation of R_3:

$$V_x = \frac{V_{ref}}{\left(\frac{R_3}{R_2+R_3}\right)} \Longrightarrow R_3 = \frac{R_2}{V_x - V_{ref}} V_{ref}$$

$$V_x = V_{BE3} + \frac{R_2}{R_1} ln(N) V_T \Longrightarrow R_3 = \frac{R_2}{V_{BE3} + \left(\frac{R_2}{R_1}\right) ln(N) V_T - V_{ref}} V_{ref}$$

Summary of the design equations:

$$R_1 = \frac{V_T ln(N)}{|I_{D2}|}$$

$$R_2 = \frac{18.81 R_1}{ln(N)}$$

$$R_3 = \frac{R_2}{V_{BE3} + \left(\frac{R_2}{R_1}\right) ln(N) V_T - V_{ref}} V_{ref}$$

From Chapter 12.2.1: $\alpha_1 \frac{\partial V_{BE3}}{\partial T}$ = -1.62 mV/°C, k_B is the Boltzmann constant and q is the elementary charge.

For the design equations of the switching threshold voltages of the Schmitt trigger in the VCO, V_H and V_L, Figure 25 is used.

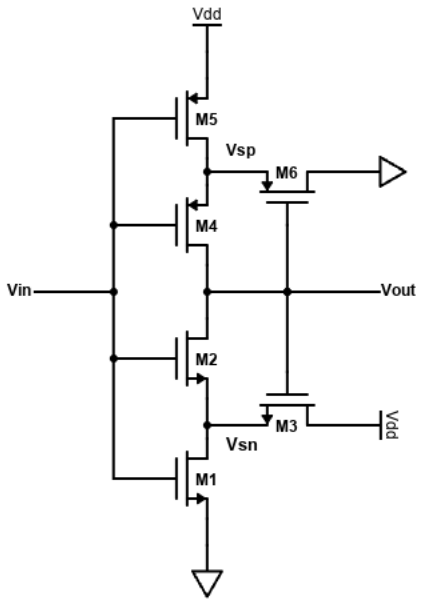

Figure 25: Schmitt trigger schematic for derivation of V_H and V_L.

Consider V_{in} = 0 V and V_{out} = V_{DD}. Increasing V_{in} to V_H turns on M1 and M2, in which M3 is still on, but starts to turn off. V_H is defined when M2 turns on.

$$\text{for M2}: \longrightarrow V_{GS2} \geq V_{TH2}$$

$$V_{G2} - V_{S2} \geq V_{TH2} \longrightarrow V_{in} - V_{sn} \geq V_{TH2}$$

$$V_{in} = V_{\mathrm{H}} = V_{sn} + V_{TH2}$$

When I_{D1} = I_{D3} (M1 and M3 both are on) and neglecting channel length modulation (CLM), we have the following:

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_{TH3})^2$$

$$\text{Use the derived equation with } \mathrm{V_{sn}} \text{ and } \mathrm{V_{out}} = \mathrm{V_{DD}}$$

$$\left(\frac{W}{L}\right)_1 (V_H - V_{TH1})^2 = \left(\frac{W}{L}\right)_3 (V_{DD} - V_H + V_{TH2} - V_{TH3})^2$$

$$\text{if } \mathrm{V_{TH2}} = \mathrm{V_{TH3}}, \text{ then}:$$

$$\left(\frac{W}{L}\right)_1 (V_H - V_{TH1})^2 = \left(\frac{W}{L}\right)_3 (V_{DD} - V_H)^2$$

Final result is then:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{V_{DD} - V_H}{V_H - V_{TH1}}\right)^2 \left(\frac{W}{L}\right)_3$$

Next, consider V_{in} = V_{DD} V and V_{out} = 0 V. Decreasing V_{in} to V_L turns on M4 and M5, in which M6 is still on, but starts to turn off. V_L is defined when M4 turns on.

$$\text{for M4}: \longrightarrow V_{SG4} \geq |V_{TH4}|$$

$$V_{S4} - V_{G4} \geq |V_{TH4}| \longrightarrow V_{sp} - V_L \geq |V_{TH4}|$$

$$V_{in} = V_L = V_{sp} - |V_{TH4}|$$

When I_{D5} = I_{D6} ignoring CLM, we have the following:

$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_5 (V_{SG5} - |V_{TH5}|)^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_6 (V_{SG6} - |V_{TH6}|)^2$$

$$\text{Use the derived equation with } V_{sp} \text{ and } V_{out} = 0V$$

$$\left(\frac{W}{L}\right)_5 (V_{DD} - V_L - |V_{TH5}|)^2 = \left(\frac{W}{L}\right)_6 (V_L + |V_{TH4}| - |V_{TH6}|)^2$$

$$\text{if } |V_{TH4}| = |V_{TH6}|, \text{ then}:$$

$$\left(\frac{W}{L}\right)_5 (V_{DD} - V_L - |V_{TH5}|)^2 = \left(\frac{W}{L}\right)_6 (V_L)^2$$

Final result is then:

$$\left(\frac{W}{L}\right)_5 = \left(\frac{V_L}{V_{DD} - V_L - |V_{TH5}|}\right)^2 \left(\frac{W}{L}\right)_6$$

Since M2 and M4 act as switches, make the M2 and M4 equal or larger than the other transistor sizes.

$$\left(\frac{W}{L}\right)_2 \geq \max\left(\left(\frac{W}{L}\right)_1, \left(\frac{W}{L}\right)_3\right)$$

$$\left(\frac{W}{L}\right)_4 \geq \max\left(\left(\frac{W}{L}\right)_5, \left(\frac{W}{L}\right)_6\right)$$

D.4.4. Settings for testing small input voltage disturbance

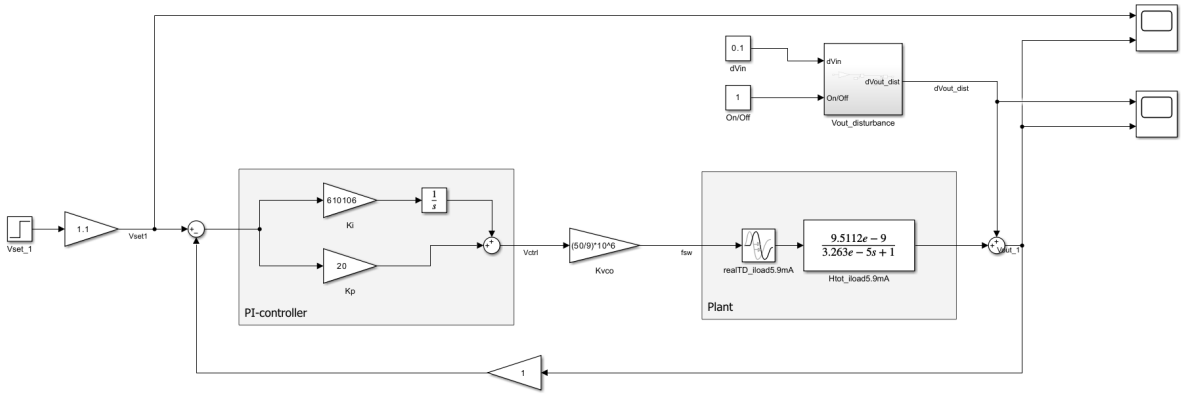

Figure 26: Block diagram with V_{in} and V_{ref} disturbance.

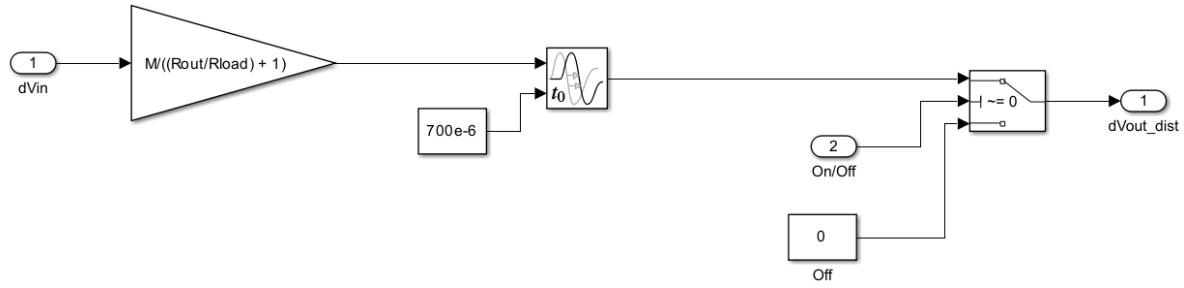

Figure 27: Block diagram within the disturbance system.

The input voltage disturbance was applied at the output of the plant model, as illustrated in Figure 26, as it directly affects the output voltage. Figure 27 shows a subsystem of the disturbance model, where the user-defined dV_{in} (for example, 0.1 V) is converted to dV_{out} using the equation $\frac{\hat{V}out(s)}{\hat{V}in(s)}$, which was derived in Appendix D.4.1.

$$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)} = \frac{M}{C_{out}\overline{R_{out}}} \cdot \frac{1}{s + \left(\frac{1}{C_{out}R_{load}} + \frac{1}{C_{out}\overline{R_{out}}}\right)}$$

Convert to $s = j\omega$, take the absolute and let $\omega = 0$

$$|\hat{V}_{out}| = \left(\frac{M}{C_{out}\overline{R_{out}}\left(\frac{1}{C_{out}\overline{R_{out}}} + \frac{1}{C_{out}R_{load}}\right)}\right)|\hat{V}_{in}| = \left(\frac{M}{1 + \frac{\overline{R_{out}}}{R_{load}}}\right)|\hat{V}_{in}|$$

D.4.5. Overview of transistor sizes and component values

Table 11: General overview of the transistor sizes of the Bandgap reference.

Bandgap reference	
MOSFETs	Transistor size (width / length)
M4, M5, M9, M10	11 μm / 4 μm
M1 - M3	33 μm / 4 μm
M6 - M8	3 μm / 3 μm

Table 12: General overview of the transistor sizes of the PI controller.

PI controller		
MOSFETs	Transistor size (width / length)	NoF (Number of Fingers)
M1, M2	2 μm / 1.2 μm	6
M3, M4	3.8 μm / 1.2 μm	1
M5, M6	3.9 μm / 1.2 μm	2
M7, M8	2.2 μm / 1.2 μm	1
M9	2.2 μm / 1.2 μm	1

Table 13: General overview of the transistor sizes of the VCO.

VCO	
MOSFETs	Transistor size (width / length)
M1	1.3 μm / 600 nm
M2	10 μm / 600 nm
M3	5 μm / 600 nm
M4	10 μm / 500 nm
M5	1.3 μm / 500 nm
M6	5 μm / 500 nm
M7	2 μm / 600 nm
M8	4.8 μm / 500 nm
M9, M13	2 μm / 1.6 μm
M10	2 μm / 600 nm
M11	5.3 μm / 500 nm
M12, M14	8 μm / 1.6 μm

Table 14: General overview of other component values.

Other components		
Component	Value	belongs to
Capacitor C	1.4 pF	VCO
PNP transistor ratio 1:N (Q1 and Q2)	1:8	BGR
Resistor R1	8.7 kΩ	BGR
Resistor R2	69.57 kΩ	BGR
Resistor R3	786.5 kΩ	BGR
Capacitor C	131.12 pF	PI controller
Resistor R	250 kΩ	PI controller
Capacitor Cconv	100 aF	SCPC
Transistors M1 and M3	290 μm / 500 nm (width / length)	SCPC
Transistors M2, M4 and M5-M7	290 μm / 600 nm (width / length)	SCPC

D.4.6. Simulation results of the other operating points

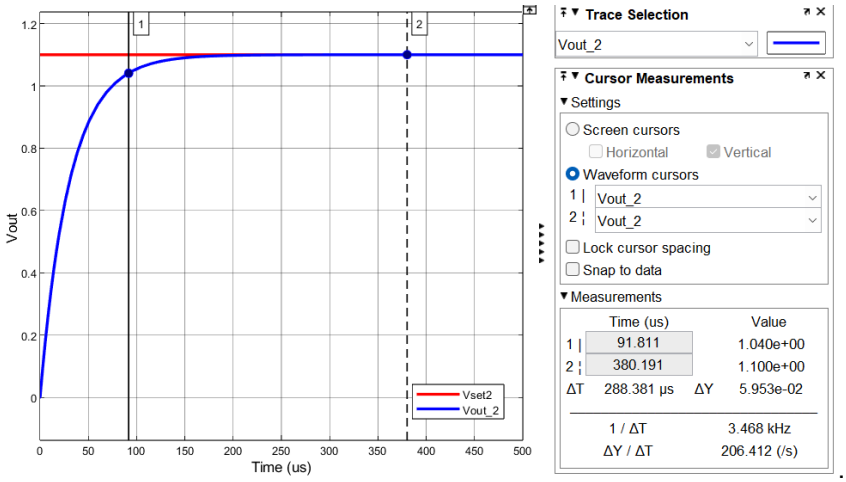

Figure 28: Settling time and overshoot at operating point I_{load} = 5.01 mA.

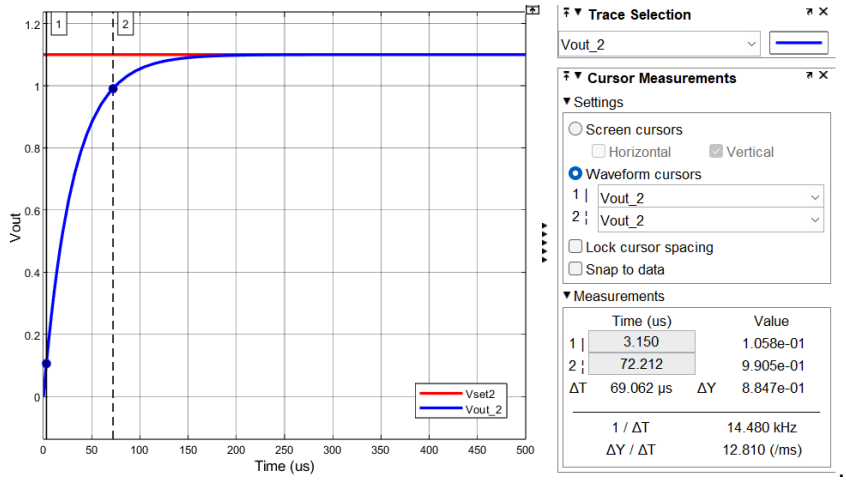

Figure 29: Rise time at operating point I_{load} = 5.01 mA.

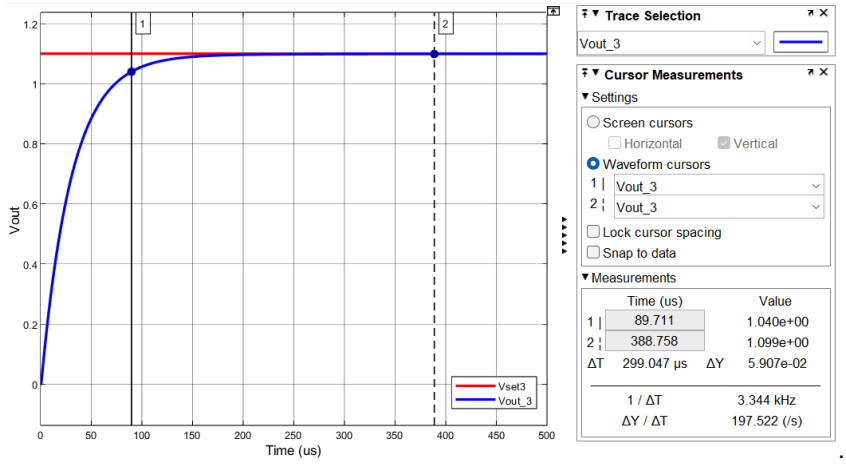

Figure 30: Settling time and overshoot at operating point I_{load} = 910 µA.

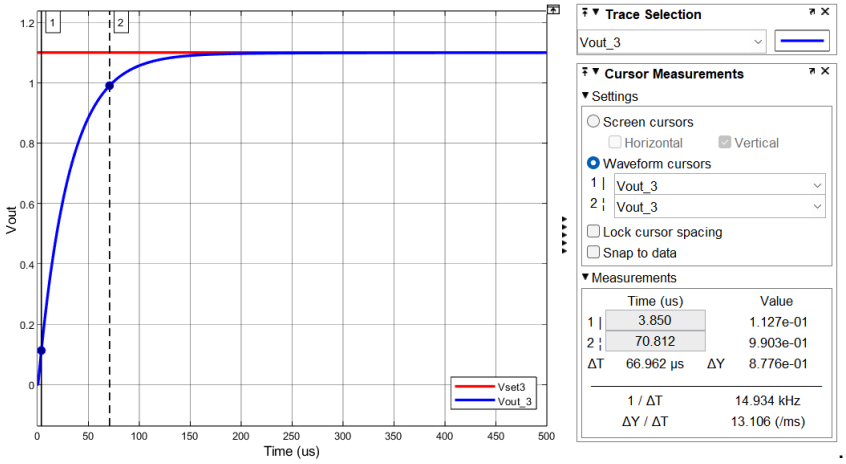

Figure 31: Rise time at operating point I_{load} = 910 µA.

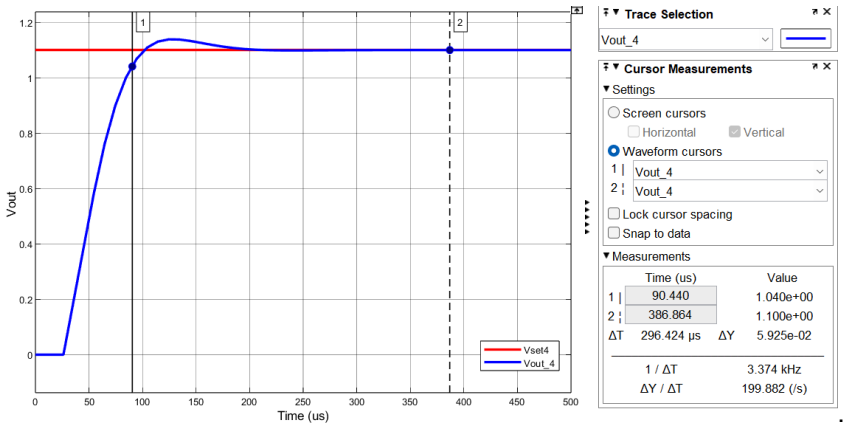

Figure 32: Settling time and overshoot at operating point I_{load} = 20 µA.

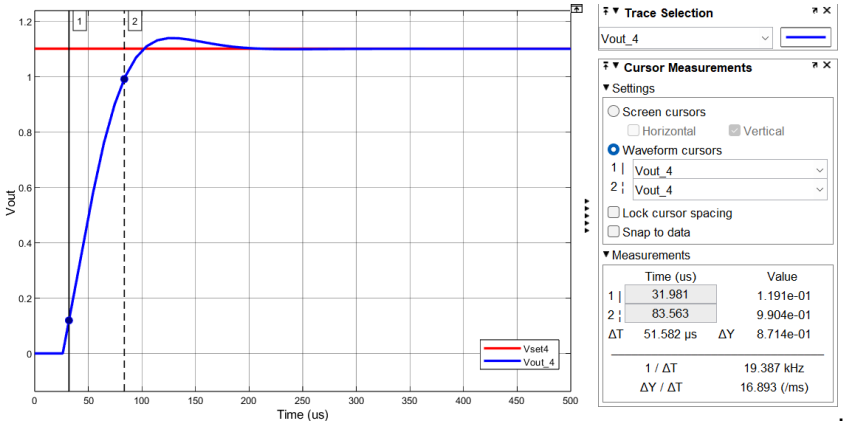

Figure 33: Rise time at operating point I_{load} = 20 µA.

D.4.7. Additional simulation results of the non-ideal control loop

Additional input voltage condition simulation results:

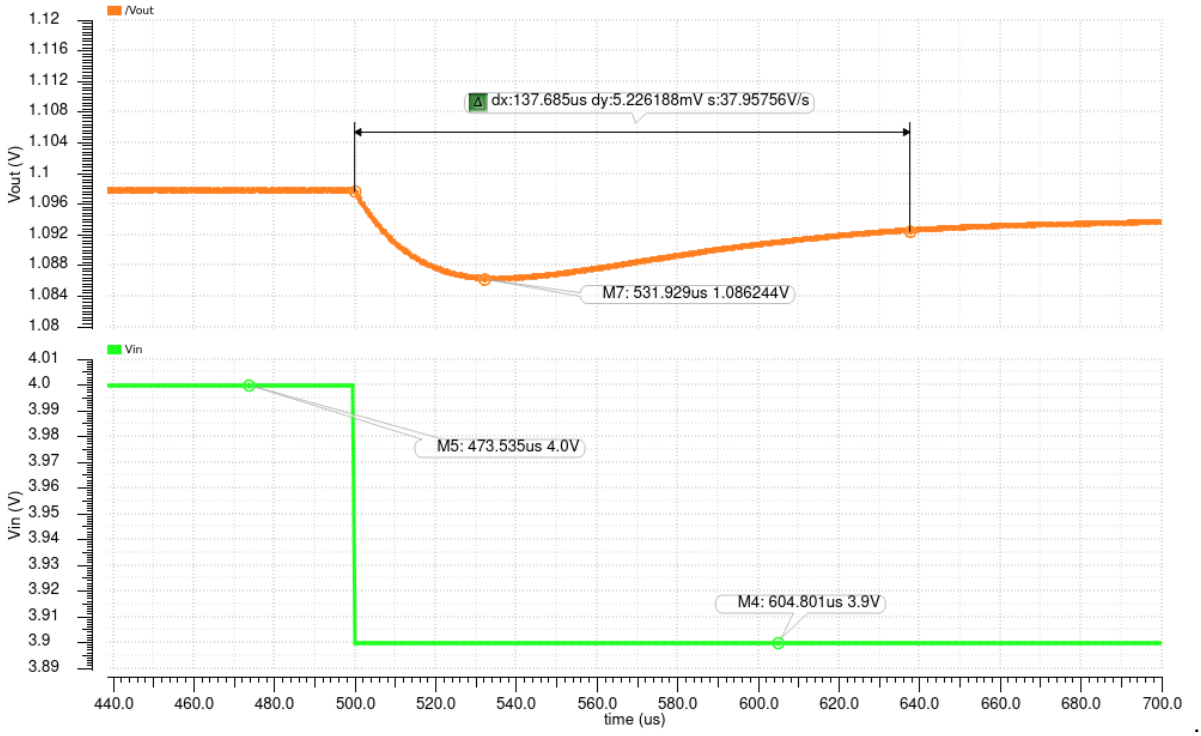

Figure 34: Small input step from 4 V to 3.9 V.

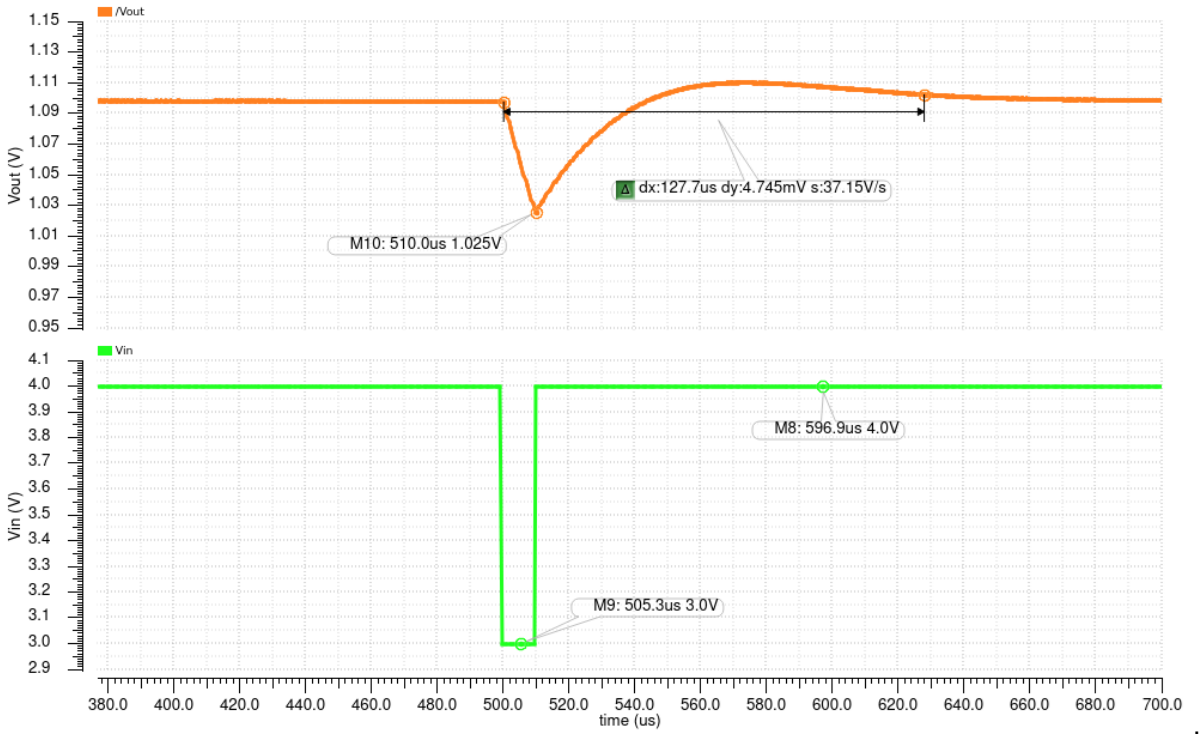

Figure 35: Large input voltage variation from 4 V to 3 V to 4 V.

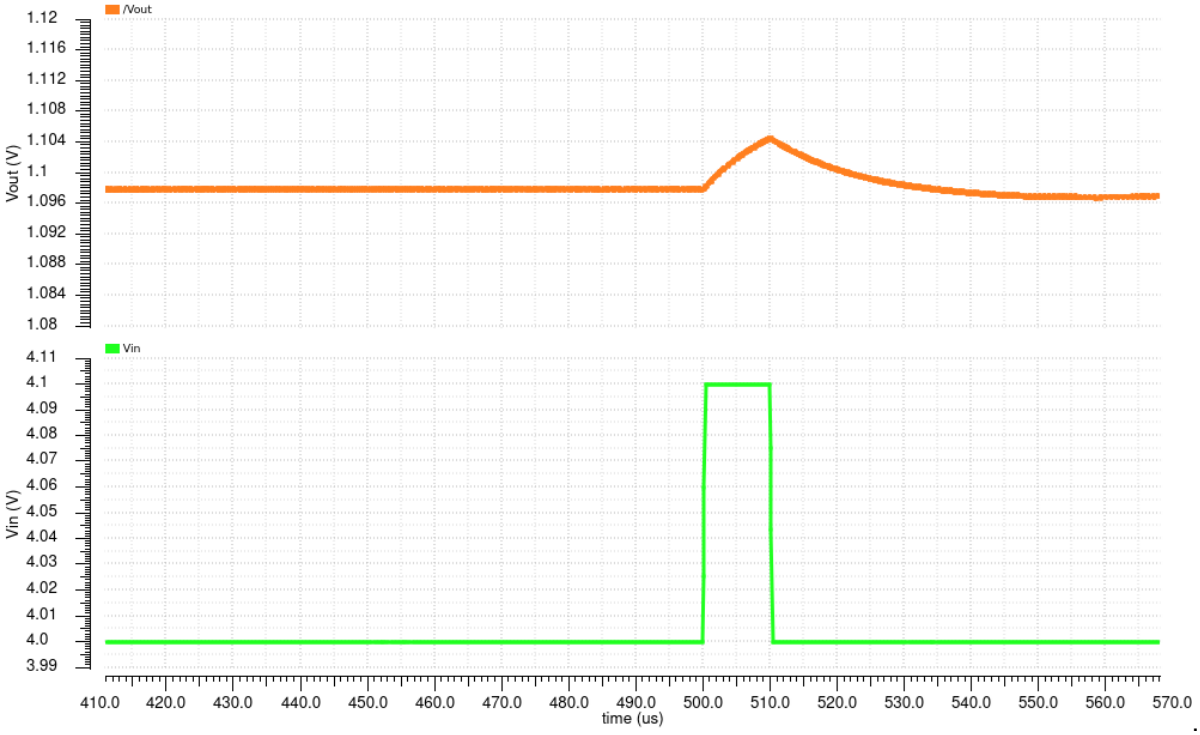

Figure 36: Large input voltage variation from 4 V to 4.1 V to 4 V.

Additional load condition simulation results:

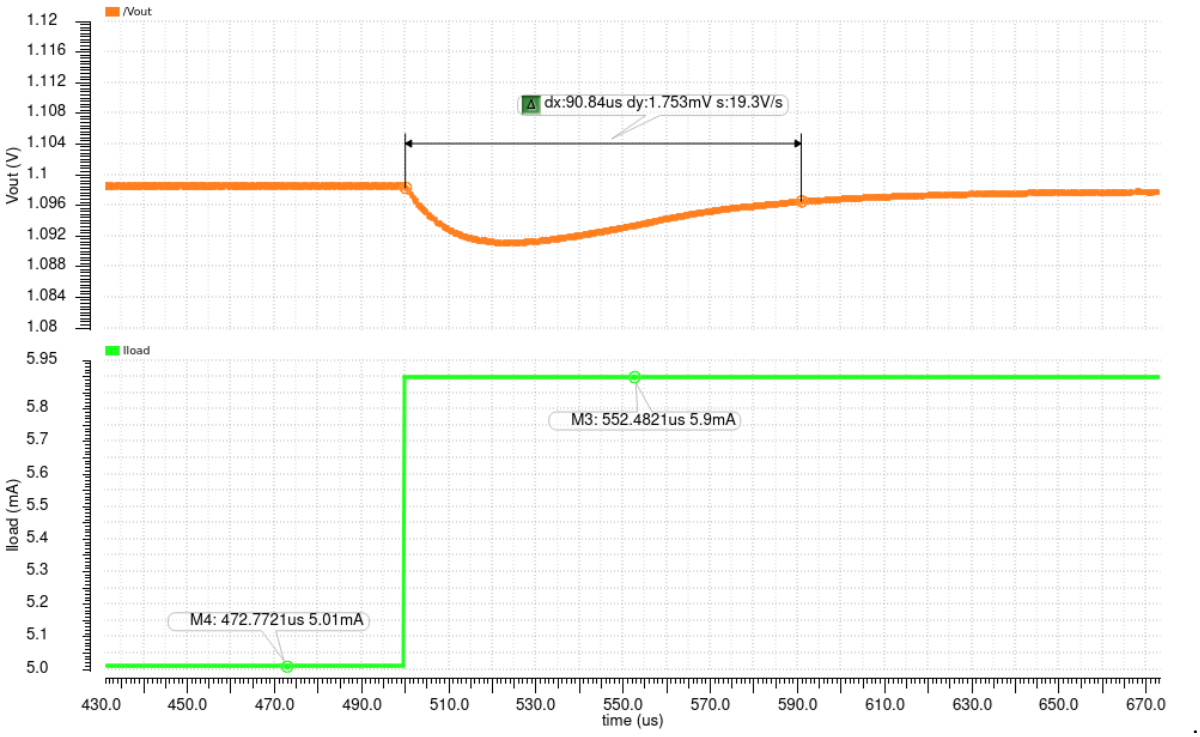

Figure 37: Fast load current step from 5.01 mA to 5.9 mA.

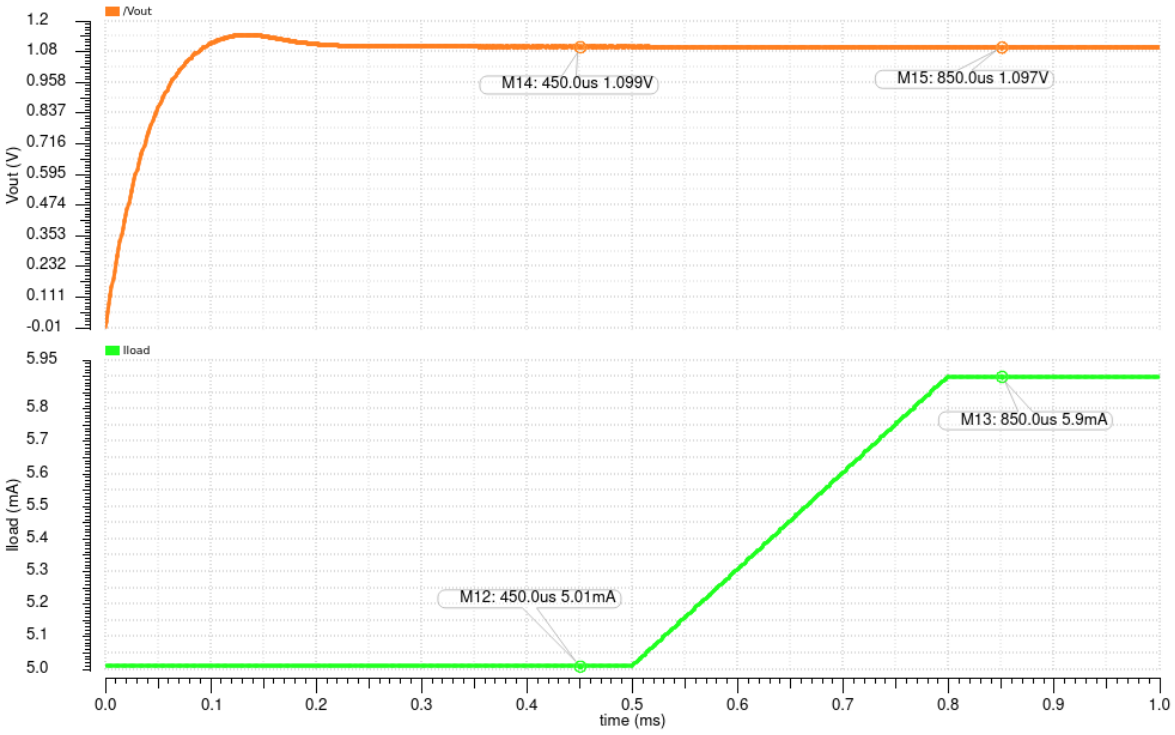

Figure 38: Slow load current step from 5.01 mA to 5.9 mA.

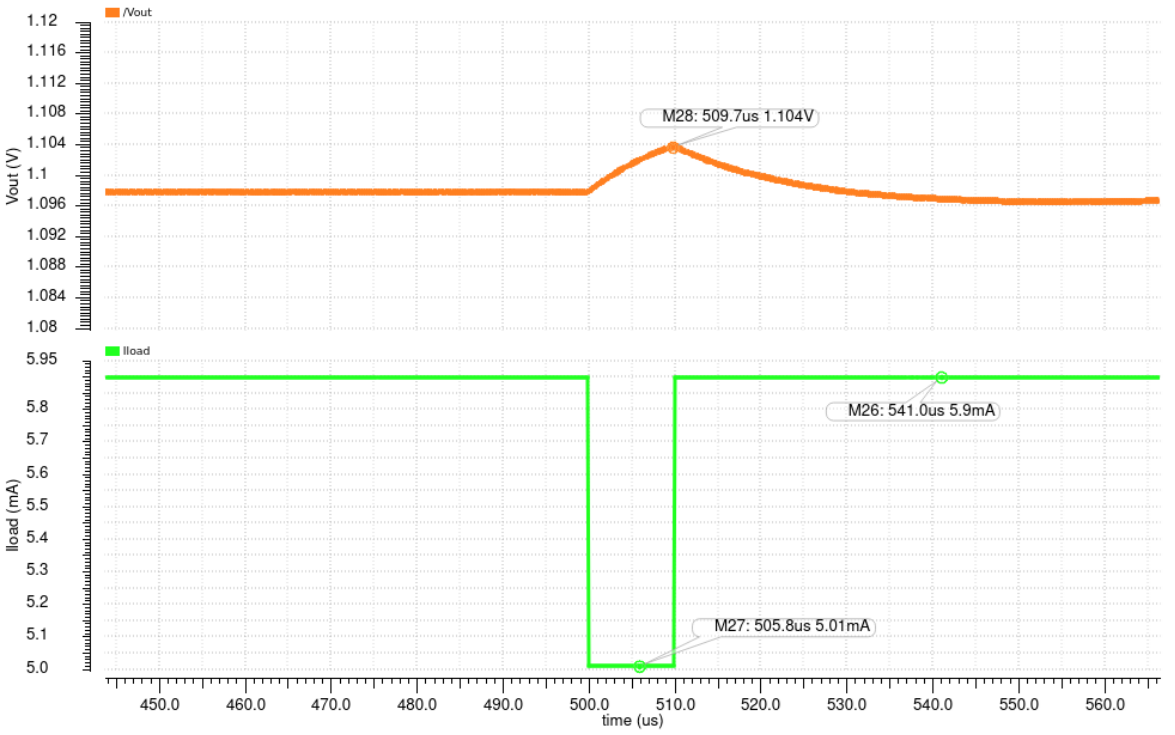

Figure 39: Load current variation from 5.9 mA to 5.01 mA and back to 5.9 mA.

Simulation results for obtaining line and load regulation plots
For load regulation:

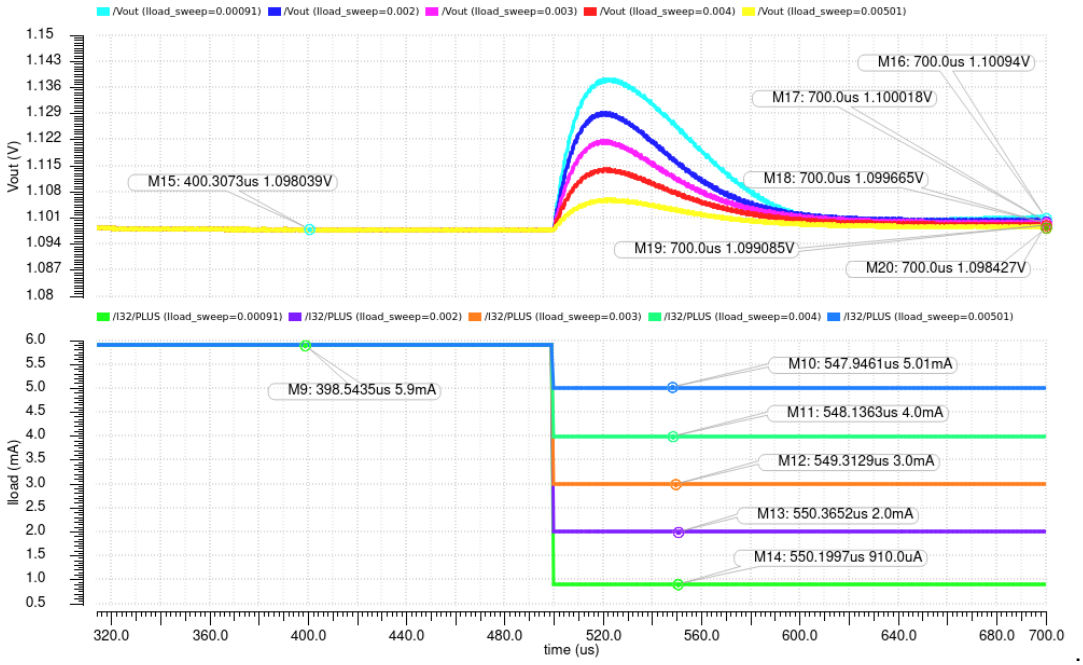

Figure 40: Load current sweeping from 910 µA to 5.9 mA (part 1).

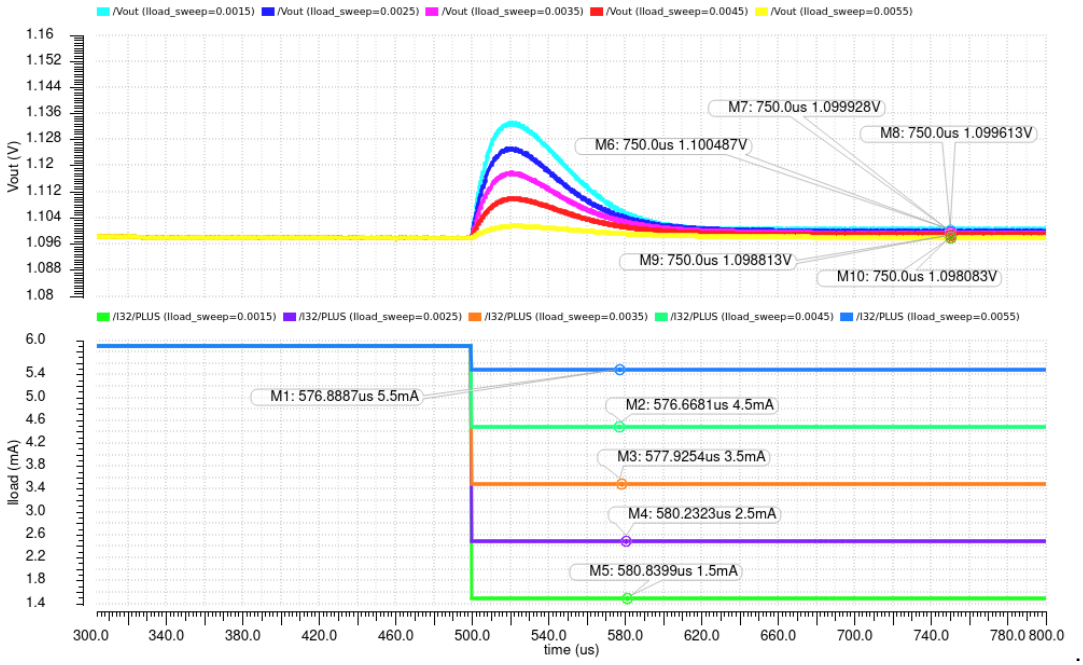

Figure 41: Load current sweeping from 910 µA to 5.9 mA (part 2).

For line regulation:

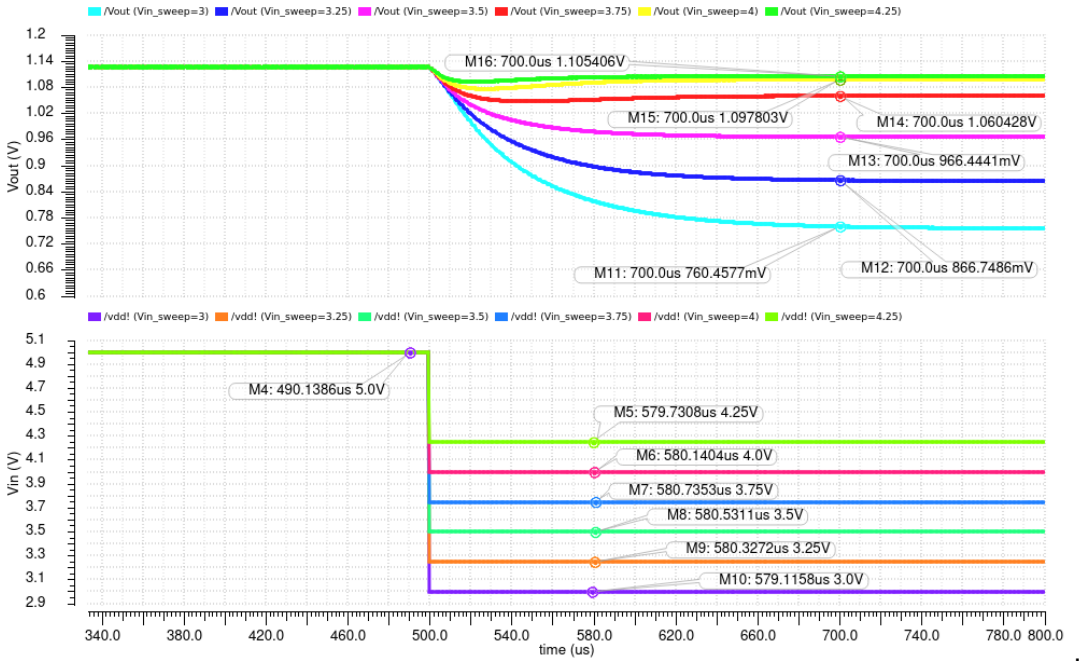

Figure 42: Input voltage sweeping from 3 V to 4.25 V starting at 5 V (part 1).

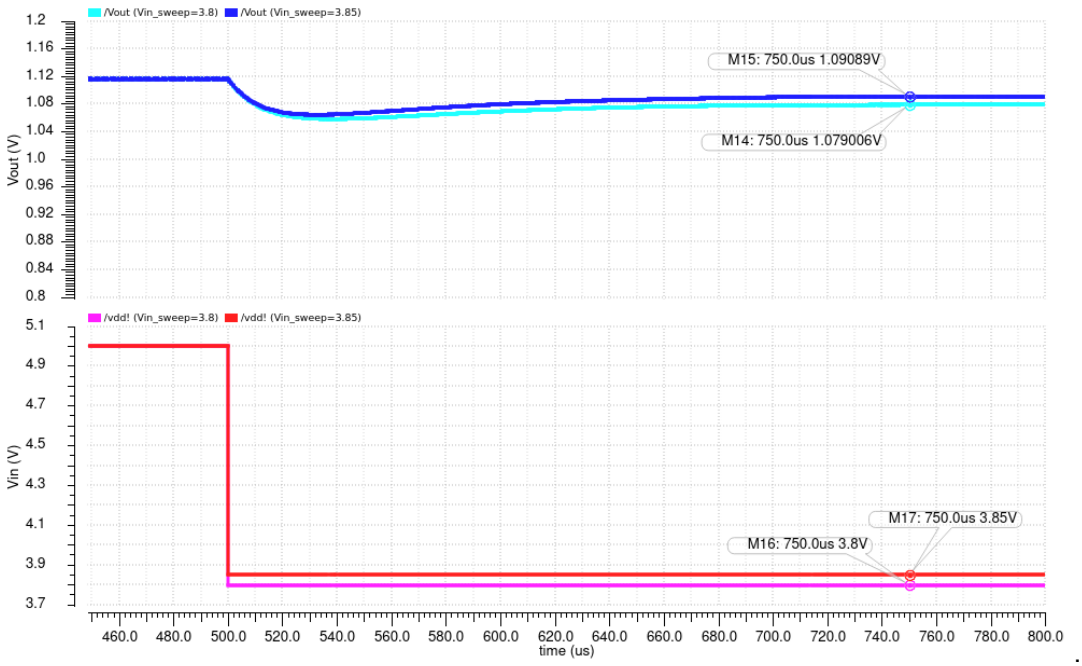

Figure 43: Input voltage sweeping from 3 V to 4.25 V starting at 5 V (part 2).

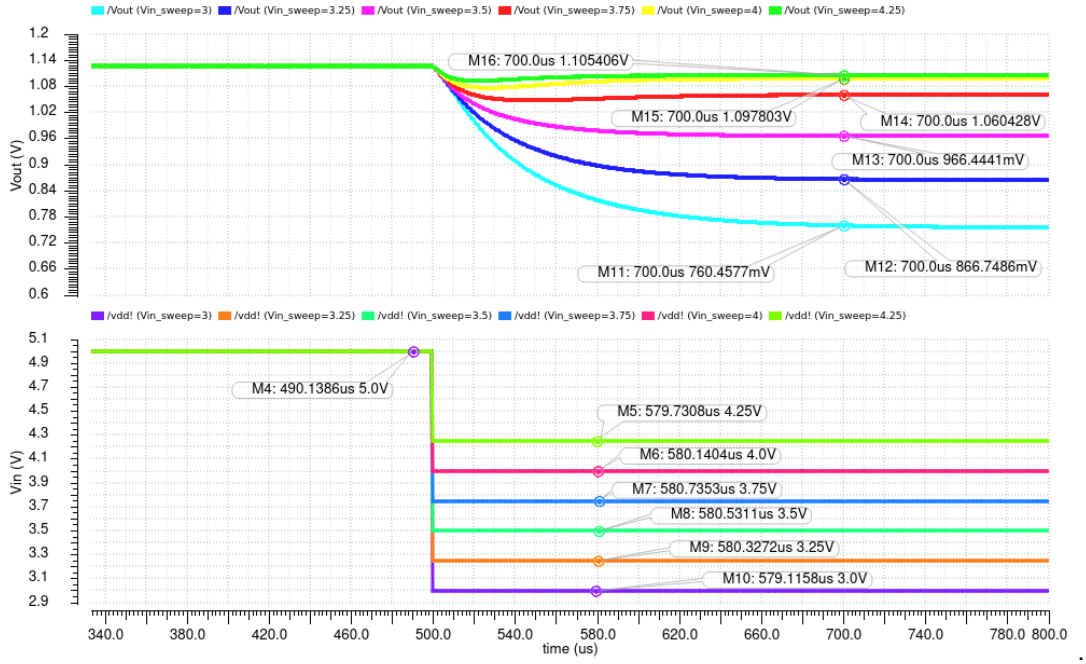

Figure 44: Input voltage sweeping from 4.25 V to 5 V starting at 5 V (part 3).