Development of Wafer Level Package Platform for High Reliability Crossover MCUs

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Abstract

Fan in and fan out wafer level packages are primarily used in the industry for applications in handheld consumer electronic products. The key benefits of wafer level package (WLP) are small form factor, reduced cost, improved electrical and thermal performance. WLP investigated in this study are directly surface mounted on PCB and have no intermediate substrate. Direct mount of package on PCB, leads to significant CTE mismatch between the package and board which stresses the package solder joint, leading to cyclic fatigue induced solder joint cracking. To overcome the solder joint cracking, stiffer solder alloys have been evaluated. However, higher stiffness of the solder alloy shifts the cyclic stress induced failure, from the solder joint to the package metal interconnect layers. Moreover, WLP on advanced silicon node have fragile low-k and extremely low-k back end of line dielectric layers that also crack or delaminate in cyclic fatigue.
In this work extensive WLP platform development has been done with following DOE variables; multi-layer package routing, dielectric materials, die thickness, PCB design. Developed packages passed and outperformed the following product reliability qualification conditions - high temperature storage life (150°C, 1000 hours), highly accelerated stress test (110°C / 85%RH / Bias, 264 hours), component level temperature cycling (-55 °C to 125 °C, 1000 cycles), board level temperature cycling (-40 °C to 125 °C, 500 cycles) and board level drop test (1500g/0.5ms, 30 drops). Excellent reliability, functional performance, and successful chip package integration was achieved for WLP for crossover MCU products.

Key words

Wafer level package, reliability, chip-package integration

I. Introduction

Over the past few years, the fan out wafer level package (FOWLP) platform has gained a lot of traction for consumer and hand-held electronic applications. Key FOWLP benefits are:

1. The absence of packaging substrate or reduced substrate layer count enables a smaller footprint area and package thickness.
2. Lack of organic substrate leads to shorter heat dissipation, interconnect path from die to printed circuit board (PCB), thus enabling better thermal and electrical performance of the package.
3. Wafer fab-like fabrication process leads to good process tolerance for high density and fine pitch package interconnects.
4. A low loss and tightly controlled package interconnect scheme also enable the excellent electrical performance of integrated packages, with significantly reduced package interconnect parasitic loss.

There are different flavors of FOWLP that have been developed and exist in the industry today [1-4]. Traditional wafer level fan out is a die first, die down FOWLP that has been in volume production for low end baseband, PMIC, Codec, Wi-Fi, RF kind of applications [1]. A die up high-density fan out package process was developed that found adoption for mobile phone processors and DRAM in a package-on-package format [4]. For the high density fan out package, multiple redistribution layers at a relatively fine pitch and high interconnect density are used. To date, most of the traditional wafer level fan out products are limited to single package interconnect layers. Both FOWLP and fan in wafer level package (FIWLP) have limitations in achieving good board level reliability (BLR) performance. During board level temperature cycling (BL-TC), both fan-in and fan-out wafer level packages have solder joint cracking as the dominant failure mode. Solder joint cracking results from the cyclic fatigue stress on the solder ball interconnects during board-level temperature cycling. The stress arises due to the coefficient of thermal expansion mismatch between

the wafer level package and the printed circuit board [5]. Stiffer solder alloys have been evaluated to minimize the fatigue damage due to cyclic stress and thus improve the solder joint fatigue life [6]. However, the higher stiffness of the solder moves the induced cyclic stress and failure from the solder joint to the package RDL trace [7]. Wafer level packages for advanced silicon nodes have fragile low-k and extremely low-k (ELK) back end of line (BEOL) dielectric layers that can crack or delaminate in cyclic fatigue [8]. The focus of this work is to improve the reliability of FOWLP, FIWLP. Design of experiment involving different dielectric materials, die thickness, PCB design, package interconnect layers were done to assess package reliability.

II. Package Development Details

Fig. 1 shows the overall fan out package process flow used in this work. The incoming silicon wafer was background to desired silicon thickness followed by laser groove and mechanical saw process. For the advanced node silicon used in the work with ELK/LK BEOL layers, both laser groove and mechanical saw were used to ensure BEOL integrity, and a defect-free die saw process. After die saw the known good die from the fab wafer map were picked and placed active side down on the metal carrier wafer. The die placement and spacing on the metal carrier were determined by the final FOWLP design. After die pick and place, the wafer was molded, and the carrier wafer was removed. This step is followed by a package redistribution layer fabrication process with six or five lithography layers to form the Under Bump Metallization (UBM) or no UBM design versions respectively. After RDL formation, the molded wafer was the background to final package thickness followed by solder ball drop and package singulation into individual units.

Figure 2 shows the FIWLP process flow. Dielectric 1, metal redistribution, dielectric 2 and under bump metallization (UBM) layers are fabricated by wafer lithography process, followed by wafer level solder ball drop. After which the wafer is the background to desired thickness and singulated into individual packages. Figure 3 shows the two FOWLP packages developed in this study. The package size is 7x7mm with 249 solder balls at 0.4mm solder ball pitch. The two packages have die/package area ratio of 0.36 and 0.41. The unique solder ball map below with depopulation at the outermost row is the result of product silicon/package/board co-design. Solder ball depopulation at the outermost row increased the reliability risk during BL-TC testing. To overcome BL-TC and the other associated package reliability, process risks an extensive DOE was evaluated. In our earlier work it was reported that BLR reliability is improved by using a stiff solder alloy with optimized package structure [9]. Reliability and process improvement in this work were evaluated through FOWLP DOE in table 1. DOE parameters are different dielectric, die thickness, PCB design, corner ball connect, no corner ball connect.

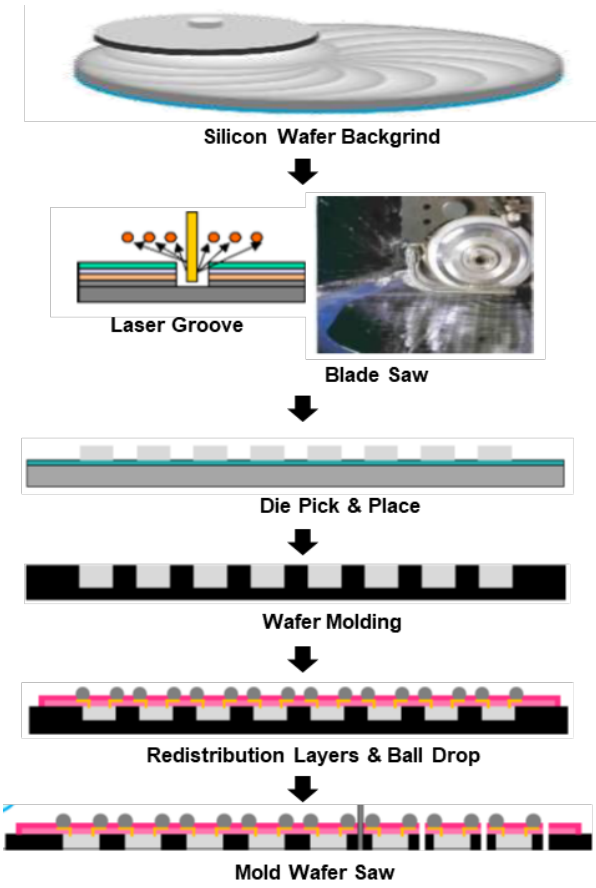

Fig. 1: FOWLP process flow

III. FOWLP Wafer Warpage Optimization

High FOWLP wafer warpage during FOWLP assembly process is a key risk. High wafer warpage issue is further acerbated for FOWLP that require multiple RDL. The FOWLP in this study required five lithography process steps for no UBM package: dielectric1, copper, dielectric 2, copper, dielectric 3 and six lithography process steps for with UBM package: dielectric 1, copper, dielectric 2, copper, dielectric 3, copper. Mold compound, dielectric materials need high temperature cure and have associated cure shrinkage, warpage which make in process FOWLP wafer warpage challenging. For FOWLP wafer warpage DOE, different die thickness, epoxy mold compound (EMC), die/package area ratio were evaluated. Silicon has a coefficient of thermal expansion (CTE) of ~3ppm, which is lower than all other package constituents like EMC, dielectric, copper. So, increase in silicon thickness, die/package area ratio will lead to a decrease in effective CTE of the FOWLP. Lowering of package CTE will increase CTE mismatch for package versus PCB, which will increase the BL-TC reliability risk. Solder joint reliability mechanical modelling was used to assess the solder joint fatigue risk comparison between the packages with die thickness of

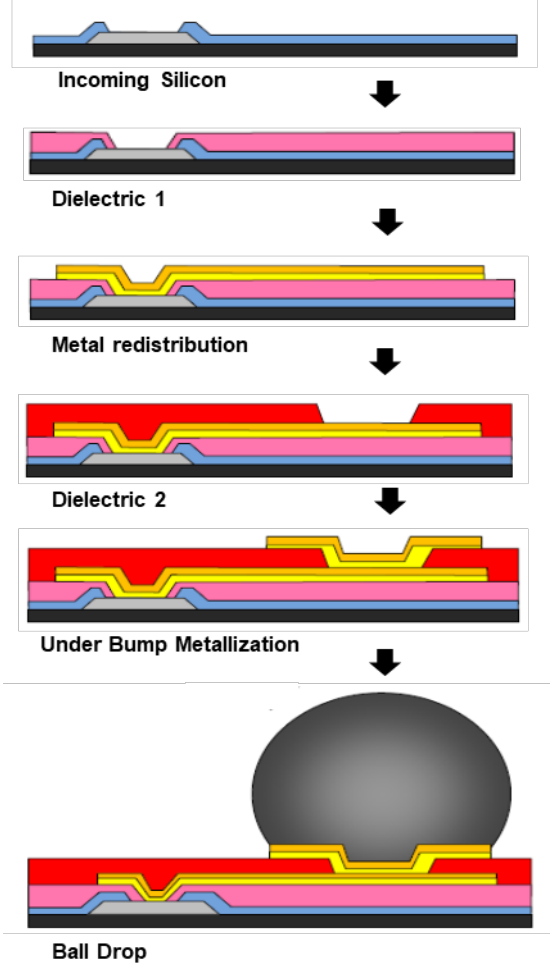

Fig. 2: FIWLP process flow

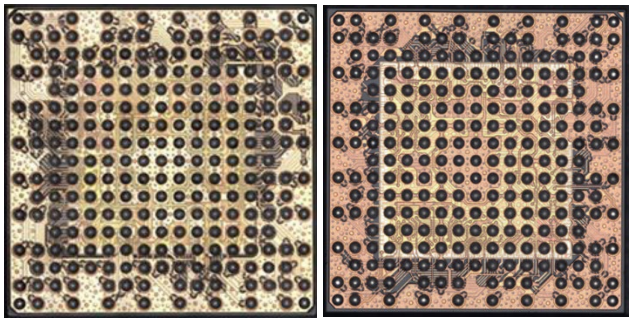

Fig. 3: 7x7mm FOWLP package, 249 I/O, 0.4mm ball pitch. (left) die/package ratio = 0.36 (right) die/package ratio = 0.41.

Table1: FOWLP DOE

DOE	REP	UBM	Die thickness	PCB	Corner ball connect
Leg 1	Diel 1	No	350 µm	10L	Yes
Leg 2	Diel 1	Yes	350 µm	10L	Yes
Leg 3	Diel 1	No	350 µm	10L	No
Leg 4	Diel 1	Yes	350 µm	10L	No
Leg 5	Diel 2	No	400 µm	8L	No
Leg 6	Diel 2	Yes	400 µm	8L	No

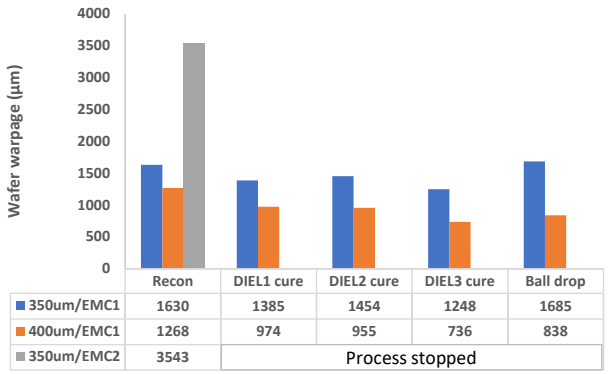

Fig.4: FOWLP wafer warpage at different in process stages. Die/package ratio = 0.36. For DOE leg with EMC2, the wafer warpage was 3543µm, after reconstitution stage, which was higher than spec of 3000µm. Further process was stopped.

Table 2: % change in FOWLP wafer warpage at different in process stages when the die thickness changes from 350µm to 400 µm.

In process stage	Recon	DIEL1 cure	DIEL2 cure	DIEL3 cure	Ball drop
% change	-22%	-30%	-34%	-41%	-50%

350µm and 400µm. Die/package area ratio was 0.41. A change in die thickness from 350µm to 400µm die was predicted to result in ~5% decrease in BL-TC solder joint fatigue life. Fig. 4 shows the results of FOWLP wafer warpage variation with different die thickness and EMC. For EMC2 the wafer warpage was outside spec of 3000µm after wafer reconstitution (recon) and post mold cure (PMC) stage, so further process was stopped. During wafer mold, PMC stage the warpage is dominated by mold compound shrinkage which was too high for EMC2. Table 2 shows FOWLP wafer warpage changes at different in process stages when die thickness changes from 350µm to 400 µm. The wafer warpage change (decrease) becomes more prominent as wafer moves downstream in the FOWLP process from reconstitution to DIEL1 to DIEL2 to DIEL3 to ball drop stages. As next step, wafer warpage was evaluated as a function of die/package area ratio. Fig. 5, shows the results. The warpage behavior is complex. At the wafer reconstitution stage the higher die/package ratio leads to less warpage. At the wafer reconstitution stage, the warpage is measured after post mold cure and warpage is mainly determined by mold compound shrinkage. A higher die/package ratio reduces the amount of mold compound and thus leads to less warpage. However, from DIEL1, DIEL2, DIEL3 to ball drop the warpage is determined primarily by the CTE mismatch between the different package constituents. Since silicon has the highest CTE mismatch with mold compound, dielectric, a higher die/package ratio leads to higher CTE mismatch and thus higher warpage.

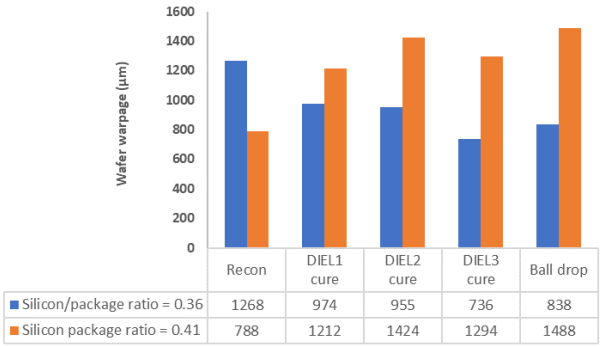

Fig. 5: In process FOWLP wafer warpage for die/package area ratio of 0.36 and 0.41. Die thickness = 400µm.

Table 3: % change in FOWLP wafer warpage at different in process stages when the die/package area ratio changes from 0.36 to 0.41. Die thickness = 400µm.

In process stage	Recon	DIEL1 cure	DIEL2 cure	DIEL3 cure	Ball drop
% change	-38%	24%	49%	76%	78%

Table 3 summarizes the relative wafer warpage change at different in process FOWLP stages. However, in process wafer warpage does not lead to any issues for unit package warpage. Fig. 6 below shows unit package warpage variation through a lead-free solder reflow temperature cycle. Higher silicon thickness of 400µm, leads to increased package stiffness and lower package warpage. Fig. 7 shows, Shadow Moire package warpage data at different temperature.

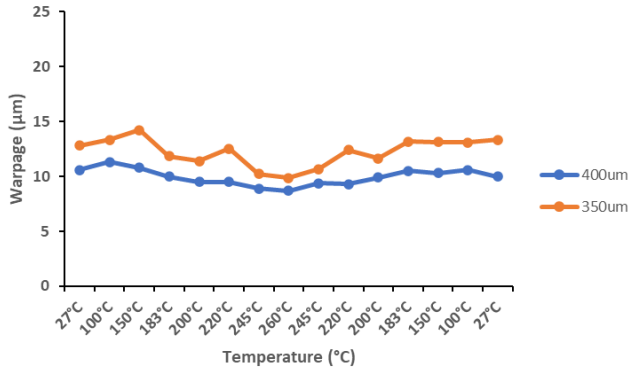

Fig. 6: Unit package warpage profile for room temperature to reflow temperature to room temperature for die thickness of 350µm and 400µm. Package warpage is well within spec of max warpage = 50µm.

IV. Package Reliability Results

Table 4 shows the reliability test conditions that the developed FOWLP passed and qualified. Based on results published earlier stiff solder alloy led to significant improvement in solder joint reliability [9]. In this work stiff

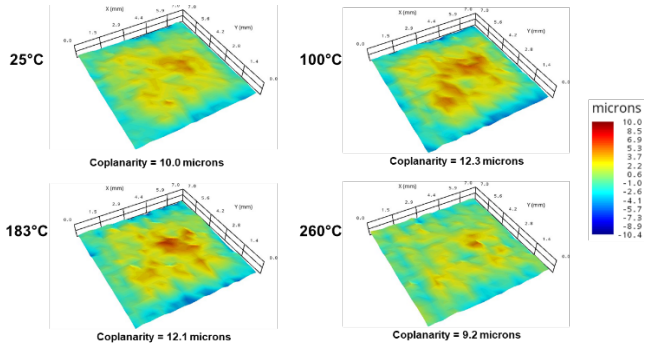

Fig.7: Shadow Moire package warpage data at different temperature. Silicon thickness = 400µm.

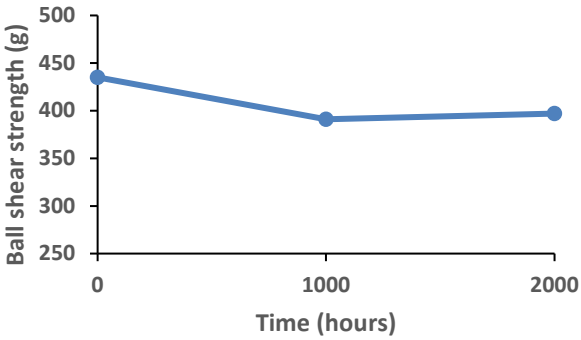

Fig. 8: Solder ball shear strength at time = 0 and after high temperature storage (HTS) at 150°C for 1000 hours and 2000 hours.

Table 4: Reliability test conditions that the developed FOWLP passed and qualified. Both UBM and no UBM versions of packages passed all reliability.

Test	Condition	Zero fail criteria	Result
Temperature cycling (TC)	Ta = -55°C to 125°C	1000 cycles	Pass
Highly Accelerated Stress Test (HAST)	110°C / 85%RH/3.3V	264 h	Pass
High Temperature Storage Life (HTSL)	Ta = 150°C	1000 h	Pass
Board Level Temperature Cycling (BL-TC)	Ta = -40°C to 125°C	1500 cycles	Pass
Drop Impact Test	1500 g / 0.5 ms	15 drops	Pass

solder alloy was used for package development and qualification. Figure 8 shows solder ball shear strength at time = 0 and after HTS at 150°C for 1000 hours and 2000 hours. For solder ball pad diameter of 250µm, the solder ball shear strength spec is 157g. At time = 0, the solder ball has 435g of shear strength. After 150°C, 2000 hours aging only ~10% degradation in shear strength is observed. Board level drop test was done on both with UBM and without UBM packages. Drop test was done as per JESD22-B111A spec. PCB was 10L copper, 1mm thickness. Packages were tested

up to 1000 drops. Fig. 9 and 10 show failures modes for no UBM and UBM packages. For early, middle, and late failed samples, the failure mode was PCB trace cracking. No package related failures could be found. The packages due to the robust structure do not fail and instead induce PCB fails.

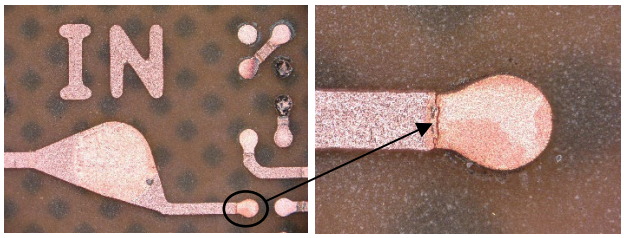

Fig. 9: No UBM drop test failure analysis. Drop test was done till 1000 drops. PCB trace cracking was failure mode for early, middle, and late failed samples. There were no package related failures.

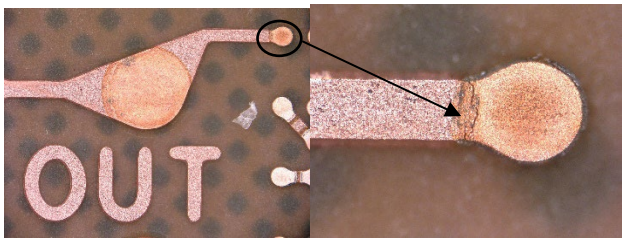

Fig. 10: UBM drop test failure analysis. Drop test was done till 1000 drops. PCB trace cracking was failure mode for early, middle, and late failed samples. There were no package related failures.

Table 5 below compares BL-TC characteristic life (~63.2% fail) for the different FOWLP DOE legs. BL-TC was done as per JEDEC spec JESD22-B111. PCB was 1mm thick with 10L copper metal for legs 1, 2, 3, 4 and 8L copper metal for legs 5 and 6. For legs 1-4, diel 1, die thickness = 350µm and 10L PCB are used. For connected solder ball UBM leads to

Table 5: BL-TC CZ life (~63.2% fail) comparison between the different FOWLP DOE legs.

DOE	REP	UBM	Die thickness	PCB	Corner ball connect	CZ life (~63.2% fail)
Leg 1	Diel 1	No	350 µm	10L	Yes	2795c
Leg 2	Diel 1	Yes	350 µm	10L	Yes	3592c
Leg 3	Diel 1	No	350 µm	10L	No	2857c
Leg 4	Diel 1	Yes	350 µm	10L	No	3803c
Leg 5	Diel 2	No	400 µm	8L	No	2963c
Leg 6	Diel 2	Yes	400 µm	8L	No	4224c

29% improvement in CZ life versus no UBM (leg 2 vs leg 1). For no corner ball connect UBM leads to 33% improvement in CZ life versus no UBM (leg 4 vs leg 3). For legs 5, 6, diel 2, die thickness = 400µm and 8L PCB are used. For this no corner ball connect case UBM leads to 42% improvement in CZ life versus no UBM (leg 6 vs leg 5).

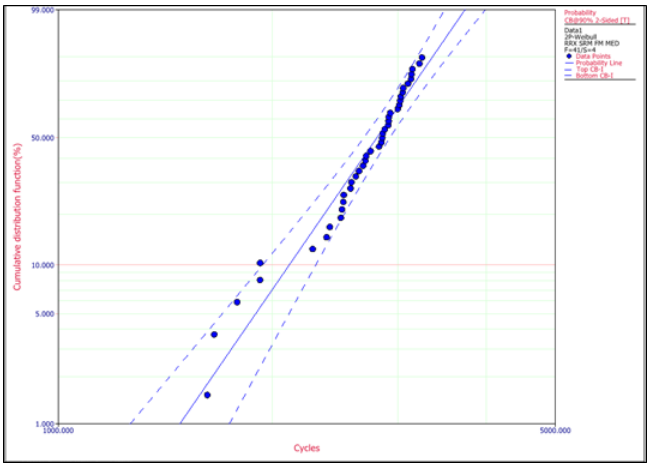

Fig. 11: BL-TC Weibull plots from DOE leg 5.

Fig. 11 shows BL-TC Weibull plots from DOE leg 5. First failure is at 1621c. BL-TC for leg 6 is still ongoing. First fail was at 1886c, and CZ life is 4224c. Failure analysis from above DOE legs is planned to be done.

Fig 12 shows FIWLP developed in this study. Table 6 shows the reliability test conditions that the package was qualified for. In FIWLP the use of very stiff alloy solder ball does not lead to solder ball failure but rather transfers the solder ball stress to package RDL, inducing RDL cracking failure [10]. On the other hand, usage of incrementally more stiff solder alloys does not necessarily lead to improvement in solder join reliability because of significant variability in creep strength of the solder alloy [11]. Fig. 13 shows the cross section of failed sample after BL-TC. Failure mode is bulk solder ball fracture at the package side, which is the typical failure mode. The package showed excellent board level drop test reliability and no failure was detected up to 1000 drops. Drop test was done as per JESD22-B111A spec. PCB was 10L copper, 1mm thickness.

VI. Conclusion

Multi-layer FOWLP are developed that were qualified to stringent reliability conditions. For muti-layer FOWLP in process wafer warpage is a key challenge, which was optimized using different EMC, die thickness, die/package ratio. Due to die/package/board co design the FOWLP had a ball map that was challenging for BLR. Stiff solder alloy was used to improve solder joint reliability. However stiffer solder alloy changes failure mode to package RDL cracking so appropriate dielectric materials and package RDL stack up were evaluated to ensure complete chip/package integration. Developed FIWLP also passed all reliability qual conditions. However, for FIWLP it is quite challenging to use stiff solder alloys for BLR improvement because the

stress due to stiff solder ball is quite high and leads to early RDL crack failures. Work is currently ongoing to improve FIWLP BLR by using combination of stiff solder alloys and different dielectric materials and RDL stack ups.

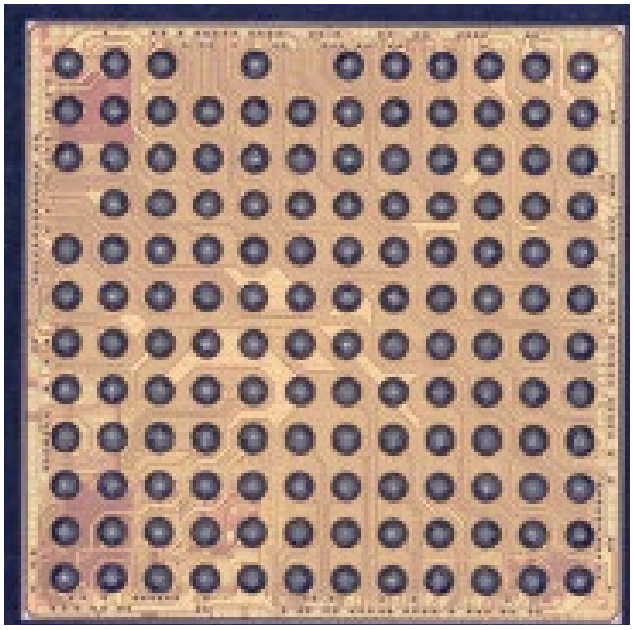

Fig.12: Developed FIWLP. Die size = 21mm^2 at 0.35mm solder ball pitch, solder ball count = 141. Some depopulation had to be done at outermost row to enable product PCB routing.

Table 6: Reliability test conditions that the developed FIWLP passed and qualified.

Test	Condition	Zero fail criteria	Result
Temperature cycling (TC)	Ta = -55°C to 125°C	1000 cycles	Pass
Highly Accelerated Stress Test (HAST)	110°C / 85%RH/3.3V	264 h	Pass
High Temperature Storage Life (HTSL)	Ta = 150°C	1000 h	Pass
Board Level Temperature Cycling (BL-TC)	Ta = -40°C to 125°C	500 cycles	Pass
Drop Impact Test	1500 g / 0.5 ms	30 drops	Pass

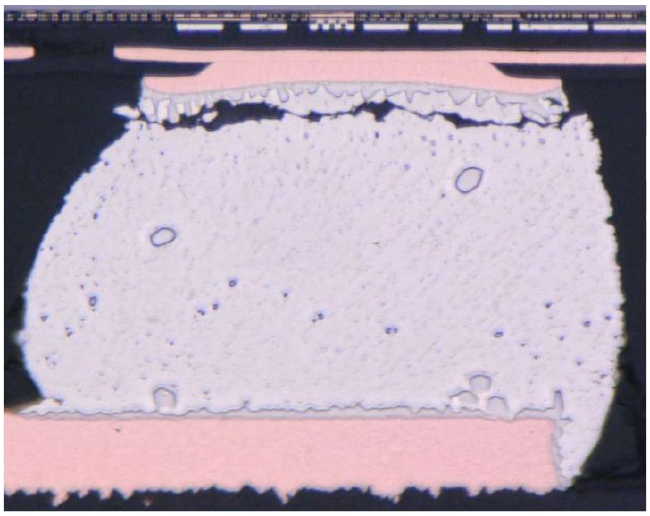

Fig. 13: Solder joint FA after BL-TC for FIWLP. Failure mode is bulk solder joint cracking near to package.

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