Power System: Lunar Zebro Rover Deployment System

The lifeline of the Rover Deployment System

Bachelor Graduation Thesis

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by

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Abstract

This thesis details the design and development of the Power System for the Rover Deployment System. This power system delivers and manages the necessary power required by the entire Rover Deployment System. The RDS is responsible for ensuring the rover's survival inside the transportation pod during transit. It also handles releasing the rover, which a mechanical mechanism will lower onto the lunar surface. The goal of Lunar Zebro is to send a nanosatellite to the moon for lunar surface exploration and radiation measurements.

The power system was designed to power the MCU and transceivers at $3.3V$, to provide power for rover charging at $12V$, and to charge a capacitor bank used to provide the necessary actuation power to the NEAs. An electrically triggered umbilical release mechanism, unfortunately, could not be implemented due to a lack of available data. The circuit for this system was created, simulated, and added to the PCB design of the RDS. The simulations of the circuit behaved desirably. Due to the lead time on orders, the PCB has unfortunately not been received yet. Because of this, the entire power system has unfortunately not been tested yet.

Preface

As the culmination of our undergraduate studies in Electrical Engineering, this thesis was prepared for the Bachelor's Graduation Project. This project was proposed by the Lunar Zebro research team. Its goal is to be the "world's smallest and lightest rover yet, built by TU Delft students"[75]. One of the necessary systems for this is the Rover Deployment System. Currently, the RDS team consists of mechanical students working on the mechanical aspects of the RDS. The RDS also requires a control system for communication, to direct power to the rover, and to deploy it. The design of this control system was the goal of this project.

This project could not have been possible without people willing to lend us their time and expertise to guide us during this project. The first person we would like to express our deep gratitude to is our supervisor and the project director for Lunar Zebro, Dr. Chris Verhoeven. While working on the 19th floor, we were always welcome to step into his office if we had a question. Through Dr. Verhoeven, we came into contact with the second person we would like to thank, namely Dr. Aditya Shekhar. His expertise in power electronics helped us design a large part of the voltage conversion portion of the system. We are grateful for the opportunity to finish our Bachelor's by adding something valuable to a research team like Lunar Zebro. They provided us with access to their facilities on the 19th floor, allowing us to work freely and comfortably. For this, we are extremely grateful. Some notable individuals on the team that we would like to thank are Project Leader Giannis Vardanikas, Chief Engineer and Head of System Engineers Ataberk Ayata, and RDS Engineer Sebastiaan Dirven. Last but not least, we would like to thank our colleagues, Diederik Aris, Henri Vanhuynegem, Noa Kant, and Tadjiro Velzel for an enjoyable and productive collaboration.

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Nomenclature

0.1. Abbreviations

Abbreviation	Definition
RDS	Rover Deployment System
NEA	Non-Explosive Actuators
HDRM	Hold Down Release Mechanism
BMS	Battery Management System
EPS	Electrical Power System
PS	Power System
MCU	Micro-Controller Unit
P-MOSFET / PMOS	P-channel Metal-Oxide Field Effect Transistor
N-MOSFET / NMOS	N-channel Metal-Oxide Field Effect Transistor
LDO	Linear Drop-Out
...	

Symbols

Symbol	Definition	Unit
V	Voltage	[volt]
R	Resistance	[Ω]
I	Current	[A]
C	Capacitance	[F]
t	Time	[s]
E	Energy	[J]
P	Power	[W]

1

Introduction

Lunar Zebro is ”World’s smallest and lightest rover yet, built by TU Delft students” [53]. The focus of the Lunar Zebro team is sending the rover to the moon as a piggyback payload, which is attached to a lunar lander. After the lander makes contact with the lunar surface, it will send a signal indicating that the Rover Deployment System (RDS) should release the rover onto the lunar surface. Thus, the primary goal of the RDS is to release the rover onto the lunar surface upon receiving a deployment signal. The rover must not be released at any other moment.

During the early stages of RDS development, the need arose for an electrical system that controls the mechanical system, allows the rover to communicate with the lander, and provides power from the lander to the rover. This functionality is crucial to the success of the entire mission, indicating the critical role of the RDS electronic subpart.

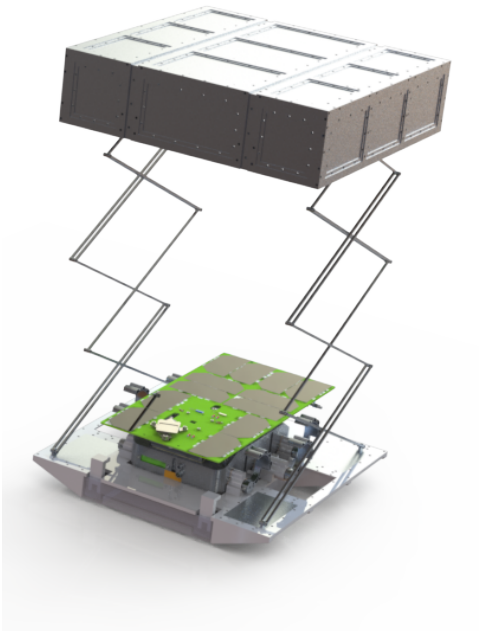

Figure 1.1: Rover Deployment System

1.1. State-of-the-Art Analysis

Space exploration started in 1957 and has since grown into a 630 billion dollar industry [73]. Large agencies such as NASA and ESA are developing various projects to extend human knowledge about extraterrestrial life. These agencies develop products with similar goals as the Lunar Zebro rover, such as nanosatellites, which also weigh between 1-10 kg and operate in the same harsh environments[58]. These nanosatellites are deployed into space to orbit in the Low Earth Orbit zone, which lies between 200 to 2,000 kilometres above Earth. The product most similar to the Lunar Zebro RDS is the deployment system used for these nanosatellites. An example would be the ISIPOD CubeSat Deployer, created by ISISPACE [46]. However, very little information about their control systems is publicly accessible. Many space agencies maintain large amounts of proprietary information, which makes it difficult to find information about their electrical control systems.

1.2. Purpose and Scope

The goal of the Rover Deployment System is to deploy the Lunar Zebro rover to the surface of the moon, as written in the system overview (Chapter 2). Non explosive actuators have been used in state of the art space applications such as the release of the solar panels, primary and secondary mirror assemblies

of the James Webb Space Telescope [31]. However, they have never been used to deploy a vehicle to the lunar surface. Therefore, methodical development of this system is crucial to the success of the Lunar Zebro mission.

The success of the mission depends on the RDS' ability to withstand the harsh environment of space, including temperatures ranging from -170 to 130 degrees Celsius [55], high acceleration during transport and low amounts of available power. Furthermore, the large cost of transporting mass to the lunar surface, and Lunar Zebro's future ambitions towards robotic swarming, underline the need for a lightweight system. Therefore, developing the RDS control system not only requires a combination of expertise in low power engineering, electronics design, and embedded systems, but also requires extensive knowledge of robust, reliable, and lightweight design.

Lunar Zebro aims to launch their rover at the end of 2025. Considering this system is crucial in order to achieve mission success, there is high urgency for a first draft design, which can subsequently be optimised and certified.

1.2.1. Stakeholders and Users

The main stakeholder for this project is the Lunar Zebro student research team, as this team provides the context in which the project takes place. The insights and methodologies developed here could be used as a basis for future Lunar Zebro projects and contribute to the broader field of electronic systems for space deployment mechanisms. Other major stakeholders are also the other two bachelor project teams working on the rest of the RDS control system, as clear communication between these groups is essential for a good design.

Another stakeholder is the company responsible for the lunar lander. As the Lunar Zebro mission is a piggyback mission, it is important that the design is cleared before it is launched. It is therefore important the design achieves the necessary certifications. However, which lunar lander will be used for the definitive launch is unknown during this project.

1.3. Thesis synopsis

This thesis will cover the power system (PS) of the RDS control system. The power that is required by each subsystem or module will be delivered and regulated accordingly by the power system. The system will use control signals received from the microcontroller and will provide power to the actuation and sensing system. The system and its place in the RDS control system will be further elaborated upon in chapter 2. The microcontroller that needs to be programmed for control and communication along with the sensing and actuation will not be treated here as they fall outside of the scope of this thesis. These systems will be designed by other sub-groups of the BAP group. For details about these design the the thesis of the two other subgroups must be consulted.

2

System Overview

The Rover Deployment System was designed with three objectives:

1. Deploy the Lunar Zebro rover on the surface of the moon.
2. Provide power from the lander to the rover during transit when needed.
3. Function as an intermediary for communication between the rover and the lander.

The RDS can only function properly if each system fulfills its designated role to achieve these objectives. The Power Flow System is one of the main systems of the RDS. This chapter, System Overview, serves as an explanation of the PS's role and position in the RDS. As stated in the Introduction, the RDS is made up of three subsystems. The entire RDS with these subsystems can be seen in figure 2.1. In this overview, the Power System is marked in red.

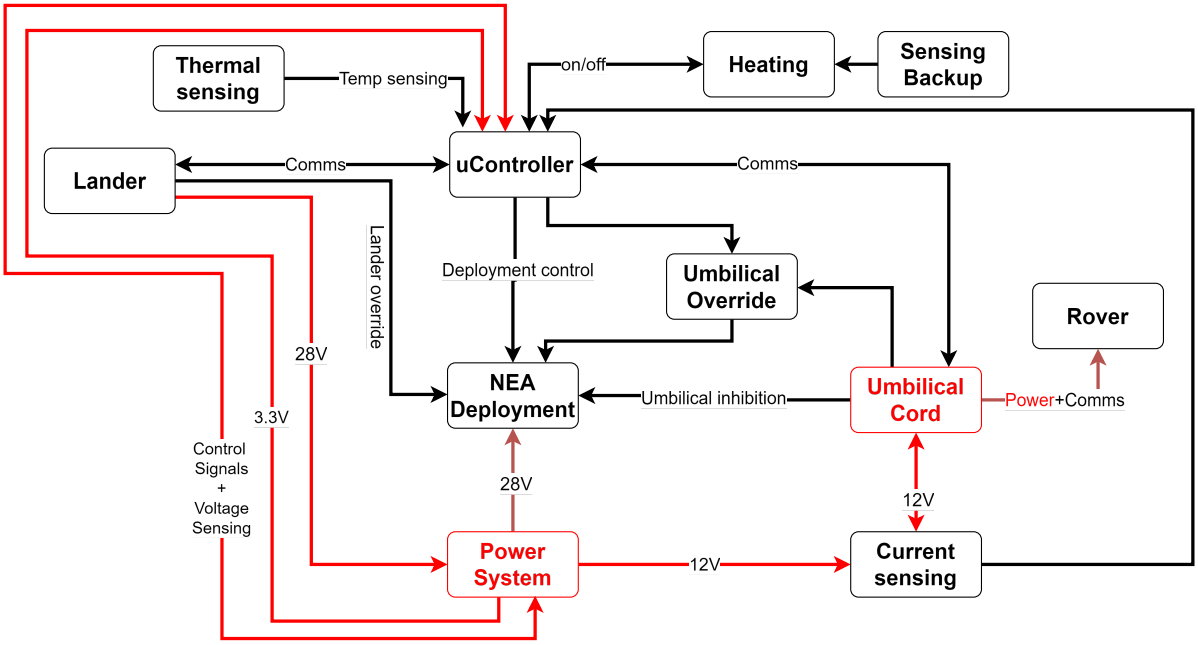

Figure 2.1: RDS and subsystem Overview

Figure 2.1 displays the connection between the PS and the MCU, lander, NEA, and rover. The connection between the lander and the PS serves as the input of the system. The lander provides the PS with $3W$ of power at $28V$. The PS's job is to then apply the appropriate methods to ensure that the other subsystems connected to it, can function properly. The MCU and rover will be provided with the necessary power for the appropriate amount of time to make sure these systems work as optimally as

possible. The PS is also connected to the NEA. The NEA is an essential part of the RDS as it is the component that physically allows the rover to be released when fired. The NEAs used are actuators consisting of a fuse that requires a current spike for a certain amount of time to disintegrate, which then leads to the NEAs actuation. This peak in current flow will be provided by the PS to the NEAs. Parts of the output of PS will be connected to sensing and actuation modules. These can be placed between the PS and NEA to sense the voltage and current flow to the NEA. As can be seen in figure 2.1, the PS and rover are connected through an umbilical cord. This connector will support power flow from the PS to the rover and optionally vice versa. This cord will also be used as the communications connector responsible for transferring data between the MCU and rover.

3

Program of Requirements

3.1. Requirements Overview

3.1.1. RDS requirements

Any reliable and qualitative system has requirements that it must adhere to. The RDS system has multiple requirements which need to be satisfied. These requirements are essential for a successful Lunar Zebro mission. The RDS requirements can be split into functional, and non-functional requirements. These, together, are the requirements that should be satisfied by the designed system for the system to be qualified as fully functioning.

The RDS department at Lunar Zebro is relatively new. It only consists of a mechanical department, without a control unit. The current RDS's mechanical department has designed a pod that will be attached to the rocket and a mechanism that lowers the rover onto the Lunar surface. The addition of the RDS control system will provide multiple capabilities. The RDS control system will supply power, do checkups on the rover (while in transit), facilitate communication between the lander and the rover, and trigger the deployment. The RDS control system will handle everything regarding deployment up until the latch of the pod opens up and the lowering mechanism lowers the rover onto the lunar surface.

The RDS control system will be formed by 3 subsystems that, when working in unison, ensure the system functions properly. The subsystems are the software system, the Power system, and the actuation and sensing system.

3.1.2. Requirements for the entire system

Functional requirements

1. The system should be able to actuate 4 Non-Explosive Actuators (NEA).
2. An umbilical cord must be used to connect the electronic RDS to the rover.
3. The system should make all unconsumed power available to the rover.
4. The rover must remain fixed to the RDS pod unless it deploys.
5. There should be a thermal control system on the RDS.
6. The system should release the rover by actuating four NEAs.
7. Fail-safe backups should be implemented to prevent single points of failure.
8. The system must relay data from the rover to the lander and vice versa.

Non-functional requirements

1. The system should be able to actuate two types of NEA, the NEA® Model 9040 Miniature Hold Down & Release Mechanism (HDRM) and NEA® Model 1120-05 Pin Puller.

2. The system should be able to operate in an environment with temperatures between -120 and $+120°$C.
3. The system should be able to withstand vibrations experienced during launch, transit, and landing.
4. The RDS control system has a mass budget of 200grams.
5. The RDS control system must be smaller than 20cmx20cmx10cm.
6. The system should be able to operate on a $3W$, $28V$ DC supply rail.
7. The system must achieve 99.9% reliability to release the rover and the pod-latch.

3.1.3. Power System requirements

The Power System has multiple general requirements and specific ones for its subsystems. To design quality subsystems that will function as effectively, efficiently, and reliably as possible, the team also formulated sub-requirements for these subsystems.

3.1.4. Functional requirements

General Power System

The power system:

- must receive power from the lander.
- must convert the voltage from the lander to satisfy the specifications of the sub-components.
- is responsible for supplying actuation power to the NEAs.
- must deliver power for rover battery charging.
- is responsible for powering the MCU (Microcontroller Unit).
- is responsible for powering the transceivers attached to the MCU.

Rover Charging Requirements

- The rover must be charged at $12V$.
- The $12V$ bus should always be available for charging, except for when the capacitor bank (5.2) is being charged.

NEA Requirements

- NEAs should be fired when the rover has landed, regardless of the state of the power system.
- The power system must deliver enough current in a short amount of time to the NEAs. This depends on the selected NEA and will be specified in Section 4.2.

MCU and Transceivers requirements

- The Power System must always deliver the necessary power to the MCU.
- The Power System must always deliver the necessary power to the transceivers.

Umbilical Cords Requirements

- The RDS-to-rover umbilical cord should detach from the rover before powering and actuating the NEAs.
- The data transfer rate of the RDS-to-rover and the lander-to-RDS umbilical cords should be at least the same as the maximum data transfer rate of the MCU.
- The RDS-to-rover umbilical cord must be able to transfer the power necessary to charge the rover's battery.
- The lander-to-RDS umbilical cord must be able to transfer the power necessary to deliver power to the subsystems of the RDS.
- The lander-to-RDS umbilical cord must remain fixed at the RDS and lander connection terminals throughout the journey.

3.1.5. Non-functional requirements

General power system

The power system:

- should have fail-safes and breakers.
- should contain as many space-graded components as possible.

Rover Charging Requirements

- The down-converters should have back-ups in case they malfunction.

NEA Requirements

- NEAs are the main priority; thus, the actuation circuit must be as independent and reliable as possible.

MCU and Transceivers requirements

- The MCU must be supplied with $3.3V$ at all times.
- The transceivers must be supplied with their required voltage at all times.

4

System Design

The goal of this project is to design and build a power-supplying system for the RDS. The design of this system will be explained in the following chapters. The team divided the design into two phases to achieve a functioning system that adheres to the requirements stated in section 3.1. The first one is the high-level design, treated in this chapter. The second is the Circuit Design, treated in chapter 5.

4.1. Subsystem Division

To start with the High-Level Design, the team must be aware of the main subsystems that will make up the final Power Flow System. By looking at the requirements, the team devised a subsystem division which will be explained in this section.

4.1.1. Voltage conversion

The requirements in section 3.1 state that although the lander provides power at $28V$, the components of the RDS control system itself require different voltages to function. The MCU and its transceivers require a constant power supply at $3.3V$ and the rover battery must be charged at $12V$. The subsystem that will actuate the NEAs may also require a lower voltage than the voltage level of the lander. To achieve this, the $28V$ needs to be down-converted to the lower voltage levels required by the other subsystems.

4.1.2. NEA actuation

An integral part of this design is the actuation of the NEAs. These components are the ones that keep the rover fixed to the RDS pod. When the lander has landed, the NEAs should be actuated to release the rover in the pod and to release the latch of the pod. Once this latch is released, the rover is lowered to the Lunar surface by a scissor hinge mechanism designed by the RDS mechanical department. This can be seen in figure 1.1. If the NEAs are not actuated, the rover remains fixed and the pod stays closed. This means that the rover does not touch the Lunar surface, ultimately meaning mission failure. The NEA actuation is thus one of the most critical points of the RDS.

4.1.3. Rover Battery

While in transit, the goal of the RDS as a whole is to monitor and regulate the state of the rover and to send this information to the lander.

The subsystems like the rover, sensors, controllers, actuators, et cetera, also use power. The RDS has to supply the rover with power so that it can decide when to draw power for the battery to charge. The on-board rover Battery Management System will decide this. The rover battery and its subsystems are connected through a $12V$ bus and multiple converters, this can be seen in figure 4.1. The PS must supply power to this bus at $12V$.

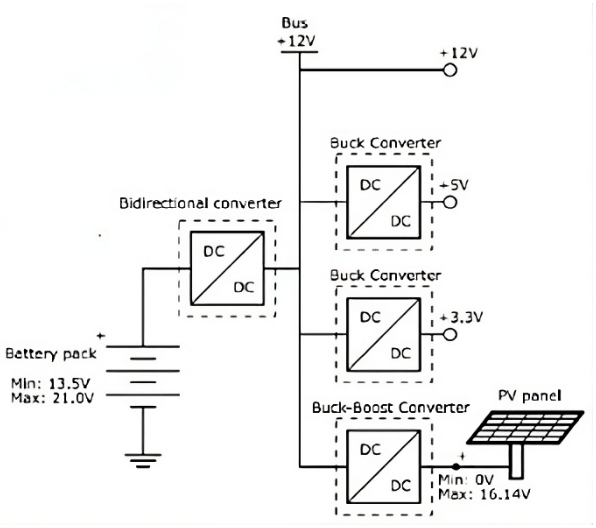

Figure 4.1: Rover Deployment System

4.1.4. MCU and Transceivers

The MCU and its transceivers function as the brain of the system. All digital decisions are made by, and communicated through, these components. Just like in the human body, these need to function at all times. Because of this, the MCU and transceivers must continuously receive power($3.3V$).

4.1.5. Umbilical Cord

Although not a ”real” subsystem, it is important to mention the relevance of the umbilical cords that connect the RDS to the lander as well as the RDS to the rover. These cords will provide bidirectional data and power flow. The only exception to this is that the current flow between the RDS and the lander will only be mono-directional because the lander will supply the RDS with power at all times.

4.2. High-Level Design

The subsystem division and the requirements give the team a clear understanding of what the system should look like. The next step is to create a high-level design for the system which will be treated in this section. This is done to first clearly work out the interactions between the main subsystems and what else is necessary for a fully functioning connected system to be designed. In this stage, the team will represent these subsystems and other extra modules with blocks in a block diagram. This allows the team to easily customize the design without going into too much detail. During this design phase, the team made multiple designs, which would eventually lead to the final design that will be explained in subsection 4.2.1. These earlier designs can be found in Appendix B In each design, the subsystems and their place in the system will be explained so that the reasoning per subsystem, is as clear as possible.

4.2.1. Final Design

After devising the previous designs, the team learned from its mistakes. Using this and the new-found knowledge achieved from research, the team began to work on a final high-level design that would be used for simulation, implementation, and testing. This final design differed quite a bit compared to the previous designs, as can be seen in figure 4.2. Here, the black lines represent the $28V$ bus, the gold lines represent the $12V$ bus, the green lines represent the $3.3V$ bus, the blue lines data and communications, and the red lines represent connections to backup systems. In the next subsections, the modified subsystems will be treated.

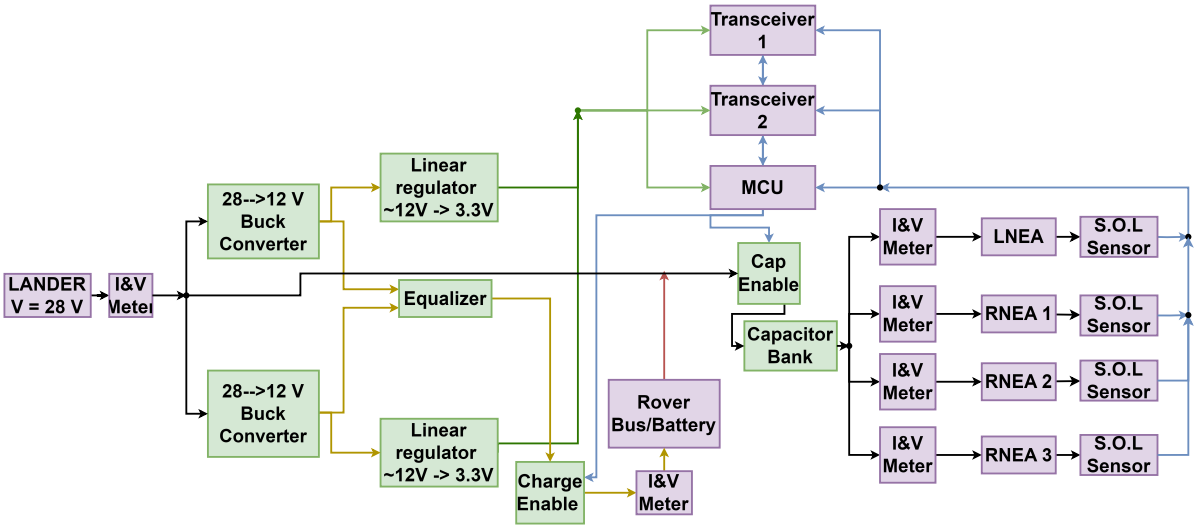

Figure 4.2: Final High-Level Design

Voltage conversion

In the previous designs, a single-buck converter was used for the $12V$ bus. This was the primary conversion method for this branch. As was the case for the LDOs, the system was initially designed to work with a single LDO for primary conversion to the $3.3V$ bus. The backup conversion methods for both branches were LDOs placed in parallel with the buck/LDO. After the second design was finished, the team noticed that only one LDO in our power range was space-graded. This was the TPS7A4501-SP low-dropout regulator [44]. Additionally, this space-grade LDO did not qualify for the intended purpose of the second design. Here, the $28V$ to $3.3V$ conversion was done by an LDO. The space-grade LDO however, does not support such a high input voltage, as can be seen from the datasheet [44]. The maximum input voltage of this component is $20V$. Another design is thus required.

In the final design, the decisions about the $12V$ bus converter drastically changed. A choice had to be made between the SVRCH2812S and the SVSA2812S, which are the $12V$ output models from the previously mentioned converter series from VPTPower in section B.0.2.1.
In the end, a configuration of two SVRCH2812S buck converters in parallel was chosen because of reliability and efficiency considerations. The two individual converters have a maximum output power of $1.5W$. By using two in parallel, the system can still benefit from all the available input power delivered by the lander ($3W$). The choice for this specific design will be further elaborated on in section C.1.

As can be seen from figure 4.2, the output of each buck branches off into two. Every buck has one branch which is connected to an LDO that converts the voltage to $3.3V$. The output of the LDOs of the two branches then reunite to form a singular $3.3V$ bus. This is represented in the graphs by the green lines at the output of the LDOs, reuniting and eventually diverging to the MCU and transceivers. The other output branches of the bucks meet at the equalizer. Even though the two bucks are the same model, components always have a (small) margin. The equalizer is a module that minimizes the differences between the outputs of the two bucks to ensure the eventual $12V$ bus is stable and reliable.

The parallelization of both the buck converters and the LDOs creates a system that does not contain single points of failure. This is achieved without adding backup components that are not used during the primary conversion method. E.g. for the bucks, during normal operation, they work together to provide the necessary power to the $12V$ bus. However, if one buck were to fail, the other buck would still perform the voltage conversion to $12V$, but at half the power. This should only have as a consequence that charging times take twice as long. This concept applies too if one LDO were to fail.
The failure mode of the overall voltage conversion system is if both bucks or both LDOs stop working. Considering the components are space-qualified, the chances of two simultaneous failures are very low.

NEA

In this final design, the number of NEAs used for fixation and release was increased from 3 to 4. The mechanical team conveyed the need for an extra NEA due to new mechanical considerations in their design. This led to figure B.2, which contains an extra NEA along with an I&V meter and S.O.L. sensor on its respective branch.

Capacitor Bank

The new capacitor bank consists of three super-capacitors that will all be charged and discharged to provide power to the NEAs. These capacitors will also be charged directly by the $28V$ bus supplied by the lander. The reason for this is that a higher charge voltage means that the capacitance decreases to store the same amount of energy. Using equation B.1, it is clear to see that for an increase from 12 to $28V$. The stored energy increases by a factor of 5.4 ($\frac{28^2}{12^2}$). To store the same amount of energy as before, this means that the capacitance can, in theory, be decreased by a factor of 5.4. Having smaller capacitors decreases the overall weight of the system and the occupied PCB real estate. This also removes the dependency on the $12V$ buck converter and isolates the capacitors from the rest of the circuit. This will be elaborated upon further in section 5.2. Just like in the voltage conversion system, each capacitor functions as a backup. Each capacitor on its own is capable of discharging enough energy in a short enough time to fire the NEAs. Because of this, the failure of one or two capacitors does not lead to the failure of the entire system.

5

Circuit Design

This section covers the second phase of the design. It differs from section 4.2 however. As the final design will be of main interest, a more in-depth reasoning will be discussed for the made choices. All components and their placement will be discussed. By doing this, the section essentially explains the conversion from the system architecture to the circuit design, formed by all individual components.

The circuit design consists of two sections. Firstly, the voltage conversion will be explained. In this subsection, the choice for and the functioning of the parallel buck converters will be explained. The equalizer will also be treated, the sub-circuit that makes parallelization of the two bucks possible. Furthermore, the LDOs will be elaborated on, and lastly, the connection between these sub-circuits to form one voltage conversion system will be explained.

5.1. Voltage conversion

As mentioned in the requirements 3.1 and in chapter 4, the power system should be able to provide power on a $12V$ and a $3V$ bus. The relevant part of this voltage conversion can be seen by zooming in on figure 4.2. The following subsystem, which can be seen in 5.1, is achieved.

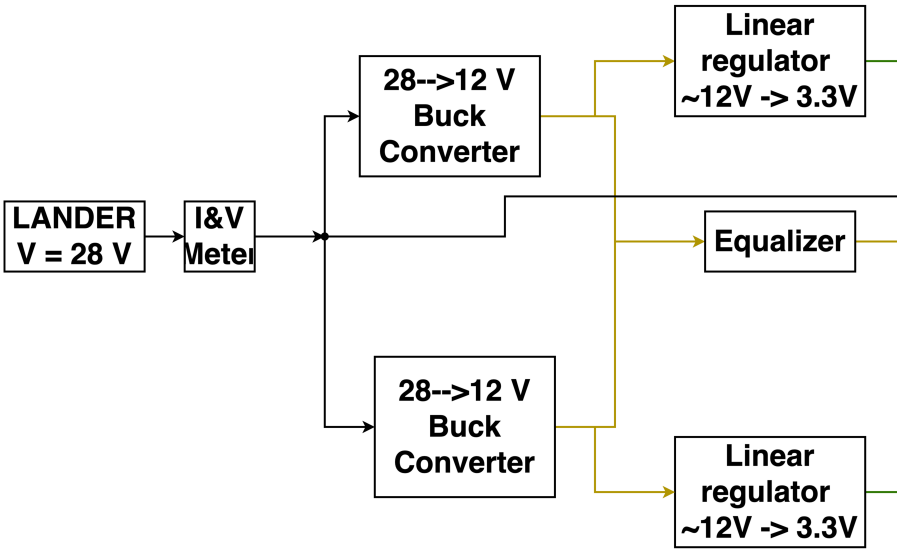

Figure 5.1: High-level design: voltage conversion

The buck converters will be treated first in this chapter. Afterwards, the LDOs and the equalizer will be discussed.

Before being able to show and explain the circuit, an important point has to be addressed.
In compliance with requirement 3.1.5.1, the most important components (bucks and LDOs, as they form the base of the voltage conversion subcircuit) used in the main design were chosen to be space-graded. The rest of the circuit, like resistors and small capacitors, are fairly easy to find space-graded versions for. Even though the requirement of being space-graded is important, it poses some big issues in terms of feasibility, especially in the scope of a Bachelor Graduation Project.
Of-the-shelf, space-graded components are often very specialized products. Therefore, they are not easy to acquire and very expensive. Due to this replacement bucks were searched, to replace the previously mentioned VPTPower bucks. An alternative for the LDOs was also found. The justification for these exact models can be found in the respective subsections 5.1.1.1 and 5.1.1.2.

Also, because of the cost and delivery times of space-graded components, they should not be used for testing purposes. The prototype of the complete circuit, with the other sub-groups, will also be made with these alternative components.
It must thus be understood that the circuits seen in this report are the ones used for testing and prototyping. Although the group's focus is still to use the space-graded versions, it will later be mentioned that the test circuit might also be eligible for the design that will be used for the mission.

A cost overview of the VPTPower, Space-graded buck converter can be found in appendix C.2.

5.1.1. Circuit analysis

In this subsection, the voltage conversion circuit will be analysed. An overview of the circuit, built in Kicad, can be seen in figure 5.2.

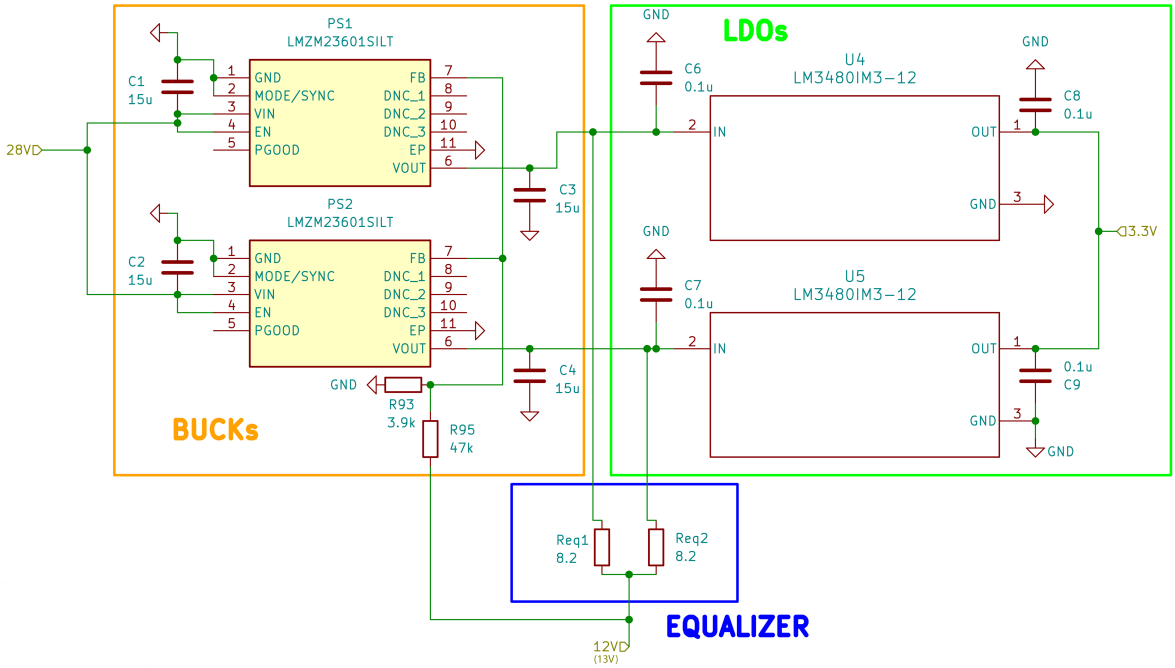

Figure 5.2: Voltage conversion circuit overview

For easier analysis, the circuit is subdivided, and marked with different colors into three different parts. On the left side, in orange, the buck converters with their necessary components, can be seen. On the right side, in green, the LDOs can be seen, and at the bottom, in blue, the so-called equalizer.

Buck converters

The discussion regarding parallel-buck configuration choice has been explained in appendix C.1. Also, the fact that alternative bucks and LDOs would be used for testing, simulation and thus the report was mentioned previously in section 5.1.
The alternative bucks chosen for the circuit were the LMZM23601. The reasons for this choice are quite simple. The converter needed to be able to handle the $28V$ input voltage and the $12V$ output voltage. Furthermore, the converter needed to be cheap and have a reasonably small output voltage ripple. In comparison to the SVRCH2812S buck, the LMZM23601 has a higher maximum output current of $1A$ and is thus capable of delivering $12W$ of output power. This will bring some changes to the testing and simulation procedures, which will be discussed further in the respective chapters 6 and 7 .
Note: please refer to [51] for a basic understanding of buck converters, if required.

Feedback network

Another difference between the SVRCH2812S and the LMZM23601 converters is the need for a feedback network. The latter one has an adjustable output and thus needs a certain feedback network to set its output voltage. This feedback network consists of a very simple voltage division between the output of the converter and ground. Note that in our circuit, the connection is not placed after the buck converter, but after the equalizer, which will be explained shortly. This is to ensure a $12V$ output on the bus after the equalizer.
The voltage over the ground resistor is fed back to the feedback pin of the buck, such that it has a reference to adjust its output. The values of these resistors are $47k$ and $3.9k$. However, the $3.9k$ should be a $4.2k$ resistor in order for the output to be at $12.1V$, but because of the unavailability (temporarily out of stock) of these resistors, the closest value to it was chosen. The consequence of this is that the output value will not be at $12V$, but at $13V$. This is an annoying, but inevitable inconvenience at this time.
The exact calculation of these values can be found in the appendix C.3.3.1.
It should be again noted that this design is made with the vision of it being used for testing. The circuit discussed in this section is the circuit that will be used in the test phase. This is to avoid differences between the theory and testing.
This thus brings the difficulty with it that not any resistance, capacitance, or other values of components, are always available. Common values have to be chosen for the circuit and they have to be in stock on time.

Input capacitors

When looking further in the buck part, we notice that there is an input capacitor placed in front of the bucks, between the V_{in} (Voltage in) and the GND (Ground) pins. This capacitor makes sure to provide small current changes to the buck converter. These input capacitors are very often found together with switching power supplies (buck in this case). The current inside of the buck undergoes very fast changes because of the rapid switching of the internal transistors. A high-quality capacitor is needed for high-end applications, in order to handle these rapid current changes.
Another reason for the placement of an input capacitor is to remove possible input voltage ripple.

In the LMZM23601 datasheet [41], a $10\mu F$ ceramic capacitor with a $50V$ rating is recommended for our design. Eventually, a $15\mu F$ one was chosen, as this is also chosen for the output capacitor, as discussed in the next subsection. This is for the simplicity of the design. The capacitor being slightly bigger does not influence the working of the circuit.

Output capacitors
The output capacitor serves several purposes. First of all, it is used to eliminate voltage ripple at the output. There is always a (small) voltage ripple present at the output voltage. This ripple fluctuates at the switching frequency of the buck converter. To attenuate this ripple, an output capacitor is placed.

A second reason that an output capacitor serves is to respond to load transients. If the load suddenly changes, it can be that the current demand drastically in -or decreases. The capacitor will then assist in providing or absorbing this load current.

A final reason is that it influences the internal control loop of the converter. The buck converter works with a feedback network that is influenced by many factors, not only the two external feedback resistors. The exact control loop functioning is very device-specific and thus the required output capacitance (range) is usually specified in the converter datasheet.

Furthermore, it should be noted that the output capacitor cannot be chosen too large, as this may cause a large current draw from the buck converter during the transient. This may cause the built-in current limiter to activate or might even damage the device over time. It is thus best to follow the manufacturer's guidelines when choosing the capacitance.
In the datasheet [41], a $15\mu F$ output capacitor is recommended for our output voltage, so this is the value chosen.

LDOs
The next part in figure 5.2 is the green part of the LDOs. We can see the two LM3480 linear regulators, with their respective input and output capacitances.
This model was chosen as it is an inexpensive regulator and its power throughput is designed for our range.
Note that the fixed 3.3V-output model was chosen. The name of this specific sub-model is LM3480IM3-3.3. On the schematic, the model LM3480IM3-12 can be seen, which corresponds to the 12V-output model. This is because the models share the same footprint for PCB design, but the LM3480IM3-3.3 model will effectively be used for the circuit.
The LDOs are each placed directly on the output of the buck converters. It is not so that the LDOs are placed on the $12V$ bus, which is only created at the output of the equalizer. Configuring the circuit in this way is more reliable. Although the bucks are placed in parallel, with one being able to take over the other one in case of failure, it is safer to connect each LDO directly to the output of a buck. In this way it is almost always assured that the $3.3V$ bus can be created correctly from one of the buck outputs, by an LDO.

The LDOs are directly connected together to form the $3.3V$ bus. This can be done without functional problems for the LDOs themselves. They are very robust devices that work quite independently of what is connected to their output (unless they draw too much current). This is again thanks to the simple internal circuitry that works with the open or closing PMOS transistor. The drawback of this circuit, compared to a buck converter, is that it works much more inefficient as a large amount of power is dissipated in the transistor. However, as the MCU and transceivers only draw very small power, this inefficiency is not of significant importance.

Input and output capacitors
The necessity for in -and output capacitors connected to the LDOs, has mostly the same reasons as for the buck converters. They are there to assist with load transient and input voltage ripple that is projected to the output of the LDO. Contrary to the buck converter, they do not serve to provide current to the LDO for rapidly changing currents. This is simply the case because an LDO is not a switching regulator. It does not involve rapid on/off transistor switching. Instead, a PMOS transistor is used that closes or opens more, depending on its internal feedback network, so that a stable output voltage is

maintained.

In the datasheet of the LM3480 [40] it is stated that both the in -and output capacitors have to be of at least $0.1\mu F$. Larger values of the output capacitor can help with the transient conditions, but should also not be chosen too large, for the same reason as for the bucks, namely a too-large current draw during transient.

Equalizer

The final part of the voltage conversion circuit is the equalizer. This name is given by ourselves. The equalizer is there in order to unite the two outputs of the buck converters into one, $12V$ bus.

Having a circuit for this is necessary as the buck converters will have small differences in their output voltages. They will never be completely identical.
Imagine a scenario where one buck delivers an output at exactly $12.0V$ and the second buck at $11.9V$. What might happen in this scenario is that the first buck always tries to keep the voltage at $12V$ and thus tries to deliver the necessary power to the load. The second buck, however, whose voltage is slightly smaller, might get the impression that it is not driving anything and will shut off. Because of this, the voltage might drop as the first buck is not able to deliver the necessary power on its own. This will be the case if $3W$ is 'asked' by the load with the two $1.5W$ buck converters. The voltage will thus drop slightly until the second buck starts to drive the load again in order to get the voltage up again. This story will repeat itself constantly and a lot of flickering might occur.
In terms of power delivery, this will probably not form a big problem. However, the current limit of the first buck might be triggered often, which may cause damage over time as the system is not designed to operate in this range. This flickering and current-limiter triggering must be tested. Details concerning testing will be explained in chapter 7.
It can be concluded that a system is thus needed to bring these outputs together in a more efficient manner without having this flickering behaviour.

Voltage droop

The method seen in figure 5.2 of uniting the outputs, is called voltage droop. This is a very simple implementation in which two resistors are connected, each with one side connected to the output of a buck, and the other side connected to the same end of the other resistor. This latter connection forms the $12V$ bus.

The result is that every buck has a so-called 'droop' resistor in series with its output. The droop voltage (over the droop resistor) increases proportionally with the output current.
In parallel operation, with a common load, the buck converter with a higher current output will have a larger voltage droop. This converter will thus have a slightly lower bus voltage (voltage after the droop resistor). This induced a current shift to the other converter to increase its current.

To choose the values of the voltage droop resistances, a consideration has to be made between reducing the current imbalance and the maximum power throughput. The higher the values of the resistors, the bigger the voltage droop due to a current imbalance. The other buck actually senses a bigger difference in voltage and will compensate faster/harder in order to counteract the imbalance. On the other side, the bigger the droop resistance, the less power can be delivered to the load, as more power will be dissipated in the droop resistor, according to the formula $P = I^2 \cdot R$.

The chosen droop resistors are 8.2Ω. This means that at almost full load, the scenario where the rover is charging, the average power dissipation for both resistors would be $45.9mW$. This is 4.5% output power of the bucks. This is quite a small percentage, as the efficiency / maximum throughput was given priority over current balancing.
The complete calculations can be found in appendix C.3.3.2.

In order to measure the specific imbalances, testing should be done. More details on this will be explained in chapter 7.

Other current sharing methods
Voltage droop is only one of many ways to implement parallel bucks. It is a passive and easy method, but on the other hand not energy inefficient nor optimal in terms of current balancing. Because of simplicity and heavy time constraints, this method was used for the design.

Active current control is another implementation method. It gives better results, but with increased complexity. There are different implementations for active control like average current control, directed master-slave and automatic master-slave.
The first one, average current control, compares the output current of the buck to the total current of the two and adjusts in this manner. This design would be difficult to implement in our design as the output of the bucks immediately branches of into the two LDOs and the equalizer. Measuring the total current is thus not easy. Furthermore, in case of a current limit triggering, the output voltage of the whole system would drop to $0V$.

In the direct master-slave method, one of the bucks is pre-defined as the master and will try to deliver the necessary current at the chosen output voltage. The second buck, the slave, takes the output current of the master as a reference and uses this as a reference. The buck will increase its output voltage and will implement current balancing in this fashion. The disadvantage of this method is that the whole system is dependent on the master buck and the system thus cannot operate if the primary buck fails. The reliability of this method has thus not increased, compared to a single buck converter.

The final implementation is the automatic master-slave. It involves an external controller and circuitry that will let the individual bucks know how to adjust their output voltage in order to achieve optimal current balancing. It is very similar to the direct master-slave method, except that the external controller can 'replace' the master converter. In case it fails, the slave will be made the master and the system will stay functional.
Because of time and complexity, this implementation was far out of the scope of this project and was thus left aside.

Supplementary design
A few additional notes should be made about the voltage conversion design.
The first is the fact that the capacitors on the lines between the output of the buck converters and the input of the LDOs, have not been combined into one. This is to avoid oscillations in the circuit. The traces in the PCB have a certain capacitance, inductance, and resistance. Together with other reactive components, these characteristics can form in-circuit resonance, which may cause relatively large oscillations. These oscillations should be avoided as they may cause instability or even damage to the components or the overall system.
By placing the capacitors as close as possible to the pins, the parasitic characteristics of the traces are minimised, and the possible oscillations consequentially too. By not combining these capacitors into one, possibly bigger, capacitor, they can each be placed closer to the components' pins.

A second point is that the buck converters chosen in this circuit, the LMZM23601's, have another important pin, the MODE/SYNC one. It can be used in various ways. When pulled high, it forces the buck to be in PWM mode. This mode is best used for increased efficiency for medium to high loads.
If the pin is pulled low, the buck converter can also go into PFM mode, which works more efficiently for lighter loads.
The exact functioning of these modes will not be explained as it falls out of the scope of this report. A brief comparison between the modes can be found in the datasheet of the buck converter [41].
A last remark about this pin is the ability to synchronise the two buck converters to an external clock.

This also gives the ability to synchronise them $180°$ out-of-phase. This may bring decreased output voltage -and current ripple and improved efficiency.
This method was not applied for the circuit as the space-graded bucks do not offer this ability of synchronisation and they are still, for now, the main bucks chosen for the final design. Also, this would increase the complexity of the design, which is not desired due to time constraints.

5.2. Capacitor Bank

The capacitor bank is the second part of the circuit design. It is responsible for delivering the necessary power for NEA actuation. Whilst both sections, the voltage conversion and the capacitor bank, are both part of the same power system, they are very different in terms of behaviour. The voltage conversion, described in the previous section 5.1, has the goal of being a reliable, source of energy for the rover, MCU, and transceivers. The steady-state functioning of this system is more important than its transient. For the capacitor bank part, this is exactly the contrary. It must form a source for the NEAs', but a very powerful one in a short amount of time. The focus for the capacitor bank thus lies on the transient, rather than steady-state.
Furthermore, as mentioned in section 4.1.2, the importance of proper NEA actuation is very high. The system must thus be designed as reliable as possible.

5.2.1. Preliminary design

As stated in requirement 1, the capacitor bank should be able to actuate two types of NEA, the NEA® Model 9040 Miniature Hold Down & Release Mechanism (HDRM) and NEA® Model 1120-05 Pin Puller. They will, for simplicity, be addressed by HDRM and Pin Puller in this report. Looking at their respective datasheets [28] [27], they both have a necessary actuation current together with a corresponding time interval. These are specified as $3A$ for $50ms$ for the HDRM and $4A$ for $25ms$ for the Pin Puller. As said in the final design section 4.2.1, no definitive choice was yet made by the mechanical team between the two models. Therefore, the system should be able to drive both NEAs, without much adjustment. The degree of freedom in designing this circuit lies in the fact that the given requirements in the datasheet are minimum requirements. Designing for higher values, e.g. more current for a longer time, will thus form no problem (up to a certain point). This is due to the fact that the NEAs are triggered utilizing an electrical fuse wire. Sufficient current should be run through it for it to melt and snap, after which the NEA is actuated. Too much current is thus no problem and neither is an extended time as the circuit will open and thus not permit any current to run through it anymore.
Because of this freedom in over-designing, the requirements of both NEAs were combined and resulted in specifications of $4A$ for $50ms$.

5.2.2. Circuit analysis

In this subsection, the capacitor bank circuit will be analysed. Again, an overview will be given first, which can be seen in figure 5.3. However, this circuit is a part of the complete capacitor bank. This is done as this subcircuit is repeated thrice and connected together to form the complete capacitor bank. The complete capacitor bank can be seen in appendix C.1. It should be kept in mind that the circuit in this subsection is repeated thrice and connected together in order to form the complete capacitor bank.

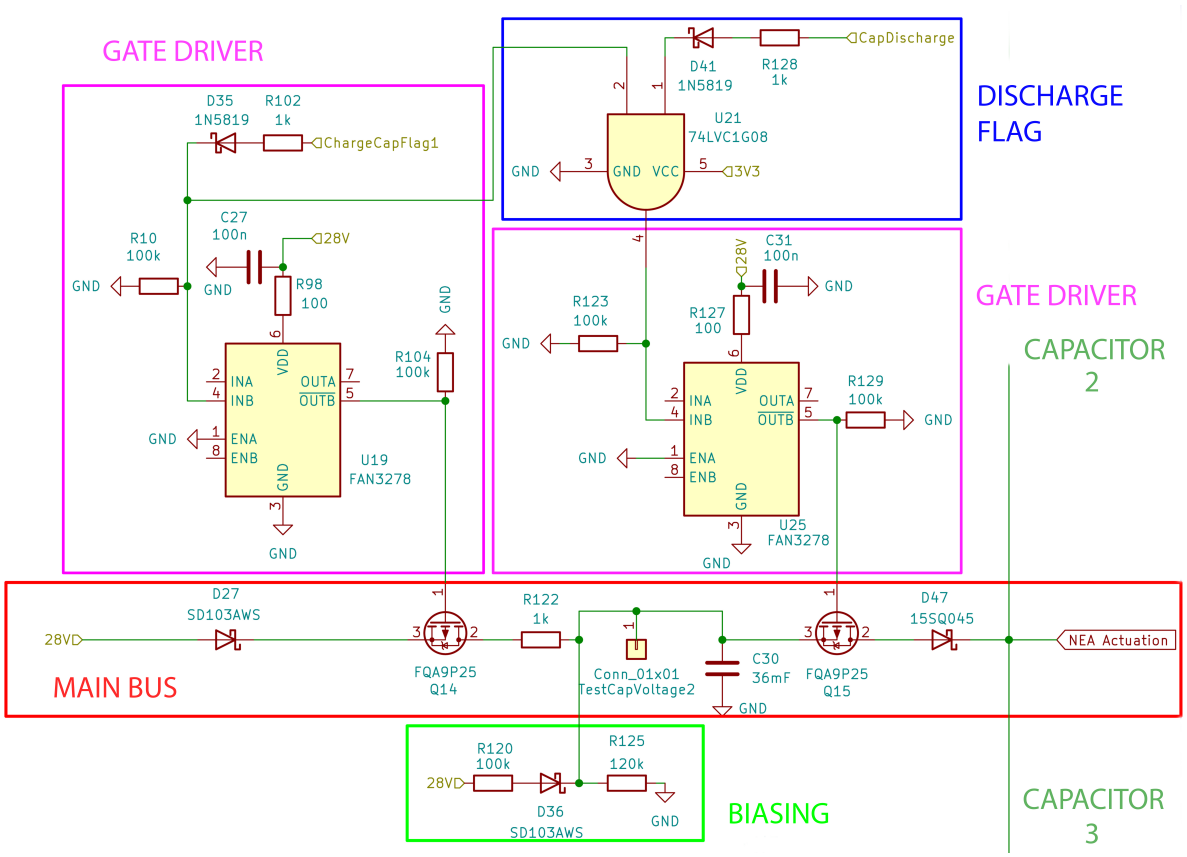

Figure 5.3: One of the three capacitor subcircuits in the capacitor bank

Four different parts can be seen in the subcircuit, each in a different colour. We thus subdivide this analysis into different parts, named Gate driver, Discharge flag, Main bus, and Biasing.
Furthermore, two connections can be noted. These are named 'Capacitor 2' and 'Capacitor 3' in the figure. These refer to the identical subcircuits, just like this one, which are put in parallel. These can be seen in appendix C.1 too.

Main Bus

The first explanation will be about the main bus, as this is where all the parts come together. This part is marked in red.
The structure of the subsection will be repeated for the other parts too.

Input bus

Starting at the left, we see the $28V$ bus, which comes straight from the lander. This is the bus that will be used for charging the capacitors. The two reasons for placement on this bus were already given in section 4.2.1.3. The first reason was already explained in this section too. The second one, isolation from the rest of the circuit, should be elaborated on. As this part of the overall system will have large transients going through it, it is better to isolate it as much as possible from the rest of the circuit.

This is for safety reasons in order to avoid damage to other components. Sudden changes in current or voltage, in combination with reactive components may cause very large current -or voltage spikes. This is especially due to the presence of a large capacitance and inductance (inside of the NEA). It is thus better to connect the circuit on the 28V-bus instead of the 12V-one in order to put it, electrically, as far as possible from the MCU. This is because the MCU should be operational at all times and it is, in comparison to other components, relatively sensitive to voltage changes.
Furthermore, the routing/placement of a subcircuit with high current throughput should be handled with care as the current induces an electromagnetic field that can become very strong, depending on the current amplitude. This EM field may cause damage to other components, but will not be further discussed in this report as it is part of the sensing and actuation group.

Component functions
In this section, the function of the different components will be explained. In order to avoid repetition, it should be realised that a specific model for a component has been used as it is able to handle the evident requirements, needed for the exact placement. E.g. a certain component needs to be able to handle a maximum voltage of $28V$, than a component will be chosen with this rating minimally and not a component with a lower rated voltage. This applies for evident choices. This subsection focuses on the main reasons for choosing a specific component in order to keep the explanation as brief as possible. If exact values are desired, we kindly refer to the components' datasheets.

From left to right, we first see diode D27 (model: SD103AWS [68]). This is a Schottky diode, see appendix C.3.1 for the complete reasoning to use these types of diodes in our circuit. Here, it is mainly used because of its low forward voltage. This makes the circuit more efficient during charging and makes sure the supercapacitor has a maximum charge voltage as close as possible to $28V$ as possible.
The diode serves the purpose of separating the capacitor bank from the rest of the circuit. This is achieved as the diode blocks current from flowing out of the capacitor to the rest of the circuit. Why this isolation is important has been discussed in subsection 5.2.2.1.

Second, in the summation, PMOS Q14 can be seen (model: FQA9P25 [67]). This transistor makes sure it is possible to control the capacitor charging. If the ChargeCapFlag1 signal, coming from the MCU, is set high, the transistor starts to conduct. The capacitor is now able to draw current from the $28V$ bus and will start to charge.
This model was picked out especially because of its high maximum drain-source breakdown voltage. In case of power failure, and the capacitor being charged, it should be able to withstand the voltage difference. This voltage should normally never exceed $28V$, but a margin was taken.
The reason behind choosing a PMOS here is elaborated on in appendix C.3.2.

Moving on, resistor R122 can be seen between the capacitor and the PMOS. It plays the role of a current limiter. According to $i = C\frac{dv}{dt}$, the current in -or out of a capacitor can become extremely high due to sudden voltage changes. When the PMOS starts to conduct (start of charging), $\frac{dv}{dt}$ becomes very high as the on-resistance of the PMOS is relatively low. This would induce a very large current draw to the capacitor, which might damage the transistor, but more importantly, take up all the power from the circuit in order to charge the capacitor. This could possibly cause the MCU not to have enough power to stay operational.
Choosing a resistor as a current limiter is not the most power-efficient way, but it is a very simple and robust way of limiting the current. Simplicity and reliability were chosen over efficiency here.
The exact value of the resistor is elaborated on in appendix C.3.3.3.

A test-pad named 'TestCapVoltage2' can also be seen in figure 5.3. This is to be able to measure the voltage across the capacitor for test purposes.

Moving on, we come to the heart of the capacitor bank, the supercapacitor. Its function has been discussed various times already. As can be seen, it has a capacitance of $36mF$. An extensive reasoning and derivation of this capacitance can be found in appendix C.3.4.

Looking further to the right, we come to another PMOS of the same model as before. The transistor has multiple purposes. First of all, the logic behind it should be understood, which is explained in subsection 5.2.2.2.
The essence of this logic is that the the PMOS conducts when the ChargeCapFlag1 signal is high and the CapDischarge signal is too. Both are control signals coming from the MCU.
When the transistor conducts, the NEA actuation system actually gets armed. Only the NMOS seen in section 6.2 of the Sensing and Actuation report [49] has to be turned on and the NEA will actuate.
Each of these three 'discharge/arming' transistors in the capacitor bank can be controlled individually. This is done to simplify the voltage measurement of the individual capacitors. The outputs of the three identical circuits come together on the NEA Actuation bus, as seen in 5.3. On this bus, the voltage can be measured. This is described in section 6.1.3 of the Sensing and Actuation report [49].
By turning on these individual transistors, one at a team, the voltage over a specific supercapacitor can be measured.
A last point to be discussed is the reasoning behind the logic of the PMOS. It will only turn on when the ChargeCapFlag1 and the CapDischarge signals are high. This is because the circuit behind the PMOS consumes a minimal amount of $85mW$. This is due to the Sensing and Actuation circuitry.
This would mean that, if one capacitor is fully charged to $28V$ (slightly lower because of the Schottky diode), and connected to the NEA actuation bus, it would be empty after $2:46min$. This is an easy calculation with equation B.1.
Therefore, the PMOS can only be closed to 'arm' the NEAs while it is connected to the $28V$ bus to compensate for these losses. Otherwise, it could for example occur that the capacitors are almost discharged after their integrity is checked by checking their voltages.

As the final component of the main bus, we have another Schottky diode. It is there to avoid current flow between supercapacitors when the circuit in 5.3 is parallelized with itself, as can be seen in figure C.1 in the appendix. The connection points of where these 'duplicates' are connected are shown as 'Capacitor 2' and 'Capacitor 3' in figure 5.3.

Discharge flag

This part of the subdivided capacitor bank is marked in blue and has one essential component, an AND gate. It is marked as component U21 in the circuit, the specific model is 74LVC1G08 [38].
Only if the two signals, ChargeCapFlag1 and CapDischarge, from the MCU are both high, it will output a $3.3V$ (high) signal. This signal will go to the gate driver, explained in the next section 5.2.2.3.
The Diode D41 (model 1N5819, [72] and the resistor are there in order to protect the MCU. Current can never enter the MCU because of the diode and high currents can not be drawn from the MCU due to the resistor. The diode thus also makes sure a pin of the MCU can never be pulled high because of external circuitry.

Gate Driver

This part is marked in pink in figure 5.3.
Gate drivers are used in the circuit for controlling the PMOS'. Why gate drivers are used specifically is very well-explained in section 6.1.6 of the Sensing and Actuation report [49] and will not be repeated here.
One additional benefit of using gate drivers is that they reduce the transition time between cutoff and saturation (conduction) mode. This makes the transition more power-efficient. However, as switching occurs very sporadic, this is not of importance for our circuit.
This specific model, the FAN3278 [66], was one of few models able to drive gates at $28V$. This was necessary as only reliance on the 28V-bus was desired and this would thus be the bus driving the gates (not directly). Furthermore, the FAN3278 had the best characteristics in terms of maximum output current.

This determines the transition speed between the previously mentioned cutoff and saturation mode.

The same reasoning as given in subsection 5.2.2.2 is valid for the diode and resistor connecting the MCU signal to the circuit (D35 and R102).
Furthermore, there are $100k$ resistors connected between GND and the in -and output pins. This is done to ensure that, if no high-signal is applied, the signal is correctly pulled to $0V$. $100k\Omega$ was chosen as the FAN3278 gate driver uses the same resistance value to pull down certain pins internally. These resistors might be redundant, but are placed to be sure.

Ultimately, there is a resistor placed before the VDD-pin and a capacitor on the 28V-bus. The resistor is to avoid high current draw by the gate driver in case of malfunctioning or when trying to attenuate oscillations, again see section 6.1.6 of [49] for an explanation on Gate Ringing.
The capacitor is placed here to attenuate voltage fluctuations due to the behaviour of the gate driver. This is done to ensure a reliable $28V$ bus.

Biasing

The final part to be discussed, in green, is the biasing circuit. This biasing is needed due to the fact that electrolytic capacitors have a unique characteristic of self-healing.
The dielectric inside of an electrolytic capacitor can show small, localized breakdown. They are little cracks in the dielectric material in essence. Because of these small cracks, it is possible for a small leakage current to flow between the plates of the capacitors. However, this small leakage current actually repairs the dielectric material slowly and the crack is 'repaired'. This phenomenon is called 'self-healing'. A detailed explanation of self-healing can be found in [13].

As the supercapacitors are electrolytic, and insulated by tantalum, they also have this self-healing property. For a leakage current to be able to run and repair possible irregularities in the dielectric, the capacitors should always have a certain voltage applied to them.
This is similar to the biasing of components in electronics. The term might not be entirely correct, but the idea is very similar.

The capacitor should thus always be 'biased', this is where the voltage division comes into play. An optimal biasing voltage is between 60% and 80% of its maximum rated voltage.
The capacitor is rated for $35V$ and should optimally be biased between $21V$ and $28V$. $21V$ may be preferred because of safety reasons and power efficiency.
With the voltage division in the green biasing part and taking the forward voltage of the diode into account, a biasing voltage of around $14.7V$ is set. This is 0.42% of the maximum rated voltage. This is due to a miscommunication between the Power -and the Sensing and actuation groups.
Better values would be $30k$, replacing the $100k$, and $100k$, replacing the $120k$. Then, the capacitor would be biased at around $21V$.
The diode is placed for the same reason as diode D27, in order to protect current from flowing into the $28V$ bus. Also, the resistor values are chosen quite high such that self-healing can take place in a controlled manner, and in case of capacitor failure, usually a short, there will be no large current running to ground.
It is recommended to test this biasing in the test phase in order to check whether the capacitor actually achieves the $21V$, or that the biasing power should be increased by decreasing the resistor value(s).

5.2.3. Alternative storage

Although the name 'Capacitor Bank' suggests that it consists of capacitors, which in the final design is true, other energy-storing methods were considered. The main alternative that was considered was the use of Lithium-ion battery cells.
Lithium-ion batteries are widely used for energy storage and delivery. Although this sounds very similar to capacitors, there is a big difference between them in terms of power -and energy density.

These parameters show how much power or energy a source can deliver per unit of volume.
A comparison is made in figure 5.4.
It can be seen that the energy density of a Li-ion battery is much higher than that of a supercapacitor, but its Power density is much lower. This source is thus fitted to deliver much more energy, but at a lower power, for a longer time interval.
A supercapacitor, is just the contrary. It cannot hold that much energy, but has a very high Power Density. It can thus deliver a large amount of time, but for a short amount of time.

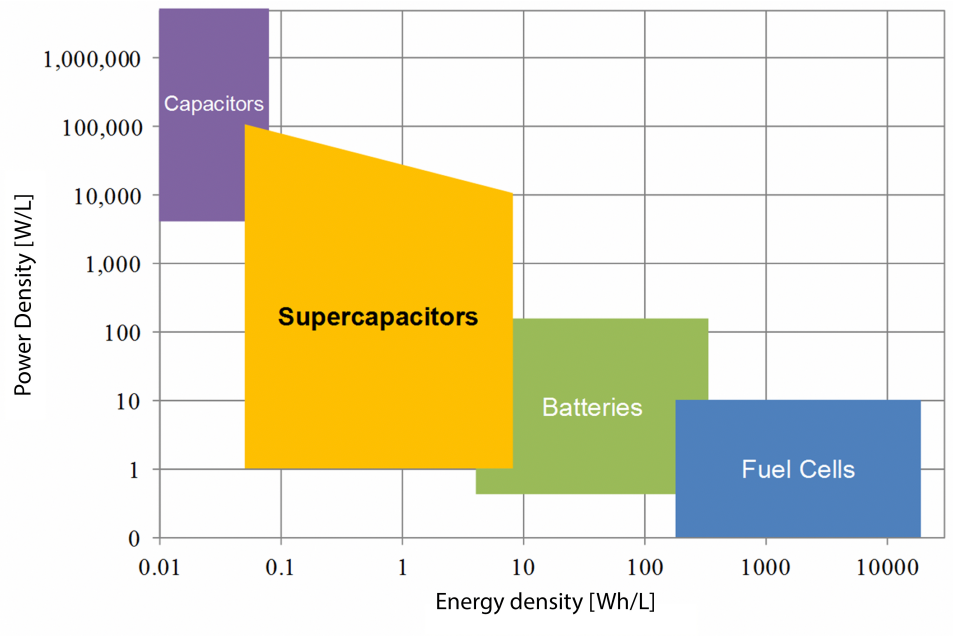

Figure 5.4: Power vs energy density, comparison of different energy storage methods

As discussed in appendix C.3.4, the NEA actuation circuit requires always a minimum voltage of $20V$ for proper NEA actuation.
For our circuit, a combination of high-performance Li-ion 18650 batteries would, in theory, be capable of delivering the necessary power for actuation. However, as the voltage of an individual can heavily vary between $2.7V$ and $4.2V$, it is not as easy as putting in series to achieve the necessary voltage. Some kind of converter, probably a high-performance buck-boost, would be needed. Although these circuits may be able to deliver the necessary output, they will come at a noticeable delay compared to using a power MOSFET with a supercapacitor. This is because the power output of these converters takes a longer time to build up. This again is due to the internal working of these converters, but is out of the scope of this project.
It is desired to give an almost instantaneous power surge upon actuation. Furthermore, these converters are in general not made for large power surges.
The design thus stuck to the use of (super)capacitors.

5.2.4. Umbilical Cord

The umbilical cords, as mentioned in subsection 4.1.5, serve as the bridge between the RDS, lander, and rover. Of the two umbilical cords used in the system, one is dictated by the lander. The other must be chosen according to the power and data transfer specifications between the RDS and the rover.

The first umbilical cord connects the RDS to the lander. The lander that the RDS is attached to is made by Astrobotic. This private company designs and manufactures robotic technology for lunar and planetary exploration. The umbilical cord that the Astrobotic landers use is the ”Glenair SuperNine connector of the MIL-DTL-38999 Series III screw type connector”[4]. The lander offers two types of

connectors, which can be seen in figure 5.5. Based on the required number of pins, the smaller variant is suitable for this system, as only 4 pins are needed.

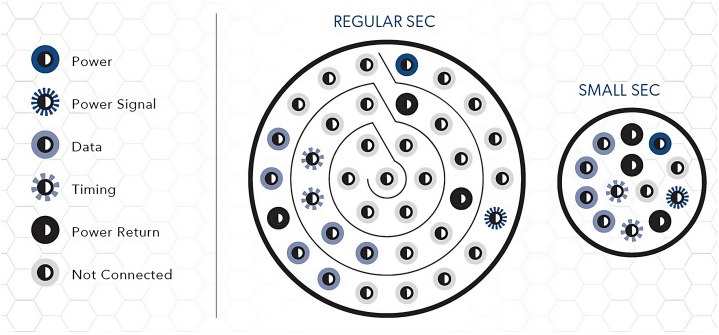

Figure 5.5: Connector types offered by Astrobotic landers

To retain consistency in component selection, the umbilical cord between the RDS and rover is the same as the lander cord. The interaction between the RDS and rover only requires 6 pins in total. The ”Small SEC” is sufficient for this pin amount. The umbilical cords contain all the different cables that are connected between the RDS and its attachments. Because of this, in the circuit design, this component was not directly used in the schematics. The use of the umbilical cords in the system will be further elaborated upon in chapter 7.

Final design remarks

It should be noted that rover charging and capacitor bank charging should never happen at the same time. This is to avoid, as there is no instantaneous current measuring but only a maximum current limiter of each subpart, that all power is drawn and that the MCU would end up without. As already stated in the requirements 3.1.4.2, the rover should always have the 12V-bus available, but the group of the power system has no control over when the rover will be charging. This decision is taken by the rover electronics system, but should be coordinated with the ChargeCapFlag1 signal coming from the MCU as this enables capacitor charging.

6

Simulations

This part of the report will be dedicated to performing simulations of the circuit. Simulations for more complicated circuits and with given manufacturer's models can, unfortunately, in general not be used for transient behaviour analysis. This is due to the fact that the simulation models are not capable of describing exact real-life behaviour and would become incredibly complex to simulate. The models thus have to be used with precaution as they might not represent reality.
This is known and expected and thus the simulation models are used with the goal of steady-state analysis.

6.1. Simulation Set-up

For simulation, due to heavy time constraints, only a model was made for the voltage conversion part of the power system. The simulation model is almost identical to the circuit seen in 5.2.

One of the differences is that another LDO model was used. This was due to the unforeseen fact that the manufacturer's simulation model of the LM3480 was not functioning correctly. Therefore, the group decided to use its successor, the TPS709. This model behaves almost identically, especially during steady state. The only difference is that the TPS709 is capable of delivering 50% more current (and thus power) to its load and that its output voltage varies slightly less with temperature.
Note that both LDO models were ordered for testing.

Furthermore, the load that plays the role of the rover during charging, is connected. The derivation of its value can be found in C.3.3.2.

Lastly, the 434Ω resistor is added to draw $25mW$ from the 3.3V-bus, close to the $21.76mW$ that the MCU and transceivers draw on average.

As previously mentioned, the goal is mainly to check the behaviour of the system at steady state. This simulation can be useful to check output voltages of bucks and LDOs, voltages -or current ripples but also behaviour when the current limiter is activated.
Transient behaviour is better analysed during testing as that is a lot more reliable representation of real-life behaviour.

An overview of the test-setup in LTSPICE [23] can be seen in figure 6.1.

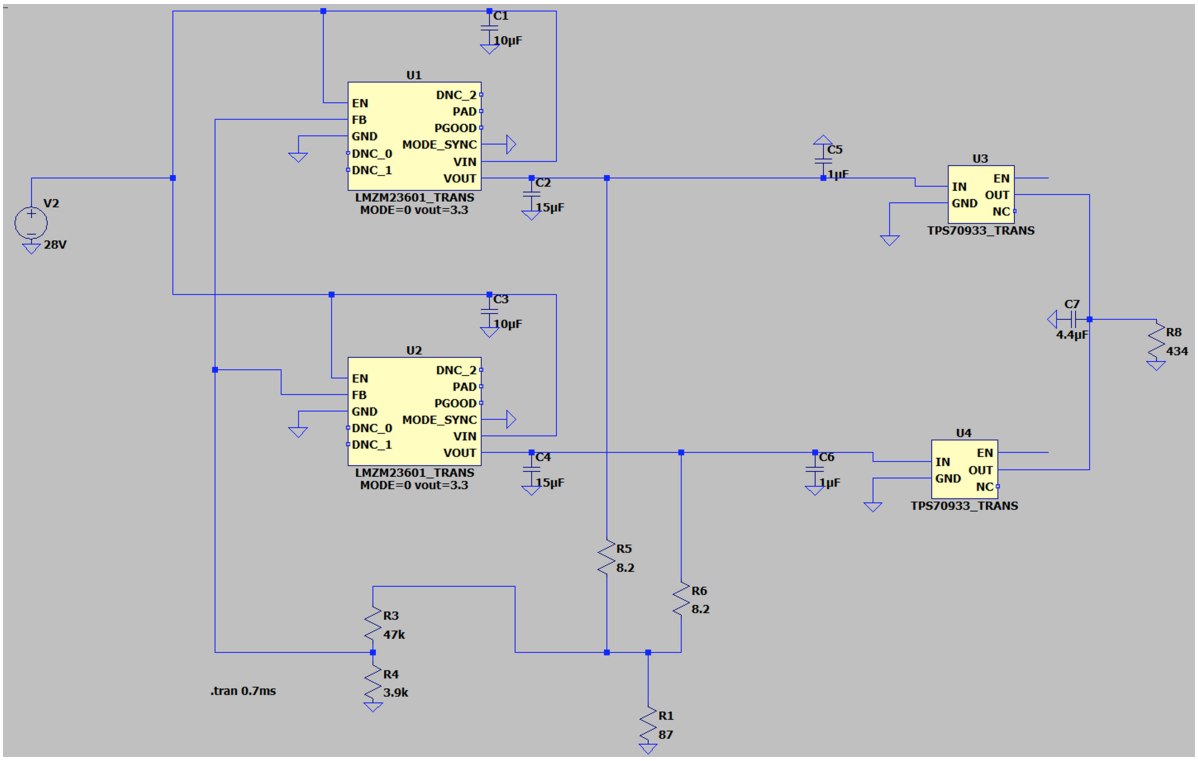

Figure 6.1: Voltage conversion simulation setup

6.2. Manufacturer models

The simulation models for the buck converters and LDOs can be found on the Texas Instruments page [42] and [43], respectively.

Texas Instruments says to have included the following behaviour in their buck converter model:

1. Peak and valley current limit with hiccup protection.
2. Softstart.
3. FPWM mode and auto mode of operation.
4. SYNC feature.
5. IBB Configuration.

Explicitly not modeled are the quiescent current, operating current and temperature effects.

For the TPS709, the modelled behaviours are:

1. Power-up with enable.
2. Power-up and power-down.
3. Peak current limit.
4. Dropout voltage.
5. PSRR Plot.
6. Reverse current Reponse.

7. Startup, line and load transient response.

Explicitly not modeled are the quiescent current and the GND pin current with respect to the input voltage. Also, temperature effects have been neglected.

6.3. Simulation goals

From this simulation, the main things we want to observe are whether the voltages at the busses are in the range of what is expected.
Furthermore, the current through the voltage droop resistors will be observed.

6.4. Results

The steady-state analysis can be summarized in graphs 6.4. The code for these graphs can be found in A.2

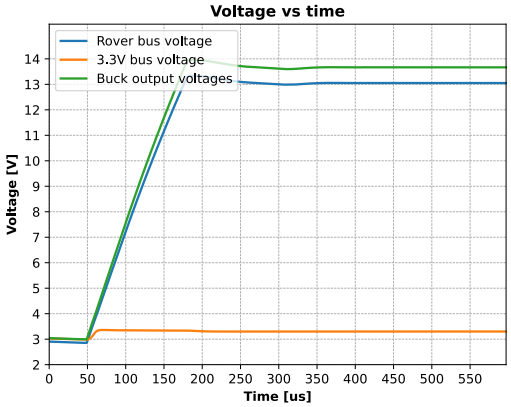

Figure 6.2: SS analysis: Voltage vs time

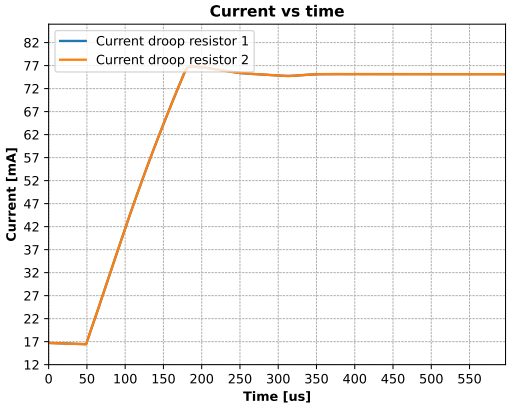

Figure 6.3: SS analysis: Current vs time

Figure 6.4: Steady-state voltage conversion simultation results

From figure 6.2, we can see that the rover bus voltage (voltage over the 87Ω resistor) is at $13.06V$ in steady-state. This is almost the same as the 13.05 theoretical value and is thus as expected.

Furthermore, the buck output voltages are $13.66V$, which is very close to the $13.63V$ calculated in appendix C.3.3.2. These values are very close together, especially considering that the $13.66V$ was the result of a (small) approximation. The output voltages of the bucks are exactly the same at all times in the simulation. In real-life this would not be the case. This shows that the models have shortcomings and that transients, imbalances, or ripples should be investigated with a test setup.

Moving on, it can be seen that the voltage of the 3.3V-bus is at exactly $3.3V$, which means that the LDOs are functioning as expected.

Going to the current simulations in figure 6.3, the current through both droop resistors is again exactly the same at all times. This is again due to the unfitness of the simulation models for other purposes than steady-state analysis.
As can be seen, the currents are $75mA$ in steady-state, which is again as expected from C.3.3.2.
This could also have been expected as the rover bus voltage was correct, as was the output voltage of both buck converters.

The same simulation procedure can be repeated easily for the $4.2k$ resistor or under different load circumstances. This will not be done as real-life testing seems more appropriate, for previously mentioned reasons 6. Voltage -or current ripples will also be analysed during testing. For now, it was desired to know whether the circuit behaves like in theory under steady-state conditions.

7

Implementation and Testing

Simulating the designed circuit was the last step in verifying the validity. The next step is to physically build the system. The goal of this project is to design a fully functioning RDS, meaning that the designs of all the subteams must work in unison. Because of this, the circuit of the ”Sensing and Actuation” team and the power system’s circuit were integrated and routed on a PCB. The design and routing of the PCB is explained in detail in the thesis ”Sensing and Actuation Lunar Zebro Rover Deployment System”[49].

The physical implementation of the umbilical cord proved to be difficult. During the design of the RDS PCB, the search for umbilical cord adapters did not amount to a usable component. A possible adapter to connect the cord to the PCB was not found. Besides this, the lead time for acquiring the umbilical cord was not within the period of the project. Due to this, the umbilical cords were not directly implemented in the circuit of the final design.

Originally, the different Power subsystems were meant to be tested individually, in unison, and together with the other systems of the RDS control system. This would yield a clear understanding of why the system does or does not behave as expected. Unfortunately, because of logistics reasons and time constraints, this could not be completed.
Only effects due to parallelization of buck converters will be investigated in this chapter.

7.1. 12V Bus

Ideally, testing should be done using the components intended to be implemented in the final physical design. As mentioned before, this was not possible due to various reasons. In the case of the buck converter, a larger non-SMD buck converter was tested instead of the LMZM23601. This was used to test the architectural behaviour of the parallel bucks with the voltage droop. The set-up consisted of:

- 2 x LM2596S[39] buck converters
- 2 x 10Ω Power resistors
- 1 x 100Ω Power resistor

To give a small overview of the bucks, the SVRCH2812S converters were used in the final high-level design. The LMZM23601 converters were used as a cheap replacement for simulation and prototyping and now the LM2596S buck converters will be used to analyse the behaviour of parallel bucks.

To replicate the input of the power system, the bucks were connected to a $3W, 28V$ DC power supply. At the output of both bucks, probes connected to a Rigol DS1104 [64] oscilloscope were placed to analyse the output-behaviour. The test set-up can be seen below in figure 7.1:

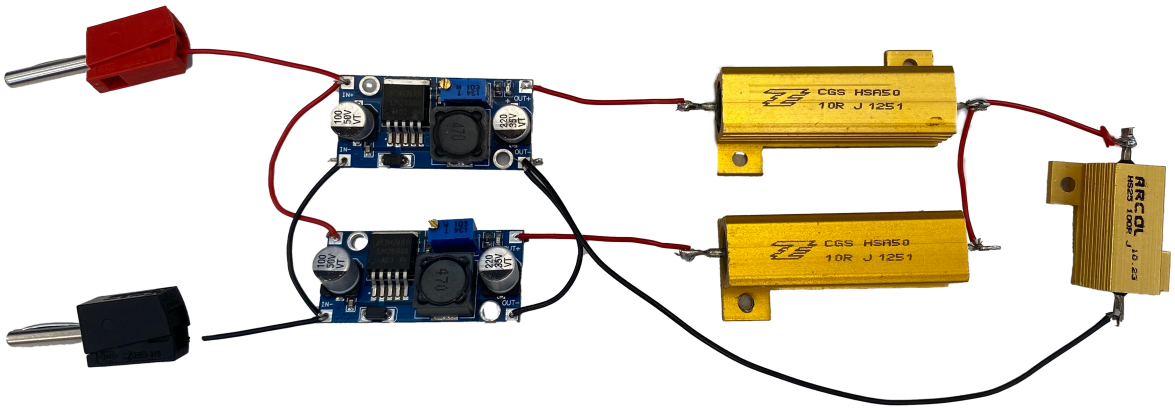

Figure 7.1: Parallel bucks test set-up

7.1.1. Test results: absolute measurements

The following output voltages were measured, as seen in figure 7.2.

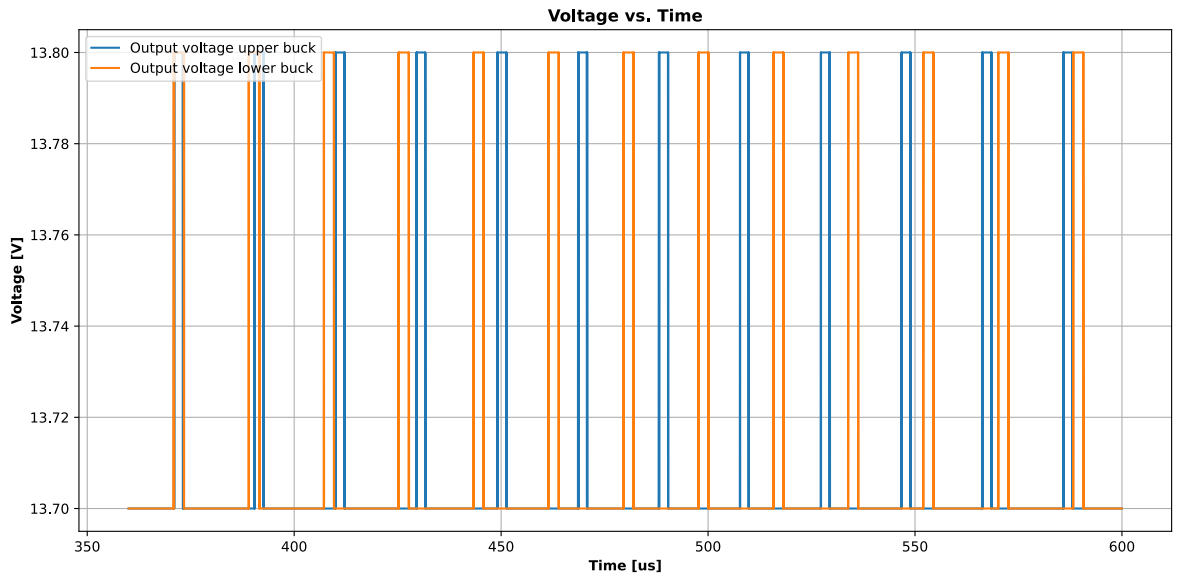

Figure 7.2: Measured output voltages parallelized buck converters with equalizer

What can be observed are voltage pulses on the output of the bucks. These pulses have an amplitude of $100mV$.
The initial thought was that these pulses occurred due to interaction between the buck converters as on the oscilloscope following signal was displayed 7.3:

This difference in graphs is probably due to filtering and down sampling of the signal in order to display the signal at a high refresh-rate. Also, the oscilloscope was zoomed in all the way to see these effects that occur in a very short time-span. It should be noted that the graphs seen in figure 7.2 are the correct ones as they are plotted from raw, unprocessed data.

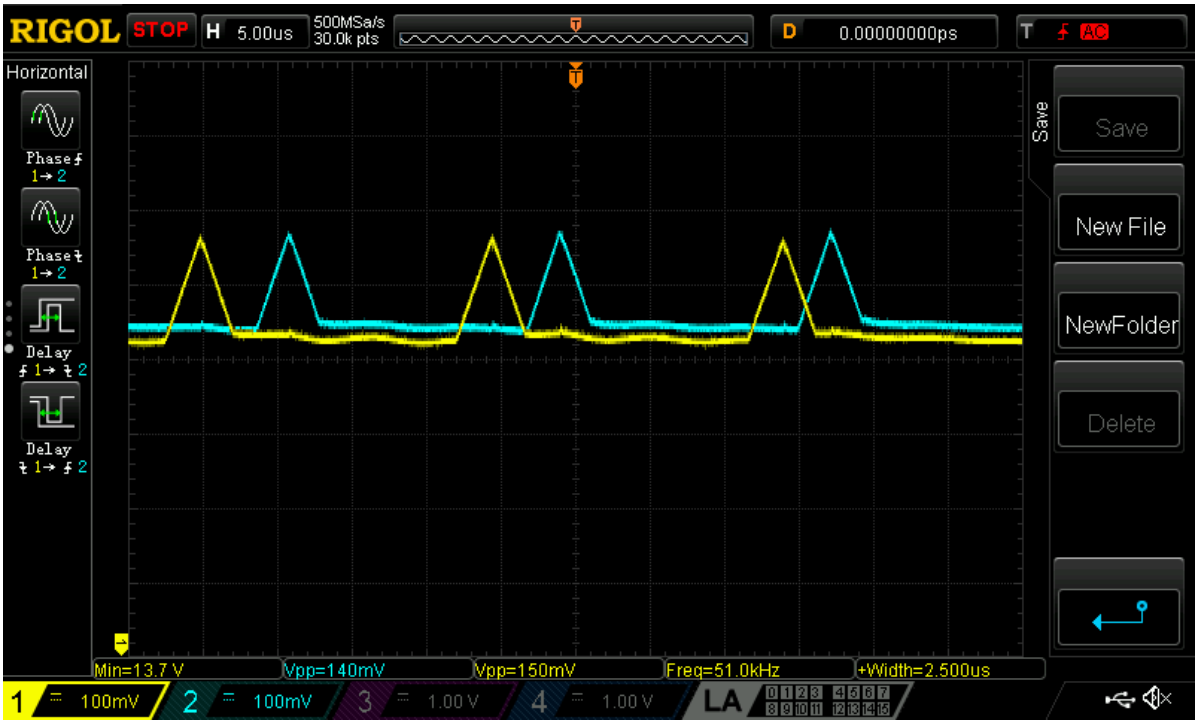

Figure 7.3: Corresponding output to 7.2, as displayed on oscilloscope (screenshot).

In figure 7.3 a much smaller interval was displayed and thus it seemed like the voltage of the first buck would give a triangular spike, which then caused a spike in the other buck too.
A possible explanation for this may be that the output voltage of the first buck (yellow signal) was slightly lower than that of the second one and that because of this, the first buck would increase its voltage until it actually overcompensates and exceeds the output voltage of the second buck. After this, it stops increasing and goes down again but as its output voltage exceeded the one of the second buck, the second buck will have started the same reaction too.
Because of this, we would see a yellow spike always followed by a blue spike.
A fault in this reasoning may be that this would have infinite voltage increase as a possible consequence. This would occur if the output voltage of the first buck has not decreased to its nominal value yet before the spike in the second output voltage occurred. This is seen in the last spike.

After analysis of the raw data 7.2, it could be seen that the output voltages actually have a rectangular pulse waveform (instead of a triangular one). It can be seen from this graph that the pulses are independent of each other as the distance between them varies along a fixed pattern, do not show to interfere the other output and are always similar in waveform.
All of this insinuates that the outputs are not related to each other and occur because of the internal working of the buck converter. It is thus highly suspected that these pulses are pulses that occur because of the internal on -and off transistor switching.

If we zoom out more we achieve figure 7.4.

Here is it even more clear that the output voltage pulses operate independent of each other, both at its own frequency. These respective frequencies are approximately $40kHz$ and $50kHz$. This frequencies fall between the internal switching frequency range of the LM2596 converter.

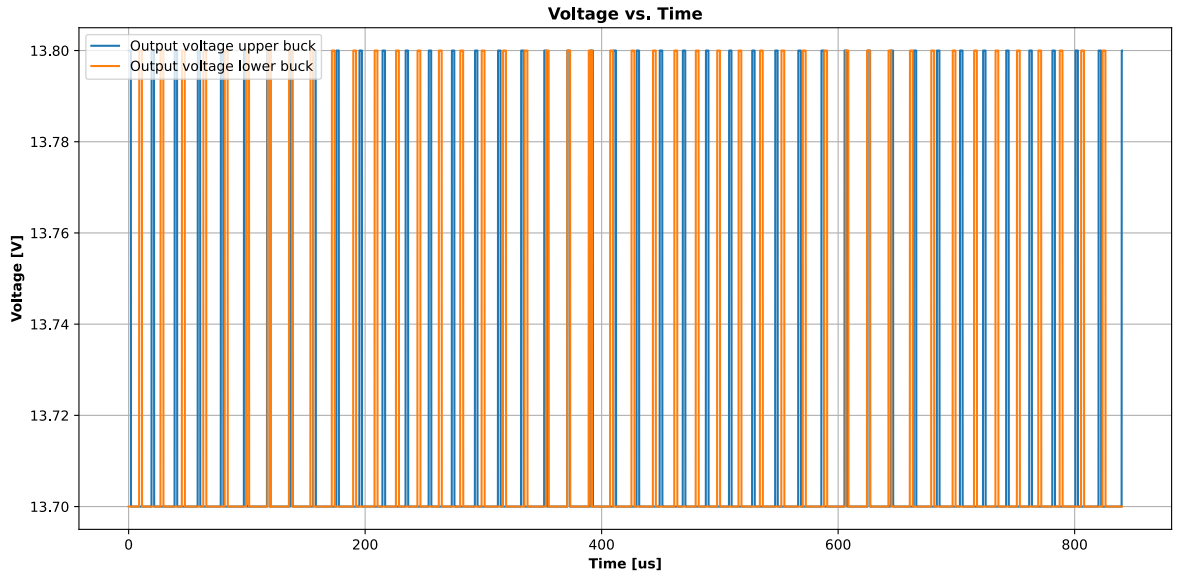

Figure 7.4: Measured output voltages parallelized buck converters with equalizer, zoomed out.

7.1.2. Test results: differential measurements

After interpretation of the absolute output voltage measurements, it seemed of interest to measure the differential signal between the two output voltages. This was done with the same set-up, but with an added mathematical subtraction expression on the oscilloscope.

The collected data is plotted in figure 7.5:

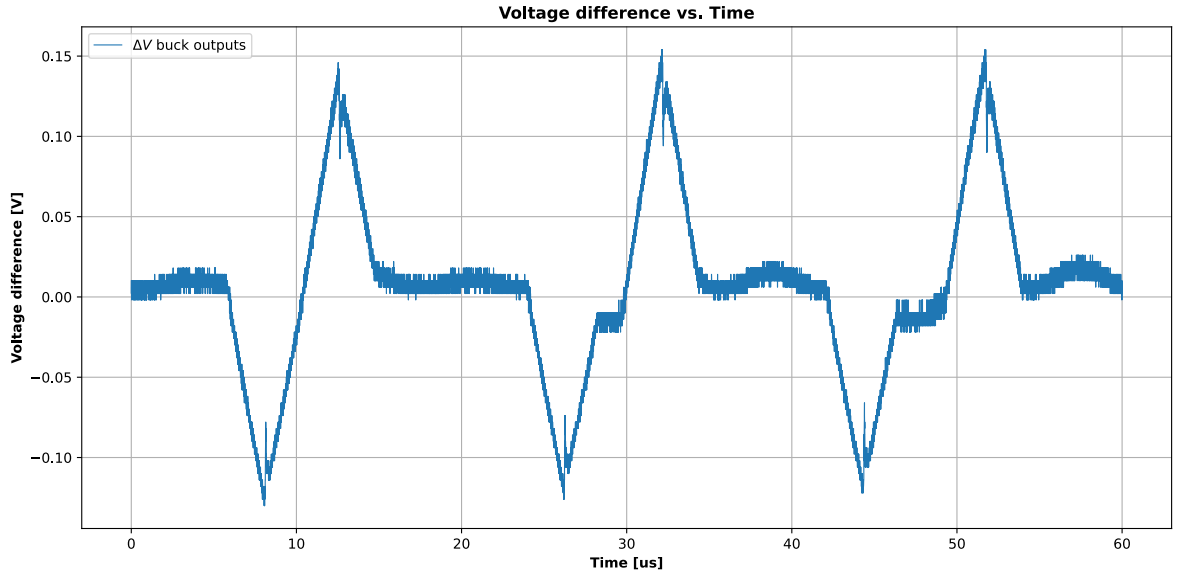

Figure 7.5: Parallelized buck converters: differential output signal

This periodic signal is no new information as it is the difference of the signals seen in 7.2, but gives clearer insight in the current imbalance between the buck converters.

As can be seen, the difference between the output voltages has a maximum absolute value of $150mV$.

This differential signal is the total voltage over the two equalizer droop resistors and resembles the imbalances during stead-state between the two buck converters.
From calculations similar to the ones seen in C.3.3.2, it can be calculated that the current through each droop resistor is approximately $70mA$.
Knowing that there is a maximum, absolute voltage difference of $150mA$ over the, in total, 20Ω resistors, the current due to this difference is $\frac{0.15V}{20\Omega} = 7.5mA$. We can see that the maximum current imbalance is approximately $\frac{7.5mA}{70mA} = 11\%$ of the total current.

It can be seen from these calculations that if the resistance is increased, these imbalances will be decreased. We again come to the consideration of section C.3.3.2, where imbalances are weighted against maximum load power.

It should be noted that all these tests can be easily repeated, for any bucks and resistor values, also the ones used in the simulation design 6.1. These concern the LMZM23601 converter, two 8.2Ω resistors and a rover load of 87Ω.

7.1.3. Transients

Also, it was intended to capture the output voltage transients on power-on of the buck converters for analysis purposes. However, it was not possible to capture these as these event occurred extremely fast. Some output voltage fluctuations were noticed for an extremely short time-span but then gave the results seen in figure 7.2.
The system comes very quickly to a balanced, steady-state operation, which shows that the circuit behaves as intended and parallelization of bucks was successful.

7.2. Prototype testing

While the prototype PCB was being built, some last-minute, rapid tests could still be done. From these, it came out that all voltage busses were at their expected voltages ($28V$, $12V$ and $3.3V$) and that the capacitor is able to charge up to at least $27.4V$ with the charging circuit. For higher values, the charge time just had to be increased. This last value indicates correct functioning of the capacitor charging circuit.

7.3. Future test plans

Although the testing phase could not be completed as a whole, a testing plan was devised. In this plan, the main points that need to be tested are treated. If all these different facets of the system are tested, the resulting data can be analyzed. This analysis will then determine if the results of the test adhere to the requirements and objectives of the system.

To achieve results that can be properly analyzed to determine the quality of the design, these parts must be tested:

- Determine the output current of each buck converter and analyze the output on the 12 V bus after the equalizer.
- Measure the output current -and voltage ripple after the equalizer.
- Long-term operation of the entire system.
- Effects of current-limit triggering for both -and individual bucks by driving a bigger load.
- Measure the power drawn by the subsystems to determine the power consumption.
- Measure the voltage over the individual capacitors in the bank to analyze their (dis)charging behavior.
- NEA actuation emulation through disintegrating test fuses by discharging the capacitor bank.

8

Discussion

The results of the final design are an indication of the success of the system. To qualify the system as a success, it is necessary to inspect if the initial requirements of the system have been met. In this chapter, the results of the tests, implementation methods, and components will be discussed.

8.1. Test component selection

Because of the availability and price of the space-grade components test alternatives were chosen. These alternatives need to have available working models to replicate the system. In the case of the LM3480 LDO for instance, this was chosen as the test LDO but turned out to have a Spice model that outputs $3.8V$ instead of $3.3V$. Because of this, the spice model for a different LDO was used which did output $3.3V$. This LDO was extremely similar as it was the successor to the LM3480. For future reference, Spice models for components must be verified before deciding to use said component.

8.2. Test results

In chapter 7, it is clear that some tests have already been done. Due to time constraints, more specific tests concerning the exact behaviour of the subsystems, individually and in unison, could not be tested to the fullest. This is unfortunate as this leads to an open end of the systems' physical design.

8.3. Simulation models

Ideally, it's best to create simulations for all subsystems and to physically test them separately as well to accurately analyze their behaviour. Unfortunately, this way of working could not be applied during this project, due to the high-level design phase taking up a majority of the duration of the project. Working out every single subsystem in simulations as well as testing them became unrealistic at this point and led to rushing the simulation phase and not being able to test most of the subsystems and the entire system as a whole.

8.4. Buck converters

The final design of the power system contains an alternative buck that can also be used to implement the parallel buck design. Initially, the focus was on using as many space-grade/space-qualified components as possible. Because of this, the space-qualified VPT buck converter was chosen.

8.5. Capacitor Bank

The ideal capacitors that were chosen to be used in the final design are the EP2B363M035AZS. Although these capacitors are perfectly made for this application, the weight at which they come is a disadvantage. The mass budget that was initially set for the entire system's requirements could unfortunately not be adhered to. The available capacitors within the necessary capacitance range were not ceramic. The next best capacitor type is wet tantalum. The used wet tantalum supercapacitor had the

right capacitance but weighed 80g. Multiply this with the amount of capacitors and the total weight is 240g. This trade-off is essential in judging the success of the system as it satisfies one requirement but negatively exceeds another.

8.6. Umbilical release mechanism

In the requirements of the RDS, in subsection 3.1.4.5, it is stated that the detachment of the RDS-to-rover umbilical cord should be done by the power system. In chapter 7, the issues with finding an umbilical adapter and acquiring the cords are stated. These same issues were encountered with the umbilical release mechanism. At the start of the project, before formulating the requirements, it was stated by the supervisor that an electrical umbilical release mechanism should be used for umbilical detachment. Research was done to find such a system. From this research, two electrical umbilical release mechanisms were found. The first was from Eaton[25] and the second from EBAD[29]. The description for both of these products seemed perfect for this application, as they both promise an electrically triggered umbilical release mechanism. Unfortunately, the search for more detailed information on the technical specifications of the products led to a dead end. Due to the lack of electrical specifications for the products, it was decided to remove this from the scope of the project.

9

Conclusion

The team designed a power system that provides power to the MCU, rover, and indirectly the NEAs. Parallelization of the buck converters and LDOs was applied to have redundancy in the system. A capacitor bank consisting of 3 wet tantalum capacitors is charged and discharged when the NEAs need to be fired. For this system to function at the right time, the MCU can communicate with it by receiving information from sensors and turning on/off enable pins such as the charge enable pin to control when to act based on the data gathered from the rover and lander.

The simulation of the voltage conversion system and its subsystems was successful.
The whole system meets all non-functional requirements except for the mass budget and the umbilical release. Unfortunately, because of logistic reasons and time constraints, the final PCB, on which the system is routed and soldered, could not be tested. It is for this reason that the system cannot be proven to be physically functioning.

10

Recommendations

Designed to the best of the team's ability, the power system does not completely fulfill the requirements that were formulated initially. At the end of the project, there are still certain facets that require further development. In this chapter, the focus will be on what needs to be done in the future to achieve an even better and more reliable system.

10.1. Simulations

As stated in section 8.3, proper qualitative simulations could not be done. The subsystems still need to be simulated and tested, separately and together.

10.2. Testing

In chapters 7 and 8, it is stated that the testing phase of the designed circuit could not be completed due to the PCB not being delivered on time. It is unable to conclude if the built circuit will truly function together with the rest of the PCB. Some extra components need to be soldered onto the delivered PCB. When completed, this then needs to be tested separately and together with the MCU with software developed by the software team. The next step is to analyze these results and see what can and should be improved upon. All of this, in combination with a requirement comparison, will then truly determine if the designed system fulfills its intended purpose.

10.3. Space-qualification

The second requirement for the PS in section 3.1.5.1 states that the selection of space-grade components must be prioritized over regular components. During the duration of this project, this proved to be a limiting factor. It forced the team to use very specific components that did not grant flexibility in the implementation of said components. In the case of the components that stand centrally in the PS, it is very noticeable that this selection criteria led to the use of components that compromised the mass budget. Such was the case, especially for the Bucks. In hindsight, the better thing to do is to use the designed test setup for more than just analyzing the electrical behavior of the system. The assembled test setup needs to go through rigorous tests that are done to see if it can sustain such conditions. Some of these tests concern the thermal and radiative integrity of the system. Were this test to be successful, a system would be achieved that works under the conditions of space, at a fraction of the weight, and possibly with a more optimized implementation of the design.

10.4. Energy storage

As stated multiple times throughout this report, the NEAs require a current surge to be actuated. Two types of energy storage methods were considered to facilitate the NEA actuation. For both the supercapacitors and the Lithium-ion batteries weight proved to be an issue if implemented. In addition to the weight, the Lithium-ion battery would also require a buck-boost converter, which introduces an-

other possible point of failure. Although the method for energy storage that was settled on was the supercapacitor, this still negatively impacted the mass budget. Because of this, it is necessary to do more research on energy storage methods that can actuate the NEAs and weigh less than the current supercapacitors and Lithium-ion batteries.

The Power system supplies power to the system at $12V$. Currently, the design assumes that the power draw will be distributed fairly. The rover only needs to be supplied at $12V$ meaning that current power is not being regulated. The rover therefore must contain a current power limiter to set an absolute maximum power that it can draw from the system.

10.5. Buck converter interleaving

The buck converter used during testing has feedback. Instead, a feedback-less converter should be used with a fixed output. Although offering control, the feedback introduces complexity and susceptibility to electromagnetic interference. Although having chosen the voltage droop as the equalizer method, active current control, mentioned in section 5.1.1.3, offers better performance but was not implemented due to the complexity and time constraints. Further research on how this can be implemented the best, will be very beneficial towards the overall performance of the system.
Furthermore, active current control heavily improves reliability, especially in comparison to the voltage droop method. The active current control should be designed such that if one buck fails, that the other takes over and that the faulty buck is 'isolated' from the rest of the circuit.

10.6. Umbilical cord & release mechanism

To satisfy all the requirements in subsection 3.1.4.5, the umbilical cord module needs to be further developed. This entails that the adapter for the umbilical cord itself must be further researched. An adapter needs to be found or created that can properly connect the data and communication pins of the RDS PCB to the rover and the lander. This adapter must "fit" on the PCB and have either a male or female connector, depending on the umbilical cord, that allows the umbilical cord to be attached. The release mechanism of the umbilical cord must be further researched. Due to the initial requirement for this release to be triggered electrically, this type of release trigger needs to be further researched. The two release mechanisms that were found are possible systems that can potentially work if more specifications become available. This can be achieved by possibly approaching the companies and requesting this data or by designing such a system.

11

Future Work

Designed to the best of the team's ability, the power system does not completely fulfill the requirements that were formulated initially. At the end of the project, there are still certain facets that require further development. In this chapter, the focus will be on what needs to be done in the future to achieve an even better and more reliable system.

One of the main discussion points of the system is the buck converters. The way the buck converter is currently implemented introduces an extra layer of liability. This is caused partly by possible common failure modes that both bucks may experience. To avoid this, the bucks should be made more modular, possibly on a separate circuit. This allows the bucks to have less of an impact on the success rate of the entire system.

The bucks that are used in the design don't have a high efficiency for the system's power rating. By designing custom interleavable buck converters, a higher efficiency and reliability rating can be achieved. The rover contains custom interleaved buck converters to convert the 12 V bus to 3.3 V and 5 V, as can be seen in figure 4.1. These converters have high efficiency. Because of this, it is advisable to design interleavable buck converters that can convert 28 V to 12 V while operating under the electrical specifications of the system.

Quite a few of the umbilical release mechanisms work mechanically through the use of a lanyard. If the developments of the electrical release do not lead to the desired outcome, it might be of use to Lunar Zebro to reconsider the structure of the current RDS pod to facilitate a mechanical umbilical release. To increase the effectiveness of such a release, the position of the umbilical plug on the rover should be reconsidered. For instance, if the umbilical plug is located on top of the rover, the umbilical cord can be detached by using the downward force exerted by the mass of the rover. This is a mere example of a mechanical release strategy that can be implemented if the electrical release proves to be an unconquerable impediment.

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A

Code Documentation

A.1. Input vs output power graph SVRCH2812S C.6

It should be noted that the initial arrays of output power and efficiency for the buck converters were read of C.2 and entered carefully by hand. Enough samples were taken in order to maintain sufficient resolution.
Also, the marked point was determined by interpolation between the points $(0.9, 1.28)$ and $(1.1, 1.47)$.

Code used to produce this image:

Listing A.1: Python code to plot Input vs output power graph of SVRCH2812S buck converter

```
import numpy as np
import matplotlib.pyplot as plt

########## 1.5W buck
output_power_1_5 = [0.3, 0.4, 0.5, 0.6, 0.7, 0.9, 1.1, 1.2, 1.3, 1.4, 1.5]
efficiency_1_5 = [50, 60, 63.5, 65, 67.5, 70.5, 75, 77, 77.5, 77.5, 77.5]
corresponding_efficiency_max_input_1_5 = 75.86

########## 4-6W buck
output_power_4__6 = [0.74, 1, 1.24, 1.7, 2, 3]
efficiency_4__6 = [38, 46, 54, 62, 64.1, 70]

########## 5W buck
output_power_5 = [0.52, 0.62, 0.74, 0.9, 1, 1.12, 1.44, 1.86, 2, 2.36, 3]
efficiency_5 = [30, 35, 40, 45, 47.5, 50, 55, 60, 61.1, 65, 69.5]

output_power = output_power_1_5
efficiency = efficiency_1_5
#max_input_power = 1.5; corresponding_efficiency_max_input =
    corresponding_efficiency_max_input_1_5


input_power = [round((a / b)*100, 2) for a,b in zip(output_power, efficiency)]

plt.plot(output_power, input_power, label='output␣power␣vs␣input␣power', linewidth=3)
plt.xlabel('Ouput␣Power[W]', fontweight='bold'); plt.ylabel('Input␣power[W]', fontweight='
    bold'); plt.xticks(output_power); plt.yticks(input_power); plt.grid(True); plt.ylim(min(
    input_power), max(input_power)); plt.xlim(0, max(output_power))

point_x = 0.97416
point_y = 1.35
plt.plot(point_x, point_y, 'ro')  # 'ro' makes the point red
plt.annotate(f'({round(point_x,2)},␣{point_y})', (point_x, point_y), textcoords="offset␣
    points", xytext=(45,-14), ha='center', fontsize=12, color='red')

```

```
#plt.plot(output_power, efficiency, label='output power')
#plt.xlabel('Ouput Power[W]'); plt.ylabel('Efficiency[%]'); plt.xticks(output_power); plt.yticks(efficiency); plt.grid(True); plt.ylim(min(efficiency), max(efficiency)+1); plt.xlim(0, max(output_power))

plt.legend(loc='upper left')
plt.tight_layout()
plt.title('Input vs output power SVRCH2812S', fontweight='bold')
plt.savefig('Input_output_power.svg')
plt.show()
```

A.2. Simulations result graphs 6.4

Listing A.2: Python code that serves as a base file for the functioning of coming voltage vs time and current vs time codes.

```

import numpy as np
def parse_ltspice_output(file_path):
    # Initialize a dictionary to store arrays for each node
    data = {}

    with open(file_path, 'r') as file:
        # Read the first line to get the node names
        header = file.readline().strip().split()
        print(header)
        # Initialize arrays for each node
        for node in header:
            data[node] = []

        # Read the rest of the lines to get the data points
        for line in file:
            values = line.strip().split()
            for i, value in enumerate(values):
                data[header[i]].append(float(value))

    # Convert lists to numpy arrays
    for node in data:
        data[node] = np.array(data[node])

    return data
```

Listing A.3: Python code to plot simulation results: voltage vs time graph.

```
import numpy as np
import matplotlib.pyplot as plt
from tkinter import Tk # Fileopen
from tkinter.filedialog import askopenfilename
import Functions_LTSpice_readout

# Choose file
Tk().withdraw() # we don't want a full GUI, so keep the root window from appearing
file_path = askopenfilename() # show an "Open" dialog box and return the path to the selected file
print(file_path)

# Load in data
data = Functions_LTSpice_readout.parse_ltspice_output(file_path)
data_length = len(data['time'])
print('Data points: ', data_length)


#### Plot settings
#plt.figure(figsize=(20, 10))
plt.grid(True, which='both', linestyle='--', linewidth=0.5)
plt.xlabel('Time [us]', fontweight='bold')
plt.ylabel('Voltage [V]', fontweight='bold')

plt.title('Voltage vs time', fontweight='bold')


```

```
start_index = int(0*data_length); end_index = int(1*data_length)
print('End_index : ', end_index)

#########################
#Average_power = round(np.mean(data['V(n001)'][start_index:end_index]*data['Ix(U1:VIN)'][
    start_index:end_index]), 3)
#print('Average power from interval: ', Average_power)


########################
plt.xlim(min(data['time'][start_index:end_index]*1000000), max(data['time'][start_index:
    end_index]*1000000))
plt.ylim(min(data['V(n008)'][start_index:end_index]), max(data['V(n003)'][start_index:
    end_index])*1.1)

plt.xticks(np.arange(0, max(data['time'][start_index:end_index]*1000000), step=50))
plt.yticks(np.arange(2, 15, step=1))
########################
#plt.plot(data['time'][start_index:end_index]*1000, data['V(n001)'][start_index:end_index]*
    data['Ix(U1:VIN)'][start_index:end_index], label=f'Instantaneous power, average power: {
    Average_power}W')
plt.plot(data['time'][start_index:end_index]*1000000, data['V(n008)'][start_index:end_index],
     label='Rover bus voltage', linewidth=1.8)
plt.plot(data['time'][start_index:end_index]*1000000, data['V(n005)'][start_index:end_index],
     label='3.3V bus voltage', linewidth=1.8)
plt.plot(data['time'][start_index:end_index]*1000000, data['V(n003)'][start_index:end_index],
     label='Buck output voltages', linewidth=1.8)
#plt.plot(data['time'][start_index:end_index]*1000000, data['V(n006)'][start_index:end_index
    ], label='Lower buck output voltage', linewidth=1.8) # Same as V(n003)
plt.legend(loc='upper left')
plt.savefig('Voltage_simulations1.svg')
plt.show()
```

Listing A.4: Python code to plot simulation results: Currents vs time graph.

```

import numpy as np
import matplotlib.pyplot as plt
from tkinter import Tk # Fileopen
from tkinter.filedialog import askopenfilename
import Functions_LTSpice_readout

# Choose file
Tk().withdraw() # we don't want a full GUI, so keep the root window from appearing
file_path = askopenfilename() # show an "Open" dialog box and return the path to the selected
     file
print(file_path)

# Load in data
data = Functions_LTSpice_readout.parse_ltspice_output(file_path)
data_length = len(data['time'])
print('Data points: ', data_length)


#### Plot settings
#plt.figure(figsize=(20, 10))
plt.grid(True, which='both', linestyle='--', linewidth=0.5)
plt.xlabel('Time [us]', fontweight='bold')
plt.ylabel('Current [mA]', fontweight='bold')

plt.title('Current vs time', fontweight='bold')


start_index = int(0*data_length); end_index = int(1*data_length)
print('End_index : ', end_index)

#########################
#Average_power = round(np.mean(data['V(n001)'][start_index:end_index]*data['Ix(U1:VIN)'][
    start_index:end_index]), 3)
#print('Average power from interval: ', Average_power)

```

```
35
36 ########################
37 plt.xlim(min(data['time'][start_index:end_index]*1000000), max(data['time'][start_index:
       end_index]*1000000))
38 plt.ylim(12, 86)
39
40 plt.xticks(np.arange(0, max(data['time'][start_index:end_index]*1000000), step=50))
41 plt.yticks(np.arange(12, 86, step=5))
42 ########################
43 #plt.plot(data['time'][start_index:end_index]*1000, data['V(n001)'][start_index:end_index]*
       data['Ix(U1:VIN)'][start_index:end_index], label=f'Instantaneous power, average power: {
       Average_power}W')
44 plt.plot(data['time'][start_index:end_index]*1000000, data['I(R5)'][start_index:end_index
       ]*1000, label='Current␣droop␣resistor␣1', linewidth=1.8)
45 plt.plot(data['time'][start_index:end_index]*1000000, data['I(R6)'][start_index:end_index
       ]*1000, label='Current␣droop␣resistor␣2', linewidth=1.8)
46 plt.legend(loc='upper␣left')
47 plt.savefig('Current_simulations1.svg')
48 plt.show()
```

A.3. Test result graphs

[59]

Listing A.5: Python code to plot Test results: Voltages vs time. This specific code was mostly written by ChatGPT in order to save time. label

```
1
2 import pandas as pd
3 import matplotlib.pyplot as plt
4
5 # Load the CSV file
6 csv_file_path = '/Volumes/BRECHT/mem_saves/NewFile1.csv'
7 data = pd.read_csv(csv_file_path)
8
9 # Load the TXT file and extract the sampling rate
10 txt_file_path = '/Volumes/BRECHT/mem_saves/NewFile1_csv.txt'
11 with open(txt_file_path, 'r') as file:
12     lines = file.readlines()
13     for line in lines:
14         if "Sampling␣Rate" in line:
15             sampling_rate = float(line.split(":")[1].strip().replace('Sa/s', ''))
16
17 # Extract the start time and time increment from the first row of the CSV
18 start_time = float(data.iloc[0]['Start'])
19 time_increment = 1 / sampling_rate
20
21 # Generate the time axis
22 time = start_time + data['X'][1:].astype(int) * time_increment
23
24 # Convert CH1 and CH2 to numeric values and ignore the first row
25 CH1 = pd.to_numeric(data['CH1'][1:], errors='coerce')
26 CH2 = pd.to_numeric(data['CH2'][1:], errors='coerce')
27
28 # Plot the data
29 plt.figure(figsize=(12, 6))
30 plt.plot(time, CH1, label='CH1')
31 plt.plot(time, CH2, label='CH2')
32 plt.xlabel('Time␣(s)')
33 plt.ylabel('Voltage␣(V)')
34 plt.title('Voltage␣vs.␣Time')
35 plt.legend()
36 plt.grid(True)
37 plt.show()
```

B

High-Level Design

In this chapter, the first two designs will be treated

B.0.1. Initial Design

The first draft system was designed after the first 2-3 weeks of the project. At this point, the other 2 teams responsible for some of the subsystems were also working on their high-level designs. Because of this some specifications regarding the subsystems were still subject to change. In this phase of the design the software team had not decided yet how many and which transceivers were going to be used. The team stated that a maximum of 4 would be used and that they would either need a $3.3V$ supply like the MCU or a $5V$ supply. Because of this the PS team designed for the "worst case" scenario which is having 4 transceivers at $5V$. The system that was designed can be seen in B.1. In this design, the red lines indicate connections to backup systems, the blue represents data signals and the black ones can be seen as electrical currents used for the primary power supply.

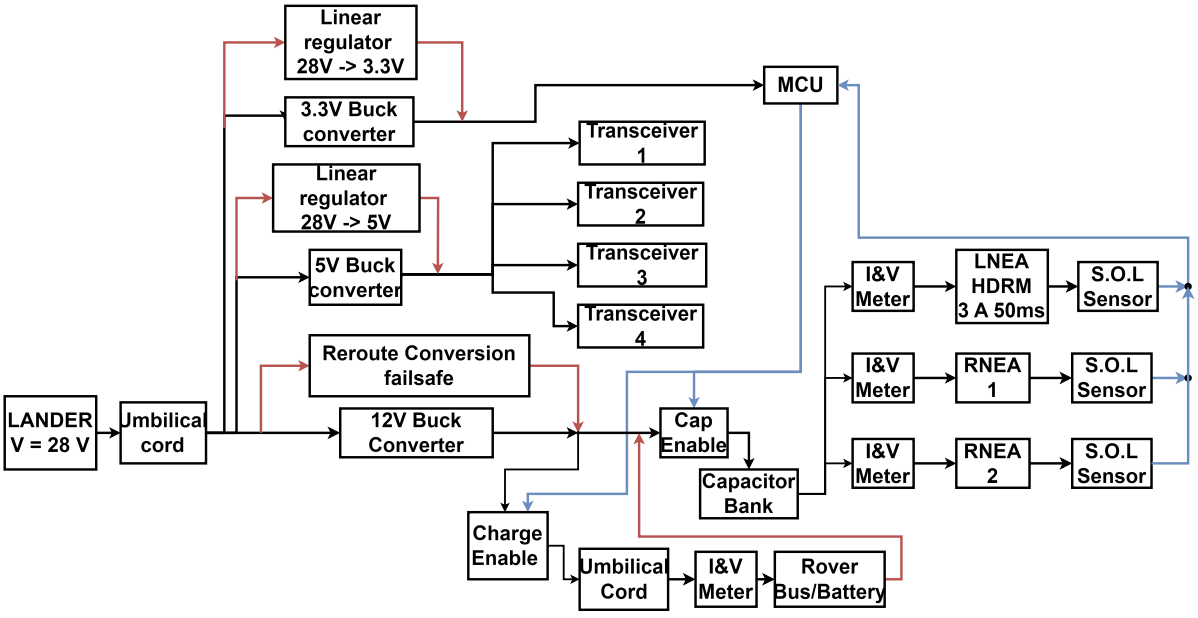

Figure B.1: Initial High-Level Design

Voltage conversion

One of the main differences between the designs that will be discussed is the $28V$ conversion to the appropriate voltages of the subsystems. In the initial design, the $28V$ bus supplied by the lander diverges into three parallel branches. On each of these branches, a voltage converter is placed to down-convert

the necessary voltages. This was done to prevent having a single point of failure as would be the case if the converters were placed in series, one after another. Here the $28V$ would be converted to $12V$ which would then be converted to $5V$ and $5V$ would then again be converted to $3.3V$. If one converter's failure leads to a $0V$ output of said converter, the next converters in the chain become useless too because their input is $0V$. This would cause some parts of the system to fail to receive the necessary power at their appropriate voltages. The down-converter that the team chose is the buck-converter. The reason for this is that for the down-conversion high efficiency and a stable output are desired. Another converter that was considered for the main conversion is the LDO regulator, Linear Drop-Out regulator. Although offering more simplicity and reliability the LDO's efficiency is extremely dependent on the voltage conversion ratio, which is undesirable. More on the team's research on LDOs and buck converters can be found in Appendix D.2.2 and D.2.3. The buck-converter placed on the first branch converts $28V$ to $3.3V$ to supply the MCU. The second branch converter converts the $28V$ to $5V$ to supply the transceivers. On the last branch, the buck converts the $28V$ to $12V$. This is used to supply power to the rover and its battery and to supply power to a capacitor bank that will be used for actuating the NEA. This will be further elaborated after this in subsection B.0.1.2. To prevent the branches from failing to convert to the appropriate voltage, a backup LDO is placed in parallel with each buck which will activate if the buck stops working. As mentioned before, LDOs are less efficient but, due to their simplicity, very reliable. As a backup system, the lack of efficiency is less of a concern because although the efficiency drops the components will still function. The MCU and transceivers in total only require .... W, meaning that the drop in efficiency will not impact their functionality. If the $12V$ buck converter stops working and the LDO takes over a drop in efficiency would mean that the rover battery and capacitor bank charge slower. As this is in buck-failure mode this is deemed acceptable.

NEA Actuation

After researching NEAs (Appendix D.1.1) the team learned that all NEAs have a similar actuation procedure. These actuators require a current surge for a certain amount of time to be fired. This amount of time ranged between $25ms$ and $8s$, depending on the brand and type of NEA. This would mean that in a short time, the system would have to deliver a relatively high current to actuate the NEAs. To achieve this, enough energy needs to be stored and discharged rapidly for the NEAs to actuate. An easy way of storing energy in this fashion is by using a capacitor. The idea is to charge the capacitor up to a certain voltage and when the NEAs need to be fired, the charge current will be cut off and the capacitor will discharge. The energy necessary for actuation will depend on the NEA and the energy that a capacitor can store depends on the charge voltage and the capacitance as can be seen in equation B.1.

$$E = \frac{1}{2} * C * V^2 \tag{B.1}$$

At this stage in the design, the RDS mechanical department informed the team that 3 NEAs would be used as can be seen in figure B.1. Each of these NEAs has a S.O.L. module connected to it. S.O.L. meaning Sign Of Life. This component will send a high or low data signal to the MCU to inform if the NEAs have been fired or not. The capacitor bank will start charging once the MCU activates the Cap Enable signal and will also discharge when the MCU is informed by the lander that the rover may deploy.

Rover Battery

The rover battery needn't be charged continuously. When the rover communicates to the MCU that it requires power, the "charge enable" will be set to high and will act as a switch that connects the $12V$ bus of the PS with that of the rover. Besides being charged, the rover battery can also be used as a back-up to charge the capacitor bank. If for some reason, like a malfunctioning of the buck converter, the capacitor bank cannot charge from the $12V$ bus anymore, the rover battery will be able to provide power to the component.

B.0.2. Second Design

After coming up with the first design, some minor changes were made to the specifications of the subsystems. The team also ran into some issues while researching some of the components. Because

of this, the team returned to the drawing board to devise a system that would work with these new changes and discoveries. The system that was designed can be seen in figure B.2. Here, the red lines indicate connections to backup systems, the blue represents data signals and the black ones can be seen as electrical currents used for the primary power supply. In this chapter, this design will be treated.

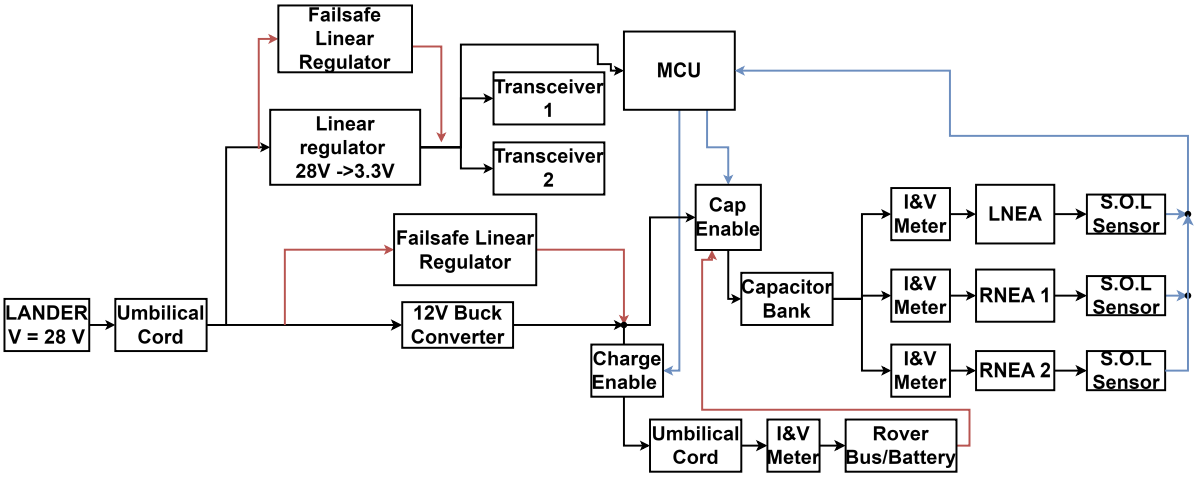

Figure B.2: Second High-Level Design

Voltage conversion

After coming up with the initial design, the software team acquired more clarity concerning their design. Due to this, the conversion buses needed changing. This can be seen when looking at the transceivers in the schematic. The software team informed the PS team that only 2 transceivers will be necessary for their design and these transceivers require a $3.3V$ supply voltage. Because of this, the $5V$ conversion bus, which was implemented in the previous design, was scrapped.

The second big change in the follow-up design lies in the converters. For the initial design, a buck converter was used for every voltage bus, the $3.3V$, $5V$, and the $12V$ one. This has changed for the second design. Firstly, it can be seen from B.2 that a Linear Regulator (LDO) is used to make the $3.3V$ bus instead of a buck converter. This decision was taken because of several reasons.
The first one is because of the increased reliability that an LDO brings compared to a buck converter. An LDO has a far simpler design and requires fewer external components to function properly, which makes it easier to implement too.
The second reason comes from the redundancy of power efficiency in this conversion. The MCU's and transceivers' power usage lies in the decimal mW power range. Even if 70% of the power is lost, it is still not significant in comparison to the total available power to the circuit ($3W$).
Furthermore, another reason is the low weight -and cost of an LDO in comparison to a buck converter. The weight -and cost difference between space-graded versions of bucks and LDOs is significant.
A final reason is because of the low load current characteristics that an LDO offers. They are typically very robust at delivering the desired output voltage, independent of the load. The load to be driven can thus be very small, and the LDO will still deliver the correct voltage at its output. A buck may sometimes, depending on the model too, need a minimal load to be driven in order to function properly. If the output current becomes too small, the buck might 'shut down' ($0V$ output) or show unexpected behaviour.
Considering the increased reliability, lack of high-efficiency needs, lower cost -and weight, and the low output current characteristics, the decision was thus made to replace the $28V <-> 3.3V$ buck with an LDO to convert this voltage.
As previously mentioned, the $5V$ bus became redundant and was thus, together with its converter, taken out of the design.
The high-level design of the $12V$ converter remained the same, but the choice of the buck converter was worked out more. A buck converter was kept here because of the necessity for good efficiency. This is the case as a relatively big amount of power will pass through the converter in order to charge the rover or the capacitor bank.

As stated in the general requirements 3.1.5.1, the circuit should contain as many space-graded components as possible. As the buck converter is one of the more important components of the power system, it seemed evident to choose a space-graded version. After a lot of comparisons, the SVRCH2800S [35] and SVSA2800S [36] series space-qualified buck converters of VPTPower [37] came out as the only options. The main drawback for alternatives was the required power range. There are not many converters available in the sub-$3W$ power range with decent efficiency. The market for high-power space-graded buck converters is a lot bigger.
After deciding between the two series, the SVRCH2800S came out as the preferred option, which is discussed in the appendix C.1.

As was done in the previous design, failsafe converters will be placed in parallel with the main converters. For both the $3.3V$ and $12V$ converters, an LDO will be placed in parallel so that if the main converter fails, the LDOs can still provide the needed conversion. In the case of the $12V$ conversion, this will mean drastically lower efficiency, especially for relatively higher power draw.

Capacitor bank

The NEA actuation and the capacitor bank's high-level design did not change compared with the initial one. Because the team focuses more on the power delivery of the components, it was decided that the NEA actuation itself will be treated by the "Actuation and Sensing" team. Because of the team's scope, the NEA actuation subsystem was limited to the capacitor bank design and therefore renamed accordingly.

Rover Battery charging

This part of the system was not modified.

C

Circuit Design

In this appendix, the circuit design will be further explained. A better image of the design will be placed here and all the circuit details will be given here.

The complete capacitor bank can be seen in figure C.1

C.1. Buck converter choice

One of the main changes in the high-level design when going from the second to the final one, is the use of parallel bucks instead of one with an LDO as a back up. This design was first addressed in section 4.2.1.1.
Also, a choice between the SVRCH2812S and the SVSA2812S buck converters had to be made. As already mentioned in section B.0.2.1, these were the only space-graded bucks that could be used for our purposes.
The reason for choosing the SVRCH2812S and parallel bucks will be further explained in this section.

C.1.1. Reliability

One of the main reasons to choose for parallel bucks is reliability. If only one buck converter would be used, it would form a single-point-of-failure. The $12V$ bus would, in this case, fully rely on this single buck converter.
In the initial and second design 4.2, there was an LDO implemented that would serve as a back up in case of buck failure. However, as said in subsection 4.2.1.1, there was no space-graded version available that could handle the $28V$ input voltage. Furthermore, an LDO would be a very inefficient back-up, which is in line with why we come to section C.1.2. This section will give an efficiency comparison between the two buck converter options.

C.1.2. Efficiency

Efficiency plays both a role in the preference for the SVRCH12S over the SVSA2812S and in the decision for using a parallel buck configuration.
When we look at the data sheets of both converters [35] [36], we find efficiency graphs C.2 and C.3, respectively.
It should again be noted that the SVRCH2812S is a converter with a maximum power output of $1.5W$, whilst this is $6W$ for the SVSA2812S.

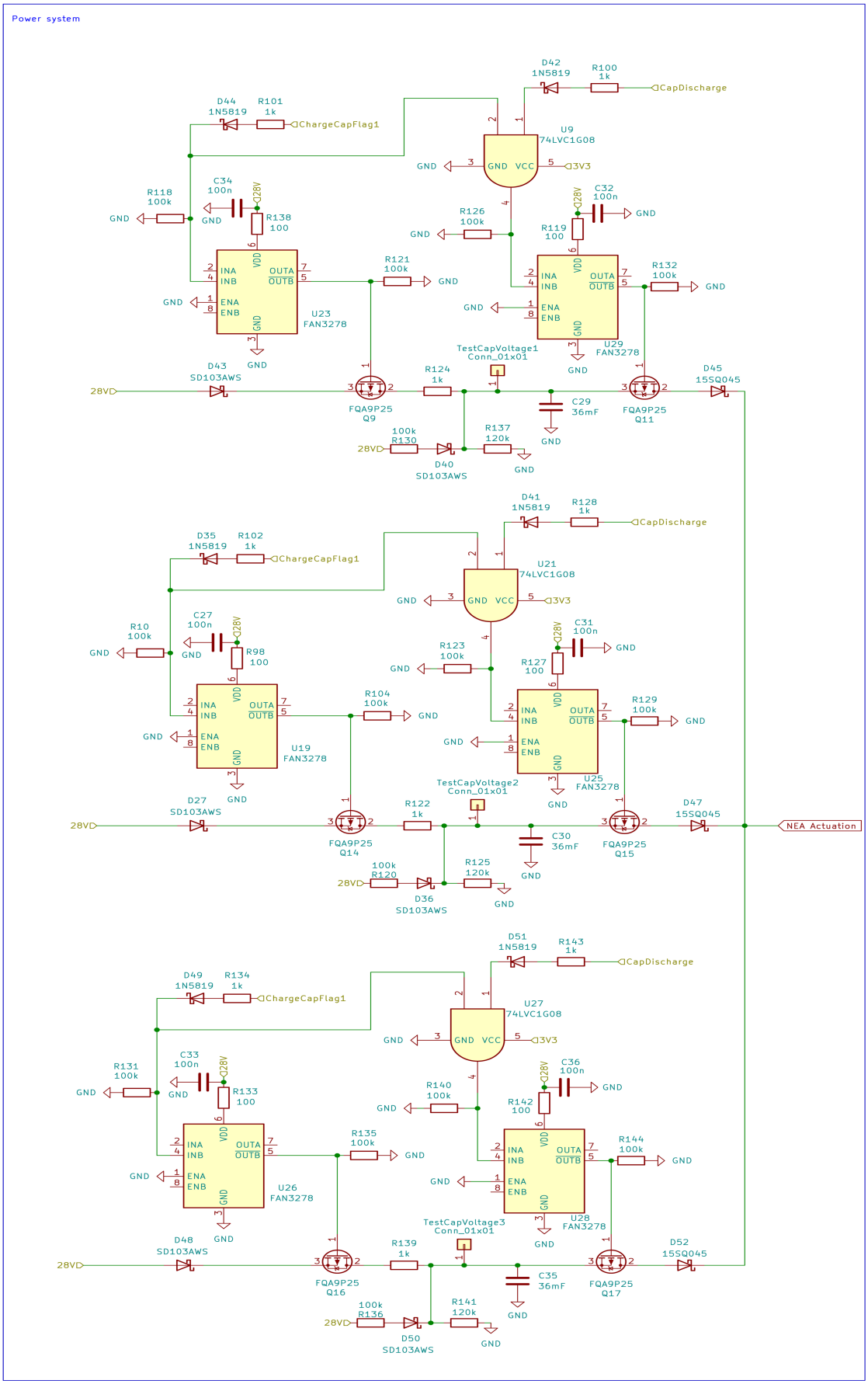

Figure C.1: Complete Capacitor bank design

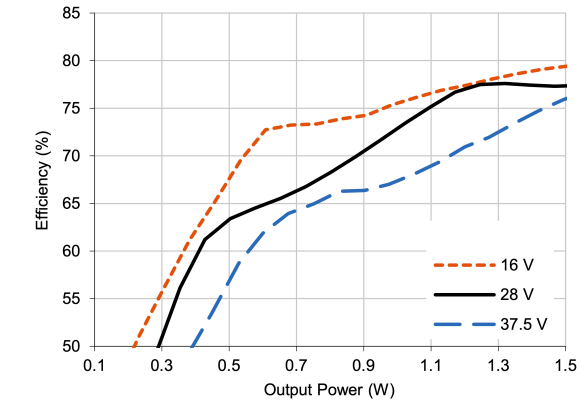

Figure C.2: Output power vs efficiency, SVRCH2812S

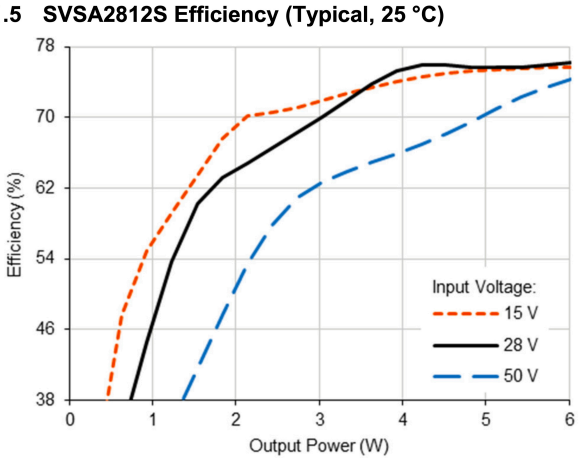

Figure C.3: Output power vs efficiency, SVSA2812S

Figure C.4: Efficiency comparison buck converters

For interpretation of these graphs, we should look at the black lines, as they represent an input voltage of $28V$. What should be noted from this comparison is the fact that the 1.5W-converter (SVRCH2812S) is a lot more efficient in the output power range from 0 to 3W, which is the maximum available power from the lander. E.g. at around $0.75W$ output power, the efficiency of the $6W$ converter is only left at around 38%, whilst the $1.5W$ converter is still at around 67% efficiency.
Furthermore, if two 1.5W-converters would be placed in parallel, it would still be possible to use the $3W$ available power to full potential, instead of $1.5W$ if only one would be used as the main buck.

Engineering-wise, it can be concluded that making a parallel configuration with two SVRCH2812S's is the way to go.
Also, the SVRCH2812S weighs $16g$, which is reasonable regarding the weight constraint stated in requirement 4.

C.2. SVRCH2812S cost overview

A quotation regarding the SVRCH2812S converter, the 1.5W-model, was requested from the manufacturer, VPTPower. An overview of prices can be found in table C.1.

Article	Delivery time [Weeks]	Cost / unit
SVRMH28/EM	±15	1.050 USD
SVRCH2812S/EM	±15	1.390 USD
SVRMH28/H+	±18	4.325 USD
SVRCH2812S/H+	±18	6.750 USD
SVRMH28/KL1	±20	6.500 USD
SVRCH2812S/KL1	±20	11.300 USD

Table C.1: Price listing VPTPower SVRCH2812S

In the table two different parts are mentioned, the SVRCH2812S and the SVRMH28. The first one is the actual buck converter and the latter one is an Electromagnetic Interference filter. This filter can be placed in front of the buck converter and improves the power quality in multiple ways. The filter helps to attenuate radiated and conducted EMI. This works in two ways. It is advantageous for the buck converter as it removes unwanted harmonics and noise on the power supply line. On the other side, it also removes the high-frequency harmonics and noise coming from the buck that is created because of the rapid switching in the converter. In essence, the filter isolates the buck converter from the circuit to ensure a more reliable operation of the overall system. Also external interference from radiation etc. will be attenuated by this filter.

It is always advantageous to have these, but not necessary. In our case, as the circuit will be quite protected from external radiation already and possible switching noise is not expected to be a problem for the circuit functioning, the use of this filter seemed redundant. This decision was also recommended by the expert on DC-DC converters under radiation of this project, Dr. A. Shekhar.
Furthermore, the high cost of the filter also plays a role in the decision not to integrate it into our circuit. A final remark should also be made that the EMI filter weighs 29g, which is quite heavy regarding the weight constraint, stated in requirement 4 and is thus conform with the decision of not implementing it in the final design.

In table C.1, different classes for the components are also mentioned. There is an EM, H+ and KL1 class.
The EM model is an engineering model for testing purposes. It is not made for flight operation, neither is it radiation hardened. It does offer identical characteristics in order to make the testing as similar as possible to the class K model, which will be discussed shortly.
There is also the class H+ model, which is a military-graded model. This means in essence that the component can withstand a large amount of external forces, temperature differences etc., all conform with the regulation about this class.
Lastly, there is the KL1 class. This is the Europe standard for class K components, as told by AVE-Electronics [6]. These components are radiation hardened and are made for space applications. They must be conform to the norms set for this class.
The exact requirements for the different classes can be found in [22].

C.3. Component choice

C.3.1. Schottky diode

A Schottky diode is a diode different from the traditional one because it uses a metal-semiconductor junction instead of a pn-junction. This makes that its characteristics are different from the conventional diode too. Some of these characteristics are relevant for our purposes. They are the following:

1. **Lower forward voltage drop**:
   the Schottky diode has a lower forward voltage drop, which reduces power dissipation and increases efficiency. As already not a lot of power is available from the lander, efficiency is an important factor in our circuit.

2. **Radiation hardness**:
   because of the metal-semiconductor junction, Schottky diodes are less sensitive to radiation-induced damage. This may play an important role in space.

3. **Improved high-temperature performance**:
   Schottky diodes perform better at higher temperatures. They work more efficient at these elevated temperatures and usually have higher temperature ratings. Also, because of their increased efficiency (see point one), they heat up less. Thermals are important in space as there is a lack of convective cooling.

C.3.2. PMOS

A PMOS (instead of a NMOS) should always be used when pulling the drain to the source voltage, which happens when applying a negative gate-source voltage. This is equivalent to making the transistor conduct. This is a basic concept of CMOS technology and will not be much further elaborated on. If a NMOS would be used, a relatively large (compared to PMOS) voltage drop will occur across the Drain-source and the NMOS will not conduct well as its channel is closing as the source voltage increases. It will end up in a sort of equilibrium in which the NMOS will slowly heat up and dissipate power. This causes inefficiency, a voltage drop and even possible damage to the transistor. A PMOS

should thus always be chosen when pulling the drain high.
Furthermore, in case of MCU failure and none of the pins are high, the PMOS' will be in conducting mode. This is preferred, as the supercapacitors will be charged and the capacitor bank will be in the 'armed'-state still. NEA actuation can thus still proceed.

C.3.3. Resistors

Feedback resistors

When looking at the datasheet of the chosen test-buck converters [41], section 8.2.2.4, an explanation for the determination of feedback resistor values can be found.
Together with image C.5 and equation C.1, following explanation is given:

'The adjustable version of the LMZM23601 regulates the output voltage such that the FB node voltage is equal to the internal VREF voltage of 1 V. The output voltage is then set by a feedback voltage divider formed by two external resistors, RFBT and RFBB. The range of adjustable output voltage is $1.2V$ *to* $15V$*'.*

$$V_{\text{OUT}} = V_{\text{REF}} \times \left(\frac{R_{\text{FBB}} + R_{\text{FBT}}}{R_{\text{FBB}}} \right) \tag{C.1}$$

Then, a value for R_{FBT} should be chosen in the $k\Omega$ and then R_{FBB} should be chosen according to formula C.2.

$$R_{\text{FBB}} = \frac{R_{\text{FBT}}}{\frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1} \tag{C.2}$$

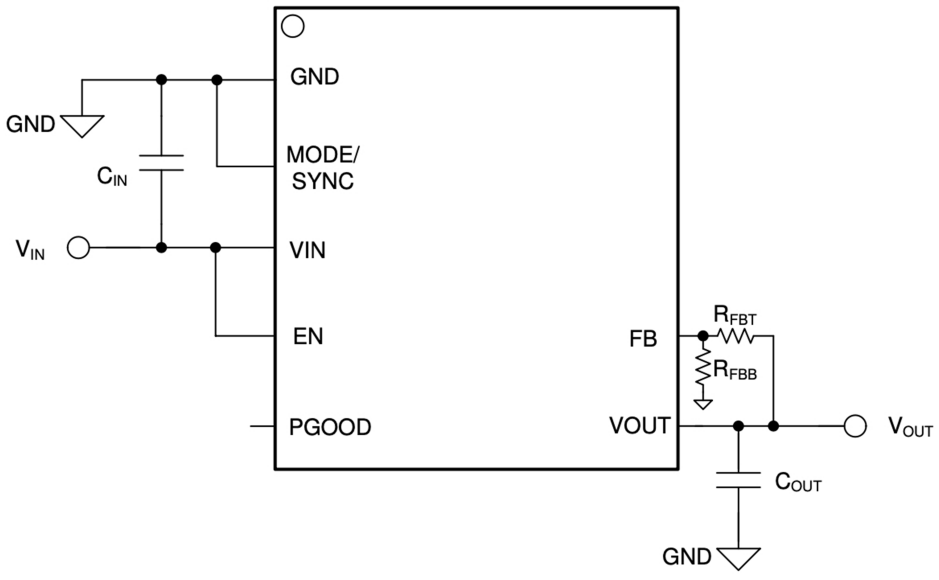

Figure C.5: Feedback network TI LMZM23601

Following this procedure, with $V_{\text{OUT}} = 12V$, R_{FBT} was set to $47k$ and consequentially, R_{FBB} determined to be $4.2k$. Both values were determined with an eye on typical resistor values.
These values give an output voltage of $12.19V$.

Voltage droop resistors

Looking at figure 5.3, we can see that the feedback network, consisting of the the $3.9k$ and the $47k$ resistors. As mentioned in section 5.1.1.1, the $3.9k$ should in theory be a $4.2k$ resistor, but this resistor was unavailable at the moment of designing. This has as a consequence that the output voltage will lay at $13.05V$ instead of $12.19V$.
Calculations will be done with the $3.9k$ in order to avoid confusion.

First of all, according to formula C.1, the voltage after the equalizer will be $13.05V$.

Now, an equivalent circuit should be made that behaves as if the rover is charging with almost maximum allowed power.
Just as for the capacitor bank, the maximum power draw at all times should be $2.7W$. In order for this to be true, the efficiency of the buck converters should be taken into account. Calculations are done under the assumption that the used bucks are the SVRCH2812S' of VPTPower.

In figure C.2, the output power vs efficiency is plotted for the converter. By the diving the first by the latter one, the input power can be calculated and re-plotted against the output power. This was done with Python and the code can be found in appendix A.1.
Following graph is achieved:

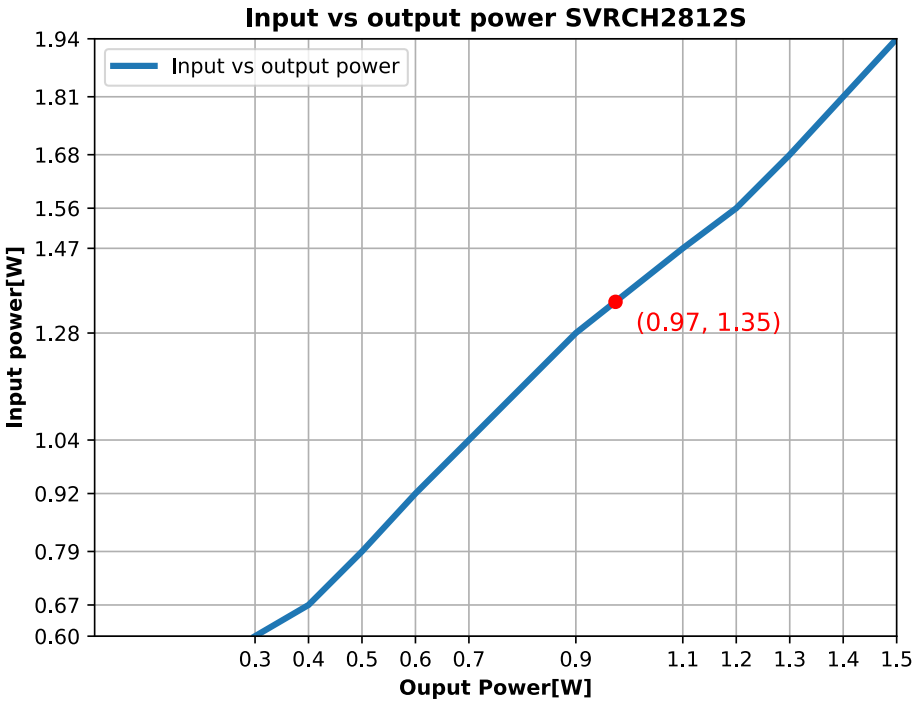

Figure C.6: Input vs output power SVRCH2812S

From this, it can be seen that if each converter gets $\frac{2.7W}{2} = 1.35W$ at its input, that it will output $0.97W$, because of inefficiency.
For to bucks in parallel, this gives a combined power output of $0.97416 \cdot 2 = 1.95W$.

Not taking the equalizer into account and knowing that a voltage of $13.05V$ will be over the equivalent resistor, the necessary resistance is calculated by $\frac{1.95W}{13V} = 0.15A$ and $\frac{13.05V}{0.15A} = 87.8\Omega$. This resistor will take resemble the rover during charging. Note that this is a very much simplified way of representing the charging process. It is just done in order to get the correct power draw from the buck converters.

87Ω will be used for calculations.

We can now use this value to form a very simple equivalent subcircuit of the equalizer with the equivalent resistor. This can be seen in figure C.7. Please note the similarity with the equalizer part in figure 5.3.

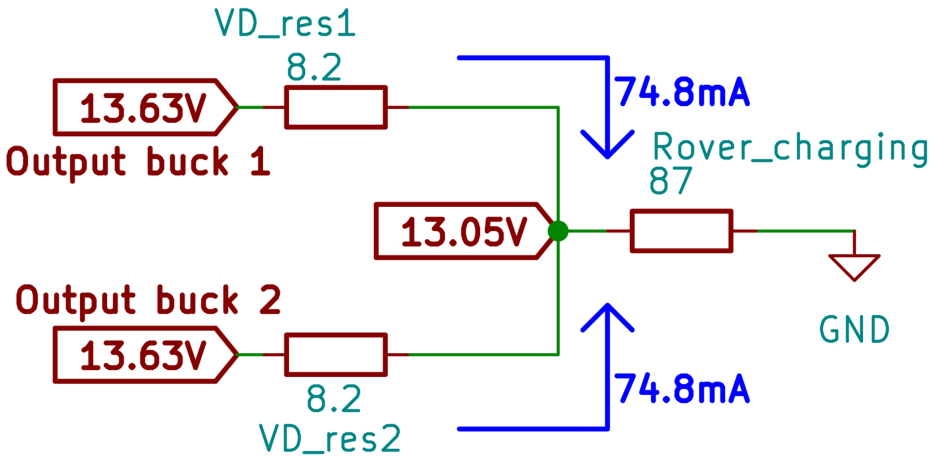

Figure C.7: Equivalent rover charging load with equalizer

As the voltage at the output of equalizer is $13.05V$, the current through the 87Ω resistor will be equal to $\frac{13.05V}{87\Omega} = 0.15A$. For the ideal case, in which the bucks are perfectly balanced, the current through each of the voltage droop resistors will be equal. This can be assumed as the average currents of both branches will be approximately equal, but the instantaneous currents will not. Because of these equal currents, both bucks will output half of the current through the 87Ω resistor, which comes down to $\frac{0.15A}{2} = 75mA$ each.
From this current and the resistance of the voltage droop resistors, 8.2Ω, the voltage at the output of the buck converters can be calculated. This is $13.63V$.

From all previously calculated values, the total power consumed can be calculated, as well as the power dissipated by the Voltage droop resistors.

The power dissipated by the voltage droop resistors:

$$P_{\text{diss}} = 2 \cdot 8.2 \cdot 0.075^2 = 91.8mW \tag{C.3}$$

The power dissipated by the total circuit:

$$P_{\text{total}} = 0.15^2 \cdot (\frac{8.2}{2} + 87) = 2.05W \tag{C.4}$$

The losses due to the equalizer circuit consume $\frac{0.0918W}{2.05W} = 4.5\%$ of the total power. This is reasonably within margin.

The calculations can be easily repeated for the $4.2k$ resistor and will thus not be repeated.

The instantaneous current imbalances should now be checked by means of testing as this is quite random behaviour of the buck converters. If the imbalances are too big, the values of the voltage droop resistances can be increased, but this will increase the power losses due to the equalizer.

1k Capacitor current limiter
A maximum power draw of $2.7W$ was assigned for the capacitor bank charging. This to always assure power is available for the MCU, it now still has $0.3W$ dedicated to it when the capacitors are being charged. The MCU and transceivers, in active mode, consume together approximately $21.78mW$. Large margin was taken for this, to address for inefficiency of the bucks and LDOs, resistive losses or unforeseen power draw elsewhere.
The calculation for the resistance goes as follows:
If $2.7W$ is assigned for cap charging and there are three capacitors to be charged, every capacitor can draw up to $\frac{2.7}{3} = 0.9W$ of power. In worst case, the largest current draw will take place when the capacitor is fully discharged and is thus at $0V$. This should normally never occur as the capacitors are biased. When the PMOS starts to conduct, there will be voltage difference of $28V$ over the resistor. To calculate the maximum allowed current under these circumstances: $\frac{0.9W}{28V} = 32.14mA$. From this we calculate the necessary resistance: $\frac{28V}{0.03214A} = 871\Omega$. Now consider some typical resistor values and take some more margin and we end up at $1k\Omega$. This value may be lowered slightly if the charging of the capacitors should be faster. As enough time is foreseen to charge the capacitors, this seemed unnecessary and extra margin for the MCU was preferred. Reverse-calculations with a $1k\Omega$ resistor give a total, maximum power draw of $2.352W$.

C.3.4. Supercapacitor
The goal of the capacitor bank is to store and discharge energy to fire the NEAs. The EBAD 9040 HDRM requires 3 A for 50 ms and has a maximum internal fuse resistance of 1.8Ω [28]. The EBAD 1120-05 Pin Puller NEA needs 4 A for 25ms and has a maximum internal fuse resistance of 1.6Ω[27]. To determine the necessary actuation energy, equation C.5 is used.

$$E = I^2 * R * t \tag{C.5}$$

When designing, it is always good to implement margins if something goes differently than expected. Because of this, the current value used is $5A$, instead of the highest current value of the two NEAs. When looking at the built circuit of the capacitor bank in figure 5.3 and figure 6.7 of the report of the Sensing and Actuation group [49], it is noticeable that multiple components between the supercapacitor and the NEA also dissipate energy. This is because of internal resistance of the NEAs, forward voltage drops across diodes, on-resistances of transistors and trace resistance.
All of these resistances added-up together, worst-case (according to respective datasheets), come in at around 3.6Ω. Taking heat into account, as it may increase the resistance of components quite significantly and some extra margin, this value is rounded up to 5Ω. As the longest actuation time out of the two NEAs is $50ms$, and quite some margin was already in calculated, this time value was used. Filling in all foregone values and solving equation C.5, leads to an energy of $6.25J$.
In order to calculate the necessary capacitor voltage, equation B.1 is needed in a slightly adjusted form. As the current should always stay above 4A for the NEAs, the voltage of the capacitor should always stay above $4\Omega \cdot 5A = 20V$. From this voltage, together with the necessary energy, we get equality C.6:

$$\frac{1}{2} \cdot C \cdot (28^2 - 20^2) = 6.25J \tag{C.6}$$

Calculating C from this, we get $C = 32.6mF$.

For the calculated capacitance, a capacitor needs to be found. This posed slight difficulties. When picking capacitors, one has to be aware of the type of capacitor. This is very dependent on the application. Aluminum electrolytic capacitors offer high capacitance at a relatively low price. Unfortunately, this type of capacitor is not suitable for space-applications. Aluminum electrolytic capacitors can release water and organic vapors as a result of parameter changes caused by ionizing or burst radiation. They also have a high probability of popping in a vacuum due to the dielectric being weakened and the DC leakage current increasing. For space applications, the capacitor types that work the best are ceramic capacitors and tantalum capacitors[3]. Although the best for this application, ceramic supercapacitors are unfortunately non-existent for such high capacitances. This led to the choice of wet tantalum supercapacitors. Based on the calculated capacitance (with a bit of extra margin) and availability of

components online, the EP2B363M035AZS capacitor was chosen. This capacitor has a capacitance of $36mF$, a mass of $80g$, and is rated for a maximum voltage of $35V_DC$. This capacitor is also specifically made for ”industrial, avionics, military/space, capacitor banks” [71]. This can also be seen when looking at its MIL-STD-202 rating. A product qualifying for this rating has undergone extensive and rigorous testing concerning its thermal and radiation resistive integrity, for example[21].

D

Literature Research

Designing an electrical power system for the RDS requires knowledge acquired during the Bachelor's. Although the team already has a base understanding of the knowledge required to design the system, it does not know everything. To find components and their specific behaviour for example research is needed to acquire the specific knowledge to be able to optimally apply said knowledge in the design. This research was divided into two separate studies. The first is the preliminary literature study in D.1 which was done before commencing the design process. The second is the Design-Phase Literature Study in D.2 which was done as the name suggests during the design to acquire extra knowledge needed.

D.1. Preliminary Literature Study

In quarter 4, the project started. In the project's first week, the team performed a literature study to familiarize itself with the knowledge necessary to begin designing a system that could satisfy the project's requirements. It also allowed the team to explore the application of different components and systems in this specific circumstance, namely space. All of this will be treated in this section.

D.1.1. Separation devices

For separators in space applications, there are broadly two categories: non-explosive actuators (NEAs) and explosive actuators (pyrotechnics). These types of devices are very important in space applications [74]. In the field, there is a trend towards using NEAs such as hold-down and release mechanisms (HDRMs), as pyrotechnics have certain issues with shockwaves and testing [57]. Because of this broad use of NEAs, the team researched different types of NEAs from multiple companies to get an idea of the type of NEAs. The three main companies of which NEAs were researched are DCubed, Airbus, and EBAD. From DCubed the team found the nD3PP [18], nD3RN [19], uD3PP [16], uD3RN [17] and nD3SP [20]. For EBAD a general catalogue of NEAs was found[26]. The last NEA found was Airbus NELS HDRM, Non-Explosive, Low Shock Holddown, and Release System [11][1].

D.1.2. Soldering

In recent years, there is a shift away from using lead in all sort of processes and products as it is highly piousness for humans. Since 2005 NASA suggested using lead free soldering for space[50]. This would be accomplished by a silver copper alloy. However this soldering comes with its own sets of disadvantages and as of today it is still possible to buy lead soldering. It is clear that SnPb tin-lead alloy is still the best possible soldering material for space applications[9] [32]. Although its health risks this material will be used throughout the project.

D.1.3. Components in space

During the mission, conditions that are extreme compared to those on earth are quite likely to occur. It is therefore necessary that the components of the design are able to withstand these extreme conditions.

The harsher conditions mainly consist of the vacuum of space, increased temperature swings, and higher background radiation. The background radiation problem is less relevant, as the RDS CS will be mounted inside a Faraday Cage.

One could also try to keep the environment around the components at a stable temperature, but there are quite significant benefits to having the components be intrinsically stable [30].

Capacitors
Ceramic capacitors still work down to -200 degrees Celcius [33]. There are high temperature ceramic capacitors available, such as [34]. As an alternative, Tantalum capacitors can be used. They often offer better characteristics related to vibrations and temperature swings. [5].

Resistors
Resistors that are as good as temperature-independent are available [63].

Inductors
Some inductors are able to withstand temperatures from -200 to +150 degrees Celcius [24].

Power MOSFET
For the power system and other subsystems power MOSFETs are used. Because of the extreme thermal conditions of space the team researched the behaviour of power MOSFETs in these conditions[69]. This paper analyzes the different characteristics of MOSFETs during a change in thermal conditions.

D.1.4. Power flow
Power flow control will be of significant importance during transport and deployment of the robot. Active control should be implemented to monitor state of charge, voltages, currents etc. and to make decisions about power delivery. NEAS also have to be powered at the right moment for deployment.

Battery related
The design of the battery pack is not treated by this subgroup but in order to design the power system, knowledge about battery functioning and effects on them in space is necessary. [62] includes a very extensive explanation and comparison between batteries. Furthermore, [7] includes guidelines on the usage of lithium-ion batteries in space. Lastly, thermal effects on lithium-ion batteries are discussed in [54]. More specifically, the datasheet of the NCR18650B lithium-ion battery [61] is included as this will most likely be the battery used in the rover.

Supercapacitors
In order to meet high and short power demand, the battery pack will be assisted by (super)capacitors [45]. This is assisted by [60].

Umbilical Cords
The RDS and the rover exchange data and power from the RDS to the rover. This is done through the use of an electrical umbilical cord. A single umbilical cord can transfer both data and power which makes it an ideal connector for the connection between the rover and RDS. In order to know how umbilical cords are used the team researched different types of existing umbilical cords. Different types from different brands were researched. The circular connector seemed to be the most popular among the different brands. The circular umbilical cords researched were SOURIAU 8D Series MIL-DTL-38999 Series III[70], TE Connectivity MIL-DTL-38999[12], LEMO unipole and multipole connectors[52], ITT connectors[47] and Cannon 38999-Style Connectors[10]. Another brand of connectors that was researched was Micro-D[56]. These connectors are not circular. Different types of connectors were researched to get an overview of the specifications of the different cords. This will make choosing a specific cord in the future easier because the pros and cons of each connector are noted.

DC/DC Converter
For the power system that needs to be implemented voltage/current conversion is required based on the different power specifications of each component in the system. Because of this, the team researched the use of DC/DC converters in space applications. This research led to an article explaining the use

DC/DC Converters for the International Space Station[8]. Although this is used for a bigger system it can be used as a source of inspiration for the to be the designed RDS power system. To design a DC/DC converter for space applications certain criteria pertain to the special circumstance of outer space. To know what these criteria are a paper from NASA[48] was found which will prove helpful during the design process. One of these criteria is that special features (for example remote sense, current sharing, inhibit, and synchronization) must be used carefully. Improper implementation of this can result in damage to the load, converter, or erratic system behavior. It is also stated that when using certain components look for "Class K" instead of other marketing statements like "Space Grade", "Space Qualified", "Radiation Hardened", and "Class K Equivalent". These other titles allow the manufacturers to change the internals of the component which is not allowed for "Class K".

Battery charging system

The main objective of the power system is to direct power to the NEAs and the rover. The Power delivered to the rover will be used to charge the rover's battery. This will happen during transit as the rover mustn't run out of Power so that it can still communicate with the RDS and sense its surroundings. For designing the charging system there are 2 different types of low-power charging topologies linear and switch-mode[2]. Switch-mode chargers are more complex, require a larger application footprint, and have a higher bill of materials (BOM) count. They do have higher efficiency and superior thermal performance compared to their linear counterparts and are advantageous in high-charge current applications. Additionally, it offers greater flexibility and ease of adjustment compared to the linear charger. In contrast to switch-mode chargers, linear chargers are straightforward with a lower required minimal application space and a lower bill of materials (BOM). In high-power applications however its efficiency and thermal performance lag behind that of switch-mode chargers. Linear chargers nonetheless excel in low-power applications that require minimal size, BOM, and cost.

D.2. Design-Phase Literature Study

After finishing the preliminary literature study, the team began brainstorming and designing the system that would provide the power necessary for the RDS unit to properly function.

D.2.1. NEA

In the study before this one, the team researched different NEAs from multiple companies to be aware of what type of NEAs are being sold on the market. Initially, the team thought they would be in charge of choosing which NEA would be used, hence the NEA research in Section D.1.1. In the early stages of the design process, the mechanical department informed the team that there were 2 possible NEAs from a company called EBAD that they wanted to use. The first is the EBAD NEA® Model 9040 Miniature Hold Down[28] & Release Mechanism (HDRM) and the second is the EBA NEA® Model 1120-05 Pin Puller[27]. These components were also observed in the initial study while researching the NEAs offered by EBAD. The team then further researched these familiar components to understand these units' electrical characteristics.

D.2.2. LDO Regualtors

For the power system, down conversion was of high importance. Multiple subsystems require specific input voltages. The power supplied to the RDS by the Lander is $3W$ at a voltage of $28V$ which needs to be down-converted to $3.3V$ and $12V$. LDOs can be used to achieve said down-conversion. To understand these components, the team needed a basic understanding of how they work. During this research, the team found a Texas Instruments article[15] that explained just that. This document outlines how Low Dropout Regulators (LDOs) provide a relatively simple and cost-effective conversion method. A simplified explanation is that LDOs function as voltage dividers with variable resistances. One of the biggest downsides of this is that as the voltage drop between input and output increases, the efficiency decreases. Even though this is the case, LDOs still offer good and simple down conversion for a fixed output in situations where high efficiency is not the main focus. Because of their simplicity, they also offer high reliability, which is useful in down-conversion fail-safe implementations, for example.

Later, during the design phase of the final design, the team considered putting LDOs in parallel. To understand the workings of such a setup, the team researched the performance and behavior of parallel LDOs. With this paper[65] and advice from our supervisor, Chris Verhoeven, the team realized that

connecting LDOs in parallel should not lead to any issues on the diverging output bus.

D.2.3. BUCK converters

Another conversion method with higher efficiency than the LDO is the buck converter. During the Electrical Engineering Bachelor's, the team learned about these systems in the course "Electrical Energy Conversion". These components were used for converting the input voltage(28 V) to the appropriate voltage needed by the subsystems. During the later stage of the design phase, while working on the final design, the team came up with the idea to put in two parallel buck converters. As was done for the LDOs, the team first researched this before including it in the design and testing it. The team found a page[14] carefully explaining different measures that can be used to deal with the consequences of directly connecting two buck Converters to the same output bus.