# Gate Driver Design for 1.2 kV SiC Module with PCB Integrated Rogowski Coil Protection Circuit

Marco Stecca, Panagiotis Tiftikidis, Thiago Batista Soeiro, and Pavol Bauer
Electrical Sustainable Energy Department
Delft University of Technology
Delft, The Netherlands
Email: t.batistasoeiro@tudelft.nl

***Abstract*—Wide band-gap materials, e.g., Silicon Carbide (SiC), allow the realization of power semiconductor with superior performance with respect to the traditional Si-based counterparts. On the other hand they require more stringent short-circuit or over-current clearing time to safeguard the device lifetime.**

**This paper focuses on the analysis, design guidelines and practical implementation of a gate drive circuit incorporating fast short-circuit/over-current protection ($< 1\mu$s) based on the device di/dt measurement through PCB-based auxiliary Rogowski coils. The target power module is a industry standard 62mm packaged 1.2kV SiC MOSFET half-bridge. The gate driver protection features are experimentally tested and the target time for the short circuit clearing was satisfied, with the gate driver effectively turning off the switches within 400 ns during a short-circuit test.**

## I. Introduction

The utilization of wide band-gap power switches in the power electronics industry has considerably contributed to improvements on power conversion efficiency and power density [1]. Lower switching times and resistive on-state behavior, higher breakdown voltage and operating temperature are the most advantageous parameters that wide band-gap materials (WBG) based power semiconductors brings over the traditional silicon based ones [2]–[6]. On the other hand, new fundamental requirements emerged on the design of the gate drivers. Firstly, the short-circuit capability of Silicon Carbide (SiC) based devices is much lower than the one of the traditional silicon devices, therefore faults need to be identified and cleared within a few microseconds [2], [7], [8]. The short-circuit withstanding time and ratio between the maximum current and rated current of commercial 1.2kV Si IGBTs and SiC MOSFETs from [9] is shown in Fig. 1. As possible to notice, SiC MOSFET show higher short circuit currents, up to eight times the nominal current, and can withstand the fault for far less time than the Si IGBTs, up to 2 $\mu$s instead of 10 $\mu$s.

The most conventional protection method, the desaturation method, is not efficient in clearing the fault in few microseconds, due to its blanking time before it can react to fault [2], [7], [10]. Thus, new advanced methods have been developed, based on the measurement of the switch's leg voltage [7], the di/dt measurement using a Rogowski coil [4], [8], [11], [12] and the direct measurement of the current that flows through the switch [13]. Secondly, the fast voltage and current transitions of WBG-based switches worsen the Electromagnetic Interference (EMI) in the gate driver [2], [8], [14]. These signals can interrupt the operation of the gate driver, so particularly common-mode noise rejection must be improved in the circuit devices that interface the control unit and the gate driver.

This paper presents the design of a gate driver for a commercially available 62mm 1.2kV 120A half-bridge SiC MOSFET module with two integrated Rogowski coils, one coil for each switch of the half-bridge module, for the short-circuit/over-current protections. The protection circuitry consists of two subsystems; the detection and the reaction subsystems. The first one includes the Rogowski coils along with the necessary integrator circuits for processing the output signals of the coils, particularly for the reconstruction of the device's measured current to be compared to a threshold value defining the maximum allowed operating current. The second circuitry includes all the ICs that handle the detection signal, a D-latching action, the management of the protection status and communication with the control unit. Finally, the control unit will react to the fault signal by turning-off all the switches. The maximum target time for the protection system to detect and isolate the fault was set to be below 1 $\mu$s, which is compatible with the switch requirements [15].

The paper is divided as follows. First, the analytical model, coil transfer function and step response, and design guideline

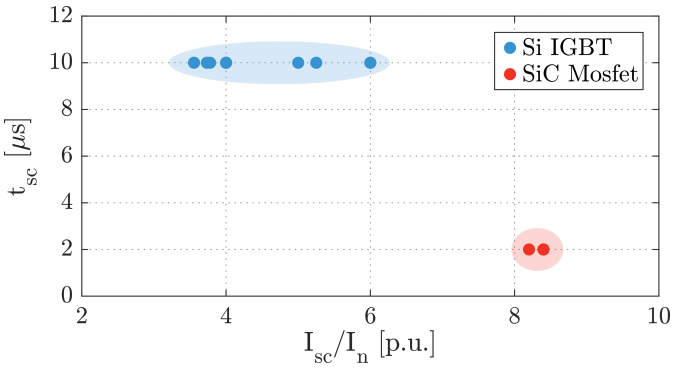


Fig. 1. Short-circuit withstanding time and ratio between peak short-circuit current and rated current of commercially available 1.2kV half-bridge Si IGBT and SiC MOSFETs power modules and TO-247 packaged discrete devices from [8].

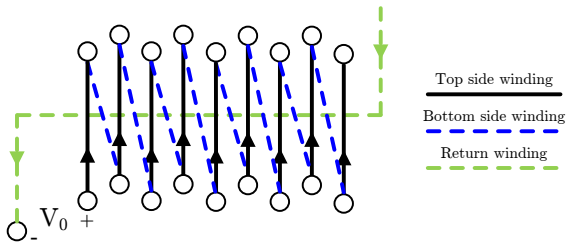


Fig. 2. Winding configuration with extra return coil to reject non-perpendicular current measurement.

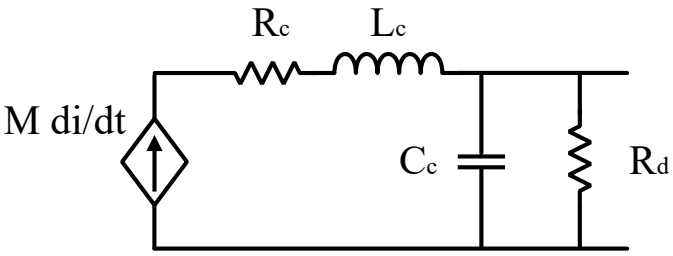


Fig. 3. Rogowski coil lumped equivalent electrical circuit.

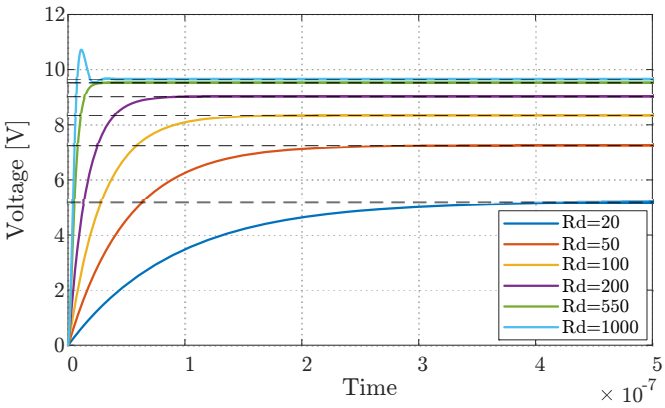


Fig. 4. Rogowski coil's step response to a $^{di}/_{dt}$ of 1kA/$\mu$s for various $R_d$.

for the selected PCB Rogowski configuration are discussed. Subsequently, the details of the proposed analog implementation of the protection circuit is presented, highlighting the different functionalities that the designed gate driver provides. Furthermore, the core gate driver circuitry is shown which features a high common-mode noise rejection capability. Finally, functional, over-current and short-circuit tests are performed in order to verify the features of the proposed gate driver and protection circuits for a 62mm packaged half-bridge SiC MOSFET power module.

## II. PCB Rogowski Coil Design

The design of a Rogowski coil is bounded by two main aspects, the physical dimension, which depend on the footprint of the power module on which the coil is built on, and the accuracy and bandwidth of the measurement, which are defined by the dimensions and number of the turns.

The power module considered in this paper has the 62mm standard footprint. From the module geometry the first physical limitation to the coil design is derived, since the window opening size depends on the size of the module pin connections. Therefore the minimum coil window opening dimensions are found to be 20x23 mm.

The appropriate winding configuration is fundamental to ensure high noise immunity and measurement accuracy from the Rogowski coil. A return coil, as shown in Fig. 2, allows the rejection of non perpendicular currents measurements. This extra coil, in fact, counterbalance the magnetic field induced by the measurement coils [12]. The next target is the mitigation of the measurement error in case the current conductor is not placed exactly in the middle of the coil. Since the positions of the coil and the module will be fixed this is not straightforward, because even a small disposition may lead to a significant error. Eventually, four extra turns are added, one at each corner, in order to reduce measurement errors [12].

Finally, the last design choice is the coil number of turns, which is geometrically limited by the dimensions of the power module and the power connections, and above all the PCB manufacturing. The operating principle behind the Rogowski coils is the Faraday's law of induction, according to which when a current conductor is placed inside a coil, there is a voltage induced in the coil, $V_0$, which is proportional to the rate of change of the current that flows through the conductor. The value of this voltage is given by the following equation:

$$V_0 = M \cdot \frac{di}{dt} \tag{1}$$

where $M$ is the mutual inductance which is given by:

$$M = \frac{N}{l} \cdot A \cdot \mu_0 \tag{2}$$

where $N$ is the number of turns of the coil, $l$ is the length of the magnetic path, $A$ is the cross section area covered by each turn and $\mu_0$ is the magnetic constant equal to $4\pi \cdot 10^{-7}$ H/m. The number of turns leads to a trade-off between the measurement accuracy and the bandwidth of the coil.

A large number of turns increases the measurement accuracy, since the output voltage increases. On the other hand, the bandwidth of the coil is limited by its resonance frequency, $\omega_0$, caused by the equivalent self-inductance, $L_c$, and the lumped winding capacitance, $C_c$:

$$\omega_0 = \frac{1}{\sqrt{L_c \cdot C_c}} \tag{3}$$

### A. Coil parameters estimation

The values for $M$, $L_c$, $C_c$, and the coil resistance $R_c$ are proportional to the number of turns $N$, while a smaller distance between the turns increases the self-capacitance. The voltage induced at the terminal of a coil is given by:

$$V_0 = L_c \cdot \frac{di}{dt} \tag{4}$$

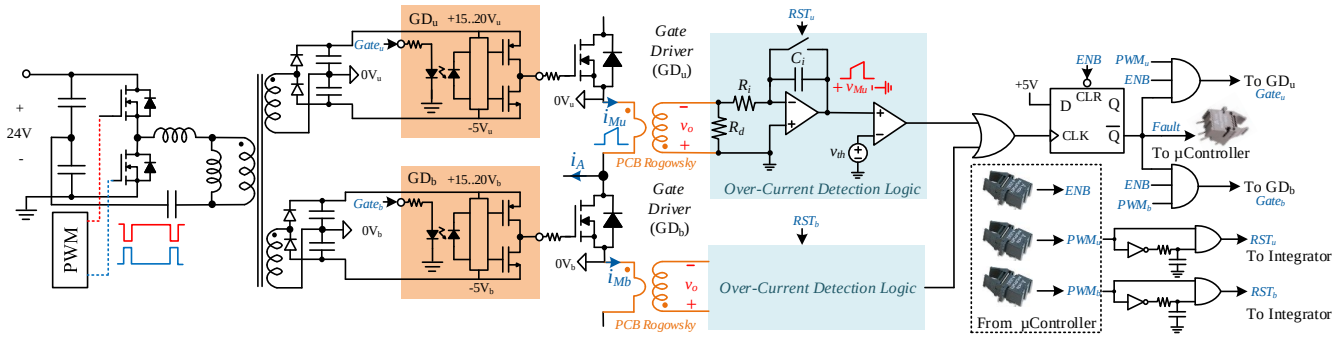


Fig. 5. Main half-bridge gate driver functional parts, including the short-circuit/over-current protection and fault handling circuits.

According to Faraday's law of induction the voltage is given by:

$$V = -N \cdot \frac{d\Phi}{dt} \tag{5}$$

The minus signal of (5) denotes only the Lenz's law and will be neglected. As for the magnetic flux flowing through an area $A$ of this equation it is equal to:

$$\Phi = B \cdot A = \frac{\mu_0 I}{2\pi x} \cdot A, \tag{6}$$

where $x$ is the distance from the measurement point of the magnetic flux with the current conductor. Considering the cross-sectional area of the turns being equal, the only parameter that does not have a fixed value is the distance $x$, since the ratios of the currents will be removed. Thus, the total magnetic flux of the coil will be $\Phi_{total} = \Phi_1 + \Phi_2 + .... + \Phi_N$, where $\Phi_1$ is the flux of turn 1, $\Phi_2$ is the flux of turn 2, and so on. Their values are given by:

$$\Phi_i = \frac{\mu_0 h}{2\pi} \cdot \ln \frac{outer_i}{inner_i}. \tag{7}$$

The coil self-inductance can be found combining (4) and 5 as:

$$L_\mathrm{c} = N \cdot \Phi_{total}. \tag{8}$$

The designed PCB Rogowski implemented in this study is composed of 269 turns which leads to a coil inductance $L_\mathrm{c}$ of 3.43 $\mu$H. This provides a close estimation to the measurement value of 3.28 $\mu$H, and a mutual inductance $M$ of 9.83 nH.

The DC resistance of the winding is proportional to its length $l_\mathrm{w}$, the resistivity $\rho$ of the material, which for copper is $1.68{\cdot}10^{-8}\Omega{\cdot}$m at 20 °C, and to the inverse of its cross section $A_\mathrm{w}$:

$$R_\mathrm{c} = \rho \cdot \frac{l_\mathrm{w}}{A_\mathrm{w}}. \tag{9}$$

The winding cross dimensions are bounded by the PCB manufacturing and therefore are 0.1 mm for the width and 35$\mu$m for the thickness. The turn length is on average 8.9mm, leading to a total winding length, $l_\mathrm{w}$, of 2.4 m and a calculated total DC resistance of 11.52 Ω.

The parameters of the Rogowski coil are listed in Table. I. The circuit parameters and the coil resonance have been measured through the Agilent 4294a Impedance Analyzer. The coil resonance was found at 53 MHz, compatible with the measurement of fast transients in the order of hundreds of nanoseconds, and with the bandwidth of commercially available high bandwidth Rogowski coils [16].

TABLE I
DESIGNED PCB ROGOWSKI COIL MEASURED PARAMETERS.

| Parameter | Value |
|---|---|
| $N$ | 269 |
| Coil inner dimensions | 22.4x29.7 mm |
| Coil outer dimensions | 27.6x34.7 mm |
| Winding cross dimension | 0.1mm x 35$\mu$m |
| $A_\mathrm{w}$ | $3.5{\cdot}10^{-9}$ m$^2$ |
| $l_\mathrm{w}$ | 2.4 m |
| $L_\mathrm{c}$ | 3.28 $\mu$H |
| $M$ | 9.834 nH |
| $R_{\mathrm{c,DC}}$ | 11.87 Ω |
| $R_{\mathrm{c,10MHz}}$ | 15.62 Ω |
| $C_\mathrm{c}$ | 2.77 pF |
| $w_0$ | 53 MHz |
| $R_\mathrm{d}$ | 500 Ω |

### B. Rogowski coil transfer function

The lumped equivalent electrical circuit model of a Rogowski coil is shown in Fig. 3, where an output damping resistance $R_\mathrm{d}$ is added to the circuit. The induced voltage at the output of the coil given a certain $^{di}/_{dt}$, according to the lumped circuit model, can be found as:

$$V_0(s) = \frac{M \cdot {}^{di}/_{dt}}{s^2 L_\mathrm{c} C_\mathrm{c} + s\left(R_\mathrm{c} C_\mathrm{c} + \frac{L_\mathrm{c}}{R_\mathrm{d}}\right) + \left(1 + \frac{R_\mathrm{c}}{R_\mathrm{d}}\right)} \tag{10}$$

The selection of the damping resistance defines its dynamic response. The coil step response for various values of $R_\mathrm{d}$ for a $^{di}/_{dt}$ of 1kA/$\mu$s is shown in Fig. 4, where it can be noted that a high $R_\mathrm{d}$ leads to a fast dynamic response and high voltage gain. In the experimental set up, $R_\mathrm{d}$ is set to 500Ω so to ensure a good trade off between response speed, oscillation damping, and output voltage amplitude, following [4]:

$$R_\mathrm{d} = 0.5 \cdot \sqrt{\frac{L_\mathrm{c}}{C_\mathrm{c}}} \tag{11}$$

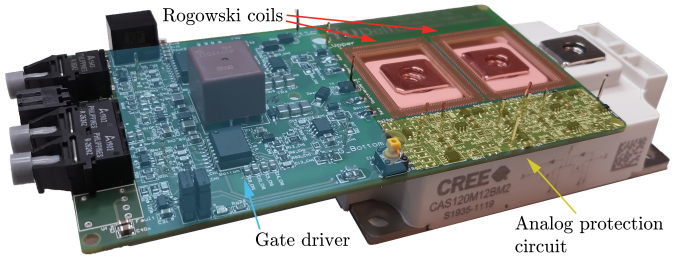


Fig. 6. Gate driver with PCB Rogowski coil based short-circuit/over-current protection for commercially available 1.2kV 120A SiC MOSFET power module.

## III. Protection Circuit

Fig. 5 shows the main functional parts of the proposed short-circuit/over-current protection circuit. A wide-band active integrator is used after each dedicated MOSFET Rogowski coil to reconstruct a realistic image of the current flowing through the device, i.e. following (1) the coil output voltage has the $^{di}/_{dt}$ current information. A reset switch is used to clear the integrator output just before the MOSFET is turned on for a better noise immunity and to improve accuracy of the over-current detection. The control signal for the reset switch is derived directly from the gate pulses which are obtained through the high common-mode noise immunity optical link from the control unit. The signal image of the MOSFET current, $v_{Mu}$, is compared to a threshold which defines the maximum allowed over-current operation. In case one of the half-bridge MOSFET detects an over-current a fault-signal is set HIGH, triggering a reaction logic of the D-latch circuit. During normal operation conditions the output of the D-latch is kept HIGH enabling that the gate of the MOSFETs follows the PWM signal generated by the control unit (PWMu or PWMb), i.e. in case the control unit has enabled the half-bridge gate driver through an optical link with the signal ENB. When a fault is detected then the output of the D-latch is turned into LOW (and this state is hold until a clear signal is applied through ENB) and by consequence all MOSFETs are turned off independently from the control unit PWM signals. The D-latch output signal FAULT is also sent to the control unit through an optical transmitter, which will trig a TRIP-Zone software protection in the control unit (or microprocessor) disabling all PWM signals.

## IV. Experimental Results

The different functionalities of the gate driver with integrated short-circuit/over-current protection described in the previous sections, namely, the reconstruction of the current waveform, the reset switch of the over-current detection logic, and the short circuit protection, have been experimentally tested. The gate driver prototype used is shown in Fig. 6, where its parts, namely the driving circuitry, the Rogowski coils, and the analog protection circuitry are highlighted with different colors.

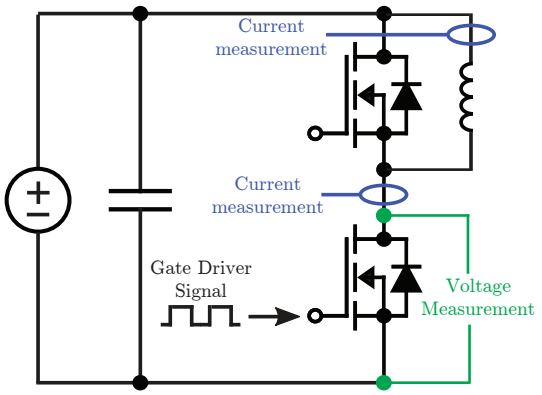


Fig. 7. Double pulse test circuit schematic.

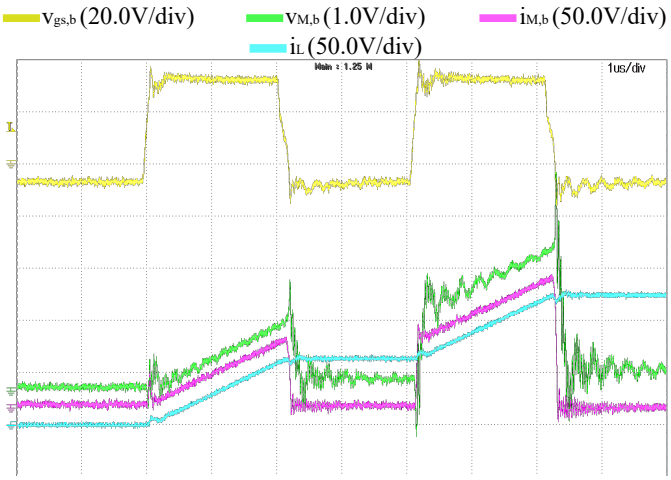


Fig. 8. Current flowing through the switch (pink), Rogowski coil output signal or reconstructed current from the integration (green), gate driver signal applyied to the bottom MOSFET (yellow), and inductor current (cyan).

### A. Current reconstruction

At first, the capability of the circuitry to accurately reconstruct the waveform of the current flowing through the switch was tested. For this purpose, the power module has been put through a Double Pulse Test (DPT), whose circuit schematic is shown in Fig. 7. This tests, typically used to characterized switching/dynamic performances of power semiconductor devices, applies two current pulses through the half bridge switches. During the DPT execution, the reconstructed MOSFET current, indicated with $v_{Mu}$ in Fig. 5, is monitored, so to compare its shape with the actual current waveform.

In Fig. 8 it can be seen that $v_{Mu}$, the green waveform, matches the actual current waveform flowing through the switch, in pink. Additionally, also gate pulses of the device under test (bottom MOSFET) in yellow, and the inductor current (in cyan) are monitored, referring to the circuit schematic of Fig. 7.

This indicates that the signal image of the MOSFET current can be advantageously compared to a threshold value for an over-current identification/protection.

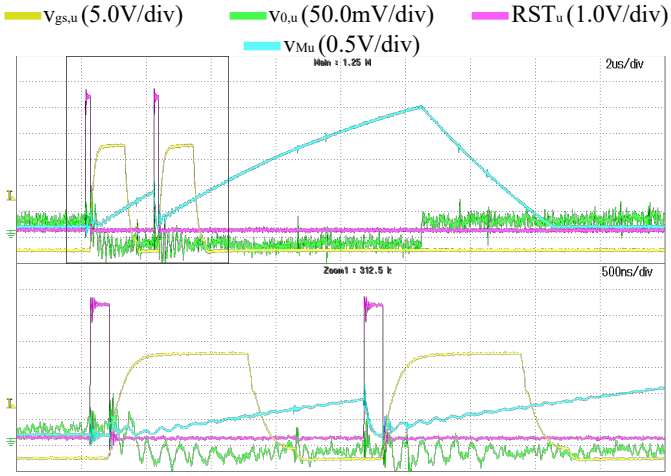


Fig. 9. Reset switch of the over-current detection logic. The reset switch whose gate signal is indicated in pink, successfully brings to zero the output of the integrator, $v_{\mathrm{Mu}}$ shown in cyan. The power MOSFET gate signal is shown in yellow, and the function generator impressed voltage $V_0$ at the input of the integrator is presented in green.

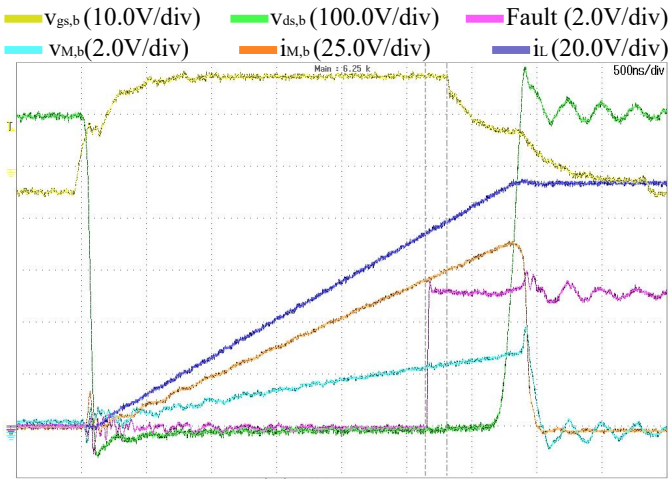


Fig. 10. Verification of the fault trip threshold in the bottom switch through double pulse test. The fault signal, in pink, goes high to 5V when the reconstructed current signal $v_{\mathrm{M,b}}$, in cyan, reaches the set threshold of 2 V, corresponding to a current flowing through the MOSFET, $i_{\mathrm{M,b}}$, in orange, of 70A. The SiC MOSFET gate driver voltage $V_{\mathrm{gs,b}}$ is indicated in yellow, the voltage across the MOSFET $V_{\mathrm{ds,b}}$ in green, and the current flowing through the inductor, $i_{\mathrm{L}}$ in blue.

### B. Reset switch of the over-current detection logic

In order to test the reset switch of the over-current detection logic, the TG5011 arbitrary function generator from TTi was connected at the output of the bottom switch Rogowski coil, while giving as output a 50 kHz square waveform with peak to peak amplitude of 100mV. This output emulates the flowing of a current ramp through the switch. Afterward, two gate pulses were released in the bottom switch, therefore activating the reset switch as well. In Fig. 9 it is possible to see that the reset switch, when turned on, successfully bring to zero the output of coil's integrator, i.e., the cyan curve goes to zero when the reset switch gate signal (in pink) goes high. The

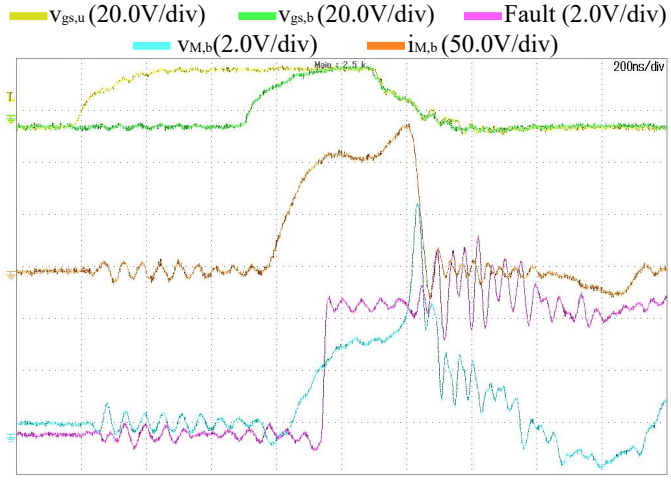


Fig. 11. Bridge shut-through/short-circuit test. Gate driver voltages, in yellow and green, MOSFET current, in orange, reconstructed current, in cyan, and SC turn off - fault signal in pink.

power MOSFET gate signal and the function generator output are represented by the yellow and green curve, respectively.

### C. Fault detection and fast turn off

The first step in the verification of the short circuit detection and fast turn off is the testing of the protection signal when the current threshold value is reached. In this context, the SiC MOSFET power module was tested through DPT, impressing a current ramp of 25A/$\mu$s, and fixing the fault trip threshold to 70A. In Fig. 10 it can be seen that when the device current reaches 70 A the fault signal goes high (in pink), and the gate driver turns off the power MOSFET with a soft turn-off action (see yellow curve), which subsequently causes the MOSFET to block the total applied DC voltage (in green). The detection and clearance time occurs within 700 ns. Note that in this figure the cyan curve is the reconstructed current flowing into the MOSFET, the orange curve is the current measured across the MOSFET through a commercial Rogowski, and the purple signal is the current flowing through the inductor of the DPT.

The missing step to verify the whole functionality of the design gate driver is to test the protection circuitry during a short circuit.

In Fig. 11 an example of short-circuit test is shown, where the shut-through of the half-bridge modules is performed. The upper MOSFET is initially turned on, its gate signal is shown with the yellow curve, then after some time the short-circuit is caused by the turn-on of the bottom MOSFET, i.e., its gate signal is shown with the green curve. The orange waveform is the measured MOSFET channel current, while the cyan curve is the analog circuit reconstructed current. The pink signal shows the output signal of the detection circuit when the over-current threshold is exceeded, which was set to a current of approximately 100 A. This fault signal pulls-down all gate signals of the bridge legs to a soft turn-off state, which will limit the rising of current across the MOSFETs. Hence, after

the fault detection all the MOSFETs are successfully turned off. This confirms that the reaction circuit operates according to the design specifications. Furthermore, the clearing time target set to be below 1$\mu$s was met successfully as the gate driver and protection circuit are able to detect and isolate the fault within approximately 400 ns.

## V. Conclusion

This paper has presented the design steps for a gate driver board with over-current protection based on Rogowski coils for a 62mm packaged 1.2kV half-bridge SiC MOSFET module. The target time for the short circuit clearing was set to be below 1$\mu$s, due to the low short circuit withstanding time and high current capability of the SiC devices. The experimental testing of the prototype, satisfied such target, with the gate driver detecting a over-current fault and safely turning off the switches within 700 ns. Furthermore, the paper discussed and analysed the implemented circuitry for the fast short circuit protection, describing and verifying its other functionalities, such as current reconstruction and reset switch.

## VI. Acknowledgment

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