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Chen, Minggang ; Zhang, Huajun; Fan, Qinwen

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A 155W −95.6 dB THD+N GaN-based Class-D Audio Amplifier With LC Filter Nonlinearity Compensation

Minggang Chen
National ASIC System Engineering & Research Center
Southeast University
Nanjing, China
chen_mg@seu.edu.cn

Huajun Zhang
Department of Microelectronics
Delft University of Technology
Delft, Netherlands
H.Zhang-13@tudelft.nl

Qinwen Fan
Department of Microelectronics
Delft University of Technology
Delft, Netherlands
q.fan@tudelft.nl

***Abstract*—Silicon MOSFETs-based medium-power (< 50W) Class-D amplifiers (CDAs) switching in the MHz range have gained popularity in recent years, which achieves better linearity thanks to a higher loop gain in the audio band while enabling the use of LC filters with higher cut-off frequencies. However, for high-power (>100 W) CDAs, such switching frequency and high load current could lead to significant power loss. Furthermore, in the presence of a large current and voltage applied to the load, the linearity of the system can quickly degrade due to LC filter component voltage/current dependency. Without any LC filter nonlinearity compensation technique, LC components with high voltage/current rating must be used to reach high system linearity, which are often expensive and bulky. This paper presents a CDA using a GaN-based output stage to achieve high switching frequency and good efficiency simultaneously, and an integrated controller implemented in a 180nm CMOS technology to compensate for the LC filter nonlinearity. Switching at 1.8 MHz, the CDA can deliver a maximum of 155W from a 50V supply into a 4Ω load with a peak efficiency of 91.7%. It achieves a peak THD+N of -95.6 dB (0.0017%) while allowing the use of cheaper and smaller nonlinear LC components.**

Keywords—Audio power amplifier, Class-D amplifier, GaN, THD, feedback-after-LC.

I. Introduction

High-power audio systems typically employ Class-D amplifiers (CDAs) to achieve high power efficiency, thereby significantly relaxing their cooling requirement compared to their Class-AB counterparts. Silicon MOSFETs-based CDAs [1-3] often exhibit limited switching speed, which results in a relatively poor THD (~ -80dB) and a relatively low PWM switching frequency (~350 kHz). The latter requires a relatively large LC filter to filter out the switching components and introduces extra distortion.

GaN-based CDAs [4-7] can offer higher switching frequency and, therefore, smaller LC filters without efficiency degradation. However, to achieve high linearity, expensive and bulky LC components can still be required. This issue is illustrated in Fig. 1, where a commonly-used feedback-before-LC architecture [1-4][8-10] and a feedback-after-LC architecture are shown. In the former case, the nonlinearity of the LC filter directly adds to the system, while the feedback-after-LC topology suppresses the nonlinearity of the LC filter with the outer loop gain and stabilizes the system with the inner loop [11-12]. A higher switching frequency is favorable since it helps to increase the outer loop gain [12], therefore achieving more LC filter nonlinearity suppression and allowing the use of smaller and cheaper nonlinear LC components.

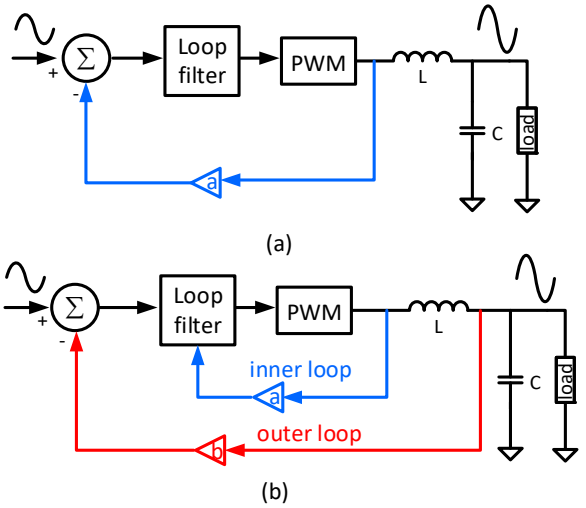

Fig. 1: Topologies of CDA (a) Feedback-before-LC; (b) Feedback-after-LC.

This paper presents a CDA employing an H-bridge output stage consisting of two GaN-based half-bridges with integrated gate drivers (EPC2152), and a fully integrated controller implemented in a 180nm CMOS technology, as shown in Fig. 2. The output stage employs BD modulation [13], and the PWM switching frequency is 1.8 MHz, enabling a control loop unity-gain frequency ~ 1MHz. The CMOS controller employs a dual-loop structure [12], in which the outer loop suppresses the nonlinearity of the LC filter and the inner loop stabilizes the CDA while suppressing the nonlinearity of the GaN-based output stage.

This paper is organized as follows. Section II introduces the adopted architecture. The implementation details and considerations are given in Section III. Section IV presents the experimental results, followed by a conclusion in Section V.

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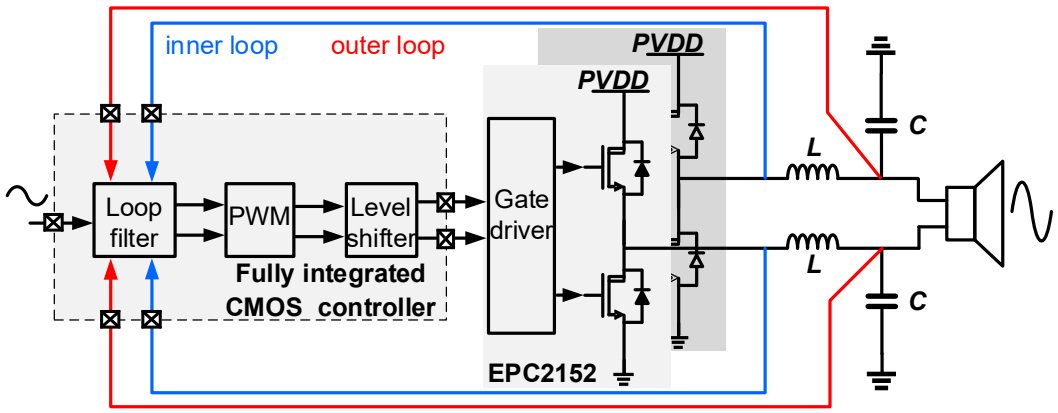


Fig. 2: Simplified block diagram of proposed CDA.

II. Feedback Loop Architecture

Fig. 3 illustrates the simplified dual-loop feedback architecture. An inner loop senses the switching node through a 1st-order low-pass filter (LPF), thus implementing a zero in its closed-loop response to compensate for the LC filter's phase shift and stabilize the system [12]. The entire inner loop behaves as a lead compensator. The outer loop, which senses the voltage across the load, is composed of 2 additional integrators (not shown for simplicity) to increase the audio-band loop gain that suppresses LC filter nonlinearity. To achieve high audio-band loop gain, the loop bandwidth is maximized, which is eventually limited by the PWM switching frequency [14].

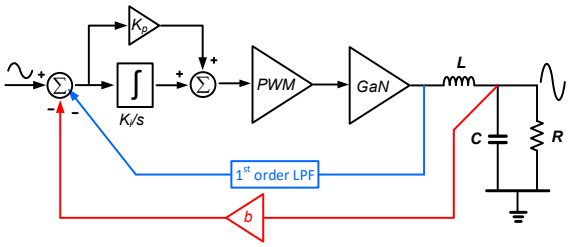


Fig 3: Simplified block diagram of the dual loop architecture of the proposed CDA.

III. Implementation Details and Considerations

Half-bridge GaN HEMTs with integrated gate drivers (EPC2152) are chosen for smaller parasitic inductance between the gate driver and the GaN HEMT, which is in principle beneficial for high switching frequency. A simplified circuit schematic of the fully integrated CMOS controller is shown in Fig. 4, which employs 3 fully-differential active-RC integrator stages (only shown in half for simplicity). Implemented in a 180nm CMOS technology, the operational amplifiers $A_{1,2,3}$ can only handle signals up to a low-voltage supply equal to 1.8V. Therefore, the feedback signals before and after the LC filter in the high-voltage domain must be attenuated when fed to the 1.8V controller. Although this can be done by properly selecting $R_{FB1\text{-}3}$, R_{IN}, etc., for flexibility and simplicity, resistor dividers $R_{s1\text{-}4}$ (as highlighted) are added such that for different GaN output stage supply voltages, only the resistor dividers need to be rescaled instead of many components in the loop filter. Unsilicided polysilicon resistors are employed for their low voltage coefficient and thus high linearity. Even so, a relatively large length (720 µm) is chosen to ensure high linearity, since the voltage coefficient is inversely proportional to the resistor length. Considering the area, power consumption, and linearity, R_{s2}=R_{s3}=30KΩ and R_{s1}=R_{s4}=10KΩ. $R_{FB1\text{-}3}$ are much higher than $R_{s1\text{-}4}$ to avoid the loading effect. The 1.8V PWM signals are first level shifted to the 5V domain and then transferred to the gate drivers of EPC2152.

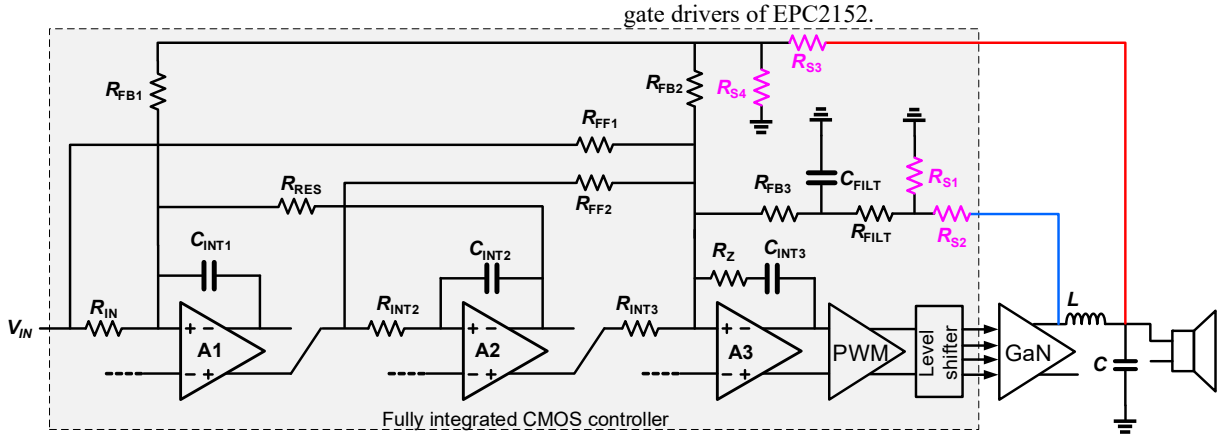


Fig. 4: Schematic of the fully integrated CMOS controller of the proposed CDA.

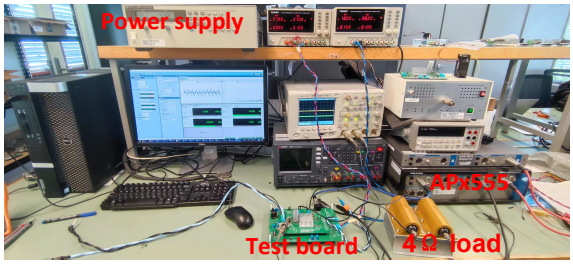
IV. Experimental Results

A. Prototype and the Key Parameters

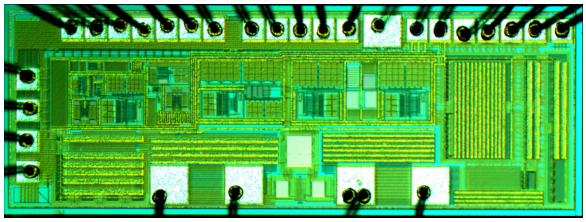
The key components information and prototype parameters are listed in Table I, where L_{filter} and C_{filter} are the LC filter component nominal values, V_{PVDD} is the GaN power stage supply, f_s is the PWM switching frequency, and V_{AVDD} is the CMOS controller supply. A typical 4Ω loudspeaker is used for the measurement (R_L=4Ω). The measurement setup is shown in Fig. 5 (a), and Fig. 5 (b) and Fig. 5 (c) are die photos of the feedback-after-LC controller and feedback-before-LC controller, respectively. An Audio Precision APx555 audio signal analyzer is used to provide the input and capture the output of the prototype.

Table I
KEY PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Quantity	Value	Unit	Remarks
GaN	--	--	EPC2512
L_{filter}	3.3u	H	--
C_{filter}	1u	F	--
R_L	4	Ω	--
V_{PVDD}	50	V	--
f_s	1.8M	Hz	--
V_{AVDD}	1.8	V	--



(a)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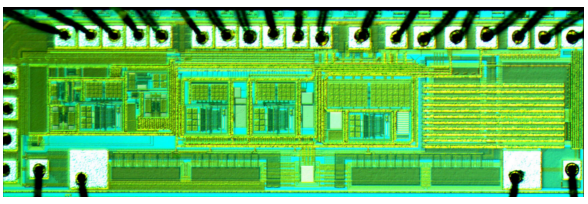
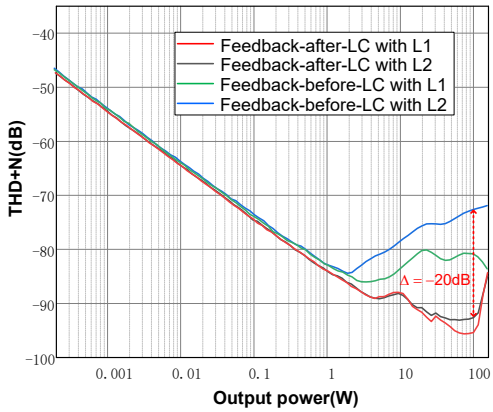

(c)

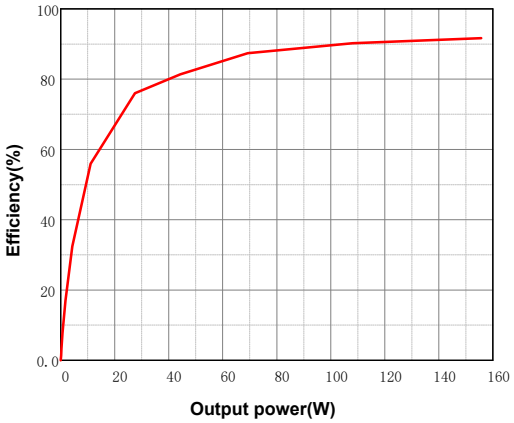
Fig. 5 Experimental prototype: (a) Testing setup; (b) Photo of the die of feedback-after-LC controller; (c) Photo of the die of feedback-before-LC controller.

Fig. 6(a) shows the THD+N of the feedback-after-LC CDA using two inductors with the same inductance but different saturation current, size, and cost: L1 (Würth Elektronik 7443640330): 100A saturation current, L*W*H=28.5mm*19.5mm*18.5mm, $9.97; L2 (Bourns SRP1265A-3R3M): 30A saturation current, L*W*H=13.5mm*12.5mm*6.4mm, $1.84. It can be seen that the THD+N is nearly unaffected (within 3 dB) by the inductors thanks to the feedback-after-LC topology.

To demonstrate the effectiveness of the feedback-after-LC topology, the two inductors L1 and L2 are also tested with a CDA using feedback-before-LC topology and the same GaN H-bridge and f_s. It is obvious that the THD+N is affected by the inductor nonlinearity, and, in both cases, worse than their feedback-after-LC counterparts with up to 20 dB of degradation. The proposed GaN-based CDA achieves a peak THD+N of -95.6 dB and a peak power efficiency of 91.7% when delivering an output power of 155W into a 4Ω load, as shown in Fig. 6 (b). When testing the efficiency, the input power is read from the power supplies, and the output power is read from APx555. Table II summarizes the key performances of the proposed CDA in comparison to other state-of-the-art GaN-based CDAs. The proposed CDA achieves at least 5.35 dB better THD+N than the other state-of-the-art GaN-based CDAs [7]. Moreover, it is the only GaN-based CDA that employs a feedback-after-LC topology and thus can tolerate a cheaper and smaller nonlinear LC filter without linearity degradation.



(a)



(b)

Fig. 6: (a) THD+N of the proposed CDA (f_{in}=1kHz); (b) Power efficiency (with L1).

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work	Infenon 2021 [4]	GaN System 2021 [5]	J. Sangid [6] WIPDA 2018	EPC 2017[7]
Control Topology	Feedback-after-LC	Feedback-before-LC	-	Feedback-before-LC	Feedback-before-LC
Supply (V)	50	±43	±32	60	±20~±30
Load resister (Ω)	4	4	4	4	8
f_s (kHz)	1800	500	-	140~450	-
Output Power (W)	155	225	300	40	150
Efficiency	91.7%	93%	96%	93.9%	96%
Peak THD+N @ 1kHz(dB)	-95.6	-86.02	-87.96	-82.16	-90.29
GaN	EPC2152	IGT40R070D1	GS61008P	EPC2301	EPC2016
CDA Topology	Full-bridge	Half-bridge	-	Half-bridge	Full-bridge

CONCLUSION AND FUTURE WORK

This paper presents a GaN-based CDA with feedback-after-LC topology. It is shown that the LC filter nonlinearity is effectively suppressed. Therefore, smaller and cheaper LC components can be used. The GaN device EPC2152 is chosen to facilitate high switching frequency and to verify the control loop topology. However, due to the relatively high parasitic capacitance (C_{OSS}), switching loss dominates the total power loss. To achieve higher peak efficiency, a GaN device with lower parasitic capacitance but higher R_{on} would be more favorable. The PCB parasitic capacitance at the switching node can be further minimized to improve efficiency. Moreover, the maximum output power is restricted by the minimum pulse width of ~20 ns. This can be improved by designing a gate driver that supports a narrower pulse width. Lastly, more inductors with even worse linearity can be tested to demonstrate the effectiveness of the feedback-after-LC control loop.

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