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Karmakar, Shoubhik; Berkhout, Marco; Makinwa, Kofi A.A.; Fan, Qinwen

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A −91 dB THD+N, Class-D Piezoelectric Speaker Driver Using Dual Voltage/Current Feedback for Resistor-Less *LC* Resonance Damping

Shoubhik Karmakar, *Member, IEEE*, Marco Berkhout, *Member, IEEE*, Kofi A. A. Makinwa, *Fellow, IEEE*, and Qinwen Fan, *Member, IEEE*

***Abstract*— This article presents a Class-D audio amplifier for capacitive piezoelectric speaker loads. Employing a dual voltage feedback (VFB)/current feedback (CFB) topology, the amplifier is capable of damping *LC* resonance without using an external damping resistor, therefore reducing system power consumption, cost, and size. Additional power savings are achieved by using a push–pull (PP)-modulated output stage. To mitigate linearity degradation due to the mismatch of the feedback resistors, they are dynamically matched by employing choppers. The prototype, taped out in a BCD 180-nm process, can drive up to 4 μF load with a peak current of 4.4 A while achieving an idle power consumption of 122 mW and a peak THD+N of −91 dB.**

***Index Terms*— Audio power amplifier, chopping, class-D amplifier, current feedback (CFB), piezoelectric speakers, push–pull (PP) modulation, resistor-less *LC* damping.**

I. Introduction

DUE to their compact size and improving audio quality, piezoelectric speakers are gaining popularity in applications constrained to a thin form factor, such as tablet computers and flat-screen TVs, [1]. However, their highly capacitive impedance makes them challenging to drive. Fig. 1 shows some of the existing approaches used to drive piezoelectric speakers with conventional Class-AB or Class-D amplifiers. To prevent amplifier instability and excessive transient currents, an external power resistor may be connected in series with the load [see Fig. 1(a)]. However, the power consumption of this resistor and the inefficiency of Class-AB amplifiers makes this approach quite power hungry, and therefore, this approach is typically limited to relatively small loads (<1.5 μF) [2], [3]. Class-D amplifiers can deliver large load currents with much higher efficiency. However, a series inductor is then required to limit the high-frequency currents generated by the amplifier's switching output stage. In addition, an external resistor of around 5–10 Ω is still required [see Fig. 1(b)] to damp the resulting *LC* resonant circuit, which would otherwise draw excessive currents when excited by large out-of-band signals, for example, during clipping events [4], [5].

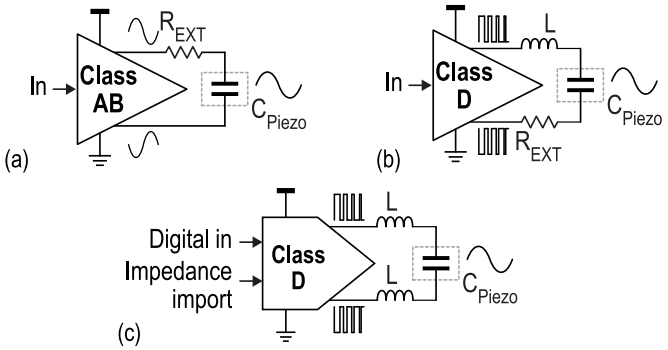

Fig. 1. Existing approaches to drive a capacitive piezoelectric speaker. (a) Class-AB amp. + ext. resistor. (b) Class-D amp. + ext. resistor. (c) Class-D amp. + calibration.

To reduce system power consumption, cost, and size, the external damping resistor should be eliminated. In [6], a digital-input Class-D piezoelectric speaker driver [see Fig. 1(c)] relies on foreground calibration to modify the input signal using *a priori* information about *LC* filter impedance. This prevents current overshoots but increases system complexity. Instead of a damping resistor, a current feedback (CFB) loop can be used to damp *LC* resonance [7], [8]. In prior art, however, a current transformer is required to sense the amplifier's output current, which increases system cost and militates against a fully integrated CMOS solution.

This article, an extension of [9], presents a fully integrated Class-D piezoelectric speaker driver that achieves resistor-less damping by employing both voltage and CFB. With the help of a single external inductor, it can drive a 4 μF load capacitance with a peak current of 4.4 A while dissipating low idle power (122 mW) and achieving a peak high THD+N of −91.1 dB across a wide range of output amplitudes ($10.2V_{rms}$).

This article is organized as follows. Section II introduces the proposed system-level architecture and describes its benefits and challenges. Section III describes the circuit implementation. This is followed by measurement results in Section IV, and finally, conclusions are drawn in Section V.

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Shoubhik Karmakar, Kofi A. A. Makinwa, and Qinwen Fan are with the Department of Microelectronics, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: q.fan@tudelft.nl).

Marco Berkhout is with Goodix Technologies, 6537 TL Nijmegen, The Netherlands.

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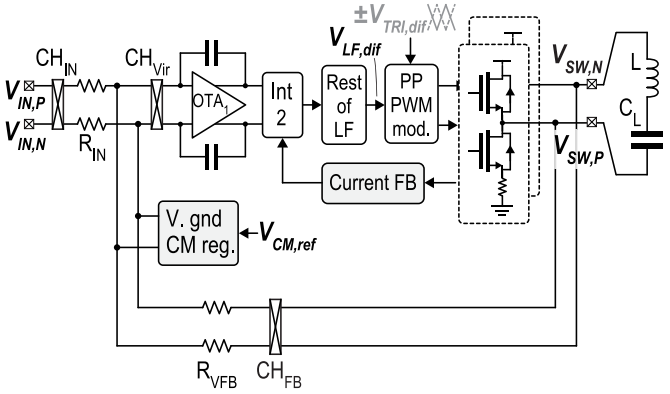

Fig. 2. Block diagram of the resistor-less piezoelectric speaker driver.

II. Proposed Resistor-Less Architecture

An overview of the proposed driver architecture is shown in Fig. 2. It employs a conventional voltage feedback (VFB) path around the loop filter and a separate CFB path to its second integrator. With the help of small on-chip current-sensing resistors, which, for a given damping factor, dissipate much less power than an external damping resistor, this path acts to damp *LC* resonance. A push–pull (PP)-modulated output stage is employed to further reduce the driver's power consumption at low signal amplitudes. However, this leads to a large common-mode (CM) swing at the input of the first integrator, whose finite CMRR would then lead to distortion. In this work, this is mitigated by employing chopping and a CM regulator at the virtual ground of the first integrator.

A. Dual VFB and CFB

To illustrate how the CFB path helps damp *LC* resonance, a simplified block diagram of a Class-D amplifier with a dual VFB/CFB network is shown in Fig. 3(a). It consists of a loop filter $H(s)$, a PWM modulator, and an output stage loaded by an undamped *LC* filter with a cutoff frequency of f_{LC}. The VFB path has a normalized feedback factor of unity ($\beta_{\text{VFB,norm}} = 1$), and the CFB path senses the load current (I_{Load}) using a small on-chip sense resistor (R_S) and amplifies the resulting voltage by a gain factor K. The output of the CFB path (V_{CFB}) is given by

$$V_{\text{CFB}} = K \cdot (I_{\text{Load}} R_S). \tag{1}$$

Since $I_{\text{Load}} = V_{\text{SW}}/Z_{\text{Load}}$, where V_{SW} and Z_{Load} denote the switching node output voltage and the load impedance seen from V_{SW}, respectively, a V/V feedback factor (β_{CFB}) for the CFB path can be defined as

$$\beta_{\text{CFB}} = V_{\text{CFB}}/V_{\text{SW}} = R_S \cdot K/Z_{\text{Load}}. \tag{2}$$

As shown in Fig. 3(b), the magnitude of β_{CFB} peaks at f_{LC} due to the presence of Z_{Load}, which is the undamped series combination of L and C_L. Setting an appropriate gain K allows $|\beta_{\text{CFB}}|$ to become larger than $|\beta_{\text{VFB}}|$ around f_{LC}, thereby creating a peak in the overall feedback factor $\beta_{\text{Total}} = \beta_{\text{VFB}} + \beta_{\text{CFB}}$. This effectively translates into a notch

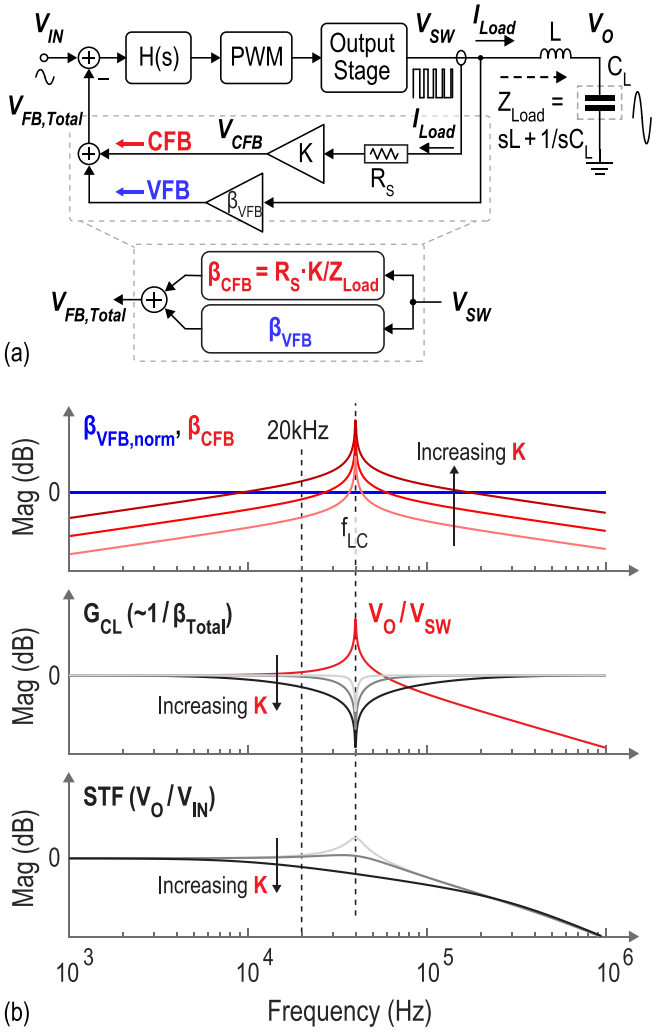

Fig. 3. (a) Simplified block diagram of dual VFB/CFB topology. (b) Magnitude response illustrating resistor-less *LC* damping.

in the closed-loop gain of the Class-D amplifier (G_{CL}), which can be approximated as

$$G_{\text{CL}} = V_{\text{SW}}/V_{\text{IN}} \sim 1/\beta_{\text{Total}}. \tag{3}$$

Together, the cascade of G_{CL} and the *LC* filter transfer function (V_O/V_{SW}) results in a damped signal transfer function (STF).

Although a larger gain K can provide greater damping, it will also reduce the flatness of the STF and increase the impact of any non-linearity in the CFB path on the linearity of the overall feedback factor. Increasing f_{LC} further allows for more flexibility in the choice of K for adequate damping while also ensuring that the VFB path dominates the STF in the audio band (20 Hz–20 kHz). At frequencies above f_{LC}, the VFB path dominates again and determines the Class-D amplifier's unity-gain frequency and stability.

B. PP Modulation and Load Current Sensing

An H-bridge output stage is used to drive high current through a bridge-tied load (BTL), which in this case is the series combination of a single inductor L and the load

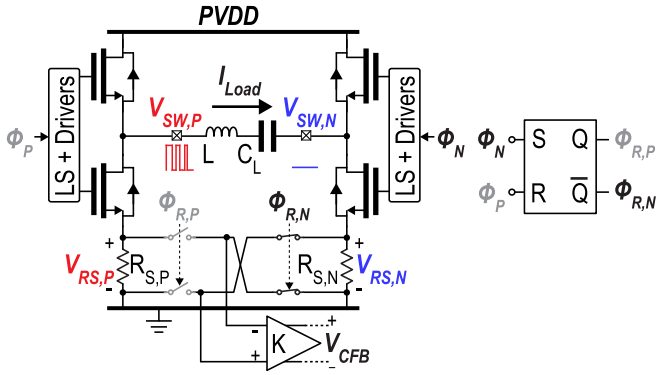

Fig. 4. Simplified schematic of the PP-modulated output stage with low-side sense resistors and readout amp, generation of controls signals of the CFB network switches.

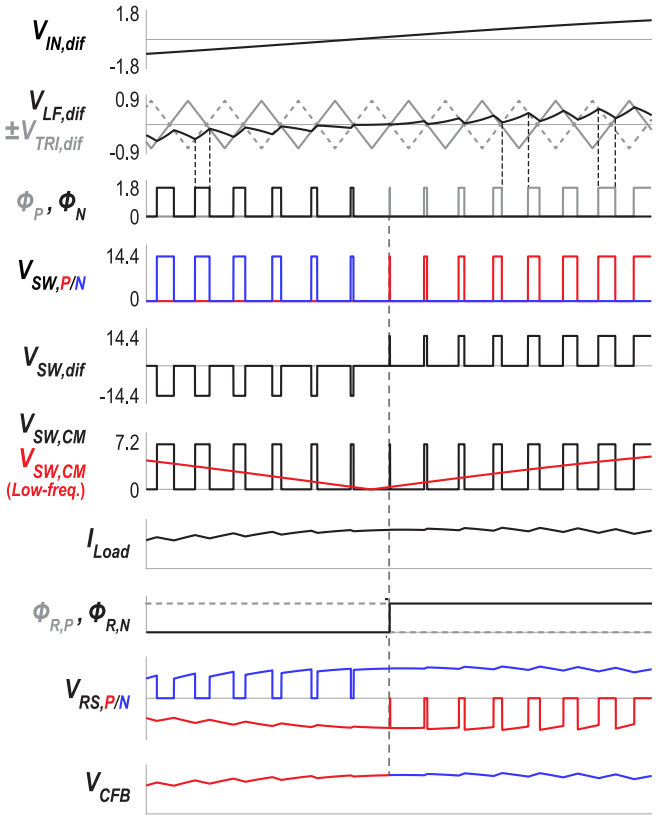

Fig. 5. Time-domain waveforms illustrating the PP modulation scheme and the operation of the CFB readout network.

capacitor C_L, as shown in Fig. 4. To reduce the power consumption of this output stage, a PP modulation scheme [10], [11], [12], [13] is employed. In such a scheme, also known as ternary modulation, BD modulation with low CM, and half-side switching, only half of the H-bridge switches, while the other half remains grounded, as illustrated by the timing waveforms in Fig. 5. The required PWM signals are generated by comparing the differential output of the loop filter ($V_{\mathrm{LF,dif}}$ in Fig. 2), with a pair of 180° phase-shifted triangular carriers ($\pm V_{\mathrm{TRI,dif}}$). When $V_{\mathrm{LF,dif}}$ is lower than both $\pm V_{\mathrm{TRI,dif}}$, $V_{\mathrm{SW},P} = 0$ and $V_{\mathrm{SW},N} = \mathrm{PVDD}$ (=14.4 V); when $V_{\mathrm{LF,dif}}$ is higher than both $\pm V_{\mathrm{TRI,dif}}$, $V_{\mathrm{SW},P} = \mathrm{PVDD}$ and $V_{\mathrm{SW},N} = 0$; and $V_{\mathrm{SW},P/N} = 0$ otherwise. The single-sided switching cuts down the gate-charging losses of the output stage by half in comparison to conventional AD modulation [13]. Furthermore, the differential switching output ($V_{\mathrm{SW,dif}} = V_{\mathrm{SW},P} - V_{\mathrm{SW},N}$) now switches across three levels (0, ±PVDD), reducing the step size by half in comparison to AD modulation, thereby reducing the ripple current and the associated losses, especially during idle-channel operation [14]. Unlike other multilevel output stages [14], [15], [16], [17] that also enable a reduction in ripple current, PP modulation does not require the use of additional large power switches, supplies, and/or off-chip components. However, the single-sided switching of $V_{\mathrm{SW},P/N}$ also results in a significant CM switching output $V_{\mathrm{SW,CM}} = (V_{\mathrm{SW},P} + V_{\mathrm{SW},N})/2$, the consequences of which are discussed in Section II-D.

To sense the load current, on-chip sense resistors are preferred over external components due to their lower cost. Ideally, such resistors would be inserted in series with the outputs of the H-bridge ($V_{\mathrm{SW},P/N}$) to get a direct measure of the load current-I_{Load}. However, due to the PWM switching activity at these nodes, the associated readout amplifiers would then have to handle large high-frequency CM signals. Low-side current sensing, with sense resistors $R_{S,P/N}$ positioned below the low-side output switches (see Fig. 4), can also be employed to indirectly sense the load current [18], [19]. However, the BD-modulated output stages used in these designs do not facilitate linear, continuous-time current sensing via low-side resistors, due to the overlapping OFF-state of both low-side switches every PWM cycle, along with the presence of other switching non-idealities. In this work, however, since the sensed current is fed back to the signal path, a continuous-time current-sensing scheme with adequate linearity is required. PP modulation is beneficial in this regard, since depending on the polarity of the input, one of either half of the H-bridge avoids high-frequency PWM switching and instead remains grounded. As shown in Fig. 5, when $V_{\mathrm{IN,dif}}$ is negative, $V_{\mathrm{SW},P}$ remains grounded, while $V_{\mathrm{SW},N}$ is switching, and therefore, I_{Load} can be sensed by connecting the readout amplifier across $R_{S,P}$. When the polarity of the audio signal changes and $V_{\mathrm{SW},P}$ starts switching, the read-out amplifier is connected to $R_{S,N}$, thereby providing a quasi-continuous readout of I_{Load}. The control signals of the CFB switches ($\phi_{R,P/N}$) are generated in the low-voltage (LV) domain by an SR-latch that is triggered by the LV control signals of the output stage ($\phi_{P/N}$), avoiding the need for a separate zero-crossing detector. The propagation delay (t_{delay}) between $\phi_{P/N}$ and $V_{\mathrm{SW},P/N}$, due to peripheral blocks in the output stage, such as level shifters and the gate drivers (see Fig. 4), ensures that the CFB switches always a transition between $R_{S,P/N}$ when both H-bridge halves are grounded. Furthermore, the transition time is less than 1 ns, thereby minimizing any current-sensing glitches. Low-side current sensing further relaxes the input CM swing requirements of the readout amplifier (∼±100 mV around 0 V).

However, both the CFB and VFB paths introduce distortion, and solutions to address this issue are discussed in the following.

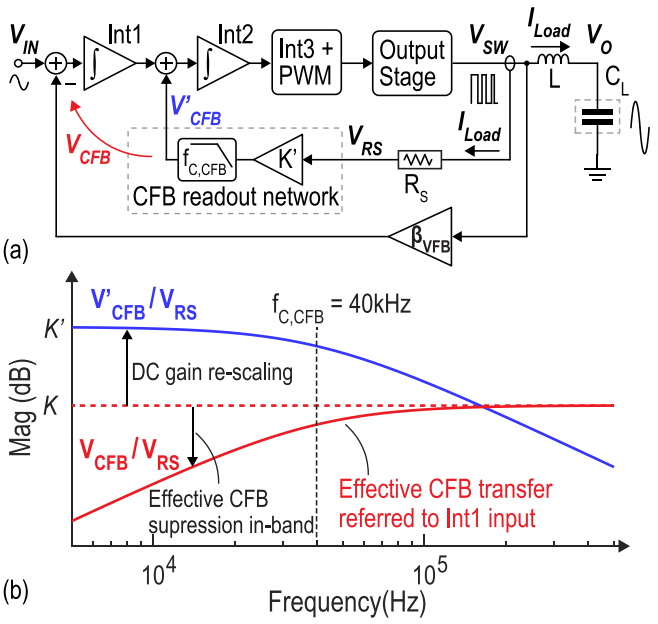

Fig. 6. (a) Simplified block diagram illustrating the CFB network and nonideality suppression. (b) Magnitude response of CFB to Int2 and referred to Int1.

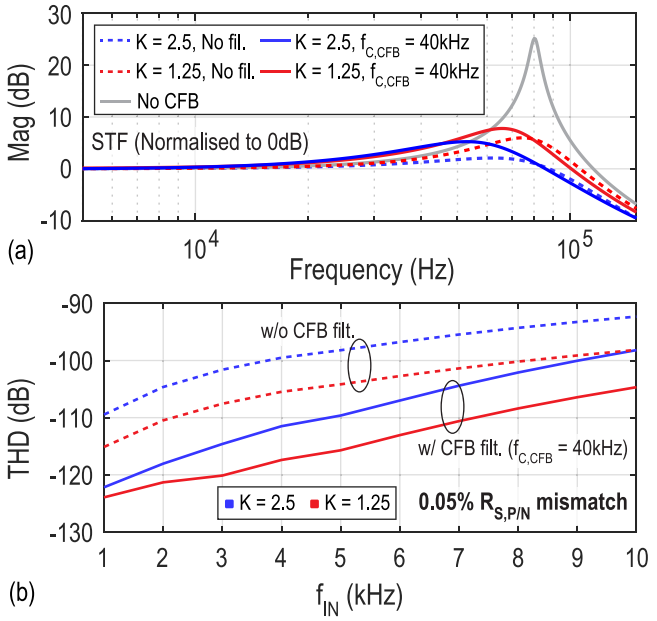

Fig. 7. Simulation results illustrating (a) effect of effective CFB gain-K on the LC peaking in the STF (normalized to 0 dB) and (b) improvement in THD with audio band CFB filtering.

C. CFB Path Nonlinearity Suppression

Since the load current readout is now a quasi-continuous measure of two different sense resistor voltages, the overall linearity of the CFB path is limited by their relative matching. Furthermore, the combination of self-heating and their intrinsic temperature dependence causes the voltage drop across the current sensing resistors to be a nonlinear function of load current amplitude and frequency. To avoid complicated calibration and trimming techniques to suppress these errors, a relatively straightforward approach is proposed.

As the CFB path is primarily required to damp the LC resonance at f_{LC}, its gain in the audio band can be reduced. This, in turn, will mitigate the effect of its non-idealities in this band. This is achieved by closing the CFB loop around Int2, as shown in Fig. 6(a) with an additional low-pass (LP) filter with a cutoff frequency at $f_{C,\mathrm{CFB}}$ and rescaling the dc gain K to

$$K' = K \cdot \left(f_{\mathrm{UG,Int1}}/f_{C,\mathrm{CFB}}\right) \tag{4}$$

where $f_{\mathrm{UG,Int1}}$ is the unity-gain frequency of the first integrator. The overall s-domain transfer function of the CFB readout network is given by

$$\frac{V'_{\mathrm{CFB}}}{V_{\mathrm{RS}}} = K' \cdot \left(\frac{1}{1+{}^{s}/_{\omega_{C,\mathrm{CFB}}}}\right) \tag{5}$$

where ω terms correspond to frequencies in rad/s. Referred to the first integrator's input, the transfer function above is given by

$$\frac{V_{\mathrm{CFB}}}{V_{\mathrm{RS}}} = \left(\frac{V'_{\mathrm{CFB}}}{V_{\mathrm{RS}}}\right) \Big/ \left(\frac{\omega_{\mathrm{UG,Int1}}}{s}\right) = K \cdot \left(\frac{{}^{s}/_{\omega_{C,\mathrm{CFB}}}}{1+{}^{s}/_{\omega_{C,\mathrm{CFB}}}}\right). \tag{6}$$

This is a high-pass filter, which ensures that CFB non-idealities are suppressed for input frequencies less than $f_{C,\mathrm{CFB}}$, as shown in Fig. 6(b). Fig. 7(a) shows the effect of the CFB gain (K) on LC peaking suppression when $f_{LC} = 80$ kHz, which is an often used cut-off frequency in Class-D amplifiers switching at MHz frequencies [14], [20], [21] ($\beta_{\mathrm{VFB}} = 1/8$, $C_L = 4\ \mu$F, and $R_{S,P/N} = 20\ \mathrm{m}\Omega$). It can be seen that, although the audio band filtering of K slightly reduces damping efficacy, it can be recovered by increasing K. Fig. 7(b) shows the linearity of an ideal amplifier in the presence of a 0.05% mismatch between $R_{S,P/N}$, which can be achieved by careful layout and proper sizing. The two graphs demonstrate that, to attain certain damping in the presence of CFB path nonlinearity, it is better to go for a larger K, e.g., 2.5 with audio band filtering, than a smaller K, e.g., 1.25 without filtering.

D. VFB Path Nonlinearity Suppression

Although PP modulation is beneficial for low power consumption, the single-sided switching of $V_{\mathrm{SW},P/N}$ creates a significant amount of CM signal ($V_{\mathrm{SW,CM}}$) at the output. As shown in Fig. 5, $V_{\mathrm{SW,CM}}$ not only comprises high-frequency components at the PWM switching frequency (f_{SW}) and its harmonics but also distorted low-frequency components in the audio band. Therefore, any mismatch in the first integrator's input stage or the feedback resistor pairs (R_{IN} and R_{VFB}) would compromise its CMRR and cause the distorted audio band CM content to leak into the differential-mode (DM) feedback path and degrade THD. In a conventional AD/BD-modulated output stage, since the low-frequency component of $V_{\mathrm{SW,CM}}$ is ideally just a dc signal, THD and PSRR degradation due to CM–DM leakage within the audio band can be mitigated by employing a CM regulation loop [22]. However, with PP

modulation, due to the inherent non-linearity, it creates in low-frequency components of $V_{SW,CM}$, and it cannot simply be regulated to a dc value. Therefore, in this work, to mitigate the adverse effects of CM–DM leakage, choppers are employed to dynamically match the R_{IN} and R_{VFB} pairs. However, to avoid intermodulation between PWM and chopping, the chopping frequency f_{CH} must be carefully chosen.

A simplified block diagram of the first integrator with choppers around $R_{IN,1/2}/R_{VFB,1/2}$ is shown in Fig. 8(a). Due to the mismatch between $R_{VFB,1/2}$, a distorted DM feedback error current ($I_{CM\text{-}DM,err}$) is created by the nonlinear CM output voltage $V_{SW,CM}$. Since $V_{SW,CM}$, and therefore $I_{CM\text{-}DM,err}$, has content both in the audio band and around f_{SW} (and its harmonics), f_{CH} must be chosen to avoid modulating components of $I_{CM\text{-}DM,err}$ into the audio band. The frequency-domain activity is shown in Fig. 8(b). Ideally, the DM switching output of the Class-D amplifier ($V_{SW,dif}$) only consists of a linear audio signal (blue) and PWM switching sidebands at f_{SW} (green). If this is chopped at an odd subharmonic of f_{SW} (e.g., $f_{CH} = f_{SW}/3$), the upmodulated audio feedback current ($I_{Aud,dif}$) overlaps with error tones of $I_{CM,DM,err}$ (red) at f_{SW} (circled). The latter will thus be modulated to the audio band by the chopper at the integrator's virtual ground (CH_{Vir}). In comparison to chopping an AD-modulated output stage [23], where both $V_{SW,CM}$ and $I_{CM\text{-}DM,err}$ have negligible content in the audio band, the distortion due to $I_{CM\text{-}DM,err}$ foldback in PP modulation can be significant. This is avoided by chopping at an even subharmonic of f_{SW} (e.g., $f_{CH} = f_{SW}/4$), as the resulting foldback is now outside the audio band. Furthermore, this choice ensures that the chopping transitions always occur when both $V_{SW,P/N}$ are grounded as shown in Fig. 8(c), minimizing the output-stage-state-dependent delays and glitches of the high-voltage (HV) feedback choppers [23]. To avoid the adverse effects of a high chopping frequency, such as clock feed-through and charge injection at the first integrator's virtual ground, while also maintaining an adequate margin from the audio band edge, f_{CH} was set to 125 kHz ($=f_{SW}/16$) in this work.

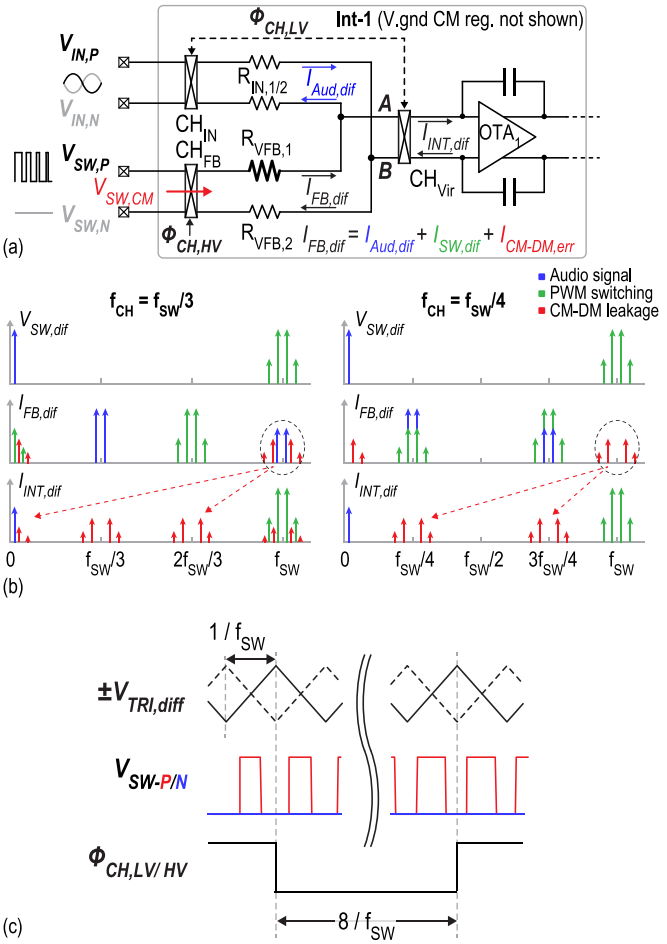

Fig. 8. (a) Simplified block diagram of the first int. and associated signals. (b) Frequency-domain behavior of chopping in the presence of mismatch. (c) Chopping phases with respect to switching nodes.

III. Circuit Implementation

Fig. 9 shows a simplified top-level schematic of the proposed Class-D amplifier. The output stage is powered from PVDD (14.4 V) and switches at $f_{SW} = 2$ MHz. Except for the output stage, the feedback chopper (CH_{FB}), and the input switches of the CFB network, all other blocks operate at LV and are realized using area- and power-efficient 1.8-V devices. They include a fully differential third-order loop filter, a virtual ground CM regulator for Int1, the CFB network feeding into Int2, and a PP PWM modulator that generates the control signals for the HV output stage and the CFB interface switches.

A. Loop Filter and Int-1 Virtual Ground CM Regulator

A third-order loop filter is realized with a cascade of active-*RC* integrators in a feed-forward (CIFF) configuration, to create high loop gain around the output stage. The unity-gain frequency of the loop-$f_{UG,Loop}$ is 570 kHz, which satisfies the stability criteria ($f_{UG,Loop} < f_{SW}/\pi$) [24]. At this frequency, the CFB path gain is significantly lower than the VFB path gain, allowing the Class-D amplifier to handle a sufficiently high f_{LC} (~200 kHz) without compromising on loop stability (phase margin > 50°) and thereby making it robust to f_{LC} spread. A closed-loop gain of 8× is set by R_{IN} and R_{VFB}. High-density MIM capacitors are used to realize the *RC* time constants. They are made 2-bit trimmable to compensate for the *RC* process spread.

As shown in Fig. 10, the single-sided switching of $V_{SW,P/N}$ also creates a non-linear CM signal at the first integrator's virtual ground $V_{Vir,CM} = (V_{Vir+} + V_{Vir-})/2$, which can swing from 0.8 to 1.6 V. Any mismatch in the integrating capacitors (C_{INT1}) or a finite CMRR in OTA_1 would therefore also degrade THD due to CM–DM leakage induced non-linear currents in C_{INT1}. To relax the matching constraints on C_{INT1} and improve the CMRR of OTA_1, a separate virtual ground CM regulator is used, as shown in Fig. 9. It detects $V_{Vir,CM}$ through $R_{CM,in}$ and regulates the voltage to a fixed dc value-V_{CMref} (~1.1 V) by sinking/sourcing currents through $R_{CM,out}$. This also reduces the input CM swing requirements on OTA_1 drastically. To relax the matching constraints of the $R_{CM,in}$ and $R_{CM,out}$ pairs, they are also dynamically matched by

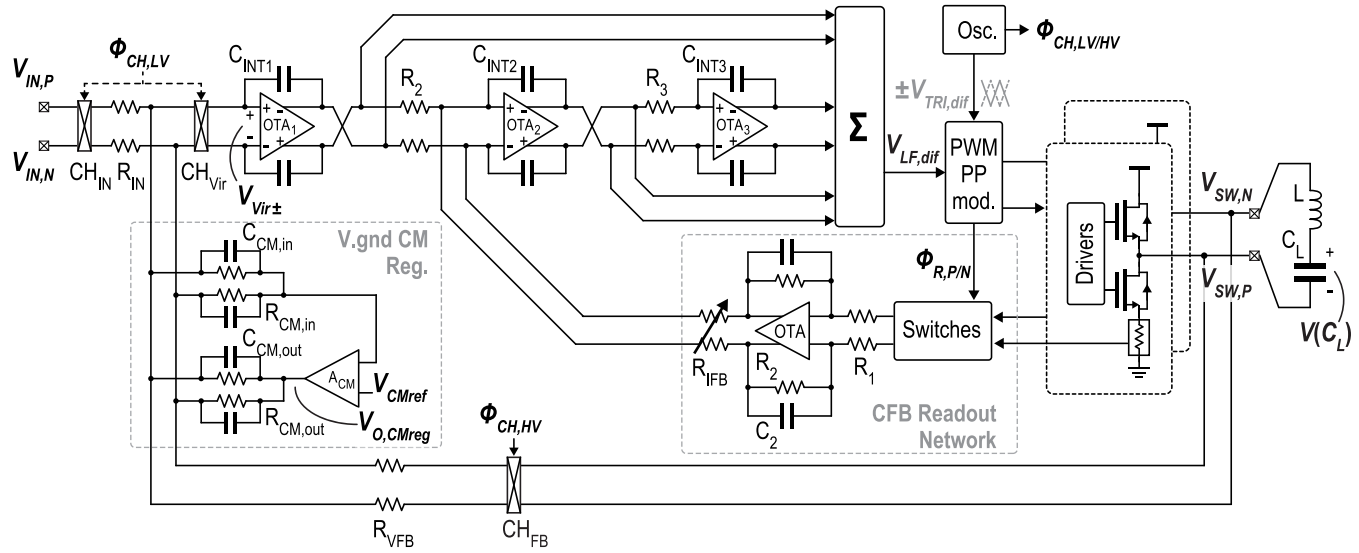

Fig. 9. Schematic of the loop filter and CFB readout network.

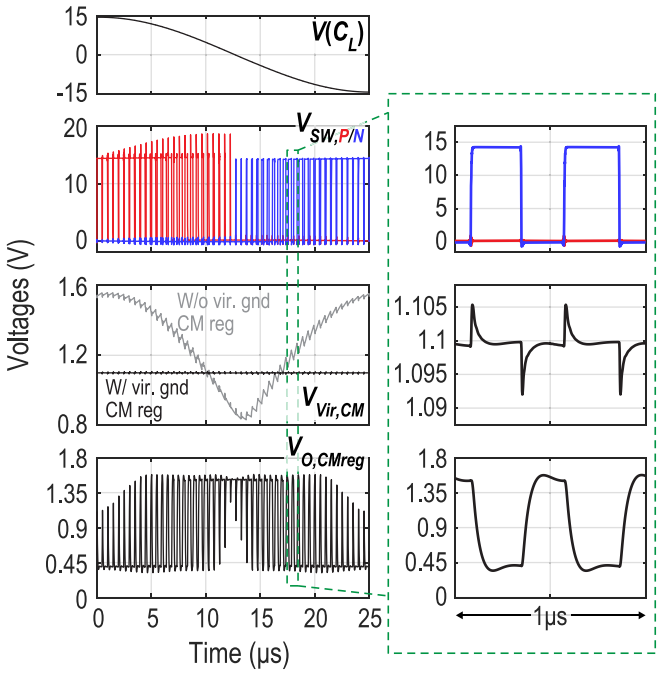

Fig. 10. Effect of the single-sided switching on the first integrator's virtual ground CM voltage with and without the virtual ground CM regulator.

connecting them before CH_{Vir}. Capacitor pairs $C_{CM,in}$ and $C_{CM,out}$ enable a fast transient response.

The noise of the Class-D amplifier is mainly dominated by R_{IN} (20 kΩ), the noise of OTA_1, and $R_{CM,out}$. While the contribution of $R_{CM,out}$ can be reduced by increasing its resistance, the swing required ($V_{O,CMreg}$ in Figs. 9 and 10) at the output of A_{CM} would increase. Therefore, as a tradeoff between noise and swing, $R_{CM,out}$ is set to 25 kΩ.

B. Choice of RS and CFB Readout Network

In this work, diffusion resistors ($R_{S,P/N} \sim 20$ mΩ) are used to sense the load current, and they are sized to satisfy area constraints and current density limits while ensuring adequate voltage linearity across the expected range of load currents. Compared to diffusion resistors, metal resistors have significantly lower sheet resistance and better voltage linearity. However, their temperature dependence is much larger, leading to greater CFB non-linearity due to self-heating. Conversely, despite their lower temperature dependence, poly-silicon resistors were not used due to their larger sheet resistance.

The choice of effective CFB gain-K is a tradeoff between the non-linearity of the CFB path and the amount of damping required, as discussed in Fig. 7. As a compromise between the two, K is programmable between 1.25 and 2.5, which can then limit the LC damping to ∼4 to 8 dB for a 4 μF capacitive load. Fig. 9 shows the implementation of the CFB path around Int2 using an active-RC filter. The dc-scaled passband gain-K' from (5) is set by R_2, R_1, and R_{IFB}, while the LP filter cutoff at 40 kHz is set by R_2 and C_2. K' is made programmable by adjusting the feedback current into the second integrator with R_{IFB}. A two-stage OTA, shown in Fig. 11, is used to achieve a high in-band gain and linearity while satisfying the input and output swing requirements. It comprises a conventional PMOS input folded-cascode input stage, to handle the low CM input, along with a class-A biased output stage that provides adequate output swing. A feed-forward compensation network, realized by capacitively coupling the inputs to the inputs of the second stage, ensures stability [25].

C. Chopper Network

The HV chopper (CH_{FB}) uses 20-V LDMOS devices to handle the 14.4-V signal swings at $V_{SW,P/N}$ [23]. The design of CH_{FB}, and those of the peripheral circuits required to drive the HV switches, is adopted from [23]. The choppers at the input (CH_{IN}) and virtual ground (CH_{Vir}) use 1.8-V devices. Both of them are bootstrapped to achieve adequate linearity and avoid the use of unnecessarily large switches, which would then cause significant charge injection and clock feed-through [23].

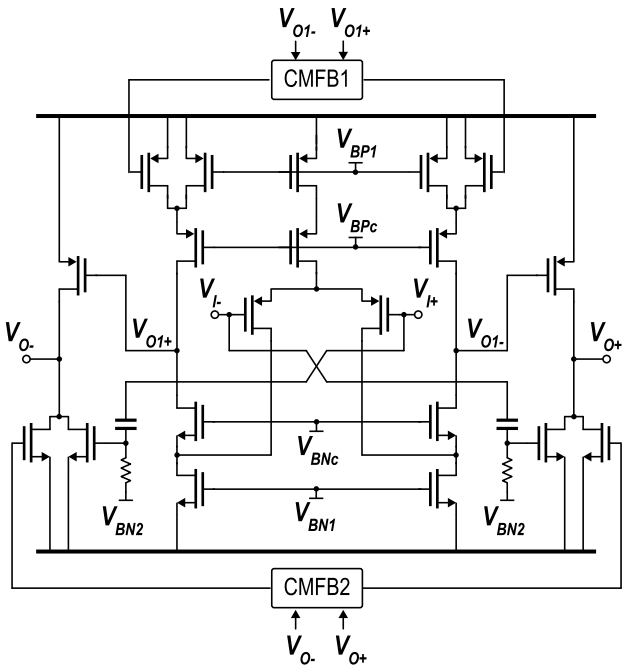

Fig. 11. Schematic of the two-stage OTA used in the CFB network.

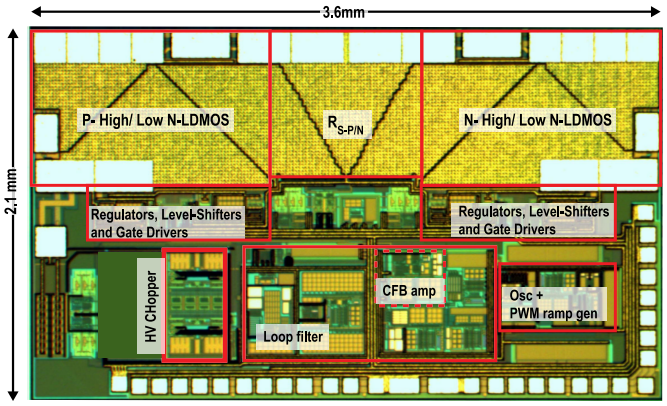

Fig. 12. Die micrograph of the prototype IC.

IV. Measurement Results

A prototype resistor-less Class-D piezoelectric speaker driver was fabricated in a 180-nm BCD process Fig. 12 shows a die micrograph of the prototype, which occupies 7 mm^2. It is powered from 14.4/1.8 V (PVDD/AVDD) supplies and drives a 4 μF capacitor in series with a 1.1-μH inductor ($f_{LC} \sim 75$ kHz). During the idle-channel operation, the amplifier consumes 122.4/9 mW from PVDD/AVDD. Of the total power consumption, the additional sense resistors and CFB readout network consume <1% and ~0.6%, respectively.

All audio measurements were performed using an Audio Precision APX-555 in combination with an AES17 filter. Fig. 13 shows the efficacy of the dual VFB/CFB topology in damping the *LC* resonance. An impedance analyzer was used to extract the undamped *LC* transfer on the test PCB itself. Two CFB gain settings, corresponding to effective CFB gains of $K = 1.25$ and 2.5, show that the STF peaking can be suppressed by 20 and 22 dB, respectively.

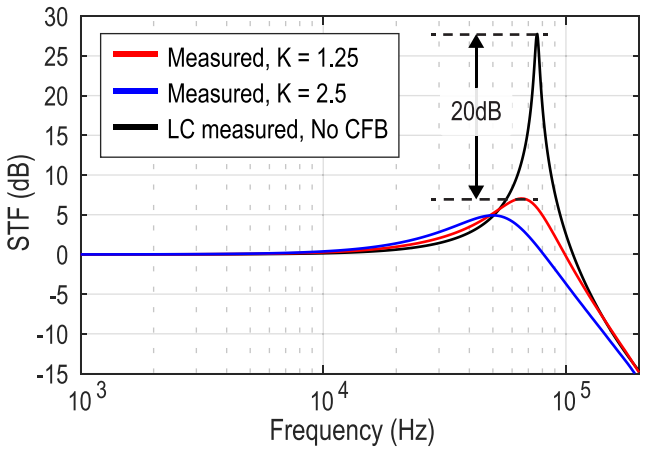

Fig. 13. Effect of CFB on the *LC* peaking in the STF (normalized to 0 dB).

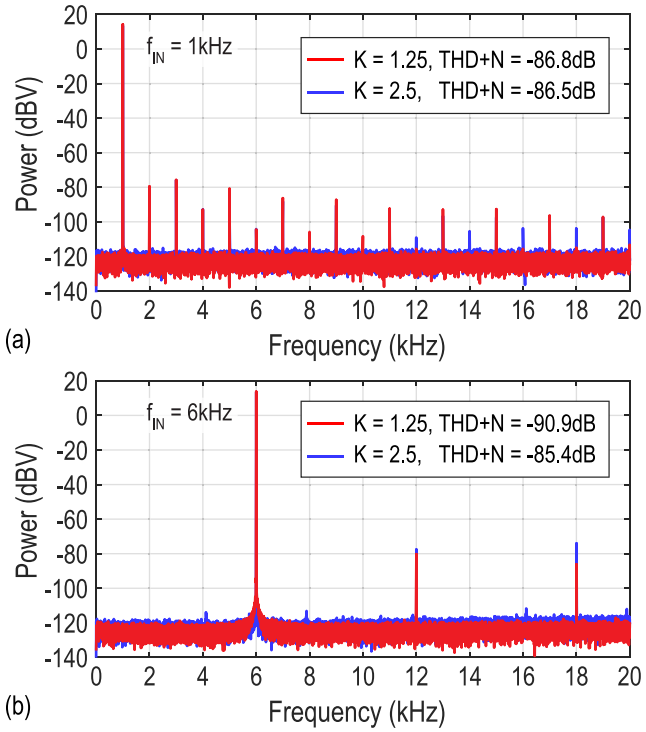

Fig. 14. FFT at $V_O = 5V_{\text{rms}}$ for (a) $f_{\text{IN}} = 1$ kHz and (b) $f_{\text{IN}} = 6$ kHz.

Fig. 14 shows the measured output spectrum when driving the 4 μF load with a $5V_{\text{rms}}$ signal for $K = 1.25$ and 2.5. For an input frequency of 1 kHz, the THD+N is $-86.8/-86.5$ dB for $K = 1.25/2.5$. Due to the smaller load current at this frequency, the linearity is primarily limited by the HV choppers in the VFB path. With the larger load current at $f_{\text{IN}} = 6$ kHz, the CFB path also contributes to non-linearity. The THD+N in this case is $-90.9/-85.4$ dB for $K = 1.25/2.5$. Fig. 15 shows the THD+N across output amplitude for input frequencies of 1 and 6 kHz for both the CFB gains. With $K = 1.25$, the THD+N peaks at -87.3 and -91.1 dB for a 1- and 6-kHz input frequency, respectively. With the higher CFB gain of $K = 2.5$, the peak THD+N numbers are similar to $K = 1.25$. However, at amplitudes close to FS ($V_O \sim 7$–$8V_{\text{rms}}$) for the larger load currents with the 6-kHz

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

	This Work		[6]		[2]	[3]	[4]
Architecture	**Analog in, Class-D**		Digital in, Class-D		Analog in, Boost + Class-H	Analog in, Boost + Class-G	Analog in, Boost + Class-D
			1 channel	2 channel			
PVDD (V)	**14.4**		12	24	3.6	3.6	3.6
Piezo Load (µF)	**4**		1	4	1.5	1	1
Resistor-less	**Yes**		Yes		No	No	No
Configuration	**L + C_L**		2L + 2C + C_L		R + C_L	R + C_L	R + L+ C_L
I_Q (mA)	**8.5**		37	130	4	8	5
P_Q (mW)	**122.4**		444	3120	14.4	28.8	18
THD+N_{PEAK} (dB) (f_{IN} = 1k)	**-87.3 (K=1.25)**	**-86.8 (K=2.5)**	-77.0	-77.6	-66.0	-94.0	-66.0
THD+N_{PEAK} (dB) (f_{IN} = 6k)	**-91.1 (K=1.25)**	**-89.5 (K=2.5)**	-	-	-	-	-
Dynamic Range (dB) [A-wt.]	**106.5**		111 (24V supply)		-	106	-
SNR (dB) [A-wt.]	**105.8**		111 (24V supply)		98	108	94
Output noise (µVrms) [A-wt.]	**45**		45		134	-	-
Peak Current (A)	**4.4**		7.5	15	2.8*	1.4*	1.2*
Power Consumption (W) (C_L = 4µF, f_{IN} = 10kHz, V_O = 10V_{RMS})	**3.5**		-	13.9	-	-	-
Power Consumption (W) (f_{IN} = 1kHz, V_O = 7V_{RMS})	**0.44 (R_{EXT} = 0Ω)**		0.46* (R_{EXT} = 0Ω)	3.2* (R_{EXT} = 0Ω)	0.75* (R_{EXT} = 10Ω)	0.35* (R_{EXT} = 10Ω)	0.14* (R_{EXT} = 10Ω)
PSRR (dB) (20- 20kHz)	**> 68**		72**		> 50	> 58	> 80

* Estimated from plots, ** reported only at f_{SUPPLY} = 1kHz

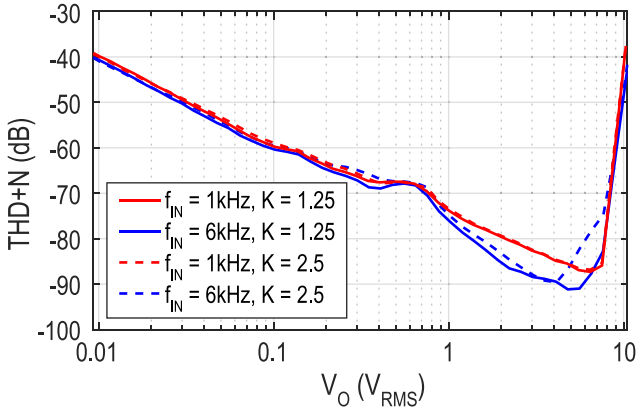

Fig. 15. THD+N across V_O.

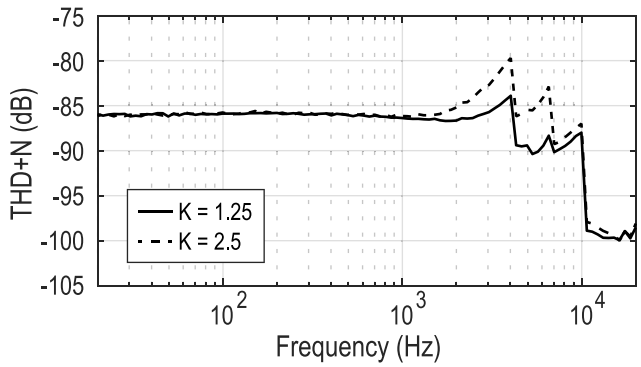

Fig. 16. THD+N across frequency ($V_O = 5V_{rms}$).

input frequency, the THD+N with $K = 1.25$ is ∼8 dB better than with $K = 2.5$, thus demonstrating a better linearity due to the lower CFB gain. The reduction in THD+N for $K = 2.5$ in this case is primarily attributed to the self-heating of $R_{S,P/N}$. Fig. 16 shows the THD+N across frequency for a fixed $V_O = 5V_{rms}$. Beyond 10 kHz, the THD+N is purely noise limited. The amplifier has an A-weighted output noise of 45 μV_{rms} and a dynamic range of 106.5 dB (measured using a −60-dB FS input).

Fig. 17 shows the measured power consumption of the amplifier when driving the 4 μF load with different input frequencies. It can deliver a peak current of $4.4A_P$, which corresponds to $V_O = 10.2V_{rms}$ (FS) at an input frequency of 12 kHz. In this situation, the amplifier consumes 4.9 W, which is mainly dominated by the conduction and switching losses of the amplifier. As per simulations for the same condition, the sense resistors account for 8%–10% of the total power consumption. To get an estimate of the power savings achieved in comparison to a conventional Class-D amplifier with a series R_{EXT}, the power losses were emulated for resistors that provide the same damping as the CFB gains used. An additional power of ∼1.9 and ∼3.5 W is then lost in $R_{EXT} = 0.2\ \Omega$ ($K = 1.25$) and $R_{EXT} = 0.35\ \Omega$ ($K = 2.5$). Due to the capacitive loading, the power consumption decreases with decreasing frequency.

Fig. 18 shows the PSRR of the amplifier (seven samples) when the supply is perturbed by a $1V_{rms}$ sine wave across

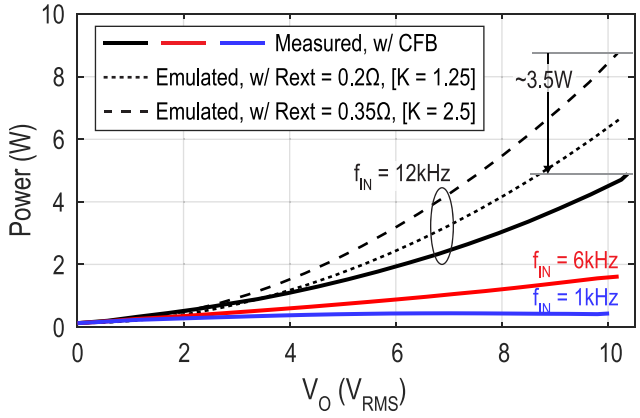

Fig. 17. Power consumption versus V_O and f_{IN} for $C_L = 4\ \mu$F.

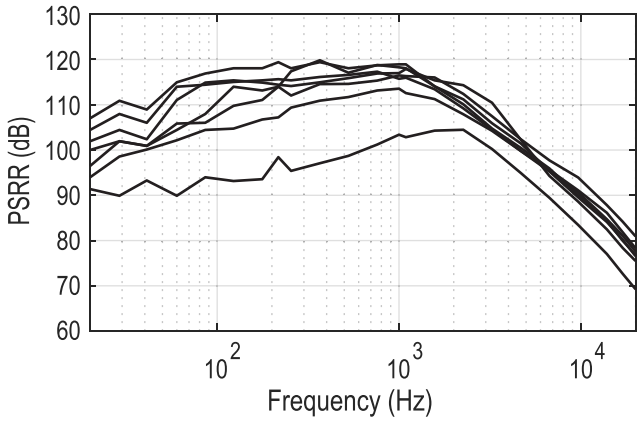

Fig. 18. PSRR of the amplifier (7× samples).

frequency. Due to chopping, the amplifier's PSRR is significantly less dependent on the matching of the $R_{\text{IN}}/R_{\text{FB}}$ pairs. Although the relatively large spread in PSRR at low frequencies is not well understood, possible causes include an over-estimation in the degree of matching in the HV chopper devices,[1] along with off-chip component variations across different daughterboards for the seven samples. The PSRR roll-off beyond 1 kHz is attributed to limitations in the measurement setup, such as a finite CMRR of the analyzer and on-board asymmetric coupling from supply to the output nodes. Overall, for all seven samples, the PSRR is >100 dB at 1 kHz and >68 dB in the entire audio band.

A comparison of the performance of this amplifier with other state-of-the-art designs is shown in Table I.

V. Conclusion

A resistor-less Class-D piezoelectric speaker driver using a dual VFB and CFB topology is presented. CFB enables resistor-less *LC* resonance damping, thereby enabling a low-power system at a reduced cost. In addition, a PP-modulated output stage lowers the power consumption of the amplifier itself. Linearity is improved by employing chopping in the VFB loop and suppressing the CFB loop gain in the audio band. The amplifier can deliver $4.4A_P$ while consuming 122 mW during idle operation. Finally, it achieves a competitive DR, output noise, and PSRR.

[1]Due to the absence of mismatch models for several LDMOS devices in this process, the degree of matching was estimated based on previous silicon measurements.

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References

[1] TDK. (2020). *PiezoListen Piezo Speakers*. [Online]. Available: https://product.tdk.com/info/en/catalog/datasheets/piezolisten_commercial_phu_en.pdf

[2] Texas Instruments. (2011). *LM48560 Mono, Analog Input, Ceramic Speaker Driver*. [Online]. Available: https://www.ti.com/product/LM48560

[3] Maxim Integrated. (2008). *MAX9788 14VPP, Class-G Ceramic Speaker Driver*. [Online]. Available: https://www.maximintegrated.com/en/products/analog/audio/MAX9788.html

[4] Texas Instruments. (2008). *TPA2100P1 Mono, Analog Input, Ceramic Speaker Driver*. [Online]. Available: https://www.ti.com/product/TPA2100P1

[5] H. Ma, R. van der Zee, and B. Nauta, "A high-voltage class-D power amplifier with switching frequency regulation for improved high-efficiency output power range," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1451–1462, Jun. 2015.

[6] Texas Instruments. (2020). *DRV5825P Digital Input, 48VPP, 7.5 A Stereo, 15 A Mono, Piezo Speaker Driver With Adaptive I/V Limiter*. [Online]. Available: https://www.ti.com/product/DRV5825P

[7] D. Nielsen, A. Knott, and M. A. E. Andersen, "Hysteretic self-oscillating bandpass current mode control for class D audio amplifiers driving capacitive transducers," in *Proc. IEEE ECCE Asia Downunder*, Jun. 2013, pp. 971–975.

[8] M. C. W. Høyerby and M. A. E. Andersen, "Carrier distortion in hysteretic self-oscillating class-D audio power amplifiers: Analysis and optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 714–729, Mar. 2009.

[9] S. Karmakar, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A −91 dB THD+N resistor-less class-D piezoelectric speaker driver using a dual voltage/current feedback for LC resonance damping," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3.

[10] M. Score, P. Dagli, R. Jones, and W. Chen, "Modulation scheme for filterless switching amplifiers with reduced EMI," U.S. Patent 6 614 297 B2, Jan. 9, 2003.

[11] T. Karaca and B. Deutschmann, "Electromagnetic evaluation of class-D switching schemes," in *Proc. 11th Conf. Ph.D. Res. Microelectronics Electron. (PRIME)*, Sep. 2015, pp. 113–116.

[12] C. E. Lokin, R. A. R. van der Zee, D. Schinkel, and B. Nauta, "EMI reduction in class-D amplifiers by actively reducing PWM ripple," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 3, pp. 765–773, Mar. 2020.

[13] J.-H. Lee, G.-G. Kang, M.-W. Ko, G.-H. Cho, and H.-S. Kim, "An 8 Ω, 1.4 W, 0.0024% THD+N class-D audio amplifier with bridge-tied load half-side switching mode achieving low standby quiescent current of 660 μA," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.

[14] H. Zhang *et al.*, "A high-linearity and low-EMI multilevel class-D amplifier," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1176–1185, Apr. 2021.

[15] M. Høyerby, J. K. Jakobsen, J. Midtgaard, and T. H. Hansen, "A 2 × 70 W monolithic five-level class-D audio power amplifier in 180 nm BCD," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2819–2829, Dec. 2016.

[16] J.-H. Lee *et al.*, "An 8Ω 10 W 91%-power-efficiency 0.0023%-THD+N multilevel class-D audio amplifier with folded PWM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 88–89.

[17] P. P. Siniscalchi and R. K. Hester, "A 20 W/channel class-D amplifier with near-zero common-mode radiated emissions," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3264–3271, Dec. 2009.

[18] A. Nagari, E. Allier, F. Amiard, V. Binet, and C. Fraisse, "An 8 Ω 2.5 W 1%-THD 104 dB(A)-dynamic-range class-D audio amplifier with ultra-low EMI system and current sensing for speaker protection," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3068–3080, Nov. 2012.

[19] M. Berkhout, L. Dooper, and B. Krabbenborg, "A 4Ω 2.65 W class-D audio amplifier with embedded DC–DC boost converter, current sensing ADC and DSP for adaptive speaker protection," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2952–2961, Dec. 2013.

[20] Texas Instruments. (2016). *TAS6424-Q1 Automotive, 75-W, 2-MHz, 4-CH, 4.5- to 26.4-V Digital Input Class-D Audio Amplifier*. [Online]. Available: https://www.ti.com/lit/gpn/tas6424-q1
[21] S. Karmakar *et al.*, "A 28-W, −102.2-dB THD+N class-D amplifier using a hybrid ΔΣM-PWM scheme," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3146–3156, Dec. 2020.
[22] W.-C. Wang and Y.-H. Lin, "A 118 dB PSRR, 0.00067% (−103.5 dB) THD+N and 3.1 W fully differential class-D audio amplifier with PWM common mode control," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2808–2818, Dec. 2016.
[23] H. Zhang, N. N. M. Rozsa, M. Berkhout, and Q. Fan, "A chopper class-D amplifier for PSRR improvement over the entire audio band," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2035–2044, Jul. 2022.
[24] M. Berkhout, "An integrated 200-W class-D audio amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1198–1206, Jul. 2003.
[25] C.-Y. Ho, C. Liu, C.-L. Lo, H.-C. Tsai, T.-C. Wang, and Y.-H. Lin, "A 4.5 mW CT self-coupled ΔΣ modulator with 2.2 MHz BW and 90.4 dB SNDR using residual ELD compensation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2870–2879, Dec. 2015.

Shoubhik Karmakar (Member, IEEE) received the B.E. degree in electrical and electronics engineering from the Birla Institute of Technology and Science, Pilani, Goa, India, in 2012, and the M.Sc. degree from the Delft University of Technology, Delft, The Netherlands, in 2017, where he is currently pursuing the Ph.D. degree.

His current research interests include energy-efficient data converters, high-performance class-D power amplifiers, and precision analog circuits.

Marco Berkhout (Member, IEEE) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the University of Twente, Enschede, The Netherlands, in 1992 and 1996, respectively.

From 1996 to 2019, he was with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He is currently a fellow with Goodix Technologies, Nijmegen. His main research interests are class-D amplifiers and integrated power electronics.

Dr. Berkhout serves as a member of the Technical Program Committee for the International Solid-State Circuits Conference (ISSCC). He was a member of the Technical Program Committees of the European Solid-State Circuits Conference (ESSCIRC) from 2008 to 2018 and ISSCC from 2013 to 2016. He received the 2002 ESSCIRC Best Paper Award and was a Plenary Invited Speaker on audio at low and high powers at 2008 ESSCIRC.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has led to 17 books, more than 300 technical articles, and more than 30 patents.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences. He was the Analog Subcom Chair of the International Solid-State Circuits Conference (ISSCC) and has served on the program committees of several other IEEE conferences. He is currently one of the organizers of the Advances in Analog Circuit Design Workshop and the IEEE Sensor Interfaces Meeting. He is also an ISSCC Top-Ten Contributor (with more than 60 articles) and was a co-recipient of 17 best paper awards, including two from JSSC, five from ISSCC, two from the VLSI Circuits Symposium, and among others. He has also served the Solid-State Circuits Society as a Distinguished Lecturer and an elected member of its Adcom.

Qinwen Fan (Member, IEEE) received the B.Sc. degree in electronic science and technology from Nankai University, Tianjin, China, in 2006, and the M.Sc. degree (*cum laude*) in microelectronics and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2008 and 2013, respectively.

From August 2007 to August 2008, she was an Intern with NXP Research Laboratories, Eindhoven, The Netherlands, where she designed a precision instrumentation amplifier for biomedical purposes. From October 2012 to May 2015, she worked with Maxim Integrated Products, Delft. From June 2015 to January 2017, she worked with Mellanox, Delft. Since 2017, she has been with the Delft University of Technology, where she is currently an Assistant Professor with the Electronics and Instrumentation Laboratory. Her current research interests include precision analog, class D audio amplifiers, dc–dc converters for energy harvesters, and current-sensing amplifiers.

Dr. Fan currently serves as a TPC Member for the International Solid-State Circuits Conference (ISSCC), the VLSI Symposium on Technology and Circuits, and the European Solid-State Circuits Conference (ESSCIRC). She is also an Associate Editor of the IEEE OPEN JOURNAL OF THE SOLID-STATE CIRCUITS SOCIETY (OJ-SSCS).