Tuning Range Extension of a Transformer-Based Oscillator Through Common-Mode Colpitts Resonance

Shahmohammadi, Mina; Babaie, Masoud; Staszewski, Robert Bogdan

Tuning Range Extension of a Transformer-Based Oscillator Through Common-Mode Colpitts Resonance

Mina Shahmohammadi, *Member, IEEE*, Masoud Babaie, *Member IEEE*,
and Robert Bogdan Staszewski, *Fellow, IEEE*

Abstract—In this paper, we propose a method to broaden a tuning range of a CMOS *LC*-tank oscillator without sacrificing its area. The extra tuning range is achieved by forcing a strongly coupled transformer-based tank into a common-mode resonance at a much higher frequency than in its main differential-mode oscillation. The oscillator employs separate active circuits to excite each mode but it shares the same tank, which largely dominates the core area but is on par with similar single-core designs. The tank is forced in common-mode oscillation by two injection locked Colpitts oscillators at the transformer's primary winding, while a two-port structure provides differential-mode oscillation. An analysis is also presented to compare the phase noise performance of the dual-core oscillator in common-mode and differential-mode excitations. A prototype implemented in digital 40-nm CMOS verifies the dual-mode oscillation and occupies only 0.12 mm² and measures 56% tuning range.

Index Terms—Common-mode oscillation, transformer, wide tuning range, Colpitts oscillator, inductor-capacitor (LC) tank.

I. INTRODUCTION

OSCILLATOR design for multi-mode multi-band [e.g., Fourth Generation (4G) wireless cellular] applications demands wide tuning range (TR) while ensuring sufficiently low phase noise (PN) for a range of targetted frequency bands. The maximum achievable TR of a traditional single-core LC-tank oscillator is limited at 35–40% by a C_{on}/C_{off} capacitance tuning ratio of its switched-capacitor network, further constrained by large size of its switches needed to prevent deterioration of the LC-tank's quality (Q)-factor. For example, the Q-factor of a switched-capacitor network in a 40-nm technology is about 80 at 4 GHz resonant frequency when $C_{on}/C_{off} = 2$. For an inductor's Q-factor of 15 at this frequency, the tank's equivalent Q-factor reduces to 12.6.

The most straightforward solution seems to be designing two *separate* oscillators [1], [2] at the expense of large area, and the need for high-frequency source-selecting multiplexers,

which increase power consumption and noise floor. A system-level local oscillator (LO) solution in [3] uses a single 40 GHz oscillator followed by a ÷2 divider and an LC-tank mixer to generate 20 and 30 GHz LO signals. However, the extra mixer costs significant power and area as well as it produces spurs. Another attempt is to decrease the area of a *two-core* oscillator by placing one inductor underneath the other [4], [5]. However, the top inductor has to be very large so the other one can be placed at its center without degrading the top inductor's quality factor. Therefore, the oscillator area is still considerably larger than that of a single-tank oscillator.

Employing switched resonator tanks, in which the tank's inductance is controlled by turning on/off interconnecting switches, is another TR expanding technique [6]–[13]. However, the switches' resistance limits the tank's Q-factor, thus degrading the oscillator PN [14]. Transformer-based dual-band oscillators [15], [16] offer wide but not continuous tuning range. A switched-shielded transformer [17] is another method to increase the oscillator's tuning range but it appears effective only at mm-wave frequencies. A shielded inductor [18] with a shorting switch is inserted between two windings of a transformer [17]. The coupling factor between the windings changes as to whether the current is flowing in the shielded inductor or not. This transformer is not large, however, its inductors' quality factor gets compromised. Consequently, this range-increasing technique is interesting for mm-wave applications where the tank's quality factor is rather limited by the capacitive part; however for the single-GHz RF frequencies the degradation of the tank's Q-factor would seem to be excessive.

Recent works on mode-switching oscillators significantly improve the PN vs. TR trade-off [19]–[21], however, they *do not* improve the TR vs. die area trade-off. For example, Li et al. [20] switches between resonant modes (even/odd) of two capacitively and magnetically coupled LC resonators, as shown in Fig. 1(a). Strong magnetic coupling enhances the difference between the two resonant frequencies; hence, a continuous TR extension calls for a low coupling factor, such that the transformer ends up to be quite large. Unfortunately, the recent CMOS technology nodes (28 nm and, to a lesser extent, 40 nm) have brought about very tough minimum metal-density requirements, therefore, the inductors and transformers should be filled with a lot of dummy metal pieces [22]. This has negative consequences on inductors as resistive losses due to eddy currents in the dummy fills degrade the Q-factor. And, that is in addition to increasing the parasitic capacitance,
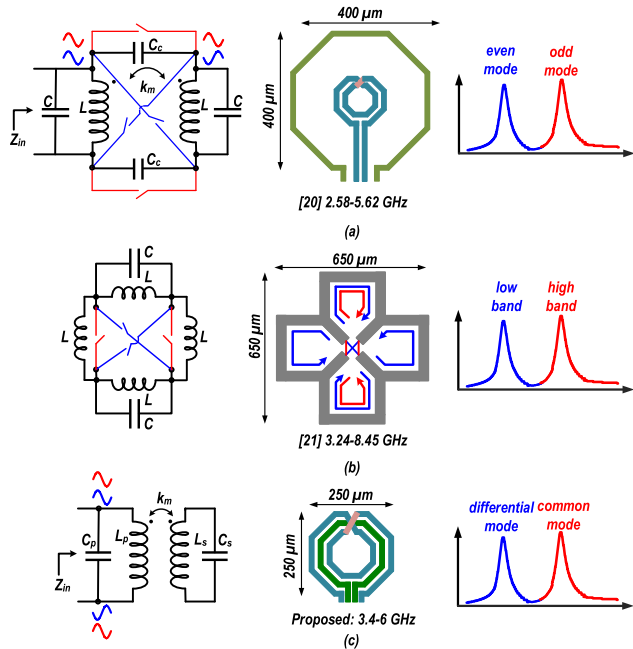
Fig. 1. LC-tanks for wide tuning range: (a) resonant mode switching technique [20]; (b) band switching technique [21]; (c) proposed technique.

Fig. 2. (a) a transformer-based tank; (b) limited DM and CM TR due C_s, c; 1:2 turn transformer: (c) DM excitation; (d) CM excitation; and (e) tank's input impedance.

thus narrowing the TR. The losses are even more severe in the weakly coupled transformers. The spacing between their primary and secondary windings is larger [see Fig. 1(a)] and must be filled with dummy metal pieces, but it is precisely where the magnetic flux is concentrated the most.

In Taghivand et al. [21], as shown in Fig. 1(b), four identical inductors are coupled through four mode-switching transistors, providing two oscillation bands. In a *low-band* oscillation mode, there is no AC current flow possibility in two of these inductors [see Fig. 1(b)], however in a *high-band* mode, the AC current can flow in all the inductors. Thus, the effective inductance value in each band could be controlled. Obviously, the four inductors significantly increase the area.

Considering that not all applications require as stringent PN performance as does cellular wireless, we concentrate in this paper on maintaining the die area similar to that of a single LC-tank oscillator, while significantly improving the TR and keeping a reasonable PN performance. The proposed single-tank oscillator employs a strongly coupled transformer-based tank and forces the tank to oscillate either in a differential mode (DM) or common mode (CM), see Fig. 1(c). The DM oscillation provides the TR equivalent of a single-tank oscillator. The TR is then *extended* by the CM oscillation. The oscillator has two separate active circuits to excite each mode. However, since the passive part is shared in both modes, the die area is comparable to that of a typical narrow TR oscillator.

Section II describes how the transformer-based tank can exhibit both DM and CM resonances. Section III describes a circuit implementation of the two-core oscillator that excites one of these resonances at a time. Section IV shows measurement results.

II. COMMON MODE RESONANCES

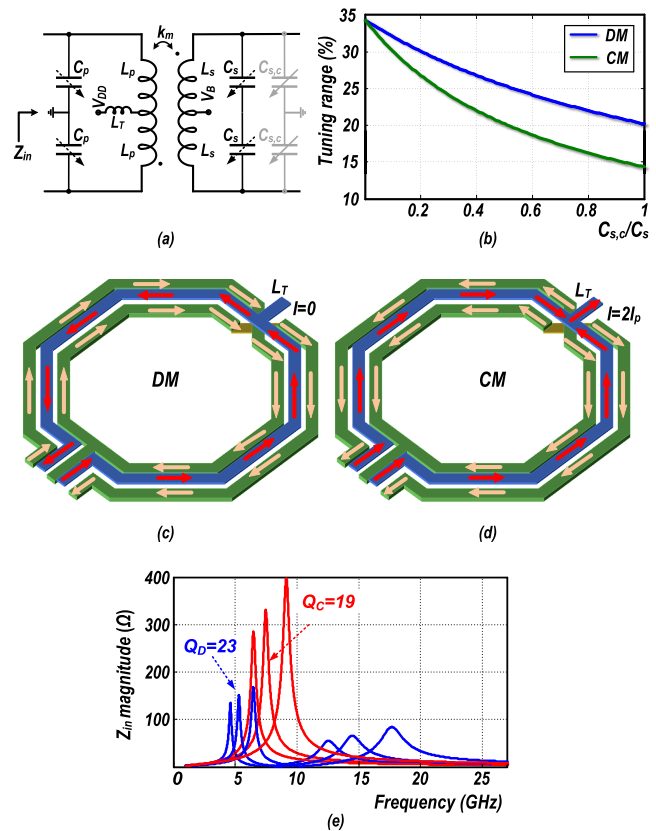A transformer-based tank, depicted in Fig. 2(a), exhibits two DM resonant frequencies. If this transformer possesses a strong magnetic coupling factor, k_m, its leakage inductance would be small and so the second DM resonant frequency would be much higher than the main one. Consequently, we would not get a continuous extension of the TR by forcing the oscillation at the second DM resonant frequency. On the other hand, in order for the transformer size to be not much larger than that of an inductor, $k_m > 0.6$ appears a necessary condition. With this constraint, the first resonance can be estimated as [24]:

$$\omega_{0,DM} \approx \frac{1}{\sqrt{L_p C_p + L_s C_s}}, \tag{1}$$

where, L_p and C_p are primary, and L_s and C_s are secondary windings' inductances and capacitances. The approximation error of (1) from the exact resonant frequency [24, eq. (5)] is less than $+6\%$ for $k_m \geq 0.7$.

Abandoning the hope of exploiting the second DM resonance, suppose now this tank is excited by CM signals, and, for now, we assume primary and secondary winding inductances and k_m are similar in DM and CM excitations. CM signals cannot see the differential capacitors, thus the tank can only exhibit CM resonances when these capacitors are single-ended. If this tank were to employ only single-ended primary and *differential* secondary capacitors, the secondary winding inductances and capacitances would not affect the CM characteristics of the tank, e.g., resonant frequency.

This tank will show a single CM resonance at

$$\omega_{0,CM} \approx \frac{1}{\sqrt{L_p C_p}}. \qquad (2)$$

The difference between the CM and DM resonance frequencies, i.e., Eqs. (2) and (1), suggests a new possibility for extending the tuning range toward higher frequencies, provided we can build an oscillator around this transformer-based tank that can excite it with either DM or CM signals, without adding any bulky passive components.

To investigate how much tuning range we can expect from a single tank, we assume the tank employs a switched capacitor bank with a 2:1 capacitance switching ratio:

$$C_{p,max}/C_{p,min} = C_{s,max}/C_{s,min} = 2, \qquad (3)$$

This ratio should guarantee a sufficiently high Q-factor of switched-capacitors in recent CMOS technologies. With this assumption, $f_{max}/f_{min} = \sqrt{2}$ in both modes, and thus, both DM and CM resonant frequencies (Eqs. (1) and (2)) will tune by $2(\sqrt{2}-1)/(\sqrt{2}+1) = 34.3\%$. To avoid any gaps between the DM and CM tuning ranges, at least $\omega_{CM,low} = \omega_{DM,high}$. Hence,

$$L_s C_{s,max} = L_p C_{p,max} \qquad (4)$$

With these conditions, the resonant frequency could theoretically cover an octave while going from DM to CM oscillations. Practically, C_{max}/C_{min} has to be >2 due to parasitics and difficulty with controlling the precise overlap between the DM and CM resonances.

It needs to be noted that the above equations are only valid if the primary inductance is the same in DM and CM excitations. However, this assumption is not entirely valid due to the metal track inductance which connects the center tap of the transformer's primary to the supply (L_T in Fig. 2(a)). Repeating the same steps for the general condition and still assuming Eq. (3), the overlap condition constraint results in,

$$L_s C_{s,max} = (2L_{p,CM} - L_{p,DM})C_{p,max}, \qquad (5)$$

where, $L_{p,CM}$ and $L_{p,DM}$ are the primary inductance in, respectively, CM and DM. Merely to avoid complications in the equations, we henceforth assume $L_{p,CM} = L_{p,DM}$

One limiting factor in the tuning range of such an oscillator is the single-ended parasitic capacitance throughout the secondary winding side. If the CM coupling factor, $k_{m,c}$, were hypothetically similar to the DM one, $k_{m,d}$; and $k_{m,c} = k_{m,d} > 0.6$, then the CM resonance would shift down to $\omega_{0,CM} = 1/\sqrt{L_p C_p + L_s C_{s,c}}$, where $C_{s,c}$ is the total of single ended capacitances on the secondary side, Fig. 2(a). At the same time, the DM resonance would also shift down to $\omega_{DM} = 1/\sqrt{L_p C_p + L_s C_s + L_s C_{s,c}}$. Interestingly, satisfying the overlap between CM and DM oscillations with the condition in (3) results in the same constraint as Eq. (4) or (5). However, the fixed parasitic capacitance, $C_{s,c}$, degrades the CM oscillation tuning range more than it degrades the DM oscillation tuning range, see Fig. 2(b).

A 1:2 turns-ratio transformer, which has distinctly different characteristics in DM and CM excitations, relieves such a degradation. Figures 2 (c) (d) show this transformer when its primary is excited, respectively, with DM or CM signals. In the DM excitation, the induced currents at the two sides of the secondary winding circulate constructively in the same direction, thus creating a strong coupling factor between the transformer windings, while in the CM excitation these induced currents cancel each other within each full turn of the secondary winding (i.e., from the secondary's terminal to the secondary's center-tap), leading to a weak coupling factor [23]. This weak $k_{m,c}$ can be interpreted as the secondary winding not being seen from the primary and, therefore, the secondary's single-ended capacitors have an insignificant effect on the tank's CM resonant frequency.

Assuming the capacitor bank is almost ideal, at least compared to the lossy inductors represented by the r_p and r_s equivalent series resistances of the primary/secondary windings, CM resonance has the quality factor of $Q_{CM} = Q_p = L_p \omega/r_p$, which is similar to that of an inductor-based tank. The high Q-factor of this resonance indicates that with an appropriate active circuitry, the CM oscillation of a reasonable quality would be possible. The DM and CM input impedances of this tank are shown in Fig. 2 (e).

The single-ended switched capacitors require two switches to provide a ground connection in the middle, which results in a 50% lower Q-factor as compared to a differential switched capacitor with the same switch size. This would appear as a disadvantage of our proposed technique; however, that is not the case. Let us compare the tuning range of a typical inductor-based tank oscillator employing the differential capacitor bank with our transformer-based tank oscillator employing the single-ended primary and the differential secondary capacitor banks. The equivalent capacitance of this bank varies from $C_{\text{on,D}} = C_p$ to $C_{\text{off,D}} = \frac{C_p C_{par}}{C_p + C_{par}}$, where C_{par} is the parasitic capacitance of the switch. For a typical $C_{\text{off,D}}/C_{\text{on,D}}$ value of 0.5 ($C_{par} = C_p$), the inductor-based oscillator employing this tank would exhibit $f_{max}/f_{min} = \sqrt{2}$. The width of each switch in the single-ended switched-capacitor bank should be twice the width of each differential counterpart for the same Q-factor. Consequently, $C_{\text{off,C}} = \frac{2C_p C_{par}}{C_p + 2C_{par}} = \frac{2}{3}C_p$. Employing this capacitor bank in a transformer-based tank at the primary winding and employing the differential bank at the secondary winding, and benefiting from the impedance transformation of the 1:2 turns-ratio transformer ($L_s/L_p \approx 3$), results in $\frac{f_{max}}{f_{min}} = \sqrt{1.9}$, which is very close to the inductor-based tank tuning range.

III. PROPOSED WIDE TUNING RANGE OSCILLATOR

A. Dual-Core Oscillator

Forcing the transformer-based tank to resonate in DM is quite straightforward. The oscillator can be realized as a one-port or a two-port structure [25], [26]. However, only the two-port structure will guarantee a reliable start-up at the first DM resonance [24], thus preventing the mixed DM oscillation.

A separate active circuit is now needed to force the tank into the CM resonance. Colpitts and Hartely topologies are two well known examples of single-ended oscillators. Invoking our ground principle of sharing the *same* tank by the active CM and DM circuits, the Coplitts structure is consequently
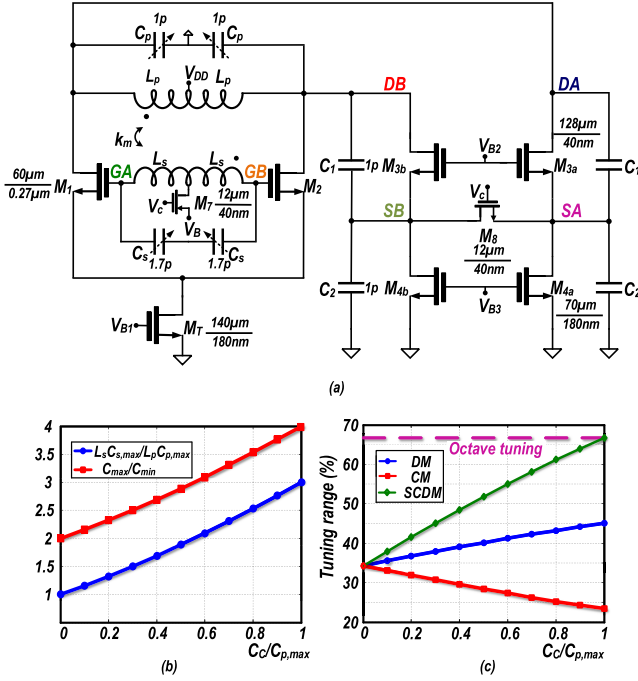
Fig. 3. Dual-core oscillator: (a) schematic; (b) overlap and octave oscillation conditions; and (c) tuning range.
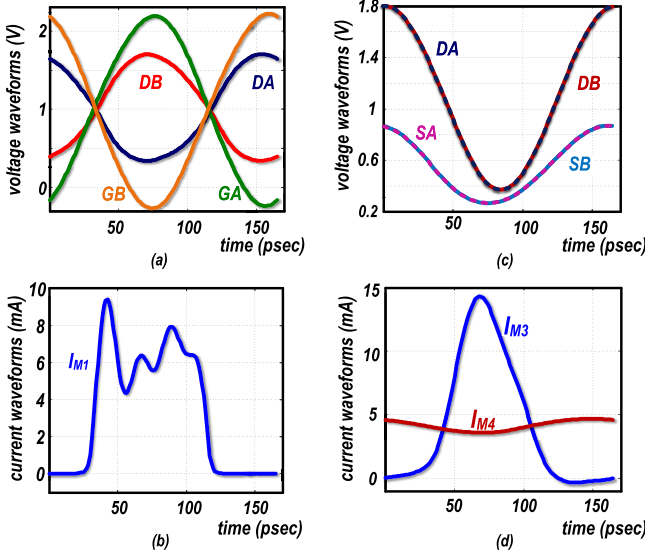

Fig. 4. Dual-core oscillator waveforms: (a)(b) DM; and (c)(d) CM.

chosen. To improve the PN, two mutually injection-locked Colpitts oscillators share the primary inductor. The schematic of the proposed dual-core oscillator is shown in Fig. 3(a). To avoid the dual oscillation, only one active circuit core is turned on at a time.

The left side of Fig. 3(a) is the two-port DM oscillator. In this mode, $V_{B2} = V_{B3} = 0V$, M_7 switch is on 'biasing' $M_{1,2}$, while M_8 switch is off. The waveforms are shown in Fig. 4 (a) (b). The transformer has the 1:2 turns ratio and its gain reduces the $M_{1,2}$ noise up-conversion to PN, and also results in a larger gate voltage compared to drain voltages, which facilitates oscillation start-up.

The right-hand side of the oscillator schematic are two locked single-ended Colpitts oscillators. M_8 switch is now

turned on to ensure the in-phase operation of the two Colpitts oscillators, without which the two cores might exhibit an arbitrary phase shift. In this mode, $V_{B1} = 0V$ to turn off the differential oscillation. M_7 switch is also off to minimize the CM inductive loading on the primary winding by the secondary one. Both single-ended oscillators start at the same frequency but could be slightly out of phase; subsequently, they lock to each other and there is no phase shift between them. The locking of the two oscillators gives an additional 3 dB PN improvement. Waveforms are shown in Fig. 4 (c) (d).

Note that an attempt of simplifying the CM structure by removing M_8 and permanently shorting the sources of M_3 transistors would be detrimental to the DM tuning range. While obviously the DM oscillation would still work – M_3 transistors are off in this mode – the extra capacitance C_{fix} due to the CM circuitry seen by C_p would be larger. With M_8 off, DA/DB node sees $C_{fix} = C_1C_2/(C_1 + C_2)$, but when M_3 sources are shorted, that capacitance raises to $C_{fix} = C_1 > C_1C_2/(C_1 + C_2)$. Furthermore, an attempt of moving M_8 from the SA/SB source nodes of M_3 to the DA/DB drain nodes would likewise increase the effective parasitic capacitance of M_8.

The C_1 and C_2 capacitors are necessary to create a negative resistance for the Colpitts oscillators; however, they are limiting the tuning range in both modes. In their presence, (3) and (4) are not valid anymore for the overlap and octave tuning. Assuming the same capacitance variation range on the primary and secondary sides, $C_{p,max}/C_{p,min} = C_{s,max}/C_{s,min}$, the octave tuning requirement is now

$$\frac{L_sC_{s,max}}{L_pC_{p,max}} = 3\frac{C_C}{C_{p,max}} + 4\frac{C_{p,min}}{C_{p,max}} - 1, \qquad (6)$$

where, $C_C = C_1C_2/(C_1 + C_2)$. The minimum overlap condition, $f_{DM,max} = f_{CM,min}$, dictates

$$\frac{C_{p,max}}{C_{p,min}} = 1 + \frac{L_sC_{s,max}}{L_pC_{p,max}}. \qquad (7)$$

Figure 3(b) shows how the required C_{max}/C_{min} increases with C_C/C_p ratio. Satisfying (7) and (6) in the presence of C_C also unbalances the DM and CM tuning range, as shown in Fig. 3 (c). For a certain value of C_C, the required $C_{p,max}/C_{p,min}$ ratio can become prohibitively large, likely leading to the Q-factor degradation. In practice, $C_{s,max}/C_{s,min}$ and $C_{p,max}/C_{p,min}$ should not be necessarily equal. The secondary-winding capacitor ratio in this design is chosen to be larger than at the primary side, due to the tougher Coplitts oscillator start-up conditions.

B. Phase Noise Analysis

Ideally, a wide TR oscillator would have a comparable PN performance in both oscillation modes. In this section, we investigate the PN of the dual-core oscillator and then compare the two modes in the neighborhood of their overlapping frequencies.

The linear time-variant model [28] suggests,

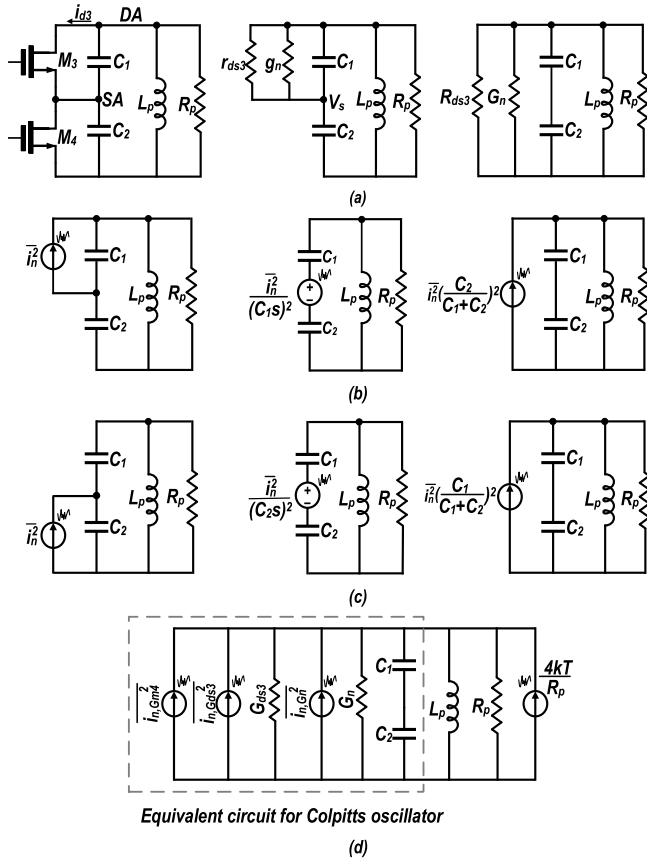$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{kT}{R_tNq_{max}^2(\Delta\omega)^2} \cdot F\right), \qquad (8)$$

Fig. 5. Procedures of referring the noise back to the tank from: (a) r_{ds3} and negative conductance; (b) g_m of M_3; and (c) g_m of M_4. (d) The equivalent circuit of the Colpitts oscillator.

where, k is Boltzmann's constant, T is temperature, R_t is the equivalent parallel resistance of the tank, and q_{max} is the maximum charge displacement across the equivalent capacitance in parallel to R_t. N is the number of resonators, which is 2 here in both DM and CM oscillators. F, the oscillator's effective noise factor, is

$$F = \sum_i \frac{N \cdot R_t}{2kT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \Gamma_i^2(\phi) \overline{i_{n,i}^2(\phi)} d\phi, \qquad (9)$$

in which Γ_i is the ISF of the ith noise source. The relevant ISF of noise sources associated with a sinusoidal waveform oscillator can be estimated by a $\pi/2$ phase shifted sinusoidal function, $\Gamma = \frac{sin(\phi)}{N}$, where $\phi = \omega_0 t$ [27]. In this work, we try to find the noise factors of different noise sources in the dual-core oscillator.

The noise sources of the Colpitts oscillator are R_t, M_3 and M_4. R_t in the CM oscillation is the parallel resistance of the primary winding, R_p. It is insightful to refer every noise source and nonlinearity back to the tank, as it is demonstrated step-by-step in Fig. 5. The negative conductance between DA and SA nodes is

$$g_n = \frac{i_{d3}}{v_{DA} - v_{SA}} = \frac{-g_{m3}v_{SA}}{v_{DA} - v_{SA}} = -g_{m3}\frac{C_1}{C_2} \qquad (10)$$

where, i_{d3} is the small-signal drain current of M_3. The equivalent negative conductance in parallel with the tank is

found as

$$G_n = \left(\frac{C_2}{C_1 + C_2}\right)^2 \cdot g_n = -g_{m3}\frac{C_1 C_2}{(C_1 + C_2)^2} \qquad (11)$$

With a similar derivation, M_3 channel resistance is referred to the tank as

$$R_{ds3} = r_{ds3}\left(\frac{C_1 + C_2}{C_2}\right)^2 \qquad (12)$$

To sustain the oscillation, the average dissipated power in the tank loss and R_{ds3} should be equal to the average power delivered by the negative resistance, which leads to the condition:

$$G_{mEF3} = \frac{1}{n(1-n)} \cdot \frac{1}{R_p} + \frac{1-n}{n} \cdot G_{dsEF3}, \qquad (13)$$

where, $n = C_1/(C_1 + C_2)$, $G_{mEF} = G_m[0] - G_m[2]$, and $G_{dsEF} = G_{ds}[0] - G_{ds}[2]$, in which $G_m[k]$ and $G_{ds}[k]$ are the kth Fourier coefficients of $g_m(t)$ and $g_{ds}(t)$, respectively [29]. The required G_{mEF3} is minimized for $n = 0.5$, which is chosen in this design to facilitate start-up.

The current noise sources are referred to the tank by a Norton to Thevenin and then a Thevenin to Norton conversions, as demonstrated in Fig. 5(b) and (c), which results in,

$$\overline{i_{n3}^2} = 4kT\gamma g_{m3}\left(\frac{C_2}{C_1 + C_2}\right)^2, \qquad (14)$$

$$\overline{i_{n4}^2} = 4kT\gamma g_{m4}\left(\frac{C_1}{C_1 + C_2}\right)^2, \qquad (15)$$

where, γ is the transistor excess noise coefficient. These equations and the fact that $n = 0.5$ indicate that the M_4 noise can substantially contribute to the oscillator PN and presuming an ideal current source would be quite misleading in noise analysis.

Assuming a sinusoidal oscillation, the tank noise factor is found as

$$F_t = \frac{2N}{2kT R_p} \cdot \frac{1}{2\pi} \int_0^{2\pi} \frac{4kT}{R_p} \frac{sin^2(\phi)}{N^2} d\phi = 1. \qquad (16)$$

M_3 and M_4 noise factors are found as

$$F_{gm3} = \frac{2N R_p}{4kT\pi} \int_0^{2\pi} \frac{sin^2(\phi)}{N^2} 4kT\gamma g_{m3}(\phi) \cdot \left(\frac{C_2}{C_1 + C_2}\right)^2 d\phi$$
$$= (1-n)^2 \gamma G_{mEF3} R_P \qquad (17)$$

$$F_{gds3} = \frac{2N R_p}{4kT\pi} \int_0^{2\pi} \frac{sin^2(\phi)}{N^2} 4kT\gamma g_{ds3}(\phi) \cdot \left(\frac{C_2}{C_1 + C_2}\right)^2 d\phi$$
$$= (1-n)^2 G_{dsEF3} R_P \qquad (18)$$

$$F_{gm4} = \frac{2N R_p}{4kT\pi} \int_0^{2\pi} \frac{sin^2(\phi)}{N^2} 4kT\gamma g_{m4} \cdot \left(\frac{C_1}{C_1 + C_2}\right)^2 d\phi$$
$$= n^2 \gamma G_{mEF4} R_P \qquad (19)$$

g_{ds4} noise is very small due to M_4 operating in a saturation region and, consequently, is disregarded in our calculations. Since g_{m4} is fairly constant throughout the period, $G_{mEF4} = g_{m4}$. To estimate the contribution of M_4 to PN, we can calculate g_{m4} as

$$g_{m4} = \frac{2I_0}{V_{gs4} - V_{th}} \approx \frac{2I_0}{V_{ds,min}}, \qquad (20)$$
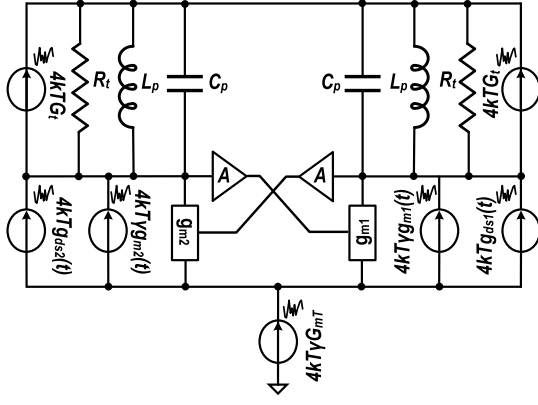
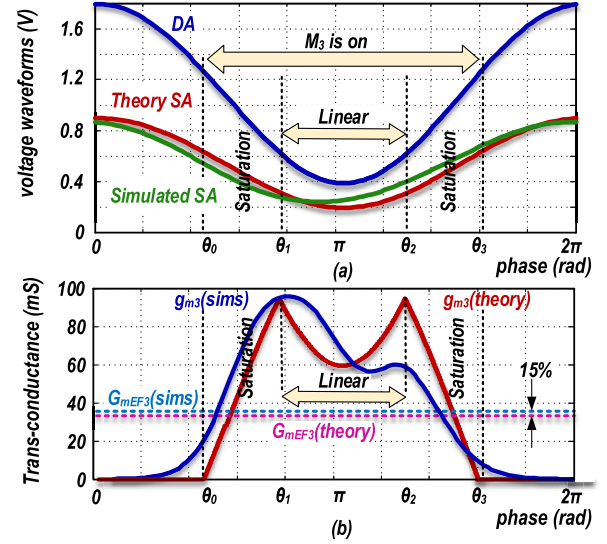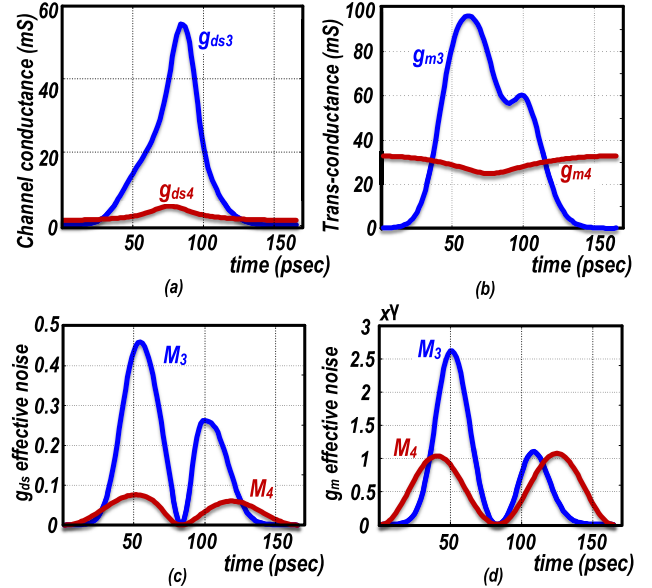Fig. 6. Noise sources of the DM oscillator [24].

Fig. 7. (a) Drain and source voltage waveforms. (b) g_{m3}: theory and simulations.

Fig. 8. Circuit to phase noise conversion in CM oscillator.

where, V_{th} is the transistor's threshold voltage. Let us assign $V_{DD}/2$ to the SA (SB) node, and $V_{DA} \approx 2I_0 R_p(1-n)$ [27],

$$g_{m4} \approx \frac{4I_0}{V_{DD} - 4n(1-n)I_0 R_p} \tag{21}$$

Disregarding g_{ds4} noise contribution,

$$F_{M4} \approx F_{gm4} = \frac{4n^2\gamma R_p I_0}{V_{DD} - 4n(1-n)I_0 R_p} \approx \gamma. \tag{22}$$

By substituting (13) in (17), with G_{mEF3} and G_{dsEF3} numerically obtained from simulations, the total oscillator effective noise factor then will be,

$$F_{CM} = R_P[(1-n)^2 G_{mEF3}(\gamma + \frac{n}{1-n}) + \frac{4n^2\gamma I_0}{V_{DD} - 4n(1-n)I_0 R_p}] - 1 \approx 2.2\gamma + 0.2 \tag{23}$$

The circuit-to-phase noise conversion of the CM oscillator is shown in Fig. 8 (a)-(d).

The noise contribution of M_3 transistor can be numerically calculated based on design parameters. For M_3, $V_d(\phi) = V_{DD} + A_C \cos(\phi)$, $V_s(\phi) \approx V_{DD}/2 + nA_C \cos(\phi)$ and $V_g = V_{B2}$. Figure 7 shows the M_3 operating regions during one oscillating period. At θ_0, V_s gets low enough for M_3 to turn on and enter the saturation region. When the drain voltage gets lower, M_3 enters the triode region at θ_1 and remains there till $\theta_2 = 2\pi - \theta_1$. M_3 finally turns off again at $\theta_3 = 2\pi - \theta_0$. θ_0 and θ_1 can be found from boundary conditions as

$$\theta_0 = \cos^{-1}\left(\frac{V_1}{nA_C}\right) \tag{24}$$

and

$$\theta_1 = \cos^{-1}\left(\frac{V_2}{A_C}\right) \tag{25}$$

where, $V_1 = V_{B2} - V_{DD}/2 - V_{th}$ and $V_2 = V_{B2} - V_{DD} - V_{th}$.

Assuming square law,

$$g_{m3}(\phi) = \begin{cases} K(V_1 - nA_C \cos(\phi)) & \text{saturation,} \\ K(\frac{V_{DD}}{2} + (1-n)A_C \cos(\phi)) & \text{linear,} \\ 0 & \text{cut off,} \end{cases} \tag{26}$$

where $K = \mu C_{ox}\left(\frac{W}{L}\right)$ is the customary designation of MOS transistor strength. G_{mEF3} now can be determined by calculating the Fourier coefficients of $g_{m3}(\phi)$. Solving the lengthy integrations results in

$$\begin{aligned} G_{mEF3} &= \frac{K}{2\pi}[2V_1(\theta_1 - \theta_0) + V_{DD}(\pi - \theta_1) + nA_c \sin(\theta_0) \\ &\quad - A_c \sin(\theta_1) + V_1 \sin(2\theta_0) + (\frac{V_{DD}}{2} - V_1)\sin(2\theta_1) \\ &\quad - \frac{nA_c}{3}\sin(3\theta_0) + \frac{A_c}{3}\sin(3\theta_1)] \end{aligned} \tag{27}$$

G_{mEF3} in (27) can be calculated by substituting θ_0 and θ_1 from (24) and (25), together with other design parameters: $V_{DD} = 1.1$ V, $V_{B2} = 1$ V, $V_{th} \approx 0.37$ V. Fig. 7 (b) shows a very good agreement (within 15%) with the simulation results.
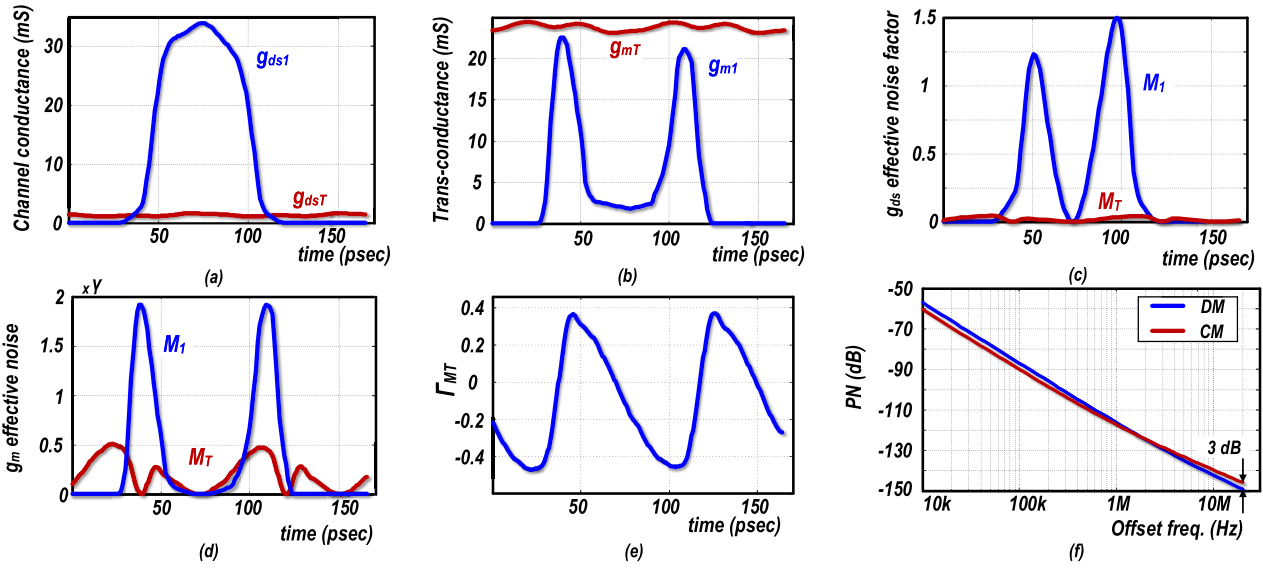
Fig. 9. (a)-(d) Circuit to phase noise conversion in DM oscillator; (e) tail transistor ISF; and (f) PN of CM and DM oscillators at the overlap frequency.

Major noise sources of the DM oscillator are shown in Fig. 6. A general result of the effective noise factor, assuming that the M_T thermal noise is completely filtered out, is derived in [24] as

$$2\Gamma_{t,rms}^2 \cdot \left(1 + \frac{\gamma}{A}\right) \cdot (1 + R_t G_{dsEF1}) \approx 1.6 + 0.9\gamma. \quad (28)$$

However, the M_T thermal noise is not completely filtered out here. To calculate the M_T's noise contribution, the tail node ISF is obtained through simulations and plotted in Fig. 9(e). From that

$$F_{M_T} = \frac{1}{2\pi} \int_0^{2\pi} 4kT\gamma\, g_{mT} \cdot \Gamma_{M_T}^2(t) \frac{R_t}{4kT} dt \approx 0.5\gamma \quad (29)$$

Hence, the DM oscillator noise factor is,

$$F_{DM} = 2\Gamma_{t,rms}^2 \cdot \left(1 + \frac{\gamma}{A}\right) \cdot (1 + R_t G_{dsEF1})$$
$$+ \Gamma_{M_T,rms} R_p G_{MTEF} \approx 1.6 + 1.4\gamma \quad (30)$$

The DM oscillator circuit-to-phase noise conversion is shown in Fig. 9 (a)-(d).

Substituting (23) and (30) in (8) at the *overlap* frequency results in

$$\mathcal{L}_{DM} - \mathcal{L}_{CM} = 10 \log_{10}\left(\frac{R_t Q_p A_C^2}{R_p Q_t A_D^2} \cdot \frac{F_{DM}}{F_{CM}}\right) \approx -2.5 dB,$$
$$(31)$$

where, $Q_p = 14$, $Q_t = 19$, $A_C = 0.7\,V$, $A_D = 0.75\,V$, $R_p = 200\,ohm$, and $R_t = 150\,ohm$, are the CM and DM tank's quality factor, oscillation voltage amplitude, and equivalent tank parallel resistance, respectively. The PN simulation results are shown in Fig. 9(f). It is important to note that due to the wide TR of this dual-core oscillator, R_p and R_t cannot be assumed constant over the TR. Thus to be fair, reporting the PN performance difference in (31) between DM and CM modes should be done at the overlap frequency.

Due to its single-ended structure and the CM resonance, the Colpitts oscillator would appear to be more sensitive to supply noise. However, that is not the case. Supply pushing is the parameter that indicates the supply noise effect on the phase noise. Figure 12(e)(f) demonstrates this parameter for the DM and CM oscillators, which is quite comparable, indicating the CM oscillation does not result in higher phase noise up-conversion sensitivity to the supply noise. To explain that, let us look at the actual mechanism: The oscillation frequency can be modulated by the supply noise by modulating the nonlinear voltage-dependent parasitic capacitors of the core transistors, C_{gs}. In the Colpitts oscillator, the supply voltage is connected to the core transistors' drains, which cannot modulate their C_{gs} directly. Consequently, the oscillation frequency modulation due to the supply noise is considerably reduced.

C. Center Tap Inductance

The single-ended nature of the Colpitts oscillator makes its characteristics especially sensitive to single-ended parasitics. A key parasitic that must be properly modeled and accounted for is the metal track inductance, L_T, which connects the center tap of the transformer's primary to the supply's AC-ground [see Fig. 2(a)]. At the DM excitation, the AC current will not flow into L_T, thus the DM inductance and DM resonant frequency are independent of its value. However, at the CM excitation, the current flowing into L_T is twice the current circulating in the inductors. Consequently, the tank inductance L_p in Fig. 2(a) is re-labeled as $L_{pd} = L_p$ in DM, and $L_{pc} = L_{pd} + 2L_T$ in CM excitations. The CM oscillation frequency will be reduced to $\omega_{CM} = 1/\sqrt{(L_p + 2L_T)C_P}$. This implies that L_T must be carefully modeled and included in simulations, otherwise the increased overlap between CM and DM oscillations would severely limit the total tuning range.

Another important parasitic that is only influential in the CM oscillation is the supply loop resistance between the V_{DD} feed to the center-tap of the primary winding and the sources of M_4 transistors (see Fig. 3), assuming sufficient decoupling capacitance on V_{DD}. This resistance is added directly to the
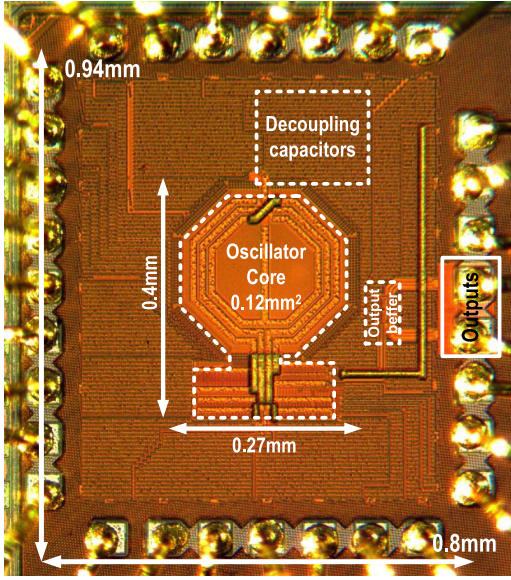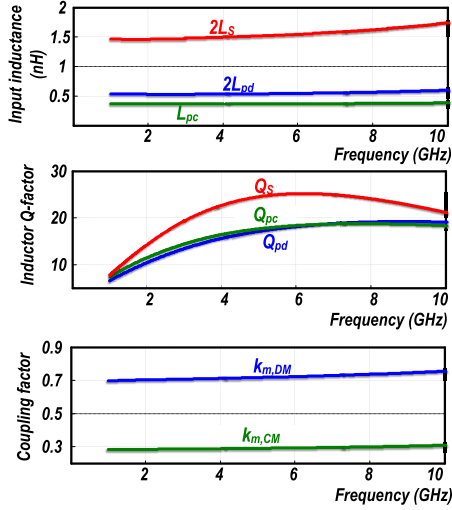
Fig. 10. Chip micrograph.


Fig. 11. Transformer characteristics.

equivalent negative resistance of the Colpitts structure and increases it from $-g_{m3}/C_1C_2\omega^2$ to $-g_{m3}/C_1C_2\omega^2 + r_b$. In our design, the average of that negative resistance at 6 GHz with $C_1 = C_2 = 1$ pF is about -25Ω, which means the r_b parasitic resistance should be kept much smaller as to not endanger the start-up.

IV. EXPERIMENTAL RESULTS

The proposed oscillator is prototyped in TSMC 40-nm 1P7M CMOS process with top ultra-thick metal. $M_{1,2}$ are $(60/0.27)\mu$m and $M_{3,4}$ are $(128/0.04)$ μm low-V_{th} devices for safe start-up of the Colpitts oscillator. The tank employs a 1.4 nH secondary inductor with Q of 25 at 5 GHz and 0.54 nH primary inductor with Q of 17 at 5 GHz. $k_{m,DM} = 0.72$ and $k_{m,CM} = 0.29$. The transformer size is $250 \times 250 \mu$m^2 and the primary-to-secondary winding spacing is 5 μm. The chip micrograph and transformer characteristics are shown in Fig. 10 and Fig. 11 respectively. The oscillator's core area
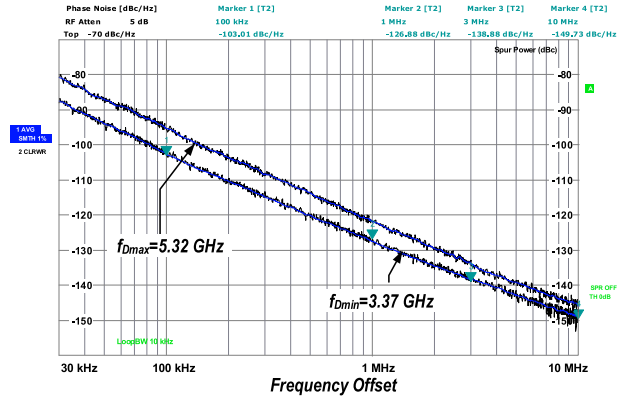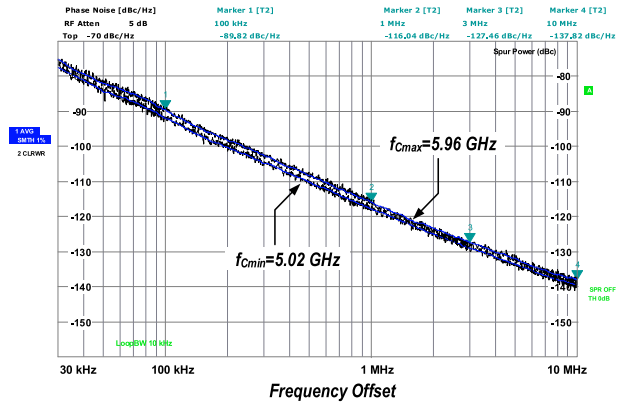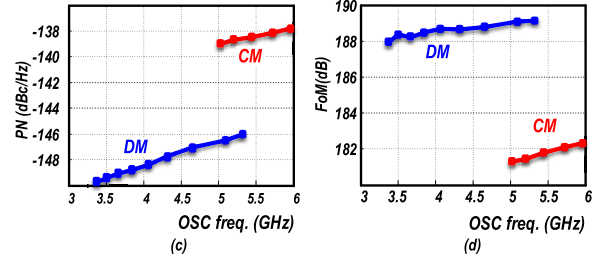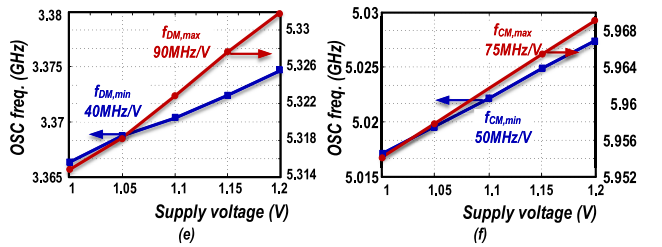
Fig. 12. Measurements: (a) PN at $f_{DM,max}$, $f_{DM,min}$, and (b) $f_{CM,max}$ and $f_{CM,min}$; (c) PN and (d) FoM at 10MHz offset across TR. Frequency pushing due to supply voltage variation in (e) DM, and (f) CM oscillators.

is 0.12 mm^2, which is similar in size to typical narrow tuning-range oscillators. The tank is shared in the two modes of oscillation and so the output is common; hence no further multiplexing is necessary. A comparison with other relevant wide tuning-range oscillators is summarized in Table I. This work is smaller than state-of-the-art by at least a factor of 2.

The oscillators are tuned via 4-bit switched MOM capacitor banks at the primary and secondary. According to post-layout circuit-level simulations, the tuning range is 46% in DM and 20% in CM, with a 100 MHz overlap, giving the

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This Work		[20]		[21]		[4]		[5]		[13]		[14]
Frequency (GHz)	**3.37-5.96**		2.5-5.6		3.24-8.45		2.4-5.3		1.3-6		3.28-8.35		3.14-6.44²
Tuning range (%)	**55.5**		76		89		75.3		128		87.2		69²
V_{DD} (V)	**1**		0.6		0.8		0.4		1.5		1.6		1.2
Technology	**40 nm**		65 nm		40 nm		65 nm		130 nm		130 nm		180 nm
OSC core area	**0.12 mm²**		0.29 mm²		0.43 mm²		0.25 mm²		0.295mm²		0.1mm²		0.35mm²
	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{mid}
P_{DC} (mW)	**16**	**12.5**	14.1	9.9	16.5	14	6	4.4	4.35¹	9.15¹	15.4	6.5	8.8
PN (dBc/Hz) 100kHz	**-103**	**-90**	-101.1	-89	-109	-91	-98	-86	NA	NA	-96	NA	-92
10MHz	**-149.7**	**-137.8**	-151.9	-145.8	-150	-142	-149	-139	-135	-132	-142	-137.2	-140
FoM† (dB) 100kHz	**181.8**	**174.5**	177.6	174	187	178.1	177.8	174.1	NA	NA	174.4	NA	175.4
10MHz	**188.2**	**182.3**	188.4	190.8	188	189.1	188.8	187	171	178	180.4	187.5	183.4
FoMA†† (dB) 100kHz	**191**	**183.7**	182.9	179.4	190.7	181.7	183.8	180.1	NA	NA	184.4	NA	180
10MHz	**197.4**	**191.5**	193.7	196.2	191.7	192.7	194.8	193	176.2	183.2	190.4	197.5	188
FoMAT††† (dB) 100kHz	**205.6**	**198.6**	200.5	197	209.7	200.7	201.3	197.6	NA	NA	203.3	NA	196.8
10MHz	**212.3**	**206.4**	211.3	213.8	210.7	219.7	212.3	210.5	198.3	205.4	209.3	216.3	204.8

†FoM= $|PN|+20\ log_{10}(\omega_0/\Delta\omega)$-10 $log_{10}(P_{DC}/1mW)$ ††FoMA= $|PN|+20\ log_{10}(\omega_0/\Delta\omega)+10log(1mm^2/A)$-10 $log_{10}(P_{DC}/1mW)$

†††FoMAT= $|PN|+20\ log_{10}(\omega_0/\Delta\omega) +20\ log_{10}(TR/10)+10log(1mm^2/A)$-10 $log_{10}(P_{DC}/1mW)$

¹ Including bias circuitry. ² Before frequency division.

total TR of 63%. However, measurements show that DM oscillator is tunable between 3.37–5.32 GHz (45% TR) and the CM oscillator is tunable between 5.02–5.96 GHz (17% TR) and the overlap between the DM and CM oscillations is wider than expected, resulting in a tuning range of 55.5%.

Figure 12 shows PN at f_{max} and f_{min} frequencies of the DM and CM oscillations. In both modes, V_{DD} is 1.1V. Figure 12 also reports the PN and FoM of this oscillator over the tuning range. The FoM increases from 188.2 dB to 189.4 dB in the DM and from 181.3 dB to 182.3 dB in the CM tuning ranges. The PN in the CM mode is worse than in the DM mode, but it is worth mentioning that not all applications demand ultra-low phase noise in all bands and channels uniformly.

Table I also compares FoMA, introduced in [31], of the proposed oscillator with other relevant oscillators. The DM oscillator shows the best FoMA and the CM oscillator's FoMA is comparable with the other state-of-the-art oscillators.

A. Supply and Ground Routing Inductances and Losses

The measurement results deviate from the simulations and theory in two ways. The first is the wider overlap between the DM and CM oscillation frequencies. The second is the degraded PN in the CM Colpitts oscillator. To explain the performance degradation, we first take a closer look at a layout of the transformer-based tank. As revealed in Fig. 13, the CM inductance should also include the impedance of the current return route, from the center-tap of the primary winding to the sources of M_{4a} (M_{4b}). The de-coupling capacitors together with the RLC routing network present an equivalent impedance that is inductive but its real part adds to the circuit losses. Therefore, unless the return current path happens to resonate at the same oscillation frequency (through the equivalent inductances and decoupling capacitors along it), the CM oscillation shifts down from the expected value, which
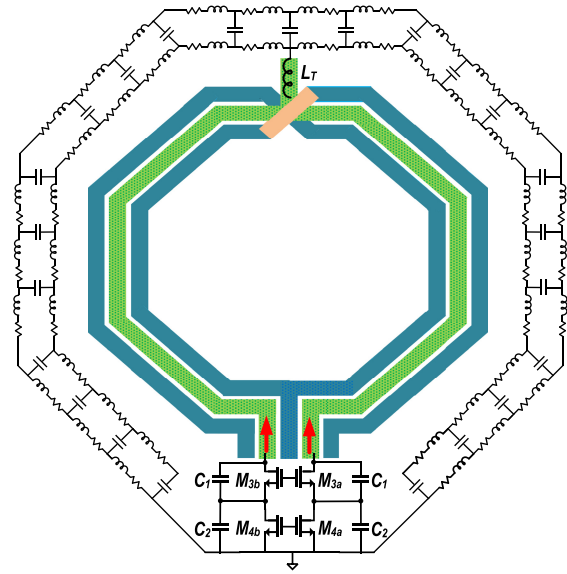

Fig. 13. Return current path in the 1:2 transformer.

is precisely what we observe in our measurements. The DM oscillation frequency is not affected, therefore, the expected TR is decreased. Furthermore, the losses in the return path are added to the losses of the primary inductor, thus degrading the quality factor of the tank. The long return path causes the losses to be comparable to the inductor's loss and this jeopardies the CM start up. Furthermore, this path also partially cancels the magnetic field of the inductor, thus degrading its Q-factor. The severe PN degradation compared to the simulation results gives thus credence to the Q degradation of the tank. Our EM simulations predict a 0.25 Ω resistance in this path and circuit simulations show that such resistance in series with the primary inductor would degrade the CM oscillator phase noise by 4 dB. This appears to agree with our measurements.

One possible solution would be employing a 2:1 transformer. A 2-turn primary inductor will have its supply connection node very close to the transistors; therefore the current return path would not be very long, thus minimizing the path inductance. However, in that transformer, the CM current in the two windings of the primary inductor has opposite direction, thus cancelling each other's flux [30]. Consequently, the CM primary inductance would be smaller than the DM one. The spacing between the transformer windings should be chosen properly to satisfy the overlap condition for the reasonable capacitor bank C_{on}/C_{off} ratios.

V. CONCLUSION

In this paper, we introduced a technique to extend a tuning range (TR) of an LC-tank oscillator without significantly increasing its die area. A strongly coupled 1:2 turns-ratio transformer-based tank is normally excited in a differential mode (DM), where it achieves the TR of 45% with a good FoM of 188.2–189.4 dB. The TR is extended by exciting the tank in common mode (CM) with two locked Colpitts oscillators. The proposed oscillator is implemented in 40-nm CMOS and delivers the total TR of 55.5% while constraining the core die area to only 0.12 mm^2. Although the measured tuning range extension and phase noise (PN) in the CM mode were worse than theoretically predicted, we have identified the root cause as a current return route inductance that not only lowers the CM frequencies but also adds losses that result in a reduced Q-factor.

ACKNOWLEDGMENT

REFERENCES

[1] M. Carusol, M. Bassi, A. Bevilacqua, and A. Neviani, "Wideband 2–16 GHz local oscillator generation for short-range radar applications," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2012, pp. 49–52.

[2] J. Borremans, K. Vengattaramane, V. Giannini, B. Debaillie, W. Van Thillo, and J. Craninckx, "A 86 MHz–12 GHz digital-intensive PLL for software-defined radios, using a 6 fJ/Step TDC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2116–2129, Oct. 2010.

[3] Y. Chen, Y. Pei, and D. M. W. Leenaerts, "A dual-band LO generation system using a 40GHz VCO with a phase noise of −106.8 dBc/Hz at 1-MHz," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 203–206.

[4] L. Fanori, T. Mattsson, and P. Andreani, "A 2.4-to-5.3 GHz dual-core CMOS VCO with concentric 8-shaped coils," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 370–372.

[5] Z. Safarian and H. Hashemi, "Wideband multi-mode CMOS VCO design using coupled inductors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1830–1843, Aug. 2007.

[6] S.-M. Yim and K. O. Kenneth, "Demonstration of a switched resonator concept in a dual-band monolithic CMOS LC-tuned VCO," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2001, pp. 205–208.

[7] N. D. Dalt, E. Thaller, P. Gregorius, and L. Gazsi, "A compact triple-band low-jitter digital LC PLL with programmable coil in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1482–1490, Jul. 2005.

[8] Z. Li and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1296–1302, Jun. 2005.

[9] D. Hauspie, E. C. Park, and J. Craninckx, "Wideband VCO with simultaneous switching of frequency band, active core, and varactor size," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1472–1480, Jul. 2007.

[10] N. T. Tchamov, S. S. Broussev, I. S. Uzunov, and K. K. Rantala, "Dual-band LC VCO architecture with a fourth-order resonator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 3, pp. 277–281, Mar. 2007.

[11] A. Buonomo and A. L. Schiavog, "Analysis and design of dual-mode CMOS LC-VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1845–1853, Jul. 2015.

[12] A. Italia, C. M. Ippolito, and G. Palmisano, "A 1-mW 1.13–1.9 GHz CMOS LC VCO using shunt-connected switched-coupled inductors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 6, pp. 1145–1155, Jun. 2012.

[13] B. Sadhu, J. Kim, and R. Harjani, "A CMOS 3.3–8.4 GHz wide tuning range, low phase noise LC VCO," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2009, pp. 559–562.

[14] W. Deng, K. Okada, and A. Matsuzawa, "A 25 MHz–6.44 GHz LC-VCO using a 5-port inductor for multi-band frequency generation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2011, pp. 1–4.

[15] S. Rong and H. C. Luong, "Analysis and design of transformer-based dual-band VCO for software-defined radios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 449–462, Mar. 2012.

[16] A. El-Gouhary and N. M. Neihart, "An analysis of phase noise in transformer-based dual-tank oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 2098–2109, Jul. 2014.

[17] J. Yin and H. C. Luong, "A 57.5–90.1-GHz magnetically tuned multimode CMOS VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1851–1861, Aug. 2013.

[18] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2943–2955, Dec. 2011.

[19] G. Li and E. Afshari, "A distributed dual-band LC oscillator based on mode switching," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 1, pp. 99–107, Jan. 2011.

[20] G. Li, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, Jun. 2012.

[21] M. Taghivand, K. Aggarwal, and A. S. Y. Poon, "A 3.24-to-8.45 GHz low-phase-noise mode-switching oscillator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 368–370.

[22] F.-W. Kuo *et al.*, "A 12 mW all-digital PLL based on class-F DCO for 4G phones in 28 nm CMOS," in *IEEE Symp. VLSI Circuits (VLSI) Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[23] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F_2 CMOS oscillator with 191 dBc/Hz FOM and long term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.

[24] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[25] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.

[26] A. Mazzanti and A. Bevilacqua, "On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2334–2341, Sep. 2015.

[27] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[28] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[29] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.

[30] D. Chowdhury, L. Ye, E. Alon, and A. M. Niknejad, "An efficient mixed-signal 2.4-GHz polar power amplifier in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1796–1809, Aug. 2011.

[31] B. Soltanian and P. Kinget, "A low phase noise quadrature LC VCO using capacitive common-source coupling," in *Proc. IEEE 32nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2006, pp. 436–439.

Mina Shahmohammadi (S'12–M'17) received the B.Sc. degree in communication systems from Amirkabir University of Technology, Tehran, Iran, in 2005, the M.Sc. degree in electronics from the University of Tehran, Tehran, Iran, in 2007, and the Ph.D. degree from Delft University of Technology (TU Delft), Delft, The Netherlands, in 2016.

From 2007 to 2011, she was with Rezvan Engineering Company, Tehran, Iran as an analog designer. She was a research assistant with the Electronic Instrumentation Lab at Delft University of Technology from 2011 to 2013, working on resistor based temperature sensors. She continued her PhD work in 2013 to 2016 in Electronics Research Laboratory at TU-Delft on wide tuning range and low flicker noise RF-CMOS oscillators. Dr. Shahmohammadi is currently an analog designer with Catena B.V., Delft. Her research interests are in analog and RF integrated circuits design.

Masoud Babaie (S'12–M'16) received the B.Sc. degree (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, and the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. (*cum laude*) degree from the Delft University of Technology, Delft, the Netherlands, in 2016.

In 2006, he joined the Kavoshcom Research and Develpment Group, Tehran, where he was involved in designing tactical communication systems. From 2009 to 2011, he was a CTO of the company. He was consulting for the RF Group , TSMC, Hsinchu, Taiwan, from 2013 to 2015, where he was involved in designing 28-nm all-digital PLL and Bluetooth low-energy transceiver chips. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA, with the Group of Prof. A. Niknejad. In 2016, he joined the Delft University of Technology as an Assistant Professor. His current research interests include analog and RF/mm-wave integrated circuits and systems for wireless communications.

Dr. Babaie was a recipient of the IEEE Solid-State Circuits Society Predoctoral Achievement Award in 2015–2016.

Robert Bogdan Staszewski (M'97–SM'05–F'09) was born in Białystok, Poland. He received the B.S. (*summa cum laude*), M.S., and Ph.D. degrees from the University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992, and 2002, respectively, all in electrical engineering. From 1991 to 1995, he was with Alcatel Network Systems, Richardson, TX, USA, where he was involved in SONET cross connect systems for fiber optics communications. He joined Texas Instruments, Dallas, in 1995, where he was elected as a Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was involved in advanced CMOS read channel development for hard disk drives. In 1999, he co-started a Digital RF Processor (DRP) Group within Texas Instruments, with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply-scaled CMOS processes. He was a CTO of the DRP Group from 2007 to 2009. In 2009, he joined the Delft University of Technology, Delft, The Netherlands, where he is currently a part-time Full Professor. Since 2014, he has been a Full Professor with the University College Dublin, Dublin, Ireland. He has authored or co-authored four books, five book chapters, and 210 journal and conference publications. He holds 160 issued U.S. patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters, and receivers.

Prof. Staszewski has been a TPC Member of ISSCC, RFIC, ESSCIRC, ISCAS, and RFIT. He is a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award.