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DOI
10.1109/EuroSimE60745.2024.10491576

Publication date
2024

Document Version
Final published version

Published in
Proceedings of the 2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)

2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) | 979-8-3503-9363-7/24/$31.00 ©2024 IEEE | DOI: 10.1109/EuroSimE60745.2024.10491576

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Abstract

Thermal management has always played a significant role in power module design. Double-sided heat dissipation is more efficient at transferring heat than the traditional package. Although there are several thermal modeling approaches to power modules, the application of the numerical models, which are computationally fast and accurate, has rarely been investigated for double-sided heat dissipation scenarios. This paper proposes a numerical heat conduction model of a double-sided heat dissipation power module with multiple chips embedded. The model was developed by solving Laplace's equation for the temperature distribution of steady state heat transfer using the separated variable method. The individual chip placement, two-chip distance and orientation, and four-chip placement were discussed through this modeling approach. The optimal layout was found. Then, a half-bridge topology module that consisted of two chips was investigated. To verify the accuracy of the numerical model, Finite Element Analysis (FEA) of the model was performed using the same boundary conditions. The experiments were applied on the power cycling tester to extract the junction temperature and case temperature. The numerical methods show good temperature prediction accuracy compared to both FEA and experiments.

1. Introduction

For efficient thermal management, it is essential to ensure stable and reliable operation of power devices. In different power electronics application scenarios, different heat dissipation methods are employed [1]. Power modules are core components in the energy conversion devices. The IGBTs or MOSFETs, which control the current flow, are the main heat sources. In the modules, heat is generated in the form of losses [2]. The resistance of the device on-state will cause conducting losses due to the electro-thermal effect. Additionally, the voltage increases before the current is completely turned off during the dynamic process, which results in switching losses. In addition, the body diode of the MOSFET would also increase the device temperature due to additional losses caused by its on-resistance.

Excessive temperatures would threaten the reliability of the device and system [3,4]. The performances of the semiconductor chips [5–7] (e.g., the threshold voltage, on-resistance, and forward voltage drop) are strongly affected by temperature. The lifetime of devices operating at high temperatures for long periods can be significantly reduced. The carriers in silicon would step under high temperature, which causes device breakdown. For packages, high temperatures can make the bonding wire and connecting layer crack [8].

In addition, because the encapsulated materials have different coefficients of thermal expansion, they are challenged by stresses at high temperature [9]. Considering these factors, chip manufacturers have limited the maximum junction temperature in datasheets. To fully utilize SiC potential characteristics, double-sided heat dissipation demonstrates better thermal management than the traditional design does. Currently, there are various packaging options for double-sided thermal modules [10]. Compared to the commercial power module, the DBC (Direct Bond Copper)-stacked hybrid packaging structure can reduce the voltage overshoot by 55% [11,12]. PCB-embedded fabrication technology also provides an approach to reducing the power dissipation and increase the switching frequency [13,14]. Excellent electrical and thermal performance has brought attention to double-sided thermal packages.

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The performance and practical applicability of thermal monitoring strongly depends on the chosen temperature-sensing approach, modeling and control methods [15]. Fast and accurate temperature prediction is also important in the design stage. Material parameters and structural dimensions have an important influence on the heat transfer. At present, two thermal modeling approaches are developed. The first approach equalizes the thermal path as an electric circuit. The solution is performed using the thermal resistance and heat capacity. This method generally requires a finite element simulation first to obtain the hear flux curve. Then, the time-efficient analytical method is used to calculate the RC parameters for the 3-D physical RC network model [16]. The thermal network of the traditional Cauer model can be obtained from the structure function [17]. The cross-coupling effects among multiple heat sources can be analyzed [18]. Through polynomial fitting, the RC parameters of the Foster network model can be modeled as a function related to the degradation degree of base solder [19]. This method identifies the heat source as a point. The temperature distribution on a continuous surface cannot be solved. The other temperature describe method is a formulation derivation based on the heat conduction equation [20,21]. The temperature equation for the one-sided heat dissipation in a steady state can be determined by solving the Fourier heat conduction equation [22]. The temperature solution for the two-sided heat dissipation model can be obtained by re-deriving the boundary conditions with specific modifications [23]. The transient temperature response can be solved using numerical solution methods. The coupled thermoelectric partial differential equations can be discretized using the finite volume method [24]. A thermal modeling tool based on the finite difference method can also be implemented to reduce the computational cost while maintaining a good accuracy of simulations for multichip power modules [25]. It is also possible to combine the analytical equations with the finite element method to evaluate the damage accumulated by a given load, which may be used to predict the lifetime or optimize the work points and module geometry [26]. Numerical methods enable the temperature distribution solution for all locations inside the structure. In this paper, a multichip module with double-sided heat dissipation will be investigated based on numerical heat conduction methods. In this work, numerical thermal modeling for multi-chip embedded is proposed. This method is applied to several cases to investigate the layout factors that would affect the junction temperature. The remainder of the paper is organized as follows: Section II illustrates the complete numerical derivation process. Section III analyzes the individual chip placement, two-chip distance and orientation, and four-chip placement. The location of the lowest junction temperature is determined. In Section IV, an embedded half-bridge module is investigated. Both finite element analysis (FEA) method and experiments are applied to verify the accuracy of the proposed numerical method. Finally, Section V summarizes the previous sections on model building and case study.

2. Double-sided power module thermal numerical modeling with multi chips

During the power module manufacturing process, each material is laminated in layers. In the horizontal plane, the materials are almost homogenous. Thus, the power module can be assumed as a rectangular block with different materials during modeling. Moreover, the chips are the components that generate heat due to the thermoelectric effect of the conductive resistance (R_{on}) and continuity of voltage changes. Fig. 1 presents the scheme of the proposed model. The origin of the coordinate system is the terminal point of the chip plane. As for the example of a module with two chips, the center coordinates of the chips are (x_{c1}, y_{c1}) and (x_{c2}, y_{c2}). The width and length of the chips are a and b, and the area is A_s. The width and length of the module are L_x and L_y, and the area is A_c. The heat generated by chip 1 and chip 2 is Q_1 and Q_2, respectively. In all, there are m layers of material on top of the chip. The thermal conductivity and thickness of each layer are k_{pm} and t_{pm} from the chip layer to the top surface. Similarly, k_{nn} and t_{nn} are the thermal conductivity and thickness of the layer underneath the chip with n layers in total.

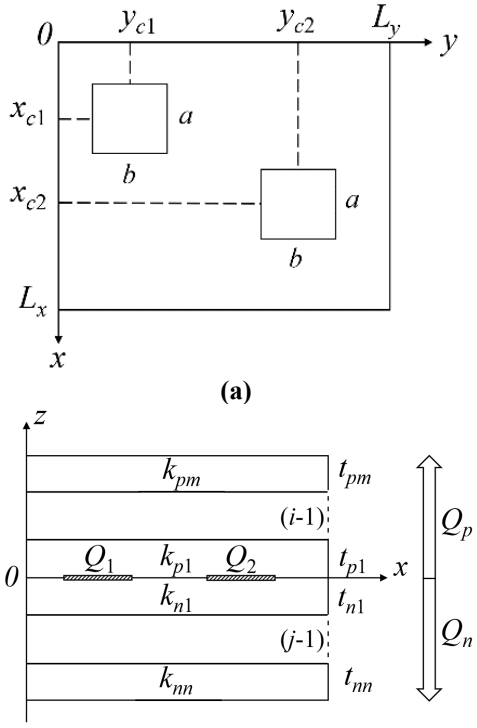

Figure 1: Double-sided power module with multi chips in the (a) front view; (b) side view

According to Fourier heat conduction equation (Eq. 1), an analytical equation for the temperature distribution in the module can be obtained (Eq. 2).

$$\nabla^2 T = \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \qquad (1)$$

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$$\theta(x,y,z) = A_0 + B_0 z + \sum_{m=1}^{\infty} cos(\lambda x)[A_1 cosh(\lambda z) + B_1 sinh(\lambda z)] + \sum_{n=1}^{\infty} cos(\delta y)[A_2 cosh(\delta z) + B_2 sinh(\delta z)] + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} cos(\lambda x)cos(\delta y)[A_3 cosh(\beta z) + B_3 sinh(\beta z)] \quad (2)$$

where $\lambda = m\pi/L_x$, $m = 1,2,3\cdots$, $\delta = n\pi/L_y$, $n = 1,2,3\cdots$, $\beta = \sqrt{\lambda^2 + \delta^2}$, and $B_i = \phi(\xi)A_i$, $i = 1,2,3$. In these equations, $T(x,y,z)$ is the temperature value in the module structure. The ambient temperature is set as T_{air}. $\theta(x,y,z)$ is the increase in temperature in the module.

The parameters in this general solution (Eq. 2) of Laplace's equation can be determined by specific boundary conditions. Considering the application of double-sided heat sink modules, five boundary conditions are implemented: (1) the surrounding area of this module is adiabatic; (2) the heat is transferred to the outside by convection from the top and bottom surfaces; (3) the ambient temperature is constant; (4) the temperature and power density are identical in the middle of different layers; (5) the chip area generates heat, and the remaining area of the chip layer conducts the heat in accordance with Boundary 4. For one heat source, the parameters of the chip layer can be expressed as:

$$A_{1.p} = \frac{\int_0^{L_x} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\lambda)\lambda}\cdot cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx} = \frac{\int_{x_c-\frac{a}{2}}^{x_c+\frac{a}{2}} \frac{-Q_p/A_s}{\phi_p(\lambda)\lambda k_{pi}} cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx} + \frac{\int_{else} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\lambda)\lambda} cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx} = \frac{-2Q_p \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\left(\frac{1+h\frac{t_{sum}}{k_{nj}}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_x\,\phi_p(\lambda)\lambda^2 k_{pi}} \quad (3)$$

$$A_{2.p} = \frac{\int_0^{L_y} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\delta)\delta}\cdot cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy} = \frac{\int_{y_c-\frac{b}{2}}^{y_c+\frac{b}{2}} \frac{-Q_p/A_s}{\phi_p(\delta)\delta k_{pm}} cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy} + \frac{\int_{else} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\delta)\delta} cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy} = \frac{-2Q_p cos(y_c\delta)sin(\frac{\delta}{2}b)(\frac{1+h\frac{t_{sum}}{k_{nn}}}{A_c - A_s} + \frac{2}{A_s})}{L_y\,\phi_p(\delta)\delta^2 k_{pm}} \quad (4)$$

$$A_{3.p} = \frac{\int_0^{L_x}\int_0^{L_y} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\beta)\beta}\cdot cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x}\int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} = \frac{\int_{x_c-\frac{a}{2}}^{x_c+\frac{a}{2}}\int_{y_c-\frac{b}{2}}^{y_c+\frac{b}{2}} \frac{-Q_p/A_s}{\phi_p(\beta)\beta k_{pm}} cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x}\int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} + \frac{\iint_{else} \frac{\partial\theta_{Q_p}}{\partial z}\cdot\frac{1}{\phi_p(\beta)\beta} cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x}\int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} = \frac{-8Q_p cos(x_c\lambda)sin(\frac{\lambda}{2}a)cos(y_c\delta)sin(\frac{\delta}{2}b)(\frac{1+h\frac{t_{sum}}{k_{nn}}}{A_c - A_s} + \frac{2}{A_s})}{A_c\lambda\delta\,\phi_p(\beta)\beta k_{pm}} \quad (5)$$

where $A_{i.p}$ $(i = 1,2,3)$ depicts the temperature distribution on the top of the chip layer. To depict the lower side temperature $A_{i.n}$ $(i = 1,2,3)$ is expressed as:

$$A_{1.n} = \frac{2Q_n \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\left(\frac{1+h\frac{t_{sum}}{k_{pm}}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_x\,\phi_n(\lambda)\lambda^2 k_{nn}} \quad (6)$$

$$A_{2.n} = \frac{2Q_n \cos(y_c\delta)\sin\left(\frac{\delta}{2}b\right)\left(\frac{1+h\frac{t_{sum}}{k_{pm}}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_y\,\phi_n(\delta)\delta^2 k_{nn}} \quad (7)$$

$$A_{3.n} = \frac{8Q_n cos(x_c\lambda)sin(\frac{\lambda}{2}a)cos(y_c\delta)sin(\frac{\delta}{2}b)(\frac{1+h\frac{t_{sum}}{k_{pm}}}{A_c - A_s} + \frac{2}{A_s})}{A_c\lambda\delta\,\phi_n(\beta)\beta k_{pm}} \quad (8)$$

where Q_p is the heat transferred through the upper dissipation, and Q_n is the heat transferred through the lower dissipation. The convective heat transfer coefficient of the top and lower surfaces is h. t_{sum} represents the thickness of the entire module.

$$\phi_{psurface}(\xi) = -\frac{\xi sinh(\xi t_{psum}) + h/k_{p3} cosh(\xi t_{psum})}{\xi cosh(\xi t_{psum}) + h/k_{p3} sinh(\xi t_{psum})} \text{ with } \kappa = k_{p(i+1)}/k_{pi} \quad (9)$$

$$\phi_{nsurface}(\xi) = \frac{\xi sinh(\xi t_{nsum}) + h/k_{n3} cosh(\xi t_{nsum})}{\xi cosh(\xi t_{nsum}) + h/k_{n3} sinh(\xi t_{nsum})} \text{ with } \kappa = k_{n(i+1)}/k_{ni} \quad (10)$$

$$\phi_{pi}(\xi) = \frac{\kappa\left[sinh(\xi t_{sum}) + \phi_{p(i+1)}(\xi) cosh(\xi t_{sum})\right] \cdot cosh(\xi t_{sum}) - \left[cosh(\xi t_{sum}) + \phi_{p(i+1)}(\xi) sinh(\xi t_{sum})\right] \cdot sinh(\xi t_{sum})}{\left[cosh(\xi t_{sum}) + \phi_{p(i+1)}(\xi) sinh(\xi t_{sum})\right] \cdot cosh(\xi t_{sum}) - \kappa\left[sinh(\xi t_{sum}) + \phi_{p(i+1)}(\xi) cosh(\xi t_{sum})\right] \cdot sinh(\xi t_{sum})} \quad (11)$$

$$\phi_{ni}(\xi) = \frac{\kappa\left[\phi_{n(i+1)}(\xi) cosh(\xi t_{sum}) - sinh(\xi t_{sum})\right] \cdot cosh(\xi t_{sum}) + \left[cosh(\xi t_{sum}) - \phi_{n(i+1)}(\xi) sinh(\xi t_{sum})\right] \cdot sinh(\xi t_{sum})}{\left[cosh(\xi t_{sum}) - \phi_{n(i+1)}(\xi) sinh(\xi t_{sum})\right] \cdot cosh(\xi t_{sum}) + \kappa\left[\phi_{n(i+1)}(\xi) cosh(\xi t_{sum}) - sinh(\xi t_{sum})\right] \cdot sinh(\xi t_{sum})} \quad (12)$$

$$A_{i.pj} = A_{i.p(j-1)} \frac{cosh(\xi t_{psumi}) + \phi_{p(i-1)}(\xi) sinh(\xi t_{psumi})}{cosh(\xi t_{psumi}) + \phi_{pi}(\xi) sinh(\xi t_{psumi})} \quad (13)$$

$$A_{i.nj} = A_{i.n(j-1)} \frac{cosh(\xi t_{nsumi}) + \phi_{n(i-1)}(\xi) sinh(\xi t_{nsumi})}{cosh(\xi t_{nsumi}) + \phi_{ni}(\xi) sinh(\xi t_{nsumi})} \quad (14)$$

where ξ is replaced by λ, δ, or β. $\phi_{psurface}(\xi)$ and $\phi_{nsurface}(\xi)$ are the Fourier coefficient of the top and bottom layers. $\phi_{pi}(\xi)$ is the Fourier coefficient of the i^{th} layer in the positive direction; $\phi_{ni}(\xi)$ is the Fourier coefficient of the i^{th} layer in the negative direction. t_{psum} is the total thickness of all structures on top of the chip, and t_{nsum} is the total thickness of all structures under the chip. $A_{i.(p/n)j}$ is the value of A_i (i =1, 2, and 3) in the analytic solution of the j^{th} layer in the positive/negative direction. t_{psumi} is the total thickness of all structures from the chip to the i^{th} layer in the positive direction; t_{nsumi} is that in the negative direction.

From the previous derivation of the general analysis solution and parameter expression, the temperature of adjacent structural layers can be derived from each other. Due to the linear superposition of temperature rise, multi heat sources would result in:

$$T(x,y,z) = \theta_{Q_1}(x,y,z) + \theta_{Q_2}(x,y,z) + \cdots + \theta_{Q_i}(x,y,z) + T_{air} \quad (15)$$

Thus, the modeling of the multichip embedded power module is complete.

3. Optimal layout of multi-chip embedded modules

The thermal performance of multichip packages can be affected by various factors. To standardize the discussion cases in this section, all package structure and material parameters are in accordance with the half-bridge embedded module with double-sided heat dissipation investigated in this study. Table I shows the thermal properties of the module. To fulfill the layout requirements in the discussion case, it is assumed that the package size is 10 mm * 10 mm, and the chip size is 2 mm * 2 mm. The heat power of each die is 0.5 W.

3.1 Individual die placement in the package

The position of individual die in a fixed package size would affect the junction temperature because the small area surrounding the package is considered an adiabatic boundary. Therefore, the closer the die is to the edge of the package, the less effective it is in dissipating heat. The junction temperature of a single chip at three different positions is discussed separately as shown in Fig. 2. It can be seen that the junction temperature is the lowest when a single die is at the center of the package. When both sides of the die are close to the edge of the package, the junction temperature will rise to the highest, which is 18.35% higher than the junction temperature when the die is located in the package center. This indicates that the die should be placed away from the edge of the package for better heat dissipation.

3.2 Distance between two dies in the package

The distance between dies directly affects the thermal coupling intensity. Thermal coupling is basically the superposition of power of different heat sources. A larger distance between the chips corresponds to a weaker thermal coupling effect. When the heat power is less affected by other chips, the junction temperature is lower. However, in a limited package space, the distance between the chips cannot be infinitely increased. Further, considering the influence of the package edge in 3.1, the die cannot be excessively close to the edge of the package to reduce the junction temperature. Fig. 3 shows the results of the junction temperature when the distance between the centers of the dies is increasing. The two dies are in a symmetric position. The horizontal axis represents the

Table 1: Thermal properties of the components in the half-bridge module

Components	Modulus E (GPa)	Poisson ratio v	Coefficient of thermal expansion α (ppm/K)	Thermal conductivity k (W/mK)
Si MOSFET	131	0.3	4.1	124
Soldermask	/	/	45	0.2
Cu	110	0.34	18	401
Sn5Sb Solder	49	0.38	31	70
EMC molding	6	/	20	0.65

distance from the chip center to the package edge. A high junction temperature can occur due to the strong thermal coupling between the dies. When the distance between the dies increases, the thermal coupling effect is weakened, and the die junction temperature decreases. However, the junction temperature would raise again when the dies are closer to the edge of the package. The lowest junction temperature is 77.36°C, when the distance between chips is 5.34 mm. The distance between the die center and the package edge at this time is 1.33 mm.

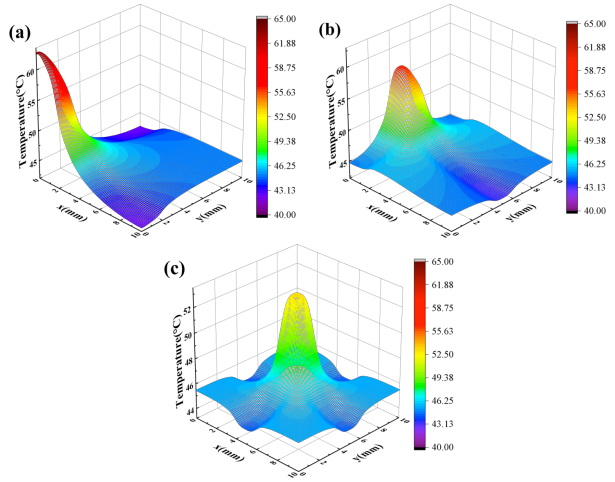
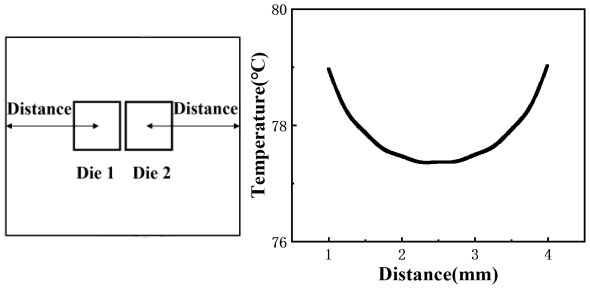


Figure 2: Numerical temperature modeling of the single-die placement: (a) two sides of the chip at the edge of the package; (b) one side of the chip at the edge of the package; (c) in the middle of the package.



(a) **(b)**

Figure 3: Schematic diagram of the symmetrical placement of two dies (a) layout; (b) junction temperatures.

3.3 Orientation of two dies

Considering the available die shape in the market, the shape may be used in packaging applications is rectangular. The placement of two rectangular dies can be categorized as long-side relative and short-side relative. Fig. 4 shows the results of two placements of a rectangular die on the junction temperature. The dimensions of the rectangular chip are 2 mm*1.5 mm. In the case of the short side relative, when the distance between the centers of the dies is 5.36 mm, the minimum junction temperature is 78.51°C, and the distance between the edge of the die and the edge of the package is 1.32 mm. In the case of the long side relative, when the distance between the centers of the dies is 5 mm, the minimum junction temperature is 78.72°C, and the distance between the edge of the die and the edge of the package is 1.75 mm. The short side relative case generally as a lower junction temperature than the long side relative. This result provides a guide to the placement of chips in practical applications.

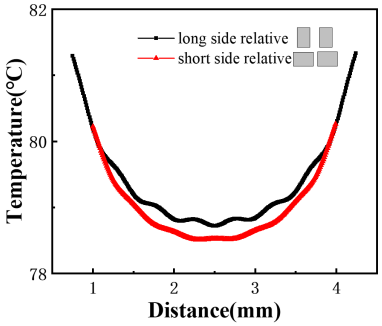
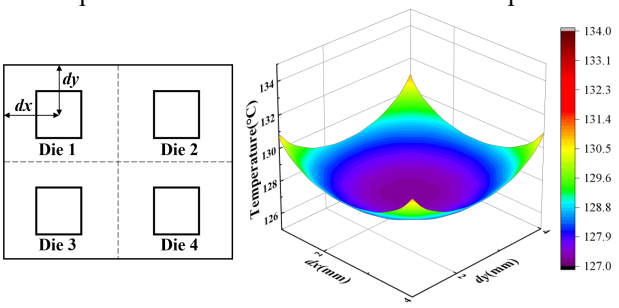


Figure 4: Junction temperature of the long side relative and short side relative.

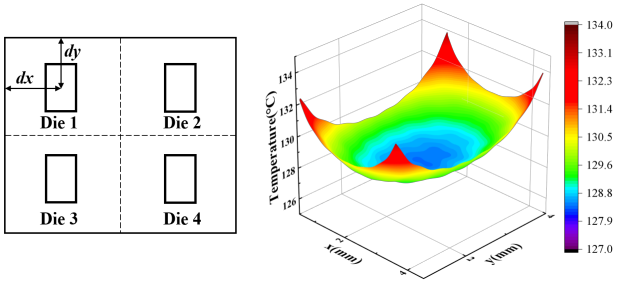
3.4 Distance among four dies in the package

When the number of the dies increases, the uniformity of the temperature distribution must be considered, especially in a paralleled topology. Differences in junction temperature will cause variations in the temperature-sensitive electrical parameters of each die. The electrical performance between paralleled dies would be affected as well. Therefore, to reduce the problem of uneven chip temperature, symmetric distribution is widely used in the multi-chip module layout. When four dies simultaneously generate heat, a fully symmetrical layout is used to make the temperature between the dies as uniform as possible.



(a) **(b)**

Figure 5: Schematic diagram of the symmetrical placement of four square dies (a) layout; (b) junction temperatures.



(a) **(b)**

Figure 6: Schematic diagram of the symmetrical placement of four rectangular dies (a) layout; (b) junction temperatures.

Fig. 5 and Fig. 6 show the junction temperatures at different locations for square chips and rectangular chips,

respectively. For the square die layout, when the die center is 2.36 mm from the package edge, the four dies have the lowest junction temperature of 127.195°C. For the rectangular die layout, when the die's long edge is 1.35 mm from the package edge and the die's short edge is 1.34 mm from the package edge, the four dies have the lowest junction temperature of 128.412°C.

4 Numerical modeling and experiments of a half-bridge module

To verify the feasibility of the proposed modeling approach in this paper, a 30 A two-chip embedded half-bridge module was adopted. The package size was 5 mm * 6 mm, and the chip size was 2.14 mm * 2.73 mm. In this case, the chips were crisscrossed. To imitate the device operating behavior, the high and low bridges turned on and off with 0.2 W power. The convection coefficient at this point was set to 100 W/(m2*K). The thickness of the entire package was 0.625 mm. The module is equivalent to an 8-layer structure in the numerical modeling. The thermal characteristics are also performed by FEA simulation. This half-bridge module was imported in COMSOL to extract the temperature at each position. All material parameters and the package structure were set to be identical. Fig. 7 and Fig. 8 show the temperature prediction results. Both numerical model FEA simulations show significant heat accumulation at chip area. Fig. 9 plots the results of the temperature predictions and errors of the two methods at six specific intercepts. The numerical model highlights the temperature difference between the two chips and the surrounding molding, whereas the finite element simulation weakens this phenomenon.

The data shows that the two methods have similar results. All errors of the numerical calculations are within 2%, with the data from the FEA as the reference. The accuracy and feasibility of the numerical prediction has been proven. For the coupled thermal field of multiple heat sources, both calculation methods show a consistent trend. The numerical calculation results show a noticeable temperature increase over the chip, and the finite element simulation shows a smoother temperature distribution.

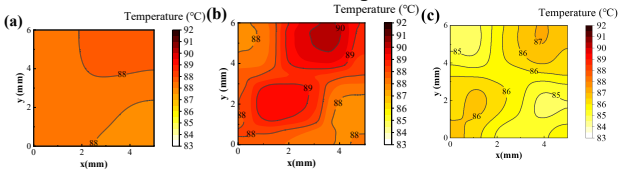


Figure 7: Numerical temperature modeling of a half-bridge module: (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.

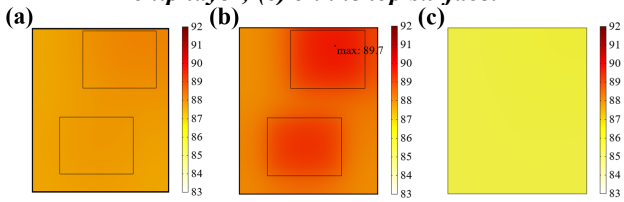


Figure 8: FEA temperature simulation of a half-bridge module: (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.

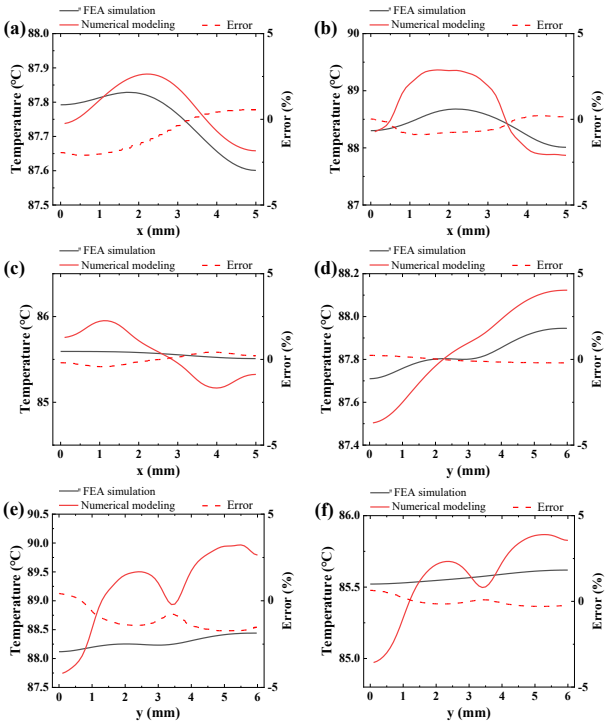


Figure 9: Half-bridge module temperature prediction and error distribution for the numerical model and FEA simulation on the bottom layer, die layer and top layer of the package with the line parallel to the (a) x-axis on the bottom layer, (b) x-axis on the die layer, (c) x-axis on the top layer, (d) y-axis on the bottom layer, (e) y-axis on the die layer and (f) y-axis on the top layer. Error refers to the error between numerical model and FEA simulation.

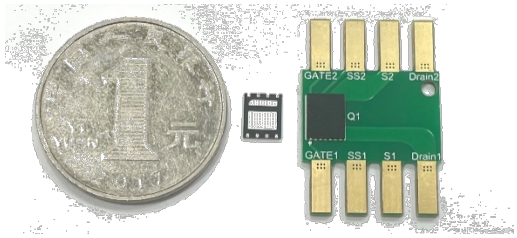


Figure 10: A 30-V/110-A half bridge MOSFET module.

To validate the accuracy of the numerical method, an experimental temperature test was conducted. A 30-V/110-A half-bridge MOSFET module was selected for the test. A PCB was soldered to lead out each electrode for easier pin connection. Fig. 10 shows the module and PCB substrate. The junction temperature and case temperature were simultaneously tested. The tested temperature data were compared with the numerical prediction to determine the reliability of the numerical method. Because the junction temperature data cannot be directly measured, it was necessary to measure the K-factor, which is the linear relationship between junction temperature and body diode voltage drop. After the heating process, the junction temperature was estimated by measuring the body diode voltage drop. A power cycle tester was used for the experiments. The tester integrated a K-factor test unit, a thermal resistance test unit, a driver circuit unit and a main power unit. The case temperature was captured using a

FLIR E96 infrared temperature tester. In this experiment, the upper and lower bridges of the half-bridge module were separately measured. The on-state current was set to be 1 A, and the hold time was 20 s. The bottom dissipated heat through the water-cooling substrate. The convective heat dissipation coefficient was considered 500 W/(m^2*K).

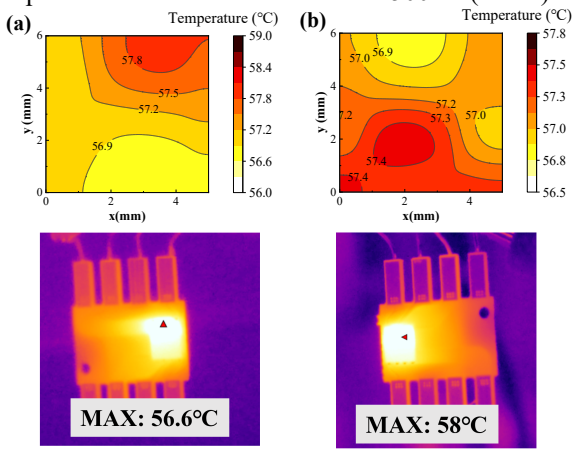


Figure 11: Comparison of numerical methods and experimental measurements of the case temperature: (a) upper bridge; (b) lower bridge.

Fig. 11 shows the infrared temperature test results of the upper and lower bridge. The input power of the upper die is 0.681 W, the k-factor is −1.98 mV/K, the junction temperature is 62.2°C, and the highest case temperature is 56.6°C. The input power of the lower die is 0.67 W, the k-factor is −1.87 mV/K, the junction temperature is 65.1°C, and the highest case temperature is 58°C. For the case temperature distribution, the numerical method errors for the maximum surface temperatures at the turn-on state for the upper and lower dies were 2.1% and 1%, respectively. The numerical methods predicted 61.5°C and 60.48°C for the junction temperatures of the upper and lower dies, respectively. The errors against the experimental data were 1.1% and 7%, respectively, which are less than 10% and prove the accuracy of the numerical method.

5 Conclusions

For the embedded multi-chip package, an accurate and efficient numerical calculation method was proposed. The temperature of each position in the multi-chip module can be quickly extracted by the formula. Firstly, applying the proposed method to optimize the multi-chip layout of embedded modules, an individual die should be placed near the center of the package layout to achieve the best heat dissipation. When arranging multiple chips, the thermal coupling between dies and the effect of the package edge distance on the junction temperature should be simultaneously considered. Rectangular dies need to account for the orientation when they are placed. The numerical results show that the junction temperature is minimal when the short side is relative to each other. Two dies and four dies should be symmetrically placed to obtain the best junction temperature balance. The location of the lowest junction temperature can be calculated by the numerical method. This method can be helpful for the chip layout during the module design process. Furthermore, the accuracy of the numerical method was verified by an embedded half-bridge module. The error is within 2% compared to the FEA simulation results. A power cycling tester was also used to validate the accuracy of the numerical method. Both junction temperature and case temperature were tested. The numerical method shows that the temperature prediction error was less than 10%, which demonstrates the feasibility of numerical methods.

Acknowledgments

This research was supported by the National Natural Science Foundation of China (Grant number: 52275559), the Shanghai Pujiang Program (Grant number: 2021PJD002), the Taiyuan Science and Technology Development Funds (Jie Bang Gua Shuai Program), and the Shanghai Science and Technology Development Funds (Grant number: 19DZ22534000).

References

1. An, Tong, et al. “Comparative Study of the Parameter Acquisition Methods for the Cauer Thermal Network Model of an IGBT Module.” Electronics, vol. 12, no. 7, Apr. 2023.
2. Chen, Cai, et al. “Flexible PCB-Based 3-D Integrated SiC Half-Bridge Power Module With Three-Sided Cooling Using Ultralow Inductive Hybrid Packaging Structure.” IEEE Transactions on Power Electronics, vol. 34, no. 6, June 2019, pp. 5579–93.
3. Choudhury, Khaled Redwan, and Daniel J. Rogers. “Steady-State Thermal Modeling of a Power Module: An N-Layer Fourier Approach.” IEEE Transactions on Power Electronics, vol. 34, no. 2, Feb. 2019, pp. 1500–08.
4. Delouei, AA, et al. “A Comprehensive Review on Multi-Dimensional Heat Conduction of Multi-Layer and Composite Structures: Analytical Solutions.” Journal of Thermal Science, vol. 30, no. 6, Nov. 2021, pp. 1875–907.
5. Eskandari, Soheila, et al. “Accurate Analytical Switching Loss Model for High Voltage SiC MOSFETs Includes Parasitics and Body Diode Reverse Recovery Effects.” 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 1867–74.
6. Heng, Ke, et al. “A 3-D Thermal Network Model for Monitoring of IGBT Modules.” IEEE Transactions on Electron Devices, vol. 70, no. 2, Feb. 2023, pp. 653–61.
7. Huang, Zhizhao, et al. “A High-Performance Embedded SiC Power Module Based on a DBC-Stacked Hybrid Packaging Structure.” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, Mar. 2020, pp.
8. Hung, Tuan-Yu, et al. “Life Prediction of High-Cycle Fatigue in Aluminum Bonding Wires Under Power Cycling Test.” IEEE Transactions on Device and

Materials Reliability, vol. 14, no. 1, Mar. 2014, pp. 484–92.
9. Kalker, Sven, et al. “Reviewing Thermal-Monitoring Techniques for Smart Power Modules.” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 2, Apr. 2022, pp. 1326–41.
10. Khazaka, R., et al. “Survey of High-Temperature Reliability of Power Electronics Packaging Components.” IEEE Transactions on Power Electronics, vol. 30, no. 5, May 2015, pp. 2456–64.
11. Klinkhamer, Corey, et al. “Jet Impingement Heat Sinks With Application Toward Power Electronics Cooling: A Review.” IEEE Transactions on Components Packaging and Manufacturing Technology, vol. 13, no. 6, June 2023, pp. 765–87.
12. Li, Wenyu, et al. “Double-Sided Numerical Thermal Modeling of Fan-out Panel-Level MOSFET Power Modules.” Case Studies in Thermal Engineering, vol. 52, Dec. 2023, p. 103763.
13. Liu, Yang, et al. “SiC MOSFET Threshold-Voltage Instability Under High Temperature Aging.” 2018 19th International Conference on Electronic Packaging Technology (ICEPT), 2018, pp. 347–50.
14. Lu, Xiaohui, et al. “Static and Dynamic Characteristics of SiC MOSFET under Extremely High Temperature.” 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 5605–10.
15. Pedersen, Kristian Bonderup, and Kjeld Pedersen. “Dynamic Modeling Method of Electro-Thermo-Mechanical Degradation in IGBT Modules.” EEE Transactions on Power Electronics, vol. 31, no. 2, Feb. 2016, pp. 975–86.
16. Pietranico, S., et al. “Thermal Fatigue and Failure of Electronic Power Device Substrates.” International Journal of Fatigue, vol. 31, no. 11, Nov. 2009, pp. 1911–20.
17. Race, Salvatore, et al. “Circuit-Based Electrothermal Modeling of SiC Power Modules With Nonlinear Thermal Models.” IEEE Transactions on Power Electronics, vol. 37, no. 7, July 2022, pp. 7965–76.
18. Savulak, Stephen, et al. “Three-Phase Inverter Employing PCB Embedded GaN FETs.” 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), 2018, pp. 1256–60.
19. Shi, Yunming, et al. “Dynamic IGBT Three-Dimensional Thermal Network Model Considering Base Solder Degradation and Thermal Coupling Between IGBT Chips.” IEEE Transactions on Transportation Electrification, vol. 9, no. 2, June 2023, pp. 2994–3011.
20. Wang, Huimin, et al. “A Thermal Network Model for Multichip Power Modules Enabling to Characterize the Thermal Coupling Effects.” IEEE Transactions on Power Electronics, 2024, pp. 1–21.
21. Wang, KJ, and ZL Pan. “An Analytical Model for Steady-State and Transient Temperature Fields in 3-D Integrated Circuits.” IEEE Transactions on Components Packaging and Manufacturing Technology, vol. 6, no. 7, July 2016, pp. 1028–41.
22. Yan, David, et al. “Time-Dependent Finite-Volume Model of Thermoelectric Devices.” IEEE Transactions on Industry Applications, vol. 50, no. 1, Feb. 2014, pp. 600–08.
23. Yang, Fei, et al. “Design of a Low Parasitic Inductance SiC Power Module with Double-Sided Cooling.” 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), 2017, pp. 3057–62.
24. Yang, Xin, et al. “Distributed Thermal Modeling for Power Devices and Modules With Equivalent Heat Flow Path Extraction.” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 6, Dec. 2023, pp. 5863–76.