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***Abstract*—Brain-computer interfaces of the future will be recorded from tens of thousands of high-density electrodes. This paper presents a neural amplifier for next-generation single-cell resolution BCIs. The amplifier leverages spatial signal correlation to introduce a novel shared DC servo loop to improve area efficiency while maintaining state-of-the-art power efficiency. Post-layout simulations in 40 nm CMOS technology achieve a 50 dB gain in a [0.1-5.2] kHz bandwidth. The amplifier consumes 920 nW and achieves a total input-referred noise of 8 μV_{rms} while occupying only 35µm×35µm per recording channel.**

***Index Terms*—Brain-computer interface (BCI), Neural amplifier, DC servo loop.**

I. Introduction

Brain-computer interfaces (BCIs) provide a direct link to the nervous system. The recorded neural signals can be used to control prosthetic devices or decode speech [1]–[3]. There is a push for increasing the number of channels in future BCIs, which poses challenges in the recording electronics [4]. Typically, the neural amplifier contributes most of the power and area consumption in multi-electrode array systems [5]–[10]. Most high-performing BCIs record action potentials (AP) from single neurons and use the spike train as input to the neural decoder. When recorded extracellularly, APs have a typical amplitude of 10-100 µV and a band of interest of 100 Hz to 5000 Hz. The recording amplifier needs to be low noise ($< 10\,\mu V_{rms}$) to accurately capture APs and low power ($< 1\,mW/mm^2$) to avoid tissue heating.

A trade-off exists between area consumption, power efficiency, and total integrated noise for the various architectures in the literature (Fig. 1). The AC-coupled capacitive feedback (CFN) amplifier requires a large input capacitance to set the gain accurately and large passives to set the high-pass pole, limiting chip area efficiency [9]. The CFN+T network achieves a similar transfer function with smaller capacitors but incurs a noise penalty due to the higher feedback resistor [11]. The AC-coupled open-loop amplifier (OLA) reduces input capacitor size but is susceptible to process variations [12], [13]. Mixed-signal DC servo loop (DSL) amplifiers can eliminate the need for input capacitors, offering area efficiency but require a digital-to-analog converter (DAC) to subtract the DC offset at the input, which might introduce a noise and

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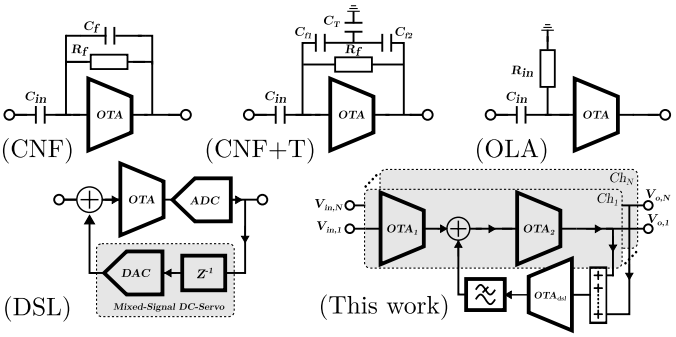
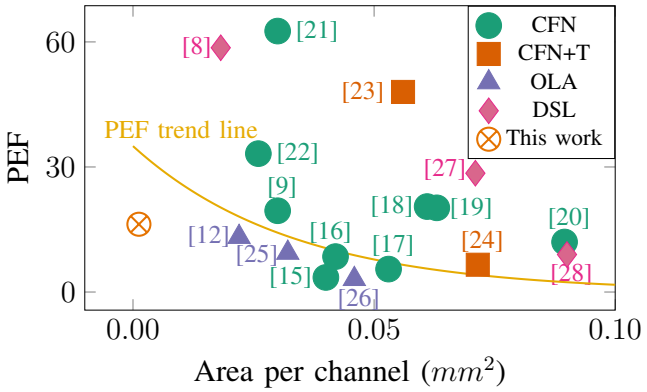


(a)



(b)

Fig. 1: A comparison of (a) amplifier architectures, (b) PEF vs. area/channel.

area penalty [8], [11], [14]. While the area of the amplifier is mainly influenced by its passive components and topology, the power consumption and noise performance are dominated by the operational transconductance (OTA). Inverter-based OTAs provide higher equivalent transconductance than differential pair OTAs, leading to better power efficiency factor (PEF) [29]. Amplifier stacking leverages current reuse to bias multiple OTAs, improving transconductance efficiency (g_m/I_D) and improving PEF [30]. Partially shared OTAs optimize area and power consumption but can lead to gain leakage and crosstalk, limiting sharing to a few channels [19].

This paper presents a novel 2 × 2 neural amplifier macro-pixel that uses a shared DSL to filter local field potentials

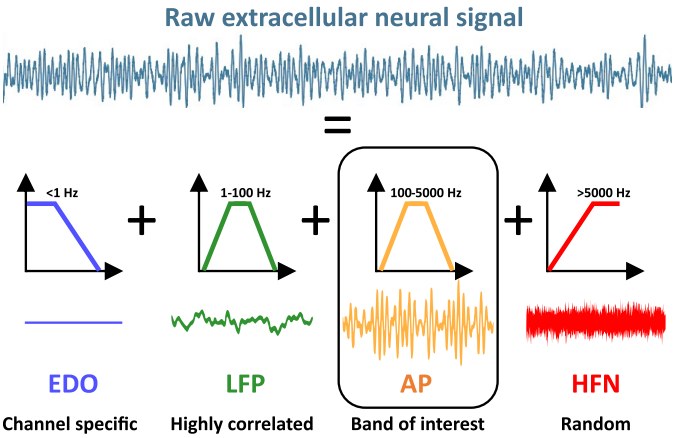


Fig. 2: Raw extracellular neural signal components.

(LFP) from all channels, reducing power and area consumption. The proposed shared DSL exploits the high correlation among LFP signals in high-density multi-electrode arrays. The amplifier uses a two-stage structure that allows the DSL integration after the second stage, effectively minimizing its noise contribution. The design achieves an area per channel of $35\,\mu\text{m} \times 35\,\mu\text{m}$, a gain of $50\,\text{dB}$ across a $100\,\text{Hz}$ to $5200\,\text{Hz}$ bandwidth, and a power consumption of $0.92\,\mu\text{W}$ per channel, demonstrating its suitability for single-cell resolution BCI applications.

II. Working Principle

A. Neural Signal Characteristics

The raw extracellular neural signal has four main components: a DC offset, the local field potential (LFP), action potentials, and wide-band noise (Fig. 2). A channel-specific electrode DC offset (EDO) that can be up to a few hundred mV is present due to electrochemical reactions at the tissue-electrode interface [31]. LFPs are low-frequency signals ($1\,\text{Hz}$ to $100\,\text{Hz}$) generated by the aggregated activity of nearby neurons. LFPs recorded from close electrodes show a high signal correlation [32]. For example, neural recordings from rats' neocortex indicate a correlation coefficient of 0.88 below $100\,\text{Hz}$ for adjacent electrodes at $22.5\,\mu\text{m}$ pitch [33]. APs are less correlated than LFP and benefit from high-density recording to perform spike sorting (i.e., assigning APs to putative neurons). Finally, wideband noise originates from the tissue, electrode impedance, and recording electronics. For the target application, the DC offset must be canceled or reduced to avoid saturating the amplifier, and a bandpass filter is needed to remove the LFP and high-frequency noise (HFN).

B. Proposed Amplifier Architecture

The proposed amplifier comprises two open-loop stages with 4-channel shared-OTAs (Fig. 3). The OTAs share the reference branch across four channels to save power and area consumption. Resource sharing is confined to $N_{\text{share}} = 4$ to limit gain leakage since there are limited benefits for $N_{\text{share}} > 4$ [19]. The first stage is AC-coupled to implement

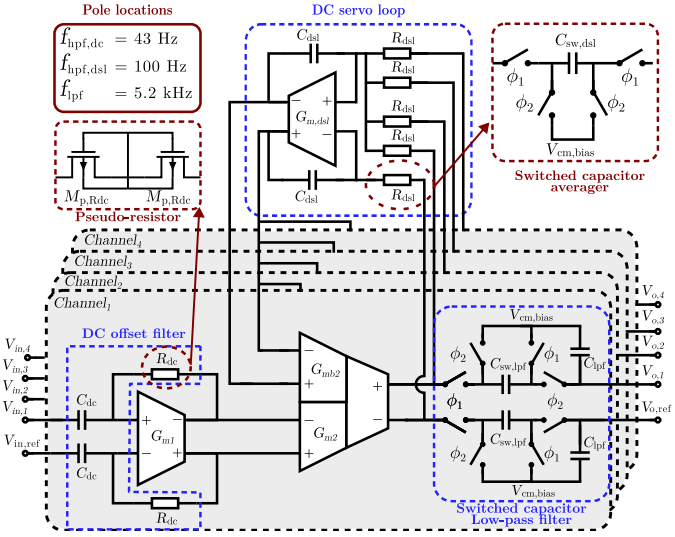


Fig. 3: Architecture of the proposed neural amplifier macro-pixel designed for single-cell resolution.

a DC-offset filter with the input capacitor and the feedback pseudo-resistor. To improve area efficiency, pseudo-resistors are used, which leads to process-dependent variations of the high-pass pole. However, this pole is set below the desired bandpass band and is only used to remove the DC-offset at the input of each channel. Hence, process-induced variations are not critical. The second stage uses a novel shared DSL across all four channels to set a pole at $100\,\text{Hz}$ and remove the LFP. The DSL is connected via the bulk terminal of the OTA input devices to avoid needing a dedicated subtraction node. Sharing the DSL across multiple nearby channels is possible because of the high correlation in the LFP band described before. The DSL uses a switched-capacitor low-pass filter (SC-LPF) to set the pole with high accuracy. Finally, a SC-LPF with a pole at $5\,\text{kHz}$ at the output stage removes high-frequency noise.

The shared-DSL approach is verified by comparing the output of the proposed architecture to a conventional architecture with an independent DSL on each channel. Fig. 4 shows the normalized mean squared error (NMSE) as a function of the signal frequency for a 60-second recording from [33] with a maximum NMSE of 0.031 in the frequency range $100\,\text{Hz}$ to $5000\,\text{Hz}$. This confirms the robustness of the proposed approach for the band of interest. Furthermore, we performed

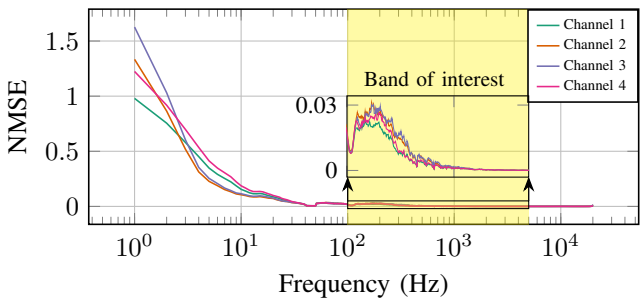


Fig. 4: Normalized Mean Squared Error (NMSE) for each channel obtained with the proposed shared DSL relative to the baseline without shared DSL.

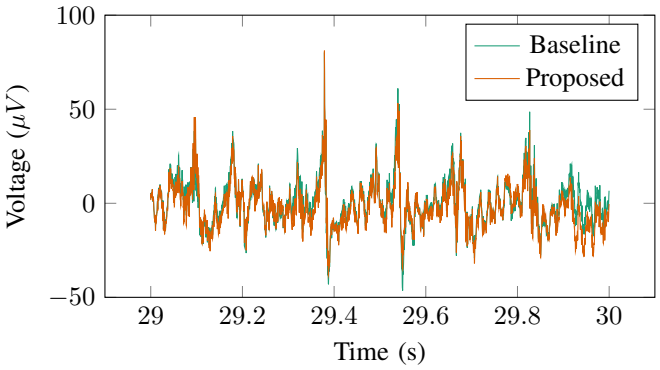


Fig. 5: A sample of a raw neural signal recorded using the proposed shared feedback and baseline amplifiers.

spike sorting in all four channels using wave_clus [34] on the baseline signal and the output of the proposed amplifier (see example of raw data in Fig. 5). Using the output of the spike sorting on the baseline signal as ground truth, this work achieves 99 % accuracy, which validates the ability to reconstruct APs faithfully from the output of the proposed amplifier.

III. Circuit Implementation

A. DC-offset and Output Low Pass Filters

A dedicated DC-offset filter for each channel provides rail-to-rail EDO rejection. The filter is a first-order passive high-pass filter formed by the input capacitor ($C_{\mathrm{dc}} = 624\,\mathrm{fF}$) and the feedback pseudo-resistor ($R_{\mathrm{dc}} = 53\,\mathrm{G\Omega}$) [35]. Although the pseudo-resistor may show resistance non-linearity with voltage changes, the expected small input range of APs makes this non-linearity negligible. However, the resistor value is influenced by process variations, leading to significant fluctuations in the high pass frequency ($f_{\mathrm{hpf,dc}} = \frac{g_{m1} r_{o1}}{2\pi C_{\mathrm{dc}} R_{\mathrm{dc}}}$). Consequently, to ensure consistency across process variations, $f_{\mathrm{hpf,dc}}$ was set below the desired bandpass transfer function [100:5000] Hz. Corner simulations result in a mean $f_{\mathrm{hpf,dc}}$ of 43 Hz with a standard deviation of 25 Hz.

A SC-LPF at the output removes high-frequency noise beyond 5 kHz. The SC filter operates at $f_{\mathrm{clock}} = 20\,\mathrm{kHz}$ and uses $C_{\mathrm{sw,lpf}} = 1.2\,\mathrm{pF}$ and $C_{\mathrm{lpf}} = 82\,\mathrm{fF}$.

Stacked capacitors, comprising an NMOS capacitor beneath a metal-oxide-metal (MOM) capacitor, are utilized for both filters to achieve high capacitance per unit area ($9\,\mathrm{fF}/\mu\mathrm{m}^2$) in the selected technology.

B. Gain Stages

Both OTAs are inverter-based and biased in weak inversion to maximize power efficiency (Fig. 6). The reference branch is shared among all channels to enhance power and area efficiency. The second stage utilizes body-controlled feedback through the body terminals of the input PMOS and NMOS devices to implement the DSL. The NMOS devices are placed in a deep n-well (DNW) structure to enable access to the body terminal. The maximum output voltage swing of the DSL is set to 300 mV to avoid forward biasing any junction. The

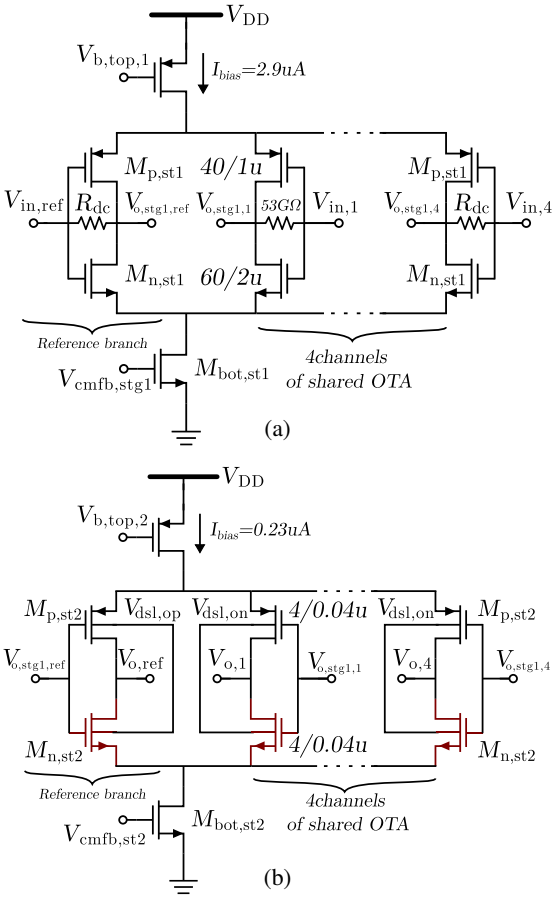


Fig. 6: Transistor level OTA implementation of (a) first gain stage and (b) second gain stage, with DNW transistors highlighted in red.

ratio between the body transconductance (G_{mb2}) and the large-signal transconductance (G_{m2}) is $\eta = 0.33$ in this technology. Hence, the DSL control range at the input of the second stage is 100 mV, which is sufficient in our application. A common-mode feedback (CMFB) circuit sets the common-mode output voltage to mid-supply for both OTAs.

The bias current is 2.9 µA and 227 nA for the first and second stages, respectively. The gain is 31.5 dB and 18.5 dB for the first and second stages, respectively, resulting in a total gain of 50 dB. The first stage contributes $6\,\mu\mathrm{V_{rms}}$ input-referred noise (similar thermal and flicker contributions), while the second stage contributes $1.3\,\mu\mathrm{V_{rms}}$ input-referred noise.

C. Switched Capacitor Shared DSL

The shared DSL sets a high-pass pole at $f_{\mathrm{hp}} = 100\,\mathrm{Hz}$. It uses a parasitic-insensitive SC analog integrator with four inputs to calculate the average low-frequency signal among all channels (Fig. 3). The resulting pole is determined by:

$$f_{\mathrm{hp}} = \left(\frac{2\pi}{f_{\mathrm{clock}}} \cdot \frac{C_{\mathrm{dsl}}}{C_{\mathrm{sw,dsl}}} \cdot |A_{\mathrm{dsl}}| \right)^{-1} \cdot (1 + A_2 A_{\mathrm{dsl}} \eta) \quad (1)$$

where A_{dsl} and A_2 represent the open-loop gain of the analog integrator and the second stage, respectively, $C_{\mathrm{sw,dsl}}$ and C_{dsl} are the input and feedback capacitors, respectively, f_{clock} is

the SC clock frequency, and η is the previously introduced transconductance ratio. When $A_2 A_{\text{dsl}} \eta \gg 1$, the required capacitance ratio can be rewritten as:

$$\frac{C_{\text{dsl}}}{C_{\text{sw,dsl}}} \approx \frac{A_2 \eta}{2\pi \frac{f_{\text{hp}}}{f_{\text{clock}}}} \tag{2}$$

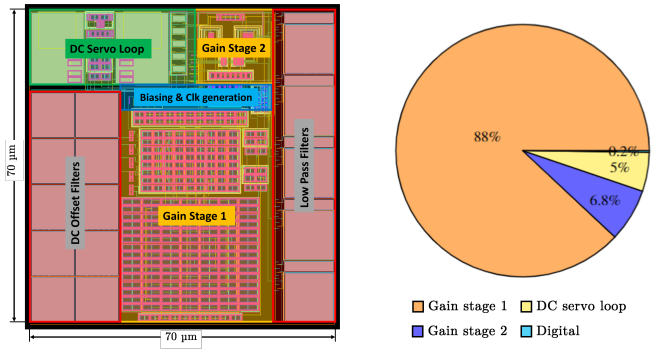
In the proposed design, $A_{\text{dsl}} = 28\,\text{dB}$, resulting in a sufficiently high $A_2 A_{\text{dsl}} \eta = 69\,\text{V/V}$. With $f_{\text{clock}} = 20\,\text{kHz}$, $C_{\text{sw,dsl}} = 10\,\text{fF}$, and $C_{\text{dsl}} = 970\,\text{fF}$, the resulting f_{hp} is at 90 Hz to allocate headroom for process variation. Low-threshold voltage NMOS devices are utilized for switches to enable large input voltage swings, and a CMFB circuit is also used to set the output common-mode voltage to mid-supply.

IV. Simulation Results

The proposed amplifier 2×2 macro-pixel was designed in a 40 nm CMOS technology and simulated post-layout (Fig. 7a). It occupies a total area of $70\,\mu\text{m} \times 70\,\mu\text{m}$, which results in an area per channel of $35\,\mu\text{m} \times 35\,\mu\text{m}$. The design consumes $1.24\,\mu\text{W}$ per channel from a 1.1 V supply voltage. The power consumption is dominated by the first gain stage, while the sharing mechanism makes the DSL power contribution only 5 % (Fig. 7b).

The amplifier achieves 50 dB of midband gain in a 0.1 kHz to 5.2 kHz bandwidth, a common-mode rejection ratio (CMRR) of 70.5 dB, and a power supply rejection ratio (PSRR) of 60.3 dB (Fig. 8). The shared-OTA structure introduces a channel crosstalk of $-47.4\,\text{dB}$ (Fig. 8), which is acceptable since AP are typically recorded with $6-8$ effective number of bits (ENOB) [4]. The total input-referred noise integrated from 10 Hz to 50 kHz is $8\,\mu\text{V}_{\text{rms}}$. The input-referred power spectral density is reported in Fig. 9.

Table I compares the proposed work (post-layout results) with state-of-the-art neural amplifiers that focus on APs. The proposed amplifier achieves the lowest area per recording channel while maintaining a competitive noise efficiency factor (NEF) and PEF.



(a) (b)

Fig. 7: (a) Final layout, and (b) the power consumption distribution of the amplifier.

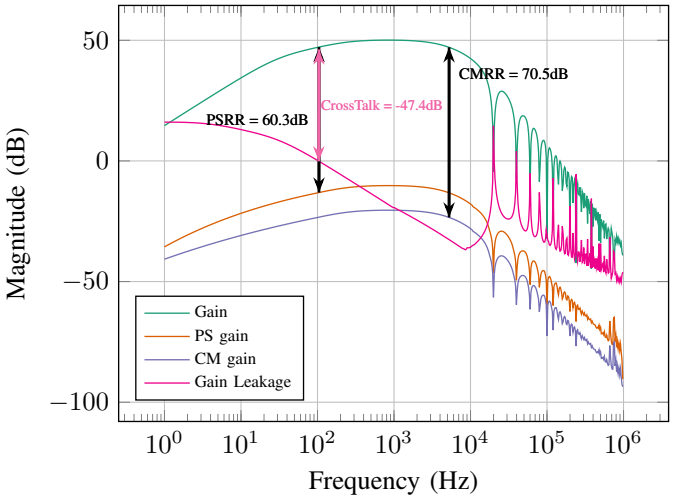


Fig. 8: Post-layout simulation results for the gain, CM gain, PS gain, and gain leakage with annotated CMRR, PSRR, and crosstalk.

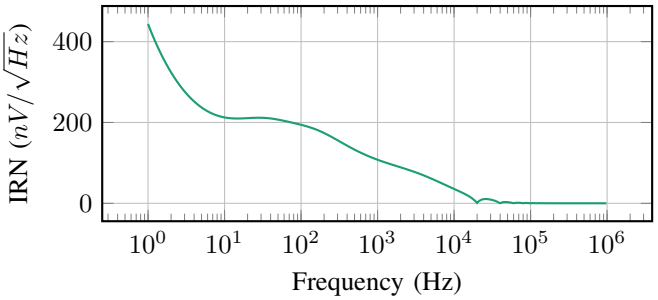


Fig. 9: Input referred noise voltage (IRN) power spectral density.

TABLE I: Performance summary and comparison with prior art.

Reference	TBCAS'11 [21]	BIOCAS'17 [12]	JSSC'17 [27]	TBCAS'21 [28]	JSEN'22 [22]	This work
Technology (nm)	180	180	40	180	180	40
Supply (V)	1.8	1.8	1.2	1.5	1.8	1.1
Bandwidth (Hz)	350-11.7k	300-10k	200-5k	200-5k	200-5k	100.6-5.3k
Area (mm2/ch)	0.03	0.022	0.071	0.090	0.026	0.001225
Gain (dB)	66	76.4	26	44	51	50
Power (uW/ch)	20	16	2	1.48	8.3	0.922
IRN (uVrms)	5.4	2.4	7	2.16	3.6	8
NEF	5.9	2.71	4.9	2.45	4.3	3.8
PEF	62.6	13.2	28.8	9	33.2	16.26
PSRR (dB)	72	-	-	-	78	60.3
CMRR (dB)	62	-	-	140	117	70.5

V. Conclusion

This paper addresses the need to improve area efficiency in neural amplifiers for future massively parallel BCI applications. We propose a 2×2 macro-pixel amplifier with a shared DC servo loop that leverages spatial signal correlation to reduce resources and improve area efficiency. The amplifier achieves 50 dB of mid-band gain in a 0.1 kHz to 5.2 kHz bandwidth, a total input-referred noise of $8\,\mu\text{V}_{\text{rms}}$ and consumes only $920\,\text{nW}$ per channel and $35\,\mu\text{m} \times 35\,\mu\text{m}$ per channel.

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