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Effects of die top system and trenches on large thin die mechanical robustness

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Abstract

Power MOSFET dies in the automotive industry are becoming larger (>5 × 5 mm) and thinner (<50 μm) to meet high-performance and lifetime requirements. Ensuring the mechanical robustness of these large ultrathin chips is crucial for reliable electronic devices and high-throughput packaging processes. The high aspect ratio and advanced chip designs incorporating trench technology present significant challenges in semiconductor assembly, packaging, and testing. This paper introduces an experimental front-end strategy aimed at strengthening the front side (FS) of large ultrathin dies using various die-top systems. Industry-equivalent 50 μm thick dummy power MOSFET dies were fabricated to evaluate the efficacy of different chip designs and materials, such as polyimide (PI), in mitigating fracture risks. Fabrication-induced stresses and warpage in the device layers were measured using a thin-film stress measurement tool. Additionally, the FS strength of the ultrathin dies was assessed using the three-point bending method, with the resulting data analyzed via two-parameter Weibull distribution plots. Results demonstrated that the deposition of 5 μm PI on the nitride die topside significantly increased die strength from 339 MPa to 760 MPa, with 5 μm PI proving more effective for die strengthening than 10 μm. The interaction between the metal-trench layer and the die was found to be critical to the robustness of ultrathin dies, influenced by the pattern and layout of the trenches. Die-top metallization designs, such as meandering patterns, showed promising improvements in die strength compared to standard designs. A proposed chip layout aims to maximize PI coverage for clip-bonded products on the die topside, leveraging its strengthening effect. The study also demonstrated that dummy reference chips can facilitate rapid and straightforward evaluation of extensive design experiments to identify robust chip designs.

Keywords: power MOSFET, large ultra-thin dies, die crack, trench, polyimide, three-point bending, Weibull distribution

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1. Introduction

Driven by environmental concerns and the need to reduce carbon emissions, the automotive industry is rapidly shifting from fossil fuel to electric-based transport. Highly efficient power MOSFET semiconductors play a key role in this energy transition process. Thinning the substrate effectively shortens the distance between the source and drain in vertical Si-based power MOSFET. This reduction in die thickness can result in a lower on-state resistance (R_{DSON}) and switching losses, improving the conduction efficiency of the MOSFET [1]. In high-power MOSFET packaging, advanced thermal management is of prime importance; therefore dies become thinner as thinner substrates allow the heat generated during operation to be conducted more effectively to the environment. Thinning the substrate also contributes to improving the die-attach solder fatigue, thus improving the overall device lifetime and reliability [2–4]. A larger die enhances the overall current carrying capacity. Therefore, large thin dies are essential to achieve high heat dissipation and increased power densities.

In addition, ultrathin dies find applications in various critical semiconductor technologies such as 3D device integration, wherein ultrathin dies (10–50 μm) are essential for enabling the vertical stacking of different functional chips ranging from memory, logic, analog, processing, and power ICs [3, 4]. Memory chips are becoming thinner and more efficient in data storage. Thin die technology, in combination with hybrid Cu bonding technology, enables the next generation of high bandwidth memory chips [5, 6]. This development is crucial to address the ever-increasing data consumption and mitigate memory storage bottlenecks in data centers.

Other technologies, such as flexible electronics in smartcards, flexible displays [7], embedded chips in hybrid system-in-foil (SiF), and miniaturization of biomedical chips for video endoscopes and subretinal implants also benefit from advancements in ultrathin chips.

However, as newer generations of power MOSFET dies become larger (>5 $\times$ 5 mm) and thinner (<50 μm), they are becoming increasingly fragile. High stress concentrations during the pick-up process, packaging, or testing result in an increased risk of fractures in dies which can potentially lead to yield losses in manufacturing. This is because the large die aspect ratio (lateral dimension/thickness), in combination with extensive back-end assembly processes, such as wafer backside grinding (BSG), dicing, die pick up, and place can induce high dynamic or residual stresses on fragile dies. The fracture strength of ultrathin dies is affected by various factors, including complex device structures such as deep trenches, the surface roughness of the die's backside (BS) and edges, and non-uniformities. These conditions can serve as potential locations for the initiation of cracks, thereby influencing the overall structural integrity of the ultrathin die. In a high-production assembly environment, thinner dies exhibit a higher frequency of rejection owing to dietop cracking resulting in high yield loss. At present, sophisticated and expensive packaging techniques are utilized in the industry to minimize die cracks and yield losses in backend processes and thus achieve high throughput with a 5-sigma yield. A few advanced dicing techniques such as dicing before grinding [3, 8], stealth dicing [9], and ultrafast laser dicing [10] have been employed to minimize sidewall damage and chippings on die edges to improve die strength. Similarly, methods such as chemical etching and mechanical polishing are essential after wafer BSG, to mitigate the effect of surface roughness from the leftover groove marks of the grinding stone on die strength. In addition, advanced assembly tools wherein ejector needles and pickup collet are optimized for their position, geometry, and forces are used, in combination with special dicing tapes to enable ultrathin die release for high-throughput pickup [8, 11, 12]. The majority of die-strengthening techniques as discussed, focus on the robust back-end assembly process, and very little work has been done to make dies inherently stronger in the front-end process. Due to dies becoming thinner, the backend process options to maintain a high robust yield are decreasing, and therefore, dies must be made more robust in front-end fabrication.

In this study, we present different front-end design approaches aimed at enhancing the frontside (FS) strength of ultrathin dies. This study investigated two distinct methodologies. The first approach involves utilizing different dietop metallizations and patterns to enhance the die strength and gain deeper insights into the interaction between the metal and trench layouts. The second approach focuses on the evaluation of polyimide (PI) as a potential die topside passivation material for increased die FS robustness. MOSFET dummy chips were prepared with different dietop systems and trench layouts, with a die thickness of 50 μm. The dummy chips are electrically inactive but closely resemble commercially available trench power MOSFET dies in terms of their layer distribution and mechanical robustness. The FS fracture strength of the ultrathin dies was characterized using a three-point bending (TPB) test, and a modified analytical equation was used to calculate die fracture strength to account for the composite die system. The measurement results for different chip designs were analyzed using Weibull distributions, and the effects of different dietop systems were compared and discussed.

2. Experimental procedure and results

2.1. Dummy unpatterned wafer preparation

Processed wafers were fabricated by adding different process layers on top of a silicon (Si) substrate. Different material layers offer varying mechanical properties, such as Young's modulus, fracture toughness, and yield stress. To understand the effect of adding different layers such as aluminium (Al), silicon oxide, and nitride on Si wafers, dummy wafers were fabricated without any patterns, and singulated dies were tested for their strength.

2.2. Fabrication of dummy power MOSFET wafers

To substitute for commercial power MOSFET dies, dummy power MOSFET wafers with FS Al, passivation layers, and

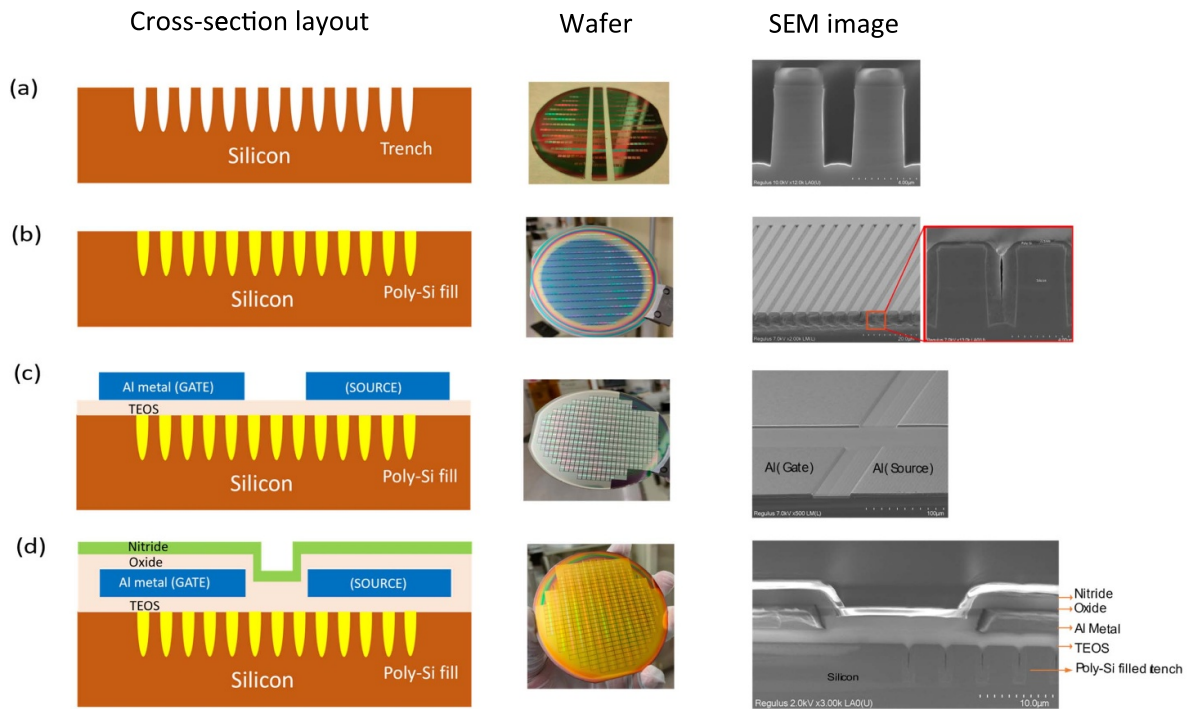


Figure 1. Process flow for dummy power MOSFET device fabrication. Processed wafers and cross-sections are shown. (a) Trench formation in silicon; (b) trenches are filled with poly-Si and etched back to remove excessive poly-Si from wafer top; (c) an insulating layer of TEOS, followed by pure Al is sputtered on top and patterned to form gate-source regions. (d) The metal top is covered with passivation films of oxide and nitride.

trenches were fabricated as shown in figure 1. Different metallization designs and layouts were patterned in the Al layer and trenches, respectively using a standard lithography process. The layer thicknesses of standard device layers, such as silicon nitride, oxide, and Al are kept the same to study the influence of different topside metallization patterns, new materials, and trench orientations. The substrates used for the power MOSFET sample fabrication were 100 mm diameter, single-side polished n-type Si wafers with 100 crystal orientation and an initial thickness of 525 ± 10 μm. An array of trench-power MOSFET devices was fabricated with a die size of 6×3 mm^2.

A wafer with dummy MOSFETs was prepared with an exact copy of the chip outline, design, and layer distributions, as in a commercial power MOSFET device. From this wafer, ultrathin dummy test dies was singulated and tested to define the baseline die strength for all other prepared samples. This allowed for a proficient evaluation of a large sample size to investigate the effect of different dietop systems, such as new metallization patterns, thick PI as a stress buffer, and trench layout variations to study their individual positive or negative influence on the robustness of ultrathin die's. This methodology has aided in accelerating research and development efforts in semiconductor manufacturing.

Vertical trenches are essential in power semiconductor devices because they minimize switching losses and enable the lowest Rdson devices by eliminating JFET regions and enabling high cell packing density compared to planar MOSFETs [13, 14]. New-generation power devices are packed with double-trench MOSFET structures wherein trenches are fabricated beneath the gate and source die area. The double-trench structure can also vary in its alignment, profile, and aspect ratio to meet the specific requirements of the region. In dummy power MOSFETs, deep trenches are essential to replicate the mechanical sensitivity of commercial MOSFETs, because they are critical spots for crack initiation and propagation in ultrathin silicon. The trenches in the dummy die were fabricated with similar grid structure alignment, wherein horizontally aligned trenches were patterned beneath the gate area (parallel to the long axis of the die), also known as snubber trenches and vertically aligned trenches beneath the source area (perpendicular to the long axis of the die), also referred to as active trenches (refer figure 2). The selection of the filling material, trench profile, and deposition technique determines the filling capability of the trenches.

In the dummy MOSFET die, the snubber and active trenches were fabricated with similar design aspects, featuring an aspect ratio of 2.5, height (h) of 5 μm, width (w) of 2 μm respectively, and pitch of 5 μm. The fabrication of dummy MOSFET wafers follows the commercial MOSFET layout and is designed to replicate its mechanical robustness as closely as possible. The key trench fabrication steps are described as follows:

- 2 μm thick patterned silicon oxide layer was used as the sacrificial layer for hard masking Si wafers. The mask offers good etch selectivity for Si (>8).
- The trenches were etched using a combination of dry and wet etching in a three-step process.

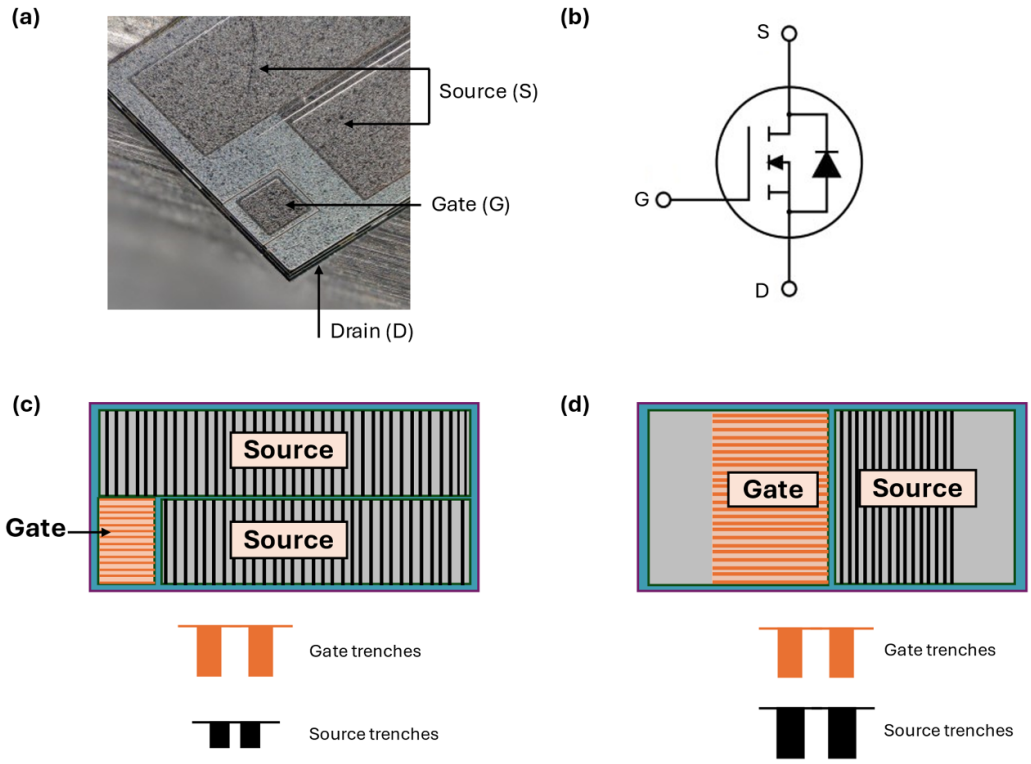


Figure 2. (a) Commercial power MOSFET chip, (b) N-channel power MOSFET schematic, (c) double-trench structure position and size comparison in commercial chips (b) versus fabricated test chip.

- o 95% of the total trench depth was etched in the first dry etching step using an inductively coupled plasma-reaction ion etching (ICP-RIE) in the Trikon Omega 201 tool with chlorine RIE chemistry.
- o This step left ∼220 nm wide silicon grooves at the trench opening (shown in figure 3(b)), and the oxide mask above the grooves was wet etched for 5 min in 0.55% hydrofluoric solution. The solution etches 200 nm oxide mask, exposing the protruding silicon grooves from both edges of the trench mouth.
- o The exposed silicon grooves and the desired trench depth were etched using another 15 sec ICP-RIE process.
- o Low-pressure chemical vapor deposition (LPCVD) was used to deposit polycrystalline silicon (poly-Si) and obtain highly conformal trench filling to minimize voids.

- The poly-silicon film outside the trench was etched back using the ICP-RIE method. During the etch-back step, the underlying silicon is protected by a thin 150 nm Tetraethyl Orthosilicate (TEOS) film.

The trench profile was optimized for minimum micro-trenching and filling voids by adjusting different parameters such as flow rate of reacting gases, pressure, time, and temperature [15]. Scanning electron microscopy (SEM) analysis of poly-Si filled trenches indicated a small filling void due to the presence of slightly curved sidewalls near the trench top, as shown in figures 3(a) and (b).

The fabricated trenches were covered with a uniform 2 μm thick TEOS insulation film using plasma-enhanced chemical vapor deposition (PECVD). 4 μm pure aluminium (Al) metal was sputtered on top and patterned using lithography to isolate the gate-source regions with a 50 μm straight line gap (refer to figure 4(a)). The Al metallization was covered with a combination of passivation layers such as silicon oxide (2 μm) and silicon nitride (1.4 μm) on a dietop to mimic an industry like passivation system. The MOSFET cross-section is shown in figures 3(c) and (d) and each layer's information is indicated in table 1.

2.3. New designs for robust gate and trenches

In a conventional trench power MOSFET, the gate occupies a small corner section, whereas the majority of the die area is occupied by the source. Fractures in ultrathin dies are dominantly observed to initiate around die edges, trenches and near die FS gate areas. To focus on the development of stresses and cracks near the gate area, the die outline design was adjusted to include an equal gate-source area as shown in figure 2. The tops Al layer was patterned with a 50 μm wide line gap to isolate gate-source metallization, as observed in commercial power MOSFETs. Figure 4 shows various fabricated die designs with new FS patterns and layer stacks as shown in table 2. These designs were evaluated on their influence on die FS strength and compare them with the reference test chip (Straight 50 μm line gap). The layouts were

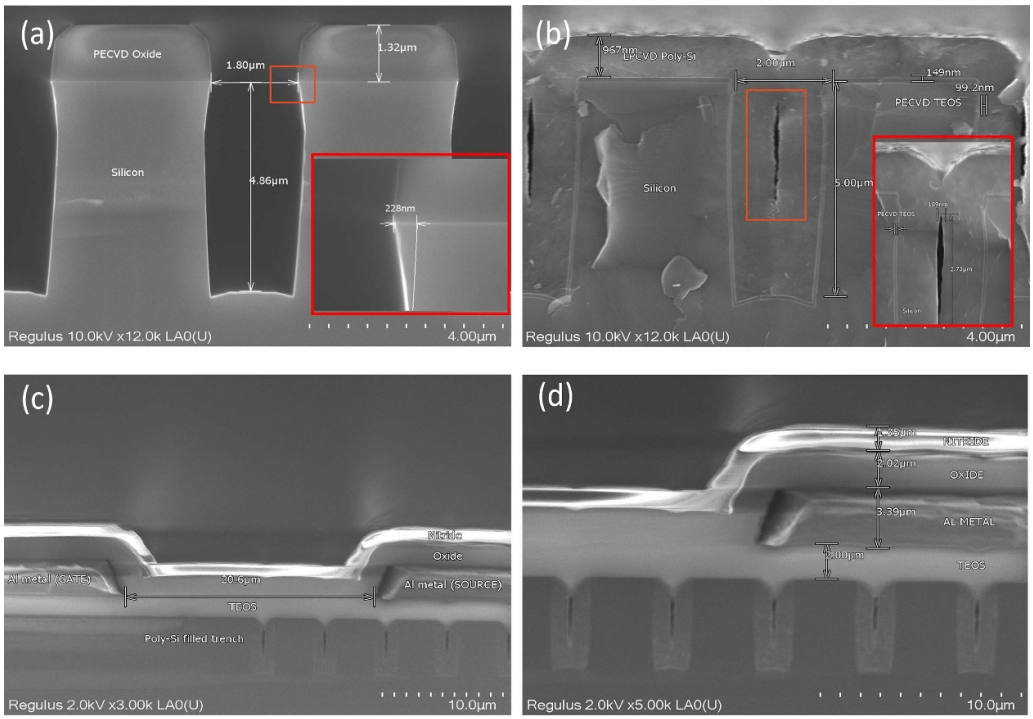


Figure 3. SEM image for wafer cross-section. (a) Hanging silicon groove in trench after dry etch step. (b) Trench void post poly-silicon filling. (c) Wafer cross-section showing MOSFET profile. (d) Close-up of the layer stack.

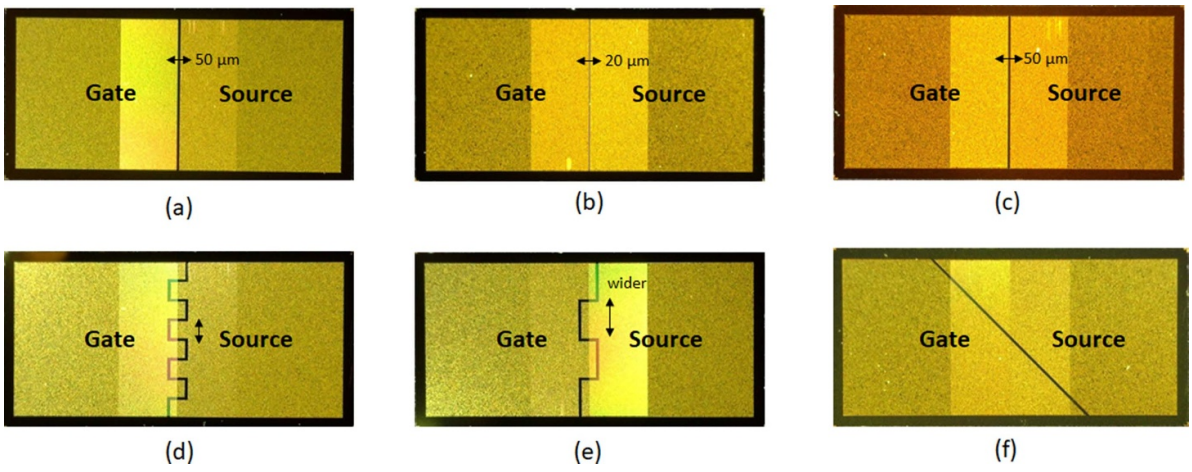


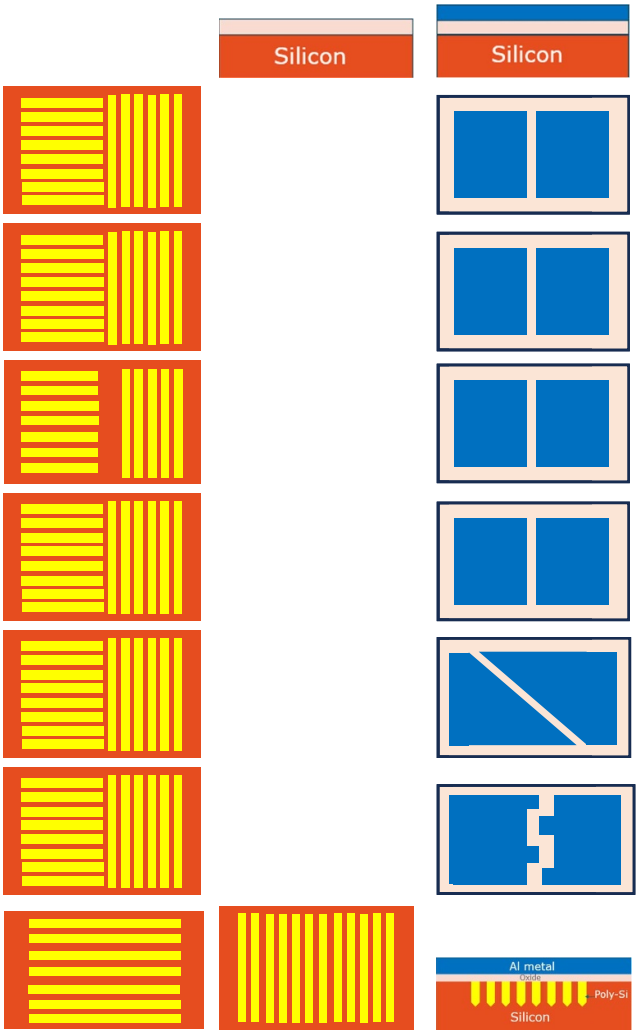
Figure 4. Die topside view showing (a) reference die with gate-source separation of 50 μm (b) gap reduced to 20 μm (c) die topside covered with PI (d) thinner meander pattern (e) meander pattern with wider metal area (f) 45° angled pattern separation.

Table 1. Different device layers and their fabrication method.

Device layer	Fabrication process	Film thickness
Trench profile	Dry + Wet etch	A.R: 2.5 (H/W: 5/2 μm)
Poly-Si trench fill	LPCVD	1 μm
TEOS (Oxide)	PECVD	2 μm
Pure Al	Sputtering	4 μm
Si oxide	PECVD	2 μm
Si Nitride	PECVD	1.4 μm
PI	Spin-coating	5 μm, 10 μm

Table 2. Design of experiments (DOE) for different fabricated samples. The table indicates different layer stacks, masks for trench and metallization patterns.

Layer stack	Trench	Oxide	Al metal	Nitride	Polyimide
Baseline samples		Silicon	Silicon		
Standard test chip					
Test die 1 Reduced gap to 20 μm					
Test die 2 No trenches in isolation gap					
Test die 3 PI for die top				T1: 5 μm T2: 10 μm	
Test die 4 Angled					
Test die 5 Meander					
Test die 6 Mono trenches					



designed to counter the crack propagation along the metal-free region. The new chip designs investigated in this study were as follows:

(a) Different insulation gaps of 20 μm and 50 μm between the gate and source area metallizations (refer to figures 4(a) and (b))
(b) Meander paths with different sizes to replace straight-line insulation path. (Figures 4(d) and (e)). The meander design was investigated for its potential resistance to Hstraight-line crack propagation.
(c) 45-degree angled insulation line pattern to replace the straight line gap as shown in figure 4(f). This design aims to minimize the risk of exposed trenches as seen in the reference device. The exposed trenches were not covered by a metal layer.
(d) Trenches patterned in different orientations across gate and source regions with varying coverage areas. Trench layouts can help investigate their alignment effect on die strength during bending.
(e) Chips with a trench-metal system to evaluate the effect of the metal film on trench alignment and sensitivity.

Two distinct chip design strategies were employed to examine the trench-metal system. The first strategy evaluates die sensitivity introduced by high aspect ratio (HAR) trenches in ultrathin Si dies by comparing the die strength of non-patterned dies with Si + 2 μm oxide + 4 μm Al to dies with trenches etched in the silicon substrate. In the second strategy, wafers with trenches in the mono-direction oriented either horizontally or vertically along the die axis and sputtered with continuous Al layers were fabricated and tested to analyze their stress-handling capability during ultrathin die bending.

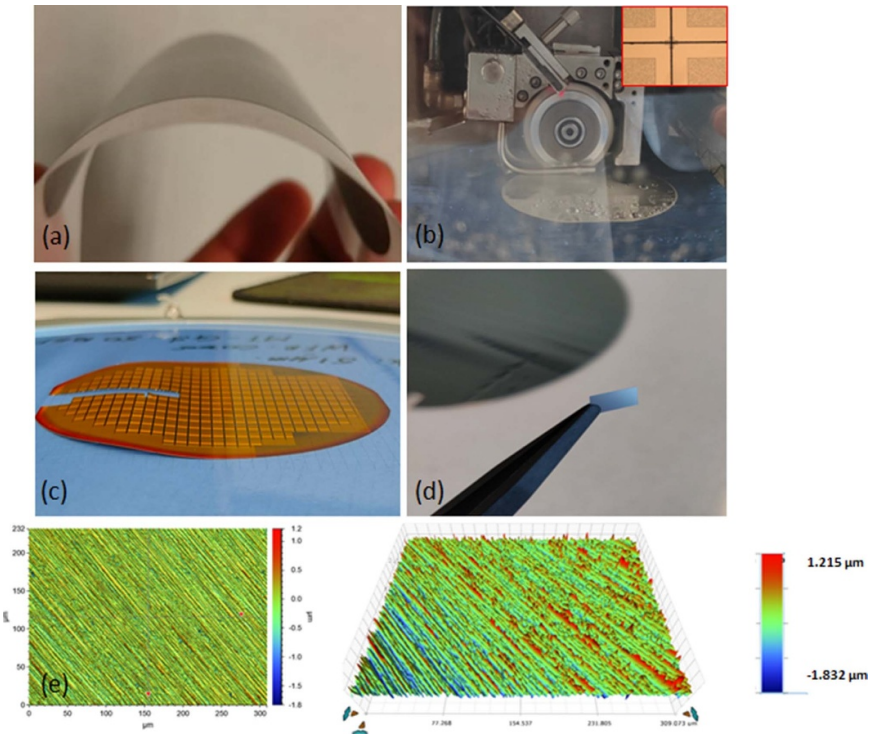


Figure 5. (a) High flexibility of ultrathin Si wafer, (b) dicing process and dicing kerf across dicing marker, (c) diced wafer on Adwill D-175 UV tape, (d) tweezer assisted manual die pickup. (e) 3D plot for die backside roughness.

2.4. Influence of PI on die strength

PI play a vital role in ensuring assembly reliability and are extensively employed in wafer fabrication and bumping processes, making them established materials in the semiconductor industry. PI polymers with low Young's modulus are widely used in flip-chip packaging because of their thermal-mechanical stress buffer action on the bonding pad, to prevent passivation cracking [16] in addition to strengthening die edges in thin dies.

Our study examined the mechanical buffering effect of a thick PI film in strengthening the die FS and preventing die cracking, particularly during the assembly process. Durimide 7520 PI (Fujifilm) was used for this process [17]. This PI offers good tensile strength (215 MPa), glass transition temperature, coefficient of thermal expansion (CTE), wide thickness deposition range (1–50 μm), and compatibility with semiconductor microfabrication processes. Two different thicknesses of 5 μm and 10 μm were deposited and evaluated to compare the effect of their respective thickness on die FS strength. The PI is deposited manually via spin coating at 3600 RPM and 2000 RPM to obtain 5 μm and 10 μm thick film respectively. Film thickness was measured using a Dektak profilometer. The PI is deposited uniformly across the wafer and is not patterned for this investigation. The coated film is first soft-baked for 3 min at 110 °C and then cured at 350 °C for 1 h. Curing was performed using a multi-step heating process to minimize the residual stress in the PI film [18]. PI layers how high shrinkage post-curing (40%), resulting in high wafer and die warpage [17, 19]. The wafers were annealed at 150 °C for 3 h to relieve the stress in PI bonds and relax the film to reduce the warpage.

2.5. Wafer thinning and dicing for ultrathin dies

The fabricated wafers were transferred to a film frame carrier (FFC) and backside (BS) thinning of Si wafers was conducted using a DAG810 surface grinder equipped with an SD1400 grinding wheel, reducing wafers with thicknesses greater than 525 μm–50 μm. The thinned wafer shows high flexibility as displayed in figure 5(a). An average roughness (Sa) of 148 nm was measured on the BS of the thinned wafers using a Bruker white light interferometer. Following the grinding process, the ultrathin wafers were affixed to Adwill D-175 UV tape in preparation for the dicing stage. The wafers were diced into dies measuring 6 × 3 mm^2 dimensions using a DAD3350 mechanical dicing saw as shown in figure 5(b). Subsequently, the diced dies were released from the mounting tape by subjecting them to a 7 min overexposure to 365 nm wavelength UV light within the Dinies UV chamber. An additional 3 min UV light exposure of the diced wafer beyond the industry-standard exposure time of 4 min was beneficial in achieving the effortless release of ultrathin dies from UV tape by significantly reducing die-tape adhesion to nearly zero.

Dies were manually picked from the FFC using plastic-tipped tweezers. A successful pickup approach involved applying slight pressure from the back of the tape, which helped to release and pop up the die edges from the dicing

tape, facilitating the pick-up of <50 μm thick dies. Before conducting mechanical bending tests, the picked-up dies were stored in waffle packs to protect fragile thin dies from external damage.

3. Die strength characterization

To evaluate the impact of new metallization patterns, trench layouts, and PI on ultrathin die's FS strength, mechanical bending tests were employed. Different configurations of uniaxial and biaxial tests are used for die-bending strength evaluation. Commonly used uniaxial bending tests such as TPB and four-point bend are widely used testing methods for evaluating the effect of die BS surface and sidewalls on die strength, whereas biaxial bending tests such as ball-on-ring tests, are utilized to assess the impact of surface flaws from wafer thinning on die strength, and sidewall damage has no significant effect [1, 20]. Both measurement tests require process optimization to minimize nonlinearity from large sample deflection with biaxial bending showing higher sensitivity to bending deformation [21]. The non-linear bending behavior is characteristic of die-bending deflection and test setup [1, 22]. The cantilever bending test is another technique that has proven advantageous in mitigating the effect of high deflection on ultrathin sample measurements [23]. This technique prevents samples from sliding during the bending test, which can result in irregular load and incorrect measurements. In this study, the TPB test was used to measure the die strength of a large sample of design of experiments (DOE), as all the measured die-bending fractures were observed in a nearly linear regime as shown in figure 6(c).

3.1. TPB test

TPB tests were performed using a dynamic mechanical analyzer (DMA) Q800-2320 tool for prepared $\sim$50 μm die samples on a customized test setup as shown in figure 6. The die specimen's position and span length were controlled using a 3D printed holder, made using a polylactic acid (PLA) filament. The 4 mm span length for a 6 mm long die specimen was found to be suitable for linear force-deflection curves in TPB tests. A sharp wedge was also designed, printed, and calibrated to ensure a fine line load indentation on the die centerline.

As shown in figure 7(a), the die sample is placed on the holder's parallel support with the die FS facing down and uniaxial load applied on the die BS. This results in a uniaxial stress state with compressive stress on the silicon BS of the die and tensile stress on the die FS. Die fracture is initiated at the FS near the centerline where the tensile stress is highest. This region is highly sensitive to metallization patterns and trenches which are hot spots for die crack. This loading method mitigates the influence of BS surface roughness and sidewall damage resulting from grinding and dicing processes, respectively. Thus, we utilize this method to assess the influence of new front-end design choices, as discussed in the DOE (refer to table 2), on die FS strength.

This was verified by die BS strength measurements, wherein a bare Si die was placed with the BS facing down and the load applied on die FS. Dies evaluated for their BS strength exhibited approximately 60% lower strength compared to dies assessed for their FS strength, as shown in figures 6(c) and (d). This discrepancy can be attributed to the presence of grooves and subsurface damage on the BS of the die resulting from the wafer grinding wheel, as well as rough sidewalls and chipping from the dicing process.

Mass calibration was performed for the 3D printed force indenter before the TPB test to adjust the bending force of the tool for the mass and material of the wedge. The 3D printed wedge from PLA shows an increased compliance of 2.5 μm N^{-1} compared to the standard $<$0.6 μm N^{-1} of stainless steel wedge. This increase in indenter compliance does not affect the bending stresses, however, bending displacement data are expected to be affected.

For each die type, 40 dies were randomly selected from the wafer and measured. Dies were visually inspected for physical damage, such as cracks, scratches, and breakage before loading in DMA. Ramp force function was employed for load applications with two discrete loads: (1) initial force of 0.010 N min^{-1} until sample contact to ensure a proper line contact and alignment between the load indenter and die centerline and (2) gradually increasing load from 0.2 N min^{-1} to maximum 2 N min^{-1} until the die fracture. The die breakage force (F) and bending displacement (D) are measured using a force versus displacement graph where the slope corresponds to the sample stiffness (figure 6).

3.2. Stress analysis

The die fractures for different samples in the DOE are observed in a linear regime. A numerical flexural stress equation is used to transform the measured die fracture force into fracture stress. Two stress equations were used to characterize the die strength. The first stress equation used is the classical flexural stress equation for measuring the maximum tensile stress in a die with a rectangular cross-section as follows [1]

$$\sigma f = \frac{3Fl}{2bd^2} \tag{1}$$

where F is the peak applied load, l is the load span, b, and d are the die width and thickness respectively, and σ_f is the maximum fracture stress in outer fibers at the midpoint of the sample die. The breaking load (F) is measured from the force-displacement plot generated during the die's TPB test whereas the other parameters were fixed and depended on the die geometry and test setup as shown in figure 7. The thinned wafers showed a thickness variation of $\pm$1–5 μms between different die types as noted in table 3. Equation (1) assumes that the thin die is made of only Si and the die material is fully elastic. The equation can be assumed to hold for standard power MOSFET compositions such as dummy test chips where bulk silicon constitutes the maximum die thickness and dominates the elastic stress. Thus, the sample can be treated as a single non-composite beam for the entire die thickness. In

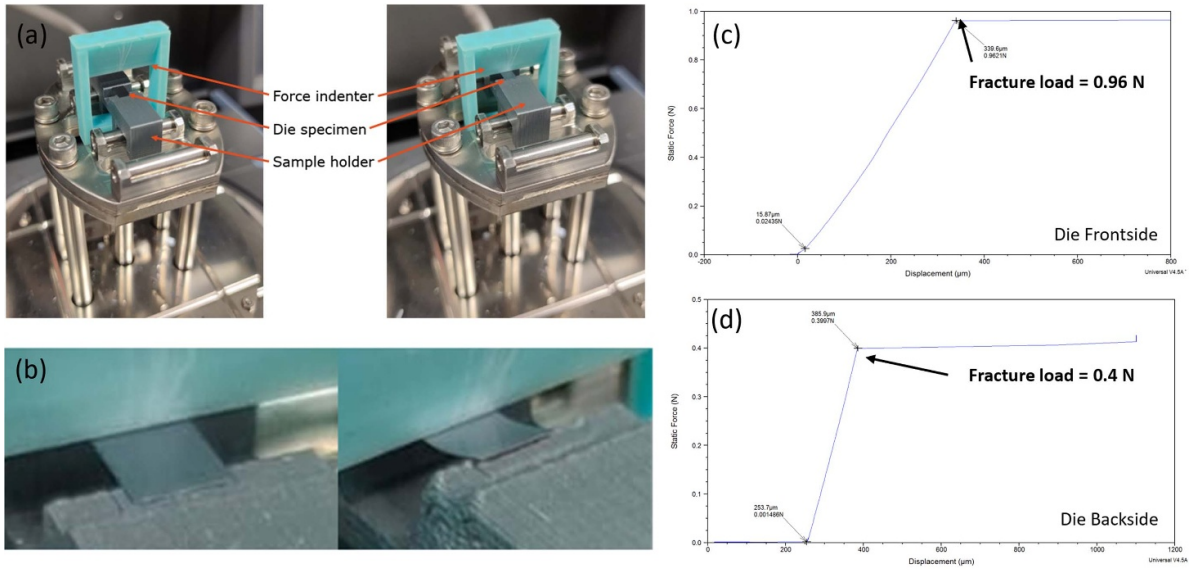


Figure 6. (a) DMA test setup with 3D printed indenter for three-point bend test. (b) Deflection as shown by die before and after applied load. (c) Load-deflection curve for bare Si frontside. (d) Load-deflection curve for bare Si backside.

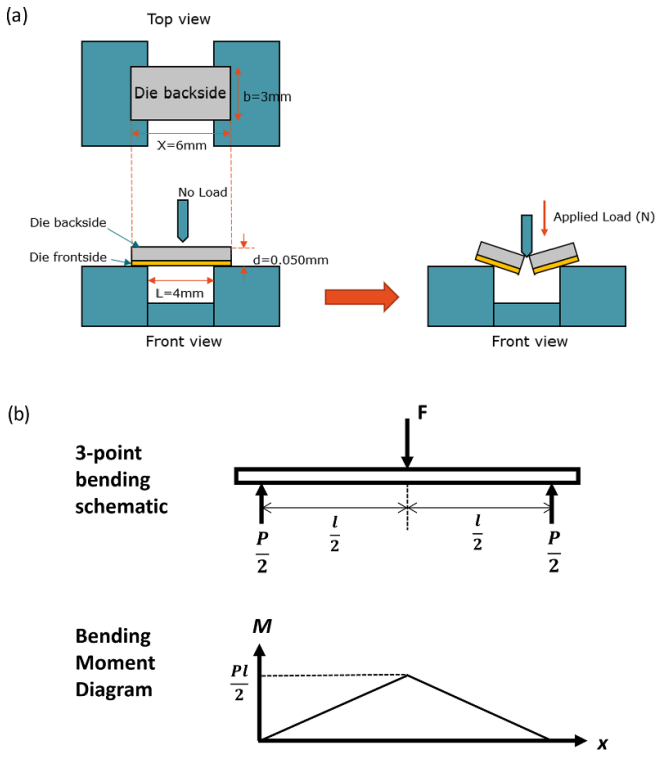


Figure 7. (a) Top and front view of die loading setup where l is span length, x, b and d are sample length, width and thickness respectively, (b) schematic of the TPB test setup with bending moment distribution where F is applied load, l is loading span.

the samples with thick PI film (5, 10 μm) on the die topside, the contribution of PI film needs to be considered in stress calculation and the bi-layer stress equation is thus employed to account for the composite nature of the die. We showcase a cross-section of two composite silicon die structures with 5 and 10 μm PI film respectively (see figure 8) and the stress equations for silicon and PI are as follows

$$\sigma_{\mathrm{Si}} = \frac{M\left(h_2 - t_{\mathrm{PI}}\right) E_{\mathrm{Si}}}{E_{\mathrm{Si}} I_{\mathrm{Si}} + E_{\mathrm{PI}} I_{PI}} \tag{2}$$

$$\sigma_{\mathrm{PI}} = \frac{M h_2 E_{\mathrm{PI}}}{E_{\mathrm{Si}} I_{\mathrm{Si}} + E_{\mathrm{PI}} I_{\mathrm{PI}}} \tag{3}$$

where σ_{Si} and σ_{PI} are the bending stresses for the Si and PI film respectively, M is the maximum bending moment for the applied force F, h_1 and h_2 are the heights of the neutral axis (NA) from the top and bottom surfaces, respectively, and E_{Si}, E_{PI} is young's modulus of Si and PI film, respectively and I_{Si}, I_{PI} are the moment of inertia of the Si and PI film respectively. The variables can be calculated using the equations derived from the parallel axis theorem as discussed in [22, 24]. Due to the low Young's modulus of PI, the position of NA was found to be largely dependent on Si thickness.

4. Results and discussion

4.1. Die strength analysis

Table 3 shows the measured data from the TPB tests and calculated via flexural stress equations to determine the FS strength of the samples and averaged for each die type. The fracture strengths of different die types were compared with those of our standard test chip (reference chip) using the probability of failure Weibull distribution function in MATLAB. Tables 3 and 4 present the average die strength and bending displacement values for the various design types, along with their corresponding measurements of the standard deviation and die thickness. Each design was tested with 40 dies to generate sufficient data points for Weibull distribution analysis. The die designs had a similar thickness of 50 μm $\pm$ 2.7 μm. The thickness variations originate from the BSG process of the silicon

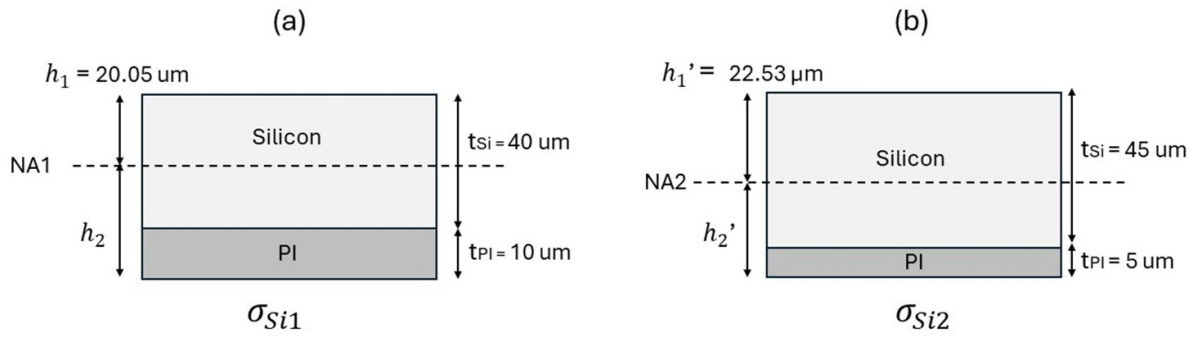


Figure 8. Cross-section diagram of the two 50 μm composite beams with different thicknesses of silicon and polyimide films, (a) indicates the overall beam neutral axis with deposition of 10 μm PI versus (b) a shift in the neutral axis with 5 μm PI deposition.

Table 3. Measurement of average fracture strength of different die types.

Die type	Avg. fracture strength (MPa)	Standard deviation	Die thickness (μm)	Number of samples	Weibull parameter (A:B)[a]
Bare silicon die	790	108	51	40	839.9: 8.6
Bare silicon + Al	920	87	51	35	957.3: 12.4
Commercial chip	318	50	52	30	338.9: 7.2
Standard test chip	339	51	51	40	362: 6.7
Meander design I	350	39	57	40	367.9: 9.2
Meander design II	283	40	52	40	301.1: 7.6
45° Angled design	261	39	51	40	278: 7.7
Reduced G-S gap (20 μm)	307	35	51	35	323.2: 9.5
Test chip with trenches removed beneath G-S metal	364	37	52	40	365: 9.7
Vertical trenches + Al	395	47	53	40	414.8: 11.3
Horizontal trenches + Al	400	51	51	40	422: 8.5
Standard test chip + 5 μm PI	760	101	46	40	802.9: 9
Standard test chip + 10 μm PI	801	104	52	35	847.4: 8

[a] A and B correspond to Weibull distribution's scale and shape parameters.

Table 4. Measurement of average bending displacement of different die types.

Die type	Average displacement (μm)	Standard deviation	Die thickness (μm)	Number of samples	Weibull parameter (A:B)
Standard test chip	207	51	51	40	218: 9.5
Standard test chip + 5 μm PI	319	39	46	40	337.4: 8.3
Bare silicon die	570	108	51	40	609: 7.7
Bare silicon + Al	757.5	87	51	35	677.7: 10.1

wafer. The effect of the difference in thickness was propagated to the final fracture strength calculations. In addition, scanning electron microscopy (SEM, Hitachi Regulus 8230) was performed to observe the fracture morphology of the cracks in the bent dies.

Figure 10 shows the Weibull probability plots for the FS strength of the different die designs where the standard test chips are plotted as circular markers in red. Figure 10(a), presents the FS mechanical robustness of lab-fabricated standard test chips, measuring 6 × 3 × 0.052 mm in comparison with a commercial Si power MOSFET chip, measuring 5.5 × 2.8 × 0.052 mm near its gate area. A similar failure distribution and spread were observed in the Weibull plot of both die types near the gate area. The average FS die strength of the standard test chip was measured as 339 MPa whereas the commercial chip was noted as 318 MPa. Thus, the mechanical sensitivity of the commercial Si power MOSFET was nearly achieved with our lab-fabricated test chip and validated its use as a reference chip for evaluating the die robustness of the new custom chip designs. The majority of the cracks were found to initiate in the die middle, following a straight-line path in the metal-free region that separates the gate and source areas. Figure 9(b) shows SEM images of the fractured interface of the ultrathin die wherein the crack passed through a poly-Si-filled trench layer indicating a point of failure and crack initiation inside the die during the TPB.

In the design evaluations from the TPB tests, some designs showed a negative response to die robustness as demonstrated

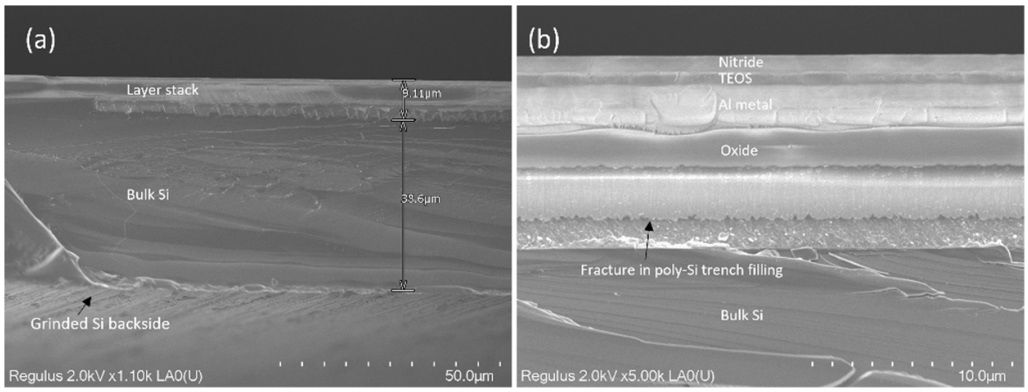


Figure 9. (a) SEM analysis of fractured die indicating Bulk Si and layer silicon of 48 μm thick die, (b) close-up indicating fracture propagation across polysilicon-filled trenches.

in figure 10(b). Surprisingly, metallization patterns such as an angled line gap and minimized isolation gap for G-S to 20 μm showed reduced die strength (table 4). Some other designs showed improved robustness such as die metallization with a thicker meander wall pattern, which showed an increase in die FS strength from 339 MPa to 350 MPa. This can be attributed to the meander pattern in the high fracture toughness material, such as pure Al resisting crack propagation in a straight line path between the G-S metal-free region as shown in the standard MOSFET device. Another die sample with a meander pattern and thinner walls negatively affected the die strength (289 MPa). The width of the metal in the meander walls was thus found critical for its impact on die robustness. Theoretically, the die strength can be further increased by optimizing the meander design to facilitate thicker walls in the direction of crack propagation. In addition, the point of crack initiation was found to be dependent on the orientation of the trenches underneath. SEM fracture analysis indicated two different die crack locations with thicker meander wall designs during the TPB test (refer to figure 11). Cracks were predominantly found to initiate across the source region of the die where vertically aligned trenches were present. A failure occurred either in the metal absent isolation gap or under the metal-covered regions of the die source area. Similarly, in thin-walled meander metallization samples, dies cracked along a straight line across the vertical trenches in the metal-free source region (see SEM figure 12).

In a different die design, the metallization pattern remained consistent with that of the standard test chip, while only the trench layout was modified. Specifically, the trenches were removed underneath the metal-absent gaps. The average die strength of the 40 samples was measured at 364 MPa (refer to figure 10(c)), representing a 7.5% increase compared to the standard test chip. This improvement was directly linked to the absence of trenches in regions susceptible to cracking. For instance, areas of the die where deep trenches are not covered with high fracture toughness materials, such as metal films, exhibit a high risk of cracking. In power MOSFETs, one such critical area is where Al is patterned to isolate the gate and source metallizations. Thus, the interaction between trenches and metal is identified as a crucial design consideration for developing high-throughput and robust ultrathin power MOSFET chips. The SEM results indicated that the majority of die cracks occurred in the source trench region (see figure 13(b)), with a small minority in the metal and trench-free regions. This is in stark contrast to the results from the standard test chip, where die cracks were observed in the middle of the die at trenches where metal film was not present.

The silicon top metallization pattern is crucial for the device's electrical functionality, but it negatively affects the mechanical robustness of the large ultrathin chip by increasing the risk of crack initiation in metal layer-absent regions. Depositing a thick PI film over the nitride layer significantly improved die strength, achieving 760 MPa for a 5 μm and 801 MPa for a 10 μm thick PI film respectively, compared to the 339 MPa strength of standard reference dies with only a nitride topside film. (refer to figure 10(d)). Interestingly, the increase in thickness of the PI film from 5 to 10 μm only leads to an additional 5% increase in die strength. It should be noted that the total thickness of the different chip designs was maintained at 50 μm. Thus an increase in PI layer thickness necessitated a further reduction in the crystalline Si wafer thickness through BSG.

This increase in die strength by more than a factor of two can be attributed to PI's properties like good fracture toughness, tensile strength, and low Young's modulus [17]. Soft PI can handle the tensile stress from die bending much better than nitride film. In a packaged device, the soft PI film can potentially relieve the stress between the hardened epoxy and stiff nitride film, thus preventing the initiation and propagation of cracks in the die. A minor increase in die strength can also be attributed to pre-stress in the PI film, as discussed in the warpage analysis in section 4.2 and the appendix. The shrinkage of the PI film post curing enables the cross-linking of polymers which leaves the PI film under tensile stress. During the TPB bending process, the load indenter must first overcome this pre-stress (tensile) in the die before the silicon is stressed. This can result in higher levels of bending forces for die cracking. The residual stress in PI also varies at different film thicknesses, which can explain the marginal increase in die strength due to the increased PI thickness

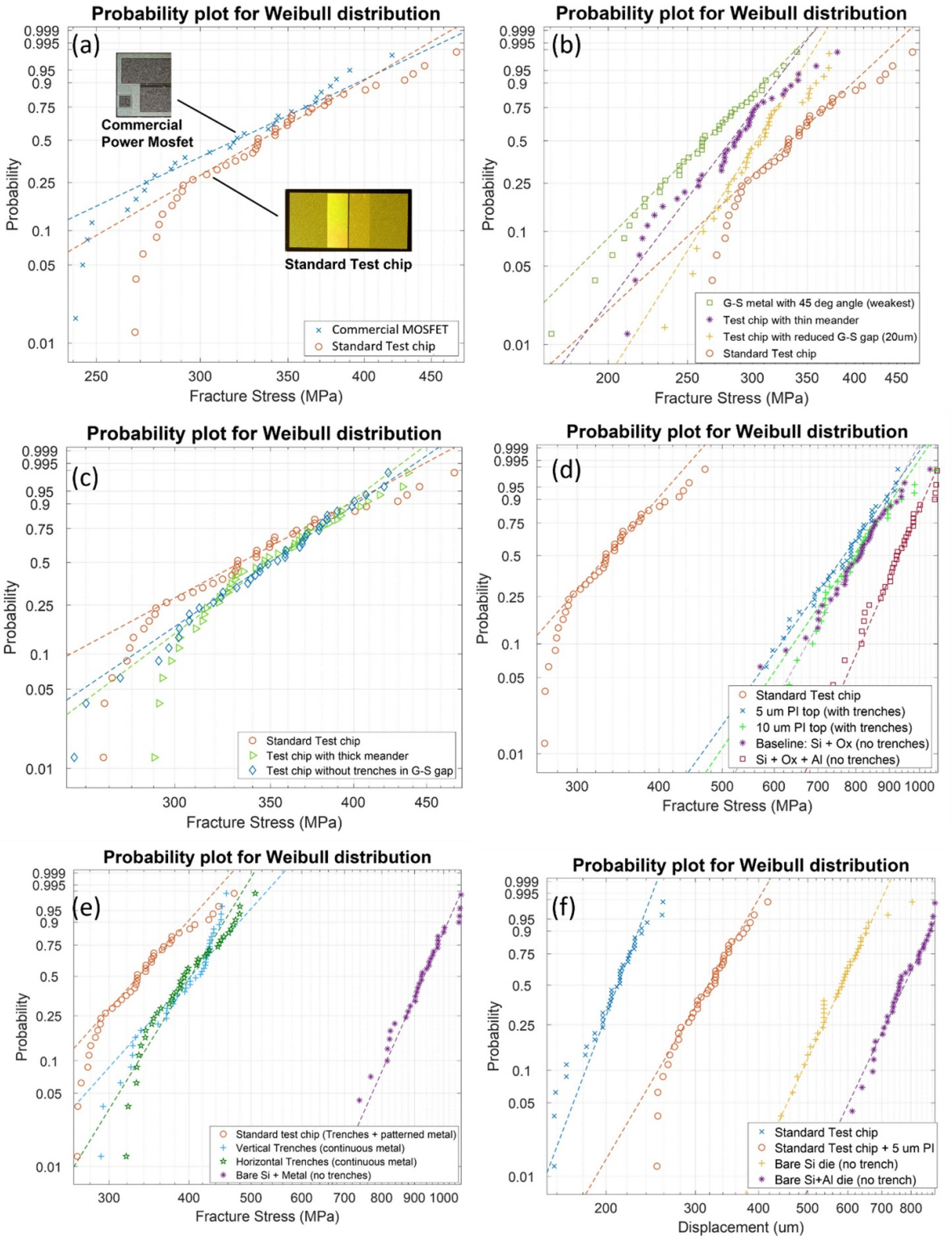


Figure 10. Probability plot for Weibull distribution (a) comparing commercial die with fabricated standard test chip. (b) Die designs with weaker strength to standard die (c) robust die designs, (d) PI influence on die robustness, (e) trench orientation influence on die strength. (f) Die bending displacement for different dietop samples.

[19]. Additionally, thinner Si dies exhibit higher bending deflection and fracture strength compared to thicker Si dies [25]. Therefore, the strengthening effect of PI film deposition on the reference dummy MOSFET chip is attributed to the combined action of the crack-resisting nature of the soft PI film and thinner Si substrate. An optimized PI thickness of 5 μm is thus found more beneficial for die strengthening as increasing PI thickness can lead to increased manufacturing costs and process challenges such as high die pre-stress and warpage.

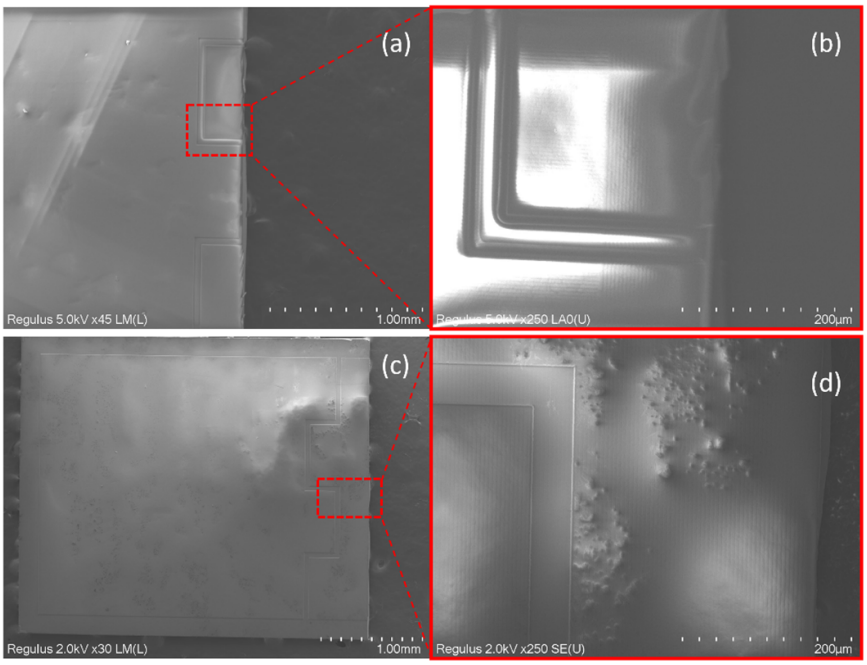


Figure 11. SEM image for die crack in thicker meander die. Two crack locations are identified (a) die fracture across metal absent insulation gap, (b) close-up image of crack origin in the vertical trench at source region. (c) Die fracture on metal-covered source region. (d) Close-up image of crack origin in vertical trench.

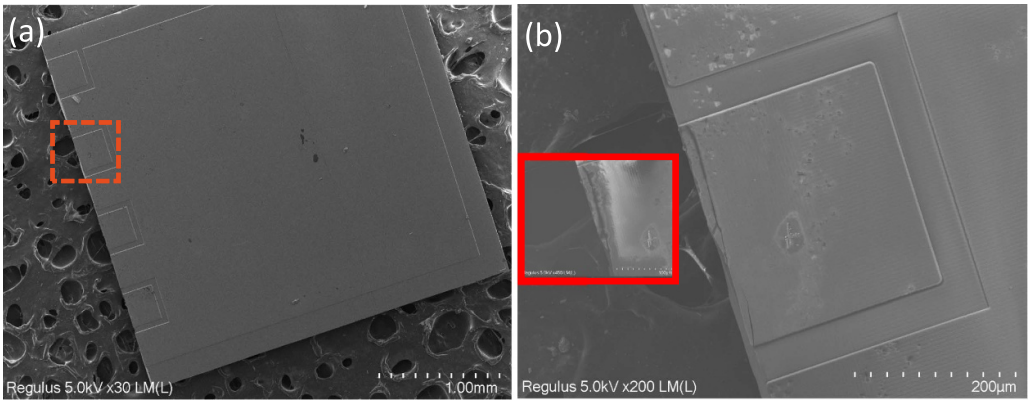


Figure 12. (a) SEM analysis of thin meander chip shows crack propagation across metal absent isolated 50 μm gap. (b) Close-up image showing fracture origin and propagation across vertical trenches underneath.

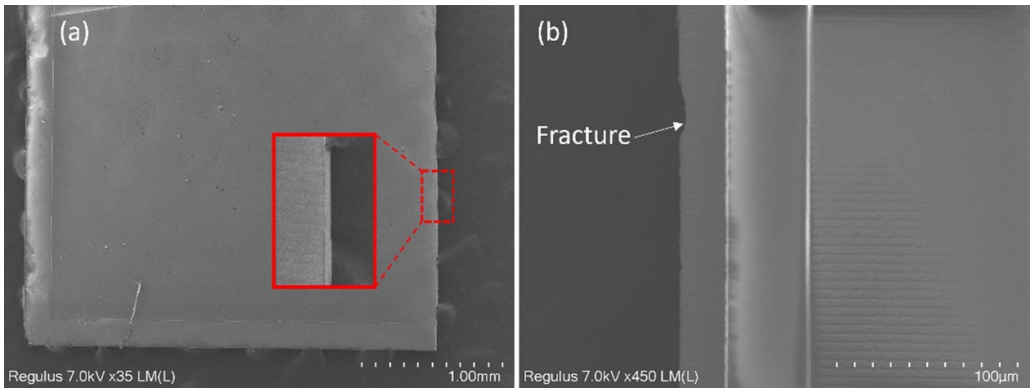


Figure 13. SEM fracture analysis of standard reference die vs die with modified trench layout, in modified samples, trenches were removed underneath metal isolation gap. (a) Die crack in middle across isolation gap in reference die, (b) crack across vertical trenches outside isolation gap in modified layout.

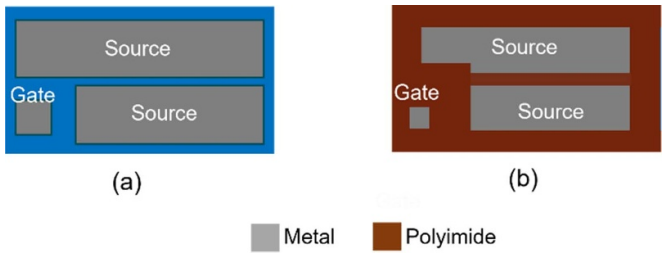


Figure 14. (a) Standard die layout; (b) proposed die layout with PI coating. The layout maximizes PI coverage with openings for gate-source interconnections. This design provides maximum robustness.

Table 5. Wafer stress and warpage measurements for deposition of different materials and thicknesses.

Process layer	Bow (μm)	Stress (MPa)	Radius (m)	Film thickness (nm)
Warpage Test 1 (Si + PI)				
Bare Si wafer	0.61	NA	−2e + 06	NA
Si + PI	−14	+30	56.5	5000
Warpage Test 2 (Si + TEOS + PI)				
Bare Si wafer	1.59	NA	−621.4	NA
TEOS	18.87	−90	−42.8	2000
PI	2.25	−1.4	−408.5	5000
Warpage Test 3 (Si + TEOS + Al + passivation O_x + Si_3N_4)				
Bare Si wafer	0.92	NA	NA	NA
TEOS	17.72	−91.5	−45.1	2000
Al	8.03	−13.4	−97.83	4000
Passivation (O_x + Si_3N_4)	25.1	−27	−31	2000 + 1400
Warpage Test 4 (Si + TEOS + Al)				
Si + TEOS	17.73	−89.9	−44.9	2000
Al 1	8.03	−13.4	−97.83	4000
Al 2 (thicker)	−1.55	+19.5	777	6000

In the Weibull distribution plot shown in figure 10(d), the strengths of the bare Si and Si + Al sputtered dies were also compared, which shows the effectiveness of PI as a stress buffer. The deposition of the polymer resulted in a thin Si die with HAR trenches and metallization patterns as strong as a similarly sized bare silicon die (without trenches and patterns). In this study, the PI film was not patterned and covered the entire chip layout, which is not the case for functional power MOSFET devices in which the die FS has openings in the gate and source areas for topside bonding, such as thick Al–Cu wire bonds, ribbons, and clip interconnections [26]. A chip layout is proposed (see figure 14) to maximize the coverage of PI for clip-bonded products on the dietop to obtain the maximum benefit of its strengthening effect.

Figure 10(e) shows the effect of the trenches and their orientations on the die FS strength when compared to bare dies. Additionally, the influence of homogeneous metal film over different trench orientations was studied to highlight the trench-metal interactions. The fracture strength of dies dropped from 920 MPa to 400 MPa after the introduction of trenches in silicon crystal (table 3). Dies with horizontally and vertically aligned trenches show surprisingly comparable strength when covered with a homogeneous Al metal layer. The effect of trench orientation is expected to have a greater influence on die strength in the absence of metal film, wherein horizontally aligned trenches show higher fracture strength due to their perpendicular alignment to force applying indenter.

The force-displacement plots generated from the TPB tests show an approximately linear behavior. 5 μm thick PI-coated dies show a high bending displacement of 319 μm as compared to 207 μm from reference chips with nitride topside of the same die thickness (refer table 4 and figure 10(f)). This is attributed to the low Young's modulus and stiffness of polymer films compared to the brittle nature of materials such as Si, oxide, and nitride [24]. Bare Si dies with Al deposition showed the highest bending displacement of 757.5 μm followed by 570 μm for bare Si dies, owing to the absence of crack initiation components such as trenches and patterned layers.

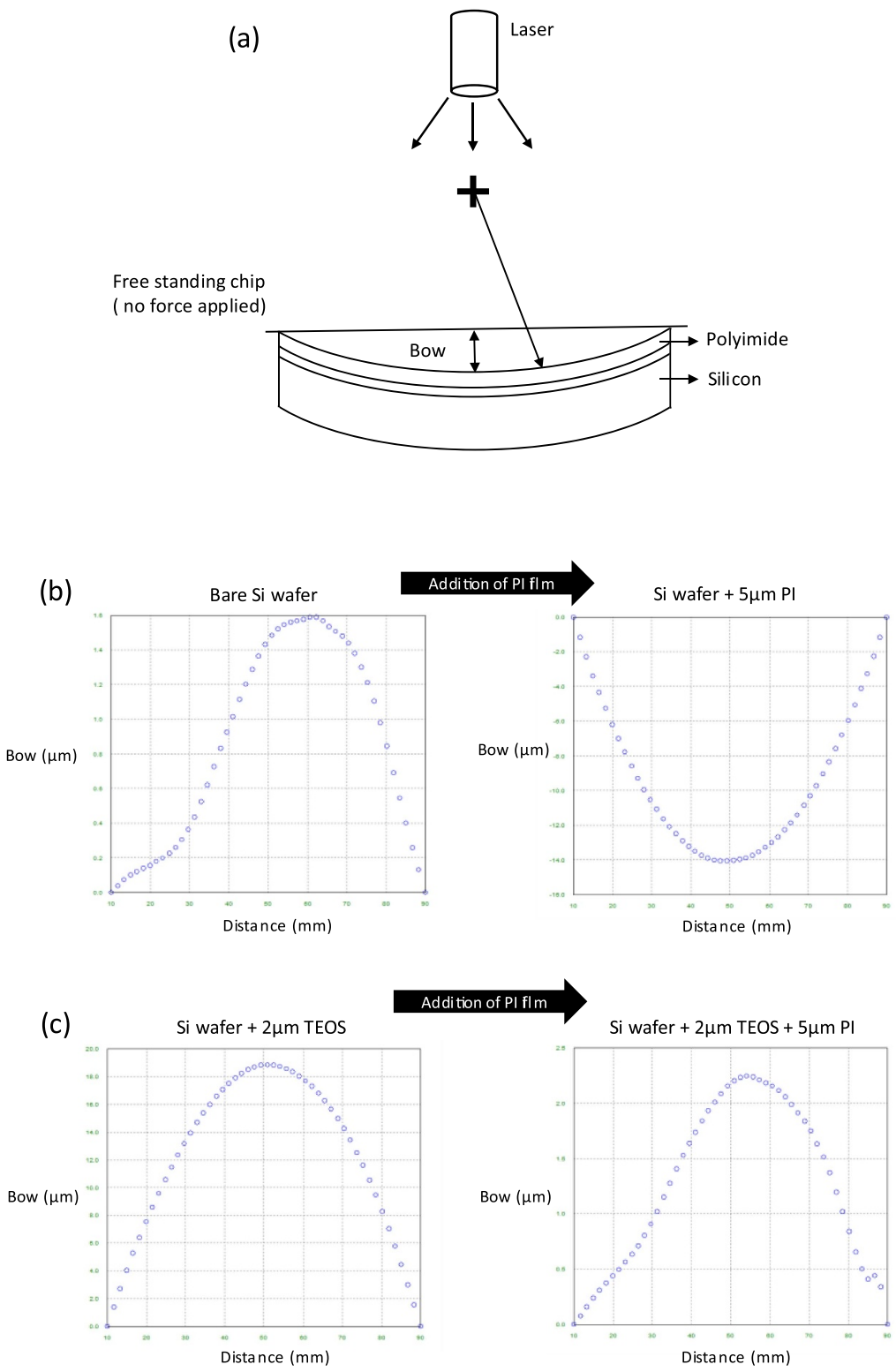


Figure 15. (a) Bow and radius of a warped Si sample with PI film as measured by Flexus thin film stress measurement tool; (b) Before and after effect of adding PI film to Si wafer bow measurements; (c) (b) Before and after effect of adding PI film to Si wafer with TEOS coating. Residual stress in cured PI exhibits tensile stress.

4.2. Thin film stress and warpage analysis

The deposition of each process layer during device fabrication adds residual stress and warpage to the processed wafer [27]. These stresses greatly influence the subsequent stages in ultrathin die manufacturing such as the grinding and dicing process. The nature of the stresses and bows induced by different deposited thin films depends on their process parameters

Table 6. Nature of residual stress for different MOSFET device layers.

Device layer	Stress behavior
Si Wafer	Near flat
Oxide/TEOS	Compressive
Pure Al	Tensile
Passivation (O_x + Si_3N_4)	Compressive
Polyimide	Tensile

and film thickness. The fabricated dummy power MOSFET device layers were measured using the Flexus-2320-S tool for their respective stress behaviors in different combinations, as listed in table 5.

Pre-stress in PI: This test investigated stress and warpage induction by the deposition of 5 μm PI film on silicon wafers. The PI film was found to induce tensile stress in wafers with an increased negative bow as shown by the smiley face configuration in figure 15(b). Residual stress is created by the polymer curing process when it shrinks to cross-link bonds for material hardening and is influenced by the curing history and morphological structure of the polymer. The CTE mismatch between the PI and the substrate during thermal curing results in residual stress in the PI film [18, 19, 28].

Effect of TEOS film on wafer warpage: The TEOS film was found to be highly compressive. A 2 μm film deposition induced 90 MPa compressive stress on the wafer. In the same test, PI was added to the TEOS to help compensate for the negative bow with the tensile nature of the PI film. The addition of PI reduced the wafer stress and bow (table 5). Thus, a balanced ratio of TEOS and PI is suitable for developing ideal flat wafers for critical applications.

Warpage induced by Power MOSFET device layers— Wafer warpage was investigated for key device layers in a Power MOSFET device. 4 μm pure Al was deposited on the TEOS-covered Si wafer. The tensile nature of pure Al was found to compensate for the highly compressive nature of the insulation film and led to lower stress and wafer bow. Further addition of passivation (SiO_2 + Si_3N_4) layers over metallization led to an increase in wafer warpage owing to the compressive nature of the passivation films. The high stress in the passivation layers of SiO_2 and Si_3N_4 is also attributed to the high residual stress during their deposition. This stress can be reduced by optimizing process parameters, such as power and gas flow rates [29].

Effect of increased metal thickness on warpage—Two different pure Al thicknesses (4 μm and 6 μm) were compared for their tensile stress behavior over a 2 μm thick deposited TEOS film on a Si wafer. A thicker 6 μm Al film was found to significantly reduce TEOS's frowny face warpage and create a near-flat processed wafer with tensile stress.

From tables 5 and 6, it is demonstrated that the right combination and thickness of different device layers can help fabricate near-flat wafers and dies with minimal internal stress and warpage.

5. Conclusions and recommendations

This study presents the effect of different dietop systems including metallization patterns, PI films, double-trench structure alignment, and layout on a 50 μm thick die's strength. Various chip designs have been studied and investigated for their mechanical robustness in resisting cracks at the large ultrathin die's FS. The fabricated test chip exhibited mechanical robustness equivalent to that of a commercial silicon power MOSFET die. This proved to be an effective method to quickly investigate new chip designs for their mechanical response to the die FS fracture strength. The method is fast, practical, and robust and eliminates the need for extensive back-end processes such as CMP and modern dicing steps. Furthermore,it is concluded that

- The addition of 5 μm PI on top of nitride shows significant strength improvement (760 MPa) as compared to dies without PI (339 MPa) with the same die thickness. The strengthening effect of soft PI can potentially help prevent passivation cracking in ultrathin dies by acting as a buffer between the stiff nitride and hardened epoxy. Interestingly, 10 μm PI was not found to have any additional strengthening effect and resulted in increased manufacturing costs and processing challenges such as die warpage. Thus, we conclude and recommend not exceeding 5 μm PI due to diminished effects on die strength. We also propose to maximize the PI coverage on the die FS to obtain the maximum benefit of its strengthening effect and only leave enough space for the die top interconnections.
- Die layouts with meander-shaped walls were found effective in improving the robustness of the gate region and replacing the traditional straight-line isolation gaps between the gate and source regions. The effect of meander wall thickness was also shown wherein wider metal areas showed an impressive 21% improvement in die strength from 289 to 350 MPa. Based on the current trend, further optimizations in the meander pattern have the potential to significantly enhance die strength.
- The experimental results show that trenches are hot spots for die crack initiation. The addition of trenches reduced the strength of the bare die from 920 MPa to 400 MPa. The effect of the trench-metal system was also demonstrated wherein covering trenches with the metal film was found effective in improving the die's overall robustness; die design where trenches were strictly kept underneath the metal film and removed from crack hotspots showed improved robustness (364 MPa). Other deep cavity structures such as through silicon vias filled with metal can potentially reduce the risk of die cracking with similar structural behavior. Deeper care is required when designing trenches and cavities in ultrathin silicon to fabricate robust devices.

- Thin film stress measurements exhibited varying natures of stresses and warpages induced by different process layers in the silicon wafer. It is demonstrated that the adverse effects of these stresses and warpages can be minimized by using the right combination and thickness of device layers to counterbalance stresses and warpages and achieve near-flat wafers and dies which can aid in robust ultra-thin die fabrication.
- SEM crack analysis showed that cracks were dominantly initiated along the vertical trenches in the die. Thus, the relationship between the die-bending axis and trench alignment was found to be critical.

As dies become even thinner (10–30 μm) and larger, die robustness becomes even more critical for device reliability and high assembly yield. This study helps to take a closer look at the key factors affecting the large thin die FS strength during the fabrication process. The effect of robustness-improving techniques on the electrical performance of the device remains to be seen and will be tested in future work.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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Appendix: Finite element analysis (FEA)

To validate experimental data with mechanical simulation for bending thin silicon dies, a brief study was carried out using COMSOL Multiphysics version 6.1. The thin silicon die with PI top was simulated using a 2D beam model with 41 μm Si and 5 μm thick PI film. Single-crystal, isotropic silicon with standard parameters is added to model the bulk Si and PI parameters are adjusted to meet Durimide 7520 material datasheet specifications [17]. A half-beam model with a prescribed displacement function was used with the following boundary conditions;

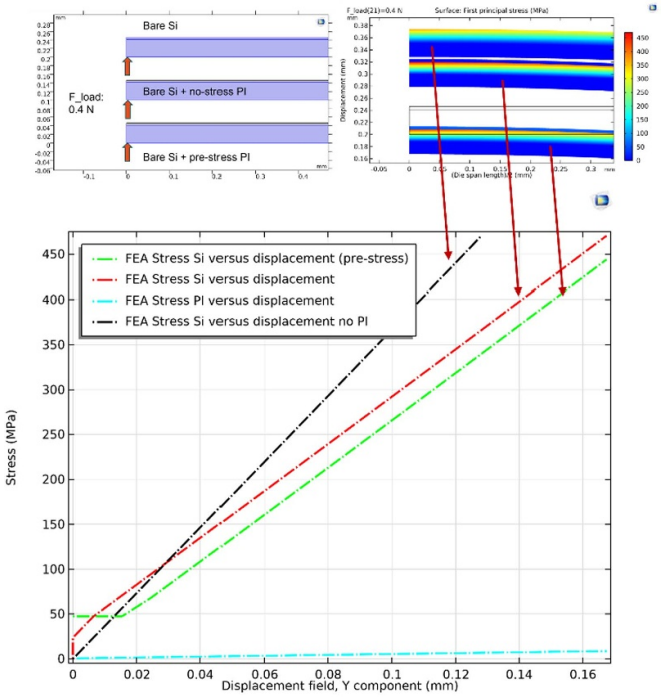

Figure 16. Different models exhibiting stress levels are required for die fracture. The sample with pre-stressed PI film shows the lowest stress.

(1) The boundary at the load point is fixed to restrict beam displacement in the x-axis and only vertical displacement (in the y-axis) is allowed.
(2) The beam end's movement is restricted in the y-axis and only displacement in the x-axis is allowed to model the die slippage from the support beams during bending.
(3) A point load is added to the silicon side of the beam to model the force indenter on the die BS during TBP testing. The simulation is carried out at a fracture load of 0.4 N, which is the mean fracture load measured in TPB experiments for bare silicon dies with PI.

Three different dies are modeled to study the effect of pre-stress in PI film during die bending. As shown in figure 16, a 46 μm thick bare Si die with no PI film exhibited the highest stress. This beam offered the lowest fracture strength. The presence of greater stress levels in the silicon resulted in lower indentation forces required to induce yield or fracture in the die. The second model incorporated 41 μm bare silicon as a base and unstressed 5 μm PI film on topside. The lower stress levels compared to the bare Si die model can be attributed to the presence of low stiffness PI which resists the propagation of cracks. The plot indicates a stress gap of 100 MPa introduced with PI addition for a 120 μm bending displacement. In the third model, PI film was simulated with 50 MPa tensile stress to represent pre-stress in film from polymer shrinkage during the curing process. The lowest stress levels were displayed in this model, which suggests that a higher bending

load is needed to first overcome the pre-stress in the PI film and then bring the silicon under enough stress for die fractur

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