Analysis of Active Control Methods to Improve Converter Reliability in Wind Turbines

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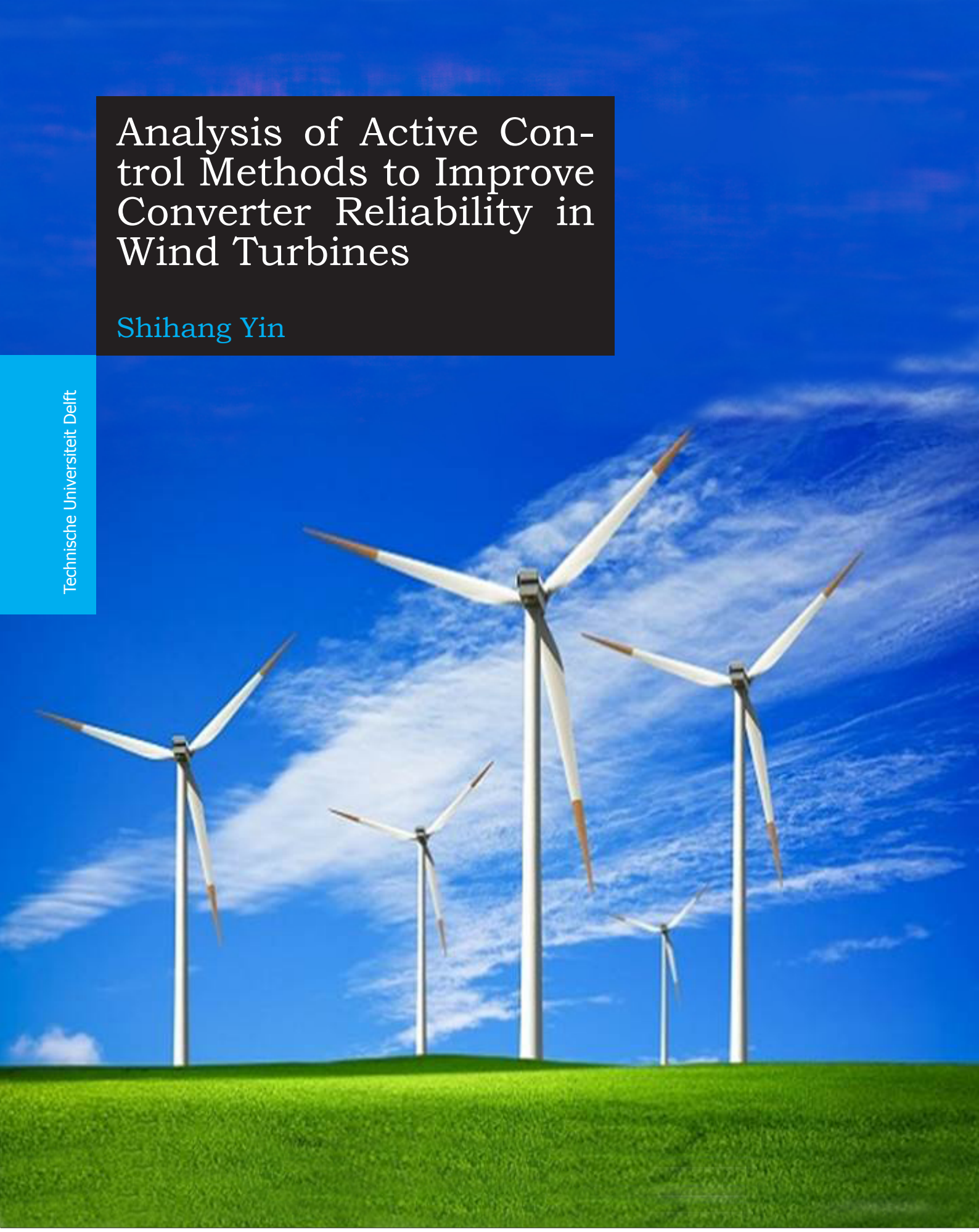

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Challenge the future

Analysis of Active Control Methods to Improve Converter Reliability in Wind Turbines

by

Shihang Yin

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Abstract

Converters are the essential devices in the energy transformation process from the wind generators to the grid. Power electronic semiconductors have a high share of failures in the power electronic converters. Therefore, the reliability based on lifetime of power semiconductor generates more and more attention. This thesis presents a comparison of different active control methods to control the lifetime of power semiconductors in wind turbines. This investigation is implemented through simulations on a 10 MW direct drive permanent magnet wind generator with three-level neutral point clamped converters. The study shows that both switching frequency control and reactive current control can improve semiconductor lifetime to certain extents. As for which control method is more effective depends on the surrounding wind environment.

Acknowledgement

During working on my thesis and studying, there are many professors and friends who help me and encourage me. I could not finish my paper without them. Thus, it is an opportunity to express my gratitude to them.

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1. Introduction

1.1 Thesis Background

Wind is a clean and pollution-free renewable source, the electricity generated using wind power makes a significant contribution to environmental protection. In addition, wind energy is sustainable, so it is increasingly valued by countries around the world.

A large wind turbine system used to adopt the squirrel-cage induction generator (SCIG) or the doubly-fed induction generator (DFIG). Both of them require a mechanical gearbox to match the rotating speeds between the turbine and the generator. Nevertheless, according to the statistics of wind energy systems, one of the major causes of downtime, maintenance and revenue loss regarding to power generation is brought by gearbox failures [22]. With the recent development of wind energy technology, a gearless wind turbine system that employs the permanent magnet direct-drive generator (PMDD) has been widely applied in this field [23].

Converters are the essential devices in the energy transformation process from the wind generators to the grid. For a gearless wind turbine system that does not need to consider the gearbox failures, the lifetime and reliability of power electronic converters becomes an important issue. Thus, this thesis aims at exploring the control of electrical parameters to improve lifetime performance of converters for the wind turbine system that consists of a 10MW PMDD generator and three-level neutral point clamped (3L-NPC) converters.

1.2 Project Motivation

The power electronic semiconductors have a high share of failures of the power electronic converters [24], thus, the possibilities of different active control methods are introduced in this thesis to enhance the lifetime of power electronic semiconductors. Existing literature proposes increasing lifetime by control methods that change load current, share power between parallel devices or modify loss distribution. Other proposals include controlling the modulation strategy along with the control of switching frequency. This thesis picks some of these methods, and compares by their effectiveness on the thermal performances of power semiconductors in a wind generator system that has a 10MW PMDD generator and the 3L-NPC converters.

1.3 Research Objectives

The research objectives can be summarized as follows:

1, An overview of existing electrical parameter-based control methods to improve lifetime.

2, Model the control methods in a wind generator system with 10MW PMDD generator and 3L-NPC converters.

3, Analyze and compare these methods based on the lifetime estimated from thermal cycling.

1.4 Overview of Chapters

This thesis consists 8 chapters in total, the main subject of each chapter is listed as following:
Chapter 1: A brief introduction to background, motivation, objectives and contributions of this thesis.
Chapter 2: An overview of active control methods in literature. The principle and implementation of each control method are explained in detail. Furthermore, choices of active control methods in the thesis are justified.
Chapter 3: Principles of the thermal model of power semiconductors are described.
Chapter 4: Different converter modulation methods are compared and chosen according to their thermal performance.
Chapter 5: Two different switching frequency active control methods: two-level regulation and three-level regulation are implemented and compared. Results how that the three-level regulation is more effective.
Chapter 6: The reactive current active control method is implemented for both the grid side converter and the generator side converter.
Chapter 7: The lifetime improvements brought by two different active control methods are estimated and compared based on the thermal cycling. Rain flow counting is introduced to show the distributions of ΔT_j under different active control methods.
Chapter 8: Conclusions of the thesis are drawn. Future work of gate voltage regulation, its limitations and possible ways to continue the research are discussed.

1.5 Contributions

Different converter modulation methods are compared considering their effects on thermal cycling. Results show that the flat-top PWM gives the most gentle thermal cycling.
Different active control methods including switching frequency regulation and reactive power regulation are analyzed. Their advantages and disadvantages are compared. The simulation models and results can help further research on similar topics.

2. Overview of Active Control Methods

There are a couple of active control methods having been investigated as effective ways to improve the reliability of power electronic converters in wind generator systems. Switching frequency regulation, DC-link voltage regulation, gate voltage regulation, power sharing regulation, reactive current regulation and active cooling control all have been proven to be able to enhance semiconductor lifetime in previous studies. This chapter evaluates the feasibility to adapt those methods to a PMDD and 3L-NPC drive-train system. The contents are as follows:

1, A brief introduction to topology and operation principle of the drive-train.

2, An overview on principles and implementations of all the active control methods mentioned above.

3, According to the requirements and characteristics of the drive-train system, choices are made on active control methods. Reasons of choices are justified.

2.1 PMDD and 3L-NPC Drive-train System

10MW Permanent Magnet Direct-drive Generator

The principle of PMDD generator is to rotate the rotor using the wind turbine blades, thus, the electricity is generated. The rotor has a structure with permanent magnets and does not require an external excitation power supply. The variable frequency AC power of PMDD generator is converted into the AC power which has the same frequency as the grid through rectifier and inverter. The drive-train with a PMDD generator and 3L-NPC converters is shown in figure 2.1 [1].

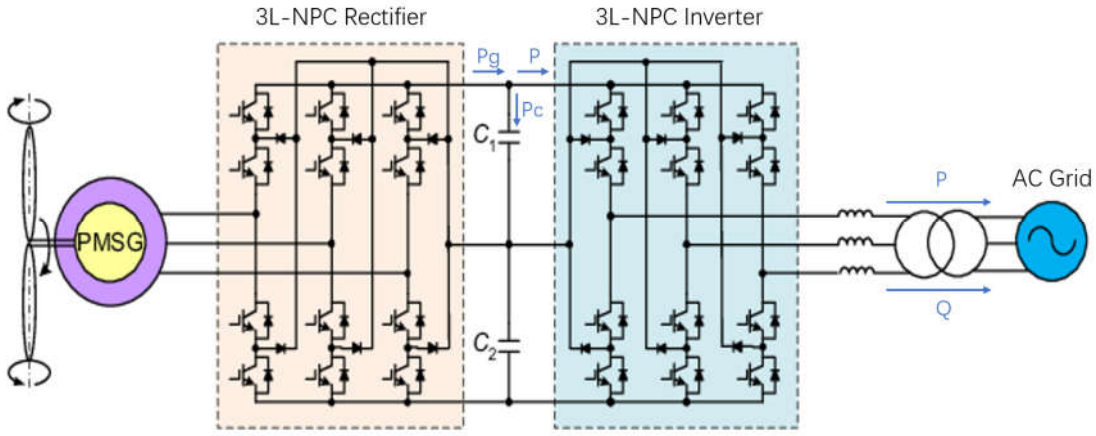

Figure 2. 1 Drive-train Diagram of PMDD and 3L-NPC [1]

Since PMDD drive-train uses full-power converters, the reliability of power electronic semiconductor is more crucial, and this reason helps the thesis determine the study direction.

Three-level Neutral Point Clamped Converter

An insulated-gate bipolar transistor (IGBT) is the composition product of a bipolar junction transistor (BJT) and a metal-oxide-semiconductor field-effect transistor (MOSFET), and it is a composite full controlled voltage driven power semiconductor device. IGBT retains both the high input impedance from MOSFET and the low conduction voltage drop from BJT, so it realizes low

drive power and low saturation voltage at the same time [25]. Due to MOSFET cannot endure the high current produced by 10MW generator, IGBT is selected as the switching device in this system. With increasing power rating leading to high voltage rating, the increased switching losses in two-level converters make this prohibitive. For this reason, multi-level topology is essential as getting popular. 3L-NPC converter is selected in this thesis because it has the most mature technology [26]. The 3L-NPC converter represents that the output voltage from each phase of the AC side has three values related to DC side structure. The positive voltage is equal to $V_{dc}/2$, the negative voltage is $-V_{dc}/2$, and the midpoint voltage is 0. The circuit structure of 3L-NPC converter is shown in figure 2.2 [2]. Each phase of the converter consists of four IGBT switches, four freewheeling diodes (FWDI) and two clamped diodes. The DC side voltage supported by two series connected capacitors C_1 and C_2, the voltage on C_1 and C_2 should be balanced through control.

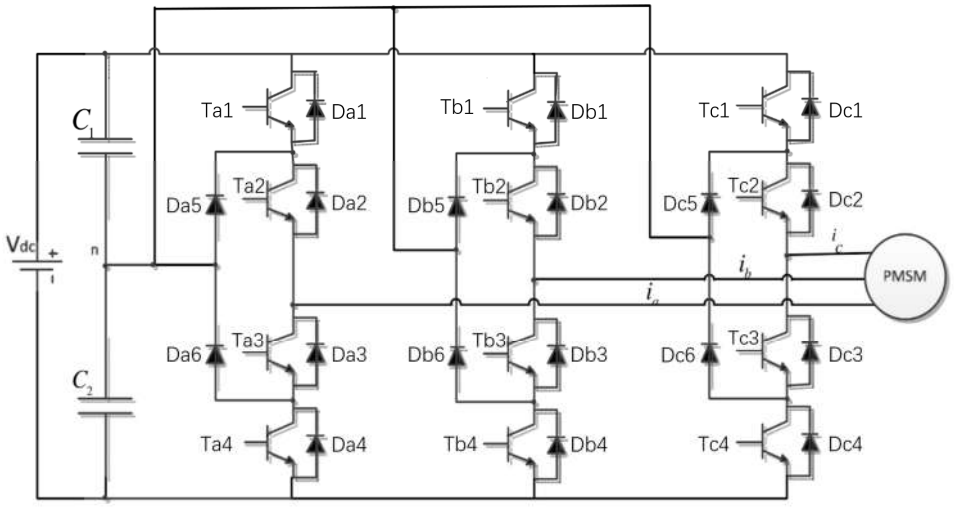

Figure 2. 2 Circuit Topology of 3L-NPC Converter [2]

To simplify the analysis, one phase leg of the 3L-NPC converter is taken out to analyze, which is shown in figure 2.3.

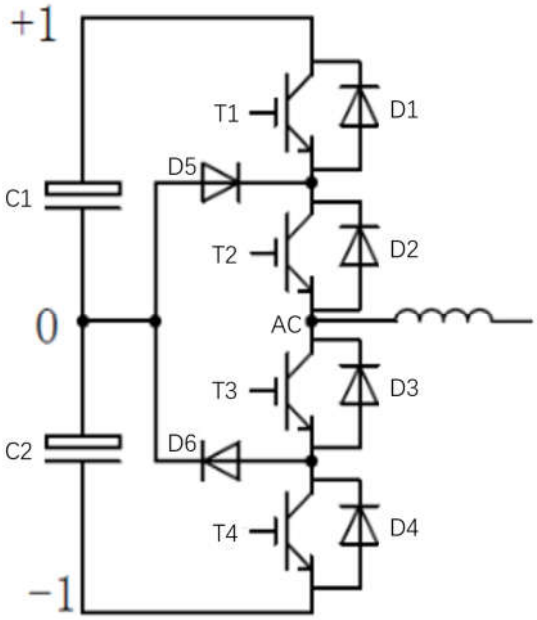

Figure 2. 3 Single Phase Leg of a 3L NPC Converter

The principle of the modulation of the phase-leg is shown in figure 2.4 [3]. $v_{control}$ is the modulation waveform, v_{tri} is the carrier waveform, and V_{A0} is the output voltage of the phase-leg. During the first half period $v_{control} > 0$, T_2 is constantly turned on while T_4 is regularly turned off, when $v_{control} > v_{tri}$, T_1 turns on and T_3 turns off, when $v_{control} < v_{tri}$, T_1 turns off and T_3 turns on. During the second half period $v_{control} < 0$, T_1 is constantly turned on while T_3 is regularly turned off, when $v_{control} > v_{tri}$, T_2 turns on and T_4 turns off, when $v_{control} < v_{tri}$, T_2 turns off and T_4 turns on.

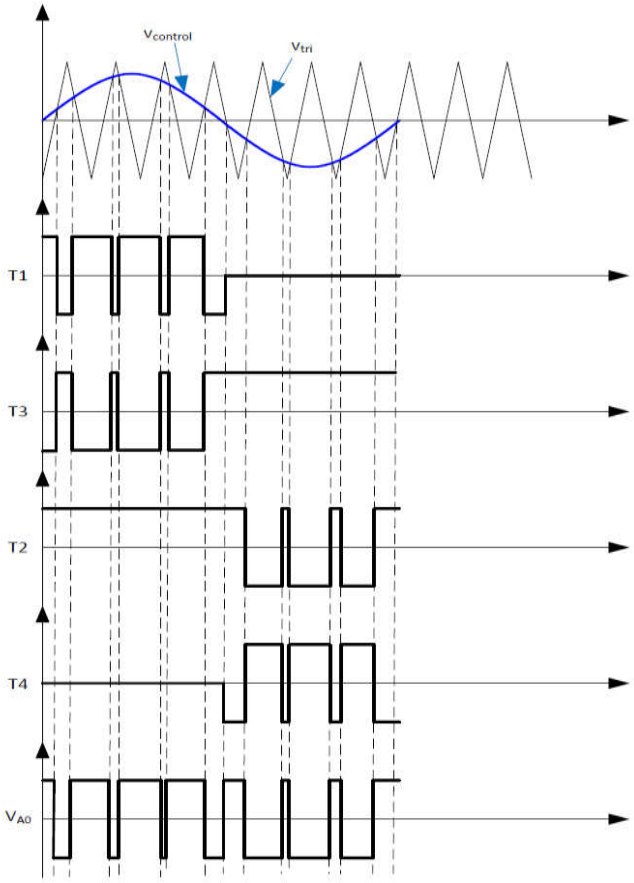

Figure 2. 4 Switching Statuses of 3L-NPC Converter [3]

2.2 Loss and Thermal Behavior of Semiconductor

The semiconductor lifetime is mainly based on mean junction temperature $T_{j,mean}$ and junction temperature difference ΔT. $T_{j,mean}$ can be defined as following equation [27]:

$$T_{j,mean} = R_{th,jh} \cdot (P_{swit} + P_{cond}) + T_h \quad (2\text{-}1)$$

where $R_{th,jh}$ represents the thermal impedance from junction to heatsink, P_{swit} is switching loss, P_{cond} is conduction loss and T_h is heatsink temperature.

The switching loss of IGBT and reverse recovery loss of FWDI are defined in equation (2-2) and (2-3) respectively [28].

$$P_{sw,igbt} = \left[E_{on}(i) + E_{off}(i)\right] \frac{V_{ce,block}}{V_{ref}} \cdot f_s \quad (2\text{-}2)$$

$$P_{rr,fwdi} = E_{rr}(i) \frac{V_{ec,block}}{V_{ref}} \cdot f_s \quad (2\text{-}3)$$

where E_{ton} and E_{toff} are switching energy losses of IGBT; E_{rr} is energy recovery loss of FWDI; $V_{ec,block}$ is the collector-emitter block voltage of IGBT that is under off-state situation, for a 3L-NPC converter it is equal to half of the DC bus voltage; V_{ref} is the collector-emitter voltage used for testing IGBT and diode; and f_s represents the switching frequency.

The conduction losses of IGBT and FWDI can be defined as following equations [28]:

$$P_{c,igbt} = V_{ce,cond}(i,T)i\frac{T_{cond}}{T_s} \tag{2-4}$$

$$P_{c,fwdi} = V_{ec,cond}(i,T)i\frac{T_{cond}}{T_s} \tag{2-5}$$

where $V_{ec,block}$ is the collector-emitter conducting voltage of IGBT that is under on-state situation and T_{cond} is the conducting period of each switching cycle.

The equivalent internal circuit of the IGBT is shown in figure 2.5 [4]. There are three parasitic capacitances in one IGBT, C_{ce}, C_{gc} and C_{ge}, they have a major impact on the switching process. According to the influence of parasitic capacitances, the IGBT switching process can be divided into eight stages, as shown in figure 2.6 [5].

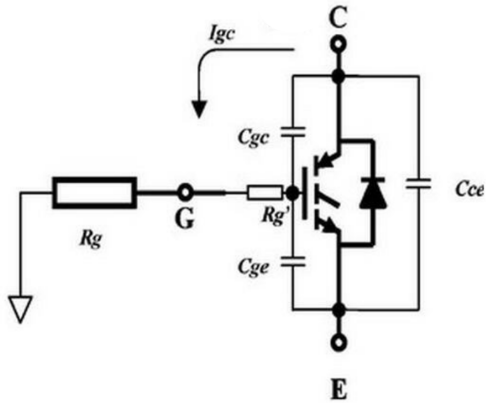

Figure 2. 5 IGBT Equivalent Circuit [4]

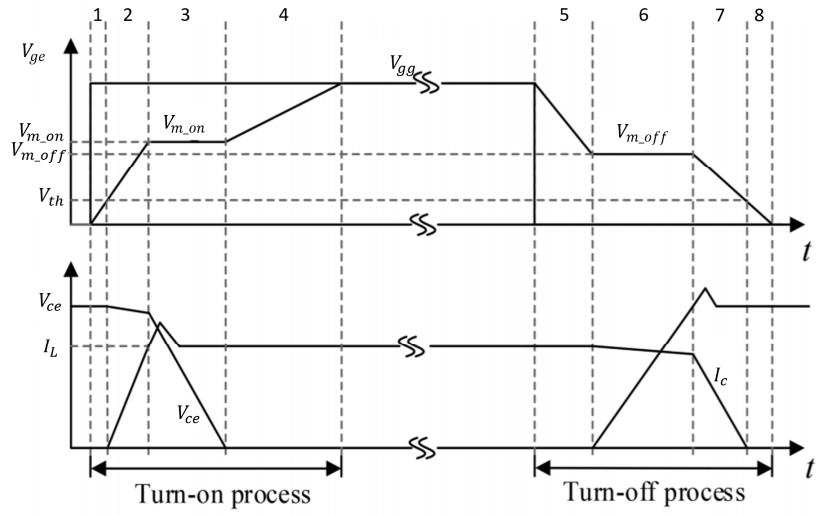

Figure 2. 6 Typical IGBT Switching Process [5]

Stage 1: Under the action of the gate drive voltage V_g, C_{gc} and C_{ge} start to charge, and the gate-emitter voltage V_{ge} rises to the threshold voltage V_{th};

Stage 2: C_{gc} and C_{ge} are continuously charged, the gate-emitter voltage keeps rising till V_m, the IGBT is turned on, and the collector current I_c begins to rise rapidly;

Stage 3: Due to the appearance of the Miller effect, the equivalent input capacitance C_{iss} is very large, which causes the voltage Miller plateau. The gate current is almost completely injected into C_{gc}, the gate-emitter voltage remains V_m, and the collector current starts to fall from the peak to a stable value (the over-shoot area represents the reverse recovery current I_f of diode);
Stage 4: The Miller effect disappears, IGBT is fully turned on, and the gate voltage continues to rise till the stable value V_{gg}.
When the fourth stage finishes, IGBT is conducted. The turn-off process of the IGBT is reversed from the turn-on process as stage 5 to stage 8 shown in figure 2.6.

2.3 Switching Frequency Regulation

From the observation of equations (2-2) and (2-3), it can be noticed that if other variables are fixed, by varying the switching frequency f_s, the IGBT switching loss and FWDI reverse recovery loss can be changed, furthermore, the mean junction temperature of semiconductors can be adjusted. As a consequence, the power converter lifetime is regulated.
The overall control system with switching frequency regulation can be set up as figure 2.7 shows [6]:

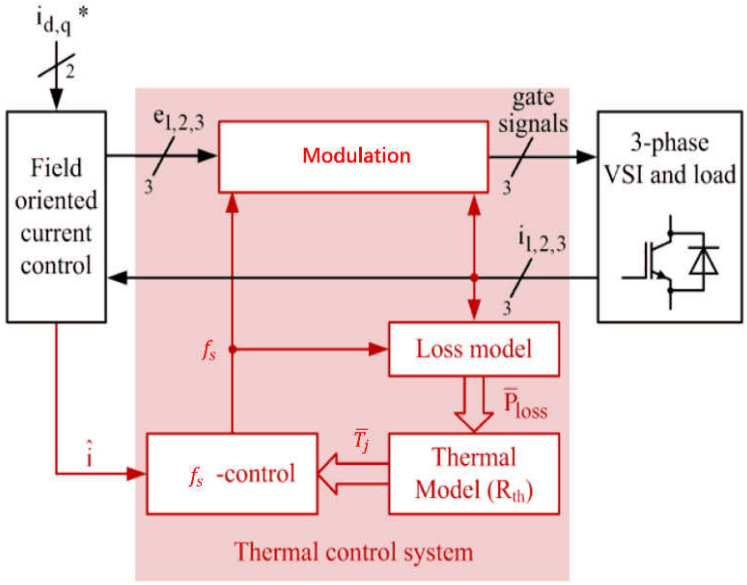

Figure 2. 7 Overall Control System Based on fs Regulation [6]

It can be seen from figure 2.7, for thermal part:
1, A switching frequency goes to thermal loss model as an input signal.
2, Based on equations (2-2) to (2-5) established in the loss model, a corresponding total thermal loss P_{loss} is achieved as a result, and it can be seen as an input signal to the thermal resistance model.
3, In the thermal resistance model, with the help of equation (2-1), a mean junction temperature can be obtained as a feedback signal to the switching frequency controller.
4, According to the value of $T_{j,mean}$, a relative judgement can be made by the fs controller, and a new corresponding switching frequency can be selected as a new input signal for the loss model.
The structure of fs controller can be established as following figure [6]:

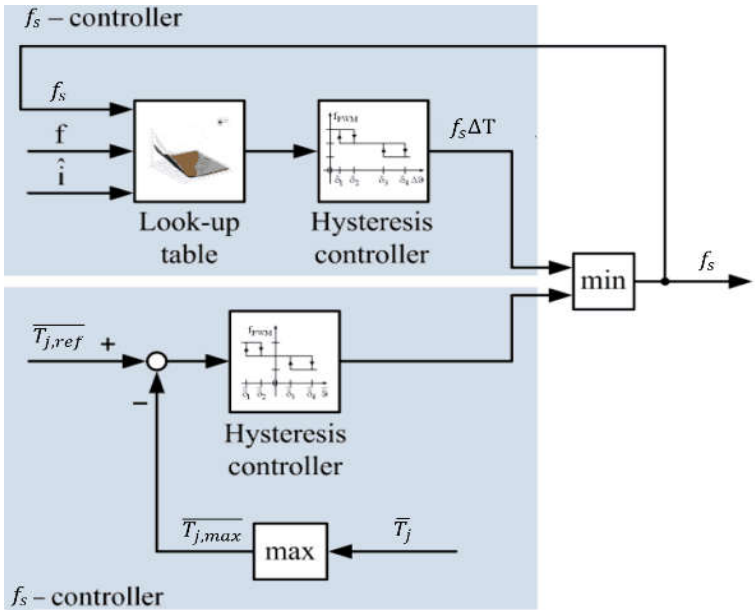

Figure 2. 8 fs Controller [6]

There are two factors determining the value of fs, one is the current affected by the switching frequency, the other one is the difference between the instantaneous maximum junction temperature and its average value. The fs look-up table contains the corresponding relation between current and switching frequency, which is built up based on a large number of data accumulation results. In order to keep the fs regulation result presents as a shape of ladder, the hysteresis controllers are added to avoid the continuous variation of switching frequency, and chapter 5 will give a particular explanation of this arrangement. The hysteresis controller diagram can be found in figure 2.9 [7].

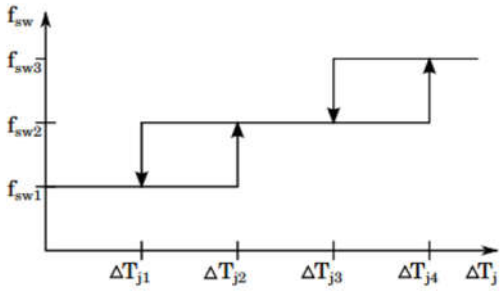

Figure 2. 9 Hysteresis Controller Diagram [7]

The hysteresis points ΔT_{j1} to ΔT_{j4} have to be set reasonable, a definition that proved good results in practice is given as following equation [7]:

$$\begin{cases} \Delta T_{j1} = 0.15 \cdot \Delta T_{j,max} \\ \Delta T_{j2} = 0.25 \cdot \Delta T_{j,max} \\ \Delta T_{j3} = 0.4 \cdot \Delta T_{j,max} \\ \Delta T_{j4} = 0.5 \cdot \Delta T_{j,max} \end{cases} \tag{2-6}$$

where $\Delta T_{j,max}$ is the maximal amplitude of thermal cycles.

Since this thesis is a continuing project based on previous study [21], which fixes the switching frequency at 2000Hz, the fs regulation could be a choice to apply to the system.

2.4 DC Bus Voltage Regulation

As it has mentioned in section 2.1, in a 3L-NPC converter $V_{ce,block} = V_{dc}/2$. For IGBT and FWDI, the relations between DC bus voltage and their switching loss and reverse recovery loss can be concluded as follows:

$$P_{sw,igbt} = [E_{on}(i) + E_{off}(i)]\frac{V_{dc}}{2V_{ref}}\frac{1}{T_s} \tag{2-7}$$

$$P_{rr,fwdi} = E_{rr}(i)\frac{V_{dc}}{2V_{ref}}\frac{1}{T_s} \tag{2-8}$$

If the switching frequency $1/T_s$ and load current are fixed, the variation of the DC bus voltage can bring the different results of switching and reverse recovery losses of semiconductors. According to equation (2-1), once those losses are changed, the junction temperature will be varied, and the thermal performance of power electronics can be regulated. The active power and reactive power from DC/AC inverter injected into the grid can be decoupled by [29]:

$$\begin{cases} \mathrm{P} = \frac{3}{2}u_m i_q \\ \mathrm{Q} = \frac{3}{2}u_m i_d \end{cases} \tag{2-9}$$

where i_d and i_q are the grid current components on d axis and q axis respectively, and u_m is the grid voltage amplitude. The generator output power can be defined as follow [29]:

$$P_g = P + P_c = \frac{3}{2}u_m i_q + U_{dc}C\frac{dU_{dc}}{dt} \tag{2-10}$$

where P_c is the capacitance power. With the dynamic adjustment of i_q, $\mathrm{P} < P_g$, the excess power flows into the capacitor, U_{dc} rises up; otherwise U_{dc} declines. The DC bus voltage can be directly controlled by adjusting i_q.

When the purpose is to decrease switching loss or reverse recovery loss, U_{dc} should be decreased by increasing i_q, however, a larger i_q brings a larger total load current, which could cause an increase in losses in theory. As for the voltage drop and the current rise, which one would play a more significant role for the losses change is difficult to judge. This thesis tends to a more intuitive control method, that is, one variable can be regulated without affecting other factors also related to thermal performance. Based on the conflict and the uncertainty brought by DC bus voltage regulation, this thesis does not take it into consideration.

2.5 Gate Voltage Regulation

The influence on the thermal performance of semiconductors achieved by varying gate voltage can be analyzed from two aspects, which are conduction loss and turn-on switching loss.

With a constant load current I_c, the decreased V_{ge} causes increased $V_{ce,cond}$, this relation can be found from the semiconductor datasheet as figure 2.10 shown [8], thus, during the conducting time, adjusting the gate voltage is equivalent to varying the collector-emitter voltage, and the conduction losses will be changed as well, as the final result, the junction temperatures are regulated to change thermal performance.

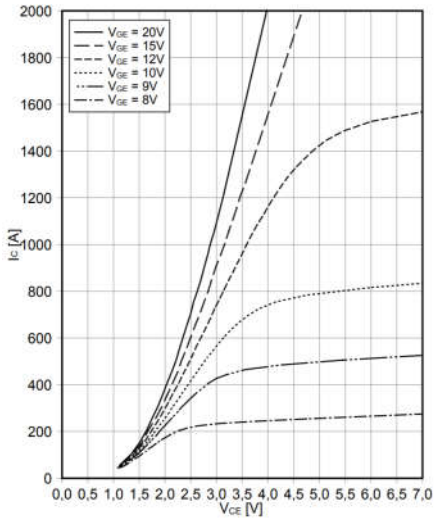

Figure 2. 10 Relation between I_c, V_{ce} and V_{ge} on IGBT [8]

The influence on turn-on switching loss brought by V_{ge} regulation is more complicated to describe. Combining the observation and analysis of figure 2.6, with the fixed parasitic capacitance, the variation of V_g actually changes the time it takes to charge C_{iss}. The switch turn-on loss that can be varied are concentrated in stage 2 and stage 3, when the collector-emitter voltage V_{ce} and load current I_L are changed simultaneously. The larger V_g, the higher V_{m_on}, the shorter charging time, and the smaller $P_{sw,on}$ will be generated. Furthermore, during stage 3, the diode reverse recovery loss P_{rr} (generated from the product of $V_{ec,block}$ and I_c overshoot area) can also be changed by V_g regulation. It can be noticed from figure 2.6, the gate drive voltage V_g is only involved in the turn-on process and conduction period of the IGBT. At the moment when the conduction time ends, the gate drive voltage will fall back to zero directly, the switch turn-off loss is not related to V_g anymore, so $P_{sw,off}$ cannot be regulated by adjusting gate voltage.

As for the implementation of gate voltage regulation, two 3D lookup tables can be established as the source of control signals, the first one for the conduction loss variation should contain the relation between junction temperature T_j, collector current I_c and gate voltage V_g, the second one for the turn-on switching loss variation should contain the relation between T_j, E_{on} and V_g. Once T_j, I_c or E_{on} exceeds an expectation level, V_g can shift values by the data recorded in the 3D lookup tables to achieve the purpose of increasing or decreasing losses at any required moment, therefore, the thermal performances are improved [30].

However, due to the limitations of the converter module datasheet, the 3D lookup tables cannot be established very accurately, the specific explanations can be found in chapter 8. Based on this issue, this thesis takes the gate voltage regulation as a recommendation for future work, the way to proceed this research in the next step will also be mentioned in chapter 8.

2.6 Power Sharing Regulation

Voltage source inverters can be coupled in parallel to share active power while keeping the frequency at a nominal value [31]. If the busbar alignment of parallel IGBT power modules have differences, it will cause the circuit impedance differences, and it will affect the current equalization of the two branches, the branch owns small impendence will share more current. To

get a quantitative analysis of the influence of the thermal imbalance, all of drive circuits, circuit parameters, copper bus bars, and components are supposed to be symmetrical, as shown in figure 2.11 [9].

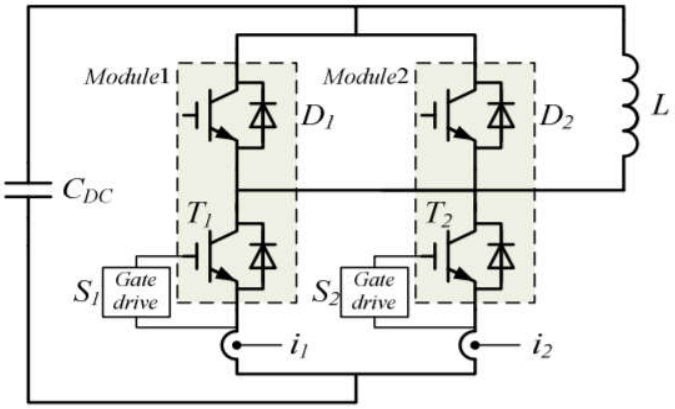

Figure 2. 11 Main Power Circuit Impedance Diagram [9]

In the controlled manner which is shown in figure 2.12 [10], by delaying the turn on and turn off signal, the current balancing under transient situation can be obtained. The function of the transient current-controller is to delay times of T_{don} and T_{doff}. Digital mode implements the control algorithm, and it is synchronized with the switching signal.

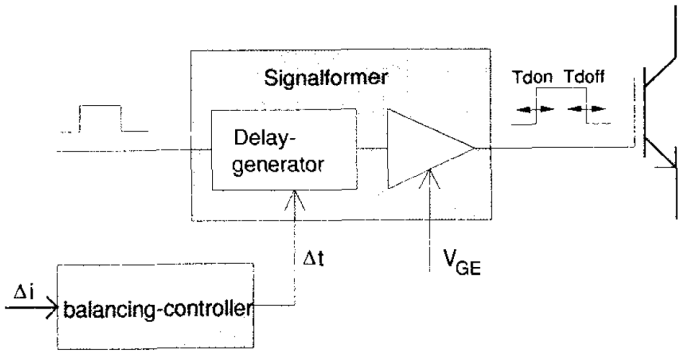

Figure 2. 12 Transient Current Balancing [10]

The purpose of controlling the conducting IGBTs gate voltage V_{ce} is to gain the static current balancing. By applying an analogue control system or a signal processor, the controller can be completed. The static current balancing diagram can be found in figure 2.13 [10].

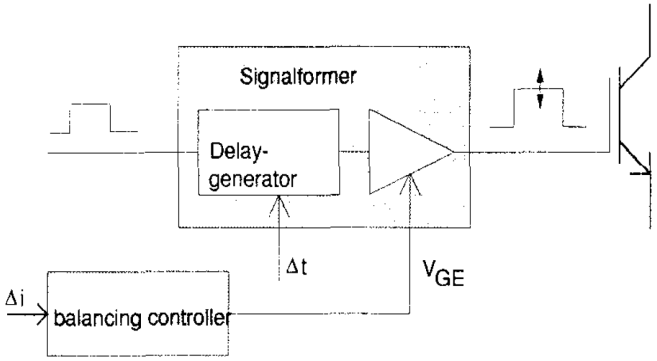

Figure 2. 13 Static Current Balancing [10]

In this case, the junction temperature of semiconductors can be further reduced by power sharing of IGBT modules in parallel, however, for a wind power system, the hardware design of converters has already considered parallel connection since the flow-in current is pretty large. The principle of power sharing regulation is similar to reactive current regulation, since they both circulate current between converters.

2.7 Reactive Current Regulation

Currently, one of the unignorable reasons based on the effects of converter lifetimes in wind power system is because of the grid is usually supported by wind generators via reactive power injection [32]. Once the reactive current has been regulated, the total current changes, and both of the switching loss and conduction loss of semiconductor are changed. [33] discusses the thermal distribution of back-to-back power converter based on a DFIG system and the reactive power circulation between the rotor side converter and the grid side converter. As a result, injecting the reactive power circulation appropriately, the thermal performance is regulated as well as the power converter lifetime. Since the principles of reactive current regulation is very easy to understand, and implementation is relatively simple, it could be another choice for the research in this thesis.

2.8 Active Cooling Control

The PMDD generator adopts the full power converter, and its capacity is approximately three times higher than DFIG. Large capacity also means that its AC system becomes more complex, increasing the risk of IGBT breakdown and so on. It needs to configure a better cooling system, meanwhile, the energy consumption of the converter cooling system also increases. Based on those issues, [34] advises a system that supplies adaptive cooling, based on the semiconductor temperature, the system has the ability to adjust the cooling system efficiency. The junction temperature cycles can be reduced by this cooling system which is dynamically controlled, and higher lifetime can be reasonable achieved. [35] indicates an active cooling control based on the variation of the cooling air flow speeds of the fan located in front of heatsink. The principle of this method can be summarized as when T_j exceeds the expected level, the fan controller can provide a command to accelerate the cooling air; when T_j drops below the expected level, it can decrease the cooling air. However, the implementation of the active cooling control is based on a large number of experimental tests. Since this thesis does not have an experiment plan, the active cooling control has been excluded.

2.9 Summary of Literature Review

This chapter introduces six commonly used active control methods from the two aspects: their principles and how to implement them. Switching frequency regulation and DC bus voltage regulation improve thermal performance by varying switching loss; gate voltage regulation, power sharing regulation and reactive current regulation aim at changing both switching loss and

conduction loss among them, only the regulation of V_g only can bring different switching loss during turn-on process, the other two regulations can change both turn-on and turn-off switching losses. Active thermoelectric cooling adopts a more direct physical cooling method, it starts from the improvement of the internal structure of the components.

This thesis will mainly focus on the comparison of the active controls between the switching frequency regulation and reactive current regulation. Their modeling and simulation results will be demonstrated in chapter 5 and 6 respectively. In chapter 7 of the thesis, the power electronic lifetimes based on these two different active control methods will be specifically quantified. As it mentioned in section 2.5, due to the limited datasheets of the 3L-NPC converter module has been used in this thesis, the gate voltage regulation cannot be adopted sufficiently, however, it will also be discussed as recommendation for future work in chapter 8.

3.Thermal Modelling of Power Electronics

The modeling of losses and junction temperatures of power electronics plays an important role in the reliability evaluation and lifetime prediction of converters. There are two types of thermal model used currently, the first one is based on the physical modelling of internal components and structure, the second one is based on lumped parameters.

To adopt the loss model based on the physical structure of power electronic components, the internal structure of semiconductors, the material equivalent circuit with parameters and micro working process should be modeled in detail, so it is complicated for engineering applications due to long calculation and modelling time. The lumped parameter based model depends on a large number of test data, and it uses a set of mathematical functions to emulate the relation between the semiconductor losses and temperature. Compared with the physical modeling, the advantage of this method is that the simulation speed is fast, so it is very suitable for on-line real-time calculation of semiconductor loss.

In a three-phase converter, the losses from IGBT and freewheeling diode (FWDI) can be separated into three parts, which are conduction loss (P_c), switching loss (P_{sw}) and diode reverse recovery (P_{rr}). The approaches to calculate them have been mentioned from equations (2-2) to (2-5).

The integral thermal model consists of the loss model and the thermal impedances equivalent circuit. R_{jc} presents the thermal resistance from junction to case, R_{cf} is the thermal resistance from case to heatsink, and they both can be found from the datasheet of the semiconductor. The complete thermal model structure is shown in figure 3.1.

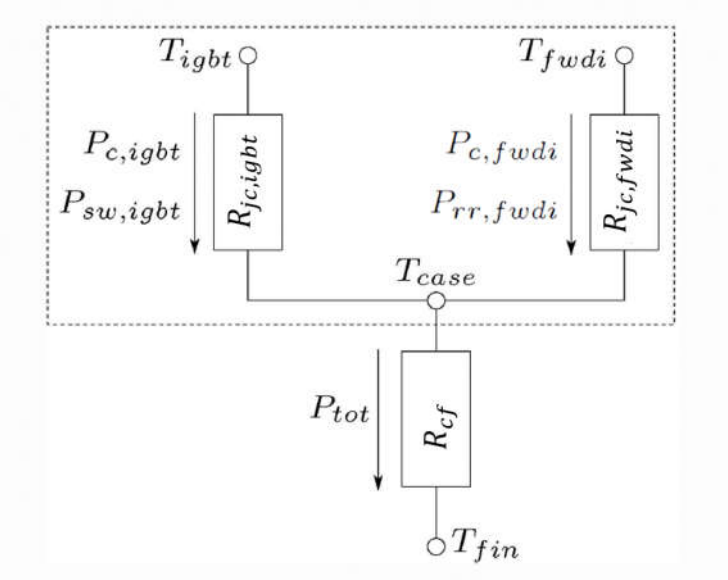

Figure 3. 1 Thermal Impedance Network

Contents of chapter 3 are as follows:

1, Modelling of losses in semiconductors.

2, Introduction to the thermal equivalent circuit of the semiconductors.

3, Introduction to the wind profile used to test the active control methods.

3.1 Loss Model

The internal loss of the IGBT module is mainly produced in the IGBT chip and diode chip, and the loss is influenced by the load current, DC voltage, chip junction temperature, gate drive resistance and gate drive voltage. The load current, the DC voltage and the chip junction temperature are related to the specific application conditions and operating conditions. The gate drive resistance is related to specific design. Therefore, the loss calculation must take the effects of these four factors into account.

3.1.1 Conduction Loss Model of IGBT and FWDI

The conduction loss is related to the current flowing through the chip and the junction temperature, u_{CE} and u_F are used to express the conduction voltage drop of IGBT chip and FWDI chip under a certain junction temperature respectively. The chip currents of IGBT and FWDI are expressed by i_c and i_F, and the calculation expression of the IGBT conduction loss P_{conT} and the diode conduction loss P_{conD} can be defined as follows [36]:

$$P_{conT} = u_{CE}(t) \cdot i_c(t) \cdot d_T \tag{3-1}$$

$$P_{conD} = u_F(t) \cdot i_F(t) \cdot d_F \tag{3-2}$$

The on-state voltages u_{CE} and u_F can be calculated by formulas [37]:

$$u_{CE}(i_c) = V_{CE0} + r_{CE} \cdot {i_c}^{A_{CE}} \tag{3-3}$$

$$u_F(i_F) = V_{F0} + r_F \cdot {i_F}^{A_F} \tag{3-4}$$

where V_{CE0} is the on-state zero-current collector-emitter voltage and V_{F0} the corresponding zero-current diode voltage while r_{CE} and r_F are the collector-emitter on-state resistance and diode on-state resistance respectively. A_{CE} and A_F are the curve fitted constants for the IGBT and the diode respectively. Therefore, the conduction loss model of IGBT and diode can be set up based on equations (3-3) and (3-4).

FZ1000R33HE3 is selected as the 3L-NPC converter model in this thesis. It should be noticed that the relationship between I_c and V_{ce} or I_f and V_f is usually given separately in the datasheet at three different junction temperature levels, as figures 3.2 and 3.3 shown below [8]. Under the same current I_c, the saturation voltage drop V_{ce} corresponding to the high junction temperature is larger than that with the low junction temperature, therefore, V_{ce} should be solved according to different junction temperature levels, and so does V_f.

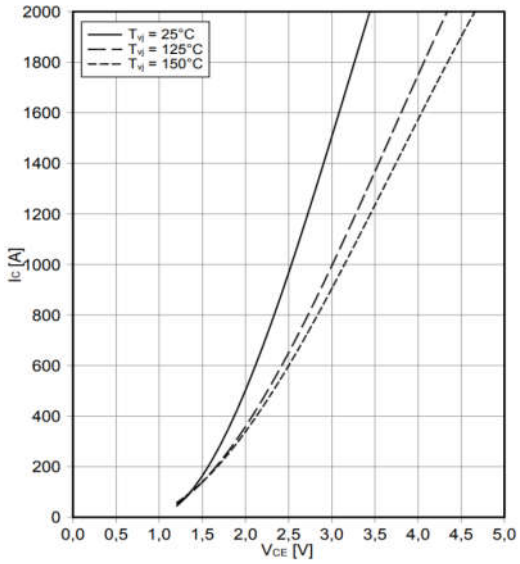

Figure 3. 2 Relation between I_c and V_{ce} on IGBT [8]

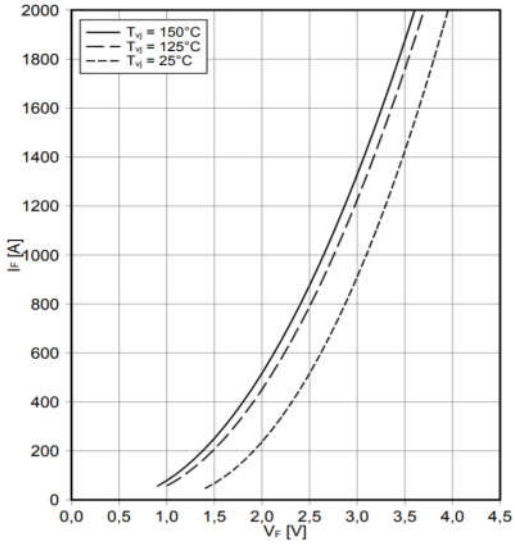

Figure 3. 3 Relation between I_f and V_f on FWDI [8]

Substituting different values of V_{ce} and V_f generated by low level junction temperature (25℃) and high level junction temperature (25℃) separately into equations (3-3) and (3-4), P_{conT_TL}, P_{conT_TH}, P_{conD_TL} and P_{conD_TH} can be achieved, and the total conduction loss model of each semiconductor can be established based on linear extrapolation equations (3-5) and (3-6) [38].

$$P_{conT} = P_{conT\_TL} + \frac{P_{conT\_Tj} - P_{conT\_TL}}{P_{conT\_TH} - P_{conT\_TL}} \tag{3-5}$$

$$P_{conD} = P_{conD\_TL} + \frac{P_{conD\_Tj} - P_{conD\_TL}}{P_{conD\_TH} - P_{conD\_TL}} \tag{3-6}$$

3.1.2 Modelling of Switching Energy Calculation

The factors that affect IGBT switching loss and diode reverse recovery loss include load current, DC voltage, chip junction temperature and gate drive resistance. The switching process of voltage and current is very complex and cannot be described with simple expressions. Therefore, switching loss and reverse recovery loss are usually not calculated from analytical equations, but they can be obtained from experimental test data, which are available in datasheet.

In general, under the specific gate voltage V_g, collector to emitter voltage V_{ce} and the chip junction temperature T_j, the datasheet gives the curve of IGBT switching turn-on loss E_{onT} and switching turn-off loss E_{offT} as a function of the collector current I_c; and the diode reverse recovery loss E_{revD} as a function of the reverse recovery current I_f. The details of the datasheet based on E_{onT}, E_{offT} and E_{revD} are shown in figures 3.4 and 3.5 [8].

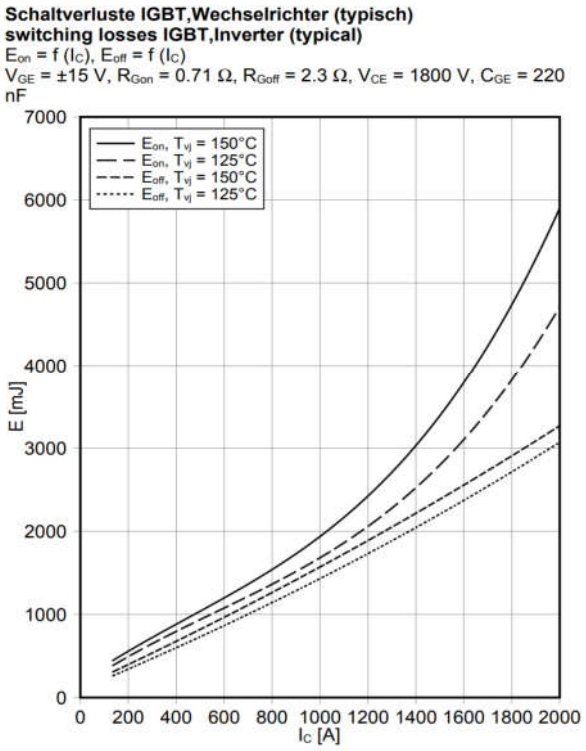

Figure 3. 4 Relation between E_{onT}, E_{offT} and I_c [8]

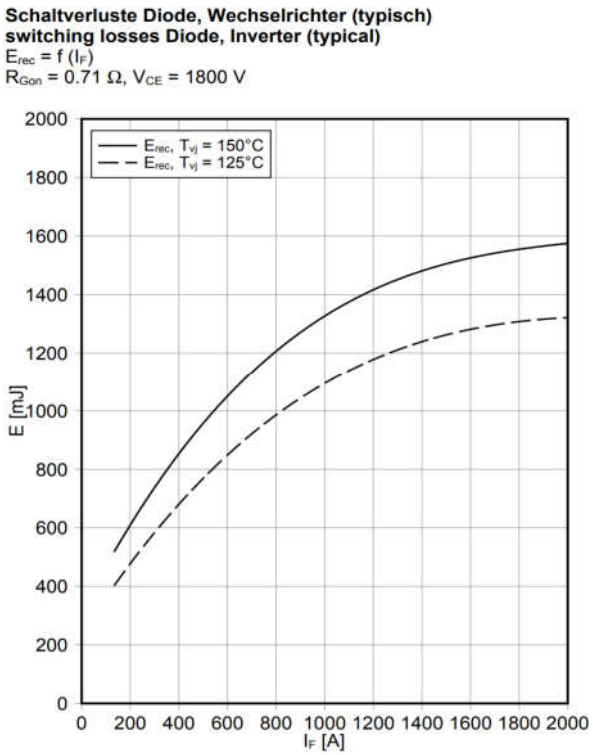

Figure 3. 5 Relation between E_{revD} and I_f [8]

[39] indicated that using a second-order polynomial equation is more accurate to describe the curve graphs shown above, therefore equations (3-7), (3-8) and (3-9) given below are the approaches to achieve E_{onT}, E_{offT} and E_{revD}.

$$E_{onT} = a_{T2on} \cdot {i_{CE}}^2 + a_{T1on} \cdot i_{CE} + a_{T0on} \tag{3-7}$$

$$E_{offT} = a_{T2off} \cdot {i_{CE}}^2 + a_{T1off} \cdot i_{CE} + a_{T0off} \tag{3-8}$$

$$E_{revD} = a_{T2rev} \cdot {i_F}^2 + a_{T1rev} \cdot i_F + a_{T0rev} \tag{3-9}$$

where a_{T2on}, a_{T1on}, a_{T0on}, a_{T2off}, a_{T1off}, a_{T0off}, a_{T2rev}, a_{T1rev} and a_{T0rev} are fitting constants. According to these equations, the calculation model of switching loss and reverse recovery loss can be established.

Similar to the conduction loss model, losses are dependent on junction temperature as well. With the help of linear extrapolation, the switching loss model of each IGBT and the reverse recovery loss model of each FWDI can be obtained based on equations (3-10) and (3-11) [38].

$$P_{switT} = P_{switT\_TL} + \frac{P_{switT\_Tj} - P_{switT\_TL}}{P_{switT\_TH} - P_{switT\_TL}} \tag{3-10}$$

$$P_{revD} = P_{revD\_TL} + \frac{P_{revD\_Tj} - P_{revD\_TL}}{P_{revD\_TH} - P_{revD\_TL}} \tag{3-11}$$

3.2 Thermal Equivalent Circuit Model

The physical structure of IGBT is complicated, it is mainly composed of chip, bond wire, ceramic substrate, solder layers and copper baseplate. The schematic diagram of the structure is shown in figure 3.6 [11]. The heat is mainly generated in the chip, when IGBT is operating, under the effects of voltage and current, the heat power loss will be created in the PN junction of the chip. This heat

will be transmitted to the copper baseplate through the other layers of the IGBT module. As a consequence, the heat is dissipated by an external heatsink, in order to ensure that the heatsink and the baseplate are fully contacted, the thermal paste is generally used between them.

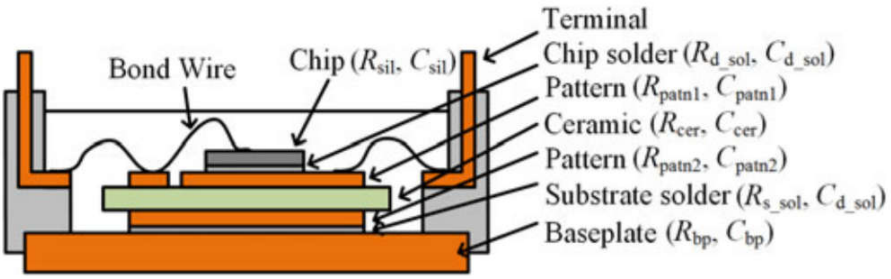

Figure 3. 6 Architecture of an IGBT Module [11]

The heat generated on the PN junction of the IGBT chip can be viewed as being dissipated through three processes, which are chip to case, case to heatsink, and heatsink to ambient. Each process has its own thermal resistance, the chip to case thermal resistance is defined as R_{thjc}, the case to heatsink thermal resistance is defined as R_{thch}, and the heatsink to ambient thermal resistance is defined as R_{thha}. The temperature differences are generated with the heat dissipation that go through each process, as shown in figure 3.7 [11], and the conventional lumped thermal equivalent circuit (TEC) for an IGBT module is shown in figure 3.8 [11].

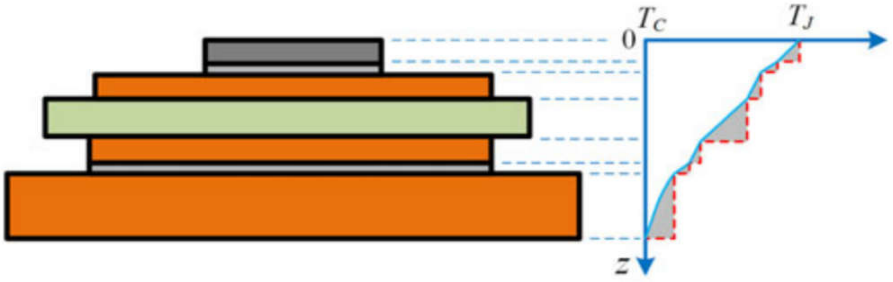

Figure 3. 7 IGBT Heat Dissipation Schematic [11]

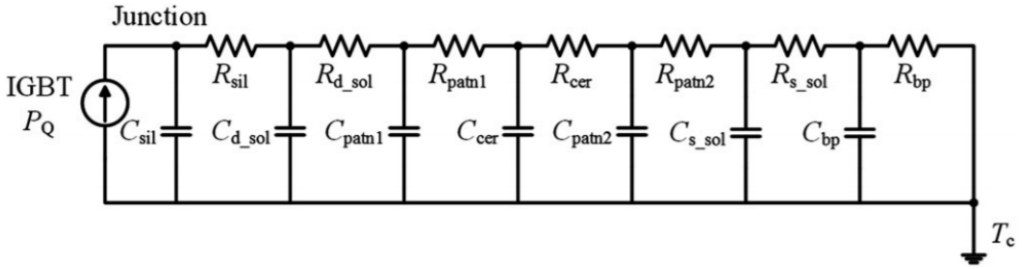

Figure 3. 8 Conventional lumped TEC for an IGBT module [11]

According to figure 3.8, the thermal model of IGBT and FWDI junctions can be implemented as the transfer functions in figure 3.9

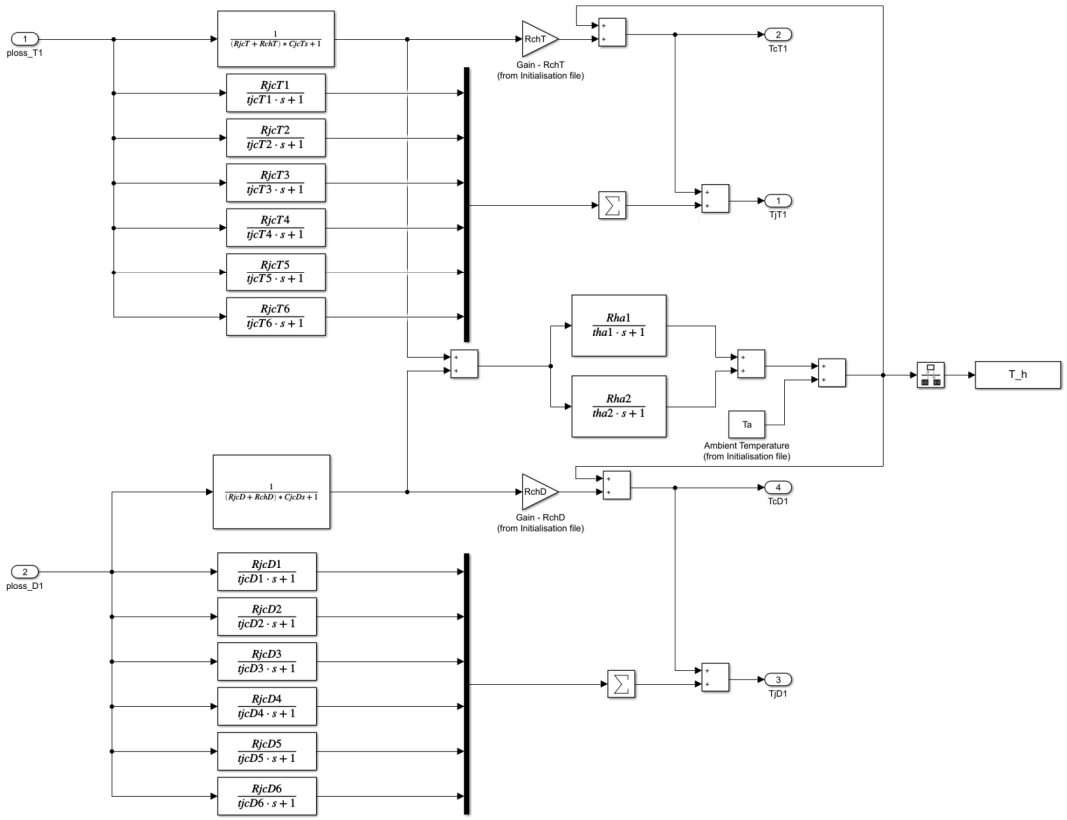

Figure 3. 9 Thermal Functions Transfer Model

3.3 Wind Profile Model

The model from previous study [21] only works around fixed average wind speed varying in limited range, which is not possible to demonstrate thermal amplitudes changing because of the limited speed variation. Since one of the most important targets in this thesis is to decrease the large thermal amplitudes ΔT_j in big thermal cycles, the wind speed model has to be extended, and the manually set profile is to test the effectiveness of control. The wind profile can be found in figure 3.10, and the principle of it is giving the small wind disturbances every 1s while providing big wind disturbances every 10s. However, the reality should be considered as an issue to aware.

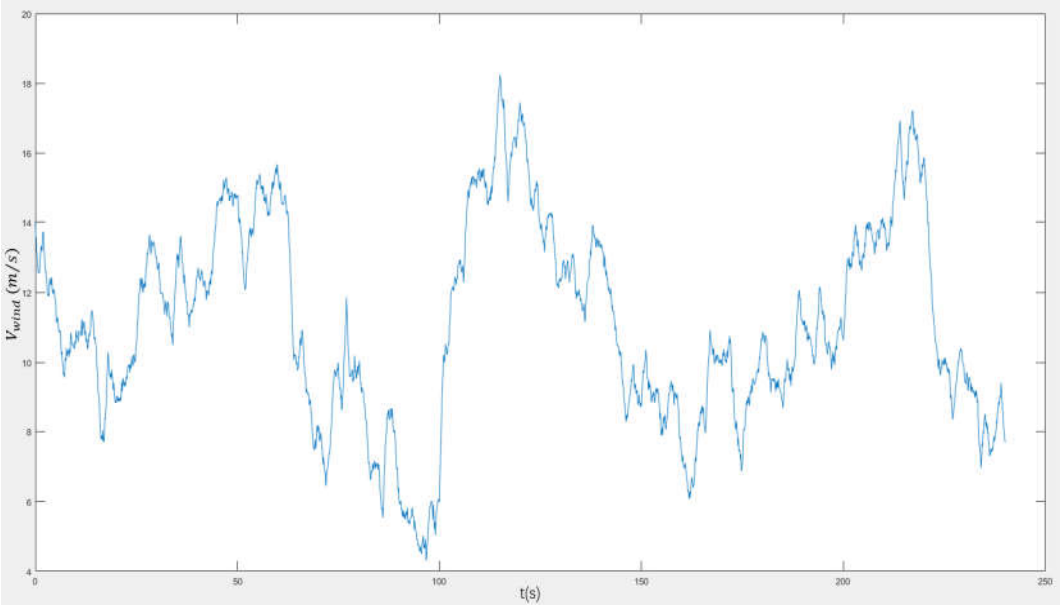

Figure 3. 10 Manually Set Wind Profile

3.4 Summary of Thermal Modelling

In this chapter, the implementation of the thermal model of power electronics is described in detail based on the lumped parameter equivalent circuits and curves from datasheet of the IGBT module. The approaches to calculate conduction loss, switching loss, reverse recovery loss and the junction temperature are discussed in detail. The model built in this chapter will be used as the basics to simulate active control methods in following chapters.

4. Modulations Based on 3L-NPC Converter

Since the pulse-width modulation (PWM) technique plays a crucial role in the performance of multi-level converters, the author decided to do the research into the thermal performance of different modulation techniques applied in the system. Chapter 4 includes the following contents:
1, Introduction to some commonly used modulation strategies.
2, Choices of modulation techniques based on the characteristics of 3L-NPC converter.
3, Apply the chosen modulation techniques to grid side and generator side of the system separately; compare the different semiconductor thermal performances brought by them.

4.1 Pulse-Width Modulation Technology

There are many ways to implement PWM, and they can be divided into two types which are carrier-based PWM and non-carrier PWM.

4.1.1 Carrier-based PWM

Subharmonic pulse width modulation (SHPWM) uses multiple triangular carriers and sinusoidal waves who have same frequency and amplitude to determine the on and off actions of switching devices in multi-level converters. N-1 carriers are required for the converter with N level, and the middle points of these carriers are zero reference points [12]. SHPWM is a respectively simple and easy modulation to achieve.
Compared with SHPWM, a zero-sequence voltage is added to the modulation wave in the switching frequency optimal pulse width modulation (SFOPWM) [13,40]. This modulation is only applicable to three-phase symmetrical load systems, when it is used in a single-phase system, the output voltage will be influenced by the third harmonics.
There is a certain phase shift between adjacent carriers in the phase shift pulse width modulation (PSPWM), compared with SHPWM and SFOPWM, PSPWM has the ability to increase equivalent switching frequency by increasing the equivalent carrier frequency, and this modulation is mostly used for the cascaded multi-level converters [14,41,42].
When the modulation index is relatively high, the variable frequency carrier bands pulse width modulation (VFCPWM) overcomes the drawbacks of the previous three modulations by increasing the frequency of the middle carrier, the action frequency of switching devices is balanced, meanwhile, the equivalent switching frequency is increased [15].
According to the principles of these four carrier-based PWMs, different modulation waveforms can be shown as follow:

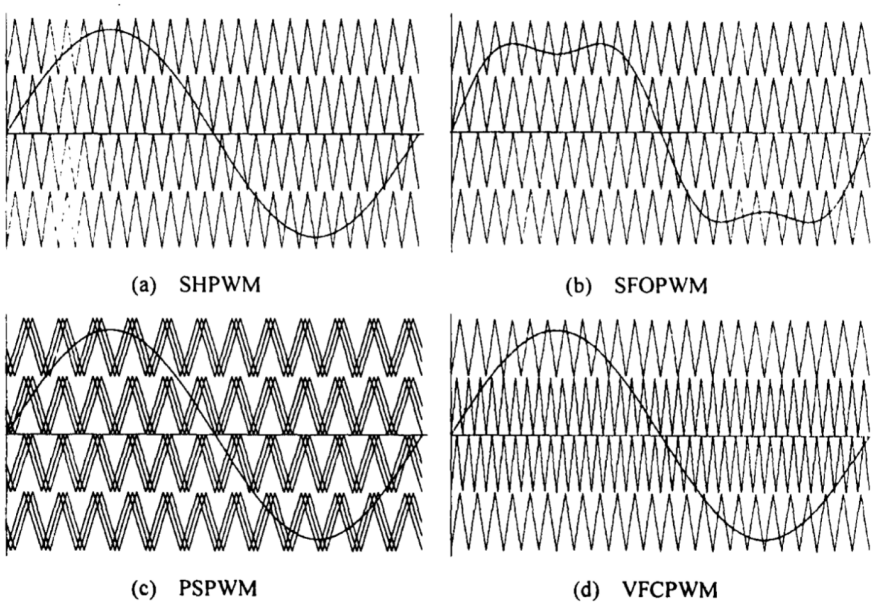

Figure 4. 1 Four Types of Carrier-based PWM [12,13,14,15]

Except the four carrier-based modulations illustrated above, flat top quasi-sinusoidal pulse width modulation (FTPWM) is a relatively novel modulation method, it uses triangular carrier sampling to generate three-phase PWM signals, compared to sinusoidal pulse width modulation (SPWM), the amplitude of the maximum output line voltage in the linear area is 19% higher [43], and it improves the DC voltage utilization significantly. In the over modulation area, it expands the modulation wave width to continue increasing the fundamental wave until the system gains the square wave as the output. Flat top quasi-sinusoidal modulation has the advantages with both simple algorithms and low total harmonic distortion (THD).

4.1.2 Non-carrier-based PWM

There are many non-carrier-based pulse-width modulations, and the most typical ones include space vector pulse width modulation (SVPWM), selective harmonic elimination pulse width modulation (SHEPWM), and hysteresis control PWM.

SVPWM uses the vectors which correspond to the converter switch state to synthesize the given vector. This modulation has flexible vector selections and high voltage utilization, however, the algorithm is very complex when a converter is designed more than five levels, which limits the extent of its application under certain conditions [44-48].

SHEPWM can eliminate any number of harmonics, and it can achieve clear waveforms of the output voltage and the output current with low harmonic content. The only disadvantage of SHEPWM is that needs to calculate large amounts of data offline, so it is inconvenient to support a spot debugging [49].

It is easy to obtain a clear current waveform by adopting hysteresis control PWM, and it has a small output current harmonic ripple. This modulation is usually applied in the systems which have strict requirements about the noise and high needs for the switching frequency. Nevertheless, due to the significant change of the switching frequencies, the hysteresis control PWM is hardly used in the large capacity converter with low switching frequency [50].

4.1.3 Modulation Technique Choices of 3L-NPC Converter

Choosing the optimal PWM is one of the prerequisites for a 3L-NPC converter to gain a good performance. As it is mentioned before, SHEPWM requires a lot of offline data, and hysteresis control PWM has large variations of the switching frequency. Compared to SPWM, excellent transient effects, larger linear modulation range, low output voltage harmonics and simple controlled DC side voltage equalization can be concluded as the characteristics of SVPWM. Therefore, for the 3L-NPC converter topology, SVPWM has been mostly applied, it is also one of the most popular research topics at current time.

The vector optimization in the SVPWM is necessary to adopt in order to obtain the reliable operation of the inverter. In order to decrease switching losses, the vector selection method indicated in [51] changes the traditional seven-segment SVPWM into four-segment, however, there is a large increase of the output voltage harmonics of the inverter.

After analyzing these different modulations, the author decided to apply non-carrier-based seven-segment SVPWM and carrier-based FTPWM to the system in sequence, and then the different thermal performances they brought can be compared with the thermal results generated by SPWM in the original model. The modulation with the best thermal performance can be selected to combine with the active controls later.

4.2 Space Vector Pulse Width Modulation (SVPWM) and Its Equivalent Alternative

4.2.1 Principles of SVPWM

In a 3L-NPC converter, the switches of each phase have three states, which are -1(N), 0(O), 1(P), and their corresponding AC side output voltage is -E, 0 and E respectively. For a three-phase symmetric system, a total number of 3^3 (27) possibilities of the switch states can be created, and each switch state corresponds to a voltage space vector. The voltage space vectors are demonstrated in figure 4.2 [16,17].

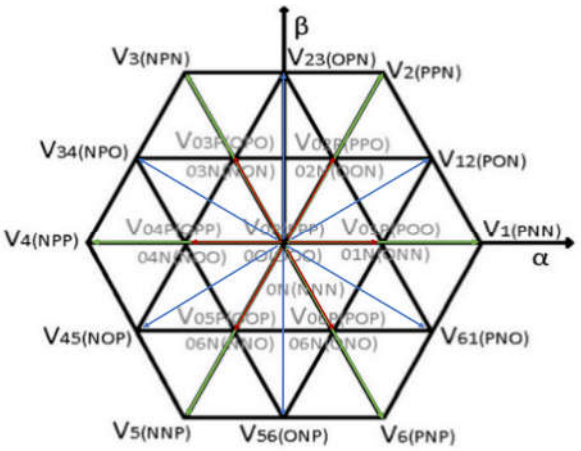

Figure 4. 2 Voltage Space Vector Distribution of 3L-NPC Converter [16,17]

The six vertices of the large hexagon are the positions of the six large vectors, each vertex of the small hexagon represents two vectors (P-type small vector and N-type small vector), thus, there are 12 small vectors, and 3 zero voltage vectors are all located at the midpoint of the hexagon, the rest of vectors are the 6 medium vectors. Table 4.1 shows the vectors and their corresponding amplitudes. These vectors can be represented by the following equation [52]:

$$\mathrm{V} = \frac{2}{3}\left(U_{ao} + U_{bo}e^{j\frac{2}{3}\pi} + U_{co}e^{-j\frac{2}{3}\pi}\right) = \frac{4E}{3}(T_a + T_b e^{j\frac{2}{3}\pi} + T_c e^{-j\frac{2}{3}\pi}) \quad (4\text{-}1)$$

where U_a, U_b and U_c express the voltages of A, B and C phases respectively, and T_a, T_b and T_c represent the switch states of A, B and C phases respectively.

Large vectors	$V_1, V_2, V_3, V_4, V_5, V_6$	Amplitude($4E/3$)
Medium vectors	$V_{12}, V_{23}, V_{34}, V_{45}, V_{56}, V_{61}$	Amplitude($2E/\sqrt{3}$)
P-type small vectors	$V_{01P}, V_{02P}, V_{03P}, V_{04P}, V_{05P}, V_{06P}$	Amplitude($2E/3$)
N-type small vectors	$V_{01N}, V_{02N}, V_{03N}, V_{04N}, V_{05N}, V_{06N}$	Amplitude($2E/3$)
Zero small vectors	V_{0P}, V_{0O}, V_{0N}	Amplitude(0)

Table 4. 1 Voltage Space Vectors and Amplitudes of Three-level Converter

In a 3L-NPC converter, if the state of phase A is P, T_{a1} and T_{a2} are switched on; if the state of phase A is O, T_{a2} and T_{a3} are turned on; if the state of phase A is N, T_{a3} and T_{a4} are switched on. In figure 4.2, for example, $V_{12(PON)}$ represents T_{a1}, T_{a2}, T_{b2}, T_{b3}, T_{c3} and T_{c4} are switched on. The rest of vectors also can be analyzed in this way.

In the αβ coordinate system of figure 4.2, six sectors can be divided by a counterclockwise rotation based on the α axis, every 60 ° is a sector, and figure 4.3 shows the vectors of 0th sector and their time distribution [16].

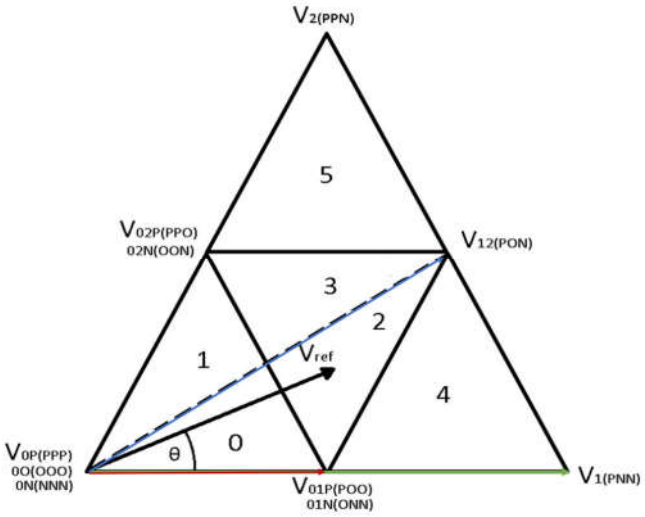

Figure 4. 3 Vectors of 0th Sector and Time Distribution [16]

The seven-segment SVPWM is adopted in this thesis. In Figure 4.3, if the reference voltage vector V_{ref} is located in region 2 and the DC side capacitor voltage is balanced, the voltage vectors adjacent to V_{ref} can be expressed as [52]:

$$V_{01} = \frac{2}{3}E, V_{12} = \frac{2}{\sqrt{3}}Ee^{j\frac{\pi}{6}}, V_1 = \frac{4}{3}E, V_{ref} = Ve^{j\theta} \quad (4\text{-}2)$$

V_{ref} is synthesized by these three vectors adjacent to it, so that:

$$T_{POO} + T_{ONN} + T_{PON} + T_{PNN} = T_s \quad (4\text{-}3)$$

$$V_{01P}T_{POO} + V_{01N}T_{ONN} + V_{12}T_{PON} + V_1T_{PNN} = V_{ref}T_s \quad (4\text{-}4)$$

where T_{POO}, T_{ONN}, T_{PON} and T_{PNN} are the durations of the vectors V_{01P}, V_{01N}, V_{12} and V_1 in one switching period T_s respectively.

From equation (4-2) and (4-4), it can be combined as:

$$\frac{2}{3}ET_{POO} + \frac{2}{3}ET_{ONN} + \frac{2}{\sqrt{3}}E\left(\cos\frac{\pi}{6}\right)T_{PON} + \frac{4}{3}ET_{PNN} = V(\cos\theta)T_s \quad (4\text{-}5)$$

where V represents the maximum value of the phase voltage of 3L-NPC converter, and E is the voltage value on each capacitor of the DC side. The sequences of SVPWM in 0th sector can be found in figure 4.4 [18], and N is the neutral point of the DC bus.

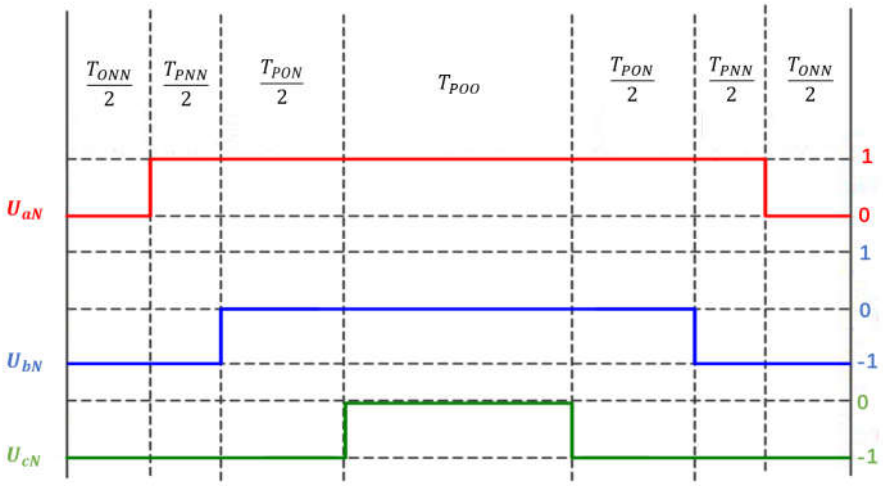

Figure 4. 4 Sequences of SVPWM 0th sector [18]

Due to the amplitude of output voltage is E, equation (4-6) can be achieved from figure 4.4.

$$\begin{cases} U_{aN}T_s = E(T_{PNN} + T_{PON} + T_{POO}) \\ U_{bN}T_s = E(T_{PON} + T_{POO}) \\ U_{cN}T_s = ET_{POO} \end{cases} \quad (4\text{-}6)$$

Thus,

$$\begin{cases} u_a = \frac{(T_{PNN}+T_{PON}+T_{POO})}{T_s} \\ u_b = \frac{(T_{PON}+T_{POO})}{T_s} \\ u_c = \frac{T_{POO}}{T_s} \end{cases} \quad (4\text{-}7)$$

Since the SVPWM model related to 3L-NPC converter includes a lot of switching selections, the simulation runs pretty slow. In order to record the performance of semiconductors with few big thermal cycles, the system has to be observed for a long time. To ensure the simulation model operating with an acceptable speed, the author decided to seek an alternative modulation which has the same modulation output as seven-segment SVPWM but owns simple simulation model and high operation velocity. The carrier-based symmetrical pulse width modulation (SYPWM) as the chosen equivalent approach of SVPWM will be introduced and established in the next section.

4.2.3 SYPWM Modelling

A universal expression of modulation signals $u_i(t)$ $(\mathrm{i} = \mathrm{a}, \mathrm{b}, \mathrm{c})$ for carrier-based three-phase PWM modulators is as follows [19]:

$$u_i(t) = u_i^*(t) + e_i(t) \tag{4-8}$$

where $e_i(t)$ are injected harmonics, and $u_i^*(t)$ represents the three-phase symmetrical sinusoidal signals as follows [19]:

$$\begin{cases} u_a^*(t) = m\sin\omega t \\ u_b^*(t) = m\sin(\omega t + \frac{2\pi}{3}) \\ u_c^*(t) = m\sin(\omega t + \frac{4\pi}{3}) \end{cases} \tag{4-9}$$

where m is the modulation index, and $u_a^*(t) + u_b^*(t) + u_c^*(t) = 0$. Thus, the line-to-neutral voltages $U_{iN}(i = a, b, c)$ for 3L-NPC converter can be expressed as follows:

$$\begin{cases} U_{aN}(t) = E[m\sin\omega t + e_i(t)] \\ U_{bN}(t) = E[m\sin(\omega t + \frac{2\pi}{3}) + e_i(t)] \\ U_{cN}(t) = E[m\sin(\omega t + \frac{4\pi}{3}) + e_i(t)] \end{cases} \tag{4-10}$$

The zero-sequence signal e_i is usually calculated by [53]:

$$e_i = \frac{1}{3}(u_a + u_b + u_c) \tag{4-11}$$

Thus, for a 3L-NPC converter, with the help of equation (4-7), the representation of e_i can be found as follow:

$$e_i = \frac{T_{PNN}}{3T_s} + \frac{2T_{PON}}{3T_s} + T_{POO} \tag{4-12}$$

The definition based on the distributions of T_{ONN} and T_{POO} in 0th sector can be written as:

$$\begin{cases} T_{POO} = K_0(\omega t)\cdot(T_S - T_{PNN} - T_{PON}) \\ T_{ONN} = [1 - K_0(\omega t)]\cdot(T_S - T_{PNN} - T_{PON}) \end{cases} \tag{4-13}$$

where K_0 is a factor that determines the durations of application of zero-state vectors V_{ONN} and V_{POO}, $1 \geq K_0(\omega t) \geq 0$, $T_{POO} \geq 0$ and $T_{ONN} \geq 0$. When $1 \geq K_0(\omega t) = k_0 = constant \geq 0$, the corresponding SVPWM has been discussed in [53]. The unique zero-sequence signal and the unified definition for $e_i(t)$ which determine a carrier-based PWM can be demonstrated as following equation [19]:

$$\begin{aligned} e_i &= K_0(\omega t)(1 - u_{max}^*) + [1 - K_0(\omega t)](-1 - u_{min}^*) \\ &= k_0(1 - u_a^*) + (1 - k_0)(-1 - u_c^*) \end{aligned} \tag{4-14}$$

[53] indicated that SYPWM can be brought by equation (4-15), and figure 4.5 shows the linear modulation range with the maximum modulation index $m_{max} = 2/\sqrt{3}$ [19].

$$e_i(t) = \frac{1}{2}(1 - u_{max}^*) + \frac{1}{2}(-1 - u_{min}^*) \tag{4-15}$$

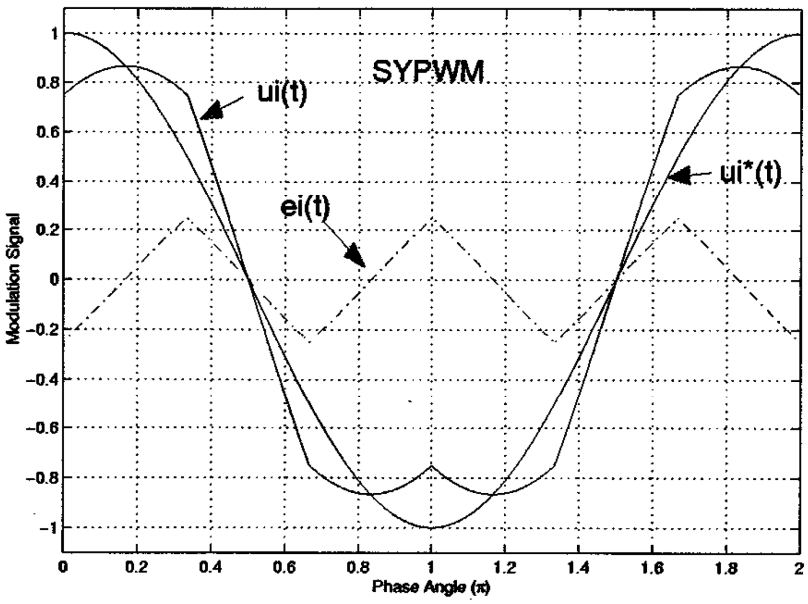

Figure 4. 5 Modulation Signal of SYPWM [19]

With SYPWM, the corresponding T_{ONN} and T_{POO} in 0th sector is shown in equation (4-16), which matches the vector duration relations of seven-segment SVPWM.

$$T_{ONN} = T_{\mathrm{POO}} = \frac{1}{2}(T_S - T_{PNN} - T_{PON}) \tag{4-16}$$

As this thesis uses the mathematical Matlab model, transferring three-phase voltages into duty ratio mode is easier to give the switching signals directly to each semiconductors of 3L-NPC converters. Based on figure 2.4, the switching statues of 3L-NPC converter can be summarized as follow:

		T_1	T_2	T_3	T_4
$v_{control} > 0$	$v_{control} > v_{tri}$	1	1	-1	0
	$v_{control} < v_{tri}$	-1	1	1	0
$v_{control} < 0$	$v_{control} > v_{tri}$	0	1	1	-1
	$v_{control} < v_{tri}$	0	-1	1	1

Table 4. 2 Different States of 3L-NPC IGBT switches

The voltage duty ratio transformation from three-phase to separate switch signals of T1, T2, T3 and T4 can be implemented by following the relations in table 4.3:

Positive cycle	Negative cycle
$d_1 = \frac{V_{out}}{V_{dc}}$	$d_1 = 0$
$d_2 = 1$	$d_2 = 1 - d_4$
$d_3 = 1 - d_1$	$d_3 = 1$
$d_4 = 0$	$d_4 = -\frac{V_{out}}{V_{dc}}$

Table 4. 3 Switching Duty Ratios of 3L-NPC Converter

The voltage duty ratio based on dq coordinate can be generated by following equation:

$$\begin{cases} D_d = \frac{V_d}{V_{dc}} \\ D_q = \frac{V_q}{V_{dc}} \end{cases} \tag{4-17}$$

With the inputs of D_{dq} and the rotational angle θ, the voltage duty ratio regards to abc coordinate can be achieved by Park and Clarke transformations. For a three-phase voltages system:

$$v_a = V_{peak}\cos(\omega_0 t) \tag{4-18}$$

$$v_b = V_{peak}\cos(\omega_0 t - \frac{2\pi}{3}) \tag{4-19}$$

$$v_c = V_{peak}\cos(\omega_0 t - \frac{4\pi}{3}) \tag{4-20}$$

The peak value of the phase voltage V_{peak} is equal to $\sqrt{2}V_{P\,RMS}$, where $V_{P\,RMS}$ is the root-mean-square (RMS) value of the phase voltage. The duty ratio waveform of three-phase input voltages is illustrated in figure 4.6.

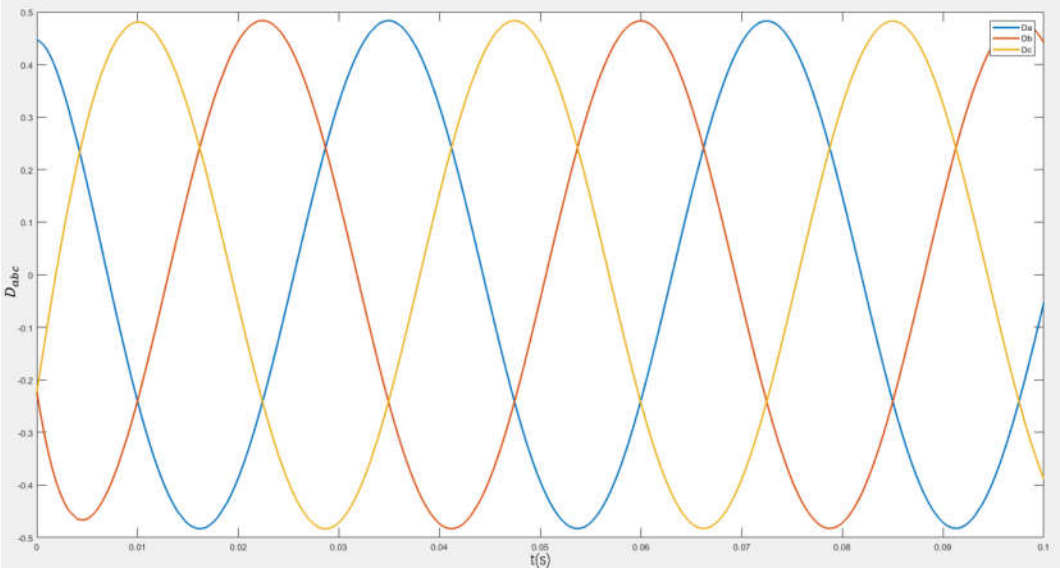

Figure 4. 6 Duty Ratio Waveform of Three-phase Input Voltage

The maximum phase voltage can be concluded as the positive terminal voltage:

$$v_{max} = \max(v_a, v_b, v_c) \tag{4-21}$$

The minimum phase voltage can be considered as the negative terminal voltage:

$$v_{min} = \min(v_a, v_b, v_c) \tag{4-22}$$

The period of these two periodic waveforms is equal to one third of the line period, in the other words, their frequency is as three times higher as the line frequency. With Fourier series expansion, the maximum phase voltage, which represents the positive terminal voltage can be expressed as [54]:

$$v_{max} = \frac{3\sqrt{3}}{\pi}V_{peak}\left[\frac{1}{2} + \sum_{n=1}^{+\infty}\frac{(-1)^{n+1}}{9n^2-1}\cos(3n\omega_0 t)\right] \tag{4-23}$$

The Fourier series expansion of the negative terminal voltage is:

$$v_{min} = \frac{3\sqrt{3}}{\pi}V_{peak}\left[-\frac{1}{2} + \sum_{n=1}^{+\infty}\frac{(-1)^{n+1}}{9n^2-1}\cos(3n\omega_0 t)\right] \tag{4-24}$$

Since the spectral components of v_{max} and v_{min} are regularly offset at even triples of the line frequency [54], n is defaulted to be an odd number. The sum of v_{max} and v_{min} can be written as:

$$v_{max} + v_{min} = \frac{3\sqrt{3}}{\pi}V_{peak}\sum_{n=1}^{+\infty}\frac{2}{9n^2-1}\cos(3n\omega_0 t) \tag{4-25}$$

The duty ratio waveforms of the maximum phase voltage and the minimum phase voltage are shown in figure 4.7.

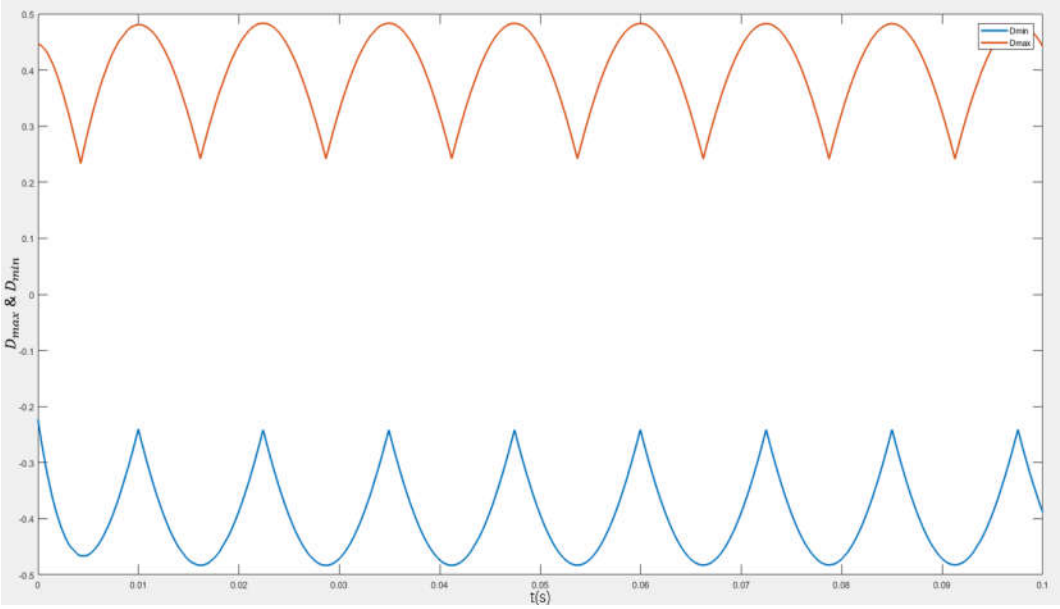

Figure 4. 7 Duty Ratio Waveforms of v_{max} and v_{min}

Zero is the constant value of the sum of the instantaneous values of the three-phase voltages:

$$v_a + v_b + v_c = 0 \tag{4-26}$$

At each point of time, one of the phase voltages stays on the track of v_{max} waveform, another one is located at the waveform of the minimum phase voltage, and the remaining one can be expressed as v_{re}. Thus, the sum of v_{max}, v_{min} and v_{re} is equal to zero as well, the following equation can be summarized as the expression for v_{re}:

$$v_{re} = -v_{max} - v_{min} = -\frac{3\sqrt{3}}{\pi} V_{peak} \sum_{n=1}^{+\infty} \frac{2}{9n^2-1} \cos(3n\omega_0 t) \tag{4-27}$$

The duty ratio waveform of the remaining voltage is shown in figure 4.8.

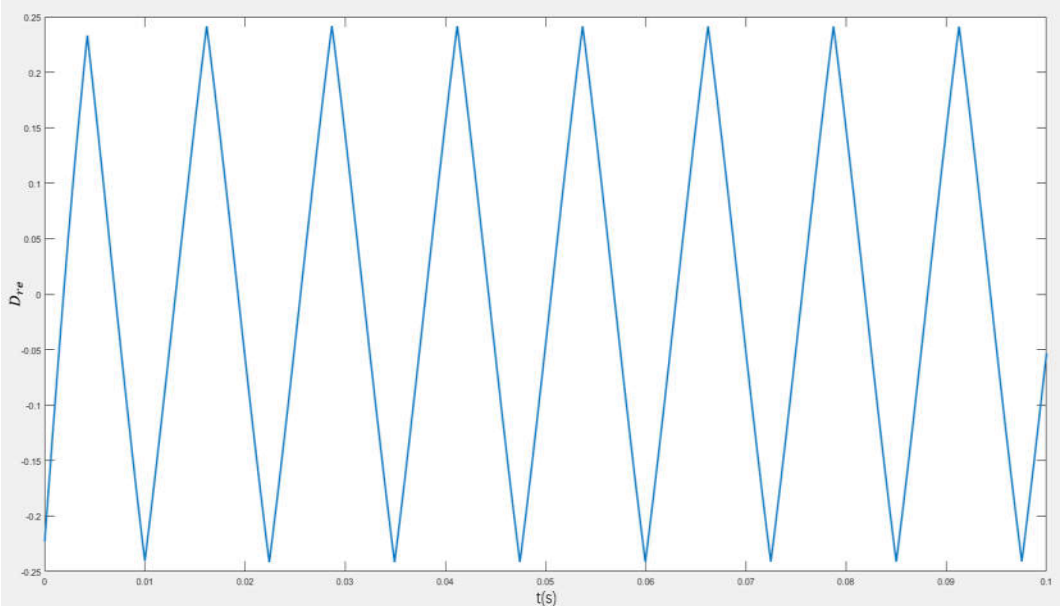

Figure 4. 8 Duty Ratio Waveform of v_{re}

Thus, half of the remaining voltage can be found as:

$$\frac{v_{re}}{2} = -\frac{1}{2}(v_{max} + v_{min}) = -\frac{3\sqrt{3}}{\pi} V_{peak} \sum_{n=1}^{+\infty} \frac{1}{9n^2-1} \cos(3n\omega_0 t) \quad (4\text{-}28)$$

Equation (4-28) gives the definition of SYPWM $e_i(t)$ that is shown in equation (4-15) and figure 4.5 with Fourier series expansion, and the superimposition of the three-phase sinusoidal fundamental waveform and the symmetrical zero-sequence signal completes SYPWM.

According to the previous explanations, the seven-segment SVPWM equivalent Matlab model, which is the SYPWM model can be set up as following:

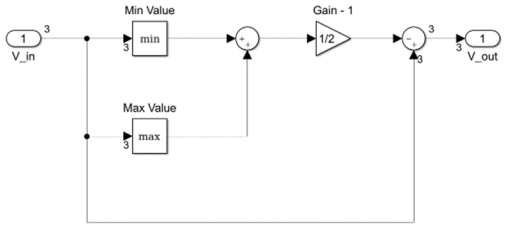

Figure 4. 9 SYPWM Matlab Model

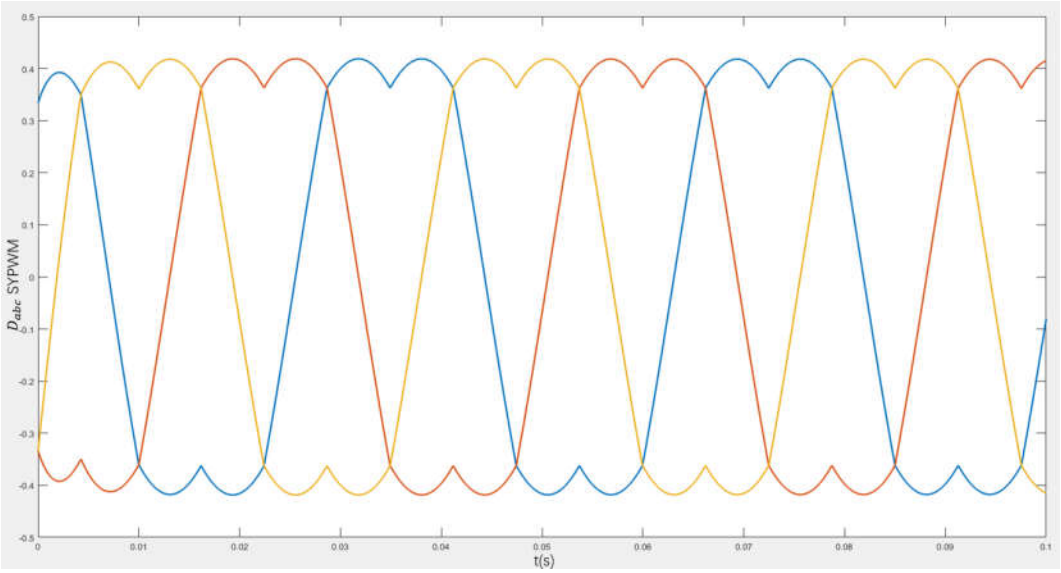

Figure 4. 10 Modulation Waveform of SYPWM

The generated saddle modulation waveform is shown in figure 4.10, comparing with the three-phase input voltages in figure 4.6, the amplitude of the modulation waveform is 0.134 times smaller than its in the fundamental waveform, which verifies their relation that has been demonstrated in figure 4.5.

4.2.3 Thermal Simulation Results with SYPWM

Adding the SYPWM to both grid side and generator side, let the system run 240s to ensure all the electronic components operating under steady state thermal conditions. When the system operates separately with the original SPWM and with SYPWM, this thesis compares the different thermal performances of each semiconductor under the fixed external situations, such as the wind profile and the ambient temperature of the electronics.

The comparison charts of average total thermal loss (the sum of switching loss and conduction loss) on each semiconductor under different modulations can be found in figures 4.11 and 4.12.

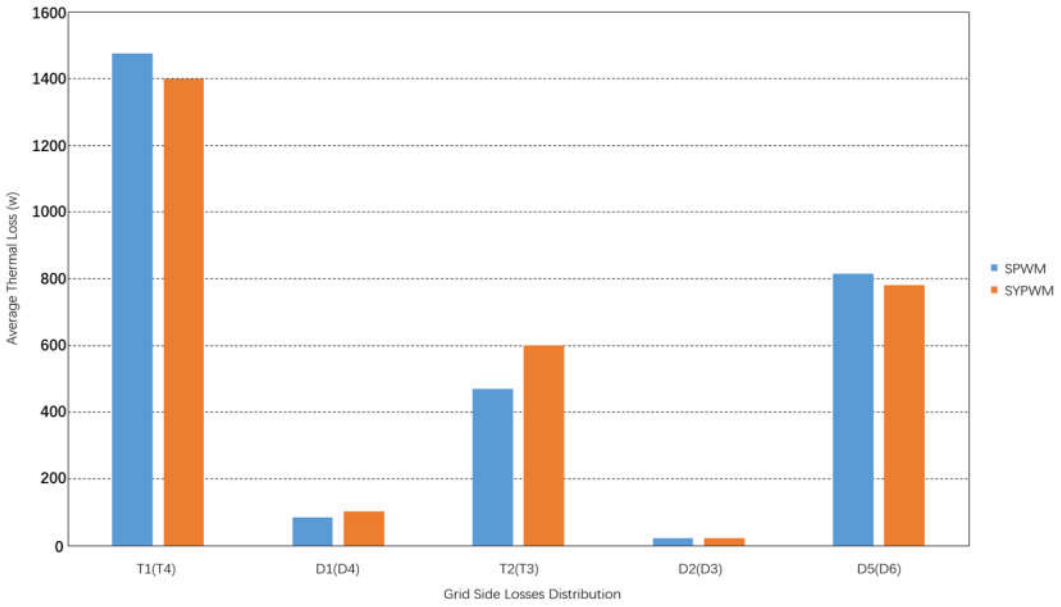

Figure 4. 11 Average Thermal Losses Distribution of Semiconductors at Grid Side (with 2 Modulations)

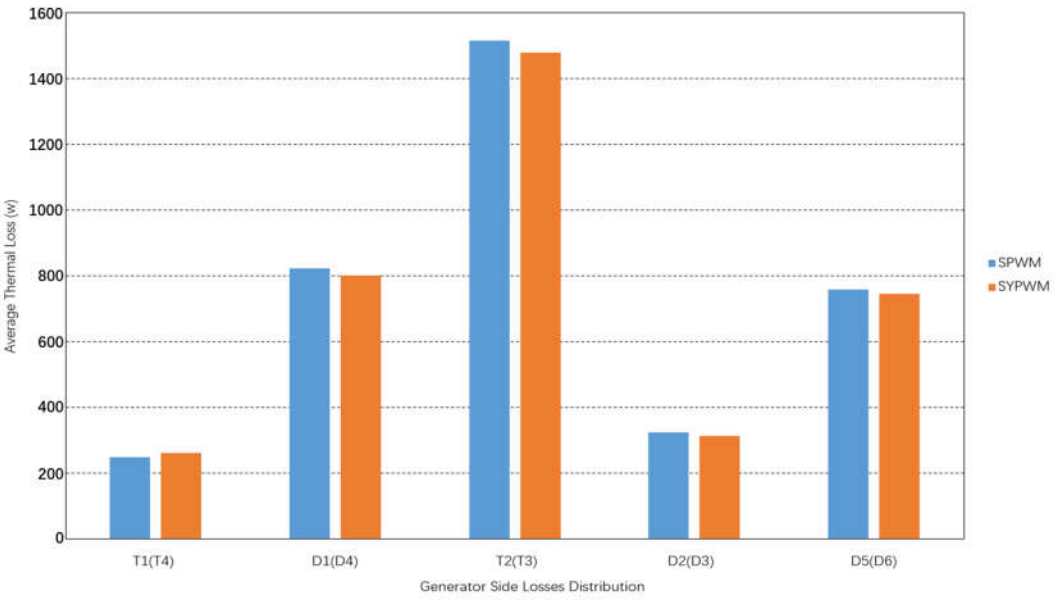

Figure 4. 12 Average Thermal Losses Distribution of Semiconductors at Generator Side (with 2 Modulations)

The three-phase current is not affected by different modulations significantly, however, the voltage is changed to saddle shape after the system adopting SYPWM, and it influences the conduction time of each semiconductor directly by eliminating the peak region of the original sinusoidal waveform. For a 3L-NPC converter, T1 and T4 have the same conducting behavior, because they both have constant switch off time in a half period of modulation waveform, T2 and T3 behave the same, they switch on and off more often depending on the positions of modulation wave and carrier wave. Similarly, their freewheeling diodes D1 and D4, D2 and D3 also have same conducting behavior respectively. D5 and D6 are the busiest diodes with freewheeling. From the results demonstrated in figures 4.11 and 4.12, at the grid side, T1(T4) and D5(D6) have relatively high thermal losses, and they are reduced after applying SYPWM. At the generator side, except T1(T4),

the thermal losses of the rest semiconductors achieve slightly decreases when the system is modulated by SYPWM.

With SYPWM, taking T1 from the grid side as an example, the results of its junction temperatures after the system running 0.5s and 240s are illustrated in figure 4.13 and figure 4.14 respectively.

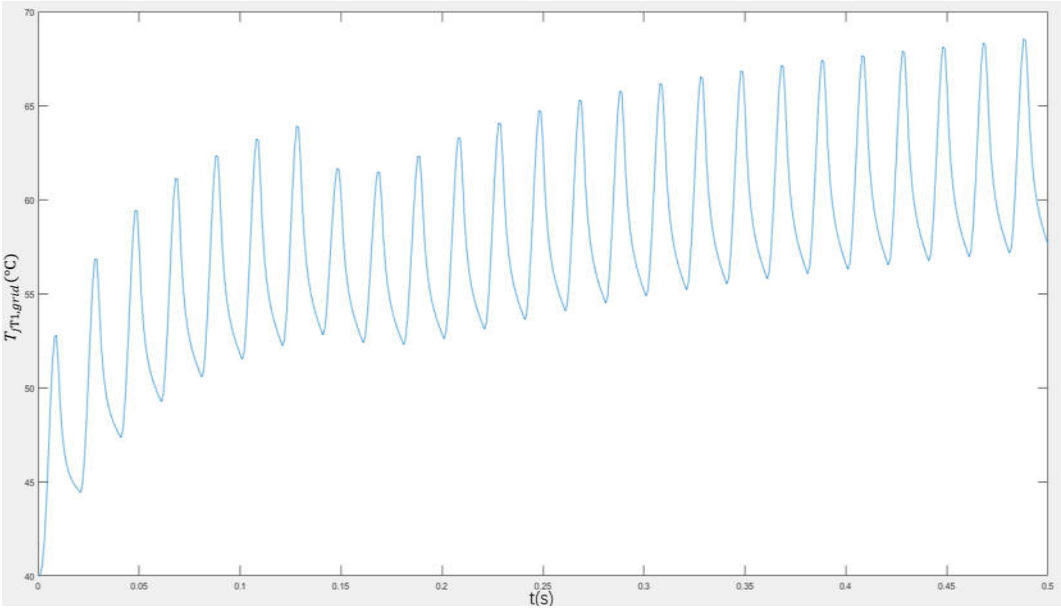

Figure 4. 13 $T_{jT1,grid}$ after 0.5s with SYPWM

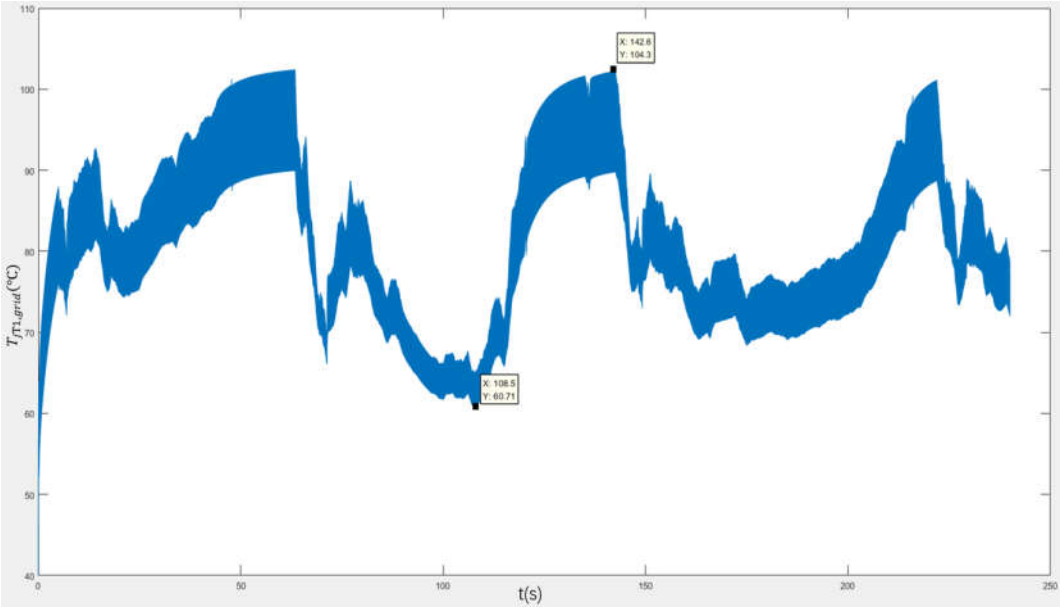

Figure 4. 14 $T_{jT1,grid}$ after 240s with SYPWM

It can be seen from figure 4.13, the junction temperature oscillates every 0.02s, and due to the grid side has constant electrical frequency as 50Hz, every electrical period the junction temperatures of the grid side components oscillate one time. Similarly, observing T1 from the generator side, the results of its junction temperature is illustrated in figure 4.15.

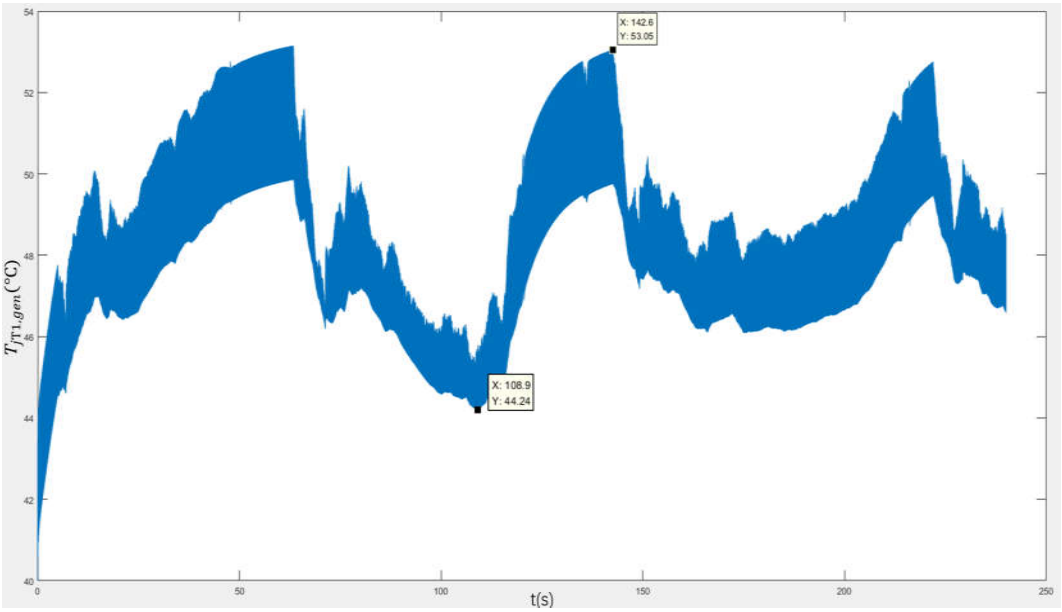

Figure 4. 15 $T_{jT1,gen}$ after 240s with SYPWM

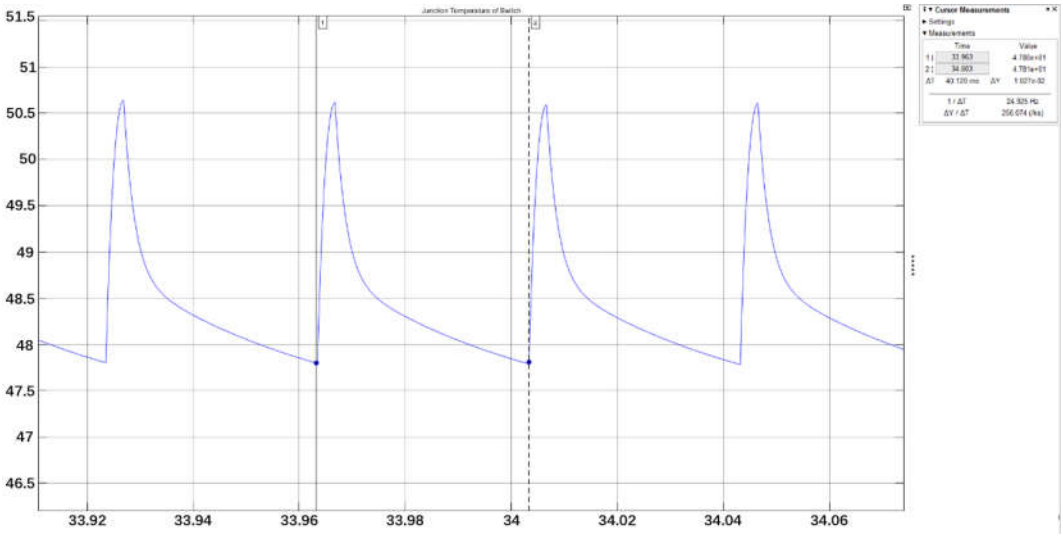

Figure 4. 16 Oscillation Period of $T_{jT1,gen}$ around 34s

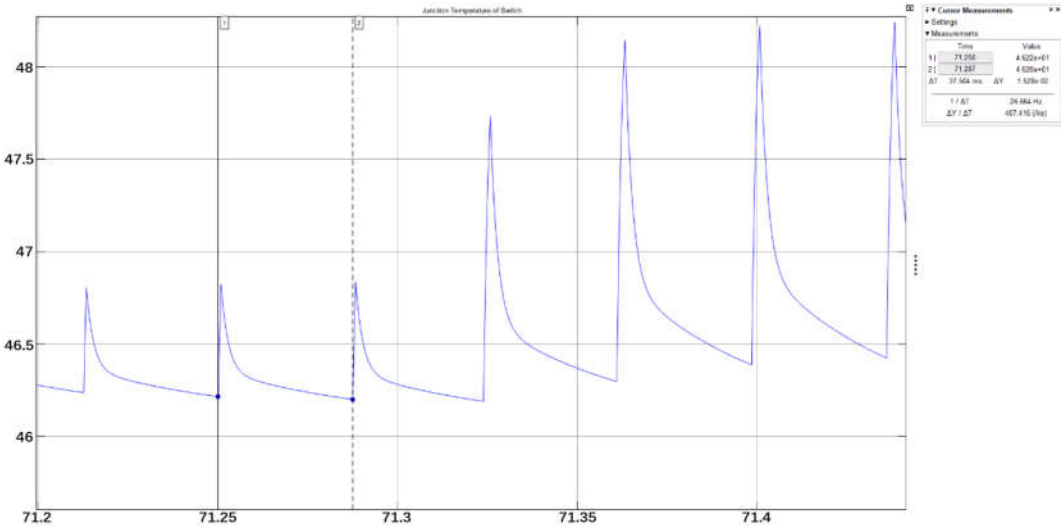

Figure 4. 17 Oscillation Period of $T_{jT1,gen}$ around 71s

Due to the wind turbine and the rotor of PMDD generator are directly connected, unlike grid side has the unique electrical frequency, the periods of the junction temperature oscillation from generator side are not fixed anymore. Figure 4.16 shows one of the $T_{jT1,gen}$ oscillation period when the system is operating around 34s, which is 40.120ms; and figure 4.17 shows the other oscillation period of $T_{jT1,gen}$ when the system works over 71s, which is 37.504ms. It can be noticed that the junction temperature oscillation periods from generator side are changed all the time depending on the wind speed, when the wind blows fast, the T_j oscillation period is short, and the frequency of T_j is relatively high, in the opposite, the frequency of T_j is low when the wind speed is low. There is a phenomenon in figures 4.13, 4.16 and 4.17 that cannot be ignored, the waveform of T_j is more similar to pulse instead of sinusoidal, because the switching loss of each semiconductor is much larger than the conduction loss.

Since mean junction temperature is a major factor influencing the semiconductor lifetime, the $T_{j,mean}$ statistic results of all semiconductors by using SPWM and SYPWM on both sides are shown separately in table 4.4 and table 4.5.

Mean junction temperatures on different components ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	81.0967
$T_{jD1mean,grid}(T_{jD4mean,grid})$	48.8976
$T_{jT2mean,grid}(T_{jT3mean,grid})$	50.9862
$T_{jD2mean,grid}(T_{jD3mean,grid})$	43.5643
$T_{jD5mean,grid}(T_{jD6mean,grid})$	77.4765
$T_{jT1mean,gen}(T_{jT4mean,gen})$	47.2109
$T_{jD1mean,gen}(T_{jD4mean,gen})$	79.0176
$T_{jT2mean,gen}(T_{jT3mean,gen})$	82.1346
$T_{jD2mean,gen}(T_{jD3mean,gen})$	62.8945
$T_{jD5mean,gen}(T_{jD6mean,gen})$	74.8712

Table 4. 4 $T_{j,mean}$ Values of 3L-NPC Components with SPWM

Mean junction temperatures on different components ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	78.8676
$T_{jD1mean,grid}(T_{jD4mean,grid})$	49.0357
$T_{jT2mean,grid}(T_{jT3mean,grid})$	52.9873
$T_{jD2mean,grid}(T_{jD3mean,grid})$	43.5582
$T_{jD5mean,grid}(T_{jD6mean,grid})$	76.6219
$T_{jT1mean,gen}(T_{jT4mean,gen})$	47.6682
$T_{jD1mean,gen}(T_{jD4mean,gen})$	78.8676
$T_{jT2mean,gen}(T_{jT3mean,gen})$	81.6462
$T_{jD2mean,gen}(T_{jD3mean,gen})$	62.7697
$T_{jD5mean,gen}(T_{jD6mean,gen})$	74.4085

Table 4. 5 $T_{j,mean}$ Values of 3L-NPC Components with SYPWM

Due to the different total thermal losses of each semiconductor generated from SPWM and SYPWM are not distinguished so much, the differences between their mean junction temperatures are not so obvious either.

The thermal cycle amplitude ΔT_j is another significant criterion to judge the lifetime of power electronics, and the lifetime increases with the decreasing of ΔT_j [55].

ΔT_j can be generated by the maximum junction temperature minus the minimum junction temperature during each thermal cycle, therefore, the values of $T_{j,max}$ and $T_{j,min}$ depend on the sampling size of thermal cycles, in order to observe the effects of different modulations more intuitive and concise, this thesis decided to record the highest junction temperature and the lowest junction temperature during the entire simulation process, using the largest difference $\Delta T_{j,max}$ to compare. Taking the examples of T1(T4) from both sides, the points of $T_{jT1max,grid}$, $T_{jT1min,grid}$, $T_{jT1max,gen}$ and $T_{jT1max,gen}$ have been marked in figures 4.14 and 4.15. The details of $\Delta T_{j,max}$ on each semiconductor under different modulated conditions are shown in table 4.6 and table 4.7.

Maximum junction temperature differences on different components ($\Delta T_{j,max}$)	Maximum values (℃)
$\Delta T_{jmaxT1,grid}(\Delta T_{jmaxT4,grid})$	44.33
$\Delta T_{jmaxD1,grid}(\Delta T_{jmaxD4,grid})$	7.98
$\Delta T_{jmaxT2,grid}(\Delta T_{jmaxT3,grid})$	15.87
$\Delta T_{jmaxD2,grid}(\Delta T_{jmaxD3,grid})$	3.56
$\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$	27.41
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	8.03
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	47.01
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	38.27
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	28.09
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	29.56

Table 4. 6 $\Delta T_{j,max}$ Values of 3L-NPC Components with SPWM

Maximum junction temperature differences on different components ($\Delta T_{j,max}$)	Maximum values (℃)
$\Delta T_{jmaxT1,grid}(\Delta T_{jmaxT4,grid})$	43.59
$\Delta T_{jmaxD1,grid}(\Delta T_{jmaxD4,grid})$	8.38
$\Delta T_{jmaxT2,grid}(\Delta T_{jmaxT3,grid})$	16.38
$\Delta T_{jmaxD2,grid}(\Delta T_{jmaxD3,grid})$	3.27
$\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$	26.88
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	8.81
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	46.25
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	36.04
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	27.34
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	28.25

Table 4. 7 $\Delta T_{j,max}$ Values of 3L-NPC Components with SYPWM

From the data shown in the tables 4.6 and 4.7, it can be summarized that the semiconductor $\Delta T_{j,max}$ values between SPWM and SYPWM modulated systems do not differ significantly. T1(T4) is the one has the largest $\Delta T_{j,max}$ from grid side, and D1(D4) is the one has the largest $\Delta T_{j,max}$ from the generator side.

4.3 Flattop Quasi-sinusoidal Pulse Width Modulation (FTPWM)

4.3.1 The Principles of FTPWM

Improving the maximum amplitude of PWM output fundamental wave, having relatively simple PWM algorithm, and decreasing the total harmonic distortion (THD) has been the goal pursued by people. With SYPWM, although the DC voltage utilization rate is increased by 15%, it is still difficult to meet the application requirements to further enhance the DC voltage utilization. Therefore, a flattop quasi-sinusoidal modulation wave is constructed as figure 4.18 shown [20]. The three-phase PWM generated after the triangular carrier wave modulation can significantly increase the amplitude of the fundamental wave from the maximum output voltage, moreover, it owns a relatively simple PWM real-time algorithm and lower THD.

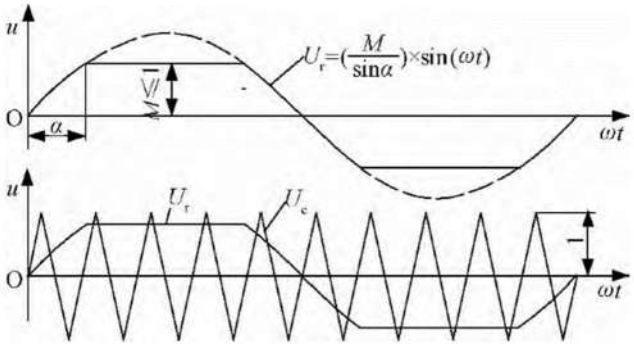

Figure 4. 18 Flattop Quasi-Sinusoidal Modulation Waveform [20]

The modulation waveform U_r shown in figure 4.18 is obtained by cutting off the top of a sinusoidal wave, and it is characterized by a flattened wave in the middle part and two sinusoidal waves at sides. The mathematical description of this waveform can be shown as follows:

$$U_r \begin{cases} \frac{M}{\sin\alpha}\sin(\omega t) & 0 \le \omega t \le \alpha \\ M & \alpha < \omega t < \pi - \alpha \\ \frac{M}{\sin\alpha}\sin(\omega t) & \pi - \alpha \le \omega t \le \pi + \alpha \\ -M & \pi + \alpha < \omega t < 2\pi - \alpha \\ \frac{M}{\sin\alpha}\sin(\omega t) & 2\pi - \alpha \le \omega t \le 2\pi \end{cases} \quad (4\text{-}29)$$

In equation (4-29), M is flat top height, $0 \le M \le 1$; α is the width of two sides, $0 < \alpha \le \pi/2$. Since the amplitude of the triangular carrier wave in figure 4.18 is taken as 1, the flat top height M of the modulation wave is equivalent to the modulation level.

From the Fourier analysis, the amplitude of the fundamental component contained in the modulation wave of equation (4-29) is larger than the flattened peak height M, and it increases with the augment of the flattened peak width of the modulation wave, in other words, the decrease of α. When α is almost equal to 0, the modulation wave evolves into a square wave, its fundamental wave amplitude is $\pi/4$. Although widening the flat top width brings the benefit of increasing the amplitude of the fundamental wave component, the components of harmonics are also fluctuated with the increase of the flat top width (the decrease of the angle α). In order to obtain the best modulation wave, the contradiction between increasing the fundamental wave and

reducing the influence of the harmonic wave must be solved. [20] indicates that $\alpha = 0.658$ rad is the best value to generate the modulation wave, the fundamental wave amplitude of the maximum output line voltage is 19% higher than SPWM and 3.2% higher than SYPWM.

4.3.2 FTPWM Modelling

When $\alpha = 0.658$ rad, in one fundamental wave period, from $0°$ to $37.7°$, $142.3°$ to $217.7°$ and $322.3°$ to $360°$, the modulation wave stays as the sinusoidal shape, and it keeps as the flattop wave in the remaining angle. For the FTPWM model, the three-phase voltages in the duty ratio mode have been used as the input signals, in order to limit the tracking angle range in 2π, the angle difference θ between rotor coordinate system and stator coordinate system should be considered as another input signal. Taking phase A as an example, figure 4.19 shows the FTPWM Matlab model.

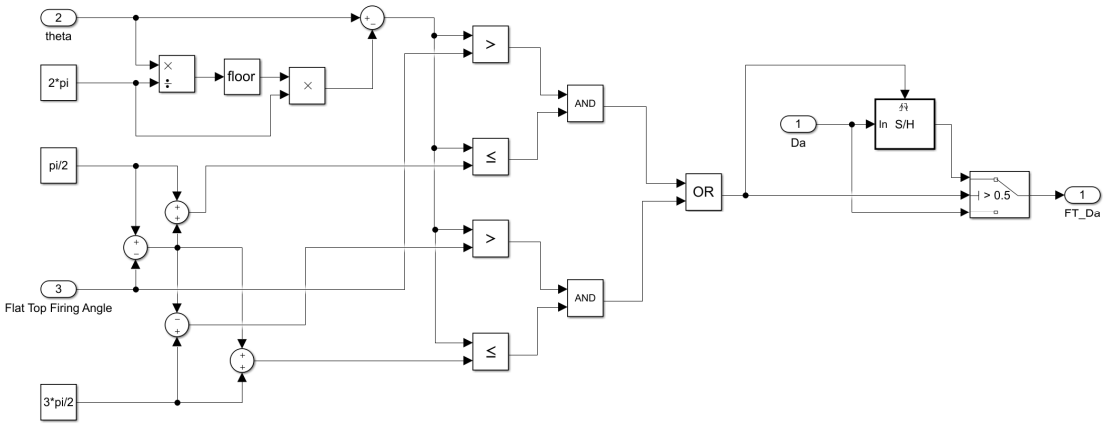

Figure 4. 19 FTPWM Matlab Model Based on Phase A

Establishing the same FTPWM Matlab Model to phase B and phase C respectively, the three-phase output voltages in duty ratio mode can be shown as follow:

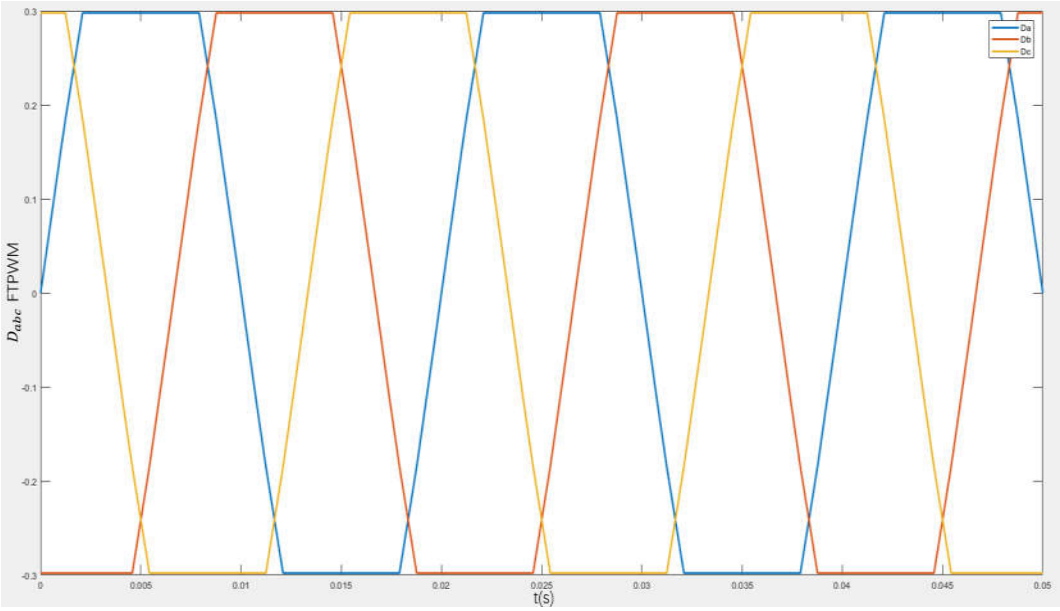

Figure 4. 20 FTPWM Result

4.3.3 Thermal Simulation Results with FTPWM

Adopting FTPWM to both grid side and generator side, let the system run 240s. Observing thermal loss and junction temperature of each semiconductor. Similar as it mentioned in last section, different modulations do not affect the three-phase current obviously, and the switching frequency and the DC bus voltage are given constantly in this system, so there is no significant change in $P_{sw,igbt}$ and $P_{rr,fwdi}$. However, the conduction losses of both IGBT and FWDI have visible differences after applying FTPWM to the system. The comparison charts of average total thermal loss on each semiconductor under three different modulations can be found in figures 4.21 and 4.22.

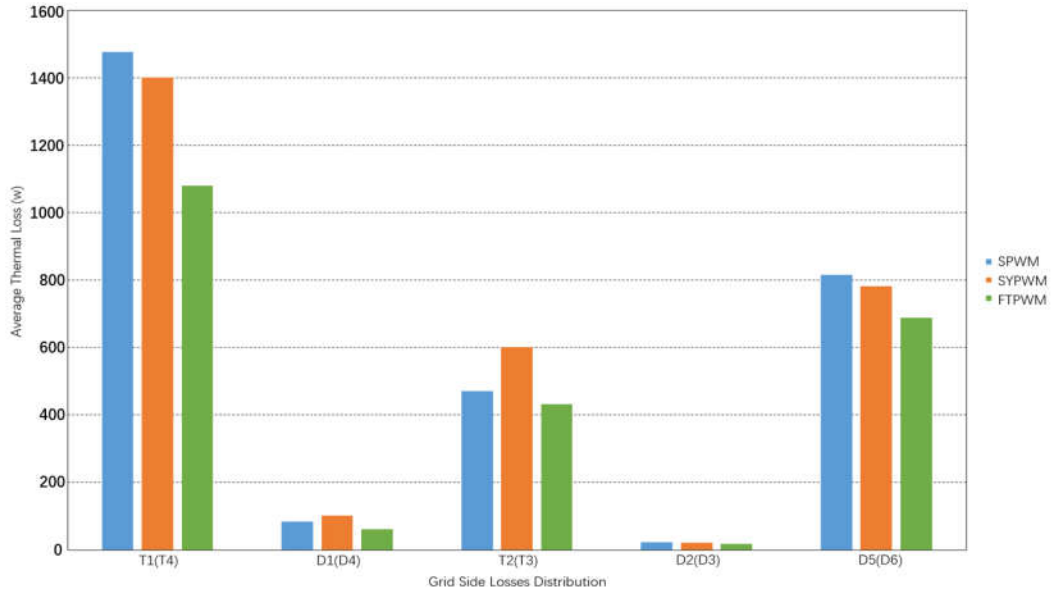

Figure 4. 21 Average Thermal Losses Distribution of Semiconductors at Grid Side (with 3 Modulations)

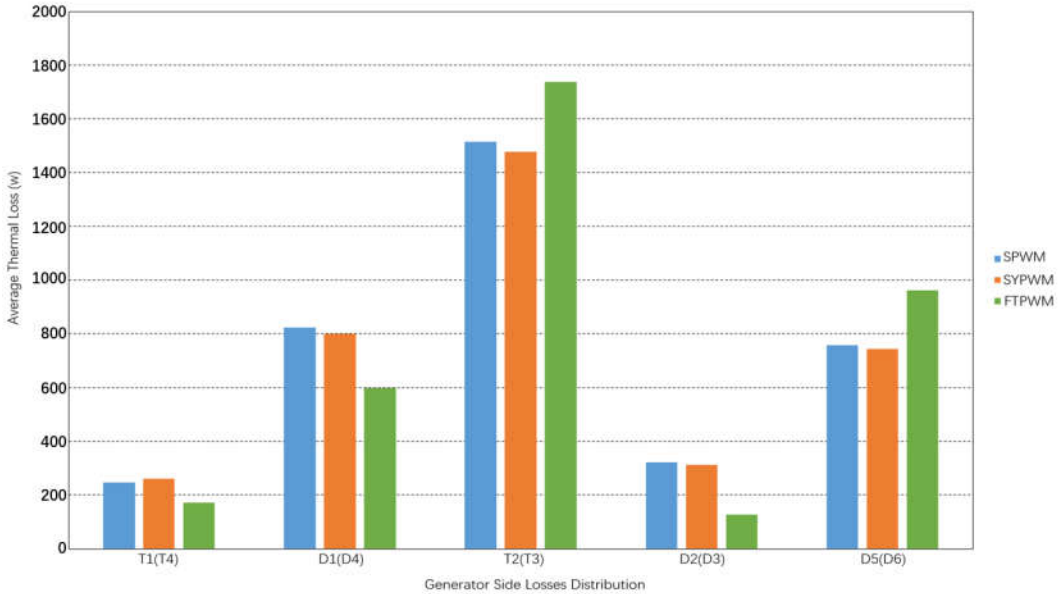

Figure 4. 22 Average Thermal Losses Distribution of Semiconductors at Generator Side (with 3 Modulations)

From the results demonstrated in figure 4.21 and 4.22, FTPWM used at the grid side gives very positive thermal performance influences of all the semiconductors. At the generator side, by applying FTPWM, the thermal losses of T2(T3) and D5(D6) get increased while the rest of semiconductors achieve less losses.

The $T_{j,mean}$ statistic results of all semiconductors by using FTPWM on both sides are shown in table 4.8. Compared to SPWM and SYPWM, FTPWM reduces the mean junction temperatures of most switches and diodes.

Mean junction temperatures on different components ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	72.2019
$T_{jD1mean,grid}(T_{jD4mean,grid})$	46.8357
$T_{jT2mean,grid}(T_{jT3mean,grid})$	48.5958
$T_{jD2mean,grid}(T_{jD3mean,grid})$	42.4100
$T_{jD5mean,grid}(T_{jD6mean,grid})$	75.2435
$T_{jT1mean,gen}(T_{jT4mean,gen})$	45.3387
$T_{jD1mean,gen}(T_{jD4mean,gen})$	68.4331
$T_{jT2mean,gen}(T_{jT3mean,gen})$	86.8118
$T_{jD2mean,gen}(T_{jD3mean,gen})$	55.1456
$T_{jD5mean,gen}(T_{jD6mean,gen})$	87.0996

Table 4. 8 $T_{j,mean}$ Values of 3L-NPC Components with FTPWM

To make the data more convenient for observation, the mean junction temperature results from each semiconductor under three different modulations are distributed comprehensively in figures 4.23 and 4.24.

Figure 4. 23 Mean Junction Temperature Distribution at Grid Side (with 3 Modulations)

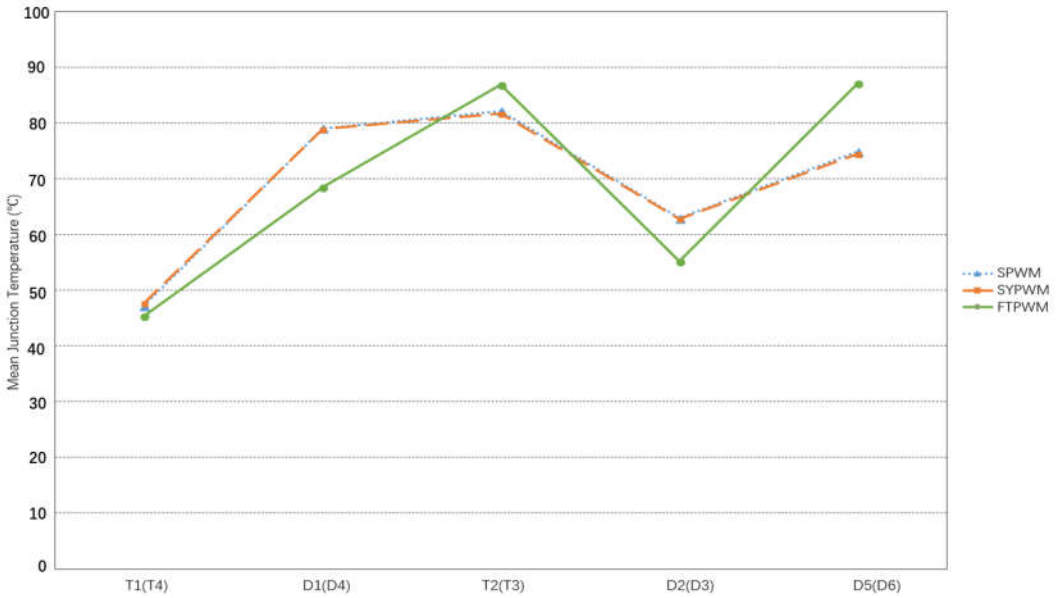

Figure 4. 24 Mean Junction Temperature Distribution at Generator Side (with 3 Modulations)

From the junction temperature distributions demonstrated in figure 4.23 and 4.24, the following two points can be summarized:

1, For one semiconductor operates under different modulations, its mean junction temperature is corresponding to the thermal loss.

2, Under the same modulation, the semiconductor with the largest thermal loss does not necessarily have the highest mean junction temperature, because the junction temperature is also related to the thermal resistance. For example, with FTPWM, T1(T4) from grid side and T2(T3) from generator side have the largest thermal losses. However, D5(D6) from both sides achieves highest mean junction temperature, because the thermal residence of diodes in the 3L-NPC converter module is chosen to be bigger than that of IGBTs.

The maximum thermal cycling amplitudes of all semiconductors with FTPWM modulated system are illustrated in table 4.9, and $\Delta T_{j,max}$ distributions under three different modulations are demonstrated in figures 4.25 and 4.26.

Maximum junction temperature differences on different components (ΔT_j)	Maximum values (°C)
$\Delta T_{jmaxT1,grid}(\Delta T_{jmaxT4,grid})$	27.96
$\Delta T_{jmaxD1,grid}(\Delta T_{jmaxD4,grid})$	4.34
$\Delta T_{jmaxT2,grid}(\Delta T_{jmaxT3,grid})$	11.16
$\Delta T_{jmaxD2,grid}(\Delta T_{jmaxD3,grid})$	1.86
$\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$	37.49
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	5.91
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	28.87
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	44.72
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	14.24
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	45.9

Table 4. 9 $\Delta T_{j,max}$ Values of 3L-NPC Components with FTPWM

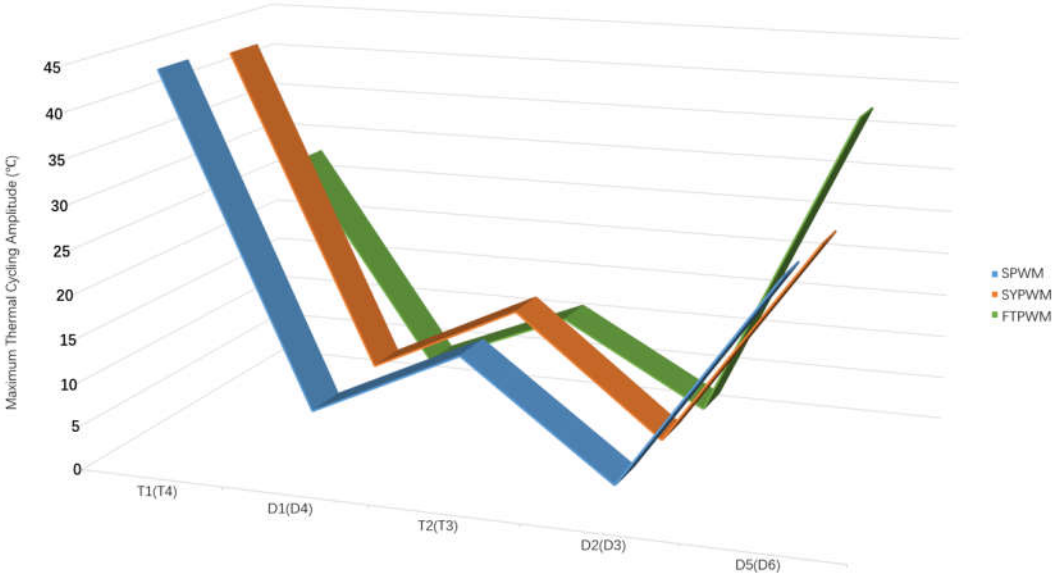

Figure 4. 25 Maximum Thermal Cycling Amplitude Distribution at Grid Side (with 3 Modulations)

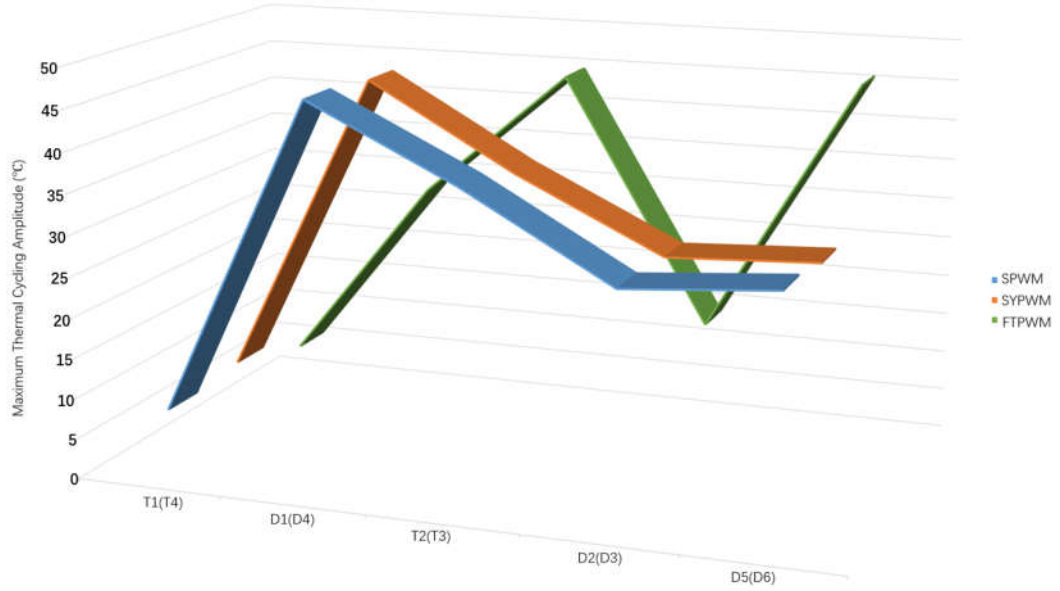

Figure 4. 26 Maximum Thermal Cycling Amplitude Distribution at Generator Side (with 3 Modulations)

From all data illustrated above, the following three points can be summarized:

1, $\Delta T_{j,max}$ results generated by FTPWM have the absolute advantage of grid side. The maximum thermal cycling amplitudes of most semiconductors achieve lower values than they are modulated by SPWM or SYPWM, only the result of $\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$ is a little bit bigger when the system operates with FTPWM.

2, The results from the generator side are more complicated. First of all, T1(T4), D1(D4) and D2(D3) from the generator side achieve smaller $\Delta T_{j,max}$ with FTPWM than other two modulations. It is also interested to realize, D1(D4) from the generator side, which has the biggest maximum thermal cycling amplitude when the system operates under SPWM or SYPWM, achieves around 17°C lower $\Delta T_{j,max}$ by applying FTPWM. Secondly, when the system applies FTPWM, the semiconductor from generator side has the biggest $\Delta T_{j,max}$ is D5(D6) instead of D1(D4).

3, Making a comparison of table 4.9 and table 4.7, it can be noticed that the largest values of $\Delta T_{j,max}$ from the grid side are 37.49℃ on D5(D6) and 43.59℃ on T1(T4) created by FTPWM and SYPWM respectively; from the generator side are 45.9℃ on D5(D6) and 46.25℃ on D1(D4) created by FTPWM and SYPWM respectively. These results show that FTPWM has certain advantages in restricting the highest junction temperature differences.

4.4 Summery of Modulation Selection

In summary, this thesis chooses FTPWM as the modulation strategy for both grid and generator sides. Although a couple of semiconductors of 3L-NPC converter obtain lower $T_{j,mean}$ and smaller $\Delta T_{j,max}$ when the system applies SYPWM, the thermal performances of most components have been significantly improved under the strategy of FTPWM, especially at the grid side.
D5(D6) as the semiconductors generate highest $T_{j,mean}$ and largest $\Delta T_{j,max}$ from both sides will be treated as the ones that give junction temperature reference signals to the active control loop in next chapters.

5. Active Control of Switching Frequency Regulation

Chapter 5 is mainly focused on the methodology, model establishment and simulation results analysis based on the switching frequency active control. Contents of chapter 5 are as follows:
1, Due to the different junction temperature oscillation frequencies of grid side and generator side in PMDD wind system, the model establishments of reference junction temperature sampling from two sides are discussed separately.
2, The two-level switching frequency regulation is introduced first in this chapter, since it has obvious deficiencies in the improvement of semiconductor thermal behavior, this thesis tries to fix it by introducing three-level switching frequency regulation.
3, The thermal simulation results of three-level switching frequency regulation are analyzed in detail at this chapter, therefore, the effectiveness of switching frequency active control is verified.

5.1 Principle of Switching Frequency Active Control

From all the results demonstrated in last chapter, it can be noticed that applying different modulation strategies can change $T_{j,mean}$ with a certain extent, but the trend of T_j will not be affected by them, those obvious drops or rises from junction temperatures when the wind speed is falling or ascending sharply are unsolvable by singly adopting modulations, such as the red regions have been marked in figure 5.1. In fact, the huge difference on T_j caused by the dramatic change in wind speed is the most important issue that effects the lifetime of power electronics.

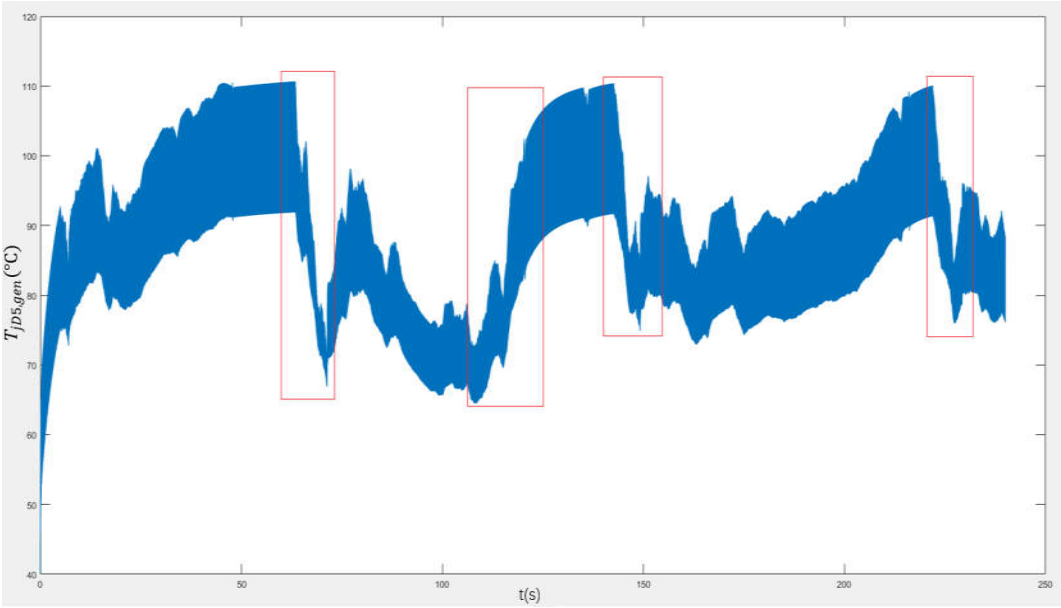

Figure 5. 1 $T_{jD5,gen}$ with FTPWM

The purpose of switching frequency active control is to minimize these huge differences on T_j, so that the system has the ability to increase or decrease T_j by shifting the switching frequency when the wind speed suddenly changes, and the ideal result is that the oscillation of T_j can be regulated as flat as possible.

5.2 Matlab Model and Simulation Results of Grid Side fs Controller

Observing figure 5.1, it can be seen that the most direct way to make T_j oscillating flatter is to enhance T_j when the wind speed is slow, so that the junction temperature staying at lower parts can be filled to higher positions. To realize this target, the system needs to be able to pick up a higher switching frequency when the wind speed suddenly drops, and later when the wind speed rises up, it is necessary for the system to shift back the switching frequency to the original one 2000Hz. Many different frequencies are selected to simulate, and the different junction temperature effects brought by them are used for comparison. As a consequence, 3000Hz is selected as the high level switching frequency based on experimental observation, thus, the two-level fs controller output signal will consist of 2000Hz and 3000Hz. The undesired example results of junction temperature obtained by two abandoned frequencies will be presented later in this section as examples, and sufficient reasons will be given for filtration.

The ability of the system to identify the proper switching frequency level depends on whether the system can instantaneously track the status of wind speed, based on that, the author decides to make a comparison between instantaneous maximum values of T_j and instantaneous average maximum values of T_j. To be more specific, $T_{jmax,ave}$ is the signal of T_{jmax} after low-pass filtering, so $T_{jmax,ave}$ is much smoother than T_{jmax}, when T_{jmax} is floating with the wind speed, $T_{jmax,ave}$ is able to stay approximately as a linear line in between. Due to the junction temperature of the grid side oscillates every 0.02s as the electrical period, and T_{jmax} needs to be sampled per oscillation period, moving maximum block is used to achieve this function. The moving maximum block defines the moving maximum of the input junction temperature signal along each channel independently over time. The sliding window method is used in this block to determine the moving maximum. The Matlab model with regards to the acquisition of T_{jmax} and $T_{jmax,ave}$ from the grid side can be established as follow:

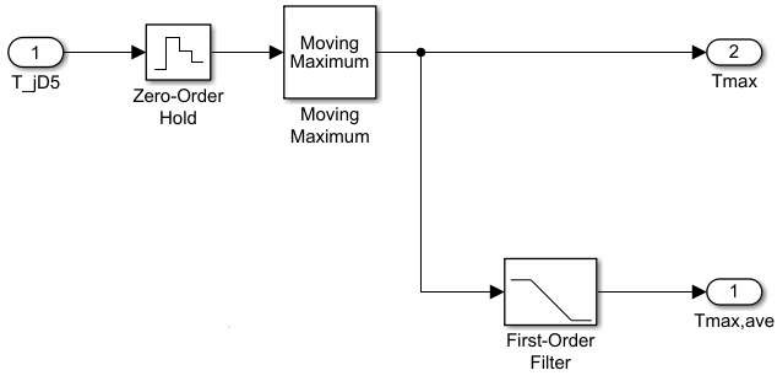

Figure 5. 2 T_{jmax} and $T_{jmax,ave}$ Grid Side Sampling Model

The semiconductor has the highest junction temperature, which is D5(D6) from grid side is considered as the one to create the shifting signals to the switching frequency. The simulation step

length of this system is 10^{-3}, so the sample time of the zero-order hold is set to 1e-3. In the moving maximum block, there is a window of specified length moving over each channel sample by sample, and in this case the window length is set to 20, because the product of 1e-3 and 20 is 0.02, which is the length of one electrical period, therefore, the sampling period of T_{jmax} coincided with the electrical period is realized. The first-order filter is selected to be a low pass type, and the time constant is set to 20, after the system running 240s, the curves of T_{jmax} and $T_{jmax,ave}$ on D5 are shown together in figure 5.3.

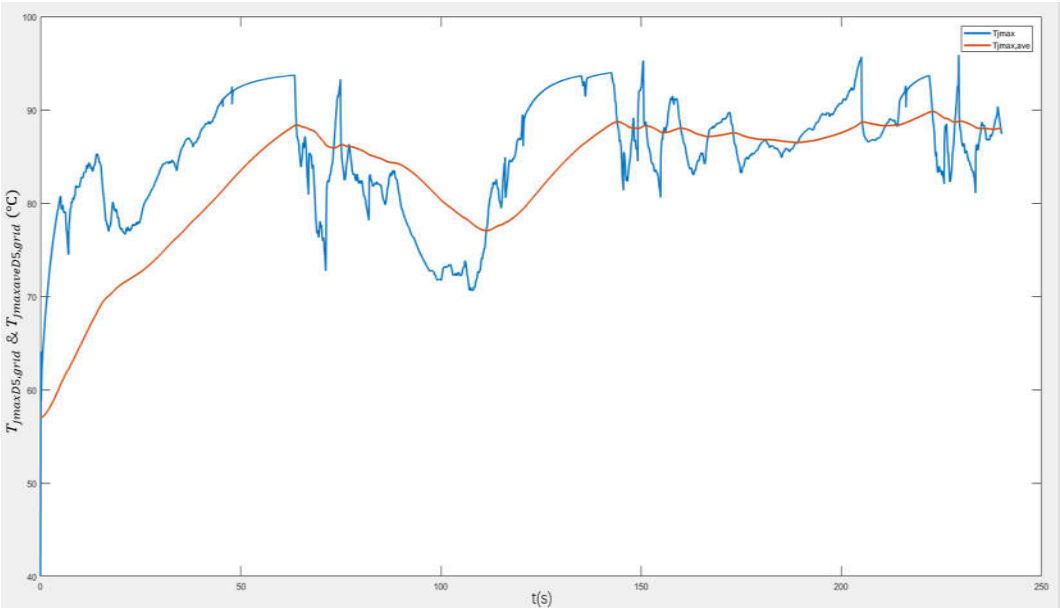

Figure 5. 3 T_{jmax} and $T_{jmax,ave}$ on D5 with 2-Level fs regulation from Grid Side

In figure 5.3, the blue line represents T_{jmax} on D5 while the yellow line represents $T_{jmax,ave}$ on D5, according to the principles mentioned above, when the wind speed is fast, which causes the blue line floating above the yellow line, the system should choose 2000Hz as the switching frequency output signal; when the wind blows slow, which leads to the blue line locating below the yellow line, the output signal of the switching frequency controller should be 3000Hz. However, the ideal situation is that the system can only recognize the obvious drops or rises of the wind speed and ignore those small fluctuations of the blue line crossing around the yellow line which are caused by the small wind disturbances, such as the situation is shown in figure 5.4.

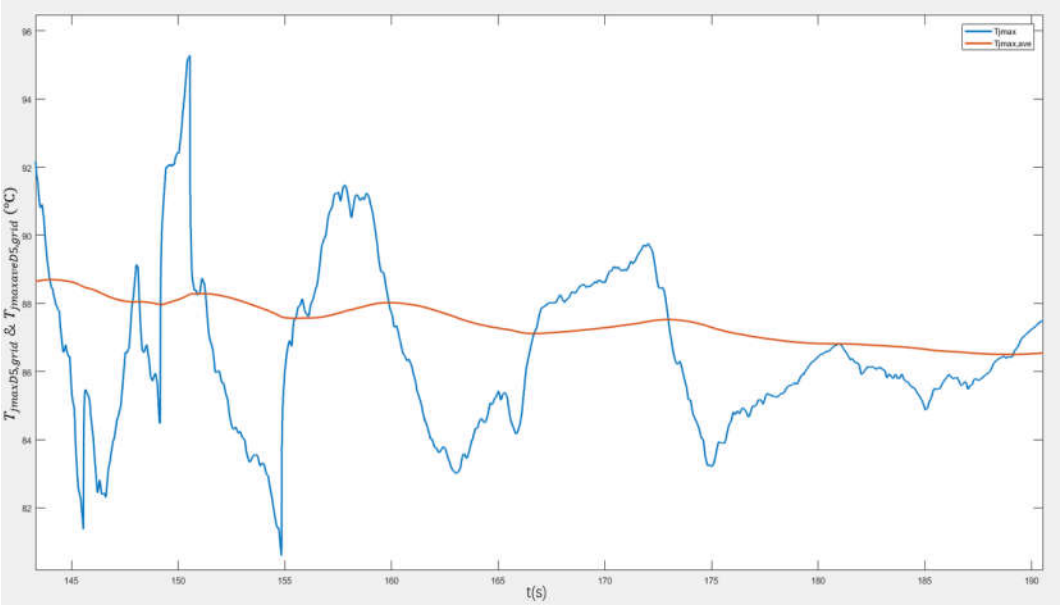

Figure 5. 4 Partial View of T_{jmax} and $T_{jmax,ave}$ on D5 with 2-Level fs Controller from Grid Side

Figure 5.4 shows a zoom in version of T_{jmax} and $T_{jmax,ave}$ when the system operates around 150s to 190s. It can be noticed that the blue line crosses the yellow line quite often during this period, and the temperature differences between them are generally smaller than 5℃. If the switching frequency shift immediately after every small fluctuation, it has very large possibility to cause fractional harmonics. To be more specific, the fractional harmonics appear when the variation frequency of switching frequency is smaller than fundamental frequency, and these harmonics cannot be filtered by a low-pass filter. This also explains why the switching frequency cannot be continuously regulated. Since the simplified Simulink model used in this project cannot provide the observation of carrier waveform variation and its corresponding harmonics around three-phase current, within a certain time, the different harmonics brought by variable carrier frequency and constant carrier frequency are shown in appendix 1 with the help of a PLECS model. To avoid the fractional harmonics brought by switching frequency shifting too often, the hysteresis control has to be introduced, and the temperature hysteresis control model can be established as figure 5.5.

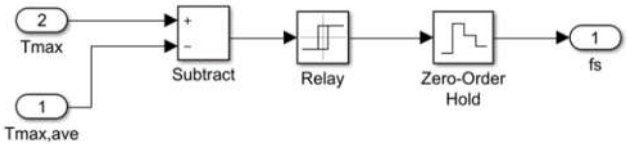

Figure 5. 5 2L Hysteresis Control Model of T_{jmax} and $T_{jmax,ave}$ from Grid Side

The relay block allows its output to select between two specified switching frequency values, which are 2000Hz for on and 3000Hz for off. When the relay is on, it remains on until the input drops below the value of the switch off point parameter; when the relay is off, it remains off until the input exceeds the value of the switch on point parameter. According to equation (2-6) mentioned in section 2.3, 7 and -7 are set for switch on point and switch off point respectively. The switching frequency variation is shown in figure 5.6.

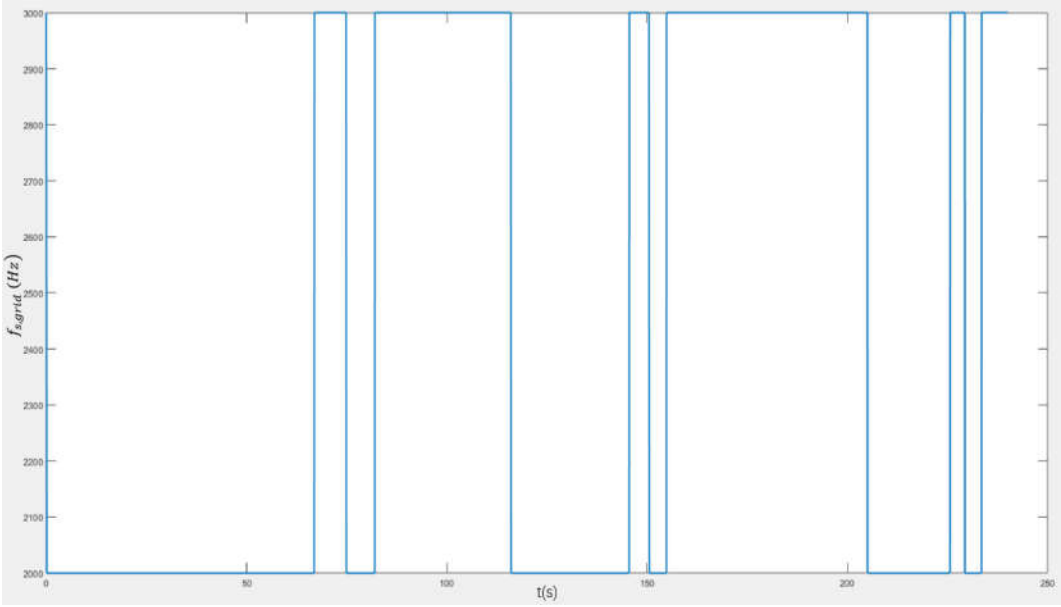

Figure 5. 6 Grid Side fs Output Signal Generated from 2L Controller

Combining figure 5.3 and figure 5.6, the switching frequency does not shift when those small fluctuations appear. Figure 5.7 shows the junction temperature of D5 from grid side after the two-level switching frequency regulation, compared to figure 5.8 which demonstrates $T_{jD5,grid}$ with constant switching frequency 2000Hz, the junction temperature in the red regions when the system operated under low wind speed condition has been raised up by the high switching frequency, and the rest of it has been kept as the previous state by the original switching frequency, thus, the obvious drops and rises on $T_{jD5,grid}$ caused by the dramatic change in wind speed have achieved a certain improvement by the two-level switching frequency regulation.

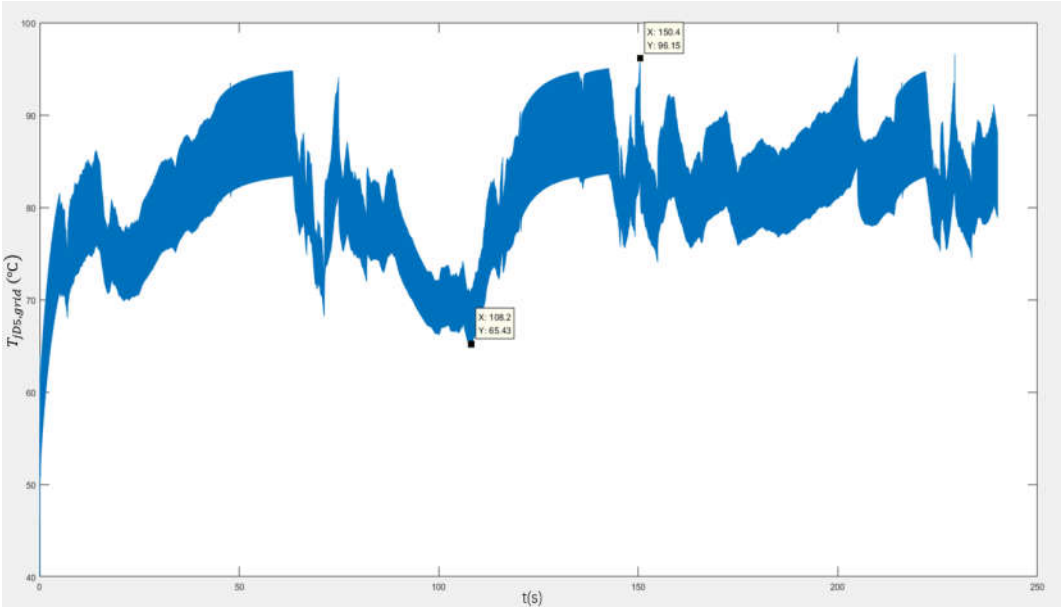

Figure 5. 7 $T_{jD5,grid}$ after 2L fs Regulation

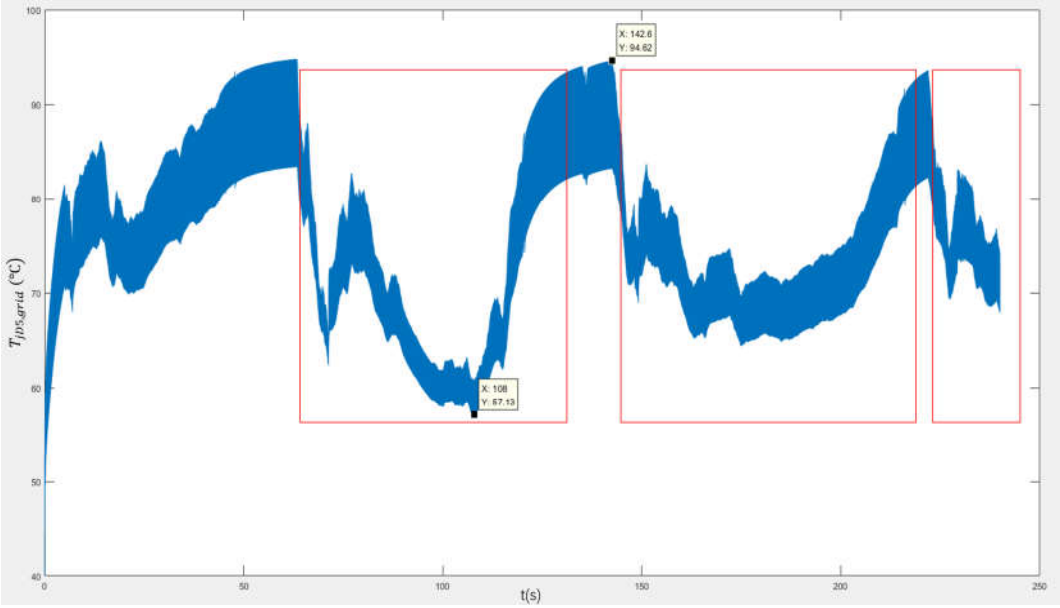

Figure 5. 8 $T_{jD5,grid}$ with Constant fs 2000Hz

The different thermal losses of grid side D5 obtained by without regulation and with two-level switching frequency regulation are distributed in figure 5.9. Due to the high level switching frequency is used to increase loss under the low wind speed condition, the average thermal loss of D5 with two-level switching frequency regulation is much more than it is without regulation.

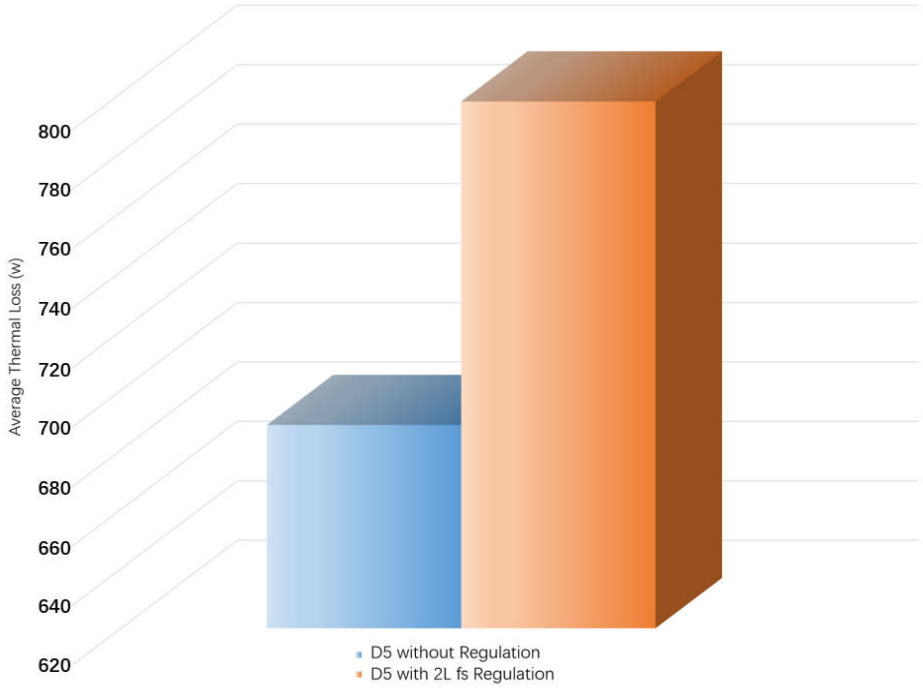

Figure 5. 9 Average Thermal Losses Distribution of D5 at Grid Side (with 2 Conditions)

The maximal amplitude of thermal cycle on D5 with two-level switching frequency regulation can be found in figure 5.7, compared to figure 5.8 which illustrates $\Delta T_{jmaxD5,grid}$ with constant switching frequency 2000Hz, $\Delta T_{j,max}$ is decreased by the two-level switching frequency regulation to a certain degree. The results of $\Delta T_{j,max}$ on different semiconductors can be seen in table 5.1, compared to table 4.9, $\Delta T_{j,max}$ of all the grid side semiconductors are reduced by two-level switching frequency regulation.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,grid}(\Delta T_{jmaxT4,grid})$	23.81
$\Delta T_{jmaxD1,grid}(\Delta T_{jmaxD4,grid})$	3.29
$\Delta T_{jmaxT2,grid}(\Delta T_{jmaxT3,grid})$	10.87
$\Delta T_{jmaxD2,grid}(\Delta T_{jmaxD3,grid})$	1.67
$\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$	30.72

Table 5. 1 $\Delta T_{j,max}$ Values of 3L-NPC Grid Side Semiconductors with 2L fs Regulation

The results of $T_{j,mean}$ on different semiconductors can be seen in table 5.2, compared to table 4.8, $T_{j,mean}$ of all semiconductors are increased by the active control of two-level switching frequency regulation, because the high-level switching frequency is applied to decrease the range of ΔT_j during those big thermal cycles, which brings higher T_j in exchange.

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	78.4051
$T_{jD1mean,grid}(T_{jD4mean,grid})$	48.1265
$T_{jT2mean,grid}(T_{jT3mean,grid})$	48.7976
$T_{jD2mean,grid}(T_{jD3mean,grid})$	42.4478
$T_{jD5mean,grid}(T_{jD6mean,grid})$	80.9740

Table 5. 2 Mean T_j Values of 3L-NPC Semiconductors at Grid Side with 2L fs Regulation

Although thermal cycle amplitudes in big thermal cycles are fixed by the two-level switching frequency regulation in a certain level, the oscillation of $T_{jD5,grid}$ is not absolutely under a flat trend. There are still some observable large differences existing on $T_{jD5,grid}$ under different wind speeds, moreover, $T_{j,mean}$ as another important factor that effects the lifetime of power electronics is raised by two-level fs active control, it cannot be considered as a positive result. Based on these phenomena, a more efficient switching frequency regulation with three-level needs to be introduced, the principle of that can be concluded as when the wind blows extremely fast, the switching frequency selection goes to a low level, when the wind speed is remarkably slow, the fs controller selects a high level, and for the rest of cases the system chooses a medium level as the switching frequency. To be more specific, the three-level switching frequency regulation should be able to complete the insufficiency brought by the two-level one that the regions of T_j when the wind blows fast cannot be pulled down.

Except the comparison between T_{jmax} and $T_{jmax,ave}$, a new comparison branch should be figured out to support the system in being conscious of the boundary conditions that give the signal to shift to the third switching frequency. An extra comparison between instantaneous minimum values of T_j and instantaneous average minimum values of T_j is made. As the same as the sampling of T_{jmax} and $T_{jmax,ave}$, $T_{jmin,ave}$ is the signal of T_{jmin} after low-pass filtering, at the moment when the wind speed is high, T_{jmin} is located above $T_{jmin,ave}$, in the opposite way, when the wind speed is low, T_{jmin} is placed below $T_{jmin,ave}$. The Matlab model with regards to the acquisition of T_{jmax}, $T_{jmax,ave}$, T_{jmin} and $T_{jmin,ave}$ from the grid side can be established as follow:

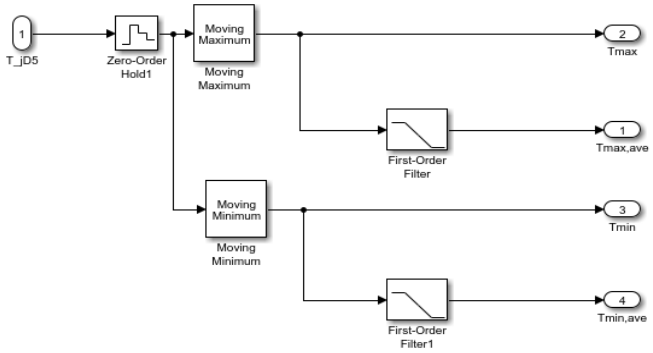

Figure 5. 10 T_{jmax}, $T_{jmax,ave}$, T_{jmin} and $T_{jmin,ave}$ Grid Side Sampling Model

D5(D6) is still chosen to be the one that creates the shifting signals to the switching frequency, the sample time of the zero-order hold and the window length have been set to 1e-3 and 20 respectively as they are explained previously. The curves of T_{jmax} and $T_{jmax,ave}$, T_{jmin} and $T_{jmin,ave}$ on D5 with three-level switching frequency regulation are shown in figure 5.11 and 5.12 respectively.

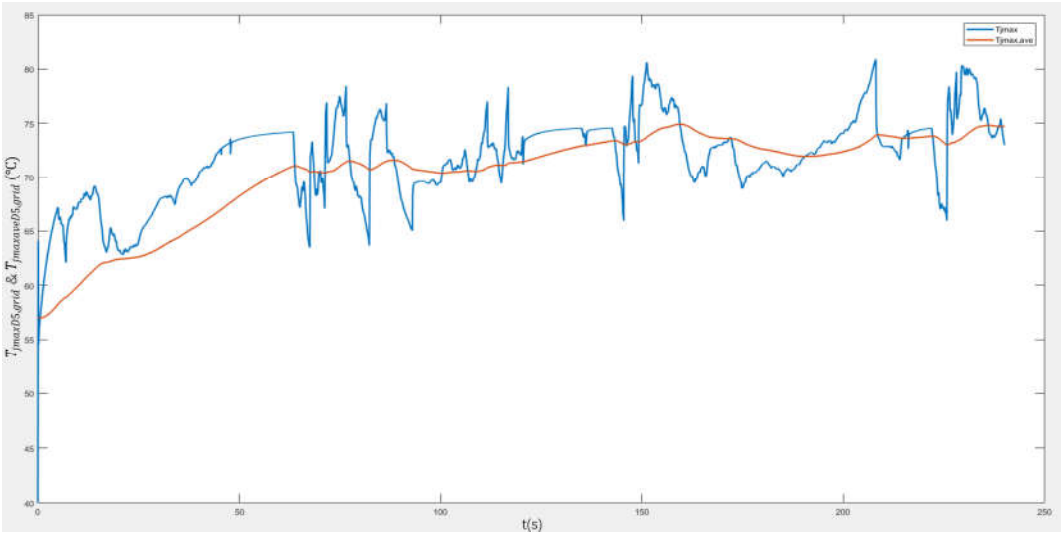

Figure 5. 11 T_{jmax} and $T_{jmax,ave}$ on D5 with 3L fs Regulation from Grid Side

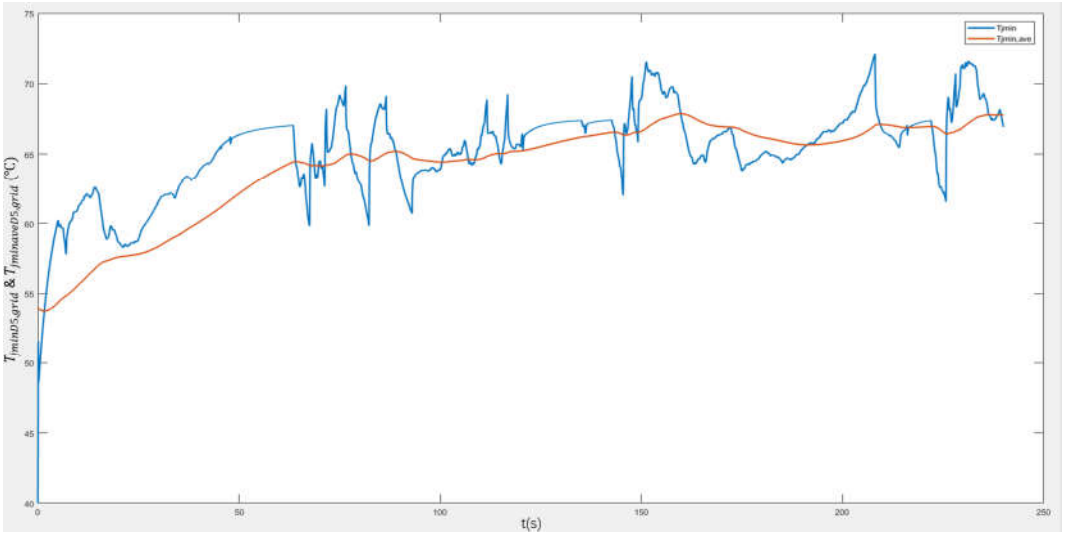

Figure 5. 12 T_{jmin} and $T_{jmin,ave}$ on D5 with 3L fs Regulation from Grid Side

In figure 5.11 and figure 5.12, the blue lines represent the instantaneous maximum and minimum junction temperatures on D5 while the yellow lines represent $T_{jmax,ave}$ and $T_{jmin,ave}$. The system selects the switching frequency out of three values, 1000Hz, 2000Hz and 3000Hz based on experimental observation. According to the principles of three-level switching frequency regulation, when the wind speed is extremely fast, which causes T_{jmax} floating above $T_{jmax,ave}$, the system should choose 1000Hz as the fs output signal; when the wind blows remarkably slow, which leads to the T_{jmin} locating below $T_{jmin,ave}$, the output signal of the switching frequency controller should pick up 3000Hz; 2000Hz should be selected under two different conditions, which are T_{jmax} below $T_{jmax,ave}$ and T_{jmin} above $T_{jmin,ave}$. However, sometimes the switching frequency decision made by figure 5.11 can be completely different than it is selected by figure 5.12, based on those conflicting moments, the author determines when the status of T_{jmax} and $T_{jmax,ave}$ chooses the medium level switching frequency, the system gives the priority to the selection made by T_{jmin} and $T_{jmin,ave}$; when the status of T_{jmax} and $T_{jmax,ave}$ chooses the low-level switching frequency, the system considers their selection as the prioritized one. Therefore, the temperature hysteresis control model based on the three-level switching frequency regulation can be established as figure 5.13.

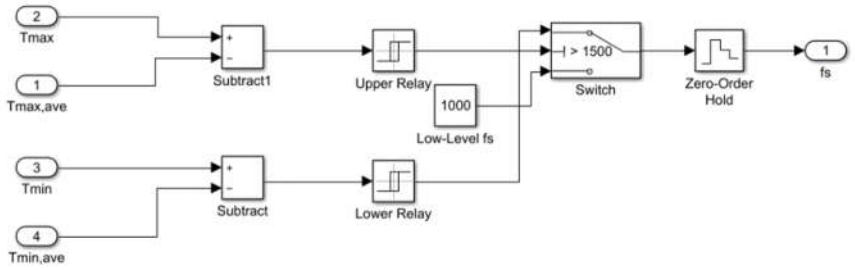

Figure 5. 13 3L Hysteresis Control Model of T_{jmax}, $T_{jmax,ave}$, T_{jmin} and $T_{jmax,ave}$ from Grid Side

The upper relay block allows its output to select between two specified switching frequency values, which are 1000Hz for on and 2000Hz for off, in order to let the system ignore the small wind disturbances, referring equation (2-6), 7 and -7 for switch on and off points are set respectively for the upper relay related to T_{jmax} and $T_{jmax,ave}$. The output switching frequency of the lower relay block is selected between 2000Hz and 3000Hz, 4 and -4 for switch on and off points are set respectively for the lower relay related to T_{jmin} and $T_{jmin,ave}$. The switching frequency variations of the upper relay and the lower relay are shown in figure 5.14 and figure 5.15 respectively.

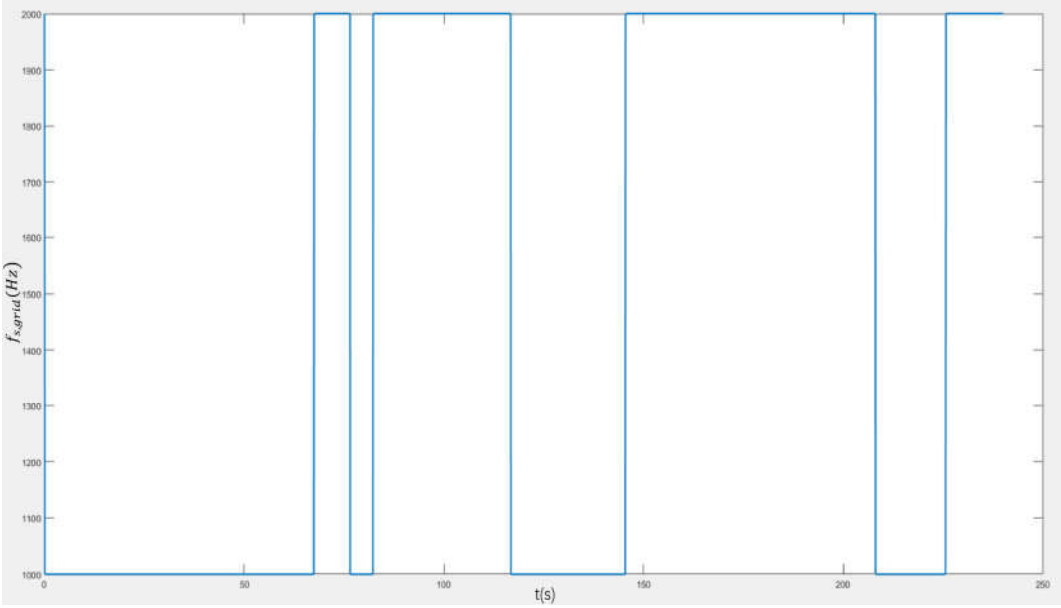

Figure 5. 14 Grid Side fs Output Signal Generated from the Hysteresis Control Related to T_{jmax} and $T_{jmax,ave}$

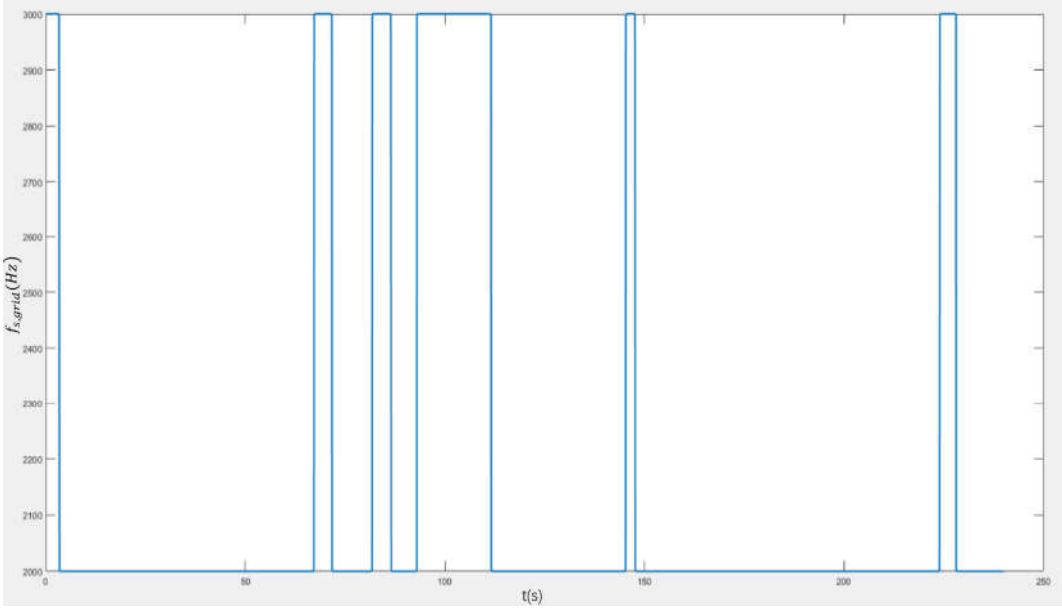

Figure 5. 15 Grid Side fs Output Signal Generated from the Hysteresis Control Related to T_{jmin} and $T_{jmin,ave}$

The function of the switch in figure 5.13 is to solve the priority issue of the switching frequency selection mentioned above. The final three-level switching frequency variation is shown in figure 5.16.

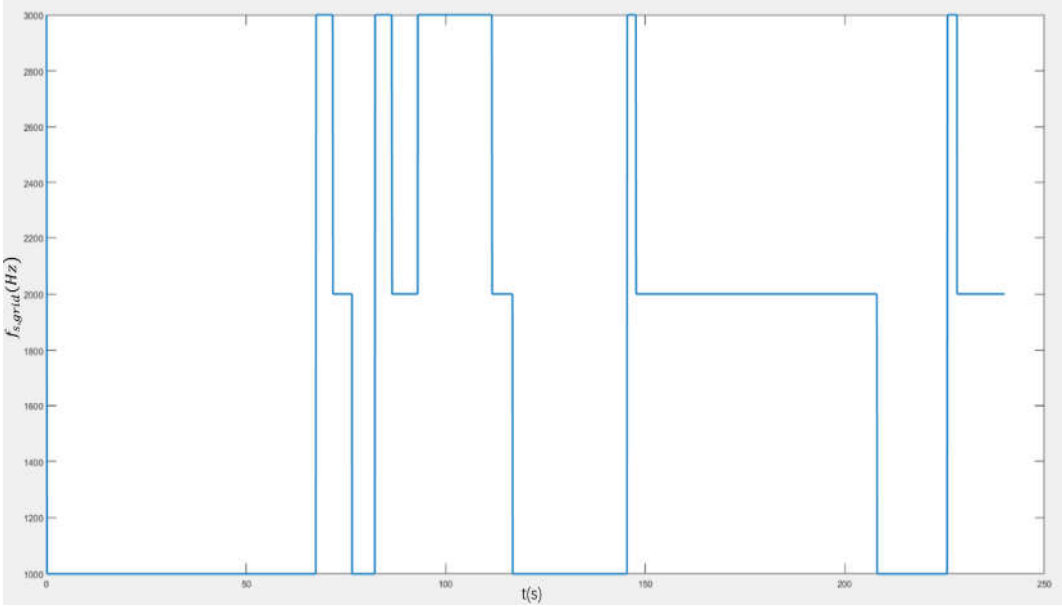

Figure 5. 16 Grid Side fs Output Signal Generated from 3L Controller

Figure 5.17 shows the junction temperature of D5 from grid side after the three-level switching frequency regulation, compared to figure 5.7 which demonstrates $T_{jD5,grid}$ with two-level switching frequency regulation, those obvious differences on $T_{jD5,grid}$ are shortened remarkably. Therefore, the obvious drops and rises on $T_{jD5,grid}$ caused by the dramatic change in wind speed achieve an effective modification by the three-level switching frequency regulation, and the oscillation range of $T_{jD5,grid}$ is much flatter than it is with two-level switching frequency regulation.

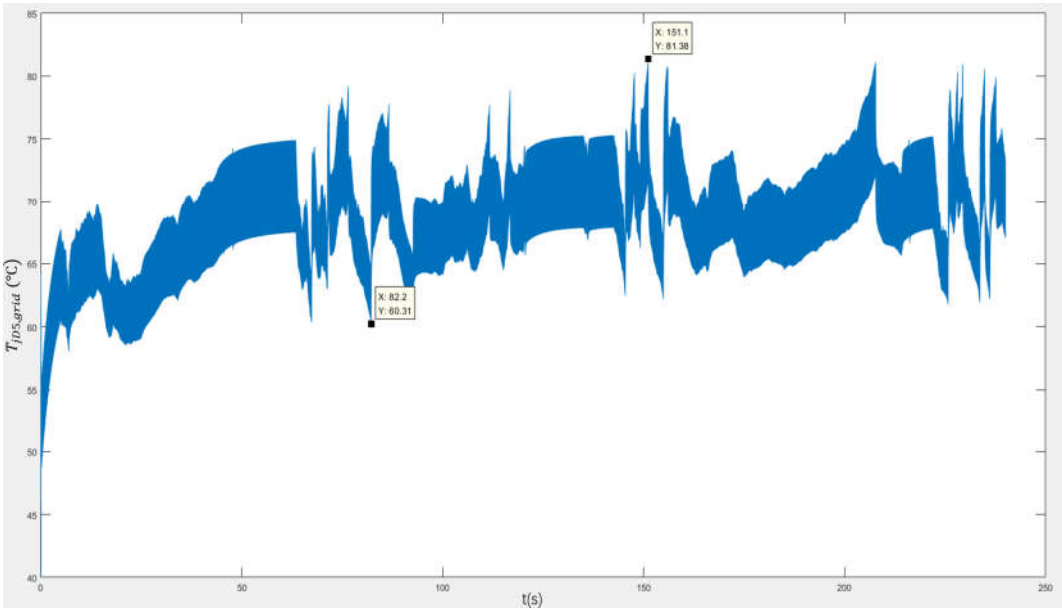

Figure 5. 17 $T_{jD5,grid}$ after 3L fs Regulation

Figure 5.18 shows the result of $T_{jD5,grid}$ when the system operates with switching frequency regulation that consists of 1500Hz, 2000Hz and 2500Hz as three levels. There are still many large amplitudes of thermal cycles existing, the oscillation of junction temperature is not as flat as figure 5.17 demonstrates. The maximum amplitude of thermal cycle is also bigger than it shows in figure 5.17.

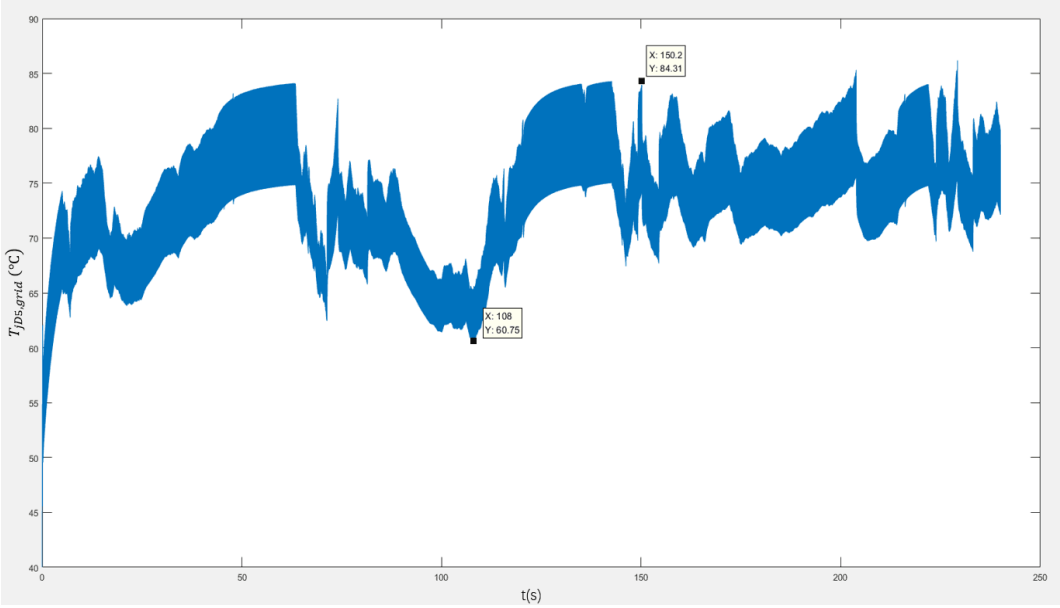

Figure 5. 18 $T_{jD5,grid}$ with fs Selection of 1.5kHz, 2kHz and 2.5kHz

Figure 5.19 shows the result of $T_{jD5,grid}$ when the system operates with switching frequency regulation that consists of 500Hz, 2000Hz and 3500Hz as three levels. It can be seen that when the system recognizes low wind speeds and shifts the switching frequency, the high frequency leads to very high junction temperature significantly. Sometimes T_j even goes higher than it is during high wind speed period, and then the system directly shifts the high-level frequency back to the low-level as the red regions marked in figure 5.19. These phenomena usually repeat in a short time, there will be a high probability of causing fractional harmonics.

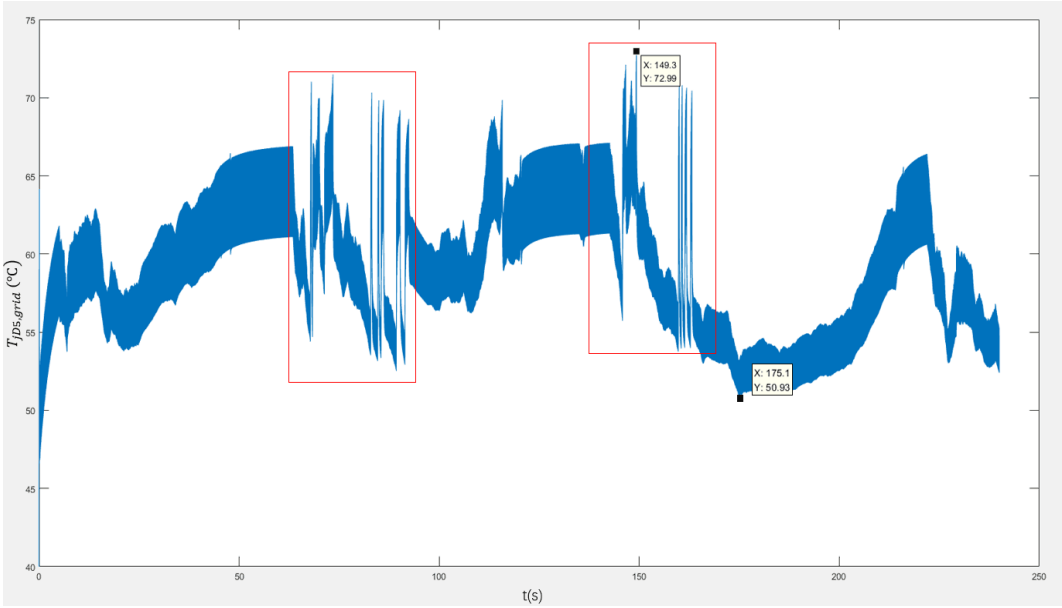

Figure 5. 19 $T_{jD5,grid}$ with fs Selection of 0.5kHz, 2kHz and 3.5kHz

Therefore, too large and too small variation ranges of switching frequency can both bring unfavorable junction temperature control results. For this system, 1000Hz, 2000Hz and 3000Hz are finally selected as the three switching frequency levels.

The different thermal losses of grid side D5 obtained by without regulation, two-level switching frequency regulation and three-level switching frequency regulation are distributed in figure 5.20. It can be noticed that the three-level switching frequency regulation has an absolute advantage in reducing losses.

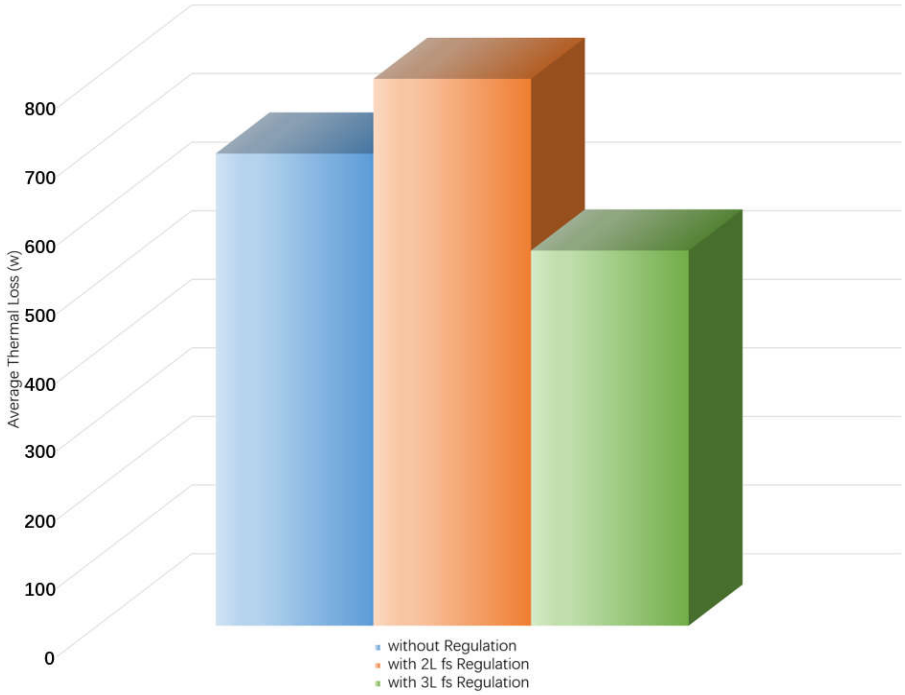

Figure 5. 20 Average Thermal Losses Distribution of D5 at Grid Side (with 3 Conditions)

The maximal amplitude of thermal cycle on D5 with three-level switching frequency regulation is market in figure 5.17. The results of $\Delta T_{j,max}$ on different semiconductors from grid side can be seen in table 5.3, compared to table 5.1, all of them are decreased by the three-level switching frequency regulation.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,grid}(\Delta T_{jmaxT4,grid})$	23.23
$\Delta T_{jmaxD1,grid}(\Delta T_{jmaxD4,grid})$	3.1
$\Delta T_{jmaxT2,grid}(\Delta T_{jmaxT3,grid})$	10.23
$\Delta T_{jmaxD2,grid}(\Delta T_{jmaxD3,grid})$	1.12
$\Delta T_{jmaxD5,grid}(\Delta T_{jmaxD6,grid})$	21.07

Table 5. 3 $\Delta T_{j,max}$ Values of 3L-NPC Grid Side Semiconductors with 3L fs Regulation

The results of $T_{j,mean}$ on different semiconductors from grid side with three-level fs active control can be seen in table 5.4, compared to table 5.2, all of them are obviously decreased.

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	63.9376
$T_{jD1mean,grid}(T_{jD4mean,grid})$	45.0500
$T_{jT2mean,grid}(T_{jT3mean,grid})$	48.3074
$T_{jD2mean,grid}(T_{jD3mean,grid})$	42.3536
$T_{jD5mean,grid}(T_{jD6mean,grid})$	68.2795

Table 5. 4 Mean T_j Values of 3L-NPC Semiconductors at Grid Side with 3L fs Regulation

According to recorded data, the comprehensive distribution charts related to average thermal loss, maximal amplitude of thermal cycle and mean junction temperature of each semiconductor at the grid side can be found in following figures:

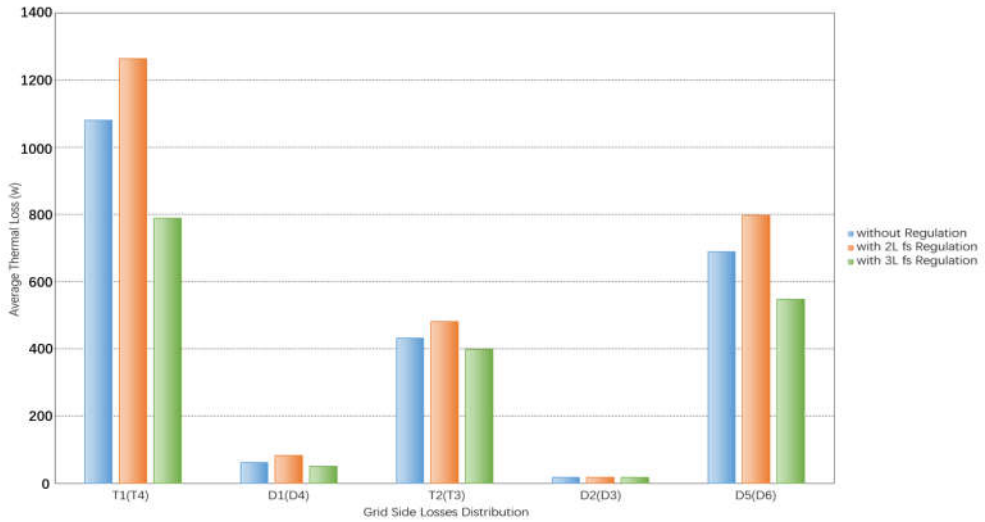

Figure 5. 21 Average Thermal Losses Distribution of Semiconductors at Grid Side (with fs Regulation)

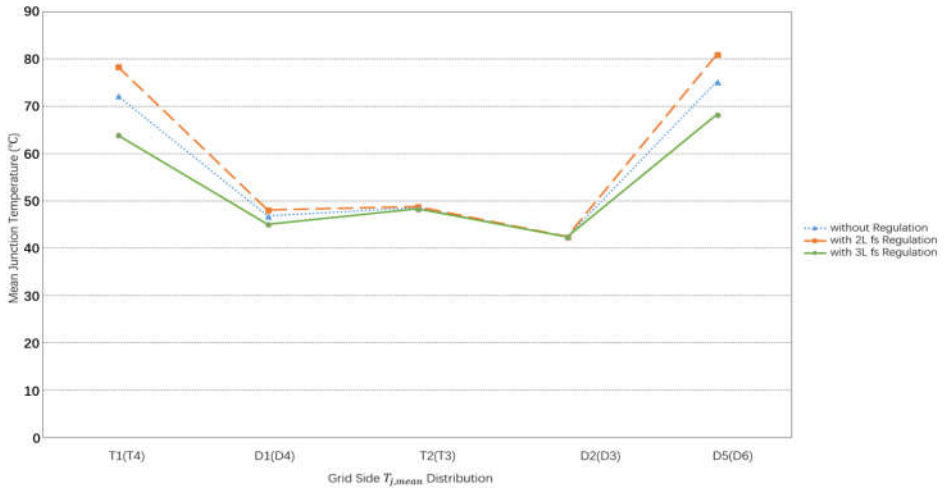

Figure 5. 22 Mean Junction Temperature Distribution at Grid Side (with fs Regulation)

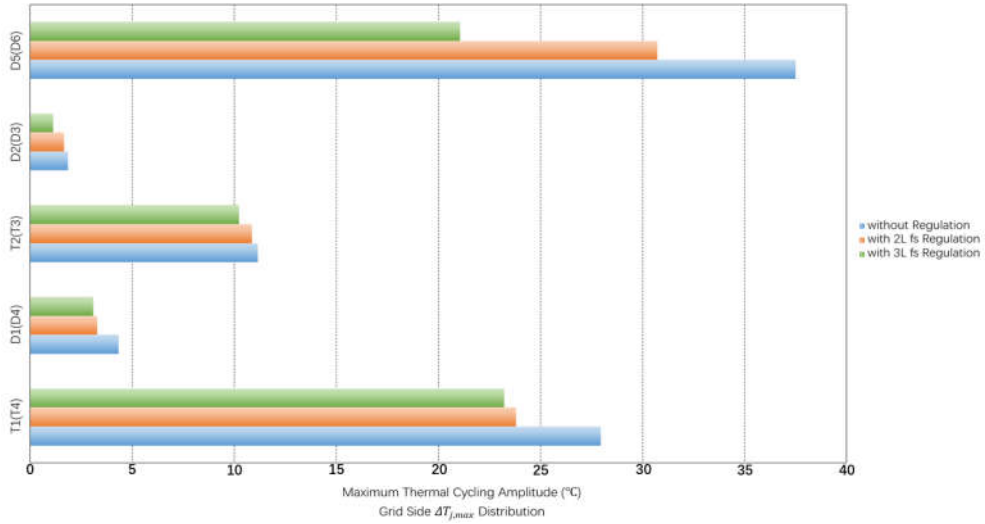

Figure 5. 23 Maximum Thermal Cycling Amplitude Distribution at Grid Side (with fs Regulation)

5.3 Matlab Model and Simulation Results of Generator Side fs Controller

The theory of the generator side switching frequency regulation is similar to the grid side, the generator side simulation results regarding to two-level fs controller and three-level fs controller will be illustrated in sequence in this section. However, from the observations of figure 4.16 and figure 4.17 which are located in section 4.2.3, the oscillation periods of semiconductor junction temperature at the generator side are randomly changed by the wind variations, hence, the sampling method of the maximum or minimum values of T_j per period should be figured out in a different way than the moving maximum and the moving minimum blocks used at the grid side. Nevertheless, no matter how unpredictable the junction temperature periods are, they are consistent with the electrical periods at the generator side, if each electrical period can be locked by the system, the junction temperature period can be known as an equivalent product. The electrical phase locked angle can be generated after giving some processing steps to the electrical rotation speed, which is shown with rad/s as the unit in figure 5.24.

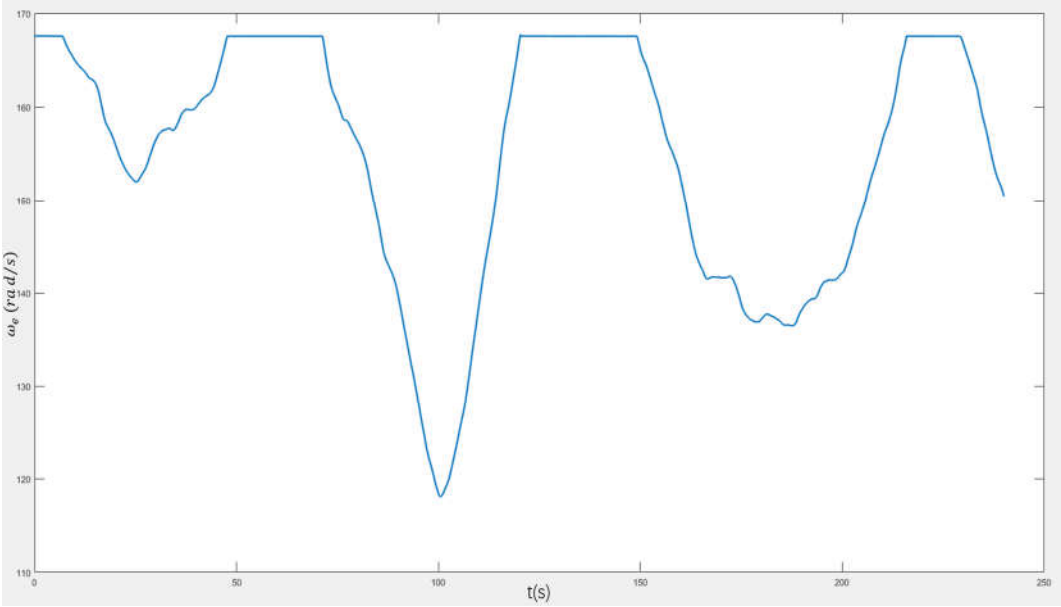

Figure 5. 24 Electrical Rotation Speed

The electrical phase locked angle is regulated to the range $0-2\pi$. The electrical angle can be achieved by integrating the electrical rotation speed, and the rotation turns can be gained after the electrical angle divided by 2π, in order to achieve the angle that has integer times of 2π, the rotation turns have to be rounded to the nearest integer value towards minus infinity, based on this target, a floor rounding function block is introduced. Using the rotation turns with integer values to multiply 2π, the integer times electrical rotation angle can be obtained, and the Matlab model with details of these approaches are shown in figure 5.25.

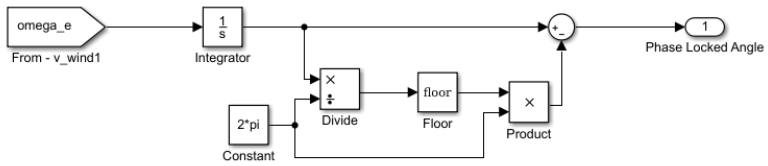

Figure 5. 25 Matlab Model of Phase Locked Angle

For the purpose of triggering the sample signals of T_j through the electrical phase locked angle, a sample and hold block is used, which acquires the input at the signal port whenever it receives a trigger event at the trigger port, the block holds the output at the acquired input value until the next triggering event occurs. The Matlab Model of $T_{j,max}$ acquisition from generator side is shown in figure 5.26.

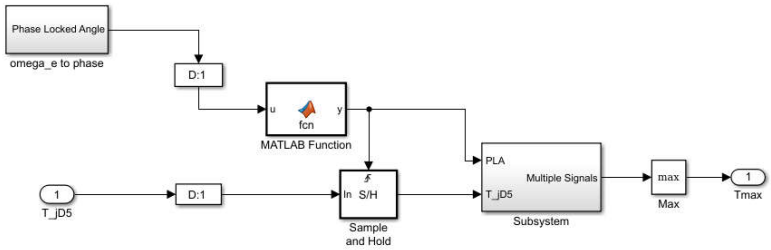

Figure 5. 26 T_{jmax} Generator Side Sampling Model

D5(D6) has the highest junction temperature at generator side is considered as the one to create the shifting signals to the switching frequency. Adding the signal specification block to make the trigger phase locked angle become a sample-based scalar with sample rate equal to the input frame rate at the signal port. It is safe to pick up the maximum value of each T_j period between twenty sampling points, so the Matlab function shown in figure 5.26 separates every phase locked angle period into twenty segments to give twenty times triggering to $T_{jD5,gen}$ during each junction temperature oscillation period. So far, the output of the sample and hold block is a single signal, in other words, the twenty sampled values each period provide the output signal in series. In order to catch the maximum point during each period, the subsystem shown in figure 5.26 establishes several switches to transfer the single serial signal to twenty signals presented in parallel. After the multiple signals are filtered by the max block, the maximum value from each $T_{jD5,gen}$ oscillation period can be obtained, and $T_{jmax,ave}$ can be achieved by T_{jmax} going through a low-pass filter as the same as the grid side. The curves of T_{jmax} and $T_{jmax,ave}$ on D5 at the generator side are shown together in figure 5.27.

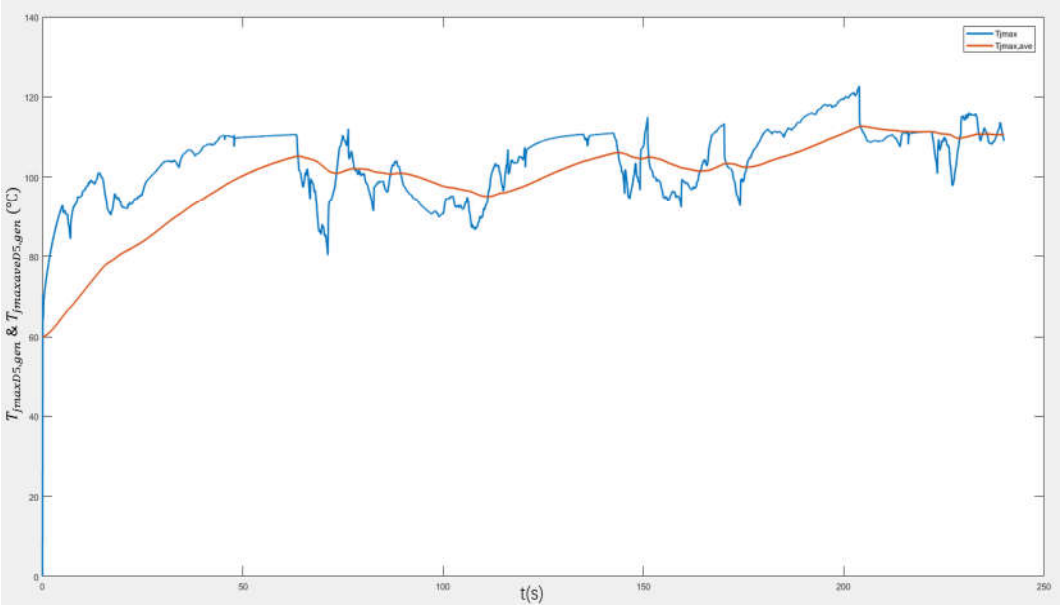

Figure 5. 27 T_{jmax} and $T_{jmax,ave}$ on D5 with 2L fs regulation from Generator Side

The theory of the hysteresis control based on two-level switching frequency is as the same as grid side, however, due to wind turbine is directly connected with the generator in a PMDD wind system, the oscillation range of the generator side junction temperature is much wider than the grid side, in order to avoid the influences brought by those small wind disturbances, the switch on and off points of the switching selection relay are set to be 10 and -10 respectively. The switching frequency variation is shown in figure 5.28.

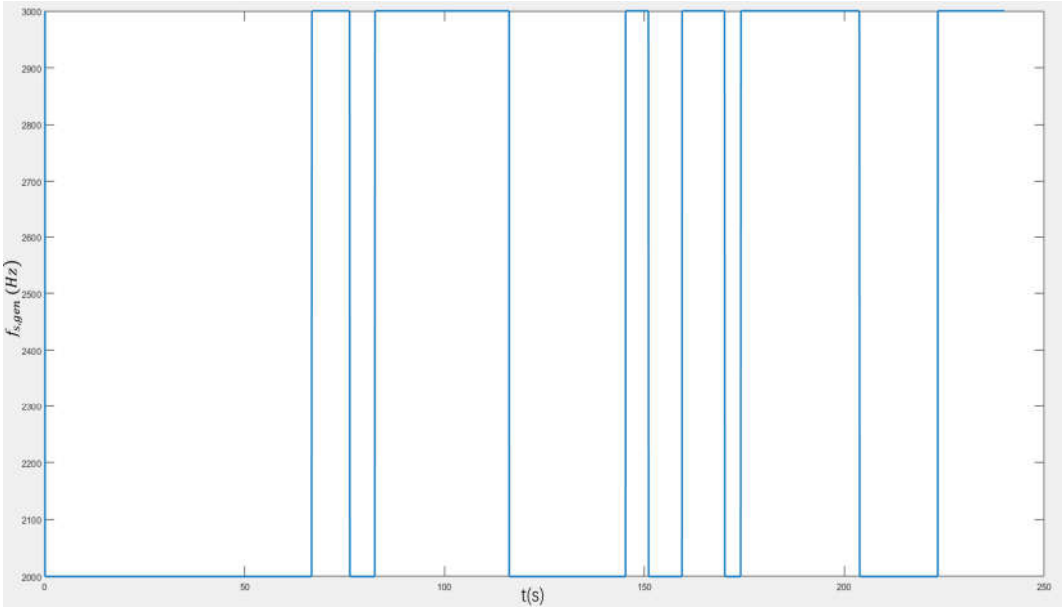

Figure 5. 28 Generator Side fs Output Signal Generated from 2L Controller

Figure 5.29 shows the junction temperature of D5 from generator side after the two-level switching frequency regulation, compared to figure 5.30, which demonstrates $T_{jD5,gen}$ with constant switching frequency 2000Hz, the obvious drops and rises on $T_{jD5,gen}$ caused by the dramatic change in wind speed achieve a certain modification by the two-level switching frequency regulation.

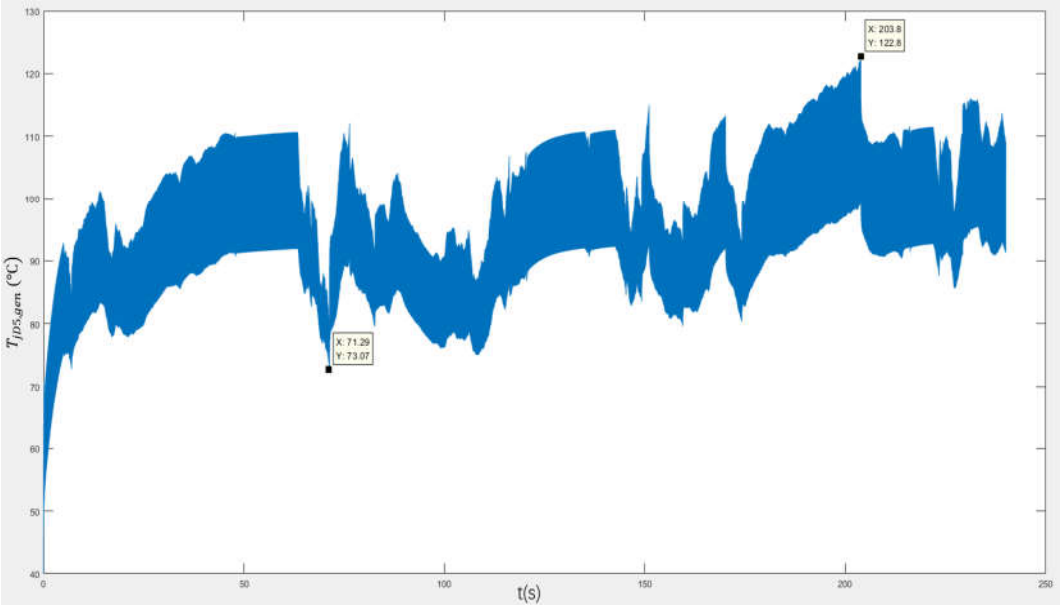

Figure 5. 29 $T_{jD5,gen}$ after 2L fs Regulation

The maximum amplitude of thermal cycle on D5 with two-level switching frequency regulation is marked in figure 5.29, compared to figure 5.30 which illustrates $\Delta T_{jmaxD5,gen}$ with constant switching frequency 2000Hz, $\Delta T_{jmaxD5,gen}$ is increased slightly by the two-level switching frequency regulation to certain degrees, because the moment of maximum T_j point appearance is shifted from 142.6s to 203.8s, and the biggest thermal cycle is changed. Due to the wind speed around 203s is relatively low, 3000Hz switching frequency is recognized as the required one by the system at that moment, it takes time before the system can realize the excessive junction temperature and shift fs back to 2000Hz, so $\Delta T_{jmaxD5,gen}$ gets higher result with a longer thermal cycle. The results of $\Delta T_{j,max}$ on different semiconductors from generator side can be seen in table 5.5, compared to table 4.9, except D2(D3), $\Delta T_{j,max}$ of all the generator side semiconductors are unremarkably increased by two-level switching frequency regulation since the maximum T_j point is shifted.

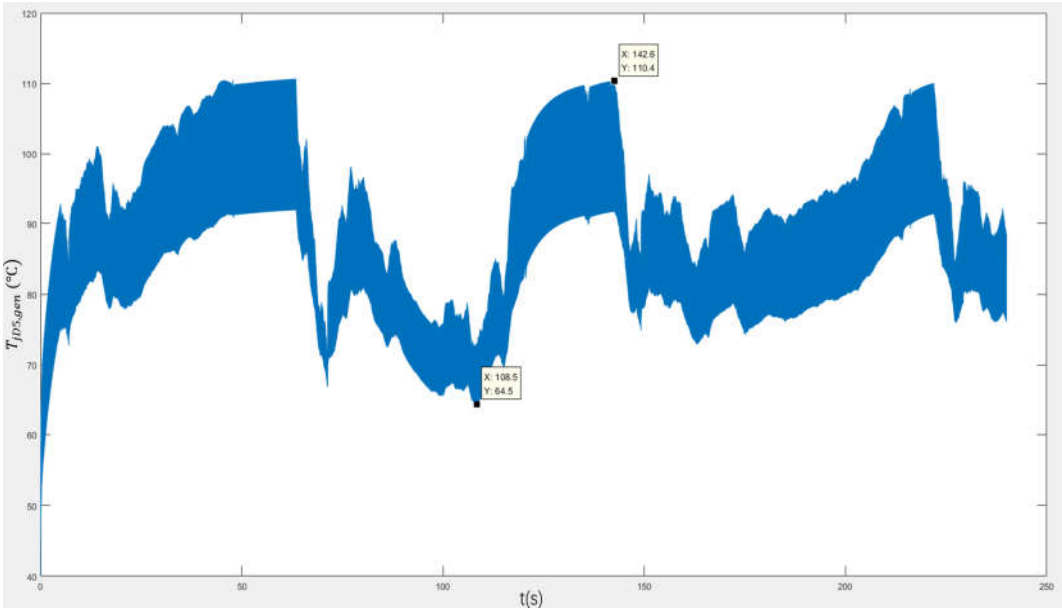

Figure 5. 30 $T_{jD5,gen}$ with Constant fs 2000Hz

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	6.13
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	33.46
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	47.5
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	12.13
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	49.73

Table 5. 5 $\Delta T_{j,max}$ Values of 3L-NPC Generator Side Semiconductors with 2L fs Regulation

The results of $T_{j,mean}$ on different semiconductors from generator side can be seen in table 5.6, compared to table 4.8, $T_{j,mean}$ of all the generator side semiconductors are increased by two-level switching frequency regulation, because the system adopts the high-level switching frequency as the alternative one at those low wind speed moments.

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,gen}(T_{jT4mean,gen})$	46.2941
$T_{jD1mean,gen}(T_{jD4mean,gen})$	74.4299
$T_{jT2mean,gen}(T_{jT3mean,gen})$	96.1938
$T_{jD2mean,gen}(T_{jD3mean,gen})$	56.6738
$T_{jD5mean,gen}(T_{jD6mean,gen})$	94.4353

Table 5. 6 Mean T_j Values of 3L-NPC Semiconductors at Generator Side with 2L fs Regulation

For the three-level switching frequency regulation at the generator side, the comparison between T_{jmin} and $T_{jmin,ave}$ should be added, the sampling theory of T_{jmin} is as the same as it shown in figure 5.26, only the max block should be adjusted to a min one, the curves of T_{jmax} and $T_{jmax,ave}$, T_{jmin} and $T_{jmin,ave}$ on D5 with three-level switching frequency regulation are shown in figure 5.31 and 5.32 respectively.

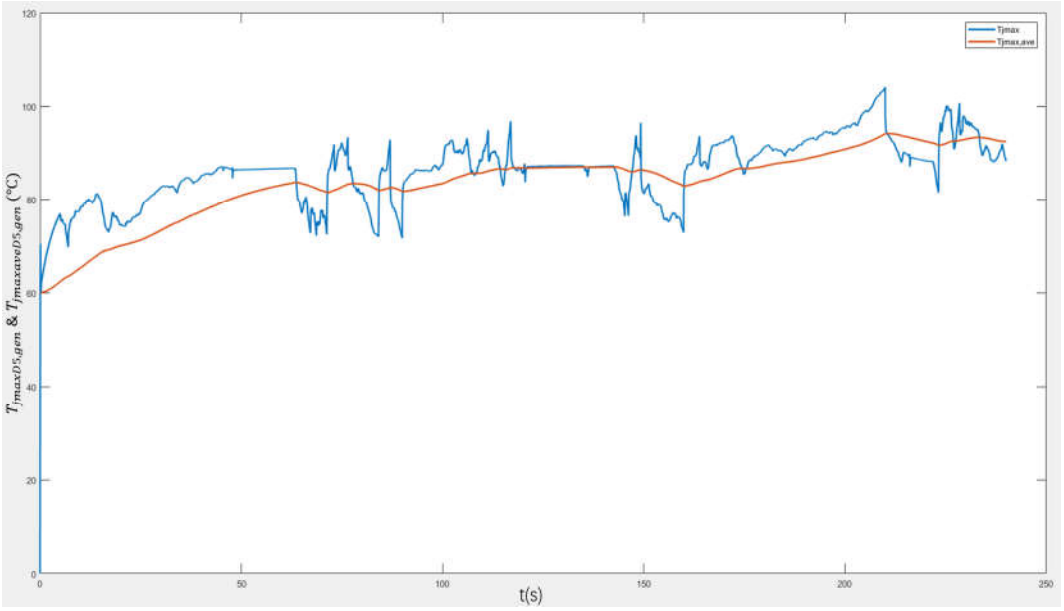

Figure 5. 31 T_{jmax} and $T_{jmax,ave}$ on D5 with 3L fs Regulation from Generator Side

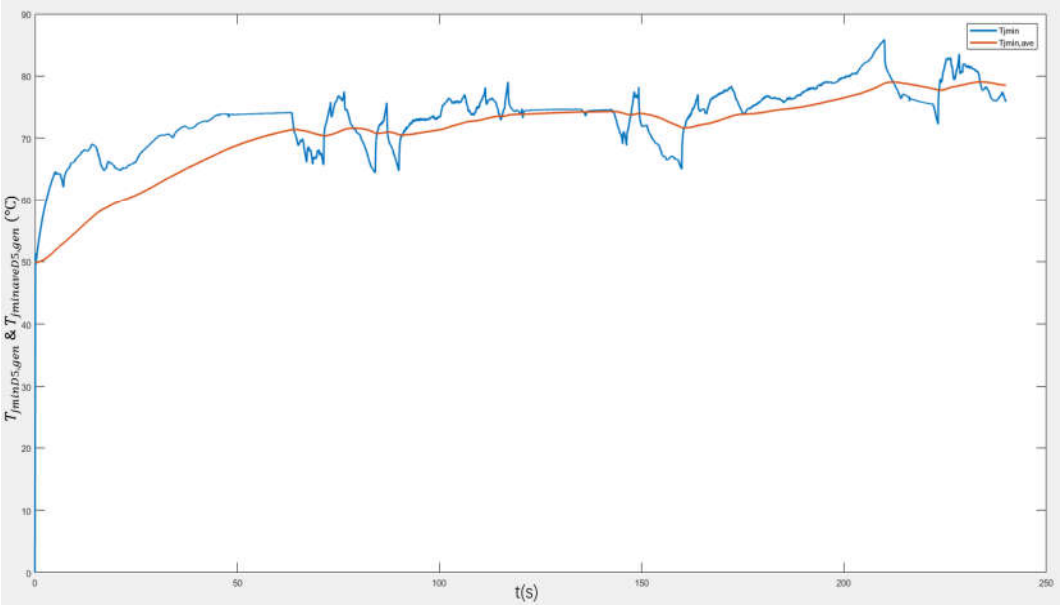

Figure 5. 32 T_{jmin} and $T_{jmin,ave}$ on D5 with 3L fs Regulation from Generator Side

At the generator side, the temperature hysteresis control model based on the three-level switching frequency regulation can be established as the same as the one at grid side which is shown in figure 5.13. 10 and -10 for switch on and off points are set respectively for the upper relay related to T_{jmax} and $T_{jmax,ave}$; 5 and -5 are set respectively for the lower relay related to T_{jmin} and $T_{jmin,ave}$. The final three-level switching frequency variation from the generator side is shown in figure 5.33.

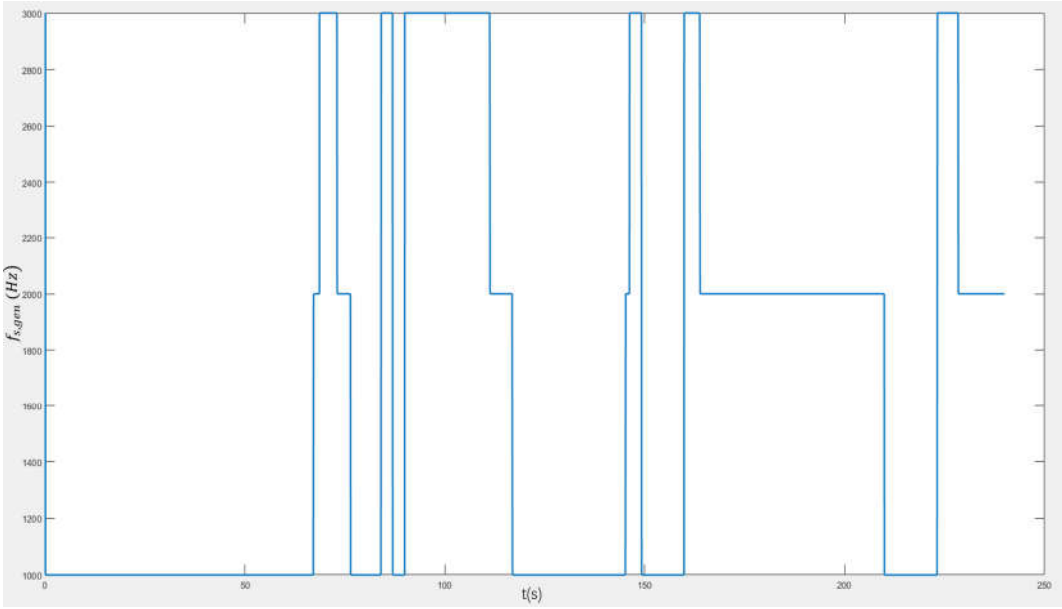

Figure 5. 33 Generator Side fs Output Signal Generated from 3L Controller

Figure 5.34 shows the junction temperature of D5 from generator side after the three-level switching frequency regulation, compared to figure 5.29, which demonstrates $T_{jD5,gen}$ with the two-level switching frequency regulation, not only the obvious drops and rises on $T_{jD5,gen}$ caused by the dramatic change in wind speed obtain a significant modification by the three-level switching frequency regulation, but also the oscillation range of $T_{jD5,gen}$ is shortened effectively.

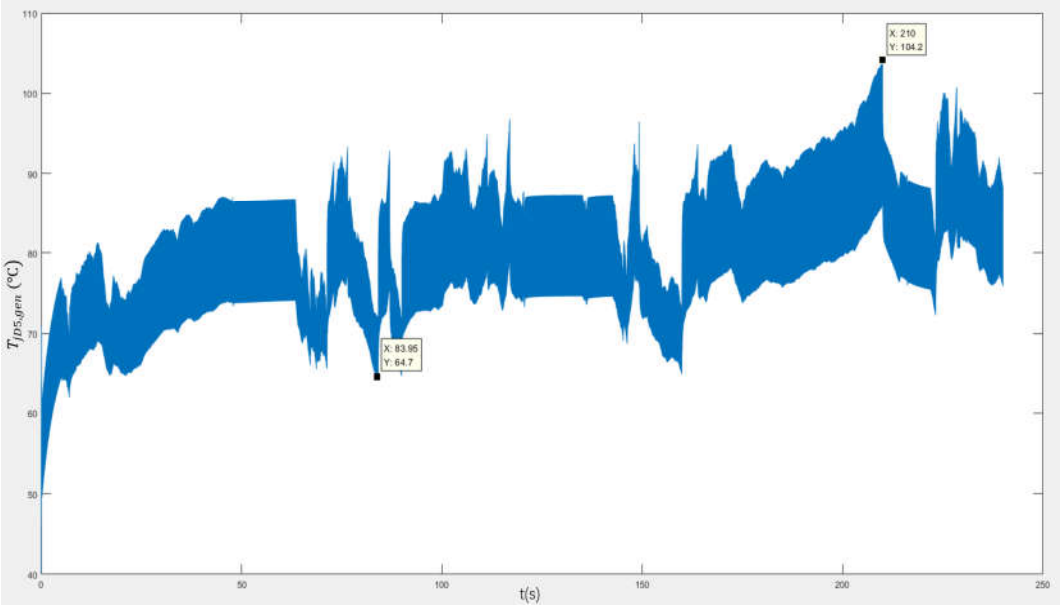

Figure 5. 34 $T_{jD5,gen}$ after 3L fs Regulation

The maximum amplitude of thermal cycle on D5 with three-level switching frequency regulation is marked in figure 5.34, compared to figure 5.30, $\Delta T_{jmaxD5,gen}$ is shortened by the three-level switching frequency regulation effectively, and the results of $\Delta T_{j,max}$ on different semiconductors from generator side can be seen in table 5.7, compared to table 4.9, all of them are decreased by the three-level switching frequency regulation.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	5.2
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	28.12
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	40.75
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	11.16
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	39.5

Table 5. 7 $\Delta T_{j,max}$ Values of 3L-NPC Generator Side Semiconductors with 3L fs Regulation

The results of the mean values of junction temperature on different semiconductors from generator side can be seen in table 5.8, compared to table 4.8, all of them are decreased by the three-level switching frequency regulation.

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,gen}(T_{jT4mean,gen})$	43.9952
$T_{jD1mean,gen}(T_{jD4mean,gen})$	62.5298
$T_{jT2mean,gen}(T_{jT3mean,gen})$	77.4339
$T_{jD2mean,gen}(T_{jD3mean,gen})$	53.0872
$T_{jD5mean,gen}(T_{jD6mean,gen})$	79.1717

Table 5. 8 Mean T_j Values of 3L-NPC Semiconductors at Generator Side with 3L fs Regulation

According to recorded data, the comprehensive distribution charts related to average thermal loss, maximal amplitude of thermal cycle and mean junction temperature of each semiconductor at the generator side can be found in following figures:

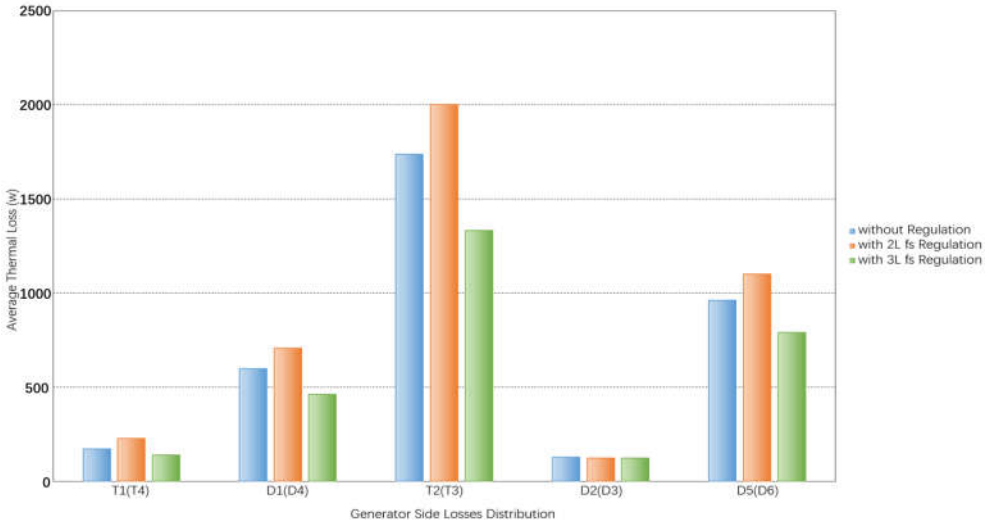

Figure 5. 35 Average Thermal Losses Distribution of Semiconductors at Generator Side (with fs Regulation)

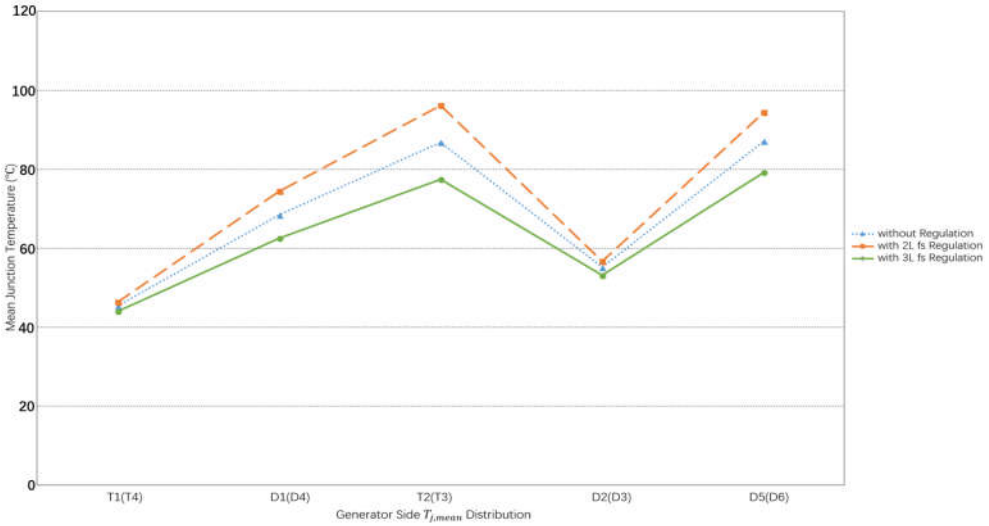

Figure 5. 36 Mean Junction Temperature Distribution at Generator Side (with fs Regulation)

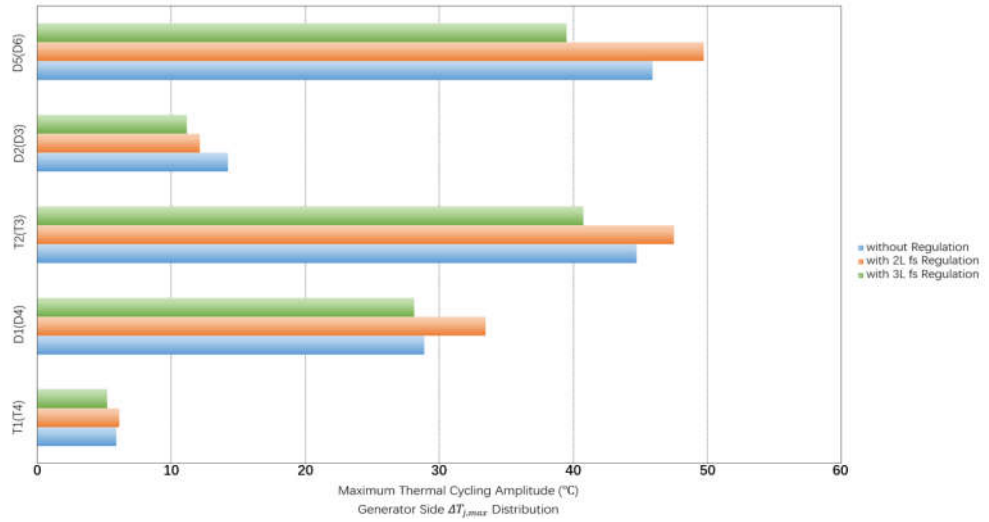

Figure 5. 37 Maximum Thermal Cycling Amplitude Distribution at Generator Side (with fs Regulation)

5.4 Summery of Switching Frequency Active Control

With all the comparisons regarding to the thermal performance demonstrated in this chapter, it can be summarized that the three-level switching frequency active control has positive regulation results on reducing the thermal amplitudes ΔT during big thermal cycles and decreasing the mean junction temperature. With the modification of these two most significant factors that influence the lifetime of semiconductors, N_f should be extended with sufficient reasons, as for the extension level brought by switching frequency regulation, it needs to be further quantified in conjunction with the lifetime model, which will be comprehensively illustrated in chapter 7 with other regulation results.

However, the selected low switching frequency brings large DC bus ripple current. Thus, to avoid big DC bus voltage ripple, the system requires a larger capacitor. A better quality filter needs to be installed on DC bus, which gives higher economic demands.

6. Reactive Current Regulation

Chapter 6 is mainly focused on the methodology, model establishment and simulation results analysis based on the reactive current active control. Contents of chapter 6 are as follows:
1, The reactive power injection is achieved by varying power factors at grid side while it is obtained by I_d current injection at the generator side.
2, The reactive current regulation is started with one-level junction temperature consideration as the reference to build up 3D lookup table together with wind speed and power factor (or I_d current).
3, The thermal simulation result of one-level T_j consideration reactive current regulation is noticed that causes pretty high mean junction temperature, based on this issue, the two-level T_j consideration reactive current regulation is introduced as an improvement.

6.1. Principle of Reactive Current Active Control

In the previous study [21], the grid side converter is considered with the constant power factor 0.9, and the d-axis current at generator side is set as 0, which represents that the system operates under a relatively high active power mode. In fact, the increasing of the reactive power required by the system causes extra losses, varying reactive power is another method to change power cycling and can therefore affect the lifetime of semiconductors. Due to these effects are not considered in the previous study, in this chapter, reactive current regulation is introduced as another active control method to improve converter reliability.
The purpose of reactive current active control is to minimize thermal cycle amplitudes similar to last chapter, and to keep the mean junction temperature as low as possible. The system should be able to vary $T_{j,mean}$ by shifting the reactive power when the wind speed changed, and the ideal result is that the system achieves more flat oscillation of T_j. Comparing with the hysteresis control method used in the switching frequency regulation method in last chapter, which is to avoid the fractional harmonics by fs shifting too often, the reactive power can be modified continuously under any time interval without harmonic effects.

6.2 Methodology and Simulation Results of Grid Side Reactive Current Control

For the grid side, the active power is defined as the following equation:

$$\mathrm{P} = \frac{3}{2} UI \cos\varphi \tag{6-1}$$

where U is bus voltage, I is output current and $\cos\varphi$ represents power factor (PF). The active power is increased by the rising wind speed, if U and $\cos\varphi$ are fixed in the system, the only variable that becomes larger as the increased active power is I, therefore, the increased current causes high switching loss and conduction loss for the grid side converter, which lead to high

junction temperature on each semiconductor, obviously this is the result that this thesis does not expect to get. Since P rises with the wind speed is not controllable, under the premise that the bus voltage keeps constant, improving $\cos\varphi$ becomes the only alternative to inhibit current increasing. In other words, when the wind speed is relatively high, PF can be increased to weaken the rising rate of output current. Thus, T_j is affected by varying PF, and $T_{j,mean}$ also depends on different wind speeds, figuring out the relation between V_{wind}, $T_{j,mean}$ and PF becomes the first target for the grid side power factor control, a three-dimension lookup table based on these variables can be established by following steps:

1, The semiconductor has the worst thermal performance is again considered as the one to provide reference junction temperature.

2, Making the system operates under one fixed PF condition each time, and then varying wind speeds.

3, The operation time should be at least 10s to make sure the junction temperature arrives steady state value.

4, Each circumstance gets a curve, all the curves are merged together to complete the three-dimension lookup table based on V_{wind}, $T_{j,mean}$ and PF as figure 6.1 shows. The details of the Matlab code to plot it can be found in appendix 2.

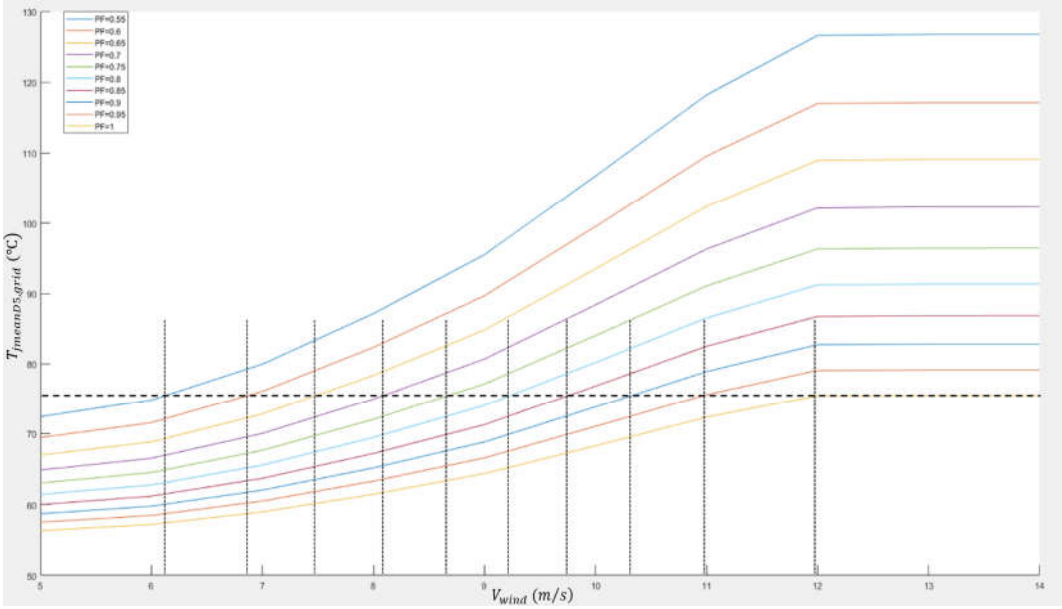

Figure 6. 1 3D Lookup Table Related to PF, V_{wind} and $T_{jmeanD5,grid}$

In figure 6.1, the vertical axis represents mean junction temperature of D5 while the horizontal axis represents wind speed, and the colored curves correspond to different PF values. The variable range of PF is set from 0.55 to 1 and divided into ten segments on average, and the wind speed points start at 5m/s up to 14m/s. Observing one degree of $T_{jmeanD5,grid}$ that can cover all the PF values under different wind speeds, which is showed as the thick horizontal dotted line in figure 6.1. The ten vertical thin dotted lines can be introduced to record all the cross points and their corresponded wind speeds. Table 6.1 demonstrates the corresponding relationship between wind speed and power factor.

Wind Speed (m/s)	Power Factor
6.1	0.55
6.9	0.6
7.5	0.65
8.1	0.7
8.7	0.75
9.2	0.8
9.7	0.85
10.3	0.9
11	0.95
12	1

Table 6. 1 Values of V_{wind} and PF

Importing those points into Matlab, the simulation model with the lookup table related to V_{wind} and PF based on one-level $T_{j,mean}$ consultation (in this case around 77℃) can be established as figure 6.2, and the regulation state of power factors is shown in figure 6.3.

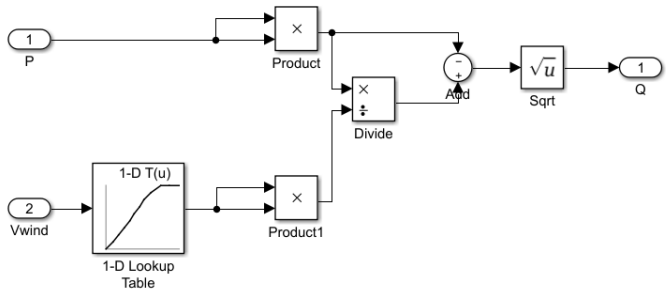

Figure 6. 2 Simulation Model with 1D Lookup Table Related to V_{wind} and PF

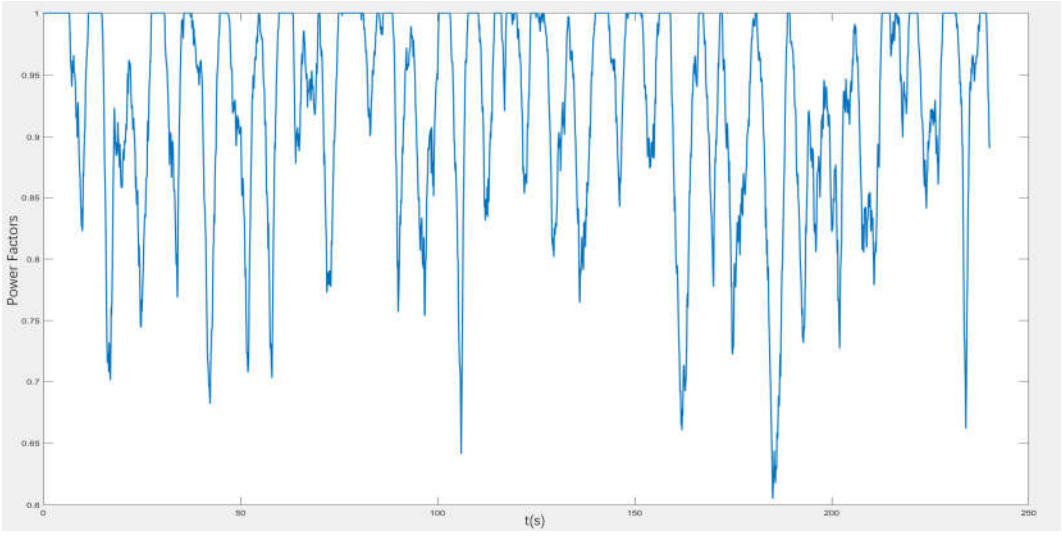

Figure 6. 3 PF Regulation Result Based on 1L $T_{j,mean}$ Consultation

Figure 6.4 shows the junction temperature of D5 from grid side after one-level $T_{j,mean}$ consultation PF regulation, compared to figure 5.17, which demonstrates $T_{jD5,grid}$ after three-level switching frequency regulation, the oscillation tendency of the junction temperature becomes flatter, however, the mean junction temperature during the whole operation rises up slightly.

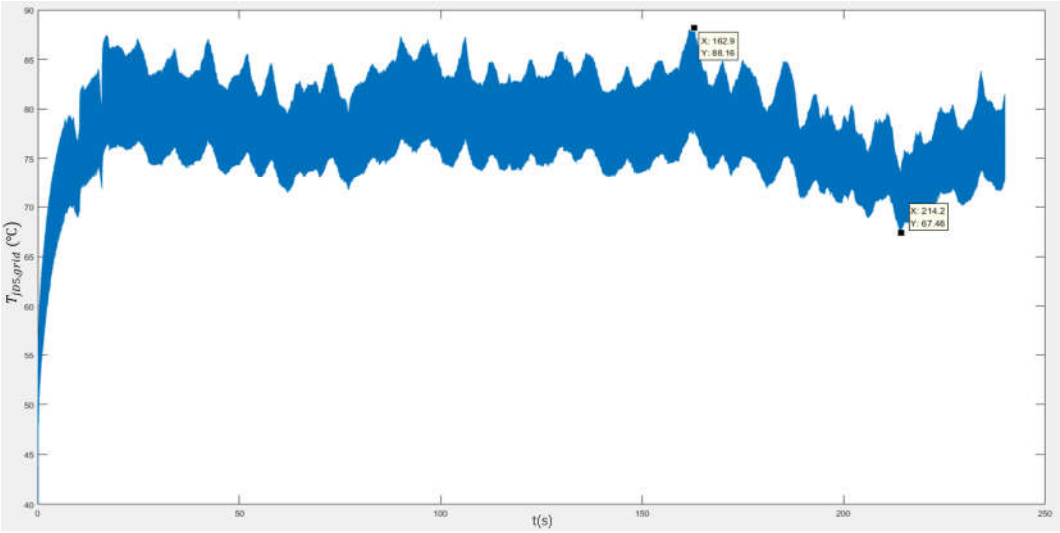

Figure 6. 4 $T_{jD5,grid}$ after 1L PF Regulation

The different thermal losses of grid side D5 obtained by without regulation and with one-level PF regulation are distributed in figure 6.5. Observing figure 6.3, since a large amount of reactive current is injected under the low wind speed conditions, the total current increases at those moments, so does the thermal loss.

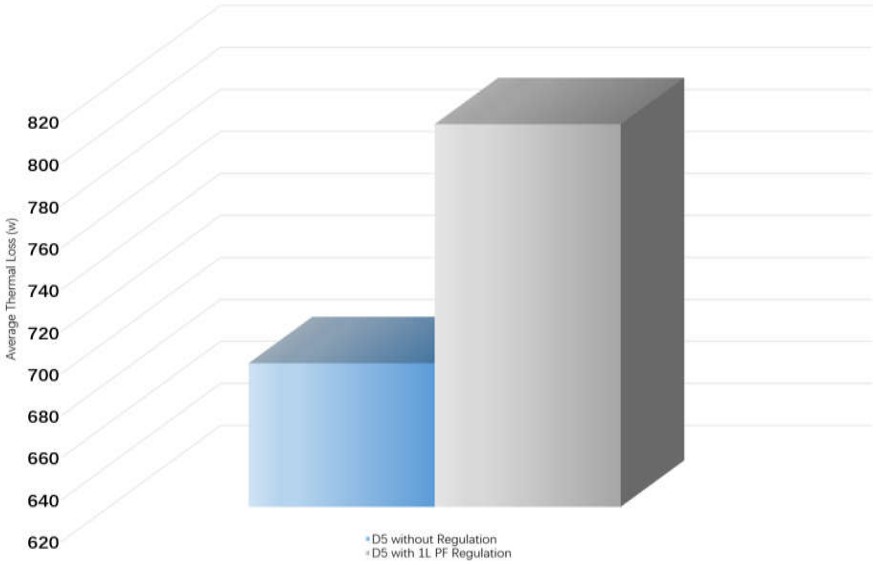

Figure 6. 5 $P_{D5,grid}$ Distribution (with 2 Conditions)

The maximum thermal cycle amplitudes and the mean junction temperatures on different semiconductors based one-level power factor regulation are recorded separately in table 6.2 and table 6.3.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (℃)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	17.02
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	8.66
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	12.94
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	1.72
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	20.7

Table 6. 2 $\Delta T_{j,max}$ Values of 3L-NPC Grid Side Semiconductors with 1L PF Regulation

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	67.5255
$T_{jD1mean,grid}(T_{jD4mean,grid})$	48.5123
$T_{jT2mean,grid}(T_{jT3mean,grid})$	52.7177
$T_{jD2mean,grid}(T_{jD3mean,grid})$	43.4692
$T_{jD5mean,grid}(T_{jD6mean,grid})$	77.3284

Table 6. 3 Mean T_j Values of 3L-NPC Grid Side Semiconductors with 1L PF Regulation

Since mean junction temperature is one of the most important factors that influences the lifetime of semiconductor, the higher $T_{j,mean}$ generated after one-level PF regulation may not be helpful to extend the lifetime of D5 from grid side. Even though those large amplitudes exist in big thermal cycles obtain significant reduction. Furthermore, figure 6.3 shows that the lowest power factor is around 0.6 after applying one-level reactive current regulation to the system, in terms of grid power supply, it is not allowed to inject such a large amount of reactive current. Based on those drawbacks illustrated above, it is necessary to find out a solution that can both decrease $T_{j,mean}$ and allow PF to float within an acceptable range for the grid. Another relatively low degree of $T_{jmeanD5,grid}$ that can cover half of the PF values under different wind speeds is introduced in the three-dimension lookup table, which is showed as the red thick horizontal dotted line in figure 6.6.

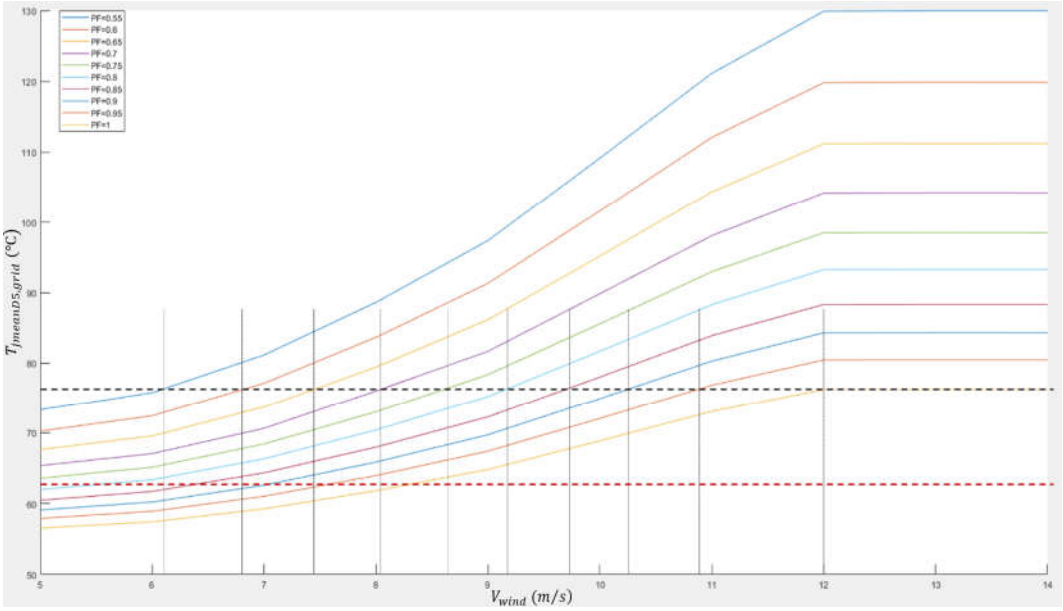

Figure 6. 6 3D Lookup Table Related to PF, V_{wind} and $T_{jmeanD5,grid}$ with 2L $T_{j,mean}$ Selection

The principle of this action can be explained as the PF points crossed by the red thick dotted line has the priority for the system to recognize and to select when it operates under certain wind speeds. The system considers the PF points crossed by the black thick dotted line only when the instantaneous junction temperature is lower than the red line, which is around 63°C. In other words, T_j will oscillate more often around 63°C instead of the previous 77°C, meanwhile, the entire grid side system will also operate under those relatively larger power factors. Table 6.4 demonstrates the corresponding relationship between wind speed and power factor based on the second level $T_{j,mean}$ consultation.

Wind Speed (m/s)	Power Factor
6.1	0.82
6.9	0.88
7.5	0.94
8.1	0.98
8.7	1
9.2	1
9.7	1
10.3	1
11	1
12	1

Table 6. 4 Values of V_{wind} and PF Based on 2nd $T_{j,mean}$ Consultation

Transferring these points into Matlab, together with the data recorded in table 6.1 based on the first level $T_{j,mean}$ selection, the simulation model with the two-dimension lookup table related to V_{wind} and PF can be established as figure 6.7. The function of the relay and the switch here is to let the system distinguish two levels of the junction temperature. The PF regulation result based on two-level $T_{j,mean}$ consultation is shown in figure 6.8.

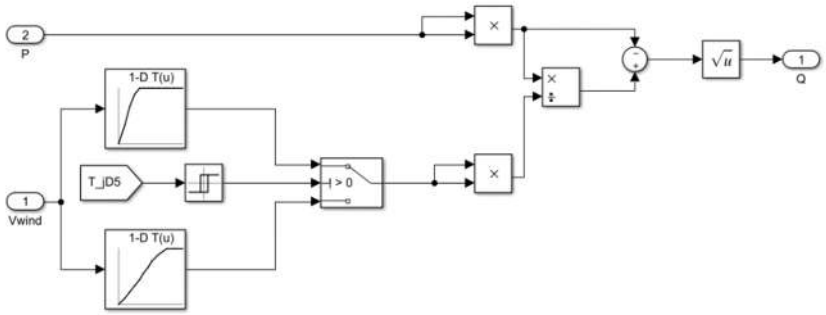

Figure 6. 7 Simulation Model with 2D Lookup Table Related to V_{wind} and PF

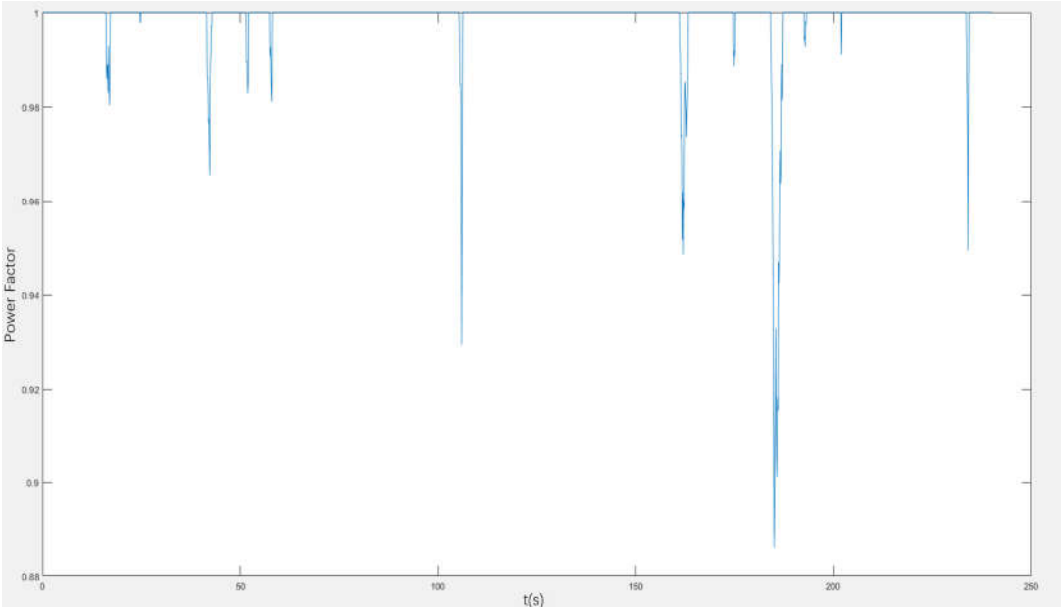

Figure 6. 8 PF Regulation Result Based on 2L $T_{j,mean}$ Consultation

The variation range of PF is from 0.89 to 1, compared with the one only applying one-level regulation, which has the PF range from 0.6 to 1, the result shows in figure 6.8 is much closer to the situation that is actually allowed by the grid side power supply. Figure 6.9 shows the junction temperature of D5 from grid side after two-level $T_{j,mean}$ consultation PF regulation, compared with figure 6.4, $T_{jmeanD5,grid}$ is reduced to a certain level.

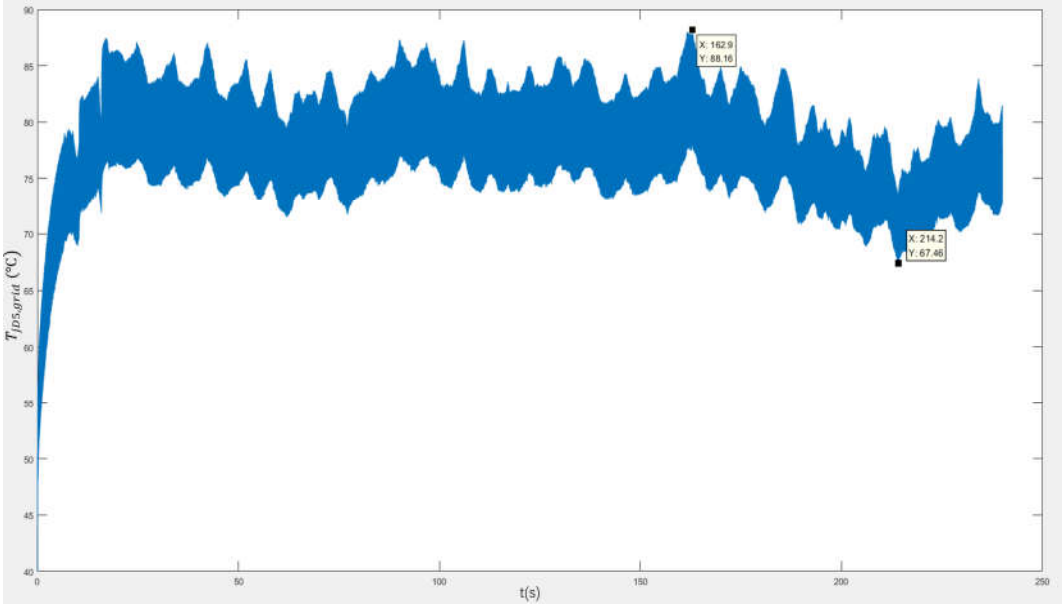

Figure 6. 9 $T_{jD5,grid}$ after 2L PF Regulation

The different thermal losses of grid side D5 obtained by without regulation, with one-level PF regulation and with two-level PF regulation are distributed in figure 6.10. Since the injected reactive current with two-level PF regulation becomes less during the entire operation process, and the mean junction temperature decreases, the thermal loss is reduced as the result.

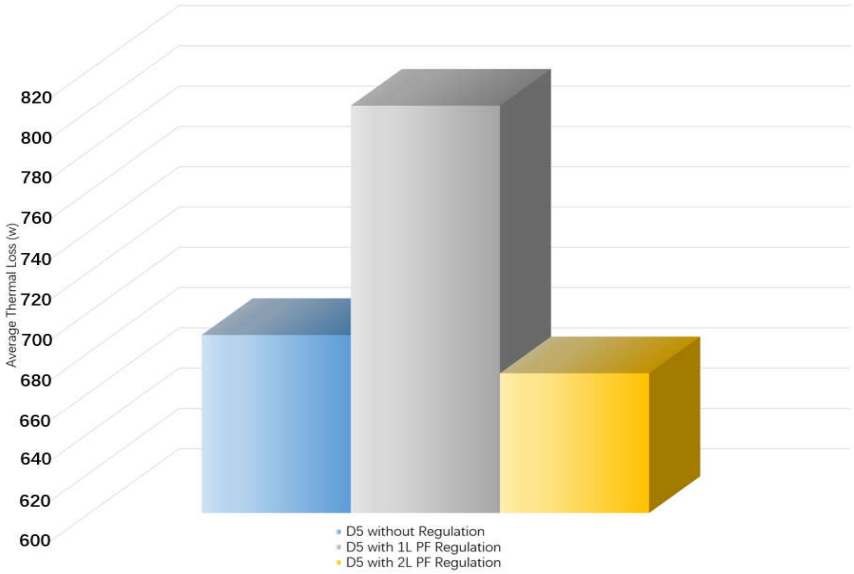

Figure 6. 10 $P_{D5,grid}$ Distribution (with 3 Conditions)

The maximum thermal cycle amplitudes and the mean junction temperatures on different semiconductors based two-level power factor regulation are recorded separately in table 6.5 and table 6.6.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	16.44
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	3.36
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	5.28
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	0.6
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	20.07

Table 6. 5 $\Delta T_{j,max}$ Values of 3L-NPC Grid Side Semiconductors with 2L PF Regulation

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	68.9766
$T_{jD1mean,grid}(T_{jD4mean,grid})$	46.4454
$T_{jT2mean,grid}(T_{jT3mean,grid})$	48.0601
$T_{jD2mean,grid}(T_{jD3mean,grid})$	42.2840
$T_{jD5mean,grid}(T_{jD6mean,grid})$	72.4651

Table 6. 6 Mean T_j Values of 3L-NPC Grid Side Semiconductors with 2L PF Regulation

According to recorded data, the comprehensive distribution charts related to average thermal loss, maximal amplitude of thermal cycle and mean junction temperature of each semiconductor at the grid side can be found in following figures:

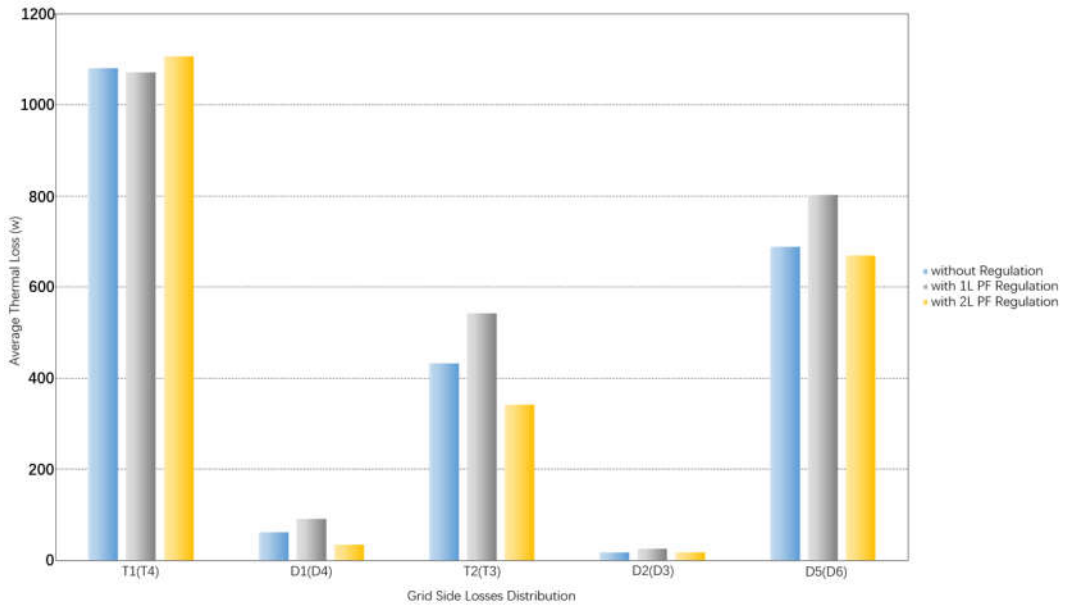

Figure 6. 11 Average Thermal Losses Distribution of Semiconductors at Grid Side (with PF Regulation)

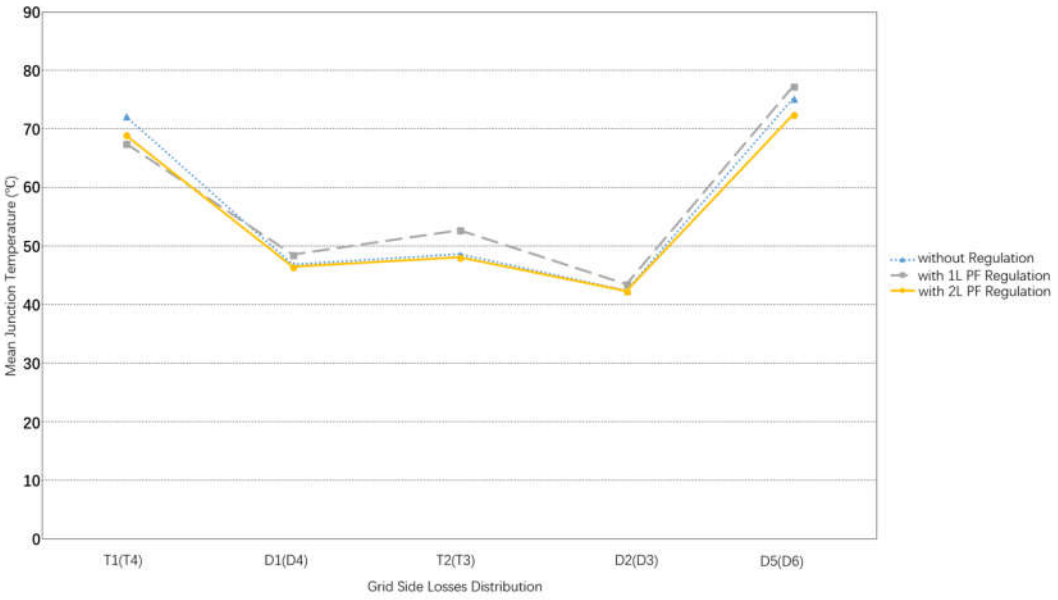

Figure 6. 12 Mean Junction Temperature Distribution at Grid Side (with PF Regulation)

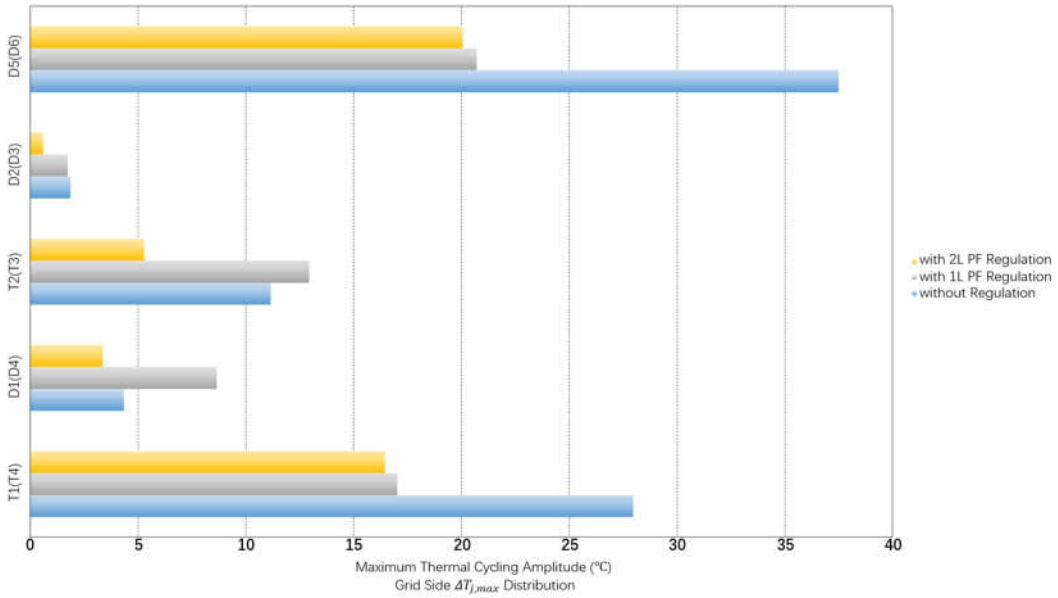

Figure 6. 13 Maximum Thermal Cycling Amplitude Distribution at Grid Side (with PF Regulation)

6.3 Methodology and Simulation Results of Generator Side Reactive Current Control

The rotor side is connected with wind turbine directly, when wind blows, the rotor starts to move, and the stator follows to rotate. The three-phase current generated from stator side can be transferred from abc frame to dq frame, which are I_d and I_q. The equivalent circuit of a PMDD generator related to d-axis and q-axis is shown in figure 6.14. The relations in this equivalent circuit are shown in equation (6-2) and (6-3).

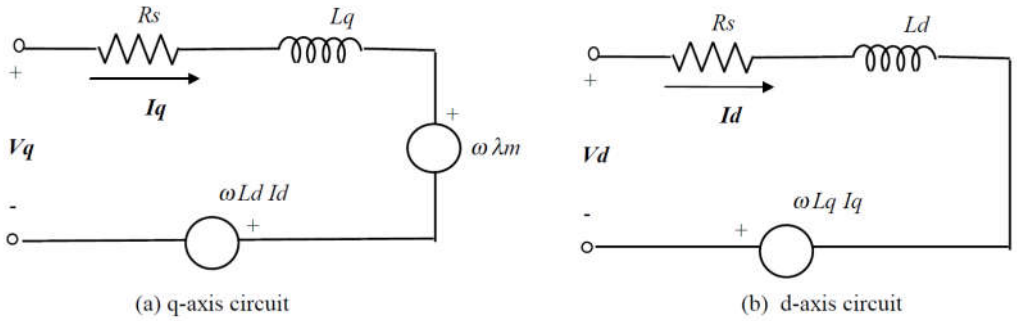

Figure 6. 14 Equivalent Circuit of PMDD Generator

$$\begin{cases}\lambda_d = \lambda_m + L_d i_d \\ \lambda_q = L_q i_q\end{cases} \tag{6-2}$$

$$\begin{cases}V_d = \frac{d\lambda_d}{dt} - \omega\lambda_q \\ V_q = \frac{d\lambda_q}{dt} + \omega\lambda_d\end{cases} \tag{6-3}$$

where,

λ_m: flux linkage induced by the rotor magnet

λ_d: flux linkage along d-axis

λ_q: flux linkage along q-axis

ω: electrical angular speed

V_d: voltage component along d-axis

V_q: voltage component along q-axis

Combine these two equations demonstrated above, the new expression of V_d and V_q becomes:

$$\begin{cases}V_d = \frac{d(\lambda_m + L_d i_d)}{dt} - \omega L_q i_q \\ V_q = \frac{dL_q i_q}{dt} + \omega(\lambda_m + L_d i_d)\end{cases} \tag{6-4}$$

Under the steady state situation, equation (6-4) can be simplified as following:

$$\begin{cases}V_d = -\omega L_q i_q \\ V_q = \omega(\lambda_m + L_d i_d)\end{cases} \tag{6-5}$$

Generally, for a permanent magnet synchronous generator, the way to calculate active power can be summarized as following equation:

$$\mathrm{P} = \frac{3}{2}\left(V_d i_d + V_q i_q\right) \tag{6-6}$$

Substituting formula (6-5) into (6-6), the active power can be defined as following:

$$\mathrm{P} = \frac{3}{2}\left[-\omega L_q i_q i_d + \omega(\lambda_m + L_d i_d) i_q\right]$$

$$= \frac{3}{2}\left[\omega\lambda_m i_q + \omega(L_d - L_q) i_d i_q\right] \tag{6-7}$$

In equation (6-7), $\omega\lambda_m$ and $\omega(L_d - L_q)$ represent E_q and $X_d - X_q$ respectively, thus, the active power can be rewritten as equation (6-8) shown below:

$$\mathrm{P} = \frac{3}{2}\left[E_q i_q + (X_d - X_q) i_d i_q\right] \tag{6-8}$$

Due to the surface permanent synchronous generator is used in the system, X_d is equal to X_q in this case, the active power is only related to E_q and i_q, hence, injected i_d does not affect the generator output power at any moment.

When the wind speed is high, the rotor rotates fast, it causes high active power, so the q-axis current i_q and the induced electromotive force E_q are also high, and the high junction temperature T_j is caused by high current. When the wind speed is low, all the factors own the opposite property. Similar to the control principle mentioned at the section of two-level switching frequency regulation, the most direct way to decrease ΔT is to raise up T_j when the wind speed is low. T_j is related to switching and conduction losses, if P_{swit} and P_{cond} can be increased when the wind speed is low, the goal can be obtained. Since power losses are proportional to current, and the generator output power is not influenced by the reactive current injection, i_d is chosen to be injected with different levels based on the wind speeds, the relation between them can be summarized as the lower the wind speed is, the larger i_d should be injected.

Similar to the grid side, the three-dimension lookup table based on V_{wind}, $T_{j,mean}$ and I_d can be established by following steps:

1, D5 as the semiconductor that has the worst thermal performance is considered to provide reference junction temperature.

2, Making the system operates under one fixed I_d condition each time, and then varying wind speeds.

3, The operation time should be at least 10s to make sure the junction temperature arrives steady state value.

4, Each circumstance gets a curve, all the curves are merged together to complete the three-dimension lookup table based on V_{wind}, $T_{j,mean}$ and I_d as figure 6.15 shows, and the details of the Matlab code to plot it can be found in appendix 3.

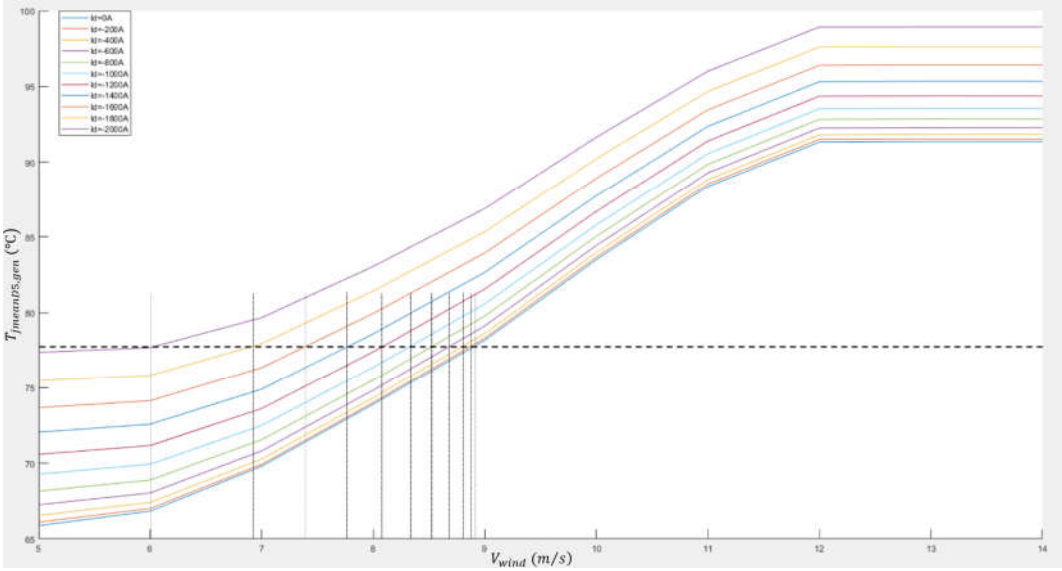

Figure 6. 15 3D Lookup Table Related to I_d, V_{wind} and $T_{jmeanD5,gen}$

In figure 6.15, the vertical axis represents mean junction temperature of D5 while the horizontal axis represents wind speed, and the colored curves correspond to different I_d values. From the perspective of demagnetizing, the injected I_d values are considered to be negative, otherwise the iron core saturation issue of stator appears, and L_d is not equal to L_q by the time, the previous derivation under this condition loses its significance. The variable range of I_d is set from -2000 to 0 and divided into ten segments on average, and the wind speed points start at 5m/s up to 14m/s. The thick horizontal dotted line in figure 6.15 represents the lowest degree of $T_{jmeanD5,gen}$ that can cover all the I_d values under different wind speeds. It can be noticed that from 78℃ to 90℃,

drawing a horizontal line at any degree ensures the chosen $T_{jmeanD5,gen}$ covering all I_d values. The reason to choose the lowest degree is to avoid higher mean junction temperature leads to shorter semiconductor lifetime. After marking ten vertical thin dotted lines to record all the cross points and their corresponded wind speeds, the corresponding relationship between wind speed and I_d is shown in table 6.7.

Wind Speed (m/s)	I_d (A)
6	-2000
6.9	-1800
7.4	-1600
7.7	-1400
8.1	-1200
8.4	-1000
8.5	-800
8.6	-600
8.8	-400
8.9	-200
9	0

Table 6. 7 Values of V_{wind} and I_d

Importing those points into Matlab, the simulation model with the lookup table related to V_{wind} and I_d based on one-level $T_{j,mean}$ consultation (in this case around 78℃) can be established as figure 6.16, and the regulation state of I_d is shown in figure 6.17.

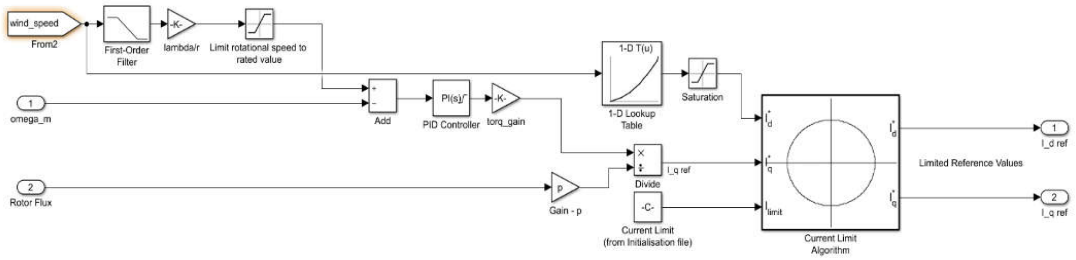

Figure 6. 16 Simulation Model with 1D Lookup Table Related to V_{wind} and I_d

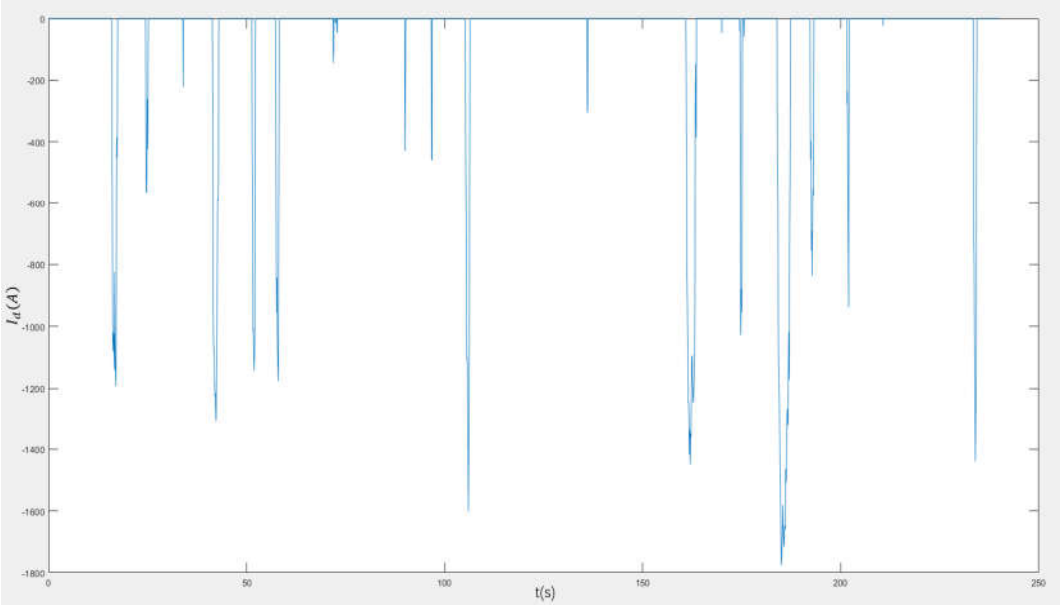

Figure 6. 17 I_d Regulation Result Based on 1L $T_{j,mean}$ Consultation

Figure 6.18 shows the junction temperature of D5 from generator side after one-level $T_{j,mean}$ consultation reactive current regulation. Those large differences existed on T_j during big thermal cycles get remarkable reduction. However, the mean junction temperature is around 91℃ instead of the chosen degree 78℃. Based on the points shown in table 6.7, reactive current injection only happens when the wind speed is lower than 9m/s. When V_{wind} is above 9m/s, this control method reaches its upper limit, the semiconductor junction temperature cannot be reduced anymore, because I_d is already kept at 0. In the given wind profile figure 3.10, the wind speed that is higher than 9m/s appears most of the time, the system mostly operates under zero reactive current mode as figure 6.17 shown, so it leads to a relatively higher mean junction temperature.

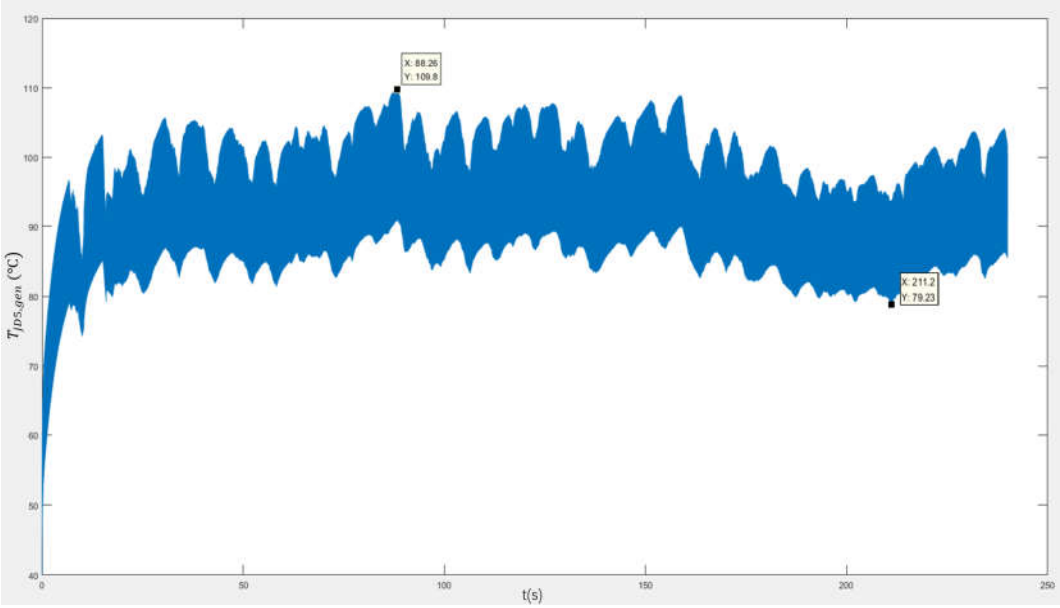

Figure 6. 18 $T_{jD5,gen}$ after 1L RC Regulation

The maximum thermal cycle amplitudes and the mean junction temperatures on different semiconductors based one-level reactive current regulation are recorded separately in table 6.8 and table 6.9.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	4.28
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	20.03
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	30.45
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	8.15
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	30.57

Table 6. 8 $\Delta T_{j,max}$ Values of 3L-NPC Generator Side Semiconductors with 1L RC Regulation

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	45.7823
$T_{jD1mean,grid}(T_{jD4mean,grid})$	70.4470
$T_{jT2mean,grid}(T_{jT3mean,grid})$	91.8939
$T_{jD2mean,grid}(T_{jD3mean,grid})$	56.4430
$T_{jD5mean,grid}(T_{jD6mean,grid})$	91.6377

Table 6. 9 Mean T_j Values of 3L-NPC Generator Side Semiconductors with 1L RC Regulation

Reference the two-level power factor regulation method is used to decrease $T_{j,mean}$ at the grid side, the reactive current at generator side can also try to be varied based on two-level $T_{j,mean}$ consultation. Another relatively low degree of $T_{jmeanD5,gen}$ that can cover half of the I_d values under different wind speeds is introduced in the three-dimension lookup table, which is shown as the red thick horizontal dotted line in figure 6.19.

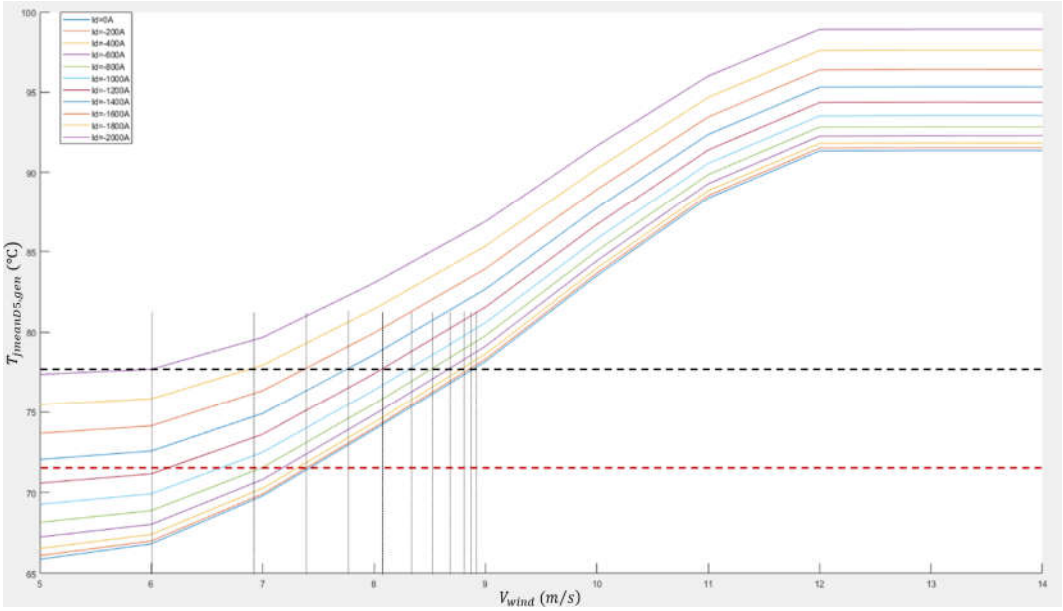

Figure 6. 19 3D Lookup Table Related to I_d, V_{wind} and $T_{jmeanD5,gen}$ with 2L $T_{j,mean}$ Selection

Table 6.10 demonstrates the corresponding relationship between wind speed and I_d based on the second level $T_{j,mean}$ consultation.

Wind Speed (m/s)	I_d (A)
6	-1250
6.9	-850
7.4	-200
7.7	0
8.1	0
8.4	0
8.5	0
8.6	0
8.8	0
8.9	0
9	0

Table 6. 10 Values of V_{wind} and I_d Based on 2nd $T_{j,mean}$ Consultation

Transferring these points into Matlab, together with the data recorded in table 6.7 based on the first level $T_{j,mean}$ selection, the simulation model with the two-dimension lookup table related to V_{wind} and I_d can be established as figure 6.20. The I_d regulation result based on 2-level $T_{j,mean}$ consultation is shown in figure 6.21.

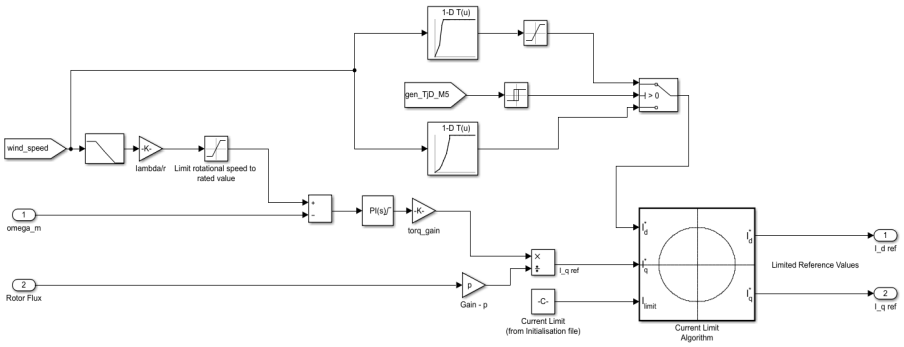

Figure 6. 20 Simulation Model with 2D Lookup Table Related to V_{wind} and I_d

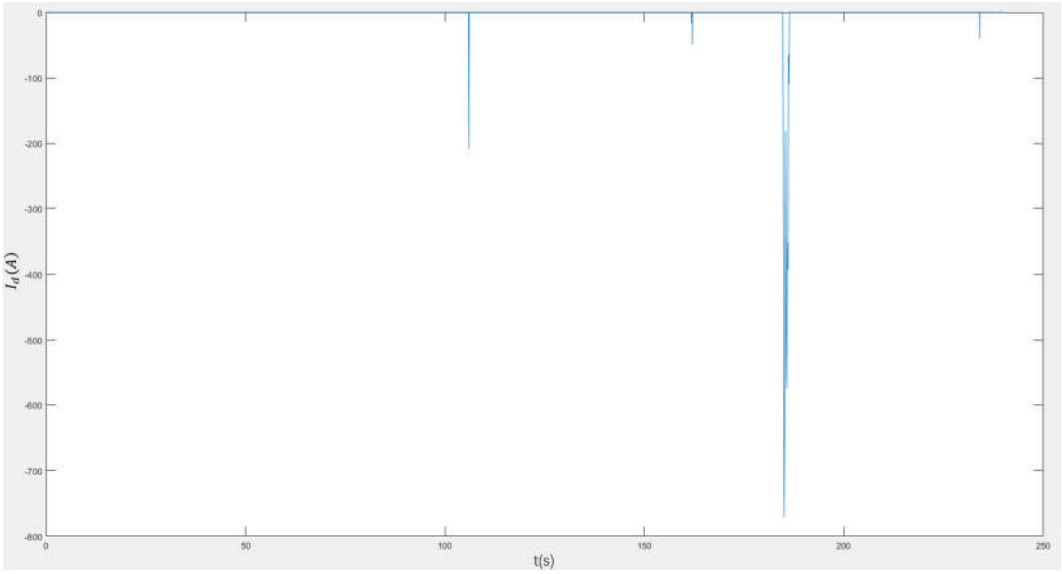

Figure 6. 21 I_d Regulation Result Based on 2L $T_{j,mean}$ Consultation

Figure 6.22 shows the junction temperature of D5 from generator side after two-level $T_{j,mean}$ consultation reactive current regulation, compare to figure 6.18, $T_{jmeanD5,gen}$ is not reduced obviously. Because with the second level $T_{j,mean}$ consultation, the reactive current is injected when the wind speed is lower than 7.7m/s, compare to the previous one-level regulation, which injects reactive current below 9m/s, the difference between these two wind speeds is too small to cause significant mean junction temperature reduction.

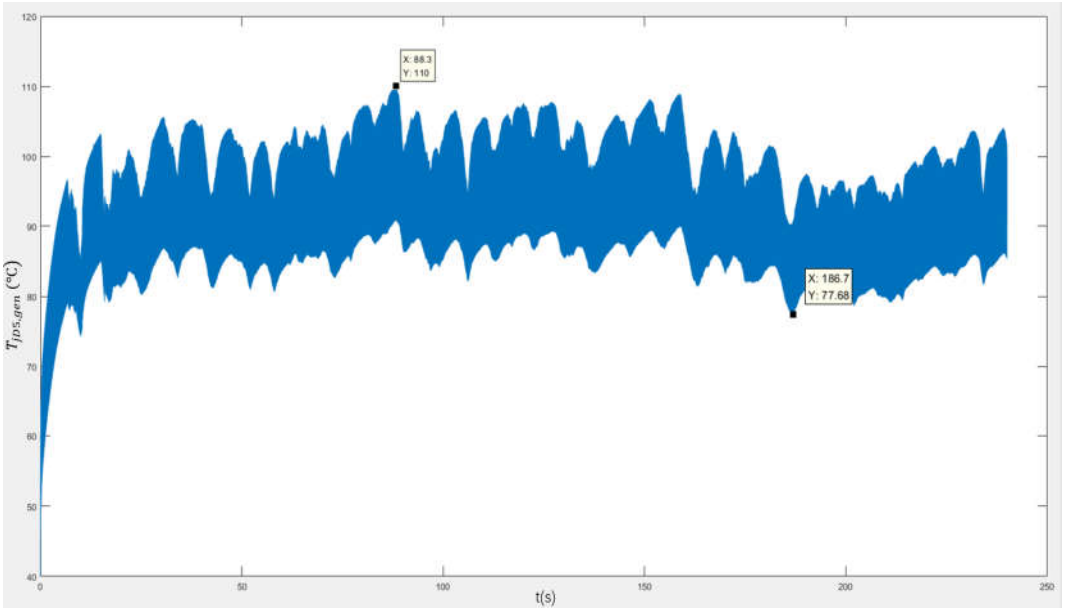

Figure 6. 22 $T_{jD5,gen}$ after 2L RC Regulation

The maximum thermal cycle amplitudes and the mean junction temperatures on different semiconductors based two-level reactive current regulation are recorded separately in table 6.11 and table 6.12.

Maximum junction temperature differences on different semiconductors ($\Delta T_{j,max}$)	Maximum values (°C)
$\Delta T_{jmaxT1,gen}(\Delta T_{jmaxT4,gen})$	4.37
$\Delta T_{jmaxD1,gen}(\Delta T_{jmaxD4,gen})$	21.12
$\Delta T_{jmaxT2,gen}(\Delta T_{jmaxT3,gen})$	30.71
$\Delta T_{jmaxD2,gen}(\Delta T_{jmaxD3,gen})$	8.24
$\Delta T_{jmaxD5,gen}(\Delta T_{jmaxD6,gen})$	32.32

Table 6. 11 $\Delta T_{j,max}$ Values of 3L-NPC Generator Side Semiconductors with 2L RC Regulation

Mean junction temperatures on different semiconductors ($T_{j,mean}$)	Average values (°C)
$T_{jT1mean,grid}(T_{jT4mean,grid})$	45.8302
$T_{jD1mean,grid}(T_{jD4mean,grid})$	70.3551
$T_{jT2mean,grid}(T_{jT3mean,grid})$	89.6280
$T_{jD2mean,grid}(T_{jD3mean,grid})$	56.4465
$T_{jD5mean,grid}(T_{jD6mean,grid})$	90.8642

Table 6. 12 Mean T_j Values of 3L-NPC Generator Side Semiconductors with 2L RC Regulation

It can be noticed that $\Delta T_{j,max}$ on each generator side semiconductor obtains slightly increase by two-level reactive current regulation. The significance of generator side reactive current regulation is to increase T_j at low wind speed to reduce ΔT_j. After introducing the second level $T_{j,mean}$

consultation, the factor points illustrated in table 6.10 have the priority to select corresponding parameters for the system. The reactive current control increases T_j when V_{wind} is lower than 9m/s with one-level regulation, and it only increases T_j when V_{wind} is lower than 7.7m/s with two-level regulation. The increasing extent of T_j is shortened by two-level regulation, so ΔT_j becomes larger.

According to recorded data, the comprehensive distribution charts related to average thermal loss, maximal amplitude of thermal cycle and mean junction temperature of each semiconductor at the generator side can be found in following figures:

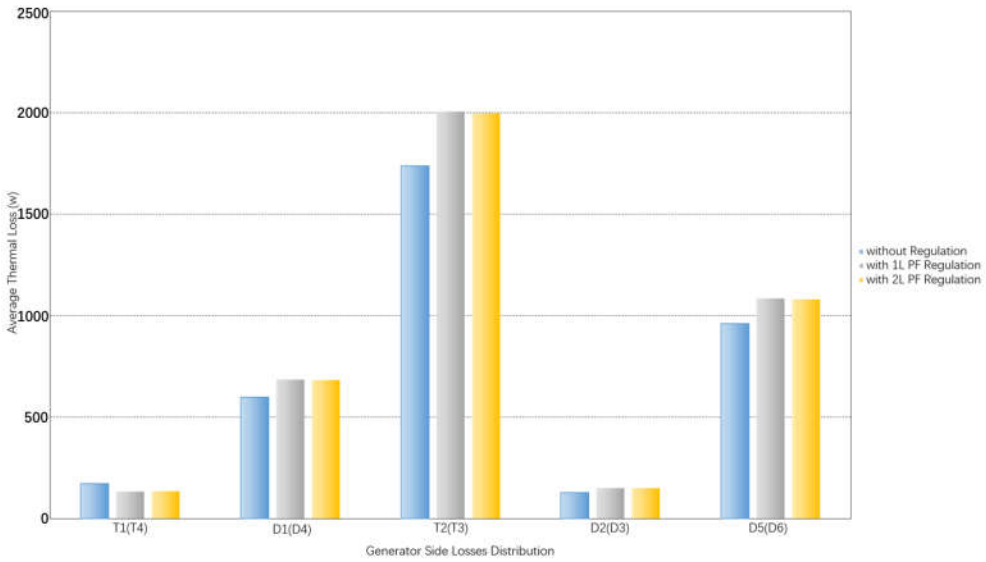

Figure 6. 23 Average Thermal Losses Distribution of Semiconductors at Generator Side (with RC Regulation)

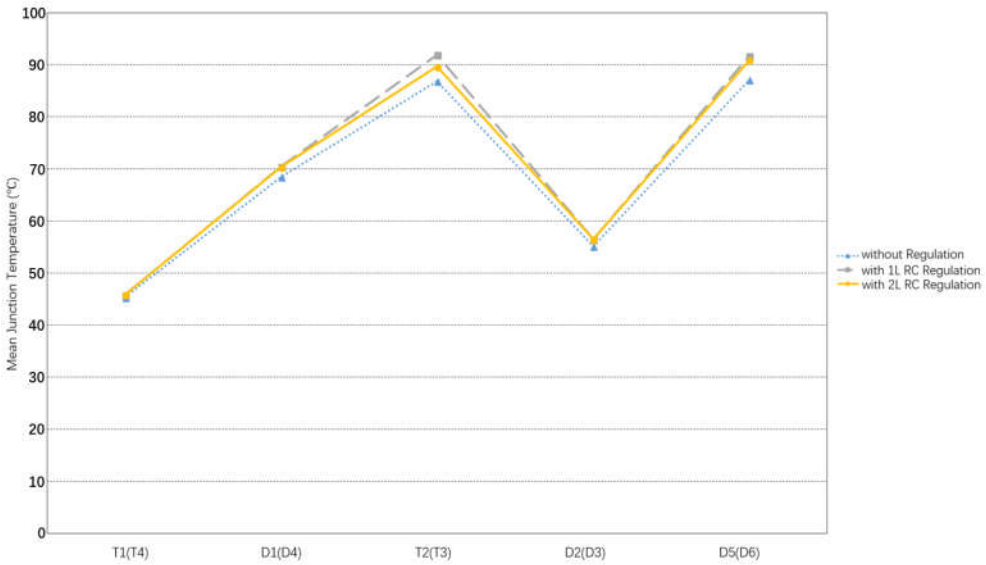

Figure 6. 24 Mean Junction Temperature Distribution at Generator Side (with RC Regulation)

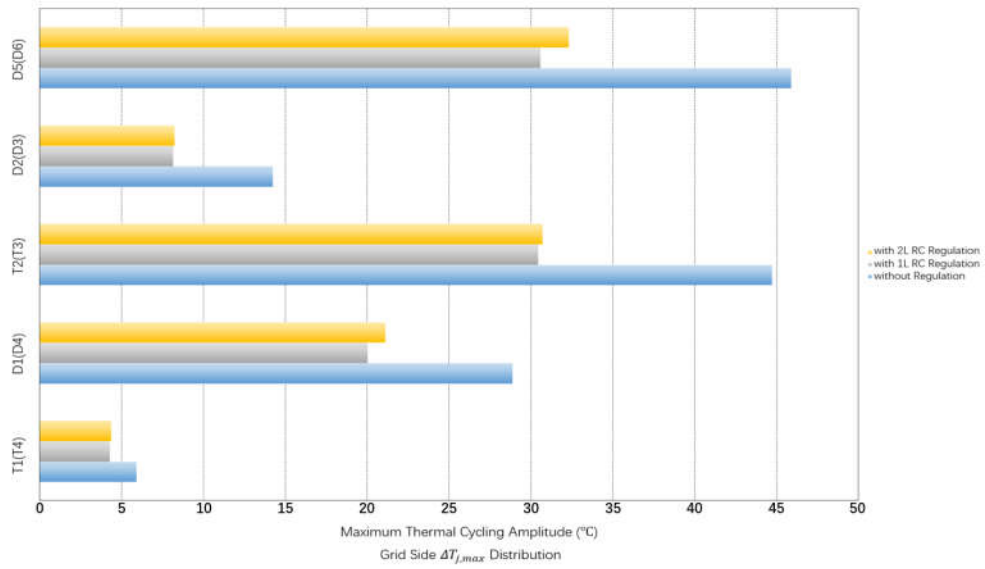

Figure 6. 25 Maximum Thermal Cycling Amplitude Distribution at Generator Side (with RC Regulation)

6.4 Summery of Reactive Current Active Control

With all the comparisons regarding to the thermal performance demonstrated in this chapter, it can be summarized that the two-level reactive current active control at grid side has positive regulation results on reducing the thermal amplitudes ΔT_j during big thermal cycles. However, compare to the system without constant power factor 0.9, the mean junction temperature at grid side does not achieve significant decrease. Because the regulated PF is mostly above 0.9, although it effectively inhibits the increase of output current when more active power is generated, the large PF values allow the system to use more active power. As long as the total thermal loss of each semiconductor does not change much, $T_{j,mean}$ will not drop remarkably. With the reduction of ΔT_j, the lifetime of grid side semiconductors should be extended, and the extension level needs to be further quantified in next chapter.

At generator side, the two-level reactive current regulation only decreases the mean junction temperature brought by one-level regulation a little bit, because the control upper limits of two different $T_{j,mean}$ consultations are relatively close. In addition, the two-level reactive current regulation causes slightly larger ΔT_j than one-level, because the upper limit of the wind speed that can be recognized becomes lower, and the increasing extent of T_j at low wind speed gets smaller. As a consequence, for the generator side control, one-level reactive current regulation is effective enough to recommend.

7. Lifetime Comparison Based on Different Control Methods

The Coffin-Manson equation indicated the characteristic of the bond wire lift off failure mechanism, there is a specific number of thermal cycles N_f that semiconductors can go through. N_f is exponentially dependent on the magnitude of the thermal cycles and average temperature. The study published by Bayerer *et al.* is used for the lifetime model establishment in this thesis [56], and the number of cycles to failure is defined by following equation:

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_j + 27\ 3}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (7\text{-}1)$$

where A is a technology factor, ΔT_j is the amplitude of the thermal cycling, T_j is the mean junction temperature, t_{on} is the pulse duration, I is the current per wire, V is the blocking voltage of the chip, and D is the diameter of the bonding wire. The impacts of these factors are represented by power laws with exponents $\beta_1 - \beta_6$. The exponential factors used are $\beta_1 = -4.416$, $\beta_2 = 1.285 \times 10^3$, $\beta_3 = -0.463$, $\beta_4 = -0.716$, $\beta_5 = -0.761$, and $\beta_6 = -0.5$. The value of A depends on the type of switch, $\mathrm{A} = 2.03 \times 10^{14}$ for standard packages and $\mathrm{A} = 9.34 \times 10^{14}$ for IGBT4 modules [57].

The method to record $\Delta T_{j,max}$ by maximum T_j point minus minimum T_j point during entire operation process, which is used in previous chapters for judging the active control influence cannot display the undulation of ΔT_j in every thermal cycle. Although that method is good enough to observe effects, $\Delta T_{j,max}$ results are definitely not sufficient or accurate to support the N_f calculation in this chapter. According to the above statements, rain flow counting method is introduced to calculate ΔT_j. It is based on the two-parameter calculation method: the dynamic strength (amplitude) and the static strength (mean). It meets the inherent characteristics of the fatigue loads. The rain flow counting method is mainly used in the engineering projects, especially in the calculation of lifetime.

Using the rain flow counting function in Matlab, the data with five columns of numbers can be achieved. The first column shows how many thermal cycles (normally between 0.5 to 1 per line), the second column is ΔT_j under these thermal cycles, the third column is the $T_{j,mean}$ under these thermal cycles, the fourth column shows the sampling start points, and the fifth column shows the sampling end points. The numbers of the second and the third columns obtained under different control methods can be imported into Excel in orders, and the comprehensive distribution based on mean junction temperatures and junction temperature differences can be demonstrated by introducing few targeted statistical graphs.

7.1 Thermal Cycle Amplitude Analysis

Since D5 has the worst performance from both grid side and generator side, the distribution comparison of ΔT_j under different control methods is based on this semiconductor. The Matlab code for rain flow counting can be found in appendix 4, and the distributions of ΔT_j under different control methods are shown from figure 7.1 to figurem7.10. In following figures, the horizontal axis represents the range of thermal cycle amplitude while the vertical axis represents the cycle counts.

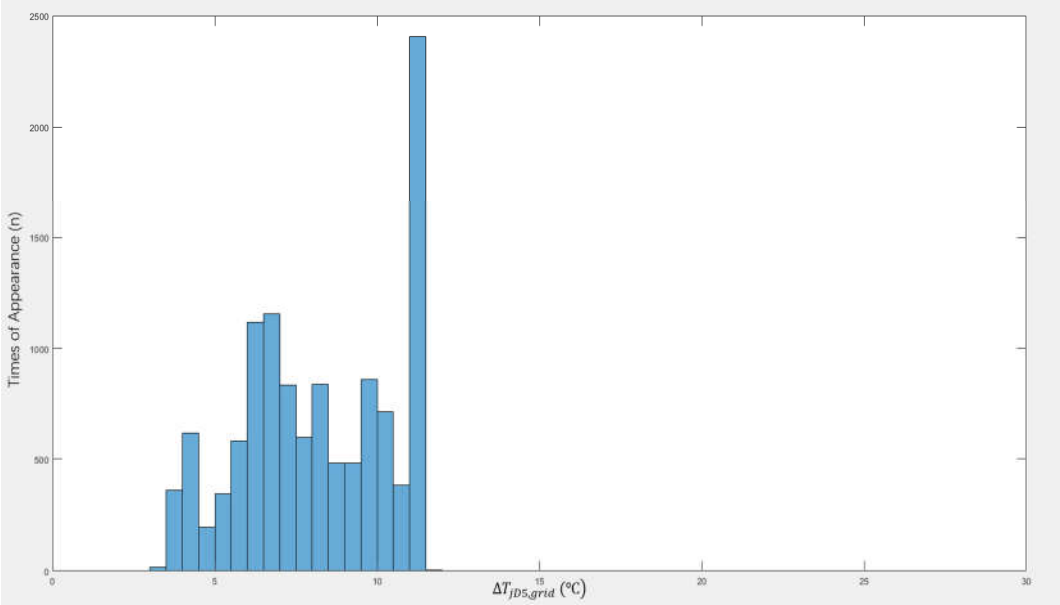

Figure 7. 1 $\Delta T_{jD5,grid}$ Distribution without Regulation

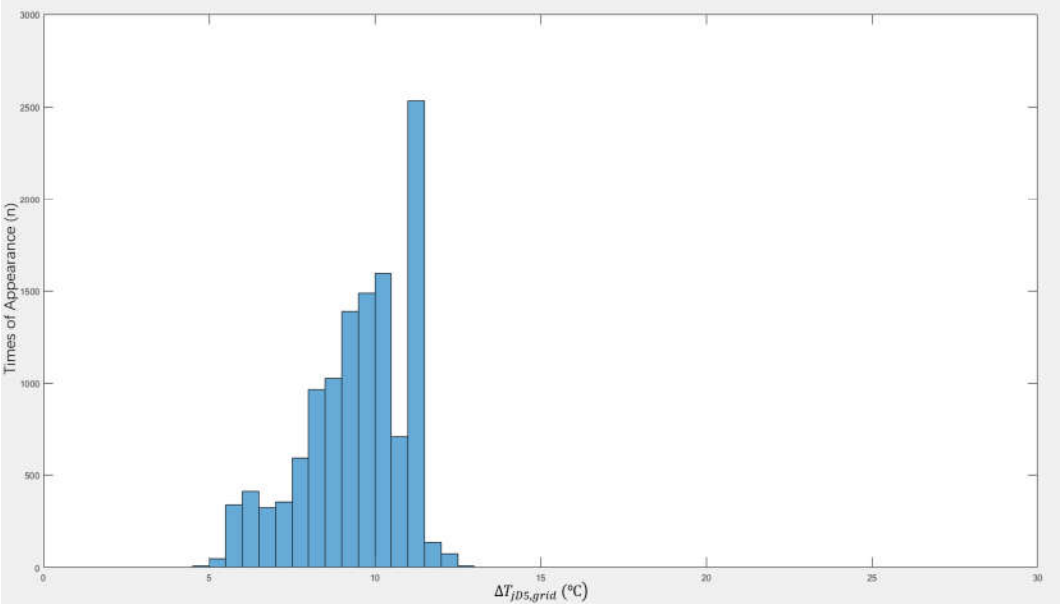

Figure 7. 2 $\Delta T_{jD5,grid}$ Distribution with 2L fs Regulation

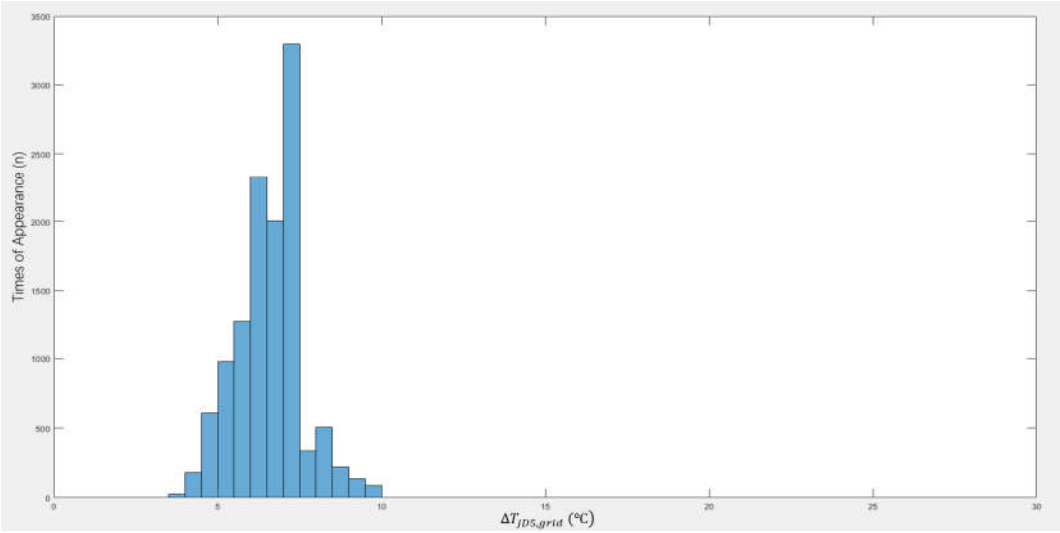

Figure 7. 3 $\Delta T_{jD5,grid}$ Distribution with 3L fs Regulation

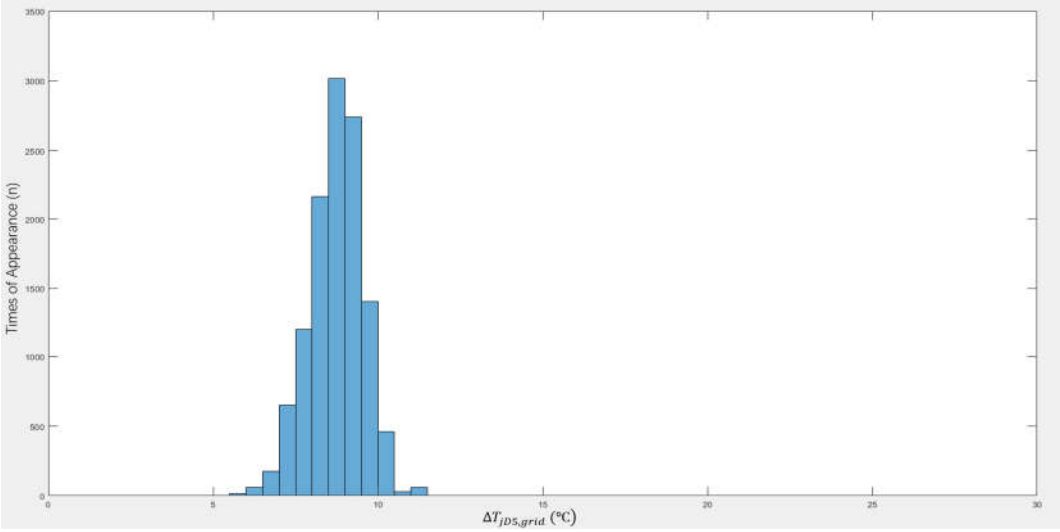

Figure 7. 4 $\Delta T_{jD5,grid}$ Distribution with 1L PF Regulation

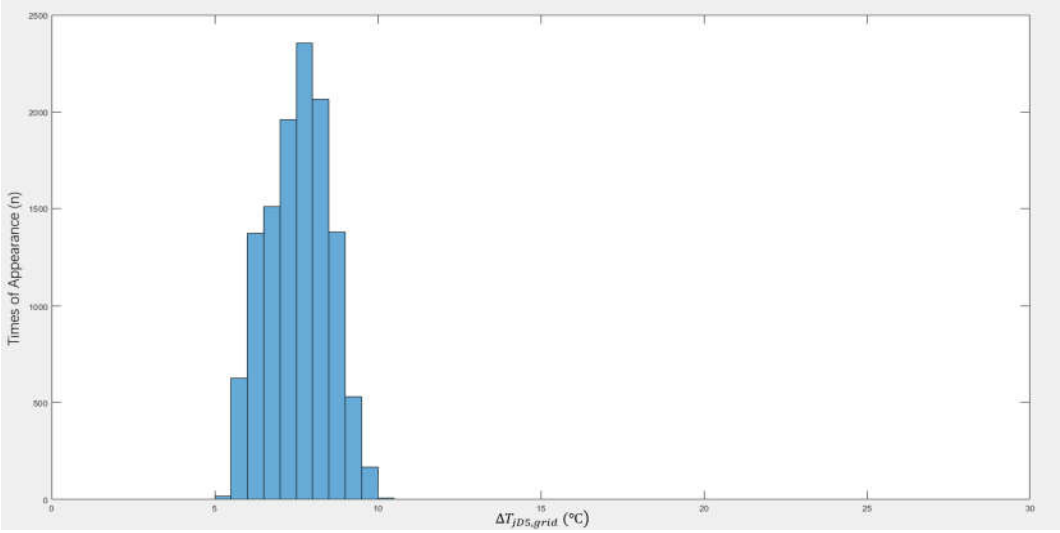

Figure 7. 5 $\Delta T_{jD5,grid}$ Distribution with 2L PF Regulation

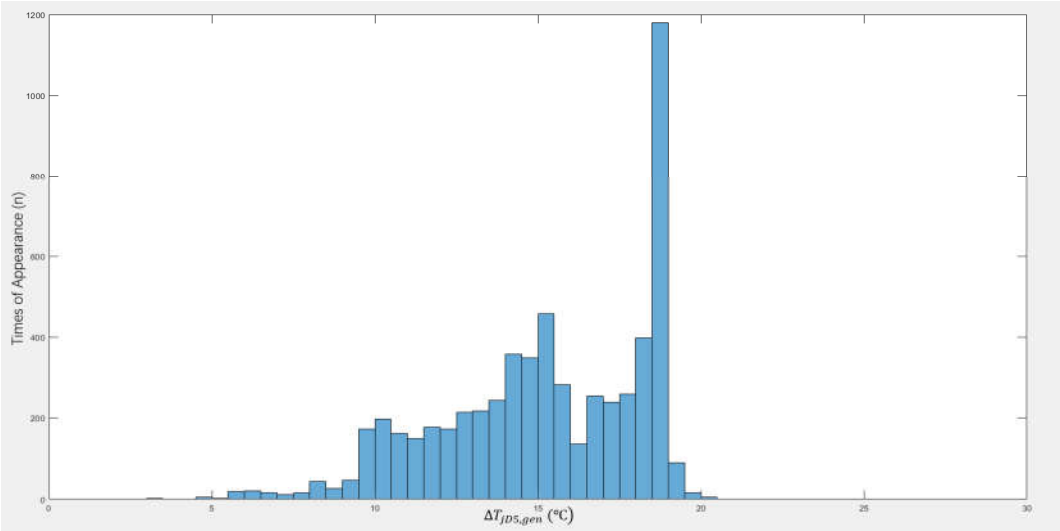

Figure 7. 6 $\Delta T_{jD5,gen}$ Distribution without Regulation

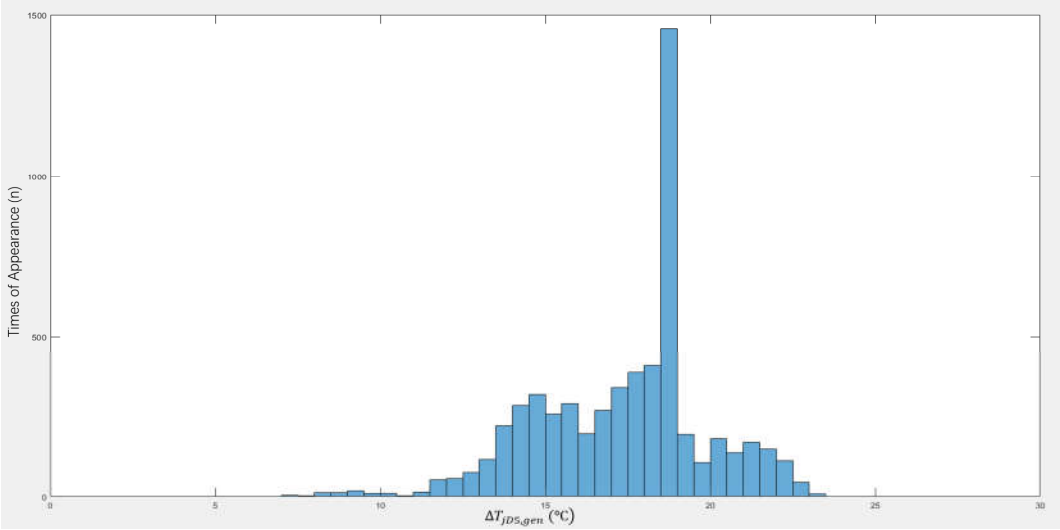

Figure 7. 7 $\Delta T_{jD5,gen}$ Distribution with 2L fs Regulation

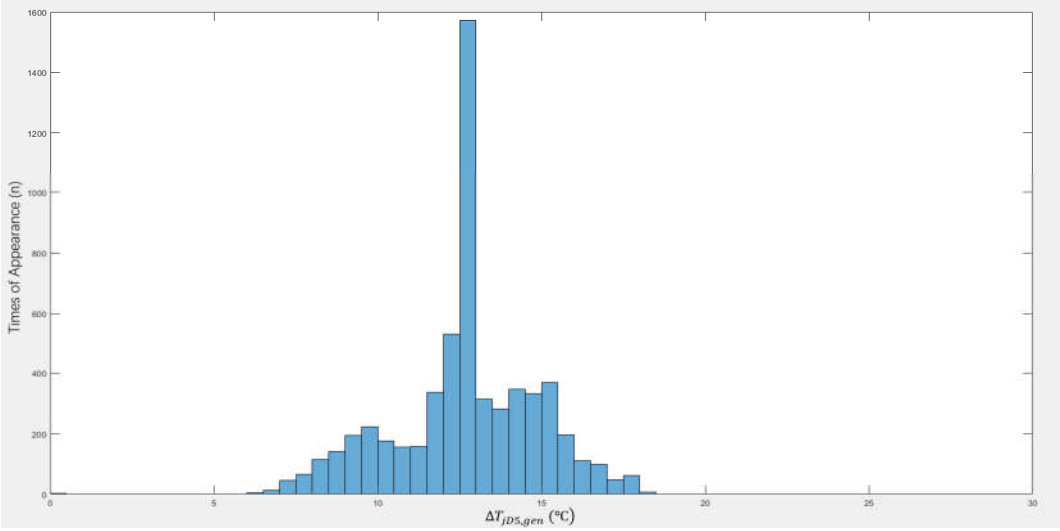

Figure 7. 8 $\Delta T_{jD5,gen}$ Distribution with 3L fs Regulation

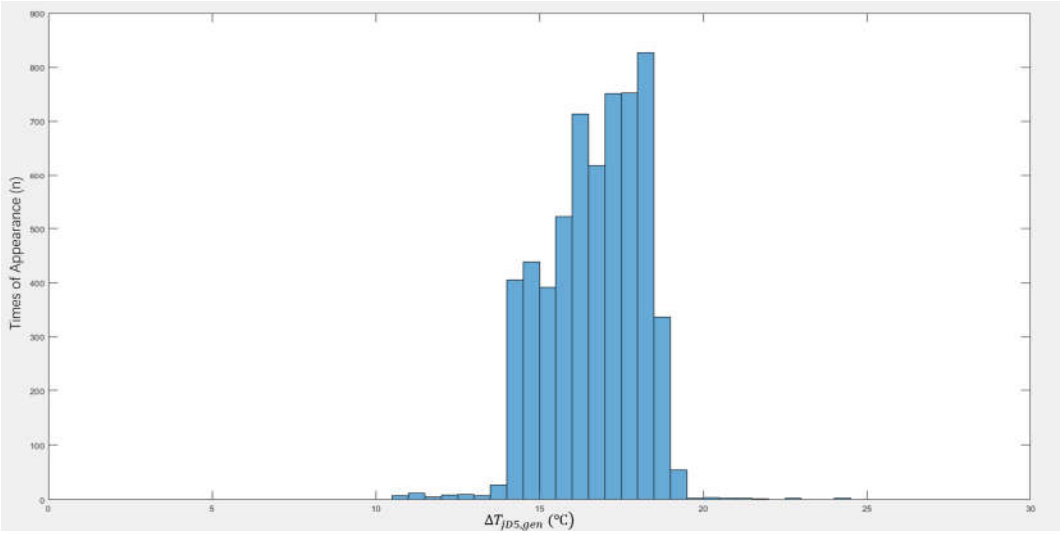

Figure 7. 9 $\Delta T_{jD5,gen}$ Distribution with 1L RC Regulation

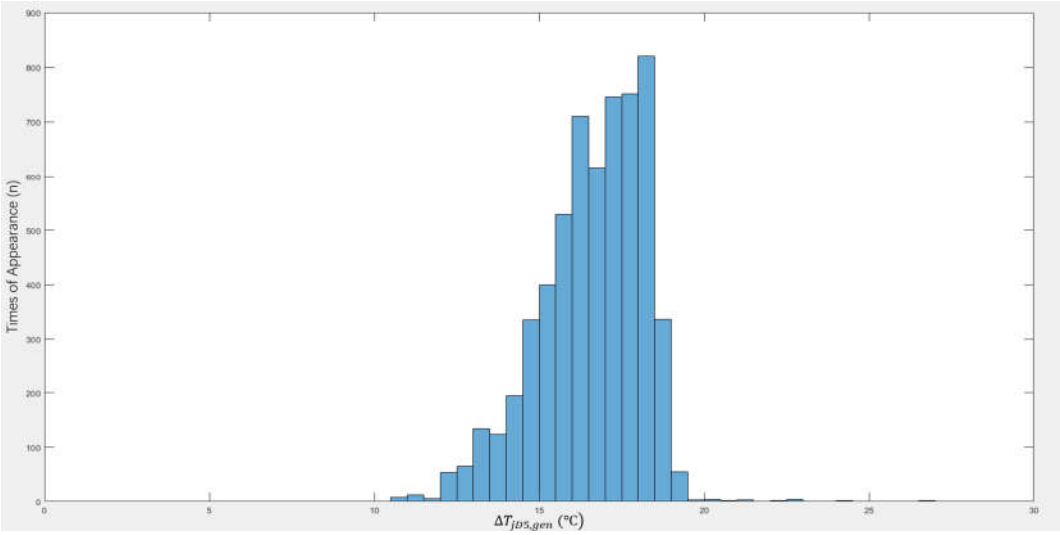

Figure 7. 10 $\Delta T_{jD5,gen}$ Distribution with 2L RC Regulation

To make the comparison of the effects achieved from different regulations become more intuitive, this thesis decided to contrast the mean values of ΔT_j during each simulation, which can be calculated by equation (7-2).

$$\Delta T_{j,mean} = \frac{\sum(\Delta T_j \cdot N_{cycle})}{\sum cycles} \tag{7-2}$$

where N_{cycle} is the thermal cycle corresponding to each ΔT_j and $\sum cycles$ is the total number of thermal cycles. The results of ΔT_j are shown in table 7.1 and table 7.2.

Different Regulation Methods Used at Grid Side	$\Delta T_{j,mean}$ on D5(°C)
Without Regulation	8.2133
2L fs Regulation	9.4952
3L fs Regulation	6.6434
1L PF Regulation	8.7396
2L PF Regulation	7.5644

Table 7. 1 $\Delta T_{jmeanD5,grid}$ with Different Regulation Methods

Different Regulation Methods Used at Generator Side	$\Delta T_{j,mean}$ on D5(℃)
Without Regulation	15.2219
2L fs Regulation	17.4075
3L fs Regulation	12.7188
1L RC Regulation	16.6889
2L RC Regulation	16.9149

Table 7. 2 $\Delta T_{jmeanD5,gen}$ with Different Regulation Methods

Observing table 7.1 and table 7.2, some conclusions can be summarized as follows:

1, The three-level switching frequency regulation gains the best result based on ΔT_j from both side, the amplitude of thermal cycles generates the maximum extent reduction from all the control methods.

2, Compare to $\Delta T_{j,mean}$ result without regulation, the effectiveness of two-level power factor control is the second for the regulation of grid side, which is only lower than the three-level switching frequency regulation.

3, Compare to $\Delta T_{j,mean}$ result without regulation, the one generated by two-level switching frequency regulation increases, because the system selects higher level as the alternative frequency when the wind speed is low.

4, Although $\Delta T_{j,mean}$ results of the one-level reactive current regulation at both sides are raised, the occurrences of large ΔT_j are significantly reduced for sure. When it comes to the lifetime calculation, these changes may still have the function to extend the lifetime of semiconductors according to the pulse duration of each sampled ΔT_j.

In order to observe the dispersion of ΔT_j under different regulations clearer, box-plot statistic graphs are used in this thesis. Importing the column of ΔT_j generated by rain flow counting to Excel, the box-plot graphs display maximum, minimum, median, upper quartile and lower quartile of sets of data are shown in figure 7.11 and figure 7.12.

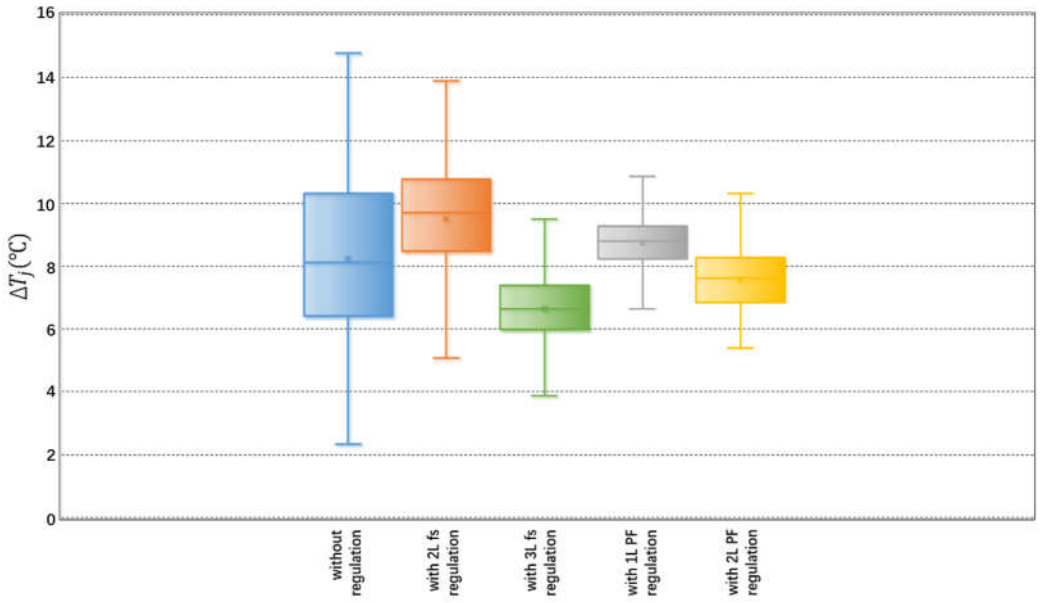

Figure 7. 11 Grid Side D5 Thermal Cycling Amplitude Distribution Based on Manually Set Wind Profile

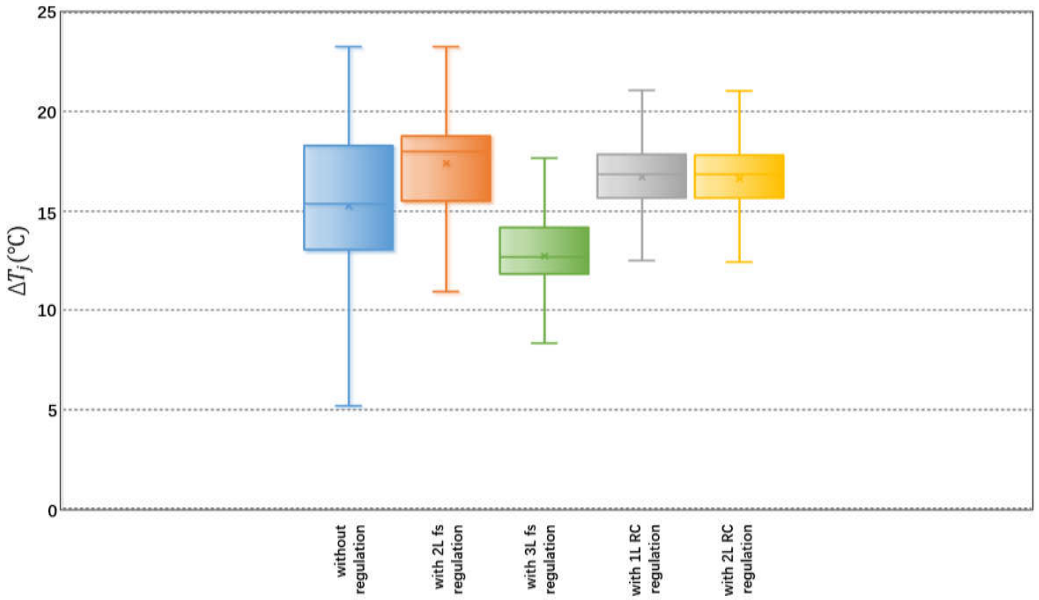

Figure 7. 12 Generator Side D5 Thermal Cycling Amplitude Distribution Based on Manually Set Wind Profile

In the above box-plot figures, the two dashes on the top and bottom edges represent the maximum and minimum values, the upper and lower sides of the rectangle indicate the first quartile (Q1) and the third quartile (Q3) respectively, the line in the middle of rectangle represents the median (Q2), and the little cross is the mean value of thermal cycle amplitudes. Q1, Q2 and Q3 are equal to the amounts of 25%, 50% and 75% respectively after all the sampled values are arranged from small to large, so the closer the distance between these values is, the more concentrated ΔT_j distribution it achieves. Observing figure 7.11 and 7.12, some conclusions can be summarized as follows:

1, Compare to the result the system operated without regulation, all the applied active control methods are effective to shorten the gap between the maximum ΔT_j and minimum ΔT_j.

2, For the grid side, from the perspective of $\Delta T_{j,mean}$, the three-level switching frequency regulation is the most effective one. However, from the view point of the concentrated ΔT_j distribution, one-level power factor regulation has narrower ΔT_j distribution.

3, For the generator side, the three-level switching frequency regulation is superior to all other methods. The difference between one-level and two-level reactive current regulations is not very visible.

To evaluate the impact of those active control methods on the lifetime of semiconductors, it will be further quantified in conjunction with the $T_{j,mean}$ brought by each regulation.

7.2 Mean Junction Temperature Analysis

Reading the column related to junction temperature to Excel after rain flow counting, the results of $T_{j,mean}$ with different active control methods are shown in table 7.3 and table 7.4, and the comprehensive $T_{j,mean}$ distribution of both grid side and generator side is shown in figure 7.13.

Different Regulation Methods Used at Grid Side	$T_{j,mean}$ on D5(°C)
Without Regulation	75.2438
2L fs Regulation	80.9740
3L fs Regulation	68.2795
1L PF Regulation	77.3284
2L PF Regulation	72.4651

Table 7. 3 $T_{jmeanD5,grid}$ with Different Regulation Methods

Different Regulation Methods Used at Generator Side	$T_{j,mean}$ on D5(°C)
Without Regulation	87.0994
2L fs Regulation	94.4353
3L fs Regulation	79.1717
1L RC Regulation	91.6377
2L RC Regulation	90.8642

Table 7. 4 $T_{jmeanD5,gen}$ with Different Regulation Methods

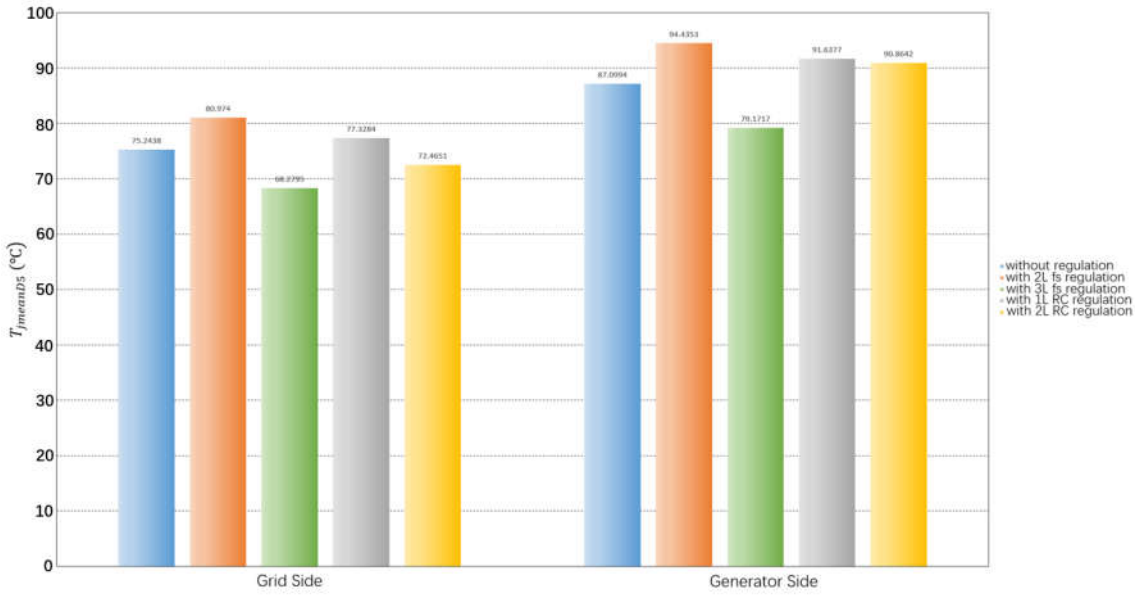

Figure 7. 13 Mean Junction Temperature Distribution of D5 Based on Manually Set Wind Profile

Observing the data illustrated above, the results can be summarized as follows:

1, The system applied three-level switching frequency regulation owns the lowest T_{jmean} from both grid side and generator side.

2, For the grid side, the effect of two-level reactive current regulation is second only to the three-level switching frequency regulation.

3, Two-level switching frequency regulation causes higher T_{jmean} compared to it in the system without any control, because a high fs is applied to rise up T_j at those low wind speed moments, and the overall average junction temperature naturally increases.

4, For the generator side, the reactive current is injected when the wind speed is low, so the larger current causes larger losses, and the overall mean junction temperature rises.

The next step is to substitute the results of the obtained thermal cycling amplitudes and junction temperature into the lifetime calculation formula, and the N_f brought by different active control methods can be quantified.

7.3 Lifetime Results

Substituting the results of ΔT_j and T_j generated by the rain flow counting into equation (7-1), and the pulse duration of each thermal cycle can be calculated by the time of start point subtracting the time of end point. However, when the pulse duration of one thermal cycle is longer than 15s, t_{on} can be fixed at 15s, because it only affects lifetime linearly. The Matlab code to calculate lifetime can be found in appendix 5. Table 7.5 and table 7.6 demonstrate different lifetime of D5 from both sides based on different active control methods.

Different Regulation Methods Used at Grid Side	The Number of Cycles to failure N_f on D5
Without Regulation	1.72×10^9
2L fs Regulation	1.71×10^9
3L fs Regulation	7.43×10^9
1L PF Regulation	3.73×10^9
2L PF Regulation	5.84×10^9

Table 7. 5 Grid Side N_f Results Based on Manually Set Wind Profile

Different Regulation Methods Used at Generator Side	The Number of Cycles to failure N_f on D5
Without Regulation	1.92×10^8
2L fs Regulation	1.11×10^8
3L fs Regulation	4.02×10^8
1L RC Regulation	2.07×10^8
2L RC Regulation	2.06×10^8

Table 7. 6 Generator Side N_f Results Based on Manually Set Wind Profile

Observing table 7.5 and 7.6, the three-level switching frequency regulation extends the lifetime of semiconductors to the utmost extent. The reactive current regulation that is applied at both sides also give positive results of the lifetime improvement. However, these results are based on the manually set wind profile which is shown in figure 3.10, the obviously varied wind speed causes a lot of large thermal cycle amplitudes. Since reactive current control can effectively reduce ΔT_j by fixing $T_{j,mean}$ at a relatively high degree, for a system consists of many large thermal cycle amplitudes that mainly influence semiconductor lifetime, the regulation results can be positive. If a realistic wind profile with longer operation time is applied, the reactive current regulation results maybe show differently.

7.4 Results on Statistic Wind Profile

For sake of evaluating the performance of different active control methods, a wind profile closer to the reality is reconstructed. In the wind profile construction, the seasonally averaged wind speed 10m/s is assumed based on the real time wind speed data in the Netherlands. According to this averaged wind speed and Weibull distribution, the wind profile is reconstructed as figure 7.14 shown. Based on the results demonstrated in table 7.5 and table 7.6, the control methods that give relatively better lifetime improvement are used for retesting, and the simulation time is extended to 600s.

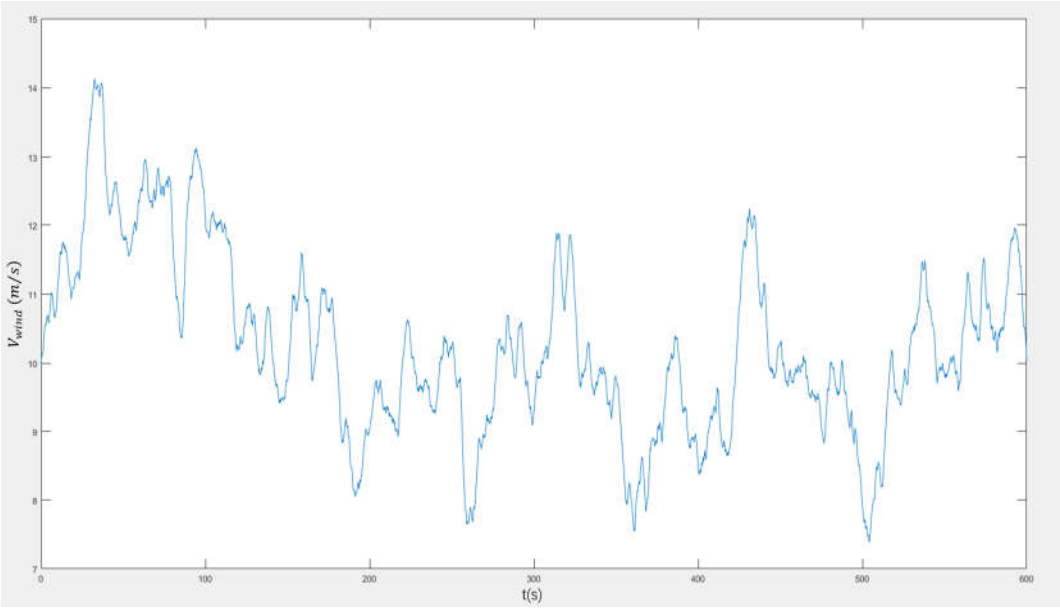

Figure 7. 14 Wind Profile from Statistics

The selected control methods are three-level switching frequency regulation and two-level power factor regulation at grid side; three-level switching frequency regulation and one-level reactive current regulation at generator side. The thermal cycling amplitude distributions of D5 from both sides with different control methods can be found in figures 7.15 and 7.16. The comprehensive $T_{j,mean}$ distribution is shown in figure 7.17. Table 7.7 and table 7.8 demonstrate different lifetime of D5 from both sides based on different active control methods.

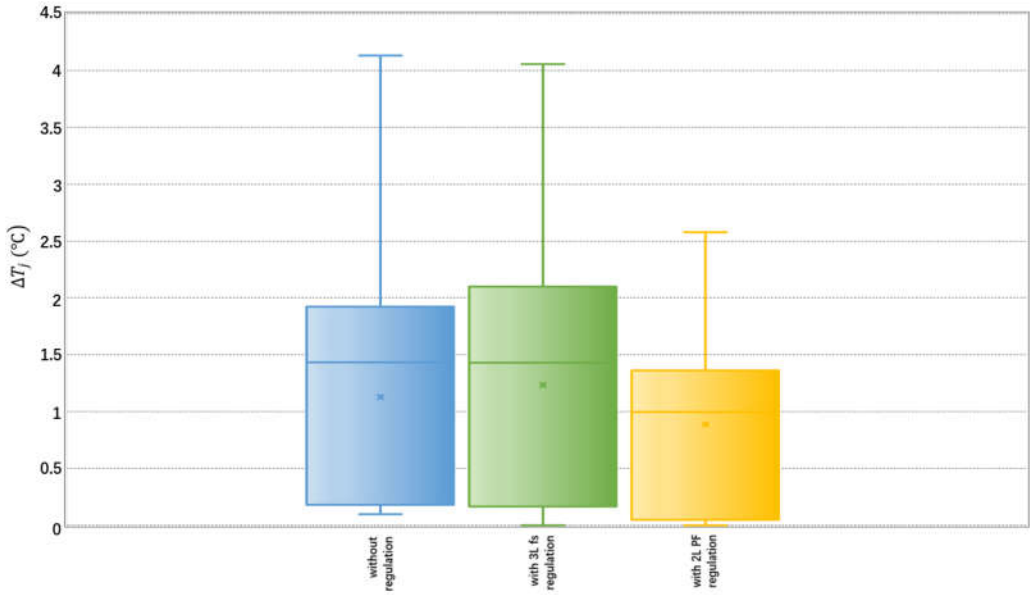

Figure 7. 15 Grid Side D5 Thermal Cycling Amplitude Distribution

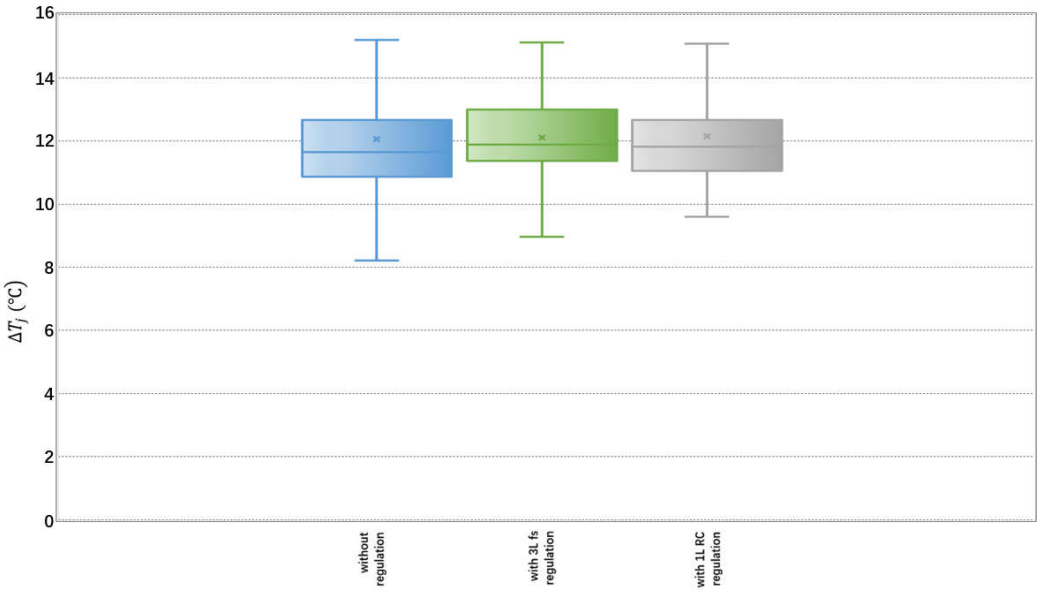

Figure 7. 16 Generator Side D5 Thermal Cycling Amplitude Distribution

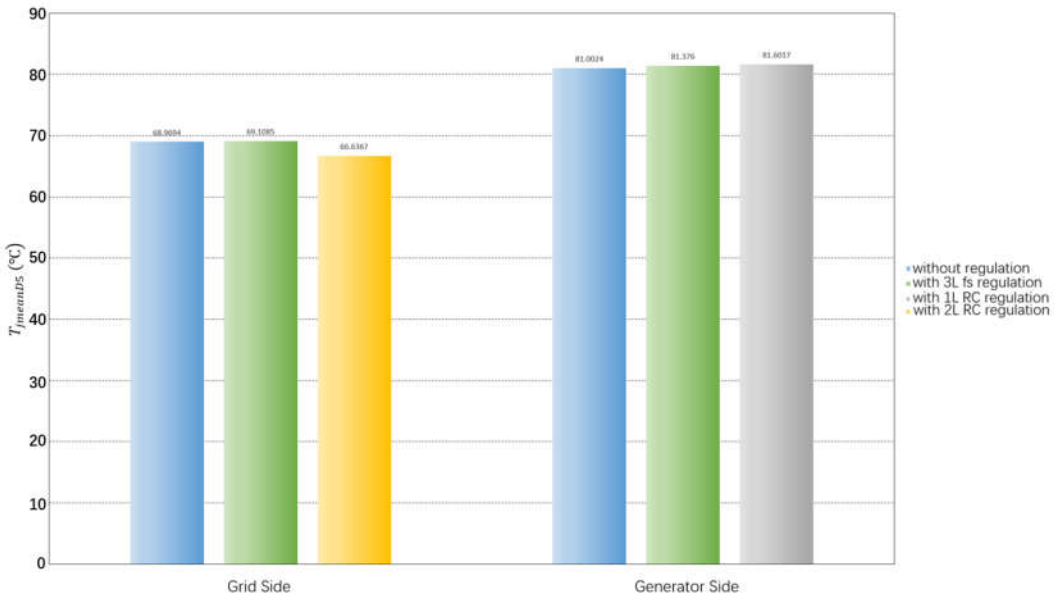

Figure 7. 17 Mean Junction Temperature Distribution of D5

Different Regulation Methods Used at Grid Side	The Number of Cycles to failure N_f on D5
Without Regulation	2.69×10^9
3L fs Regulation	3.05×10^9
2L PF Regulation	6.17×10^9

Table 7. 7 Grid Side N_f Results

Different Regulation Methods Used at Generator Side	The Number of Cycles to failure N_f on D5
Without Regulation	8.68×10^8
3L fs Regulation	10.8×10^8
1L RC Regulation	8.53×10^8

Table 7. 8 Generator Side N_f Results

It can be seen, at the grid side, two-level reactive current control improves semiconductor lifetime more effectively than switching frequency control, which is in contrast to the results obtained by applying manually set wind profile. The reasons can be concluded as follows:

1, In the manually set wind profile, the extreme changes in wind speed cause more large thermal cycle amplitudes, three-level switching frequency control works best because it reduces ΔT_j and $T_{j,mean}$ at the same time.

2, When the realistic wind profile is applied, the variation of wind speed is much smoother than before, and there are not so many large thermal cycle amplitudes. According to [58], ΔT_j within 3K does not affect lifetime, therefore, the loop width in the hysteresis control for switching frequency regulation is selected to be ± 3℃. Such a setting makes the system recognize the switching frequency shifting signal less sensitive than the recognition under extreme wind speed variation. The system keeps operating at one frequency level for a longer time, so the lifetime improvement is significantly lower than before. However, N_f achieved by three-level switching frequency regulation is still 13.38% better than the uncontrolled system.

3, The power factor of grid side can be regulated at any time depending on the wind speed variation, so it is more effective in reducing thermal cycle amplitudes when the wind profile is not extreme. Therefore, at grid side, N_f obtained by two-level power factor regulation is around two times better than the three-level switching frequency regulated system.

At the generator side, instead of improving, the one-level reactive current even shortens the lifetime of semiconductor in 1.73%. The reasons can be concluded as follows:

1, The d-axis current is fixed at zero when the system operates without control, which means that the injected I_d can only make the total current larger, and semiconductors generate more losses, so the mean junction temperature is higher.

2, Under the extreme wind speed conditions, the reactive current control improves lifetime slightly because it can effectively shorten those large thermal cycle amplitudes. When ΔT_j of a system is relatively small and its impact on lifetime is not so evident, the reactive current regulation cannot effectively play the advantage of reducing large thermal cycle amplitudes anymore.

3, With the realistic wind profile, the reactive control that reduces ΔT_j by increasing $T_{j,mean}$ is not applicable to generator side. However, it can still improve the thermal performance properly under bad weather conditions.

7.5 Summery of Lifetime Results

One control method applied to different wind profiles can give different extents of lifetime improvement. When the wind speed changes dramatically, three-level switching frequency regulation is the most effective control to increase semiconductor lifetime at both grid and generator sides. When the wind speed changes relatively tender, two-level reactive current control becomes the most recommended method at grid side, and three-level switching frequency regulation keeps the most effective control result at generator side.

As a consequence, three-level switching frequency regulation is very applicable for generator side control, therefore, the selection of grid side control method should be determined based on actual environment. For example, for those wind turbines established on the ocean and operates under extreme wind conditions, three-level switching frequency control is worth to recommend; for wind turbines built on the mainland and usually works under gentle wind conditions, two-level reactive current regulation could be a better choice.

8. Conclusion and Recommendation

8.1 Conclusion

This thesis analyses active control methods to improve converter reliability in wind turbines, and it completes the following contents:

1, By introducing the principle and implementation of each regulation method, the overview of existing electrical parameter-based controls to improve lifetime is completed. In addition, each control affects whether switching loss or conduction loss is explained.

2, Switching frequency regulation and reactive current regulation are modelled in the wind generator system with 10MW PMDD generator and 3L-NPC converters. The semiconductor thermal performance they bring is also analyzed from three aspects: thermal loss, maximum thermal cycling amplitude and mean junction temperature.

3, By applying a manually set wind profile and a statistical wind profile separately to the system, different control methods based on the lifetime estimation from thermal cycling are analyzed and compared.

Besides, the implementation of the thermal model of power electronics is described in detail. The approaches to calculate thermal losses are discussed. By comparing different semiconductor thermal performance obtained from three modulations, FTPWM is selected as the modulation strategy for both grid and generator sides.

As a consequence, for grid side, both three-level switching frequency regulation and two-level reactive current regulation are applicable, and the control method selection can be determined based on actual environment. For generator side, three-level switching frequency regulation is recommended.

8.2 Future Work Recommendations

8.2.1 Research on Gate Voltage Regulation

As it mentioned in section 2.5, two 3D lookup tables should be established for the implementation of gate voltage regulation. The relation between T_j, I_c and V_g should be involved in the lookup table to control conduction loss, and the relation between T_j, E_{on} and V_g should be contained in the lookup table to control turn-on switching loss.

In the converter module datasheet [8], during the conduction process, one graph fixes T_j at 150℃ and gives the corresponding curves between I_c and V_{ce} under six different values of V_g. The other graph fixes V_{ce} at 20V and shows the corresponding curves between I_c and V_g under three different values of T_j, which are 25℃, 125℃ and 150℃. In theory, the lookup table based on T_j, I_c and V_g can be established based on the above data. However, the junction temperature operation area of semiconductors in this system is generally from 40℃ to 110℃.

Although the required data can be approximated by a roughly linear translation of the curves, the accuracy of the regulation results should be considered as an issue to aware.

As for the switch-on process, with the constant $V_g = \pm 15V$, the relations between E_{on} and I_c are given under $T_j = 125℃$ and $T_j = 150℃$ separately. There is no other reference curve for different values of V_g, the required data even cannot be estimated by linear translation.

As a consequence, in order to implement the gate voltage control in future works, it is necessary to build up an applicable datasheet through physical experiment tests.

8.2.2 Lifetime Calculation Procedure Based on Long Duration Profile

It is impossible to use full year wind profile with high resolution to calculate the lifetime with current model because of the simulation speed is slow. One alternative solution is proposed in [21], the comprehensive lifetime calculation involves two different time scales, which can be found in figure 8.1 [21]. The short duration applies a stochastic 10 minutes wind profile combined with a dynamic model. The long duration uses the annual wind profile with wind speed averaged over 10 minutes period together with a steady state model to achieve a temperature profile.

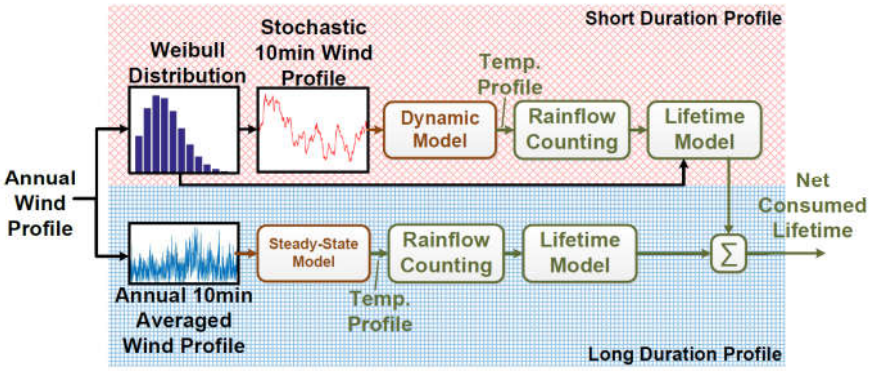

Figure 8. 1 Lifetime Calculation Procedure [21]

Since it is complicated to modify a dynamic model to a steady-state model, the lifetime calculation based on long duration profile is not executed in this thesis. Nevertheless, for future studies, if a more comprehensive lifetime calculation is desired, long duration profile is necessary to be taken into consideration.

Appendix

Appendix 1

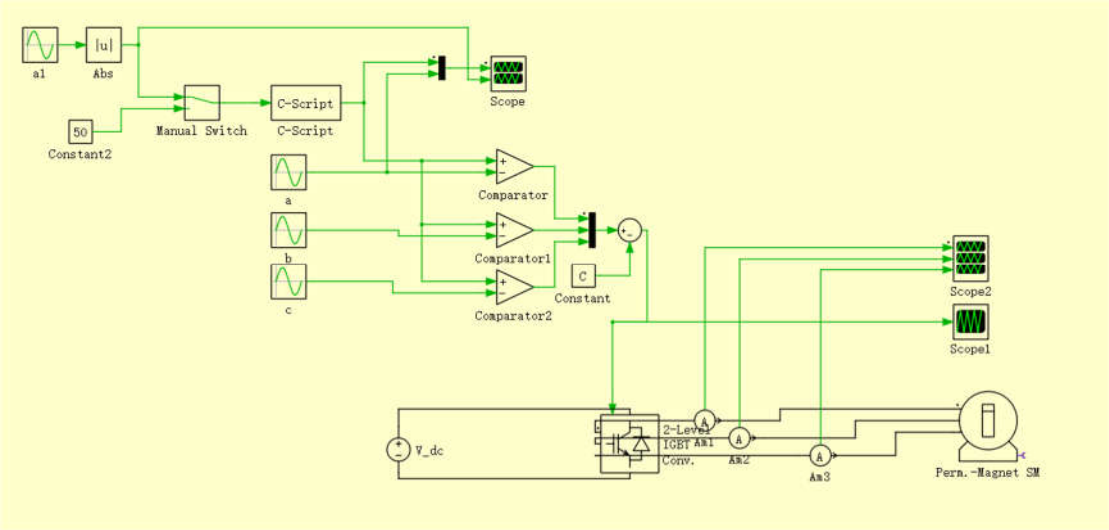

Figure A1. 1 Constant fs VS Changing fs Simulation Model

To avoid algebraic loop issue, C-script is used to implement an integrator. Therefore, the carrier waveform is completed. The input signal a1 represents that the switching frequency changes as a sinusoidal type. The comparison between carrier and three-phase modulator can be implemented by applying comparators. The bias there is used to make bipolar signals. In order to let the verification process simple, a two-level inverter module is applied, connect it with DC bus and a PM machine, the simulation model for the comparison of constant switching frequency and changing switching frequency is implemented.

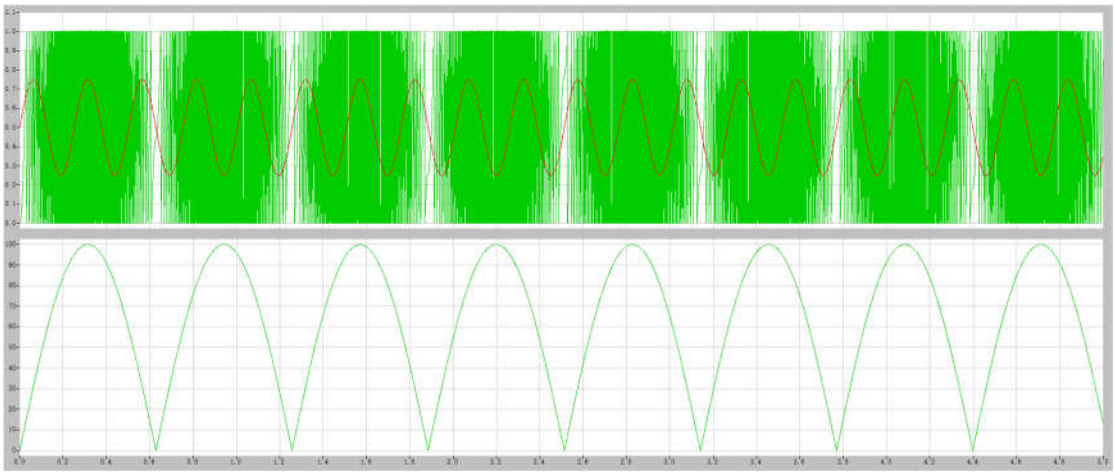

Figure A1. 2 Waveform of Changing Switching Frequency

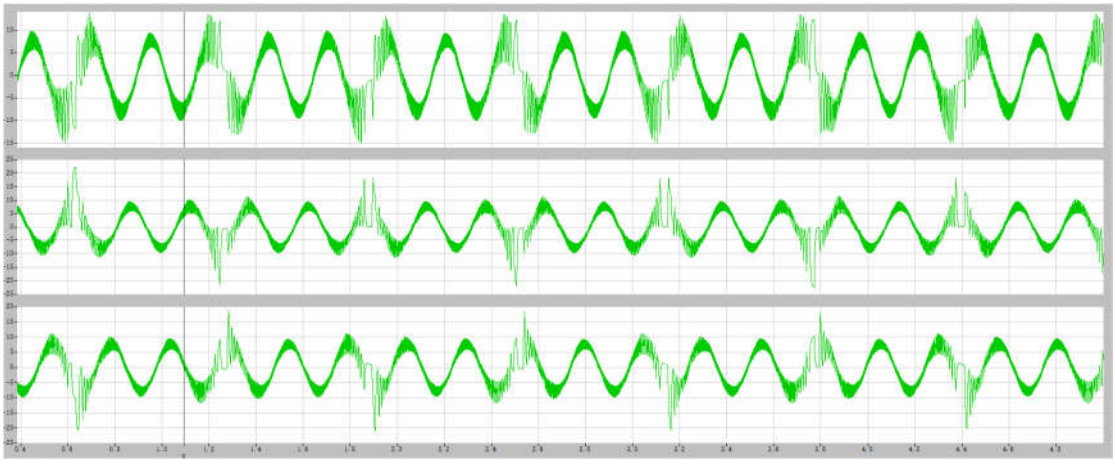

Figure A1. 3 Three-phase Current Generated by Changing Switching Frequency

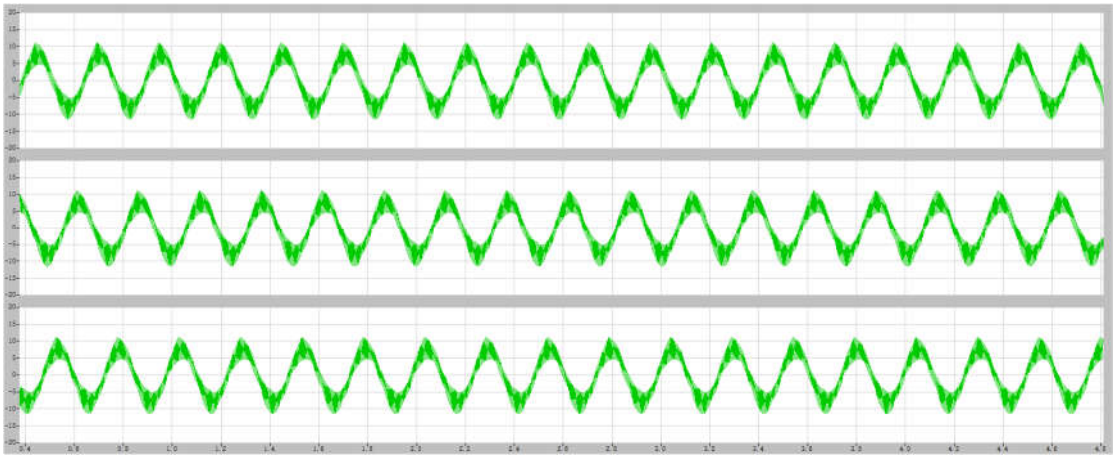

Figure A1. 4 Three-phase Current Generated by Constant Switching Frequency

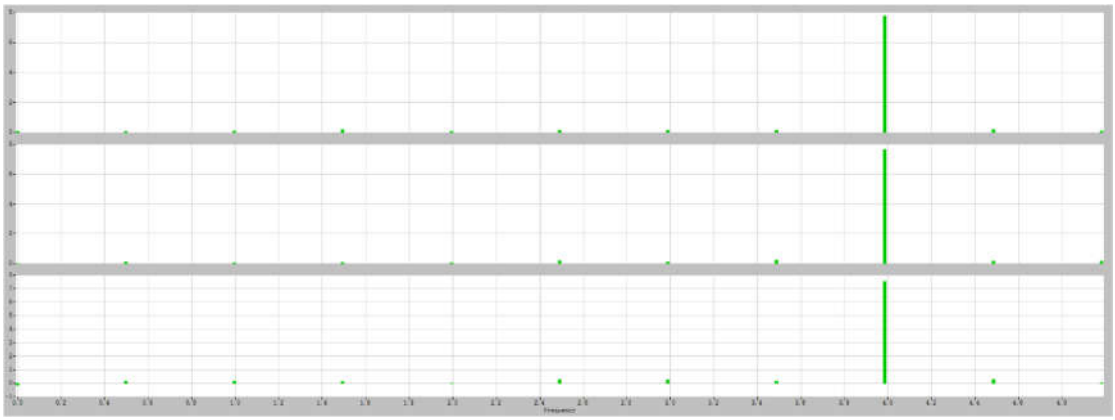

Figure A1. 5 FFT Generated by Changing Switching Frequency

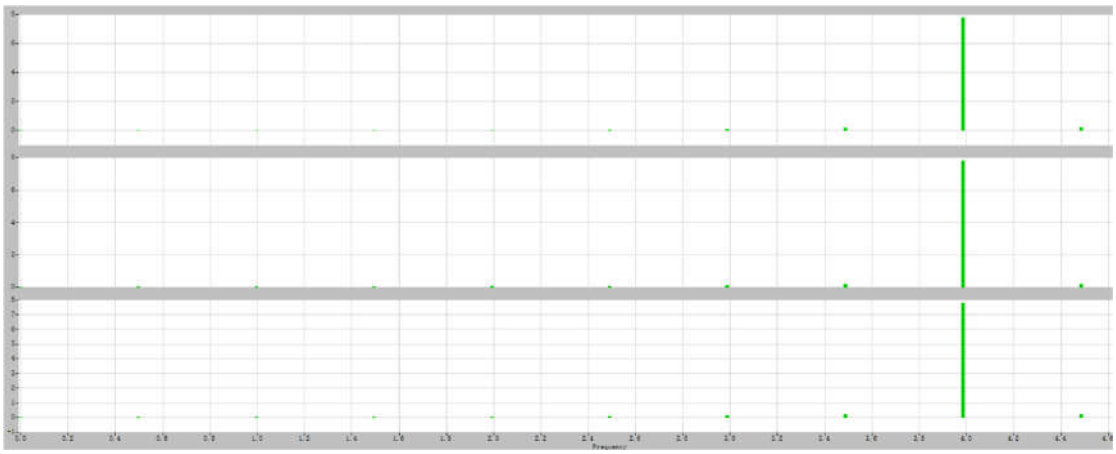

Figure A1. 6 FFT Generated by Constant Switching Frequency

Appendix 2

```
%%%%Target: During each time operation, it can get graphs of different wind speeds and temperatures under fixed PF conditions.
%%%%Modify PF before each operation, it gets few graphs, and then merge them.
    wind_speed_set1=4;%%Setting the start wind speed;
    WS_cons=10;%%Setting the desired wind speed point. If speed_set1=4 and cons=12, the wind speed point starts at 4, 4.5.6.7... up to 16;

    PF_set1=0.5;%%The initial PF value has been converted and the PF setting range is 0 to 1.
    PF_cons=10;%%Setting how many PF points are needed. If set1=0.5 and cons=10, then PF's points are 0.5, 0.55, 0.6... up to 1;

    simu_time=10;%%The simulation duration is generally 10s when the system reaches stable environment;
for j=1:1:PF_cons
PF_set=PF_set1+j*(1-PF_set1)/PF_cons;

for i=1:1:WS_cons    %%Setting range;
    wind_speed_set=wind_speed_set1+i;%%Wind speed setting;
    wind_speed(i)=wind_speed_set;
    sim('gridside_PF_control',simu_time);
    TjD5_temp(i)=mean(T_jD5_temp_avg(:,2));
end
figure (1)
hold on
plot(wind_speed,TjD5_temp);
xlabel('Vwind(m/s)');
ylabel('Tj_meanD5,grid(C)');
hold off
end
```

Appendix 3

```
  %%%%setting grid side PF&Vwind
  PF_set=0.9;
   wind_speed_set1=4;%%Setting the start wind speed;
   WS_cons=10;%%Setting the desired wind speed point. If speed_set1=4 and cons=12, the wind speed point starts at 4, 4.5.6.7... up to 16;

    Id_set1=0;%%The initial Id value has been converted as 0.
    Id_interval=-200;%%Setting the distance between each Id point;
    Id_cons=10;%%Setting the desired Id point. If Id_set1=0 and cons=10, the Id point starts at 0,-300,-600... down to -3000;

    counter=0;
    simu_time=10;%%The simulation duration is generally 10s when the system reaches stable environment;


for j=Id_set1:Id_interval:(Id_cons*Id_interval+Id_set1)    %%Setting range;
    counter=counter+1;
    Id_set=j;
    Id(counter)=Id_set;

for i=1:WS_cons    %%Setting range;
    wind_speed_set=wind_speed_set1+i;%%Wind speed setting;
    wind_speed(i,1)=wind_speed_set;
    sim(' genside_Id_control ',simu_time);
    gen_T_jD5_temp(i)=mean(gen_T_jD5_temp_avg(:,2));
    end
figure (1)
hold on
plot(wind_speed,gen_T_jD5_temp);
xlabel('Vwind(m/s)');
ylabel('Tj_meanD5,gen(C)');
hold off
end
```

Appendix 4

```
[c,hist,edges,rmm,idx] = rainflow(gen_T_jD5.signals.values);
T = array2table(c,'VariableNames',{'Count','Range','Mean','Start','End'});
delta_Tj_sum = 0;
cycle_sum = 0;
```

```
histogram('BinEdges',edges','BinCounts',sum(hist,2));
xlabel('Stress Range');
ylabel('Cycle Counts');
for i = 1:length(c)
delta_Tj_sum = c(i,2)*c(i,1)+delta_Tj_sum;
cycle_sum = c(i,1)+cycle_sum;
end
delta_Tj_mean = delta_Tj_sum/cycle_sum;
```

Appendix 5

```
Nfk = zeros(length(c),1);
N_loss = 0;
for i = 1:length(c)
    if (gen_T_jD5.time(c(i,5))-gen_T_jD5.time(c(i,4))) > 15
    Nfk(i,1) = 9.34e14*(c(i,2)^(-4.416))*((15)^(-0.463))*((10)^(-0.716))*((33)^(-
0.761))*((500)^(-0.5))*(exp(1285/(c(i,3)+273)));
    else
    Nfk(i,1) = 9.34e14*(c(i,2)^(-4.416))*((gen_T_jD5.time(c(i,5))-gen_T_jD5.time(c(i,4)))^(-
0.463))*((10)^(-0.716))*((33)^(-0.761))*((500)^(-0.5))*(exp(1285/(c(i,3)+273)));
    end
    N_loss = N_loss+(c(i,1)/Nfk(i,1));
end
N_total = sum(c(:,1));
Nf = N_total/N_loss;
```

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