Predictive Mitigation of Short Term Voltage Instability Using a Faster Than Real-Time Digital Replica

Joseph, Arun; Cvetkovic, Milos; Palensky, Peter

DOI
10.1109/ISGTEurope.2018.8571803

Publication date
2018

Document Version
Final published version

Published in
2018 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe)

Citation (APA)
Joseph, A., Cvetkovic, M., & Palensky, P. (2018). Predictive Mitigation of Short Term Voltage Instability Using a Faster Than Real-Time Digital Replica. In *2018 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe): Conference Proceedings* (pp. 1-6). IEEE. https://doi.org/10.1109/ISGTEurope.2018.8571803

Predictive Mitigation of Short Term Voltage Instability Using a Faster Than Real-Time Digital Replica

Arun Joseph, Miloš Cvetković and Peter Palensky
Department of Electrical Sustainable Energy
Delft University of Technology
The Netherlands
Email: arun.joseph@tudelft.nl

***Abstract*—Predictive mitigation of undesired events has long been seen as a supportive complement to corrective mitigation that could relax the stringent requirements on the corrective actions and increase reliability of the overall system. This article describes one such predictive measure, i.e. the use of faster than real-time simulation in detecting faults and predicting the dynamic behavior for the resilient operation of future smart grid systems. A predictive mitigation strategy is proposed for a fault induced dynamic voltage recovery (FIDVR) event. These events, although rare, are typically addressed with under voltage load shedding schemes (UVLS) which leave significant portion of load under-supplied. We show that, by using the digital faster than real-time replica, the minimal level of UVLS can be determined on-the fly as the event develops while ensuring only the minimal amount of load shed.**

***Index Terms*—Faster than Real-Time Simulation, Fault Induced Dynamic Voltage Recovery (FIDVR), Composite Load Model (CLM), Under Voltage Load Shedding (UVLS).**

I. Introduction

Smart grids integrate physical infrastructure, information and communication technology, and market mechanisms with policy regulations and business processes. Assessing the resiliency of such a system of systems requires new methods and tools, since existing ones typically focus on one of the subsystems and their particular mathematical properties. In this work, we propose one overarching simulation-based method for real-time action in response to disturbances and faults.

This article describes the use of faster than real-time simulation for predictive mitigation of short term voltage stability issues, in particular FIDVR, occurring in power systems. The voltage stability problems in the traditional power systems are monitored using information from protection devices and other traditional supervisory control and data acquisition (SCADA) elements. The time scale of this measurement stream is in the order of a few seconds up to several minutes. Modern wide area protection and control (WAMPAC) systems offer much quicker time scales and are capable of detecting the catastrophic cascading effects associated with some faults that may lead to system black outs. They rely on the control room operator knowledge and skills to solve this problem as it develops and before it escalates. In this article the described problem is addressed in a smart grid paradigm, where we expect the electricity grid to develop more towards a self-healing grid with automated fault detection and response.

In this paper we focus particularly on the short term voltage instability problems such as the fault induced dynamic voltage recovery (FIDVR). The main characteristic of these FIDVR phenomena is that they occur in a time frame of few seconds (most often less than 30 seconds) which is sufficiently long for automated fault prediction and mitigation to take place. The FIDVR problem has been encountered by many power utilities throughout the world [1]–[4] mostly during the mid summer season with increased penetration of air conditioner (AC) loads in the power system. An FIDVR event is manifested as a low voltage sag at the load bus due to the clearance of a severe fault, like a transmission line fault. This voltage sag induces a stalling behavior in the induction motors present in the system. The stalling behavior results in increased reactive power consumption by these induction motor loads. This increased consumption is about 5-8 times the normal reactive power requirement and it leads to a delayed voltage recovery. The delayed voltage recovery may cause rapid tripping of other loads and even lead to collapse of an entire area of a power system.

The mitigation strategies for such delayed voltage recovery problems can be divided into categories such as supply side control solutions [6]–[8] and demand side control solutions [9]–[13]. The supply side control solutions focus on the mitigation of FIDVR by providing the required dynamic reactive power support from adequate supply sources. To implement this mitigation strategy system operators conduct optimal placement [6] of reactive power sources such as dynamic var reserve of local generators, shunt capacitors or advanced dynamic var compensator's to provide required reactive power support to the system. However, the wide-spread installations of such big systems are not economically viable as their cost increases with the size and with the reactive power capacity they are to provide. In addition, these are implemented in the planning and development stages of the power system. Hence, when it comes to real-time mitigation of the FIDVR event during the system operation, only a few methods exist in the literature (e.g. dynamic control of distributed generators like PV systems [7]).

On the other hand, demand side control solutions rely on adequate shedding of loads to provide the dynamic reactive power support. Under voltage load shedding (UVLS) [10] is a widely used method in this aspect. Many variants of under voltage load shedding have been proposed in the literature over the past few years [10] and can be classified in terms of features as centralized [11], [12] or decentralized [9], static or dynamic, closed or open loop, algorithmic rule based or decision based. Under all the features considered the main focus of an intelligent UVLS scheme is to shed the lowest possible amount of load. For this purpose, it is crucial to decide on the key aspects such as time, amount and location of load shedding to be done for a particular FIDVR phenomena happening.

The exact modeling of a system plays a crucial role in the analysis of the system behavior during an FIDVR. The models of load dynamics are especially important to accurately capture the events. These models can be used within the time domain simulations to replicate or to predict time-domain response of voltages and currents during the event. The period of concern for FIDVR is in the order of several seconds, and time domain simulation can be fast enough to capture the system dynamics during the event. In-order to develop a better UVLS scheme for the mitigation of FIDVR event, it is of utmost importance to use accurate models and to exactly capture the system dynamics in fast time domain simulations.

In this paper we propose the use of a digital replica of a power system that can accurately and efficiently model the system dynamics and predict the FIDVR event. Our solution relies on the ultra-fast time domain simulation of an accurate system model. Many recent literatures [18], [19] have shown the possibility of having faster than real-time dynamic simulations. The present work uses python API for PowerFactory software for having faster than real-time capability. The high level of details that can be achieved using the PowerFactory models for system simulation allow us to accurately describe the FIDVR event propagation and ultra fast simulation allows us to take action fast enough to prevent possible damage from the FIDVR event.

The rest of the article is divided into five main sections. Section II gives the basic description of the faster than real-time digital replica used for the present study. Section III explains the modeling of FIVDR event and UVLS scheme for a test system developed. Section IV explains the simulation results and the implementation of a basic predictive algorithm. Section V concludes the paper with a discussion and future scope of the work.

II. Faster Than Real-Time Digital Replica (FTRTDR)

A faster than real-time digital replica, as shown in Fig. 1, is proposed with a Python based master algorithm that is controlling three different functional units. The first unit represents the real power system. For this purpose, we use a real-time simulation. This simulation provides the measurement data in real-time emulating the in-feed of measurements to the control room. Once the FTRTDR is deployed in the field, the intention is to swap the real-time simulation with an online stream of measurement data. The real-time simulation contains a transmission network model of a power system. This simulation provides the PMU data, i.e. voltages and currents with phase angles and frequency. The data is communicated through a TCP/IP socket connection.

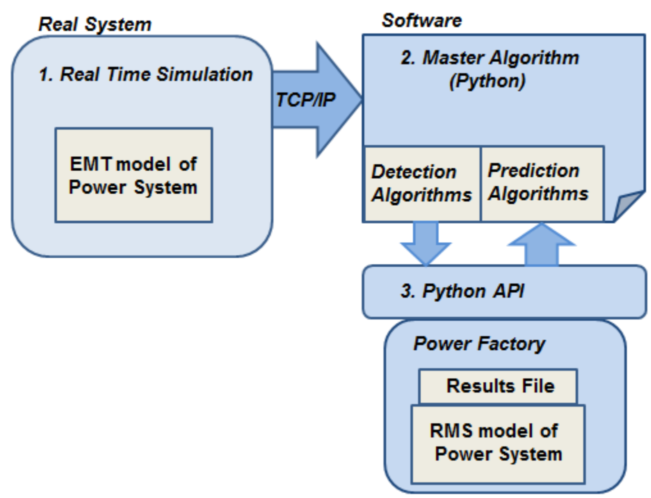

Fig. 1. Structure of FTRTDR implementation with: 1) real-time simulation, 2) master algorithm, 3) digital system replicas in PowerFactory

The second unit contains different fault detection and post-fault behavior prediction algorithms. These algorithms process the real measurement data from the first unit and the simulation results from the third unit. The main purpose of the detection algorithm is to detect any topological changes that can lead to the occurrence of an FIVDR event. The methods such as the quickest change detection (QCD) using the Cumulative Sum(CUSUM) algorithm [16] can be used for this purpose. These types of methods have a very short detection time. The prediction algorithm is activated after the detection of an FIDVR event. For the sake of clarity, we describe the prediction algorithm after the the working principles of the third unit.

The third unit consist of a faster than real-time, time domain simulation model of the same transmission network simulated using DigSilent PowerFactory. This unit provides the post-fault dynamic behavior of the system model in faster than real-time. This post-fault behavior is simulated after the fault has been detected by the second unit and the results are used by the second unit to predict where the system dynamics might converge. The simulated transmission system model is an RMS/phasor model and it is re-configurable to different post-fault scenarios. The PowerFactory software is running in *engine mode* which is capable of producing faster than real-time simulation results. The simulation results of PowerFactory model are stored as an ElmRes object [17], and can be accessed by the master algorithm for further processing. The ElmRes object consist of all the variables monitored as a result of PowerFactory model simulation and is stored in a tabular form as time series data. The number of the monitored variables plays a crucial role in the performance of the replica since the PowerFactory engine takes additional time to process and store the ElmRes object file.

The prediction algorithm consists of the following steps:

1) Start N number of parallel faster than real-time, time domain simulations,
2) Process the data in the ElmRes object and calculate the chosen metric values (e.g. the settling voltage as further explained in Section III),
3) Use this metric to choose the best corrective action (e.g. the most appropriate UVLS scheme),
4) Communicate the control actions to the equipment in the field (e.g. voltage relay).

A. Timing of the FTRTDR

The operation of the faster that real-time digital twin can be explained using the timing diagram as shown in Fig. 2. The first part of the timing diagram shows the real-time measurements obtained by the master algorithm from the real-time simulation. Period T_n is the time window with n samples of real-time data. Each data sample contains the bus voltage magnitude and phase angle values along with their time stamp. This data is processed by the fault detection part of the master algorithm as shown in the second part of the timing diagram. The T_d denotes the maximum time taken for the detection algorithm to detect a fault. Hence, a fault happening in the real-world power system at t_{f1} is detected in a time that is surely less than $t_{f1}+T_n+T_d$. At this time, the PowerFactory replica is updated with fault details and the simulation is started (as seen in the third part of the diagram). The PowerFactory model is simulated for time T_p till the next event is detected in the system (in this case at t_{f2}). If the simulation time is short enough the PowerFactory model will provide the dynamic response plots that can be used for prediction of the true state of the power system.

To validate that the PowerFactory simulations are fast enough to be used for prediction, we perform the investigation of the RMS and EMT simulation times. Table I shows the time taken for 5 second simulation of two readily available PowerFactory models with a step time of 1 milliseconds. The small step size of 1 millisecond is intentionally chosen to put more computational burden to the simulator. The time taken for each type of simulation is represented as sum of two terms. The first term denotes the time taken for initialization of the PowerFactory engine and for loading a

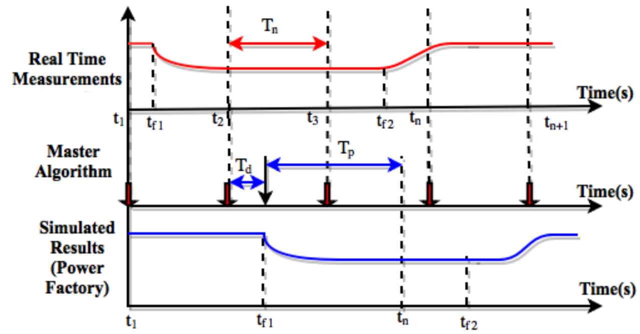

Fig. 2. Timing diagram of FTRTDR with three levels: 1) the real-time simulation (real-time measurements), 2) Detection and prediction in the master algorithm, and 3) PowerFactory replica simulation results

particular model. The second term denotes the time taken for dynamic simulation of the model. All simulation are run from a personal computer (DELL i7, 2.6 GHz(4 CPU's), 8 GB RAM).The RMS simulation model takes the total of $3.07sec$ and $4.26sec$ in these two cases, and hence, is able to provide faster than real-time simulation results. Thus, by properly selecting the factors such as type, size, step-size and the number of monitored variables of PowerFactory simulation model, we have a possibility of having a faster than real-time PowerFactory simulation. As visible from the results, by increasing the size of the power system model the simulation time will increase and the faster than real-time property will be lost. Thus, we confine our argumentation for faster than-real time performance to simplified models of the realistic power systems. A similar claim can be found in [19], where the authors claim to have faster than real-time, time domain dynamic simulations for a 17000 bus system with 30 seconds simulation possible in less than 20 seconds.

TABLE I
TIME TAKEN FOR 5 SECOND SIMULATION WITH 1 MILLISECOND STEP SIZE FOR VARIOUS POWERFACTORY MODEL SIMULATION

PowerFactory Models	RMS	EMT
9-bus system	Init = 2.82 sec Dyn = 0.25 sec	Init = 2.78 sec Dyn = 2.92 sec
39-bus system	Init = 2.88 sec Dyn = 1.38 sec	Init = 2.75 sec Dyn = 16.22 sec

III. COMPOSITE LOAD MODEL AND A UVLS SCHEME

This section describes the composite load model (CLM) used to create the FIDVR event and further explains the UVLS scheme implementation for the test system shown in section IV. The FIDVR event is primarily caused by the composite load model in response to the three-phase fault that is not cleared in less than 3 cycles. The UVLS scheme sheds the load in response to the FIDVR event. The following subsections further explain the composite load model and the UVLS scheme.

A. Composite Load model

The CLM model is created in resemblance to the model from [14] and the parameters of different components are mostly obtained from [15]. Some parameters are modified for the sake of better illustration of the FIDVR behavior.The Fig. 3 shows the composite load model implementation for the present study. Motor A and B models collectively rep-

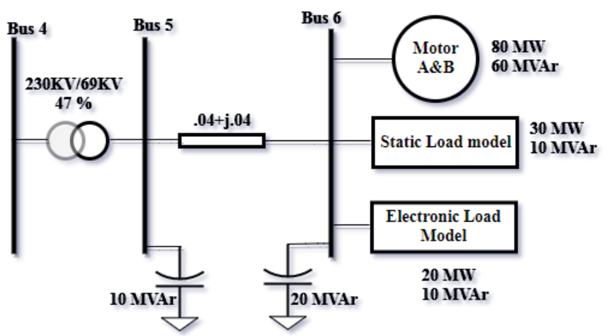

Fig. 3. Composite load model as specified in [14]

resent the load behavior of many single-phase residential air conditioning systems. They differ in the post stating behavior. The residential air conditioner loads are the major cause of the delayed voltage response and their behavior can be modeled by algebraic equations as describes in [14]. For the present study the stalling behavior is created by making these loads consume 1.65 times the nominal active power and 5 times the nominal reactive power. Fig. 4 shows the control logic implemented for motors A and B.

```
if V > 0.86 :
  P = P0
  Q = [Q0 + 6*(V−0.86)^2]
if V < 0.86 and V > V stall :
  P = [P0 + 12*(0.86−V)^3.2]
  Q = [Q0 + 11*(0.86−V) 2.5]
if V < V stall :
  P = Gstall*V*V
  Q = −Bstall*V*V
if V < Vstall and t > Tstall :
  P = P0* 1.65
  Q = Q0* 5
```

Fig. 4. Pseudocode of the control logic for Motor A and B load models

Fig. 5 shows the control logic implemented for electronic load model. Since the main focus of the present work is to create the delayed voltage response resembling an FIDVR event, we use fewer load models than in [14]. The three-phase induction motor model collectively represent by motor C and D along with PV system model and the thermal relay and contractor characteristics are not used in the present study. Both the Motor A and B load along with the electronic load are described in PowerFactory using the composite frame which gives active and reactive power set points to a constant impedance load. The static load is modeled with a simple zip load model.

```
if (V < Vmin)
      Vmin = V
if( Vmin < Vd2 )
      Vmin = Vd2
if( V < Vd2 )
  Fvl = 0.0
else if( V < Vd1 )
  if( V <= Vmin )
    Fvl = (V−Vd2)/(Vd1−Vd2)
  else
    Fvl = ((Vmin−Vd2)+frcel*(V−Vmin))/(Vd1−Vd2)
  endif
else
  if( Vmin >= Vd1 )
    Fvl = 1.0
  else
    Fvl = ((Vmin−Vd2)+frcel*(Vd1−Vmin))/(Vd1−Vd2)
  endif
endif
Pel = Fvl * Pel0
Qel = Fvl * Qel0
```

Fig. 5. Pseudocode of the control logic for electronic load model [14]

B. UVLS scheme for FIDVR event

We use the stage-based UVLS scheme to illustrate and compare the effectiveness of UVLS using FTRTDR. This type of UVLS scheme is currently implemented in decentralized relays. The UVLS scheme is modeled in the same composite frame used for the load models in PowerFactory software. Fig. 6 shows the control logic used for the stage based UVLS scheme.

```
if t > 2 and V < 0.8:
  PL  =  0.2*f*P
  QL  =  0.2*f*Q
if t > 2.5 and V < 0.8:
  PL  =  0.4*f*P
  QL  =  0.4*f*Q
if t > 3 and V < 0.8:
  PL  =  0.6*f*P
  QL  =  0.6*f*Q
if t > 3.5 and V < 0.8:
  PL  =  0.8*f*P
  QL  =  0.8*f*Q
```

Fig. 6. Pseudocode of the control logic for UVLS scheme

The variable f denotes the increment in the shed load. The value of f determines the percentage of load shed at each time interval i.e. by selecting a value of 0.5 for the variable f, $f \cdot 0.2 \cdot 100 = 10\%$ of load is shed in each time interval.

In the next section, we compare the typical stage-based UVLS scheme as described above, with the UVLS scheme using FTRTDR. FTRTDR compares different proposed stage-based UVLS schemes on-the-fly and chooses the best one for implementation in real-time.

IV. Simulation Results

The test system, shown in Fig. 7, is developed as in [3], using the PowerFactory software. Buses 3 and 4 of the test system are having static loads and the composite load model is connected to Bus 4.

A three-phase fault is applied at Bus 4 at exactly one second of the simulation time and is cleared at 0.4 seconds, which triggers the delayed voltage recovery in the test system.

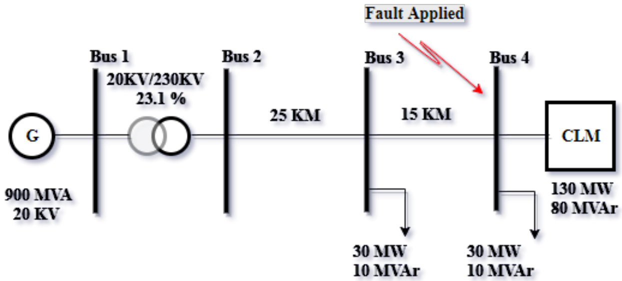

Fig. 7. Test system with an FIDVR event.

Fig. 8 illustrates the FIDVR event chosen for the present study. As seen from the figure, delayed voltage response during the FIDVR event is more predominant at Bus 6, which is the bus close to the composite load and at low voltage level.

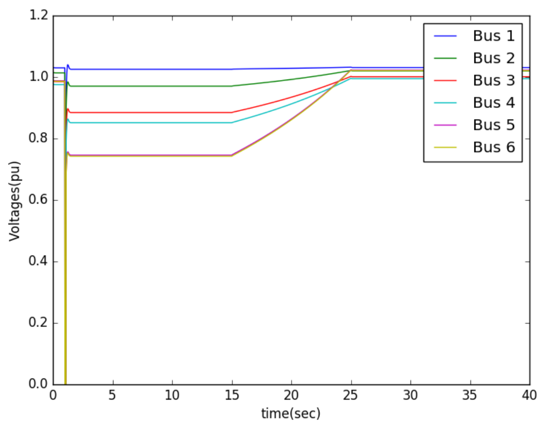

Fig. 8. FIDVR event in the test system from Fig. 7

A. Typical stage based UVLS implementation

The Fig. 9 shows the implementation of the stage based UVLS scheme on the test system with an FIDVR event explained above. Fraction f is chosen as 0.25 which corresponds to 5% of load shed. Each 0.5 seconds additional amount of 5% of load is being shed. This repeats starting from 2 seconds until 4 seconds.The voltage value of Bus 6, which is experiencing the lowest delayed voltage response, is shown Fig. 9 along with the voltage limit value. The voltage limit value is set as 0.8 pu and is used to determine effectiveness of the UVLS scheme for the mitigation of an FIDVR event. We also define settling voltage, which is the voltage value at Bus 6 after the implementation of the UVLS scheme and is further used by the prediction algorithm as a metric to identify the exact percentage of the load to be shed.

It can be noticed that a stage based UVLS scheme with 5% of load shed used in conventional relays is not able to mitigate the FIDVR event since the settling voltage is significantly lower than the voltage limit. Thus, for the effective mitigation of FIDVR event the key challenge is to identify the exact

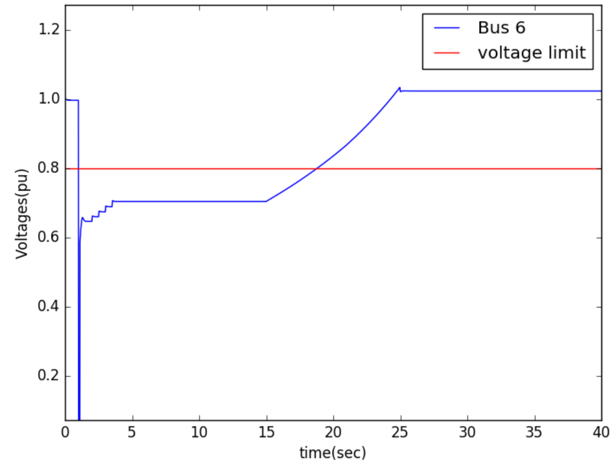

Fig. 9. Conventional stage-based UVLS scheme

amount of load to be shed using an UVLS scheme. We show that the proposed FTRTDR can successfully overcome this challenge and find such a value.

B. UVLS using FTRTDR

This section illustrates how faster than real-time, time domain simulation results can be used along with a predictive algorithm to determine the exact value of load fraction to be shed for the mitigation of the FIDVR event. Fig. 10 shows the simulation results for stage based UVLS scheme for four different fractions of load shed: 0.1, 0.3, 0.5 and 0.7.

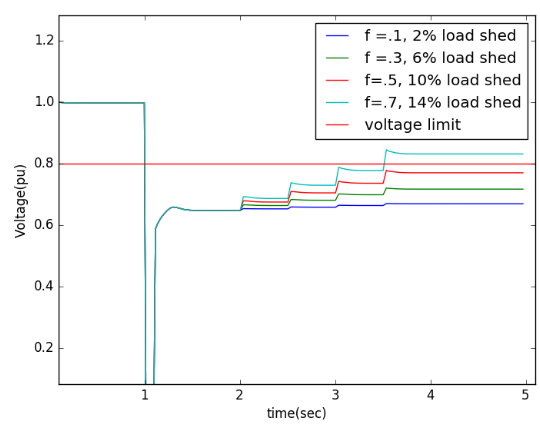

Fig. 10. UVLS scheme with different fractions of the load shed

It can be seen that for an f value of 0.7, i.e. corresponding to a 14% of load shed at intervals of 0.5 seconds, the FIDVR event is mitigated well before 5 seconds, with a settling voltage much greater than the voltage limit of 0.8 pu. As we shown in Table I, Section II, the time required to run a 5 second simulation is shorter than 5 seconds. For the test system modeled in PowerFactory with all the composite load models and UVLS scheme, the time taken for initialization of the simulator is 2.95 seconds and the time take for dynamic RMS simulation is 0.45 seconds. If the initialization of the simulator is done ahead of time, then the time taken for the dynamic simulation is short enough to be able to compute the consequences of proposed UVLS fractions and to apply the best UVLS scheme in the real system.

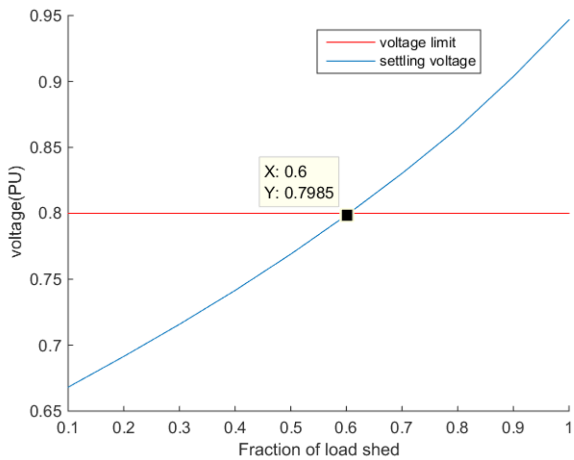

Fig. 11. Settling voltage for different load shed fractions

Fig. 11 plots the settling voltage for different load shed fractions. In this case, the load shed fraction f is varied from 0.1 to 1 with the step of 0.1. It can be found that the lowest possible value of the load shed corresponds to the point where the settling voltage curve intersect the limit voltage of 0.8 pu. This point happens for $f = 0.6$, i.e. a minimum of 12% of load shed is required for the mitigation of this FIDVR event.

For this analysis we use 10 different values of the load shed fraction f. The simulation with each of the fractions would be ran as a different digital replica. A fewer number of digital replicas could also be used, but the resolution of the analysis would be worse. In this way, a simple predictive algorithm can be implemented to find out the minimum fraction of load shed required for the mitigation of an FIDVR event.

V. Conclusion and Future Work

The paper presents a faster than real-time digital replica that can be used to mitigate FIDVR by predicting the exact amount of load to be shed. We have shown in Table I that the predictions can be made in time so that it is possible to have an online implementation of the proposed FIDVR mitigation scheme. In addition, as seen in Fig. 11 the proposed methodology allows for exact computation of the minimal load to be shed to achieve stability. The method can be used both, in centralized and decentralized fashion by running the replicas locally at the substations or centrally in the control room.

To improve the methodology even further, we will look at different voltage stability indices in relation to FTRTDR. Such indices will be used to more accurately determine the effectiveness threshold of the FTRTDR. In addition, an exact methodology is needed to determine how many replicas should be ran in case of different events.

References

[1] R. J. Bravo, R. Yinger, and P. Arons, Fault Induced Delayed Voltage Recovery (FIDVR) indicators, in 2014 IEEE PES T D Conference and Exposition, 2014, pp. 1-5.

[2] R. J. Bravo and D. P. Chassin, Fault Induced Delayed Voltage Recovery (FIDVR) model validation, in 2016 IEEE/PES Transmission and Distribution Conference and Exposition (T D), 2016, pp. 1-4.

[3] H. Wu, H.-D. Chiang, and B.-K. Choi, Slow voltage recovery response of several load models: Evaluation study, in 2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008, pp. 1-6.

[4] Q. Huang and V. Vittal, Application of Electromagnetic Transient-Transient Stability Hybrid Simulation to FIDVR Study, IEEE Transactions on Power Systems, vol. 31, no. 4, pp. 2634-2646, Jul. 2016.

[5] Y. Xu et al., Assessing Short-Term Voltage Stability of Electric Power Systems by a Hierarchical Intelligent System, IEEE Transactions on Neural Networks and Learning Systems, vol. 27, no. 8, pp. 1686-1696, Aug. 2016.

[6] M. Paramasivam, A. Salloum, V. Ajjarapu, V. Vittal, N. B. Bhatt, and S. Liu, Dynamic Optimization Based Reactive Power Planning to Mitigate Slow Voltage Recovery and Short Term Voltage Instability, IEEE Transactions on Power Systems, vol. 28, no. 4, pp. 3865-3873, Nov. 2013.

[7] M. Islam, N. Mithulananthan, and M. J. Hossain, Dynamic voltage support by TL-PV systems to mitigate short-term voltage instability in residential DN, IEEE Transactions on Power Systems, vol. PP, no. 99, pp. 1-1, 2017.

[8] S. Dasgupta, M. Paramasivam, U. Vaidya, and V. Ajjarapu, Entropy-Based Metric for Characterization of Delayed Voltage Recovery, IEEE Transactions on Power Systems, vol. 30, no. 5, pp. 2460-2468, Sep. 2015.

[9] S. M. Halpin, K. A. Harley, R. A. Jones, and L. Y. Taylor, Slope-Permissive Under-Voltage Load Shed Relay for Delayed Voltage Recovery Mitigation, IEEE Transactions on Power Systems, vol. 23, no. 3, pp. 1211-1216, Aug. 2008.

[10] K. Mollah, M. Bahadornejad, N. K. C. Nair, and G. Ancell, Automatic under-voltage load shedding: A systematic review, in 2012 IEEE Power and Energy Society General Meeting, 2012, pp. 1-7.

[11] Y. Dong, X. Xie, K. Wang, B. Zhou, and Q. Jiang, An Emergency-Demand-Response Based Under Speed Load Shedding Scheme to Improve Short-Term Voltage Stability, IEEE Transactions on Power Systems, vol. 32, no. 5, pp. 3726-3735, Sep. 2017.

[12] H. Bai and V. Ajjarapu, A Novel Online Load Shedding Strategy for Mitigating Fault-Induced Delayed Voltage Recovery, IEEE Transactions on Power Systems, vol. 26, no. 1, pp. 294-304, Feb. 2011.

[13] M. Ojaghi, M. Azari, and A. C. Valujerdi, Robust UVLS scheme to improve transmission line performance considering interruption cost and voltage stability index, in 2014 IEEE International Conference on Industrial Technology (ICIT), 2014, pp. 541-546.

[14] WECC Composite Load Model Specifications 01-27-2015. [Online] Available: https://www.wecc.biz/Reliability/WECC Composite Load Model Specifications 01-27-2015.docx

[15] Q. Huang et al., A Reference Implementation of WECC Composite Load Model in Matlab and GridPACK., CoRR, vol. abs/1708.00939, 2017.

[16] Y. C. Chen, T. Banerjee, A. D. Domnguez-Garca, and V. V. Veeravalli, Quickest Line Outage Detection and Identification, IEEE Transactions on Power Systems, vol. 31, no. 1, pp. 749-758, Jan. 2016.

[17] C. D. López and J. L. Rueda-Torres, Python Scripting for DIgSILENT PowerFactory: Leveraging the Python API for Scenario Manipulation and Analysis of Large Datasets, in Advanced Smart Grid Functionalities Based on PowerFactory, Springer, Cham, 2018, pp. 19-48.

[18] Z. Huang, S. Jin, and R. Diao, Predictive Dynamic Simulation for Large-Scale Power Systems through High-Performance Computing, in 2012 SC Companion: High Performance Computing, Networking Storage and Analysis, 2012, pp. 347354.

[19] Y. Chen, E. Fitzhenry, S. Jin, B. Palmer, P. Sharma, and Z. Huang, An integrated software package to enable predictive simulation capabilities, in 2016 Power Systems Computation Conference (PSCC), 2016, pp. 1-6.