DC link capacity enhancement for dynamic operation of back-to-back modular multilevel converters

MSc Thesis Report

R.P.J. van der Sande BSc

September 2022

TU Delft Delft University of Technology

DCE&S DC systems, Energy conversion & Storage

ESP Lab Powered by TenneT

DC link capacity enhancement for dynamic operation of back-to-back modular multilevel converters

Thesis

by

R.P.J. van der Sande BSc 4690311

Delft University of Technology

Faculty of Electrical Engineering,
Mathematics and Computer Science

Submitted in partial fulfilment of the requirements for the degree of

Master of Science

In Electrical Engineering

To be defended in public on 23 September 2022 at 12:30 PM

Supervisors:	Prof. dr. ir. P. Bauer	
	Dr. ir. A. Shekhar	
	R. Deshmukh MSc	
Thesis committee:	Prof. dr. ir. P. Bauer	TU Delft, DCE&S
	Dr. A. Lekić	TU Delft, IEPG ESE
	Dr. ir. A. Shekhar	TU Delft, DCE&S

An electronic version of this thesis is available at http://repository.tudelft.nl/.

Abstract

With the increasing appearance of DC loads and DC sources in the Medium Voltage Alternating Current (MVAC) distribution grids, the need for DC power systems is getting more and more pronounced. As a result, the Multilevel Modular Converter (MMC) has become a promising and innovative technology that can serve as the interface between a DC and AC network. The MMC-based Medium Voltage Direct Current (MVDC) distribution link is one of the solutions to incorporate DC in power grids. This link consists of two back-to-back configured MMCs connecting two possibly asynchronous AC networks. Generally, an MVDC distribution link is operated at a fixed rated DC voltage set through the MMC. This work explores the possibility of enhancing the DC link voltage beyond the nominal value to improve the power transfer capacity of the distribution link. The enhancement is achieved while preserving the average energy stored in the MMC and maintaining the AC-side harmonic performance.

First, a control strategy was developed that qualified for the static operation of back-to-back configured MMCs. This control strategy was designed using multiple sub-control modules, each regulating one or multiple circuit quantities using a closed-loop Proportional-Integral (PI) or Proportional-Resonant (PR) control strategy. Second, the analytical limitation to the DC link voltage enhancement was determined. This provided the enhancement boundary expression, which revealed the dependence between the enhancement limit and the grid-injected reactive power. Third, the MMC control strategy was adapted to dynamically incorporate the DC link voltage enhancement. This was performed using the open-loop DC link voltage control, which dynamically enhanced the link voltage by using the reactive power input reference. The controller is realised using a finite state machine that provides an event-driven control system with conditional state transitions. Simulations verified the performance of this controller. Finally, the dynamic DC link voltage controller is implemented for a lab-scale MMC and optimally tuned using the MO tuning method. This is to provide experimental verification of the DC link voltage enhancement. Three experiments were performed to: demonstrate the workings of the enhancement concept, verify the analytical enhancement boundary expression, and show the performance of the dynamic DC link voltage controller. The experiments concluded that the open-loop dynamic control successfully achieved the DC link voltage enhancement and limited the grid injection of harmonic elements during system transients.

So, it is concluded that the power transfer capacity of an MMC-based MVDC distribution link can be enhanced by applying dynamic DC link voltage control. This while operating with the same submodule stresses and preserving the AC-side harmonic performance. When the DC current of the distribution link is fixed at the rated value, the power transfer capacity of the link increases linearly with the controller enhancement function. For system transients, the dynamic controller uses smart control logic to avoid harmonic element injection. Combined, this concludes that the dynamic DC link voltage control achieves a proper DC link capacity enhancement that meets the requirements for both steady state and dynamic conditions.

Acknowledgements

First of all, I would like to express my deepest gratitude to my supervisors, Dr. ir. Aditya Shekhar and Rohan Deshmukh MSc, for their excellent guidance, constructive advice, and endless support throughout this project. I truly enjoyed our interesting discussions and enlightening measurement sessions. Also, I would like to express my sincere gratitude to Prof. dr. ir. Pavol Bauer and Dr. Aleksandra Lekić, for being part of the thesis committee and providing insightful comments on future applications of the research topic. I am grateful to bring a contribution to this exciting and rapid involving field of research together with all of you. I have the utmost respect for your work and expertise.

I also want to give a special thanks to my family: Romee van der Sande, Cora Grootjen, Erik van der Sande and Klara Uleman, for their exquisite help and support, especially during difficult times. Their confidence kept me highly motivated to keep on improving myself throughout the project.

Finally, thanks should also go to all my study mates, friends, and the lab technicians for being part of this enjoyable journey.

Robin van der Sande
Delft, 12/09/2022

Contents

List of Figures

List of Tables

List of Abbreviations

AC Alternating Current

ADC Analog-to-Digital Conversion

ALA Arm-Level Averaged

BEV Battery Electric Vehicle

DC Direct Current

D-ZSS Discontinuous-Zero Sequence Signals

FC Flying Capacitor

FCEV Fuel Cell Electric Vehicle

FPGA Field-Programmable Gate Array

FSM Finite State Machine

HVDC High Voltage Direct Current

IGBT Insulated Gate Bipolar Transistor

LSC-PWM Level Shifted Carrier-PWM

LPF Low-Pass Filter

LVDC Low Voltage Direct Current

MMC Multilevel Modular Converter

MO Magnitude Optimum

MVAC Medium Voltage Alternating Current

MVDC Medium Voltage Direct Current

NLC Nearest Level Control

NPC Neutral Point Clamped

PHEV Plug-in Hybrid Electric Vehicle

PI Proportional-Integral

PID Proportional-Integral-Derivative

PLL Phase-Locked Loop

PR Proportional-Resonant

PSC-PWM Phase Shifted Carrier-PWM

PWM Pulse Width Modulation

SM Submodule

SLA Submodule-Level Averaged

SHE Selective Harmonic Eliminated

SPWM Sinusoidal-PWM

STATCOM Static Synchronous Compensator

SV-PWM Space Vector PWM

THD Total Harmonic Distortion

THI Third Harmonic Injection

THI-ZSS Third Harmonic Injection-Zero Sequence Signals

VSC Voltage Source Converter

ZOH Zero-Order Hold

Chapter 1

Introduction

With the 2015 Paris agreement, the community agreed on limiting global warming to a maximum of 2 degrees Celsius. This agreement caused the decision of the European Union to achieve climate neutrality by the year 2050 [1]. Consequently, a global shift is observed away from fossil fuels and towards sustainable alternatives. This decarbonisation imposes a set of ongoing changes for the energy generation, energy transport, and energy consumption. For example, the transport sector introduced the Battery Electric Vehicle (BEV), Plug-in Hybrid Electric Vehicle (PHEV) and Fuel Cell Electric Vehicle (FCEV) as alternatives to internal combustion cars. The heat sector has started to renounce coal and natural gas and shifts towards a more sustainable heat pump implementation. Besides, the energy sector transitions from fossil fuel powered to a more renewable energy supply.

Although these changes bring humanity closer to the goal of climate neutrality, they do impose a significant strain on the power transmission and distribution systems. Loads like the BEV and heat pump draw excessive amounts of energy from the grid. Meanwhile, renewable energy sources like wind and solar have low capacity factors and are highly weather dependent. Consequently, grid congestions are starting to appear more frequently. Currently, about 17 percent of the global energy demand is provided through the power grids, but by the year 2050, this is expected to grow to as much as 57 percent [2]. As current AC grids start to face frequent congestions and future grid demands only tend to rise, a commonly proposed solution is the implementation of a DC power grid. Future grids will be powered to a significant extent by DC sources and used by DC loads. Thus the need for DC power system in grids is getting more and more pronounced.

MMC-based MVDC distribution systems are seen as one of the solutions to incorporate DC in power grids. The Multilevel Modular Converter (MMC) technology is well suited for high-power medium-voltage applications like medium-voltage motor drives, power quality improvement and power transmission systems [3]. Due to its structure, the MMC has many advantages including: low AC and DC side harmonics, reduced switching losses and high controllability [4]. Because of this superior performance, MMCs can be used to support the exciting MVAC distribution networks by incorporating two terminal MVDC distribution links. Besides, exciting AC architectures can be reconfigured to multi-terminal MVDC networks. Both concepts allow for a higher power transfer capacity, improved control, and a more stable grid implementation. Overall it provides a better utilisation of the existing grid infrastructure to meet future demands.

Figure 1 shows the structure of a MVDC distribution link, connecting two AC networks 1,2. Generally, this MVDC distribution link is operated at a fixed rated DC voltage, set through the MMC. Though,

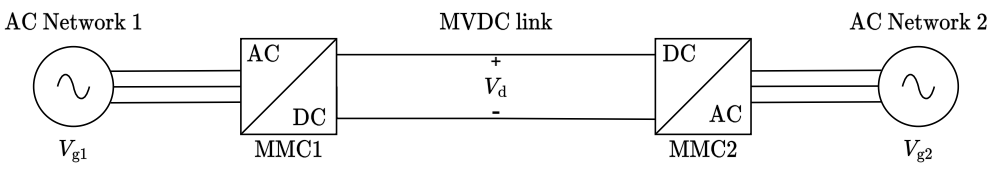


Figure 1.1: Overview of the MMC based MVDC distribution link.

as proposed in [5], the distribution link can be operated at an enhanced DC voltage V_{d} that exceeds the rated value V_{dr} while maintaining the average energy stored in the MMCs. Thus the MMC can be operated at an enhanced DC voltage while encountering the same submodules stresses. When operating at the rated DC link current, the voltage enhancement improves the power transfer capacity of the MVDC distribution link, e.g. during grid congestions. Alternatively, when operating at rated power, the DC link current and thus the circulating currents can be reduced. This lowers operating losses of the converters and improves the efficiency of the distribution link.

This thesis explores the possibility of operating an MMC-based MVDC distribution link at an enhanced DC voltage while maintaining the average energy stored in the MMCs. This combines the superior performance of the MMC with a smart control architecture to achieve an enhancement in the power transfer capacity of the link. The control structure is designed to enhance the capacity during dynamic operation, where the introduced concept can be extended to multi-terminal MVDC application.

1.1 Research objective

The focus of this thesis is to analyse the power transfer capacity enhancement that can be gained when operating an MMC-based MVDC distribution link under dynamic DC link voltage control as opposed to the static operation at the rated DC voltage. This thesis, therefore, answers the following research question:

To what extent can the power transfer capacity of an MVDC distribution link be enhanced by using dynamic DC link voltage control for the back-to-back operation of modular multilevel converters?

To structure the analysis of the main research question, it is decomposed into four sub-research questions. First, a control strategy is required that regulates the modular multilevel converter when it is back-to-back configured in a MVDC distribution link. Therefore, the first research question is posed as follows:

1. Which control strategy qualifies for the static operation of back-to-back configured MMCs?

Before, the control strategy can be adapted to include the DC link voltage enhancement. First, the limitations to the enhancement must be comprehended. As the MMC energies must be kept within rated limits, this imposes a limiting constraint. The impact of this constraint on the DC link voltage enhancement must be examined. This results in the second research question:

2. What is the analytical limitation to the DC link voltage enhancement?

By combing the control strategy and the analytical limitation, the existing control strategy is adapted to incorporate DC link voltage enhancement. The enhancement should be achieved for both steady-state and transient conditions. Therefore, the third research question is defined as follows:

3. How can the MMC control strategy be adapted to incorporate the DC link voltage enhancement during dynamic operation?

Finally, the enhancement performance must be investigated using the adapted control strategy. This involves both the steady-state and transient performance of the implemented dynamic DC link voltage control. This defines the final research question as follows:

4. To what extent can the dynamic DC link voltage control enhance the DC link voltage of the MVDC distribution link?

1.2 Thesis outline

This thesis is structured in 9 chapters. Each chapter relates to one of the sub-research questions. The contents of the chapters can be defined as follows:

Chapter 2: Provides an overview of the literature review on MMCs in MVDC applications. This chapter puts the MMC technology into perspective, analysing the advantages and disadvantages. Besides, it elaborates on the structure of the MMC, the submodule design, and modulation techniques. Finally, it contains an overview of the submodule balancing strategies.

Chapter 3: Defines a dynamic model of the MMC in a MVDC distribution link application. Which includes a per-phase MMC model, dynamic DC-side model, DC bus model and a AC network model. Furthermore, it provides a complete derivation of the MMC control structure. This includes the plant model derivation, controller design and parameter constraint definition.

Chapter 4: Describes the analytical derivation of the DC link voltage enhancement boundary for the back-to-back operation of MMCs. This chapter further provide an interpretation of the enhancement boundary along with the analysis of its limitations

Chapter 5: Defines the alteration of the MMC control strategy to incorporate the DC link voltage enhancement dynamically. This chapter provide two approaches on the design of the dynamic controller: direct controller and the open-loop controller.

Chapter 6: Elaborates on the implementation of the modulator and controller for the lab-scale Imperix MMC. This comprises the design philosophy, control structure, parameter selection and experimental verification.

Chapter 7: Provides the experimental results regarding the DC link voltage enhancement that is achieved by the implemented dynamic DC link voltage controller. Both the steady-state and transient character of the open-loop controller are measured and discussed.

Chapter 8: Delves into the concept of third harmonic arm voltage injection to extend the DC link voltage enhancement boundary. This concept is explained and verified using simulations and experiments.

Chapter 9: Provides the conclusion of the research project and discusses future work.

Chapter 2

Literature Review

As introduced in Chapter 1, this thesis considers the enhancement of the MMC-based MVDC distribution link. Before starting the enhancement concept, this chapter provided a literature review of MMCs in MVDC applications. First, Section 2.1 describes the relevant basics of MVDC distribution systems and discusses the advantages and disadvantages of MMC in MVDC. Second, Section 2.2 explains the MMC topology and elaborates on the design of a submodule. Third, Section 2.3 defines the modulation concept and discusses the modulation techniques. Finally, Section 2.4 explains the concept of submodule balancing with the associated strategies.

2.1 MMC-based MVDC distribution systems

Following the definition of the IEC and IEEE, the MVDC voltage class has recommended rated DC voltages between $1kV$ and $35kV$ [6]. All with a voltage tolerance of $\pm 10\%$. Rated DC voltages below $1kV$ are classified as Low Voltage Direct Current (LVDC) and above $35kV$ are classified as High Voltage Direct Current (HVDC). Nowadays, electrical power is mostly transmitted using high-voltage AC systems and HVDC links [7]. Whereas MVAC grids are often utilised for power distribution. The reason for an AC distribution grid over an MVDC grid lies in a cost perspective. As mentioned in [8], the break-even distance for choosing a DC transmission over an AC transmission is between 800km and 1000km for overhead lines and about 50km for submarine cables. This is caused by the simplicity and low-cost implementation of AC voltage conversions. Different voltage levels can be reached using low cost, reliable and highly efficient transformers [7]. Therefore the starting cost of a DC transmission system surpasses the AC system. Then with each kilometre transmission line, the DC system becomes more feasible as a result of its smaller cable diameter.

Though, over the past five decades, the development of high-power electronic converters has rapidly improved the performance of DC voltage conversions [7]. Where new converters topologies, e.g. MMC, become highly efficient, reliable and cost-effective competitors to the AC transformers. This allows for more practical implementation of MVDC transmission and MVDC distribution. Note that, besides the cost perspective, the MVDC link has many properties that make it advantageous as a distribution line over an AC system [9, 10]:

- The power flow is uninterruptible and fully controllable by the power electronic converter.
- With the use of an appropriate control strategy, transmission losses can be actively reduced.
- With the use of an appropriate control strategy, high converter reliability can be assured.
- No reactive power is transferred. This results in a loss reduction and a higher transfer efficiency.
- No DC-link synchronisation is needed.
- The thermal capability of an exciting AC link can be enhances by using a DC operation.

The idea of the MVDC distribution link can be extended to a multi-terminal link, denoted as a MVDC grid. The MVDC grid is an innovative power distribution infrastructure that allows the simultaneous

connection of multiple DC loads and sources like: Electric vehicles, PV systems, (offshore) wind farms and grid-connected converters [10]. Note that the control of the power electronic converters is enhanced for a multi-terminal link application.

Although multi-terminal links are of interest, in the remainder of this thesis the two-terminal MVDC distribution link is considered. The MVDC link connects to two asynchronous MVAC networks using back-to-back configured multilevel modular converters. An overview of the circuit configuration was provided in Figure 1.1. In this figure, v_{g1} and v_{g2} are the primary and secondary three-phase grid voltages respectively.

2.1.1 Advantages and disadvantages of MMC in MVDC

As introduced in Chapter 1, the MMC technology has significant advantages over other converter topologies for implementing high-power medium-voltage AC-DC and DC-AC conversions. To put the modular multilevel converter into perspective, a comparison is made with the two- or three-level Voltage Source Converter (VSC) for the medium-voltage application. The three-phase 2L-VSC is constructed using three phase legs that comprise two switches. Each leg is connected to an output phase (a,b,c) and all thee connect to the DC side terminal, as shown in Appendix A.1. The converter can generate only two voltage levels, $V_d/2$ and $-V_d/2$. The advantages of the modular multilevel converter over the 2L-VSC are defined as follows [4, 11–13]:

- Because of the higher number of output levels in the MMC, the AC-side harmonic distortion is significantly reduced compared to the 2L-VSC. This allows for the absence of an AC-side grid filter, reducing implementation costs and lowering conduction losses.
- The large number of submodules in the MMC allows for a reduction of the submodule switching frequency while maintaining a high effective switching frequency. This reduces switching losses and allows for the optimisation of condition losses.
- Due to its structure, the MMC does not require a DC side capacitor. This reduces cost and improves the DC-side dynamic performance of the converter.
- Due to the series connected submodule, the switches require a lower blocking voltage which reduces implementation cost and lowers the on-state resistance of the switches.
- The design structure of the MMC allows for easy scalability, modularity and provides a simple method to introduce redundancy. As a result, MMC outperforms the 2L-VSC in its applicability and security of supply.

Although these aspects show the superior performance of the MMC, the downsides of the technology should also be mentioned. The disadvantages of MMC compared to the 2L-VSC are defined as follows [4, 12]:

- Due to its design structure, the MMC requires significantly more components, including switches and submodule capacitors. Besides, the converter control needs significantly more voltage and current sensors to regulate the operation.
- The control structure of the MMC is more complicated than the 2l-VSC alternative. The controller needs to process more data from the voltage and current sensors, which results in a more complicated Analog-to-Digital Conversion (ADC). Furthermore, additional to the input-output control, the MMC needs a controller that balances the submodule capacitor voltages.

2.2 The MMC topology

The modular multilevel converter is a sub-class of the cascaded converter topology, also known as the multi-cell converters. These cascaded converters are built using multiple series-connected converter elements, denoted as submodules or power cells. The submodules each contain the main components of the two-level voltage source converter: a DC capacitor and semiconductor switches. In a cascaded converter, the submodules are connected in series which is referred to as submodules strings. The submodule strings are used to limit the required blocking voltage across an individual submodule when the DC link voltage is increased to large values. When the DC link voltage of a cascaded converter is increased, the converter performance can be maintained by simply adding more submodules. This creates modality and scalability without significantly increasing the complexity of the converter.

The general circuit configuration of a modular multilevel converter is provided in Figure 2.1. In this figure V_{d} indicates the DC link voltage and i_{d} the DC link current. Furthermore, $v_{\mathrm{g,a}}$, $v_{\mathrm{g,b}}$, $v_{\mathrm{g,c}}$ and $i_{\mathrm{s,a}}$, $i_{\mathrm{s,b}}$, $i_{\mathrm{s,c}}$ indicated the three-phase AC side voltages and currents, respectively. Figure 2.1 also shows the submodule strings, which are connected in series with the arm inductors L. The inductor is used to limit the high-frequency components of the circulating current and prevent large current rises in the case of a DC fault [14]. The strings-inductor assembly is together denoted as an MMC arm. The upper and lower arm which are connected to a single phase are together denoted as an MMC leg. This MMC configuration consist of three upper arms: $SM_{\mathrm{u1}} - SM_{\mathrm{uN}}$ and three lower arms: $SM_{\mathrm{l1}} - SM_{\mathrm{lN}}$.

Note that the MMC circuit configuration shown in Figure 2.1 is referred to as the double-star configured MMC. This configuration is most applicable for medium and high voltage DC applications. However, other MMC configurations exist like: the star-configured MMC (Figure A.2), delta-configured MMC (Figure A.3) and Dual MMC (Figure A.4) [15]. Note that the first two MMC configurations have no DC link terminals. As a result, these topologies can only control the active power flow back and forth between the AC terminals and the floating submodule capacitors. The MMC in these configurations does not achieve a DC-AC or AC-DC conversion.

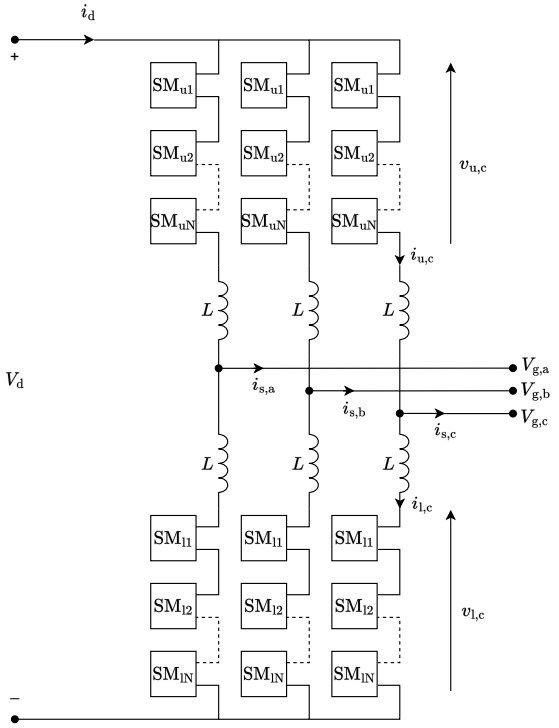


Figure 2.1: Schematic diagram of modular multilevel converter in double-star configuration.

2.2.1 Submodule design

Now that the circuit configuration of the modular multilevel converter is discussed, the structure of a Submodule (SM) can be explained. A submodule is a device that consists of one or multiple DC capacitors connected to the output terminals via semiconductor devices. A submodule in an MMC can either be inserted, when the DC capacitor is connected to the terminals, or bypassed. There are many possible configurations for implementing a submodule, where the chosen topology can significantly impact the performance of the MMC. The submodule choice effects: the number of output levels, the switch blocking voltage, the power losses, the DC-fault blocking capability and a lot more. It is therefore essential to select the submodule dependent on the application of the converter.

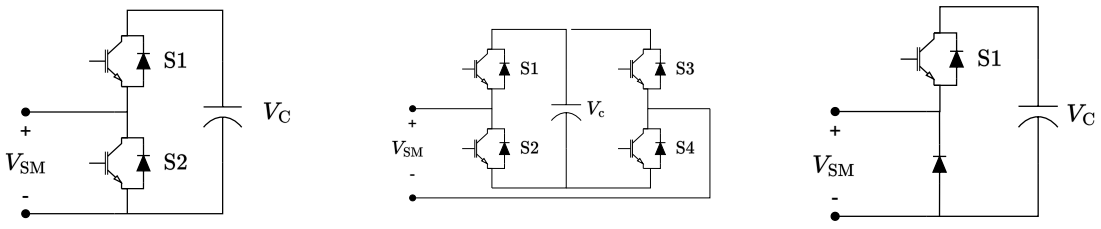
Half-bridge SM

The first submodule that is discussed is the half-bridge submodule topology (HB-SM). This topology has a structure similar to the two-level voltage source converter, which was explained in Section 2.1.1. The submodule consists of two Insulated Gate Bipolar Transistor (IGBT) $S1$ and $S2$, which are connected to a DC capacitor. The circuit diagram of the submodule is presented in Figure 2.2a.

With the half-bridge submodule, two switching states are possible [11]. First, the submodule can be bypassed, then switch $S2$ is closed while $S1$ is left open. As a result $v_{\mathrm{SM}} = 0V$. Second, the submodule can be inserted, then switch $S1$ is closed while $S2$ is left open. As a result $v_{\mathrm{SM}} = v_{\mathrm{c}}$. To represent the output voltage, the switching function s can be defined as given in Equation (2.1), for which bypassed $s = 0$ and inserted $s = 1$.

$$v_{\mathrm{SM}} = s v_{\mathrm{c}} \tag{2.1}$$

Note that the submodule can also be operated in blocking state when both switches $S1$ and $S2$ are turned off. In this case, the arm current flows through the anti-parallel diodes and therefore, the direction of current determines the output voltage. This state is not used during normal operations but only during startup and malfunctions [11].



(a) Half-bridge submodule

(b) Full-bridge submodule

(c) Unidirectional SM

Figure 2.2: Common submodule topologies

Full-bridge SM

The second submodule topology is the full-bridge SM (FB-SM). This topology has a structure similar to half-bridge SM, but it comprises four IGBTs instead of two. The IGBTs $S1$ and $S2$ are connected to the positive output terminal, while the IGBTs $S3$ and $S4$ are connected to the negative output terminal. The circuit diagram of the submodule is presented in Figure 2.2b.

Similar to the half-bridge SM, the full-bride SM has limited switching states. For the full-bridge SM, the output voltage can take three values. The first state: $v_{\mathrm{SM}} = +v_{\mathrm{c}}$ which is achieved when $S1$ and $S4$ are closed and $S2$ and $S3$ are open. The second state: $v_{\mathrm{SM}} = -v_{\mathrm{c}}$ which is achieved when $S2$ and $S3$ are closed and $S1$ and $S4$ are open. The last state: $v_{\mathrm{SM}} = 0V$ can be achieved by either opening the top two or bottom two switches. These two are usually alternated to achieve an even distribution of power losses [11]. To represent the output voltage, a switching function s_1, s_2 can be defined as given in Equation (2.2).

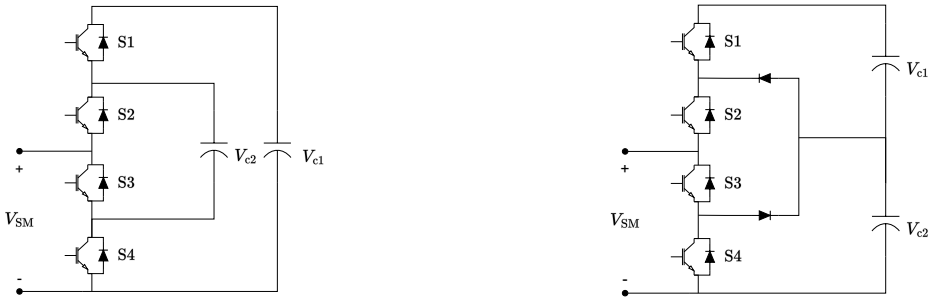
$$v_{SM} = (s_1 - s_2)v_c \tag{2.2}$$

Unidirectional SM

The third submodule that is discussed is the unidirectional SM (UN-SM). This power cell topology is similar to the half-bridge SM though IGBT $S2$ is replaced with a pn-diode. This topology is proposed to reduce the number of semiconductor devices needed in a power cell. The circuit diagram of the submodule is presented in Figure 2.2c. The main drawback of the topology is that the switching state of the submodule becomes dependent on the current direction [16].

Three-level SM

The fourth submodule topology is the three-level SM. In contrast to the previously discussed submodules, the three-level SM has multiple capacitors that can be combined to set the output terminal voltage. Because of its design, this topology allows for more discrete voltage levels at the output terminals [17]. There are two common configurations: the three-level Flying Capacitor (FC) configuration, shown in Figure 2.3a, and the three-level Neutral Point Clamped (NPC) configuration, shown in Figure 2.3b. Note that the three-level FC and three-level NPC configurations perform like an FC converter and NPC converter as explained in [14].



(a) Three level FC submodule

(b) Three level NPC submodule

Figure 2.3: Three level submodules

Other SM topologies

In addition to the five discussed topologies many other possible submodule configurations are possible like: the clamp-double SM [17], the five-level cross-connected SM [17], a submodule with resonant inverter for IPT [16] and many more. However, their applications are limited due to the control's complexity and practical limitations. Therefore they are not further discussed in this report.

2.2.2 Submodule comparison

Now that the five submodule topologies have been discussed, the submodules can be compared based on their aspects and performance. As mentioned in the introduction of this section, the chosen SM configuration of the modular multilevel converter can significantly impact its operating performance. The performance aspects of the five discussed submodule topologies are described in Table 2.1 [14, 17].

Using this table, the optimal submodule can be selected given the application of the MMC. As can be concluded from Table 2.1 the full-bridge submodule has more output voltage levels compared to a half-bridge submodule. This leads to better harmonic performance of the MMC. Furthermore, The full-bridge SM has a bipolar operation and can thus operate with a non-positive DC component. The half-bridge submodule can only operate with a positive DC component, so its application is limited to a DC-connected MMC [18]. Besides, the half-bridge submodule has no dc fault blocking capability because of the free-wheeling diodes. Even though the full-bridge submodule performs better in some aspects, a trade-off is made on the submodule cost and power losses. So dependent on the MMC application, one submodule

Table 2.1: Comparison table of aspects and performance submodules.

Performance index:	HB-SM	FB-SM	UN-SM	FC-SM	NPC-SM
Number of SM output levels	2	3	2	3	3
Maximum blocking voltage of SM	v_c	v_c	v_c	$2v_c$	$2v_c$
Number of DC capacitors	1	1	1	2	2
Number of swishing devices	2	4	1	4	4
Power losses	Moderate	High	Low	Moderate	High
Bipolar operation	No	Yes	No	No	No
SM control complexity	Low	Low	Moderate	High	Low
DC fault blocking	No	Yes	No	No	No

can perform better than the other. For the remainder of this report, the half-bridge submodule configuration is considered. This submodule is currently the most widely adopted SM for HVDC applications of MMC [17]. The main reason being the use of only two IGBTs per SM, which decreases cost, simplifies the control, and increases the converter's efficiency.

2.3 Modulation techniques

Like all other power converters, the modular multilevel converter is an autonomous system [19]. Consequentially, the MMC's performance depends not only on the hardware design but also on the implemented control strategy. Following [19], power electronic control strategies can be classified into: modulation-base controllers, controllers without modulator and controllers with embedded modulator. To achieve a scalable and structured design, a modulation-base controller is used to regulate the MMC. Figure 2.4 presents the structure of the modulation-base controller, in which the modulation and control parts are segregated.

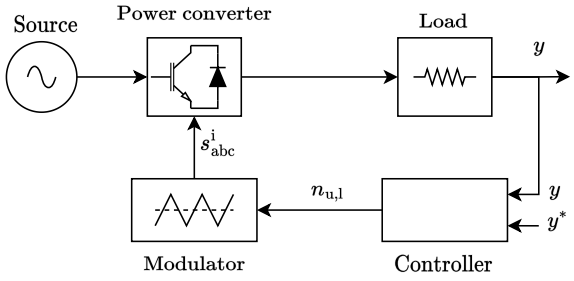


Figure 2.4: Schematic of the modulation-base controller.

The modulation and control modules each contribute to the operation of the MMC. First, the controller determines the six references for the MMC arms such that the MMC operates at the desired: output current, circulating current, active and reactive power, DC-link voltage and is synchronised with the three-phase grid. Figure 2.4 contains a closed-loop controller structure where y indicates the measured state and y^* the input desired state. The output $n_{\mathrm{u,l}}$ is the arm insertion index which is defined as the instantaneous ratio of the number of inserted SMs and the total number of SMs in an MMC arm. The controller is usually composed of multiple smaller controllers that each achieve a subtask. The controller design is further discussed in Chapter 3. Second, the modulator defines the switching signals of the individual submodules $s^{\mathrm{i}}_{\mathrm{abc}}$. The modulation process involves the conversion of arm insertion indices $n_{\mathrm{u,l}}$ into the switching signals such that the MMC arms supply the intended arm voltage.

Note that the primary focus of the modulator is to provide the intended arm voltage, which is achieved by inserting and bypassing submodules. As the submodules encounter different operational conditions,

their capacitor voltages v_c^i can easily diverge, which is detrimental to the performance of the MMC. This deviation is often opposed with a SM capacitor balancing module that enhances the modulation process [11]. The SM capacitor balancing is further explained in Section 2.4.

2.3.1 Modulator structure

Recall that the arms of the MMC are composed of series-connected half-bridge submodules, each consisting of two semiconductor switches. These switches are controlled using gate switching signals that can turn on or off the device. For an MMC with N submodules per arm, $12N$ switches have to be regulated. But according to Section 2.2.1, during normal operation the switches $S1$ and $S2$ should operate complementary. This reduces the complexity of the modulation to the generation of $6N$ switching signals. These switching signals are created using a modulation technique that is focused on a single arm. This means that the N switching signals s_{abc}^i are generated such that the arm voltage $v_{u,l}$ is set at the desired value $v_{u,l}^*$.

Following [11, 14, 20, 21], it can be concluded that there are multiple modulation formats proposed in literature. These formats have the same output: the switching signals s_{abc}^i. Though, vary in terms of their input definition, examples include: the arm insertion indices $n_{u,l}$, the individual modulation indices m_{abc}^i and the arm voltage references $v_{u,l}^*$. Note that the effective task of the modulator is the same for all formats, though different notations are used. To provide an overview of the MMC modulation, Figure 2.5 is used. This figure shows the three stages of the modulator: the pre-Pulse Width Modulation (PWM) stage, the PWM stage and the SM capacitor balancing stage with their corresponding in- and outputs.

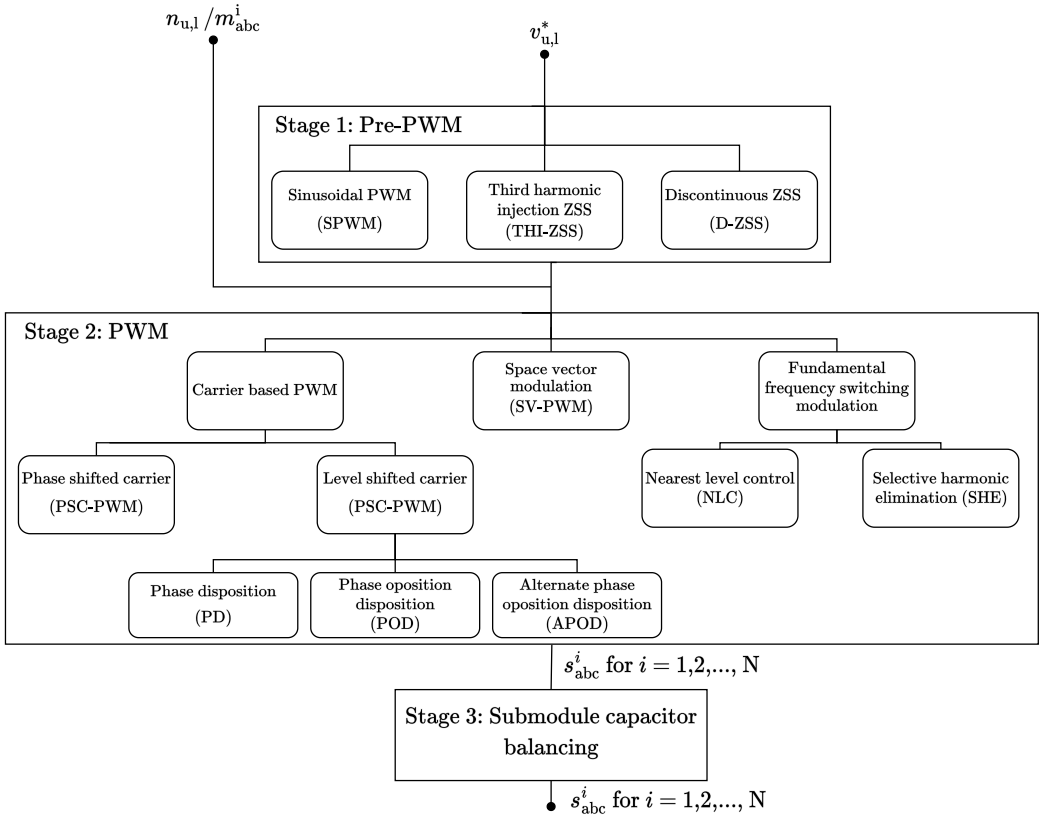


Figure 2.5: Schematic overview of modulation for MMC.

First, in the pre-PWM stage, the arm voltage reference $v_{u,l}^*$ is used to determine the arm insertion index reference $n_{u,l}$. This conversion is performed by using the sum of the capacitor voltages in an MMC arm

$v^{\Sigma}_{\mathrm{cu,l}}$. Note that in some cases the controller directly provides $n_{\mathrm{u,l}}$ / $m^{\mathrm{i}}_{\mathrm{abc}}$, which makes the pre-PWM stage redundant. Second, the PWM stage is used to create the submodule switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$ using the arm insertion index reference. After the PWM stage, the third stage: SM capacitor balancing, is applied. In this stage, the switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$ can be altered to account for submodule capacitor imbalances. This third stage is further discussed in Section 2.4.

2.3.2 Pre-PWM stage

When the MMC controller has defined the arm voltage reference $v^{*}_{\mathrm{u,l}}$, the pre-PWM stage is applied. This stage defines the arm insertion index $n_{\mathrm{u,l}}$ to create an arm voltage equal to the reference voltage $v^{*}_{\mathrm{u,l}}$. Following Figure 2.5 the process is performed using three possible topologies: Sinusoidal-PWM (SPWM), Third Harmonic Injection-Zero Sequence Signals (THI-ZSS) and Discontinuous-Zero Sequence Signals (D-ZSS) [21].

At first consider the SPWM topology. This topology converts the arm voltage reference into the insertion index using Equation (2.3). The arm insertion index is defined as the instantaneous ratio of the arm reference voltage and sum capacitor voltage [21]. Note that for most applications $v^{*}_{\mathrm{u,l}}$ are sinusoidal functions of time which makes $n_{\mathrm{u,l}}$ a normalised sinusoid.

$$n_{\mathrm{u,l}} = \frac{v^{*}_{\mathrm{u,l}}}{v^{\Sigma}_{\mathrm{cu,l}}} \tag{2.3}$$

Second, consider the THI-ZSS topology, which is a sub-class of the zero sequence signals. With the THI-ZSS, a third-order harmonic is added to the fundamental frequency reference signals of the three phase legs in the MMC. This to enhance the converter performance. The idea is based on the fact that the odd-multiple third-order harmonics ($3f_1$,$9f_1$,$15f_1$...) become zero-sequence components, which cancel out in the line-to-line voltage of a three-phase converter. The ZSS are used to reduce grid current harmonics and increase the linear modulation range of the converter.

In THI-ZSS a third harmonic component ($3f_1$) is added to the reference arm voltage $v^{*}_{\mathrm{u,l}}$ to maximise the usage of the DC-link. The added third-order component reduces the reference signal's peak value such that the fundamental component's amplitude can slightly exceed the DC-link voltage. This allows for an effective modulation index larger than one, without facing the drawbacks of overmodulation. Following [11], the optimal amplitude of the third harmonic component is 1/6 of the fundamental amplitude, which extends the linear modulation range by 15%. Alternatively, following [21], the harmonic spectrum of the output voltage can be minimised when the amplitude of the third harmonic component is 1/4 of the fundamental component.

Finally, consider the D-ZSS topology, which is again a subclass of the zero sequence signals. In this topology an offset is added to the arm insertion index $n_{\mathrm{u,l}}$ of Equation (2.3) in order to clamp the output voltage to a particular voltage level. In [21] it is shown that the converter voltages are clamped over 30°, 60°, and 120°intervals. During these intervals, no switching operations are performed, which reduces switching losses.

2.3.3 Pulse width modulation stage

After acquiring the reference indices via either the controller or pre-PWM stage, pulse width modulation is performed. In the PWM stage, the reference indices are converted into appropriate submodule switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$, such that the desired arm voltages are created. Following Figure 2.5, it can be concluded that there are multiple techniques for implementing PWM.

A: Carrier-based PWM
The first class of PWM is the carrier-based PWM. In this class, the arm insertion index $n_{\mathrm{u,l}}$ is compared

to triangular carrier signals to generate the N switching signals s^{i}. The comparison process is further discussed in Appendix A.3. In carrier-based PWM the triangular carrier signals are arranged either horizontally or vertically in the linear modulation range [14].

A1: Level shifted carrier PWM
For the Level Shifted Carrier-PWM (LSC-PWM), N triangular carrier signals with the same magnitude and frequency are spread vertically within the linear modulation region. Now each of the carrier signals refers to two voltage levels. For the LSC-PWM three sub-classes are distinguished based on the phase relation of the carriers:

- Phase-disposition (PD): The triangular carriers are vertically arranged and all in phase.
- Phase-opposition-disposition (POD): The triangular carriers below the zero line voltage are out of phase with the ones above.
- Alternate-Phase-opposition-disposition (APOD): The triangular carriers are out of phase with their vertical neighbours, creating an alternating phase pattern.

The three sub-classes of LSC-PWM are presented graphically in Figure A.6. The main advantage of the LSC-PWM is that the modulator implementation is relatively simple. Furthermore, this modulator allows for easy scalability, in which triangular carrier signals are added to implement an increase in the number of submodule N. The main drawback of this type of modulator is that the load distribution among the SM is uneven during normal operation. This means that some submodules experience greater power losses than others. This in turn, causes harmonic distortion, reducing the MMC performance. A solution is to implement a carrier rotation or SM selection technique in stage 3 of the modulation process [17].

A2: Phase shifted carrier PWM
For the Phase Shifted Carrier-PWM (PSC-PWM), N triangular carrier signals with the same magnitude and frequency are displaced horizontally within a fundamental period. The N carrier signals are shifted by $\phi_{\mathrm{c}} = 360^{\circ}/N$. These carrier signals are then compared with the reference insertion index to generate the switching signals s^{i} with $i \in [1, N]$. The PSC-PWM is presented graphically in Figure A.7. The main advantage of the PSC-PWM over the LSC-PWM is that it provides a natural balancing of the submodule capacitor voltages, which limits the divergence of the capacitor voltages. The balanced capacitors then improve the harmonic performance of the MMC. In addition, switching stresses and losses are more evenly distributed over the submodules.

B: Fundamental frequency switching modulation
The second class of PWM is the fundamental frequency switching modulation. This class of modulation is operated at a swishing frequency close to the fundamental frequency $f_{\mathrm{sw}} \approx f_1$. The method is used to reduce switching losses and is widely applied in high power converters [14]. Although to achieve the switching losses reduction, a trade-off is made on the output harmonic distortion. The fundamental frequency switching modulation has two main subclasses: Nearest Level Control (NLC) and Selective Harmonic Eliminated (SHE).

B1: Nearest level control
First, consider the nearest level control. NLC is a non-carrier based modulation method that generates N switching signals s^{i} from the arm insertion index $n_{\mathrm{u,l}}$. This method maps the reference index to a rounded number of cells $N_{\mathrm{u,l}}$ that the MMC arm must insert. $N_{\mathrm{u,l}}$ is calculated using Equation (2.4). From this equation, it can be concluded that the reference arm voltage is approximated by inserting the closest integer number of submodules [21].

$$N_{\mathrm{u,l}} = round(N * n_{\mathrm{u,l}}) \tag{2.4}$$

The output of the nearest level control is the number of inserted SMs $N_{\mathrm{u,l}}$, which can then be converted into the switching signals s^{i} with $i \in [1,N]$. The selection of submodules is generally performed using a sorting procedure in stage 3, where the SM capacitor voltages and current direction are taken into account. NLC is presented graphically in Figure A.8.

The main advantage of NLC over other modulation techniques is the simple modulator implementation. This type of modulator also allows for a straightforward scaling in N. Furthermore, the switching frequency of NLC is close to the fundamental frequency, which reduces the number of switching events compared to the carrier-based PWM, improving the operating efficiency of the MMC. A main drawback of NLC is the increased output harmonic distortion at the AC-side terminal. Besides, the method allows for the presence of large circulating currents [17].

B2: Selective harmonic elimination

The second type of fundamental frequency switching modulation is selective harmonic elimination (SHE). This method provides high-quality output waveforms at the AC-terminal $v_{\mathrm{g,abc}}$ by actively counteracting the low-harmonic content of the switching operation. This modulation method uses an optimisation technique which calculates the switching angles that minimise switching losses and eliminate particular low order harmonics [17]. This optimisation is done either in offline or real-time mode and requires solving a set of nonlinear equations [14]. Due to the complexity of optimising the nonlinear equations, the selective harmonic elimination method is not applied for large values of N [17]. This limits the application of SHE in MVDC applications.

C: Space vector PWM

The last type of PWM is Space Vector PWM (SV-PWM). Till now the modulator operated on an arm basis, using n_{u} to creased the arm switching signals s^{i} with $i \in [1,N]$. Meanwhile, SV-PWM uses the arm reference voltages of the three upper or lower arms $v^*_{\mathrm{u,abc}}$ directly to create $3N$ switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$. The first step of space vector PWM is the generation of the normalised reference vectors. The normalised reference vectors for the upper and lower arm are provide in Equation (2.5) and (2.6) respectively. In these equations, m_{a} is the amplitude modulation index and the three-phase AC output voltage references $v^*_{\mathrm{u,abc}}$ are assumed to be well balanced and sinusoidal.

$$\overrightarrow{v_u} = \frac{N}{V_{\mathrm{d}}} \begin{bmatrix} v^*_{\mathrm{u,a}} \\ v^*_{\mathrm{u,b}} \\ v^*_{\mathrm{u,c}} \end{bmatrix} = \frac{N}{2} \begin{bmatrix} 1 - m_{\mathrm{a}} sin\left(\omega_0 t\right) \\ 1 - m_{\mathrm{a}} sin\left(\omega_0 t - \frac{2\pi}{3}\right) \\ 1 - m_{\mathrm{a}} sin\left(\omega_0 t - \frac{2\pi}{4}\right) \end{bmatrix} \tag{2.5}$$

$$\overrightarrow{v_l} = \frac{N}{V_{\mathrm{d}}} \begin{bmatrix} v^*_{\mathrm{l,a}} \\ v^*_{\mathrm{l,b}} \\ v^*_{\mathrm{l,c}} \end{bmatrix} = \frac{N}{2} \begin{bmatrix} 1 + m_{\mathrm{a}} sin\left(\omega_0 t\right) \\ 1 + m_{\mathrm{a}} sin\left(\omega_0 t - \frac{2\pi}{3}\right) \\ 1 + m_{\mathrm{a}} sin\left(\omega_0 t - \frac{2\pi}{4}\right) \end{bmatrix} \tag{2.6}$$

Once the reference vectors of the upper and lower arm are calculated, the corresponding switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$ are created. This process involves the usage of switching states. A switching state refers to a specific configuration of the $6N$ SM switches. Each switching state generates a particular set of arm voltages, creating in total $3N(N+1)+1$ unique switching states [22]. The switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$ are created by operating the MMC in switching states for specific periods. So to create the intended arm voltage, the nearest switching vectors are selected and applied for a fraction of the fundamental period T_{s}. Following [14], the nearest four switching states $\overrightarrow{v_{\mathrm{y1}}}$, $\overrightarrow{v_{\mathrm{y2}}}$, $\overrightarrow{v_{\mathrm{y3}}}$, $\overrightarrow{v_{\mathrm{y4}}}$ are selected and applied for specific dwell times T_{y1}, T_{y2}, T_{y3} and T_{y4}. This is in accordance with Equation (2.7). The selection procedure and dwell time calculation can be found in [14].

$$T_{\mathrm{s}} * \overrightarrow{v_{\mathrm{u,l}}} = T_{\mathrm{y1}} * \overrightarrow{v_{\mathrm{y1}}} + T_{\mathrm{y2}} * \overrightarrow{v_{\mathrm{y2}}} + T_{\mathrm{y3}} * \overrightarrow{v_{\mathrm{y3}}} + T_{\mathrm{y4}} * \overrightarrow{v_{\mathrm{y4}}} \tag{2.7}$$

The main advantage of space vector modulation as PWM is that the method has: enhanced harmonic performance, high DC bus utilisation and allows for a regulated common-mode voltage. However, the

number of switching states increases quadratically with the number of SMs. It is therefore challenging to implement SV-PWM when $N > 20$. Consequently, the usage of space vector modulation in MVDC applications is limited.

2.4 Submodule capacitor balancing

In contrast to the 2L-VSC, the DC capacitance in an MMC is not centralised at the DC terminal but distributed among the submodules. This causes a problem during the operation of the converter, as a SM capacitor voltage changes with the current flow. Not all submodules are inserted simultaneously, which makes the SMs encounter different operational conditions. These conditions can lead to a spread in the capacitor voltages. As mentioned in Section 2.3, it is essential that the divergence of capacitor voltage remains limited for the performance of the MMC. Capacitor divergence leads to controller stability issues and reduced harmonic performance. Therefore, a system is implemented in stage 3 of the modulator that actively balances the arm submodule capacitor voltages to counteract divergence. Besides the capacitor balancing inside the arm, the arm energies must be regulated. This regulation is achieved in the controller and is further discussed in Chapter 3.

The SM capacitor balancing can be performed using various methods. All methods use the output of the modulation stage: the switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$. These switching signals define the instantaneous number of inserted submodules $N_{u,l}$ in an MMC arm. The number of inserted cells $N_{\mathrm{u,l}}$ is described in Equation (2.8) and is applicable to the six MMC arms.

$$N_{\mathrm{u,l}} = \sum_{i=1}^{N} s^{\mathrm{i}}_{\mathrm{u,l}} = n_{\mathrm{u,l}} * N \tag{2.8}$$

An overview of the SM capacitor balancing methods is provided in Figure 2.6 [11]. This figure indicates the three SM capacitor balancing implementations: submodule sorting, predictive sorting, and the tolerance band method. Note that these balancing methods can be combined with all PWM methods. However, for some modulation techniques, the active balancing performance is poorly. An example appears for PSC-PWM, introduced in Section 2.3.3. PSC-PWM provides natural balancing of the submodule capacitor voltages as similar submodule pulse patterns are created [14]. Therefore, the contribution of active balancing after PSC-PWM is limited. Alternatively, for SV-PWM, the switching sequence can directly be modified to limit divergence, restricting the impact of active balancing.

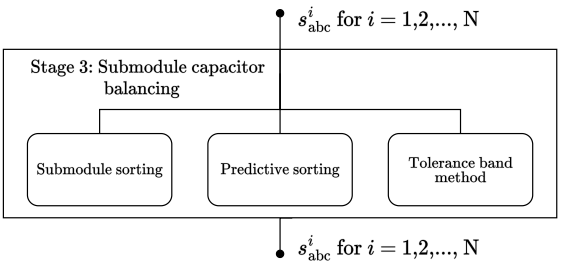


Figure 2.6: Schematic overview of submodule capacitor balancing for MMC.

2.4.1 Submodule sorting

The submodule sorting method, proposed in [23], is a simple implementation of submodule capacitor balancing. This method use the arm current i_{u} and submodule capacitor voltages $v^{\mathrm{i}}_{\mathrm{c}}$ with $i \in [1,N]$ to select the N_u submodules that are inserted. The procedure inserts the submodules with the most excessive capacitor voltage to minimise the voltage spread. If at some time point the number of inserted cells N_u is changed by the modulation stage, four cases for the balancing can be identified [11]:

- $i_u \geq 0$ and N_u increases: Then the bypassed SM with the lowest instantaneous capacitor voltage must be inserted. This is because the positive arm current will charge the capacitor, so v_c increases.
- $i_u < 0$ and N_u increases: Then the bypassed SM with the highest instantaneous capacitor voltage must be inserted. This is because the negative arm current will discharge the capacitor, so v_c decreases.
- $i_u > 0$ and N_u decreases: Then the inserted SM with the highest instantaneous capacitor voltage must be bypassed. This is because the positive arm current will no further charge the capacitor, keeping v_c from increasing.
- $i_u \geq 0$ and N_u decreases: Then the inserted SM with the lowest instantaneous capacitor voltage must be bypassed. This is because the negative arm current will no further discharge the capacitor, keeping v_c from decreasing.

A simple implementation of the submodule sorting method is to use the measurements of all N submodule capacitor voltages v_c^i in the arm as an input of a Field-Programmable Gate Array (FPGA). Then every sampling period $(1/f_s)$ the N submodule capacitor voltages v_c^i are measured and processed in an ordered list. Every switching period $(1/f_{sw})$, the reference number of inserted cells N_u can change. Then dependent on the current direction, the first N_u submodules of the ordered list are inserted. Using the list in ascending order if $i_u > 0$, or descending order if $i_u < 0$. Figure A.9 provides the flowchart of the submodule sorting method. The submodule sorting method provides a simple implementation to achieve balancing though it is not an efficient algorithm [11].

2.4.2 Predictive sorting

One of the main drawbacks of the submodule sorting method is that the SMs are balanced every sampling period. This procedure results in switching operations even if the capacitor voltages are close. The sorting method, therefore, comes with unnecessary switchings that impose additional losses. Furthermore, the method requires high computational power. To enhance the performance of the submodule balancing, the predictive sorting method is introduced. This method allows for a small spread in the capacitor voltages but limits the peak values. The peaks of the submodule capacitor voltages are constrained according to Equation (2.9) and (2.10) [11].

$$\max_t (v_{cu,l}^i) = v_{u,l}^{T+} \; for \; i \in [1,N] \tag{2.9}$$

$$\min_t (v_{cu,l}^i) = v_{u,l}^{T-} \; for \; i \in [1,N] \tag{2.10}$$

Equation (2.9) imposes a maximum target value of $v_{u,l}^{T+}$ for the submodule capacitor voltage. Similarly, Equation (2.10) imposes a minimum target value of $v_{u,l}^{T-}$ for the submodule capacitor voltage. $v_{u,l}^{T+}$ and $v_{u,l}^{T-}$ are calculated each fundamental period $(1/f_1)$ using either a explicit formula for the capacitor voltage ripple or by using the ripple over the last fundamental period [11]. Where a fundamental period is composed of a charging part $i_{u,l} > 0$ and discharging part $i_{u,l} < 0$.

Having established this definition, the working principle of the predictive sorting method can be explained. First, at the beginning of each fundamental period the target voltages $v_{u,l}^{T+}$ and $v_{u,l}^{T-}$ are calculated. Then every sampling period $(1/f_s)$ the N arm submodule capacitor voltages v_c^i are measured. Using these voltages and the state of the fundamental period (charging/discharging), the submodule peak/valley voltages $\hat{v}_c^i$ are predicted. Third, an ordered list is created based on the submodules for which $\hat{v}_c^i$ satisfies Equation (2.9) if $i_{u,l} > 0$ or 2.10 $i_{u,l} < 0$. Finally, the list's first N_u submodules are inserted like the submodule sorting method. The flowchart that represents this sorting method is provided in Figure A.10.

The advantage of the predictive sorting method is that the switching frequency can be reduced significantly, removing unnecessary switching operations. This comes with the drawback of operating with a larger voltage capacitor spread. Furthermore, the algorithm fails if all submodules have reached a target value. The reference number of inserted SMs: N_{u} can then not be reached anymore [11].

2.4.3 Tolerance band method

The last method for submodule capacitor balancing is denoted as the tolerance band method. This method allows the submodule capacitor voltages to vary freely inside an interval though controls the voltages outside the band. Due to its structure, the tolerance band method operates at a variable switching frequency. This is an advantage in terms of efficiency though a trade-off is made on harmonic performance.

In [11], two subclasses of tolerance band control are proposed: average submodule voltage tolerance band (ATB) and individual submodule voltage tolerance band (CTB). The first subclass, ATB, uses the sum of capacitor voltages to define the middle of the tolerance band at $v_{\mathrm{cu}}^{\Sigma}/N$. Then the submodule capacitor voltages can vary freely inside the interval given in Equation (2.11).

$$v_{\mathrm{c}}^{\mathrm{i}} \in [\frac{v_{\mathrm{cu}}^{\Sigma}}{N} - \delta, \frac{v_{\mathrm{cu}}^{\Sigma}}{N} + \delta] \tag{2.11}$$

The second subclass, CTB, uses the minimum and maximum acceptable charge of the capacitor during operation to define the tolerance band. Then the submodule capacitor voltages can vary freely inside the interval given in Equation (2.12).

$$v_{\mathrm{c}}^{\mathrm{i}} \in [v_{min}, v_{max}] \tag{2.12}$$

The flowchart that represents the average submodule voltage tolerance band and individual submodule voltage tolerance band are provided in Figure A.11 and A.12, respectively. An improvement on this method is proposed in [24] where v_{min} and v_{max} are made dynamic.

Chapter 3

Dynamic Models and Control Structure

Now that the structure and working principle of the modular multilevel converter have been discussed, the next step is to define the dynamic model of the MMC-based MVDC distribution link. This dynamic model is later used for the distribution link simulations and serves as the basis for controller design. After establishing the dynamic model, the remainder of the chapter is focused on the derivation of the control structure for the MMC. The controller is one of the fundamental components required for the operation of the multilevel modular converter, as the MMC has complex internal dynamics and inherent instabilities.

First, in Section 3.1, the dynamic model of the MMC-based MVDC distribution link is constructed by considering three dynamic model segments. Second, Section 3.2 provides an overview of the MMC controller. Third, in Section 3.3 the output current controller is discussed. Then in Section 3.4 the energy balancing control is elaborated, after which Section 3.5 explains the voltage control. Finally, the higher-level control is discussed in Section 3.6. For each part of the controller, both the methodology and implementation are explained, together with a description of the associated parameters and constraints.

3.1 Dynamic Models

To analyse the dynamic behaviour of a MMC-based MVDC distribution link, a dynamic model is developed. This distribution link model is composed of three parts. The first part is the dynamic per-phase MMC model, which is discussed in Section 3.1.1. The second part is the dynamic DC-side model, which is elaborated in Section 3.1.2. The last part considers the DC bus and AC network models, which are evaluated in Section 3.1.3. Together, these three dynamic model segments define the dynamic model of the MMC-based MVDC distribution link.

3.1.1 Dynamic MMC model

The dynamic MMC model is an important tool for understanding the converter operation and the design of its control system. In [25], six different types of MMC models are compared. These models differ in the degree of accuracy and complexity: from a full physics-based model to an average values model. With limited assumptions, the full physics-based model can accurately present the switching transients and switching losses of the IGBTs. However, the time step of this model must be small to achieve accuracy, which results in a considerable computational time for a single simulation. The detailed simulation is of lesser interest in studies investigating the power-system behaviour of the MMC. Instead, a more computationally efficient dynamic model can be used in which the MMC submodules appear as controllable voltage source [26]. As the dynamic DC link voltage enhancement is mostly involved with the power-system behaviour of the MMC, an average value model is used in this and later chapters for the modelling and control of the converter.

As mentioned in Section 2.2 the MMC is composed of 3 phase-legs (a,b,c) with each a lower and upper arm. These arms consist of N submodules that together define the arm voltage $v_{\mathrm{u,l}}$. The relation between the upper arm voltage and the SM capacitor voltages $v^{\mathrm{i}}_{\mathrm{cu,l}}$ is provided in Equation (3.1), which corresponds to the upper arm of phase ψ in Figure 2.1. Note that a similar equation holds for the lower

arm voltage. For simplicity, the ψ term is dropped in the remained of the chapter. Though, all equations remain applicable to all three phases of the MMC.

$$v_{\mathrm{u},\psi} = v^{1}_{\mathrm{SMu},\psi} + v^{2}_{\mathrm{SMu},\psi} + \cdots + v^{\mathrm{N}}_{\mathrm{SMu},\psi} = s^{1}_{\mathrm{u}} v^{1}_{\mathrm{cu}} + s^{2}_{\mathrm{u}} v^{2}_{\mathrm{cu}} + \cdots + s^{\mathrm{N}}_{\mathrm{u}} v^{\mathrm{N}}_{\mathrm{cu}} \tag{3.1}$$

Now using the concept of Equation (3.1), a per-phase dynamic model of the MMC is created in which the MMC arms are represented as controllable voltage sources. The model that is proposed in [26], is provided in Figure 3.1. In this model L represents the arm inductance, C the SM capacitance and R the arm resistance. The arm resistance R is used to model the conversion losses of the MMC. Furthermore, the upper and lower arm voltages are presented as controllable voltage sources v_{u} and v_{l}, respectively. The output voltage of these sources is controlled by the submodules switching signals $s^{\mathrm{i}}_{\mathrm{u,l}}$ with $i \in [1, N]$.

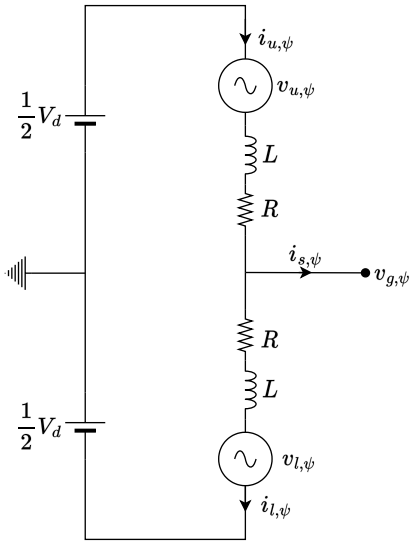


Figure 3.1: The per-phase equivalent model of MMC for phase a.

The control of the MMC provides the arm insertion indices $n_{\mathrm{u,l}}$. The insertion index is defined as the instantaneous ratio between the number of inserted submodules in an arm to the total number of submodules per arm N [26]. This is presented in Equation (3.2), in which $s^{\mathrm{i}}_{\mathrm{u,l}} = 1$ if the SM is inserted and $s^{\mathrm{i}}_{\mathrm{u,l}} = 0$ if the SM is bypassed.

$$n_{\mathrm{u,l}} = \frac{1}{N} \sum_{i=1}^{N} s^{\mathrm{i}}_{\mathrm{u,l}} \tag{3.2}$$

As mentioned in Section 2.4, because the submodule capacitors encounter different operational conditions, their voltages can start to diverge. This causes a non-uniform voltage distribution among the submodules. Though, to reduce the complexity of the simulation, it is assumed that the MMC control ensures an even distribution of sum capacitor voltage $v^{\Sigma}_{\mathrm{cu,l}}$ among the SMs. With this assumption, the dynamic model does not need to account for the individual capacitor voltages, and Equation (3.1) can be simplified to Equation (3.3).

$$v_{\mathrm{u,l}} = n_{\mathrm{u,l}} \cdot v^{\Sigma}_{\mathrm{cu,l}} \tag{3.3}$$

In this equation $v^{\Sigma}_{\mathrm{cu,l}}$ is the sum of the upper/lower arm capacitor voltages, denoted as the sum capacitor voltage. Note that arm current causes a change in the sum capacitor voltage, where the impact depends the insertion index $n_{\mathrm{u,l}}$. This relation is expressed in Equation (3.4).

$$v^{\Sigma}_{\mathrm{cu,l}} = \frac{n_{\mathrm{u,l}} \cdot N}{C} \int_{t_0}^{t} i_{\mathrm{u,l}} \cdot dt \tag{3.4}$$

Next consider the phase output current i_s and the circulating current i_c which are provide in Equation (3.5) and (3.6), respectively. In these equations i_u and i_l are the upper and lower arm current, respectively.

$$i_s = i_u - i_l \tag{3.5}$$

$$i_c = \frac{i_u + i_l}{2} \tag{3.6}$$

The linear expressions of Equation (3.5) and (3.6) can be inverted by solving for the phase-arm quantities. The result is provided in Equation (3.7) and (3.8).

$$i_u = i_c + \frac{i_s}{2} \tag{3.7}$$

$$i_l = i_c - \frac{i_s}{2} \tag{3.8}$$

The same linear transformation process is done for the output voltage v_s and the internal voltage v_c. Where v_s is used to drive the output current i_s and v_c drives the circulating current i_c. The transformations of v_s and v_c are done from Equation (3.9) and (3.10) to (3.11) and (3.12), respectively.

$$v_s = \frac{v_l - v_u}{2} \tag{3.9}$$

$$v_c = \frac{v_l + v_u}{2} \tag{3.10}$$

$$v_u = v_c - v_s \tag{3.11}$$

$$v_l = v_c + v_s \tag{3.12}$$

Now that the phase-arm quantities are expressed, the dynamic circuit equations can be derived. This is done using Kirchhoff's voltage law on the two inner loops in Figure 3.1. The result of the two loops are given in Equation (3.13) and (3.14).

$$\frac{1}{2}V_d - v_g - Ri_u - L\frac{di_u}{dt} - n_u * v_{cu}^{\Sigma} = 0 \tag{3.13}$$

$$-\frac{1}{2}V_d - v_g + Ri_l + L\frac{di_l}{dt} + n_l * v_{cl}^{\Sigma} = 0 \tag{3.14}$$

Using the linear transformations of Equations (3.7) and (3.8) while subtracting and adding Equations (3.13) and (3.14) results in Equations (3.15) and (3.16)

$$L\frac{di_c}{dt} = \frac{1}{2}V_d - Ri_c - \frac{n_u * v_{cu}^{\Sigma} + n_l * v_{cl}^{\Sigma}}{2} \tag{3.15}$$

$$\frac{1}{2}L\frac{di_s}{dt} = -v_g - \frac{1}{2}Ri_s + \frac{n_l * v_{cl}^{\Sigma} - n_u * v_{cu}^{\Sigma}}{2} \tag{3.16}$$

Finally, the output voltage v_s and internal voltage v_c in Equation (3.9) and (3.10) can be substitute which results in Equation (3.17) and (3.18)

$$L\frac{di_c}{dt} = \frac{1}{2}V_d - Ri_c - v_c \tag{3.17}$$

$$\frac{1}{2}L\frac{di_s}{dt} = -v_g - \frac{1}{2}Ri_s + v_s \tag{3.18}$$

In addition the dynamics of the sum capacitor voltages v_{cu}^{Σ} and v_{cl}^{Σ} can be found using Equations (3.3), (3.4), (3.7) and (3.8). The resulting equations are provided in Equation (3.19) and (3.20).

$$\frac{C}{N}\frac{dv_{\mathrm{cu}}^{\Sigma}}{dt} = n_{\mathrm{u}}\left(\frac{i_{\mathrm{s}}}{2} + i_{\mathrm{c}}\right) \tag{3.19}$$

$$\frac{C}{N}\frac{dv_{\mathrm{cl}}^{\Sigma}}{dt} = n_{\mathrm{l}}\left(\frac{-i_{\mathrm{s}}}{2} + i_{\mathrm{c}}\right) \tag{3.20}$$

By using Equations (3.15), (3.16), (3.19) and (3.20), the dynamic MMC model of one phase leg can be presented as a state space model [26]. The state space model equations of the MMC are given in Equation (3.21).

$$\frac{d}{dt}\begin{bmatrix} i_{\mathrm{c}} \\ i_{\mathrm{s}} \\ v_{\mathrm{cu}}^{\Sigma} \\ v_{\mathrm{cl}}^{\Sigma} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & -\frac{n_{\mathrm{u}}}{2L} & -\frac{n_{\mathrm{l}}}{2L} \\ 0 & -\frac{R}{L} & -\frac{n_{\mathrm{u}}}{L} & \frac{n_{\mathrm{l}}}{L} \\ \frac{Nn_{\mathrm{u}}}{C} & \frac{Nn_{\mathrm{u}}}{2C} & 0 & 0 \\ \frac{Nn_{\mathrm{l}}}{C} & -\frac{Nn_{\mathrm{l}}}{2C} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{c}} \\ i_{\mathrm{s}} \\ v_{\mathrm{cu}}^{\Sigma} \\ v_{\mathrm{cl}}^{\Sigma} \end{bmatrix} + \begin{bmatrix} \frac{V_{\mathrm{d}}}{L} \\ -\frac{2v_{\mathrm{g}}}{L} \\ 0 \\ 0 \end{bmatrix} \tag{3.21}$$

Note that this equation suggests a decoupling between the AC side and DC side character of the MMC. This appears as circulating current and phase current do not directly depend on each other in the state space equations.

3.1.2 Dynamic DC side model

To achieve a dynamic enhancement of the DC link voltage, the DC side dynamics are of great importance. In this section, a model is developed for the DC side dynamics of the MMC. This model is later used to define the expected system response to changes in the DC link voltage reference.

First, consider Figure 3.2. This figure shows the MMC with a DC bus capacitor C_{d}. From this figure can be concluded that the mismatch between the DC side current i_{d} and the sum of the upper arm currents $i_{\mathrm{u,abc}}$ flows into the DC bus capacitor. From this observation Equation (3.22) can be defined. Note that the same equation can be applied to the lower arm.

$$2C_{\mathrm{d}}\frac{dv_{\mathrm{du}}}{dt} = i_d - \sum_{k=abc} i_{\mathrm{u,k}} \tag{3.22}$$

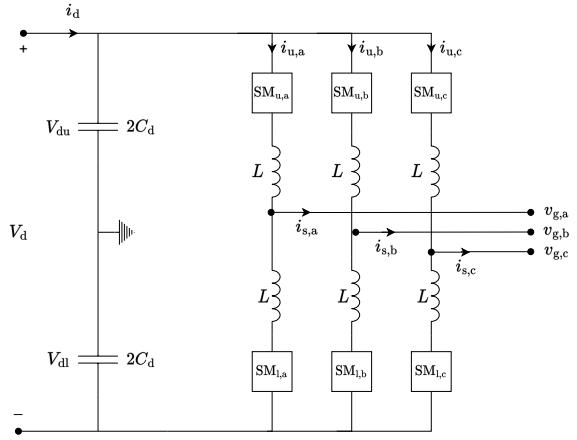


Figure 3.2: MMC model for DC bus dynamics.

Using Equation (3.22) for the upper and lower arm, and substituting Equation (3.6) gives the DC bus dynamics as can be found in Equation (3.23).

$$C_{\mathrm{d}}\frac{dv_{\mathrm{d}}}{dt} = i_d - \sum_{k=abc} i_{\mathrm{c,k}} \approx i_d - 3i_{\mathrm{c}} \tag{3.23}$$

Second, the sum capacitor voltage dynamics of Equation (3.19) and (3.20) are used to define Equation (3.24).

$$\frac{C}{N}\frac{d(v_{\mathrm{cu}}^{\Sigma} + v_{\mathrm{cl}}^{\Sigma})}{dt} = \frac{C}{N}\frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = n_{\mathrm{u}}\left(\frac{i_{\mathrm{s}}}{2} + i_{\mathrm{c}}\right) + n_{\mathrm{l}}\left(\frac{-i_{\mathrm{s}}}{2} + i_{\mathrm{c}}\right) \tag{3.24}$$

Next the ideal insertion indices are used for n_{u} and n_{l}, as later discussed in Section 3.5. The result of the substitution is given in Equation (3.25). In this equation the circulating voltage reference $v_{\mathrm{c}}^{*} = V_{\mathrm{d}}/2$ is used.

$$\frac{C}{N}\frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = -\frac{v_{\mathrm{s}}^{*} i_{\mathrm{s}}}{V_{\mathrm{d}}} + i_{\mathrm{c}} \tag{3.25}$$

The time average of the $v_{\mathrm{s}}^{*} i_{\mathrm{s}}$ term in Equation (3.25), represents the AC side per-phase power of the MMC. Using this observation Equation (3.25) can be simplified to Equation (3.26).

$$\frac{C}{N}\frac{d\overline{v_{\mathrm{c}}^{\Sigma}}}{dt} = -\frac{P}{3V_{\mathrm{d}}} + i_{\mathrm{c}} \tag{3.26}$$

Finally, combining Equation (3.23) and Equation (3.26) gives Equation (3.27) which provides the dynamic DC side model of the MMC. Note that the average leg sum capacitor voltage $\overline{v_{\mathrm{c}}^{\Sigma}}$ is assumed to be fixed at the reference of $2V_{\mathrm{d}}$. Analysing Equation (3.27), it can be concluded that for a practical implementing of the MMC, most fluctuations in the DC link voltage are dampened by the submodule capacitors as $C >> C_{\mathrm{d}}$.

$$\left(C_{\mathrm{d}} + \frac{6C}{N}\right)\frac{dV_{\mathrm{d}}}{dt} = C_{\mathrm{d}}'\frac{dV_{\mathrm{d}}}{dt} = i_d - \frac{P}{V_{\mathrm{d}}} \tag{3.27}$$

3.1.3 DC and AC side models

As introduced in Chapter 1, the MVDC distribution link is characterised by the back-to-back configuration of two MMCs. These MMCs each interact with an AC network and the DC distribution line. Therefore, to obtain the dynamic model of the MVDC distribution link, a model is required for both the DC transmission line and the AC grid.

The DC transmission line model is derived from Telegrapher's equations and the associated distributed components model in Figure 3.3 [27]. In this figure R_{x} is the distributed resistance, L_{x} is the distributed inductance, C_{x} is the distributed capacitance and G_{x} is the distributed conductance. However, as the transmission line is operated at DC, with separated supply and return lines, the distributed capacitance and conductance are negligible. Therefore the DC transmission line model can be simplified to a series connection of a lumped inductance L_{l} and a lumped resistance R_{l} as shown in Figure 3.4.

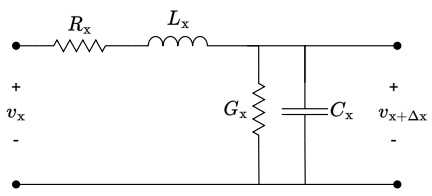


Figure 3.3: Distributed components model.

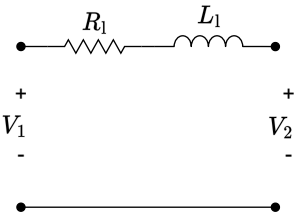


Figure 3.4: Simplified DC transmission line model.

The simplified model of a three-phase AC system is presented in Figure 3.5. In this model, the Wye configured three-phase grid voltages $v_{\text{gr,abc}}$ are connected via RL branches to the AC terminals of the modular multilevel converter. The three-phase voltages are assumed to be a well-balanced three-phase system: the three phases have equal magnitudes and their phases differ by 120 degrees. Furthermore, only the fundamental positive sequence component is present in v_{gr}. Equation (3.28) presents the expression of the three phases voltages.

$$\begin{aligned} v_{\text{gr,a}} &= \hat{V}_{\text{g}} * cos(\omega_1 t) \\ v_{\text{gr,b}} &= \hat{V}_{\text{g}} * cos\left(\omega_1 t - \tfrac{2}{3}\pi\right) \\ v_{\text{gr,c}} &= \hat{V}_{\text{g}} * cos\left(\omega_1 t - \tfrac{4}{3}\pi\right) \end{aligned} \tag{3.28}$$

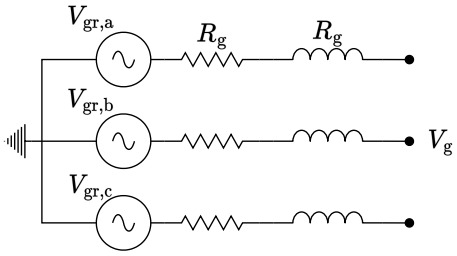


Figure 3.5: The simplified model of a three phase AC grid.

3.2 Control overview

After establishing the dynamic models, the MMC control structure can be derived. As mentioned in the introduction of this chapter, the control strategy becomes a fundamental part of the operation of the converter. This is because the MMC has complex internal dynamics and inherent instabilities that must be adequately regulated. The control module defines the upper and lower arm insertion indices $n_{\text{u,l}}$ for the three phases (a,b,c) such that the MMC establishes the desired output current, circulating current, active and reactive power, DC link voltage, and is synchronised with the three-phase grid. As mentioned in Section 3.1.1, the MMC controller considers the N arm submodules as a single submodule string, thus ignoring the individual devices. This was suggested to create a control hierarchy between the modulator and the controller. Whereas the modulator is designed to operate on an individual device level, the controller assumes proper balancing of the submodule capacitor voltages inside an arm.

To obtain the intended operation, multiple circuit quantities are regulated, which is achieved using subcontrol modules. The complete block diagram of the MMC control is provided in Figure 3.6. This figure indicates the set of subcontrol modules that make up the MMC controller together with its in and outputs. Another crucial aspect of the controller is the measurement block. This block represents the Analog-to-Digital Conversion (ADC) of the measured circuit quantities. These signals are then used as feedback in the control modules. The MMC control structure discussed in the remained of this chapter is analogous to the one proposed in [11].

First, consider the voltage control module. This module defines the arm insertion indices $n_{\text{u,l}}$ based on the reference the internal voltage v_{c}^* and the output voltage reference v_{s}^*. The output of the voltage control module is directly used in the MMC modulator to synthesise these reference voltages. The second control module, the vector output current control, determines the output voltage reference v_{s}^* to eliminate any error in the output current $i_{\text{s}} - i_{\text{s}}^*$. This is achieved using a closed-loop control structure. The third control module, the energy balancing control, defines the internal voltage reference v_{c}^* based on the measured circulating current i_{c}. The module forces i_{c} to its reference using a closed-loop implemented circulating current controller. The reference of i_{c} is generated in the arm-leg energy balancing control, which tries to enhance the output performance of the MMC by controlling the average arm capacitor voltages. The last

control module in the MMC control is the higher-level control. The higher-level control performs three sub-tasks which are divided over three smaller control modules. The first of which controls the AC-side active and reactive power. This module uses an open-loop control structure to define the output current reference i_s^* in order to achieve the active power reference P^* and reactive power reference Q^*. Besides this sub-module, the higher level control contains a Phase-Locked Loop (PLL). The PLL determines the transformation angle θ from the measured three-phase grid voltage $v_{g,abc}$. This angle is later used for direct-quadrature transformations. The last sub-module, the DC link voltage control determines the active power reference P^* based on the error in the DC link voltage $V_d - V_d^*$. Note that the active power reference P^* of the DC link voltage control replaces the one of the active and reactive power control. Generally, in a DC link application, one of the MMCs regulates the DC link voltage V_d and the other the DC link current i_d (and thus the active power P).

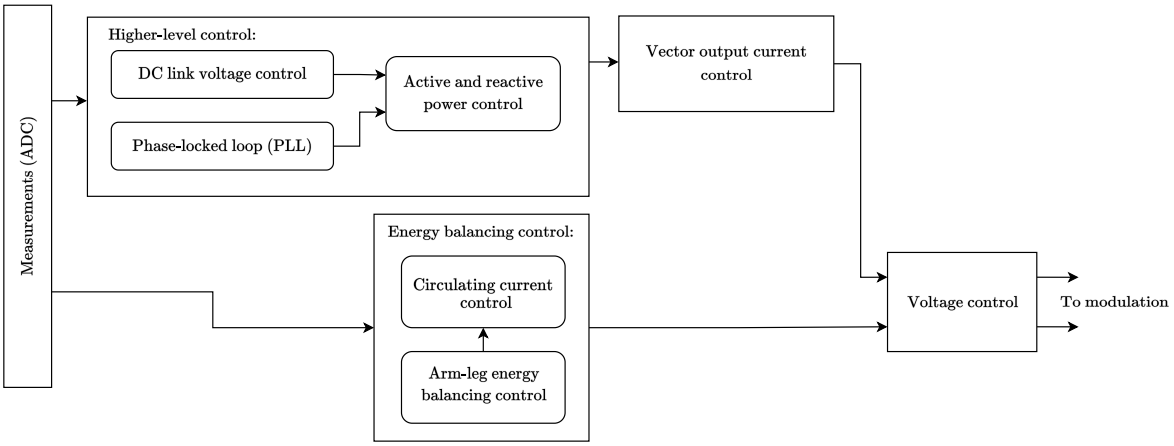


Figure 3.6: Schematic block diagram of the MMC control system.

3.3 Vector output current control

The first part of the MMC control system that is discussed is the vector output current control. Recall that the output current i_s is defined as the difference between the upper arm and lower arm current as in Equation (3.5). The task of this controller is to regulate the output current by defining the reference of the output voltage v_s^*. This is achieved by utilising the difference between the measured output current i_s and the reference output current i_s^*. The output current control is based on the dynamic relation provided in Equation (3.18). This equation can be redefined as the plant model in Equation (3.29). Note that the dependency on the grid voltage v_g in Equation (3.29) can be reduced by implementing a feedforward of the measured grid voltage v_g in the controller.

$$i_s = \frac{2}{(s + j\omega_1)L + R}(v_s - v_g) \tag{3.29}$$

To achieve control of the output current a PI controller is used in a closed-loop control configuration. The block diagram of the output current controller is provided in Figure 3.7. Where the output voltage reference v_s^{*0} is defined according to the control law as in Equation (3.30). In this equation the input error is defined as $e = i_s^* - i_s$. Note that in Equation (3.30) the quantities: i_s, i_s^*, v_a and v_s^* are space vectors that are provided in the dq-reference frame (or synchronous reference frame). This means that the fundamental frequency rotation is removed from the space vectors and thus fundamental frequency components pre-transformation are seen static afterwards.

$$v_s^{*0} = K_p e + \frac{K_0}{s} e' + \frac{\alpha_f}{s + \alpha_f} v_a + \frac{j\omega_1 L}{2} i_s \tag{3.30}$$

Equation (3.30) is composed of several terms. The first term, $K_p e$, implements the proportional part of the PI controller. The second, $K_0 e'/s$, implements the integral part of the PI controller. The proportional

gain K_p can be selected by first assuming that the arm resistance R is small compared to ωL and that $K_0 = 0$. Then define α_c as the closed-loop bandwidth of the system. Where α_c is chosen small compared to angular switching frequency ω_s to prevent switching transients from disturbing the control. Thus the closed-loop bandwidth is limited $\alpha_c \leq \frac{\omega_s}{10}$. The proportional gain K_p can then be defined as in Equation (3.31).

$$K_p = \frac{\alpha_c L}{2} \tag{3.31}$$

For the selection of the integral gain K_0 of PI controller, Equation (3.32) is used. In this equation, K_0 is defined as a function of the integrator bandwidth α_0 and the proportional gain K_p. The integrator bandwidth is selected smaller than the one of the proportional part, $\alpha_0 \ll \alpha_c$. This is done to maintain the closed-loop bandwidth of the system when integral action is added. Note that a large value of α_0 results in faster reference tracking of i_s^* with a zero steady state error. However, a too-large α_0 gives undesired oscillatory behaviour, poor robustness and possibly instabilities [28].

$$K_0 = 2\alpha_0 K_p \tag{3.32}$$

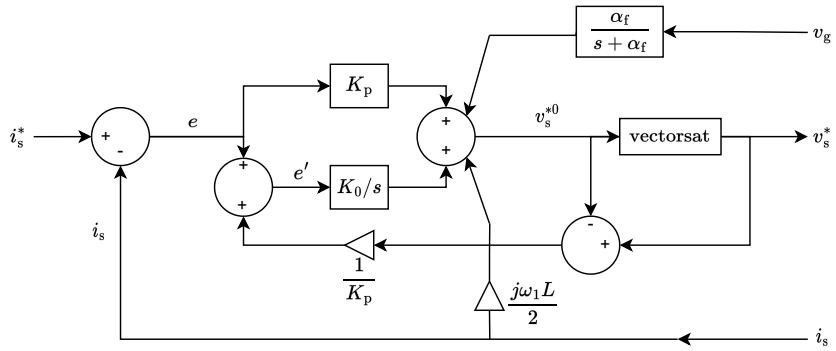


Figure 3.7: Block diagram of the vector output current controller.

As can be concluded from Equation (3.29), the output current i_s depends on the difference between the MMC output voltage v_s and the grid voltage v_g. As a result, a drop in the grid voltage due to e.g. a grid fault, causes an increase in i_s. In order to cancel the dependency between v_g and i_s the third term in Equation (3.30) is added. This term implements a feedforward of the measured grid voltage v_g, to oppose the impact of grid voltage changes. However, the measured grid voltage does contain undesired harmonics elements, which would inject high frequency disturbances into v_s^*. To eliminate these harmonics a first order Low-Pass Filter (LPF) is implemented, with a bandwidth α_f. The transferfunction of this filter is provided in Equation (3.33).

$$H_a(s) = \frac{\alpha_f}{s+\alpha_f} \qquad with\ \alpha_f < \alpha_c \tag{3.33}$$

The final term in Equation (3.29), $j\omega_1 L/2$, is used to remove the cross-coupling between the direct and quadrature axis. The cross-coupling is introduced in the dynamic model of Equation (3.29) by the $-\frac{j\omega_1 L}{2} i_s$ term. By adding the inner positive feedback of $\frac{j\omega_1 L}{2} i_s$ to the controller, the cross-coupling is removed.

The output voltage reference v_s^{*0} defined in Equation (3.29) can exceed the maximum output voltage set for v_s. Note that the magnitude of v_s is always limited by the DC link voltage V_d. Therefore, v_s^{*0} is saturated to define a reachable output voltage reference v_s^*. The saturation is performed using vector saturation, in which the phase of v_s^{*0} is maintained, and only the magnitude is reduced to fit the limit. One drawback of the output saturation is that windup will occur in the integrator. If the output voltage operates in prolonged saturation, the saturation errors accumulate on the integrator. By accumulating these errors,

the time spent to unwind the integrator becomes more extensive. This negatively impacts the reference tracking performance of the output current controller. Therefore, the controller is implemented with an anti-windup system, which performs back-calculation in accordance with Equation (3.34).

$$e' = e + \frac{1}{K_\mathrm{p}} \left(v_\mathrm{s}^* - v_\mathrm{s}^{*0} \right) \tag{3.34}$$

As mentioned, the output current control the uses space vectors: i_s, i_s^*, v_g and v_s^* in the dq-reference frame. However, the measured quantities as i_s and v_g are obtained as three phase vectors and the output reference v_s^* should be provided as a three phase vector. Therefore the abc to dq transformation is used as provided in Figure 3.8. Note that the transformation angle θ is provided by the PLL.

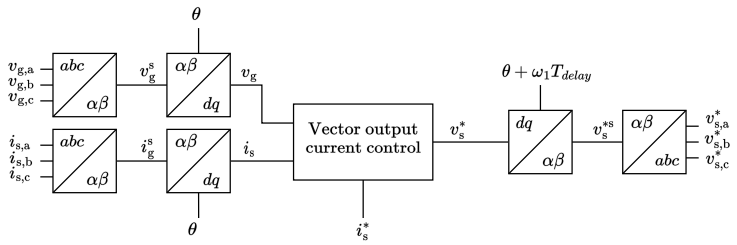


Figure 3.8: Vector output current control input and output transformations.

3.4 Energy balancing control

The energy balancing controller, is the second sub-control module that is part of the MMC controller. The task of this controller is to define the internal voltage reference v_c^* in order to regulate the circulating current i_c. The reference of the circulating current i_c^*, is constructed to balance the energies of the MMC at the desired set-point. Recall that the circulating current is defined as the average of the upper and lower arm current as in Equation (3.6). As the energy balancing control has to execute two separate tasks the controller can be split into:

- The circulating current control: defines the internal voltage reference v_c^* to regulate the circulating current i_c to its reference i_c^*.
- The arm-leg energy balancing control: defines the circulating current reference i_c^* in order to regulate the total and imbalance energy of the MMC legs.

3.4.1 Circulating current control

As defined in [29], uncontrolled circulating currents are unfavourable to the operation of the MMC. AC components in i_c result in increased arm currents $i_\mathrm{u,l}$. This in turn increases conduction and switching losses, reducing the operational efficiency of the MMC. Besides, increased arm currents cause a need for larger component ratings and reduce the lifespan of the converter. Limiting the circulating currents by the means of control can thus significantly increase the performance and reliability of the MMC. The circulating current controller is used to control i_c and is based on the dynamic relation provided in Equation (3.17). This equation can be redefined as the plant model in Equation (3.35). Equation (3.35) indicates that the circulating current is depends on both the internal voltage v_c and the DC link voltage V_d.

$$i_c = \frac{1}{sL+R} \left(\frac{V_\mathrm{d}}{2} - v_\mathrm{c} \right) \tag{3.35}$$

A simple way of limiting the circulating current that follows directly from Equation (3.35), is to increase the arm inductance L. This passive control technique, however, deteriorates the converter's dynamic

performance by creating a slower frequency response [29]. Furthermore, the implementation cost of the MMC is increased due to the larger arm inductance. Therefore an active circulating current controller is proposed to control the oscillations in i_c.

To control the circulating current in the MMC legs, a closed-loop control structure is used based on a PR controller. The block diagram of the controller is provided in Figure 3.9, where the design of the controller is based on the control law given in Equation (3.36). The control law provides the internal voltage reference as a function of the circulating current tracking error and the DC link voltage. Note that in the circulating current control the quantities: i_c, i_c^*, and v_c^* are space vectors provided in the $\alpha\beta$-reference frame. This means that the fundamental frequency ω_1 rotation of the three-phase quantities is maintained in the $\alpha\beta$ space vector components.

$$v_c^* = -R_a \left(1 + \frac{2\alpha_2}{s^2 + (2\omega_1)^2}\right)(i_c^* - i_c) + \frac{V_d}{2} - Ri_c^* \tag{3.36}$$

Similar to the output current control, the control law (3.36) is composed of several terms. The first term, $-R_a(i_c^* - i_c)$, implements the proportional part of the PR controller. The proportional gain R_a can be selected by the bound: $R \ll R_a < K_p$. This rule applies as R_a provides damping of parasitic components in v_c, though the damping must be less aggressive than the output current control [11]. The second term in Equation (3.36) implements the resonant part of the PR controller. The resonant part is tuned for the double-line frequency component $2\omega_1$, as the internal voltage v_c contains significant parasitic components at this frequency. Therefore, resonant action is implemented instead of integral action as was used in the output current controller. The bandwidth of the resonant part α_2 can be selected using the constraint $\alpha_2 < \omega_1$.

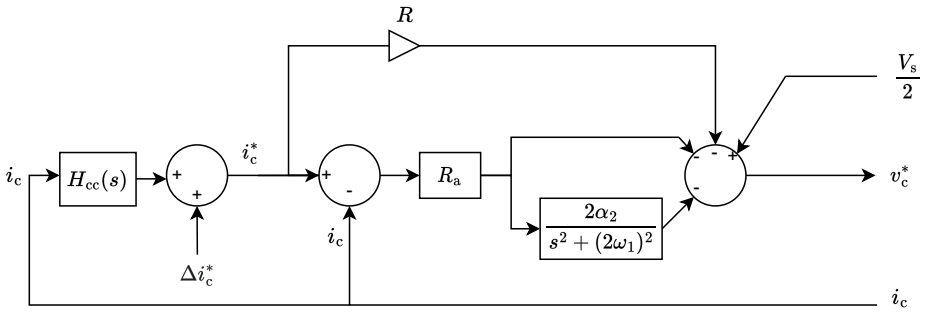


Figure 3.9: Block diagram of the circulating current controller.

From Equation (3.35) can be concluded that the circulating current i_c depends on the difference between the internal voltage and half the DC link voltage. As a result, a change in V_d directly impacts the circulating current. To remove the dependency of i_c on the DC link voltage, a feed-forward of $V_d/2$ is added to the control law. In addition, to compensate for the voltage drop across the arm resistance R the term $-Ri_c^*$ is added in Equation (3.36).

Besides the PR control, Figure 3.9 also shows the generation of the circulating current reference i_c^*. The generation of i_c^* is prescribed in Equation (3.37), where i_c is the measured circulating current and Δi_c^* an optional increment.

$$i_c^* = \left(\frac{\sqrt{2}\alpha_1^2}{s^2 + \sqrt{2}\alpha_1 s + \alpha_1^2}\right) i_c + \Delta i_c^* \tag{3.37}$$

In this equation a second-order Butterworth low pass filter $H_{cc}(s)$ is used to prevent the high frequency components of i_c from entering i_c^*. By choosing the LPF bandwidth $\alpha_1 < \omega_1$, only the DC component of i_c is present in the reference i_c^*. The main reason for this structure lies in the output current control. The

output current control of the MMC controls the output current i_s of the three phases. If is is assumed that i_s is set according to the higher-level control, then the DC-link power and DC link voltage are controlled by the two MMCs, as seen in Section 3.6. So the DC side current i_d is fixed by the output current control which imposes a controlled DC component of i_c when the MMC operates under balanced gird conditions. Now to prevent the output current controller and circulating current control from both controlling the DC component of i_c this component is removed from the circulating current control. This is simply achieved passing the measured DC component of i_c on to the reference.

3.4.2 Arm-leg energy balancing control

The second part of the energy balancing control is the arm-leg energy balancing control. This controller is used to alter the circulating current reference i_c^* to better balance the arm capacitor voltages. The controller alter i_c^* via the increment Δi_c^* in Equation (3.37) and Figure 3.9. In the arm-leg energy balancing control, the arm capacitor voltages are not directly balanced, but this is performed via the total and imbalance energies. To define these two energies, first, consider the upper and lower arm energies as defined in Equation (3.38). The upper and lower arm energies are linearly proportional to the submodule capacitance C and depend on the square of the arm sum capacitor voltage $v_{cu,l}^{\Sigma}$.

$$W_u = \frac{C\left(v_{cu}^{\Sigma}\right)^2}{2N} \qquad W_l = \frac{C\left(v_{cl}^{\Sigma}\right)^2}{2N} \tag{3.38}$$

The total energy W_Σ and imbalance energy W_Δ can then be defined as the sum and difference of the arm energies, respectively. This is indicated in Equation (3.39). The dynamics of the total and imbalance energy can be derived from the sum capacitor voltage dynamics in Equation (3.19). The resulting dynamic equations are provided in Equation (3.40).

$$W_\Sigma = W_u + W_l \qquad W_\Delta = W_u - W_l \tag{3.39}$$

$$\frac{dW_\Sigma}{dt} = 2v_c^* i_c - v_s^* i_s \qquad \frac{dW_\Delta}{dt} = v_c^* i_s - 2v_s^* i_c \tag{3.40}$$

For the ideal performance of the MMC, the submodule capacitor voltages $v_{cu,l}^{i}$ are operated at the value V_d/N. So to balance the sum capacitor voltages at the ideal value, the upper and lower arm energies must have a reference value of $CV_d^2/2N$. Therefore, the total arm energy W_Σ and imbalance arm energy W_Δ have references as given in Equation (3.41).

$$W_{\Sigma 0} = \frac{CV_d^2}{N} \qquad W_{\Delta 0} = 0 \tag{3.41}$$

According to the analysis, the balancing of the sum capacitor voltages $v_{cu,l}^{\Sigma}$ at V_d is equivalent to balancing the total and imbalance energies at $W_{\Sigma 0}$ and $W_{\Delta 0}$, respectively. To perform the arm-leg energy balancing control the control circuit given in Figure 3.10 is used.

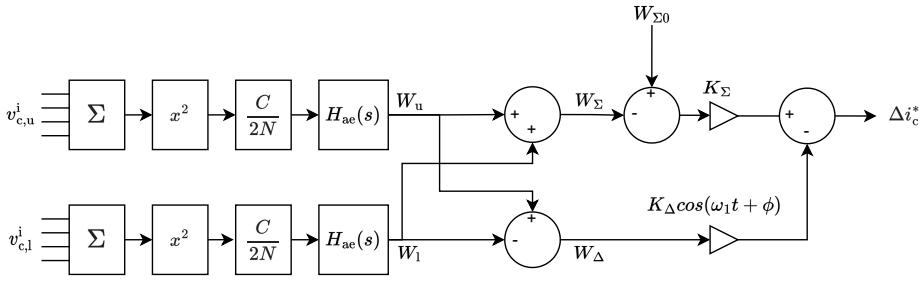


Figure 3.10: Block diagram of the arm energy control.

This control circuit defines current increment Δi_c^* based on the submodule capacitor voltages $v_{cu,l}^i$. Equation (3.42) reflects the output of the controller. In this equation $H_{\text{ae}}(s)$ is a second order Butterworth low pass filter that blocks all voltage components above ω_1.

$$\Delta i_c^* = K_\Sigma(W_{\Sigma 0} - H_{ae}(s)W_\Sigma) - K_\Delta(H_{ae}(s)W_\Delta) * cos(\omega_1 t + \phi) \tag{3.42}$$

3.5 Voltage control

Once the output voltage reference v_{s}^* and internal voltage reference v_{c}^* are provided by their control modules the voltage control can be applied. The voltage control defines the arm insertion indices $n_{\text{u,l}}$ such that the generated internal voltage v_{c} and output voltage v_{s} approximate their references. The output of the voltage control module is directly used in the MMC modulator to synthesise the output.

Following [11], there are multiple ways of implementing the voltage control module. This application uses direct voltage control because of its simplicity and stability. In contrast to the other voltage control methods proposed in [11], direct voltage control is inherently stable and does not require measurements of the arm capacitor voltages. This greatly reduced the complexity of the voltage control and energy balancing module. The direct voltage control implementation is based on Equation (3.43) and presented as a block diagram in Figure 3.11.

$$n_{\text{u}} = \frac{v_{\text{c}}^* - v_{\text{s}}^*}{V_{\text{d}}} \qquad n_{\text{l}} = \frac{v_{\text{c}}^* + v_{\text{s}}^*}{V_{\text{d}}} \tag{3.43}$$

Combining Equations (3.3), (3.9) and (3.10) the expression of the ideal insertion indices can be found. The resulting indices are defined in Equation (3.44). By comparing Equations (3.43) and Equation (3.44) it can be concluded that, with direct voltage control the assumption is made that the upper/lower sum capacitor voltage $v_{\text{cu,l}}^\Sigma$ is constant and equal to the DC link voltage V_{d}. This assumption is feasible as the energy balancing control regulates the arm capacitor voltages. Although the direct voltage control defines insertion indices that deviate from the ideal values, the control simplification offsets the mismatch.

$$n_{\text{u}} = \frac{v_{\text{c}}^* - v_{\text{s}}^*}{v_{\text{cu}}^\Sigma} \qquad n_{\text{l}} = \frac{v_{\text{c}}^* + v_{\text{s}}^*}{v_{\text{cl}}^\Sigma} \tag{3.44}$$

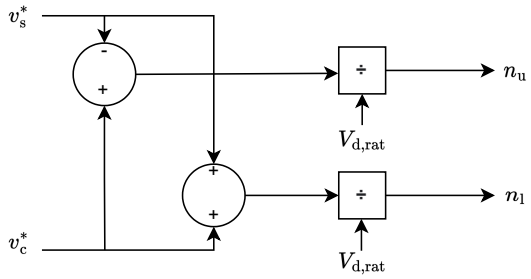


Figure 3.11: Block diagram of the voltage control module.

3.6 Higher-level control

The final segment of the MMC control system is the higher-level control. As mentioned in Section 3.2, the higher-level control comprises three smaller control modules: the active and reactive power control, the phase-locked loop and the DC link voltage control. The higher-level control uses the operational parameters and MMC measurements to define the output current reference i_{s}^* and transformation angle θ. These two quantities are used in the vector output current control.

3.6.1 Active and reactive power control

The active and reactive power control module controls the active and reactive power that flows through the AC-side of the MMC. The module first defines the active power reference P^* and reactive power reference Q^* based on the defined load percentage of the rated power and the desired power factor. The reference P^* and Q^* are defined as in Equation (3.45) and (3.46), respectively.

$$P^* = pf * \%load * S_{max} \tag{3.45}$$

$$Q^* = \sin(\arccos(pf)) * \%load * S_{max} \tag{3.46}$$

The output of the active and reactive power control is the output current reference i_s^*. So if P^* and Q^* are provided, then the output current reference is found according to Equation (3.47). Note that this control law implements the active and reactive power control in an open-loop structure. Before providing i_s^* to the vector output current control, vector saturation is applied to limit the magnitude of i_s^*.

$$i_{s,d}^* = \frac{2P^*}{3|v_g|} \qquad i_{s,q}^* = \frac{-2Q^*}{3|v_g|} \tag{3.47}$$

3.6.2 Phase-locked loop

The phase-locked loop (PLL) determines the transformation angle θ which is required for grid synchronisation of the converter. The PLL is implemented as a feedback loop for the grid voltage v_g around the *abc* to *dq* transformation. θ is then provided as an input to the vector output current control. The control circuit of the PLL is provided in Figure 3.12. In this circuit, the grid voltage $v_{g,abc}$ is first transformed to the $\alpha\beta$-reference frame. Second, v_g^s is transformed to the *dq*-reference frame, provided the current value of θ. The output v_g, is then filtered with a second-order Butterworth low pass filter $H_p(s)$ to retrieve the fundamental grid frequency component of $v_{g,abc}$ at DC: v_g^f.

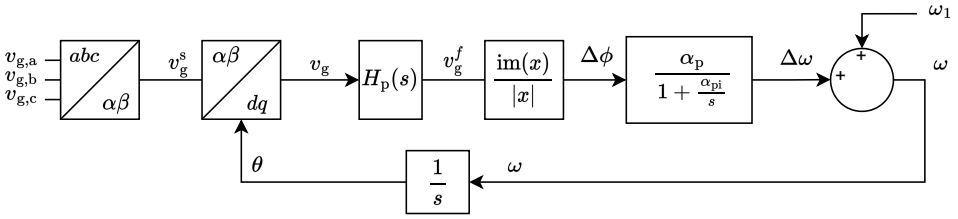


Figure 3.12: Block diagram of the phase locked loop.

After filtering using $H_p(s)$, the most dominant signal that remains is the positive sequence line-frequency component of $v_{a,abc}$. This component of v_g^f is given in expression (3.48).

$$v_g^f = \hat{V}_+ e^{j(\omega_1 t + \phi_+)} * e^{-(j\omega_1 t + \hat{\phi}_+)} = \hat{V}_+ e^{j(\phi_+ - \hat{\phi}_+)} \tag{3.48}$$

After filtering, the transformation angle error $\Delta\phi$ can be found as in Equation (3.49).

$$\frac{Im\{v_g^f\}}{|v_g^f|} = sin(\phi_+ - \hat{\phi}_+) \approx \phi_+ - \hat{\phi}_+ = \Delta\phi \tag{3.49}$$

To make sure that the transformation angle θ accurately presents the grid angle, $\Delta\phi$ is controlled to zero using a close loop control system. This is done using a PI controller with proportional gain α_p and integral bandwidth α_{pi}. Proportional gain α_p is selected below the fundamental frequency, $\alpha_p < \omega_1$. The integral bandwidth α_{pi} is selected slightly smaller than the proportional gain, $\alpha_{pi} < \alpha_p/2$. The PLL filter implemented by the second-order Butterworth low pass filter $H_p(s)$ is selected with a bandwidth larger

than the proportional gain, $\alpha_p < \alpha_b < 2\omega_1$. The output of the PI controller is then combined with the fundamental frequency component and integrated to create the transformation angle θ. The closed-loop PLL system makes sure that under steady-state conditions the reference tracking error of θ becomes zero

3.6.3 DC link voltage control

The last element of the higher-level control is the DC link voltage control. This module defines an active power reference P^* based on the difference between the DC link voltage V_d and its reference V_d^*. Note that both the DC link voltage control and active power control define a reference P^*. Depending on the operation of the MMC, the active power reference P^* can be taken from either the DC link voltage or the active power control. Generally, in a DC link application, one MMC regulates the DC link voltage V_d while the other controls the DC current i_d.

For the DC link voltage control, the DC-side MMC dynamics are used as defined in Equation (3.28). From this equation becomes clear that the DC link voltage changes because of a mismatch between supplied and drawn DC link current. Multiplying both sides with v_d gives the dynamic relation of the DC link energy W_d as in Equation (3.50). In this equation P_d and P are the DC-side and AC-side active powers, respectively.

$$\frac{dW_d}{dt} = P_d - P \tag{3.50}$$

According to Equation (3.50) any mismatch in the DC-side and AC-side power accounts for a change in the DC link energy. To retain constant energy that matches the reference link voltage V_d^*, the DC link voltage control, provided in Figure 3.13 can be used. Figure 3.13 indicates that the reference power P^* is created using a PI controller. Note that the energy mismatch is determined using Equation (3.51). In which $H_p(s)$ is a low pass filter similar to the one explained in Section 3.6.2.

$$\Delta W = \frac{1}{2}C_d'(H_p(s) * V_d)^2 - \frac{1}{2}C_d'V_d^{*2} \tag{3.51}$$

Afterwards a PI controller is applied with proportional gain α_d and integral bandwidth α_{di}. For this PI controller the bandwidth can be chosen small, with $\alpha_d < \omega_1$ and $\alpha_{di} < \alpha_d/2$. This is done to prevent control interaction with the output current controller. Another feature that is present in Figure 3.13 is the anti-windup. Similar to Section 3.3, vector saturation is applied to limit the reference output current $i_{s,d}^{*0}$ to $i_{s,d}^*$. To eliminate the windup on the integrator an anti-windup circuit is installed.

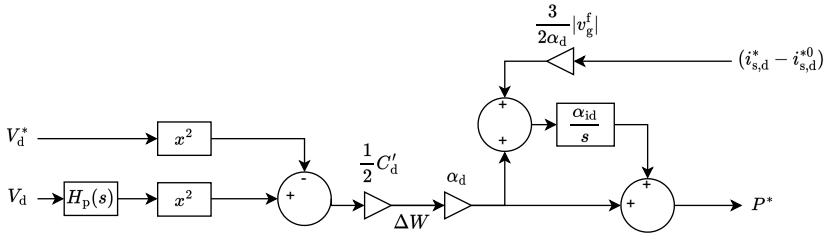


Figure 3.13: Block diagram of the DC link voltage control.

Chapter 4

Analytic DC Link Voltage Enhancement

The MVDC distribution link is, in current applications, operated at a fixed rated DC voltage, set through one of the MMCs. Though, as proposed in Section 1.1, the link can be operated at an enhanced DC voltage V_d that exceeds the rated value V_{dr} while encountering the same submodules stresses. The raised DC link voltage is thus achieved while maintaining the same average stored energy in the MMCs, ensuring the preservation of reliability and performance over long-term operation. The increment in the DC link voltage is used to enhance the performance of the distribution link. Operating at the rated link current, improves the power transfer capacity of the MVDC distribution link, e.g. during congestions. Alternatively, when operating at rated power, reduced operating currents improve the conversion efficiency of the link. As the maximum DC link enhancement is heavily dependent on the operational conditions of the MMC, the determination of the link voltage enhancement limit is important for both the dynamic operation and control of the MMC. Therefore, this chapter is aimed toward the analytical determination of the DC link voltage enhancement boundary for the back-to-back operation of MMCs.

4.1 Enhancement boundary

To determine the boundary of the DC link voltage enhancement, first, the limiting constraint is defined. As mentioned in [5], the average submodule capacitor voltage can differ from the DC link voltage provided that the sum capacitor voltage v_{cu}^{Σ} is larger than the arm voltage v_u for every time instant t. This provides the constraint that is given in Equation (4.1). This constraint represents a physical limitation of the MMC, where v_u can never be larger than v_{cu}^{Σ}. If the reference of v_u exceeds v_{cu}^{Σ}, the generated arm voltage saturates at the sum capacitor voltage, causing significant output harmonics at the AC-side of the MMC. Note that the expression must hold for both the upper and the lower arm for all three phases (a,b,c). So while keeping the MMC energies within the rated limits, the DC link voltage can be raised as long as Equation (4.1) is satisfied.

$$v_{cu}^{\Sigma} - v_u \geq 0 \tag{4.1}$$

To visualise the enhancement process Figure 4.1 can be used. This figure shows the sum capacitor voltage v_{cu}^{Σ} together with two upper arm voltages v_u as a function of $\omega_1 t$. It is observed that the ripple in the sum capacitor voltage creates a spacing between v_{cu}^{Σ} and v_u. This space can be used for the biasing the arm voltage without violating constraint (4.1) (from $k_d = 1$ to $k_d = 1.08$). Following Equations (3.10) and (3.17), it can be concluded that an increment in the DC component of the arm voltage directly appears at the DC terminal. Thus biasing v_u increases V_d in steady state. Note that the DC voltage enhancement is limited by constraint (4.1) as the intersection of v_u and v_{cu}^{Σ} causes flattening of v_u. This introduces output harmonics as can be visualised in Figure 4.2. Note that in Figures 4.1 and 4.2 the DC link voltage enhancement is achieved while maintaining the average sum capacitor voltage $\overline{v_{cu}^{\Sigma}}$.

For the DC link voltage enhancement of the MMC, two quantities are of importance: the sum capacitor voltage v_{cu}^{Σ} and the upper arm voltage v_u. Both must be expressed analytically to determine a expression of the enhancement boundary. First, the analytical expression of the sum capacitor voltage is derived using the dynamic MMC model of Section 3.1. In this Section the phase-leg dynamics of the MMC were described using the four fundamental Equations (3.17)-(3.20). These were then evolved in Section 3.4 to the upper and lower arm energies W_u,W_l which then defined the total energy W_{Σ} and imbalance energy

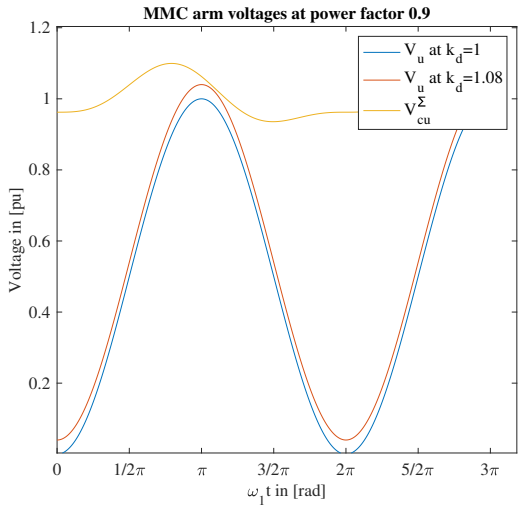


Figure 4.1: The sum capacitor voltage and upper arm voltage with and without DC enhancement.

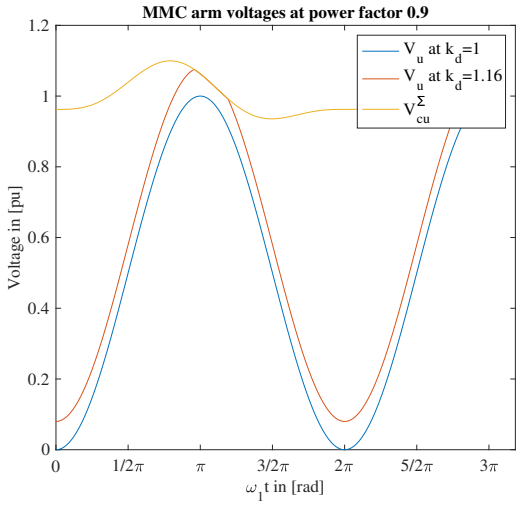


Figure 4.2: The sum capacitor voltage and upper arm voltage harmonic introduction.

W_Δ as in Equation (3.39). Using the ideal insertion indices, the dynamic behaviour of W_Σ and W_Δ is found as in Equation (3.40) and is re-listed in Equation (4.2).

$$\frac{dW_\Sigma}{dt} = 2v_c^* i_c - v_s^* i_s \qquad \frac{dW_\Delta}{dt} = v_c^* i_s - 2v_s^* i_c \tag{4.2}$$

For the DC link enhancement, assumptions are made for the DC and AC-side quantities. These assumptions are listed in Equation (4.3).

$$\begin{aligned} v_c^* &= \tfrac{1}{2}V_d \\ i_c &= \text{DC component} \\ v_s^* &= \hat{V}_s \cdot \cos(\omega_1 t) \\ i_s &= \hat{I}_s \cdot \cos(\omega_1 t - \phi) \end{aligned} \tag{4.3}$$

Now using Equation (4.2) with the assumptions of Equation (4.3), the dynamic behaviour of the total energy W_Σ and imbalance energy W_Δ can be found as in Equation (4.4) and (4.5) respectively.

$$\frac{dW_\Sigma}{dt} = V_d i_c - \frac{\hat{V}_s \hat{I}_s}{2}\cos(\phi) - \frac{\hat{V}_s \hat{I}_s}{2}\cos(2\omega_1 t - \phi) \tag{4.4}$$

$$\frac{dW_\Delta}{dt} = \frac{V_d \hat{I}_s}{2}\cos(\omega_1 t - \phi) - 2\hat{V}_s i_c \cos(\omega_1 t) \tag{4.5}$$

In Equation (4.4), the $V_d i_c$ term indicates the DC-side power of a single phase. In addition, the $\frac{\hat{V}_s \hat{I}_s}{2}\cos(\phi)$ term in the equation indicates the per phase AC-side power. Because of the law of conservation of energy, these terms must be equal in steady state applications. Then performing a time integration on both equations, constructs the expressions of the total energy W_Σ and imbalance energy W_Δ as in Equations (4.6) and (4.7), respectively.

$$W_\Sigma = W_{\Sigma 0} - \frac{\hat{V}_s \hat{I}_s}{4\omega_1}\sin(2\omega_1 t - \phi) = W_{\Sigma 0} + \Delta W_\Sigma \tag{4.6}$$

$$W_\Delta = W_{\Delta 0} + \frac{V_d \hat{I}_s}{2\omega_1}\sin(\omega_1 t - \phi) - \frac{2\hat{V}_s i_c}{\omega_1}\sin(\omega_1 t) = W_{\Sigma 0} + \Delta W_\Delta \tag{4.7}$$

Recall from Section 3.4 that to operate at the ideal submodule capacitor voltage $v^{i}_{cu,l} = V_{\mathrm{d}}/N$, the total arm energy W_{Σ} and imbalance arm energy W_{Δ} have a reference as given in Equation (4.8).

$$W_{\Sigma 0} = \frac{CV_{\mathrm{d}}^2}{N} \qquad\qquad W_{\Delta 0} = 0 \tag{4.8}$$

Now following from Equation (3.39) the upper arm energy can be defined as in Equation (4.9). Then utilising the definition of Equation (3.38) gives the expression for the sum capacitor voltage v^{Σ}_{cu} in Equation (4.10).

$$W_{\mathrm{u}} = \frac{W_{\Sigma 0} + \Delta W_{\Sigma} + \Delta W_{\Delta}}{2} \tag{4.9}$$

$$v^{\Sigma}_{\mathrm{cu}} = \sqrt{\frac{2N}{C} W_{\mathrm{u}}} = \sqrt{\frac{N}{C}(W_{\Sigma 0} + \Delta W_{\Sigma} + \Delta W_{\Delta})} \tag{4.10}$$

This expression can be simplified to Equation (4.11).

$$v^{\Sigma}_{\mathrm{cu}} = V_{\mathrm{d}} \sqrt{1 + \frac{N}{CV_{\mathrm{d}}^2}(\Delta W_{\Sigma} + \Delta W_{\Delta})} \approx V_{\mathrm{d}} + \frac{N}{2CV_{\mathrm{d}}}(\Delta W_{\Sigma} + \Delta W_{\Delta}) \tag{4.11}$$

Note that the square root term in the equation is approximate by a linear expression of the ripple energies. This approximation is further justified in Appendix C.1, which elaborates on the limitations imposed through this assumption.

The second step in finding the DC link voltage enhancement boundary is the determination of the arm voltage v_{u} expression. The arm voltage caries half of the rated DC link voltage as a circulating voltage. Besides, both the upper and the lower arm voltage comprise the sinusoidal output voltage v_{s}. The upper arm voltage expression is defined in (4.12).

$$v_{\mathrm{u}} = \frac{V_{\mathrm{d}}}{2} - \hat{V}_{\mathrm{s}} \cdot \cos(\omega_1 t) \tag{4.12}$$

As proposed, the DC link voltage is increased beyond its rated value V_{dr} while maintaining the MMC energies at the rated value. The enhanced DC link voltage V_{d} can be expresses as a function of the rated voltage, using the enhancement factor k_d. This relation is provided in Equation (4.13).

$$V_{\mathrm{d}} = k_{\mathrm{d}} V_{\mathrm{dr}} \tag{4.13}$$

By substituting Equation (4.11) and (4.12) into the limiting constraint of Equation (4.1), the redefined constraint of Equation (4.14) can be found. Note that Equation (4.11) is substituted with the rated DC link voltage V_{dr}. This is important as the average arm energy must be maintained at the rated value when the DC link voltage is enhanced. In contrast, Equation (4.12) is substitute with the enhanced DC link voltage V_{d}. This higher DC component in the arm voltage is needed to achieve the enhanced DC link voltage.

$$V_{\mathrm{dr}} + \frac{N}{2CV_{\mathrm{dr}}}(\Delta W_{\Sigma} + \Delta W_{\Delta}) - \frac{k_{\mathrm{d}} V_{\mathrm{dr}}}{2} + \hat{V}_{\mathrm{s}} \cdot \cos(\omega_1 t) \geq 0 \tag{4.14}$$

Now substituting Equations (4.6) and (4.7) into this equation, results in Equation (4.15). Note that Equation (4.7) is substituted with the enhanced DC link voltage. This as the circulating voltage is directly proportional to the operating DC link voltage V_{d}.

$$V_{\mathrm{dr}} + \frac{N}{2CV_{\mathrm{dr}}}\left(-\frac{\hat{V}_{\mathrm{s}}\hat{I}_{\mathrm{s}}}{4\omega_1}\sin(2\omega_1 t - \phi) + \frac{k_{\mathrm{d}} V_{\mathrm{d}} \hat{I}_{\mathrm{s}}}{2\omega_1}\sin(\omega_1 t - \phi) - \frac{2\hat{V}_{\mathrm{s}} i_{\mathrm{c}}}{\omega_1}\sin(\omega_1 t)\right) - \frac{k_{\mathrm{d}} V_{\mathrm{dr}}}{2} + \hat{V}_{\mathrm{s}} \cdot \cos(\omega_1 t) \geq 0 \tag{4.15}$$

To simplify this expression Figure 4.1 can be used, which showed v_{cu}^{Σ} and v_u as a functions of $\omega_1 t$. Note that spacing between v_{cu}^{Σ} and v_u is most stringent near $\omega_1 t = \pi$. This indicates that constraint (4.1) would first be violated when $\omega_1 t = \pi$. This observation allows for a simplification of Equation (4.15) to Equation (4.16).

$$V_{dr} + \frac{N}{2CV_{dr}} \left(\frac{\hat{V}_s \hat{I}_s}{4\omega_1} \sin(\phi) + \frac{k_d V_d \hat{I}_s}{2\omega_1} \sin(\phi) \right) - \frac{k_d V_{dr}}{2} - \hat{V}_s \geq 0 \tag{4.16}$$

To further simplify the expression, $X_c = \frac{N}{C\omega}$ is defined as the arm impedance and the output voltage amplitude $\hat{V}_s$ is set at its maximum of $V_d/2$. This results in Equation (4.17).

$$V_{dr} + X_c \frac{\hat{I}_s}{2} \sin(\phi) \left(\frac{1}{4} + k_d \right) - k_d V_{dr} \geq 0 \tag{4.17}$$

Note that $k_d = 1$ corresponds to the operation at rated DC link voltage, and thus qualifies the minimum of the enhancement factors. Therefore, the DC link voltage enhancement region can be defined as in Equation (4.18). With $k_{d,max}$ defining the DC link enhancement boundary.

$$1 \leq k_d \leq \underbrace{1 + \frac{X_c \frac{\hat{I}_s}{2} \sin(\phi)}{V_{dr}} \left(\frac{1}{4} + k_d \right)}_{k_{d,max}} \tag{4.18}$$

4.2 Boundary interpretation

Equation (4.18) defined the limit of the DC link voltage enhancement. The boundary, $k_{d,max}$, can be computed by iteratively applying the equation. The result of the first four iterations is presented in Figure 4.3, where the enhancement factor k_d is initialised at 1. Figure 4.3 also contains the analytical limit of Equation (4.18). The calculation of $k_{d,max}$ in this figure is performed with $X_c = 8.68\Omega$ and $V_{dr} = 16.3kV$ in line with the MMC properties proposed in Appendix B.1. It can be concluded from Figure 4.3 that the DC link voltage enhancement boundary increases with a decrease in the power factor, when operating at the rated output current i_s. This observation suggests that the DC link enhancement depends on the operational reactive power of the MMC.

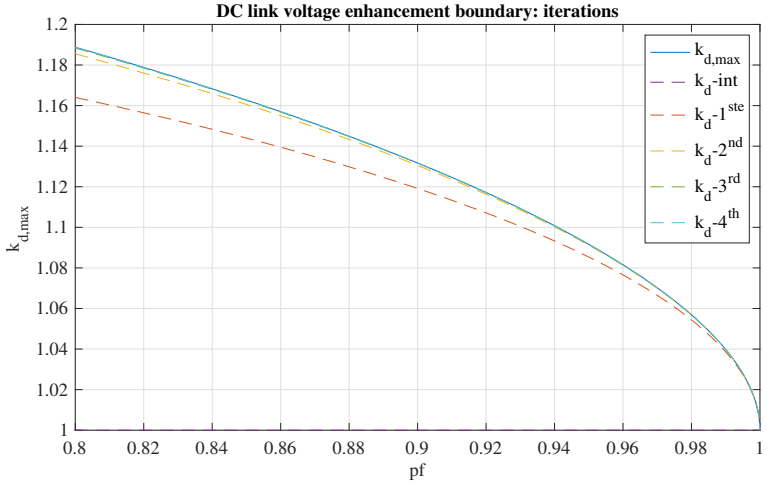


Figure 4.3: The maximum DC link voltage enhancement for different number of applied iterations.

This observation is substantiated by the closed form solution of Equation (4.18), provided in Equation (4.19). This equation indicates that the DC link voltage enhancement boundary depends on the rated DC link voltage V_{dr}, the arm impedance X_c, and the reactive power Q injected into the AC network.

$$1 \leq k_{\mathrm{d}} \leq \underbrace{\frac{6V_{\mathrm{dr}}^2 + QX_{\mathrm{c}}}{6V_{\mathrm{dr}}^2 - 4QX_{\mathrm{c}}}}_{k_{\mathrm{d,max}}} \tag{4.19}$$

The dependence of $k_{\mathrm{d,max}}$ and Q is illustrated in Figure 4.4, which shows the enhancement boundary as a function of the power factor for multiple apparent power levels expressed as a percentage of the rated operation. It can be seen that an increase in Q, either via the decrease in power factor or increase in apparent power, allows for a larger DC link voltage enhancement.

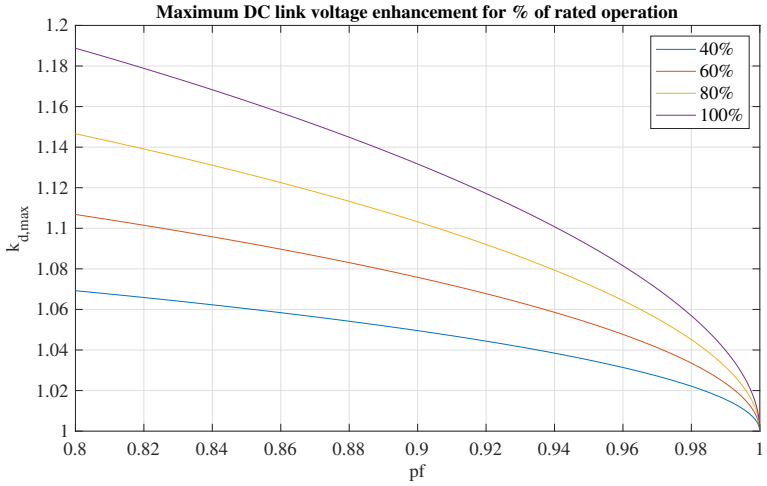


Figure 4.4: The maximum DC link voltage enhancement for different operating reactive energies.

The dependency of $k_{\mathrm{d,max}}$ and Q can also be interpret physically by using Equation (4.17). In this equation, $\frac{1}{2}\hat{I}_{\mathrm{s}} \sin(\phi)$ represents the reactive current component that flows through an MMC arm. Meanwhile, X_{c} characterises the arm impedance. As a result, the product of the two defines the voltage drop across the arm impedance due to the reactive arm current component. This voltage drop is later defined as the reactive voltage V_{rec} and is provided in Equation (4.20). If the voltage drop across the arm impedance is positive, then the DC component of the upper arm voltage $\frac{1}{2}k_{\mathrm{d}}V_{\mathrm{dr}}$ can be enhanced while maintaining V_{dr} as the average sum capacitor voltage. This all while not without violating constraint (4.1).

$$V_{\mathrm{rec}} = \frac{1}{2}X_{\mathrm{c}}\hat{I}_{\mathrm{s}} \sin(\phi) \tag{4.20}$$

In case the multilevel modular converter is operating at unity power factor $pf = 1.0$, so no reactive power is injected, the reactive voltage becomes zero. This corresponds to a situation were no DC link voltage enhancement $k_{\mathrm{d,max}} = 1$ can be obtained. If the injected reactive energy is made positive, $pf < 1.0$, V_{rec} increases. In a way, this positive reactive voltage V_{rec} creates the space for the upper arm voltage to be biased without intersecting the sum capacitor voltage. This is graphically illustrated in Figure 4.5 for three operating power factors. For illustration Figure 4.5 does neglect the saturation of v_{u} at v_{cu}^{Σ}. From this figure can be concluded that at time point $\omega_1 t = \pi$ the positive reactive voltage V_{rec}, allows for a DC link voltage enhancement $k_{\mathrm{d,max}} \geq 1$ when the operating power factor is bellow 1.0.

The dependency of $k_{\mathrm{d,max}}$ and V_{rec} can be further examined by redefining Equation (4.17) as Equation (4.21). In this equation V_{rec} presents the reactive voltage across the MMC arm.

$$V_{\mathrm{rec}}\left(\frac{1}{4} + k_{\mathrm{d}}\right) \geq (k_{\mathrm{d}} - 1)V_{\mathrm{dr}} \tag{4.21}$$

Equation (4.21) can be altered to obtain Equation (4.22). In this equation $V_{\mathrm{rec,pu}}$ is the normalised reactive voltage. Then solving this equation for k_{d} results in Equation (4.23).

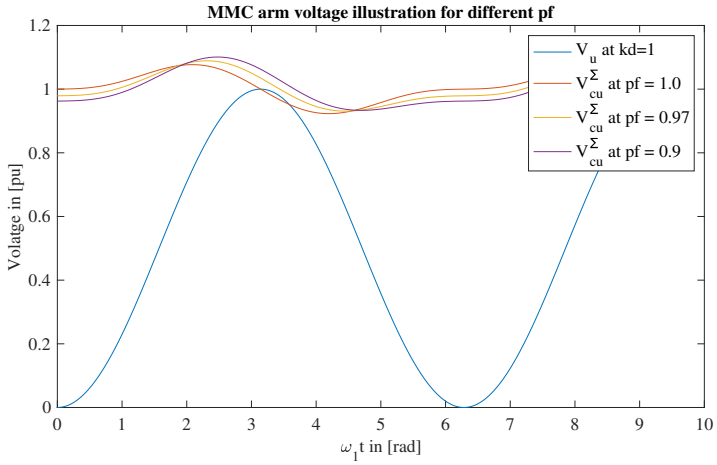


Figure 4.5: The upper arm voltage and sum capacitor voltages for different power factors with $V_{\text{base}} = V_{\text{dr}}$.

$$V_{\text{rec,pu}} = \frac{V_{\text{rec}}}{V_{\text{dr}}} \geq \frac{k_{\text{d}} - 1}{\frac{1}{4} + k_{\text{d}}} \tag{4.22}$$

$$k_{\text{d}} - 1 \leq \frac{1\frac{1}{4} V_{\text{rec,pu}}}{1 - V_{\text{rec,pu}}} \tag{4.23}$$

Note that the inequality in Equation (4.23) can be made more stringent by using the Equation (4.24). As a result a linear approximation of the DC voltage enhancement boundary $k_{\text{d,max}}$ can be made as proposed in Equation (4.25). This linear approximation is most accurate for small values of the reactive voltage $(V_{\text{rec,pu}} << 1)$.

$$1\frac{1}{4} V_{\text{rec,pu}} \leq \frac{1\frac{1}{4} V_{\text{rec,pu}}}{1 - V_{\text{rec,pu}}} \tag{4.24}$$

$$k_{\text{d,max}} \approx 1 + 1\frac{1}{4} V_{\text{rec,pu}} \tag{4.25}$$

The analytical DC link voltage enhancement of Equation (4.18) and the linear approximation of Equation (4.25) are shown in Figure 4.6 as a function of the reactive voltage $V_{\text{rec,pu}}$. From this figure can be concluded that the DC link voltage enhancement boundary $k_{\text{d,max}}$ increases approximately linear with the reactive voltage observed in an MMC arm. This fundamental characteristic of the MMC is later utilised for the dynamic DC link voltage engagement.

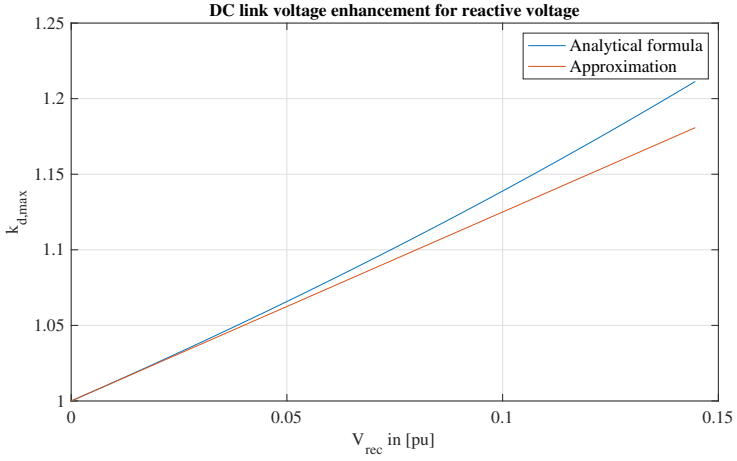


Figure 4.6: The DC link voltage limit as a function of the reactive voltage with $V_{\text{base}} = V_{\text{dr}}$.

4.3 Limitations to the enhancement

During the analytical derivation of the DC link voltage enhancement limit, multiple assumptions were made to simplify the boundary expression. Although these assumptions are applicable for most operating cases, in some parts of the operating range, they can cause significant errors. As a result, a discrepancy can occur between the maximum enhancement observed during simulations/experiments and the one expected from the analytical expression. The assumptions thus limit the accuracy of Equation (4.18) in representing the actual DC link voltage enhancement boundary. In this section, the assumptions are further analysed to define the limitations they cause on the DC link voltage enhancement boundary.

The limitations of Equation (4.18) can directly be observed during simulations. Using the Arm-Level Averaged (ALA) simulation model that is discussed in Appendix B.1, the simulated DC link voltage enhancement limit can be found. This is achieved by observing the minimal distance between the sum capacitor voltage v_{cu}^{Σ} and the upper arm voltage v_{u} when the MMC is operated at rated link conditions. The simulated enhancement boundary can be calculated using Equation (4.26), which is derived by comparing Equation (4.15) and (4.18). Note that the outcome of this simulation $k_{\mathrm{d,sim}}$ effectively reflects the first iteration of Equation (4.18), when k_{d} is initialised at 1. This as a DC link voltage enhancement causes the ripple in v_{cu}^{Σ} to increase, which allows for further biasing of the arm voltage.

$$k_{\mathrm{d,sim}} = 1 + \frac{2 \cdot min_{\mathrm{t}}\{v_{\mathrm{cu}}^{\Sigma} - v_{\mathrm{u}}\}}{V_{\mathrm{dr}}} \tag{4.26}$$

The results of the simulation is shown in Figure 4.7. This figure contains the analytic enhancement boundary $k_{\mathrm{d,max}}$, the first iteration of Equation (4.18) and the simulated enhancement limit $k_{\mathrm{d,sim}}$, all as a function of the power factor. The simulations are performed when operating at the rated output current i_{s}, with an arm impedance $X_{\mathrm{c}} = 8.68\Omega$, and at a rated DC link voltage $V_{\mathrm{dr}} = 17.1kV$, in line with the MMC properties proposed in Appendix B.1. From Figure 4.7 can be concluded that the simulated DC link voltage enhancement approximates the first iteration curve with significant accuracy for power factors close to 1.0. For lower values of pf, the simulated DC link enhancement limit is significantly lower than the first iteration curve. This difference can be caused by the linear approximation of the square root as discussed in Appendix C.1. According to this appendix the discrepancy between the two curves should increases at lower power factors and higher DC link voltages. Therefore, it can be concluded that for lower values of pf the actual DC link voltage enhancement limit that can be achieved during simulation will be significantly lower than the analytical boundary expression $k_{\mathrm{d,max}}$.

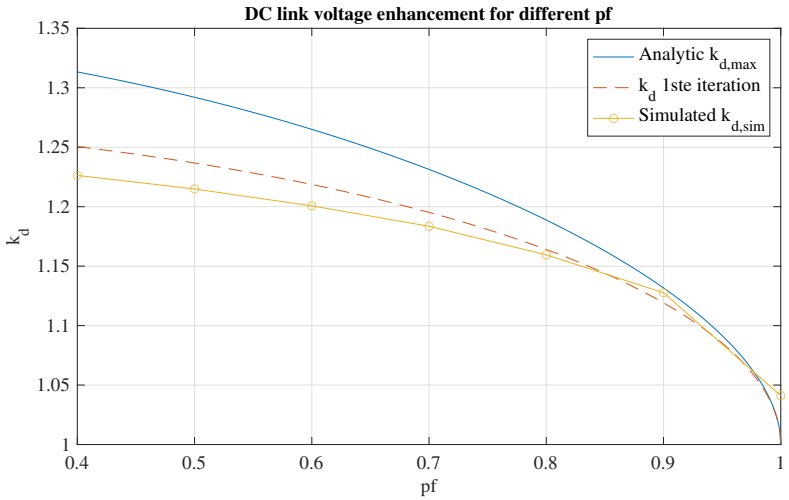


Figure 4.7: Analytic and simulated k_d for a wide range of pf.

As can be observed in Figure 4.7, the analytical boundary $k_{\mathrm{d,max}}$ and simulated limit $k_{\mathrm{d,sim}}$ are almost

identical for power factors close to 1.0. Therefore, a second simulation is performed on a more accurate power factor range of $pf \in [0.9, 1]$. The result of the ALA simulation is provided in Figure 4.8. This figure contains three curves: the first iteration of Equation (4.18), the simulated enhancement limit $k_{\text{d,sim}}$, and a compensated version of the simulation curve $k_{\text{d,com}}$, all defined as a function of the power factor. The first aspect that can be observed in Figure 4.8, is that the simulated enhancement limit $k_{\text{d,sim}}$ exceeds the analytical first iteration curve over the entire interval. This observation can be explained by considering the grid voltage and DC link voltage. As defined in the simulation properties of Appendix B.1, the simulations are performed at a rated DC link voltage $V_{\text{dr}} = 17.1kV$ and with a grid voltage amplitude $\hat{V}_{\text{g}} = 8.17kV$. Though note that in section 4.1 the assumption was made that the output voltage amplitude $\hat{V}_{\text{s}}$ was fixed at the maximum of $V_{\text{dr}}/2$. As $V_{\text{dr}} > 2\hat{V}_{\text{g}}$ these is about a 5% voltage spacing in which output voltage amplitude $\hat{V}_{\text{s}}$ can vary. As mentioned in [11], injecting reactive power into a grid often requires a higher output voltage. Therefore, $V_{\text{dr}} > 2\hat{V}_{\text{s}} > 2\hat{V}_{\text{g}}$ when reactive energy is injected into the AC network[1]. This statement explains why the simulated enhancement limit $k_{\text{d,sim}}$ exceeds the analytical curve. With no reactive power the 5% voltage spacing between $2\hat{V}_{\text{s}}$ and V_{dr} adds to the existing enhancement limit of 0. Then to inject reactive power into the AC network, the amplitude of v_{s} must be increased, lowering the spacing between V_{dr} and $2\hat{V}_{\text{s}}$ and thus contributing less to the existing enhancement.

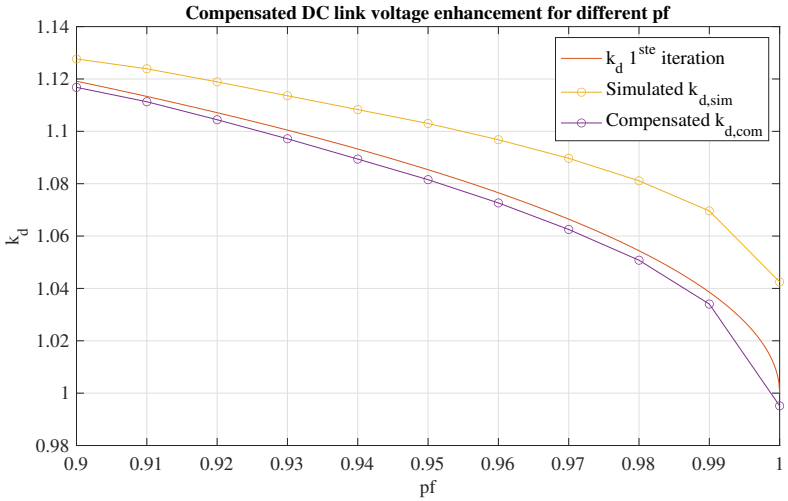


Figure 4.8: Analytical, simulated and compensated k_{d} for the high power factor range.

To differentiate between the enhancement caused by the injection of Q and the enhancement caused by the voltage spacing, the third curve: $k_{\text{d,com}}$ in Figure 4.8 can be used. In this curve, the simulated spacing between V_{dr} and $2\hat{V}_{\text{s}}$ is subducted from the simulated enhancement limit $k_{\text{d,sim}}$. This is done to solely indicated the enhancement caused by the ripple in v_{cu}^{Σ}, which is due to the injection of Q. As can be seen in the Figure 4.8, the compensated DC link voltage enhancement $k_{\text{d,com}}$ and the first iteration curve are almost identical over the operating range $pf \in [0.9, 1]$. This complies with the requirement of the MVDC distribution link. As the main task of the link is to transmit active power between the two AC networks, where the MMCs operate at high power factors. Note that if the MVDC link is used for power quality improvement, where lower power factors are essential, the analytical enhancement formula must be altered significantly to compensate for the varying $\hat{V}_{\text{s}}$. This is considered to be outside the scope of this report.

Although the compensated simulation curve $k_{\text{d,com}}$ seems directly conformable to the first iteration curve, small errors are present. First, at $pf = 1$ the found enhancement factor limit is below 1. This phenomenon was also observed in Figure 4.5 and can be caused by the stringent time-point assumption of $\omega_1 t = \pi$. The impact of this assumption is further discussed in Appendix C.2. Second, over the complete power

[1] Assuming the grid injected active power P of the MMC is positive.

factor range, the compensated simulation curve is below the first iteration curve. This can be caused by the assumption of i_c and v_c being constants. In practice, the energy balancing control adds fluctuating components to v_c that can increase the amplitude of v_u [30]. This in turn can negatively impact the simulated enhancement limit.

To cope with the limitations caused by the assumptions, the controller enhancement function is proposed. The controller operates at a fixed percentage lower enhancement, e.g. 5%, than the analytical boundary $k_{d,max}$. The k_d curve of the controller enhancement function is provided in Figure 4.9. This curve is later used by the dynamic DC link voltage control in Chapter 5. It can be seen that the controlled k_d curve does clear both the analytical boundary and the simulated enhancement limit $k_{d,sim}$ in the practical operating range of the MVDC distribution link.

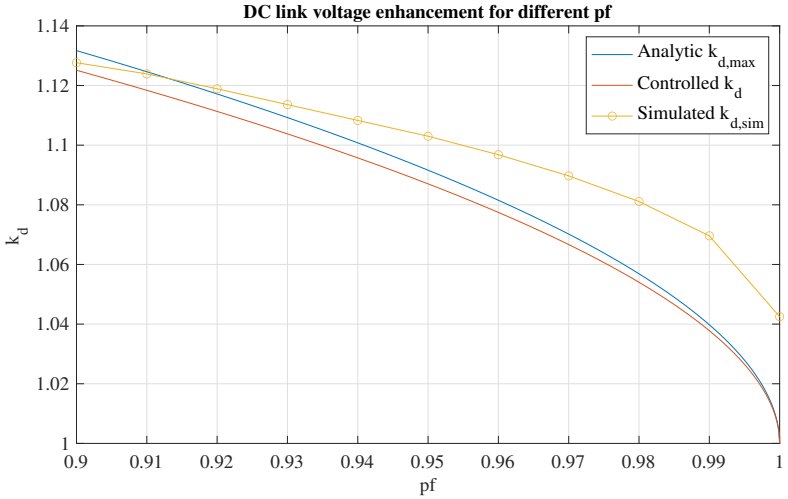


Figure 4.9: Practical interpretation for k_d control for different pf.

Chapter 5

Dynamic DC Link Voltage Control

As the analytical boundary of the DC link voltage enhancement was derived, the next step is to alter the MMC control strategy to incorporate the enhancement dynamically. The alteration of the MMC control strategy is performed with the introduction of a new controller: the dynamic DC link voltage control. This controller dynamically alter the DC link voltage reference given the operational reactive power injected into the AC network. In this chapter, the design of the dynamic DC link voltage controller is elaborated. First, Section 5.1 analyses a direct control method for implementations of the dynamic DC link voltage control. Then in Section 5.2 the requirements of the dynamic controller are defined. Third, Section 5.3 discusses the design of the dynamic open-loop control strategy after which it is simulated and verified in Section 5.4.

5.1 Direct DC link voltage control

The simplest approach towards the design of the dynamic DC link voltage controller is to alter the DC link voltage reference V_{d}^{*} by directly following the analytical boundary expression of Equation 4.19. This way, the output reactive power reference and the DC link voltage reference are simultaneously changed upon a change in the input reactive power reference Q_{ref}.

To verify the workings of the direct DC link voltage control strategy, the implemented controller is simulated using an arm-level averaged model of the MMC. The ALA model and the configuration parameters used in the simulation are discussed in Appendix B.1. The implemented control structure used to regulate the MMCs is based on the topology explained in Chapter 3. Note that the output of the direct control, the DC link voltage reference V_{d}^{*}, is applied as an input to the DC link voltage control of Section 3.6.3. In the simulation the two MMCs are back-to-back configured and connected via a DC link. The result of the simulation is provided in Figures 5.1, 5.2 which show the reactive power, the DC link voltage, and the arm voltages as a function of time. In this simulation the power factor reference is decreased from $pf = 1.0$ to $pf = 0.9$ at time-point $t = 3.0s$ and increased from $pf = 0.9$ to $pf = 1.0$ at time-point $t = 4.0s$ while operating at the rated output current.

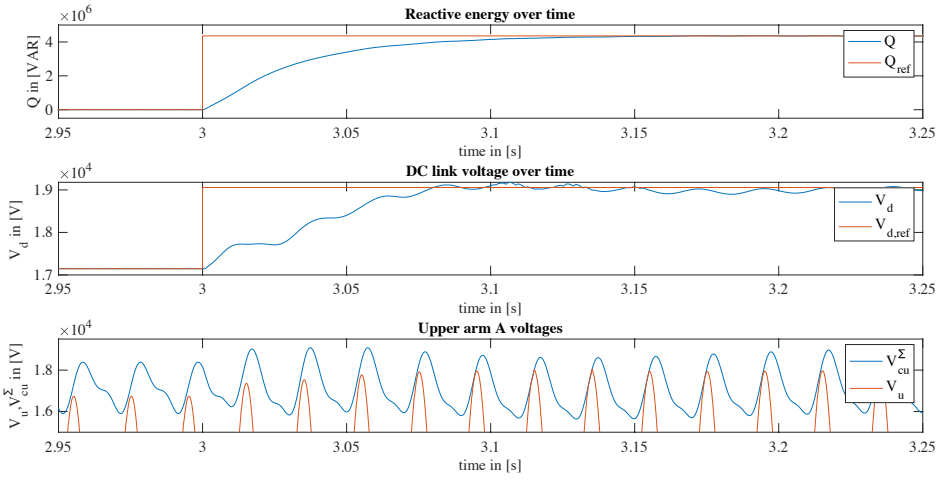


Figure 5.1: Direct DC link voltage control decreasing power factor.

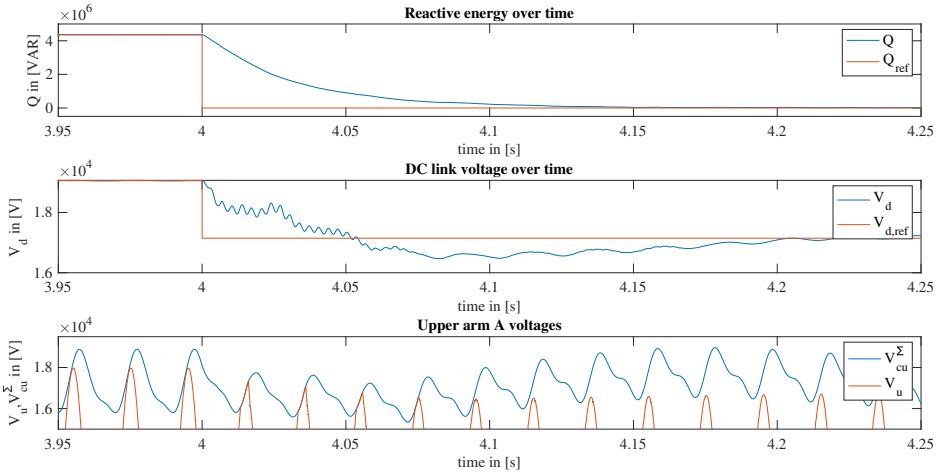


Figure 5.2: Direct DC link voltage control increasing power factor.

From Figures 5.1, 5.2 can be concluded that, with the direct control method, the upper-arm voltage v_{u} intersects the sum capacitor voltage v_{cu}^{Σ} for both an increases and decreases in Q_{ref}. Note that this is in violation with constraint (4.1). The saturation of v_{u} at v_{cu}^{Σ}, effects the normally sinusoidal arm voltage to become a capped of sine wave. The clipping of the arm voltage $v_{\mathrm{u,l}}$ induces high frequency components in the output voltage v_{s}. This in turn causes the injection of high frequency output current components into the AC network. Note that the harmonic distortion negatively impacts the performance of the AC networks: higher eddy current losses, core losses, load distortion, over-voltages, and increased RMS currents that limit the effective power transfer capacity [13]. Overall these harmonic elements are undesirable to the operation of the MMC and must thus be avoided.

5.2 Controller requirements

In order to achieve a reliable operation while operating at an enhanced DC link voltage, the dynamic DC link voltage controller has to follow a set of requirements as defined in Table 5.1.

Table 5.1: Requirement for the dynamic DC link voltage controller

	Dynamic DC link voltage control requirements:
D1.	The controller must maximise the enhancement of the DC link voltage reference V_{d}^{*} based on the injected reactive power Q of the converter.
D2.	The controller must have a fast dynamic response to changes in the reactive power reference Q^{*}.
D3.	The controller must make sure that the sum capacitor voltage v_{cu}^{Σ} is larger than the arm voltage v_{u} at all times.
D4.	The controller keeps the MMC energies within the rated limits.
D5.	The controller must be implemented as a discrete control system operated at a control frequency of $f_{\mathrm{c}} = 5kHz$.
D6.	The controller must operate in a safe steady state during startup, after which it pursues an enhanced operation.
D7.	The controller must incorporate a fault trigger mechanism, by which it returns to a safe steady state.

The requirements set in Table 5.1 provide a guideline for the design of the dynamic DC link voltage control. Though, note that among these requirements, conflicts exist which impose trade-offs in the design. For instance, requirements D1 and D3 are conflicting. This was noted in Section 4.1, as the DC link

enhancement is limited by the intersection of the sum capacitor voltage and the arm voltage. Another conflict is imposed between requirements D2 and D3. Requirement D2 emphasises the importance of the dynamic aspect of the controller. The speed at which the controller can react to reference changes is of great significance in dynamic distribution link applications. Note that when the MMC operates at an enhanced DC link voltage, an increase of Q is directly allowed. However, a decrease in Q can only be done after the V_{d} has significantly been lowered. Otherwise, harmonic components are injected into the AC network. Similarly, a decrease in V_{d} is directly allowed tough an increase in V_{d} can only be done after Q has significantly been increased. This causes a trade-off is between the speed of the controller and its ability to comply to constraint (4.1).

In the remainder of this chapter a dynamic DC link voltage control strategy is proposed which should fulfil the requirements of Table 5.1. The proposed control strategy: the open-loop control strategy is designed in Section 5.3 and verified in Section 5.4. This controller is designed with a more stable and reliable design philosophy, favouring no constrain violation over dynamic performance. An alternative to this approach, would be the closed-loop control strategy, where dynamic performance is defined as a higher priority. This controller is not seen as part of the project, but a brief introduction is provided as future work in Section 9.1.

5.3 Open-loop control design

The open-loop DC link voltage controller is designed to dynamically enhance the DC link voltage V_{d}, by solely using the reactive power reference Q^* as an input. This design is constructed to achieve a stable and reliable implementation of the controller that does require any feedback. With this conservative approach, the compliance of constraint (4.1) is prioritised over a fast dynamic performance of the converter.

Following requirement D5 the open-loop DC link voltage controller is implemented using a discrete control strategy. To incorporate smart behaviour in the controller, the control logic is realised using a Finite State Machine (FSM). This provides an event-driven control system where state transitions are made conditional to the operational parameters. The finite state machine of the open-loop DC link voltage controller is provided in Figure 5.3.

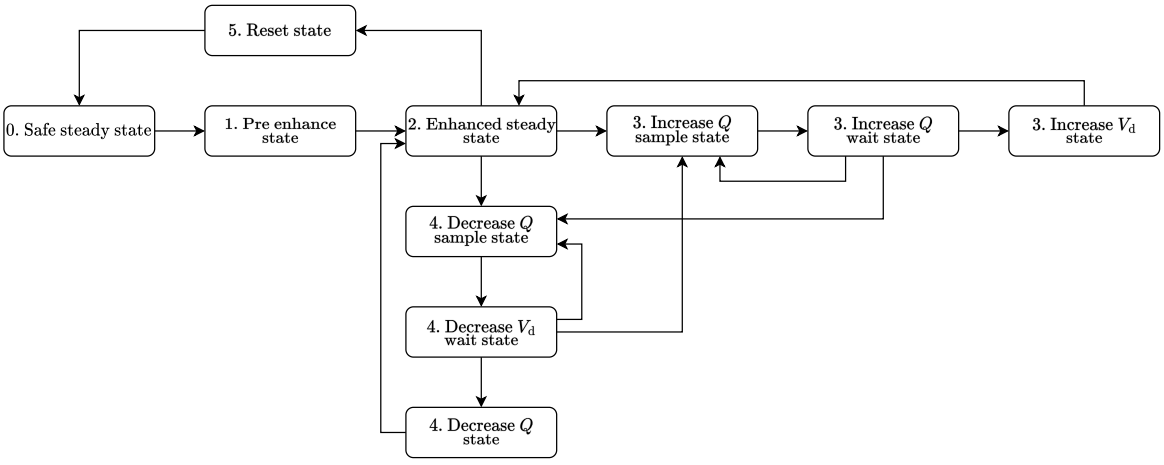


Figure 5.3: Finite state machine of the open loop DC link voltage controller.

The finite state machine in Figure 5.3, consists of 10 states implementing four main process transitions. Each of these is discussed in more detail in the following sections. For the explanation of the process transitions, the following input/output parameters are defined:

- Q_{ref}, is the input reactive power reference in $[VAR]$, to be injected into the grid

- Q^*, is the output reactive power reference of the dynamic DC link voltage control in $[VAR]$
- P_{ref}, is the input active power reference in $[W]$, to be injected into the grid
- P^*, is the output active power reference of the dynamic DC link voltage control in $[W]$
- k_{d}^*, is the output enhancement factor reference of the dynamic DC link voltage control.

As was concluded from Figure 4.8, the dynamic DC link voltage controller should operate at a fixed fraction of the analytical enhancement. For this, a 5% lower enhancement was proposed than the analytical boundary $k_{\text{d,max}}$. Therefore the controller enhancement function given in Equation (5.1) can be defined. Note that the 5% reduction is subjected to the MMC properties and the operating range. Therefore the reduction fraction should be optimised for the application.

$$\text{f}_{\text{kd}}(Q) = 1 + 0.95 * (\underbrace{\frac{6V_{\text{dr}}^2 + QX_{\text{c}}}{6V_{\text{dr}}^2 - 4QX_{\text{c}}}}_{k_{\text{d,max}}} - 1) \tag{5.1}$$

5.3.1 Safe steady state

When the MMC is initialised, the DC link voltage enhancement is inactive. This is compliant with requirement D6 and is done to provide a reliable and secure MMC startup at rated conditions. This initial state is called the *safe steady state* in which the controller outputs are defined as follows:

- $Q^* = Q_{\text{ref}}$, The reactive power reference is passed through directly.
- $P^* = P_{\text{ref}}$, The active power reference is passed through directly[1].
- $k_{\text{d}}^* = 1$, the DC link voltage reference is maintained at rated condition.

After the startup period of τ_{startup} seconds, the FSM transitions to an enhanced state. Note that in case the *reset* signal is set high or the input reference Q_{ref} changes, the controller maintains to operate in the *safe steady state*.

5.3.2 Pre enhanced state/Enhanced steady state

After the startup in *safe steady state* the FSM transitions to the *pre enhanced state*. This state is used to increase the DC link voltage to the intended reference as a preparation to the *enhanced steady state*. In the *pre enhanced state* the controller outputs are defined as:

- $Q^* = Q^*$, The reactive power reference is kept constant at the last sampled value.
- $P^* = P_{\text{ref}}$, The active power reference is passed through directly[1].
- $k_{\text{d}}^* = \text{f}_{\text{kd}}(Q^*)$, the DC link voltage reference is enhanced to 5% below the analytical boundary.

After the time period of τ_{kd} seconds, needed for the V_{d} to reach its reference $k_{\text{d}}^* V_{\text{dr}}$, the FSM transitions to the *enhanced steady state*. When the MMC operates in the *enhanced steady state*, the DC link voltage is maintained at the enhanced level, and the reactive power reference Q^* is kept constant. The FSM remains in this state while changes occur input reactive power reference Q_{ref} or the *reset* signal is maintained high.

[1] The active output power reference P^* is saturated based on the rated apparent power S_{max} and Q^*

5.3.3 Increase Q

When operating in the *enhanced steady state* the input reactive power reference Q_{ref} can increase such that $Q_{\text{ref}} > Q^*$. This increase initiates a process in the dynamic DC link voltage control to enhance the DC link voltage. Recall from Section 5.2 that the order in which the reactive power reference Q^* and the enhancement factor reference k_{d}^* are altered, significantly impacts the harmonic performance of the MMC. So to limit output distortion, the increase reactive power transition is implemented as a three-state sequence in the FSM. Upon an increase in Q_{ref} first, the FSM transitions to the *increase Q sample state* by which Q_{ref} is sampled, setting $Q^* = Q_{\text{ref}}$. Second, the FSM transitions to the *increase Q wait state* at which the reactive power Q increases over τ_{Q} seconds to the reference Q^*. Finally, when the reactive power output is increased, the FSM transitions to the *increase Vd state*. In this state the DC link voltage is enhanced to 5% below the analytical boundary $k_{\text{d}}^* = f_{\text{kd}}(Q^*)$. This transition happens over a time period of τ_{kd} seconds. Note that this step-wise approach makes sure that the sum capacitor voltage v_{cu}^{Σ} is larger than the arm voltage v_{u} at all times during the process. The increase Q transition is also depicted in Figure 5.4

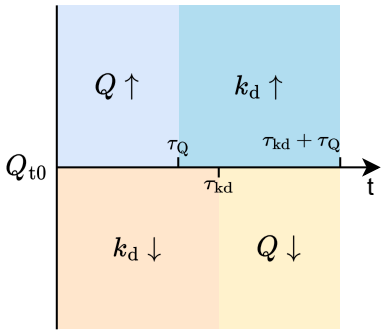


Figure 5.4: Open loop controller increase and decrease Q process.

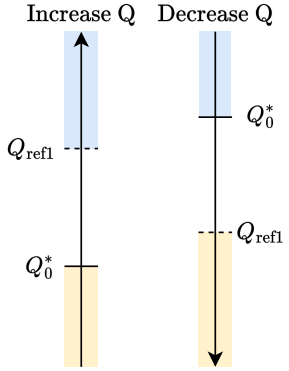


Figure 5.5: Open loop controller added state transitions.

Besides the standard process, Figure 5.3 indicates two additional transitions in the *increase Q wait state*. These state transitions are added to enhance the dynamic behaviour of the open-loop controller. The transitions are explained using Figure 5.5. Consider that at time point t_0 the MMC operates at a reactive power $Q = Q_0^*$ and the input reactive power reference is increased such that $Q_{\text{ref1}} > Q_0^*$. Then the FSM initiates the increase Q process and sequentially enters the *increase Q sample state* and *increase Q wait state*. In the *increase Q wait state* the FSM has to wait for τ_{Q} seconds, before entering the *increase Vd state*. During this waiting period Q_{ref} can be changed. Consider that before the waiting period of τ_{Q} seconds has ended, the reactive power reference is changed to Q_{ref2}. Now if $Q_{\text{ref2}} > Q_{\text{ref1}}$ the FSM transition back to the *increase Q wait state* to incorporate the further enhancement. Though if $Q_{\text{ref2}} < Q_0^*$ the net transition is a decrease in Q so FSM transition the decrease Q process. These transitions are used to enhance the dynamic response of the MMC to changes in the reactive power reference. This act is in line with requirement D2.

5.3.4 Decrease Q

Similar to the increase in Q, the input reactive power reference Q_{ref} can also decrease when operating in the *enhanced steady state*: $Q_{\text{ref}} < Q^*$. This decrease initiates a process in the dynamic DC link voltage control to lower the DC link voltage. Upon a decrease in Q_{ref} first, the FSM transitions to the *decrease Q sample state* by which Q_{ref} is sampled and the enhancement factor reference is set to 5% below the analytical boundary $k_{\text{d}}^* = f_{\text{kd}}(Q_{\text{ref}})$. Second, the FSM transitions to the *decrease Vd wait state* at which the DC link voltage is lowered over τ_{kd} seconds while maintaining the initial reactive power reference. Finally, when the DC link voltage has settled, the FSM transitions to the *decrease Q state* in which the

reactive power reference is lowered $Q^* = Q_{\text{ref}}$ over τ_{Q} seconds.

Similar to the increase Q process, the decrease Q process has added state transitions to enhance the dynamic behaviour of the open loop controller. Again using Figure 5.5, Consider that at time point t_0 the input reactive power reference is decreased such that $Q_{\text{ref1}} < Q_0^*$. Then the FSM initiates the decrease V_{d} process over τ_{kd} seconds. Though before the end of this period the reactive power reference changes to Q_{ref2}. Now if $Q_{\text{ref2}} < Q_{\text{ref1}}$ the FSM transition back to the *decrease Q sample state* to incorporate the further lowering of V_{d}. Though if $Q_{\text{ref2}} > Q_0^*$ the net transition is an increase in Q so FSM transition an increase Q process. These transitions are again used to enhance enhance the dynamic response of the open loop controller.

5.3.5 Reset trigger

To return back from the *enhanced steady state* to the *safe steady state*, the *reset* signal is used. Once the *reset* signal is set high, the FSM enters the *reset state* in which the controller outputs are defined as follows:

- $Q^* = Q^*$, The reactive power reference is maintained at the last initial value.
- $P^* = P_{\text{ref}}$, The active power reference is passed through directly[1].
- $k_{\text{d}}^* = 1$, the DC link voltage reference is set at the rated value V_{dr}.

After operating for τ_{kd} seconds in the *reset state*, the DC link voltage has settled at the rated DC link voltage value and the FSM can safely enter the *safe steady state*.

With the open loop DC link controller and effective and reliable approach is taken towards implementing the dynamic DC link voltage controller. The parameters τ_{startup}, τ_{kd} and τ_{Q} are tuned for the MMC application as is further discussed in section 6.3.

5.4 Open-loop control simulation

To verify the working of the open-loop dynamic DC link voltage control, the controller is simulated using the arm-level averaged model of the MMC. The simulation setup is similar to the one performed in Section 5.1 with the used configuration parameters as defined in Appendix B.1. During the simulation, the operating power factor is decreased from $pf = 1.0$ to $pf = 0.9$ at $t = 3.0s$ and increased from $pf = 0.9$ to $pf = 1.0$ at $t = 4.0s$. The parameters τ_{startup}, τ_{kd} and τ_{Q} are tuned for the back to back configured MMC application and are set at:

- $\tau_{\text{startup}} = 1.8s$
- $\tau_{\text{kd}} = 0.6s$
- $\tau_{\text{Q}} = 0.3s$

The result of the simulation is provided in Figures 5.6 and 5.7 which show the reactive power, DC link voltage and arm voltages as a function of time. Figure 5.6 and 5.7 indicate the system response for a decrease in pf and increase in pf, respectively. Analysing Figure 5.6, it can be concluded that the open-loop controller successfully increases both the reactive power and the DC link voltage. Comparing Figures 5.1 and 5.6, it can be concluded that the open-loop dynamic DC link voltage controller first increases the reactive energy for 0.3s, before enhancing the DC link voltage. In contrast to the direct

[1]The active output power reference P^* is saturated based on the rated apparent power S_{max} and Q^*

control method, the upper-arm voltage v_u does not intersects the sum capacitor voltage v_{cu}^{Σ} for an increases in Q_{ref}. The dynamic DC link voltage controller does therefore satisfy requirement D3, limiting the injection of harmonic elements into the grid.

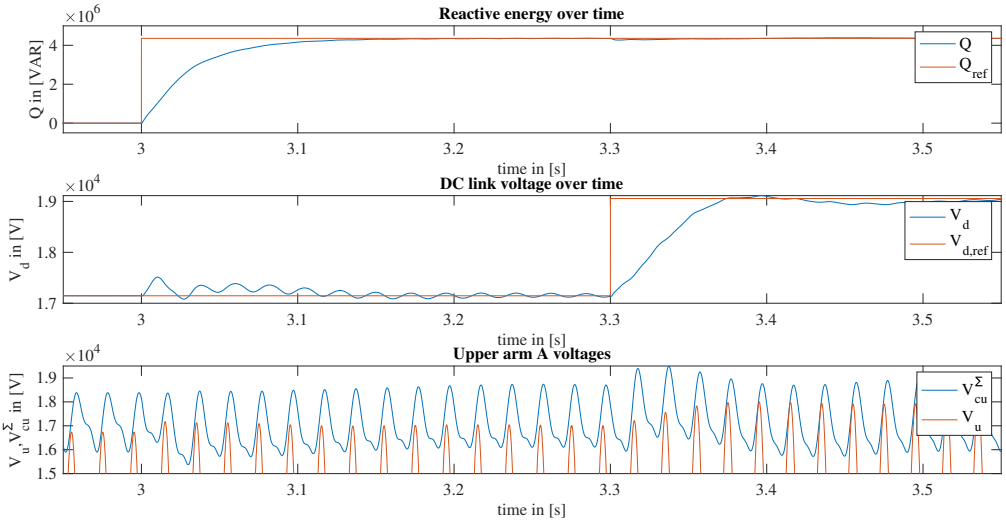


Figure 5.6: Direct DC link voltage control decreasing power factor.

A similar behaviour can be observed for the increase in pf. Analysing Figure 5.7, it can be concluded that the open-loop controller successfully decreases both the reactive power and the DC link voltage. By comparing Figures 5.2 and 5.7, it can be concluded that the open-loop dynamic DC link voltage controller first decreases the DC link voltage for 0.6s before lowering the reactive energy. In contrast to the direct control method, the upper-arm voltage v_u does not intersects the sum capacitor voltage v_{cu}^{Σ} for a decrease in Q_{ref}. Therefore requirement D3 is again satisfied. Overall the harmonic performance of the open-loop dynamic DC link voltage controller exceeds the direct control method. Though, note that this is achieved at the expense of the dynamic performance of the controller.

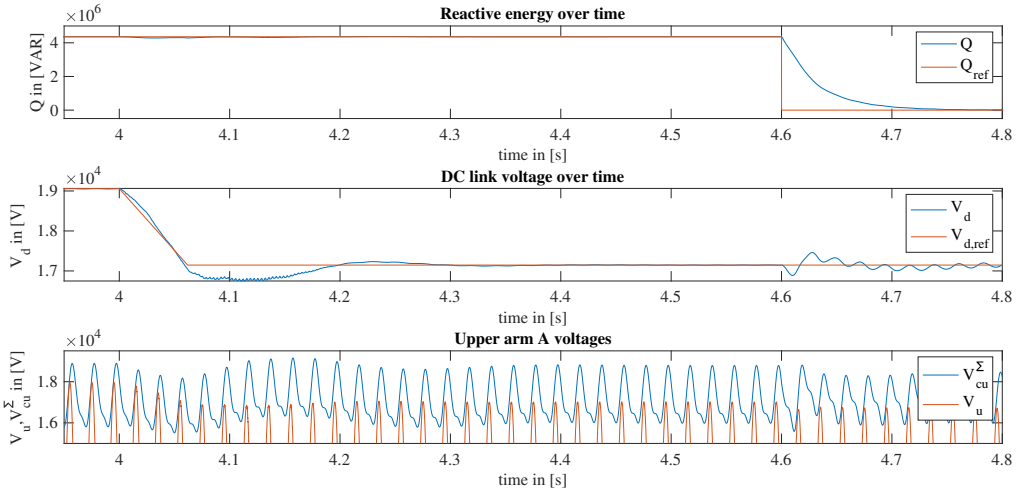


Figure 5.7: Direct DC link voltage control increasing power factor.

Chapter 6

Lab MMC Control Implementation

After establishing the MMC control structure in Chapter 3 and the dynamic DC link voltage control in Chapter 5, this chapter focuses on implementing the control strategy for a lab-scale MMC prototype. The control strategy is then used in Chapter 7 to experimentally demonstrate the workings of DC link voltage enhancement and verify the enhancement boundary expression. The lab-scale MMC used for the experiments is denoted as the "Imperix MMC". A detailed overview of the Imperix MMC is provided in Appendix D.1. As mentioned in this appendix, the Imperix MMC is controlled via the B-Box RPS controllers, which are coded using the ACG SDK software in Matlab Simulink.

As implied in Chapter 3, the MMC control strategy can be decomposed into a modulator and a controller. In this chapter, both the modulator and the controller are implemented for the Imperix MMC. First, Section 6.1 discusses the modulator's implementation, which includes the modulation strategy's definition and the design of a fault trigger mechanism. Second, the MMC controller is implemented in Section 6.2. This control implementation is similar to the topology discussed in Section 3.2 and is composed of a voltage controller, SM balancing controller, output current controller, energy balancing controller and a higher-level control. Finally, in Section 6.3 the open-loop DC link voltage controller is added and tuned for the Imperix MMC.

6.1 Imperix modulator

The MMC modulator is used to convert the modulation index $m^{\mathrm{i}}_{\mathrm{abc}}$, defined by the MMC control, into a switching signal s^{i}_{abc}, used by the gate driver. The principle of modulation was introduced in Section 2.3 with multiple types of commonly used modulation techniques. In this section, a modulation technique is chosen and implemented for the Imperix MMC.

6.1.1 Modulation strategy

In Section 2.3 various modulation techniques were discussed. Each technique has advantages and disadvantages, and thus is prominent in a specific application. In [31], the applicability and performance of the modulation techniques are compared. Table 6.1 provides an overview of the results. From Appendix D.1 can be concluded that the Imperix MMC has $N = 4$ submodules per arm. This eliminates NLC as the used modulation technique. Note that NLC has a low output performance, which comprises large AC side harmonics and heavily fluctuations in the DC-side voltage. This would cause issues during later applications of the MMC.

Table 6.1: Comparison table for performance modulation techniques

Performance index:	LSC-PWM	PSC-PWM	NLC	SHE	SV-PWM
Switching Frequency	f_{s}>2kHz	f_{s}>2kHz	f_{s}<100Hz	f_{s}<100Hz	$f_{\mathrm{s}} \in$[0.1,2]kHz
Number of SM	All	All	Large (N>12)	Small (N<12)	Small (N<12)
Output performance	Moderate	High	Low	High	High
Design complexity	Moderate	Complex	Easy	Complex	Complex

Then using Appendix B.2, it can be concluded that the switching frequency is $f_s = 5kHz$. This eliminates SHE and SV-PWM, and leaves LSC-PWM and PSC-PWM. Then, based on the higher output performance, PSC-PWM is chosen as the modulation technique for the Imperix MMC. This choice is made because the B-Box RPS controllers are fully capable of performing the higher complexity modulation. The higher output performance thus easily offsets the higher complexity. Another main advantage of PSC-PWM over LSC-PWM is that it provides natural balancing of the submodule capacitor voltages. Which simplified the SM balancing controller implementation.

For the implementation of PSC-PWM in the Imperix modulator, the CB-PWM block is used as part of the ACG SDK software. This Simulink block generates the triangular carrier wave signal and displaces the carrier horizontally over an assigned fraction of the fundamental period. Then the carrier signal is compared with the reference modulation index m^{i} to generate the switching signal s^{i}. This block also performs dead-time generation to prevent cross-conduction. The simulation of the operation of the CB-PWM block is provided in Figure 6.1. This figure shows the output switching signal of the upper s_1^i and lower switch s_2^i, resulting from the input modulation index m^{i}.

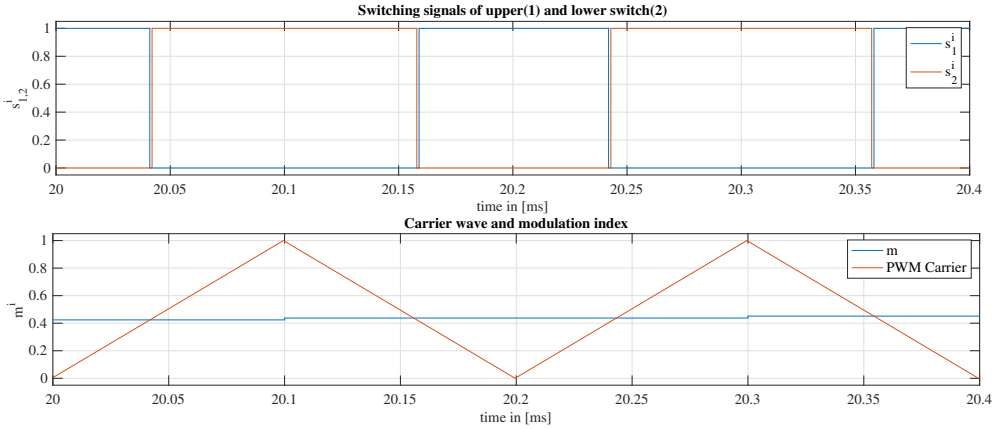


Figure 6.1: PSC-PWM implemented for Imperix modulator.

6.1.2 Fault trigger module

One of the main features of the CB-PWM block is the ability to operate the SMs in blocking state. As motioned in Section 2.2.1, when operated in blocking state, both switches of the SM are in a non-conducting mode. This state is used during the startup of the MMC and in emergency conditions. A fault trigger module is implemented to ensure a safe operation while testing the designed controllers. The module forces all SMs into blocking state if a safety limit is surpassed.

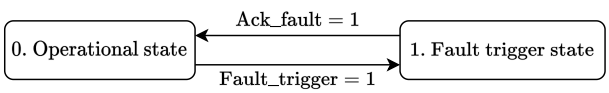


Figure 6.2: Finite state machine of the fault trigger module.

The control logic of the fault trigger module is realised using a FSM. The finite state machine of the fault trigger module is provided in Figure 6.2. The FSM contains two conditional transitions between the states. The initial state of the FSM, denoted as the *operational state*, is used for the normal operation of the MMC. In this state, the reference modulation index is provided by the MMC control and the modulators perform PSC-PWM to generate $s_{1,2}^i$. Now if a safety limit is surpassed, the $fault\_trigger$ signal is set high, and the FSM transitions to the *fault trigger state*. All modulation indices are fixed to zero in this

state, and the modulators generate zero output switching signal $s^i_{1,2} = 0$. For the considered applications, safety limits are set for both the individual submodule voltages $v^{\mathrm{i}}_{\mathrm{cu,l}}$ and the DC link voltage V_{d}.

The working of the fault trigger module is verified though experiments. The result of the Imperix measurements are provided in Figures 6.3 and 6.4. Figure 6.3 indicates the fault triggering based on a exceedance of the SM voltage limit, $v^{\mathrm{i}}_{\mathrm{cu,l}} > 14$ [1]. Figure 6.4 indicates the fault triggering based on a exceedance of the DC link voltage limit, $V_{\mathrm{d}} > 75$ [1].

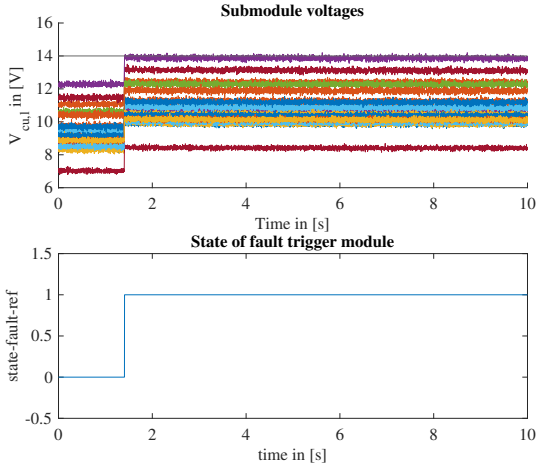


Figure 6.3: Fault trigger on SM voltage limit.

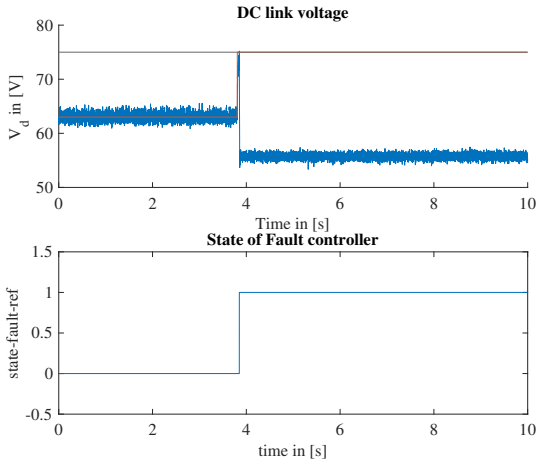


Figure 6.4: Fault trigger on DC link voltage limit.

6.2 Imperix controller

Besides the modulator, the implementation of the MMC control strategy requires a control module. The control module defines the modulation index $m^{\mathrm{i}}_{\mathrm{abc}}$ by which it forces the operation of the MMC to the desired set-point. The design philosophy behind the MMC controller has been elaborated in Chapter 3, in which Figure 3.6 gives an overview of the control topology. Recall that the MMC controller must regulate multiple quantities, which is performed using multiple sub-control modules. This section focuses on implementing and tuning the sub-control modules of the Imperix MMC.

6.2.1 Voltage control

The first sub-control module of the MMC controller is the voltage control. The voltage control module defines the modulation index $m^{\mathrm{i}}_{\mathrm{abc}}$ of a submodule given the output voltage reference v^*_{s} and the internal voltage reference v^*_{c}. Instead of using direct voltage control, as proposed in Section 3.5, the Imperix voltage control uses indirect modulation. This method utilises the measured submodule capacitor voltage $v^{\mathrm{i}}_{\mathrm{cu,l}}$ to calculate the modulation index. Even though direct voltage control has the property of inherent asymptotic stability, it does impose significant second-order circulating currents due to fluctuations of the SM capacitor voltages [32]. During experiments, these were found to be detrimental to the MMC operation. Although indirect modulation does provide advantages on the circulating current, it requires external SM voltage, arm energy and leg energy balancing, as the method is inherently marginally stable.

Note that indirect voltage control is performed for each submodule individually rather than on a arm basis. This allows for a SM capacitor balancing strategy to be deployed. The voltage control is implemented as in Figure 6.5, in which $v^{\mathrm{i}}_{\mathrm{SMb}}$ is the voltage used for the SM capacitor balancing and $-v^*_{\mathrm{s}}$, $+v^*_{\mathrm{s}}$ are used for the upper and lower SMs, respectively. Another aspect that can be seen in Figure 6.5 is

[1] The limits $v_{\mathrm{ci}} = 14$ and $V_{\mathrm{d}} = 75$ are used for illustration purposes. Higher values are chosen during later experiments

the saturation component. This limits the modulation index range to $m^{\mathrm{i}}_{\mathrm{abc}} \in [0.02, 0.98]$ as implied by Imperix.

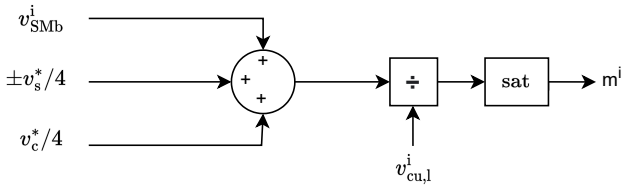


Figure 6.5: Imperix voltage control implementation.

6.2.2 SM balancing control

Throughout Chapter 3 the assumption is made that the SM capacitors voltages $v^{\mathrm{i}}_{\mathrm{cu,l}}$ inside an arm are properly balanced. The importance of this assumption was explained in Section 2.4, which mentioned that the divergence of capacitor voltages should remain limited for both the stability of the MMC and its harmonic performance. In that section, various control strategies were proposed that actively balance submodule capacitor voltages to counteract divergence.

Recall that PSC-PWM had the property of natural balancing of the submodule capacitor voltages. This allows for a simplified implementation of the SM balancing controller. As a result a PI controller is used to actively balance the submodule capacitor voltages. The SM balancing controller shown in Figure 6.6, defines a balancing voltage $v^{\mathrm{i}}_{\mathrm{SMb}}$ that adds as a DC component to the internal voltage reference v^{*}_{c}. $v^{\mathrm{i}}_{\mathrm{SMb}}$ is defined to converge a SM capacitor voltage to the arm average SM capacitor voltage $\overline{v}_{\mathrm{cu,l}}$.

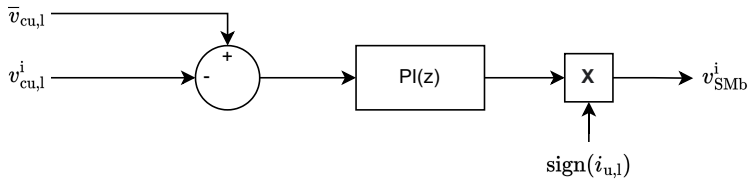


Figure 6.6: Imperix SM balancing control implementation.

The SM balancing control is based on the concept, that for a positive arm current $i_{\mathrm{u,l}}$, the modulation index is slightly decreased for a SM with an above average $v^{\mathrm{i}}_{\mathrm{cu,l}}$ and slightly increased for a SM with a below average $v^{\mathrm{i}}_{\mathrm{cu,l}}$. The opposite holds for a negative arm current. These alternations are done via $v^{\mathrm{i}}_{\mathrm{SMb}}$.

For the implementation of the SM balancing, a discrete-time PI controller is used. The transfer function of the PI controller, in forward Euler configuration, is provided in Equation (6.1). The proportional and integral gain selection is done via iterative tuning using the simulated system response. After various iterations the gains were defined at: $K_{\mathrm{p}} = 4$, $K_{\mathrm{i}} = 0.2$.

$$PI(z) = K_{\mathrm{p}} + K_{\mathrm{i}} T_{\mathrm{s}} \frac{1}{z-1} \tag{6.1}$$

During simulations, it was observed that the integrator action remained crucial to the balancing of the capacitors as it eliminated an otherwise significant steady-state error. However, the integral action is chosen to be small compared to the proportional part to restrict output discrepancies. The simulation and experimental results are shown in Figures 6.7 and 6.8, respectively.

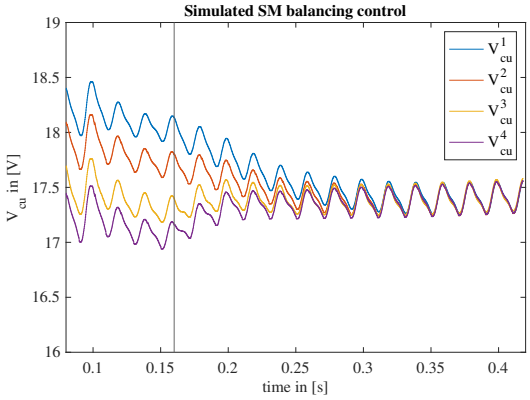


Figure 6.7: Simulated SM capacitor voltages with SM balancing control.

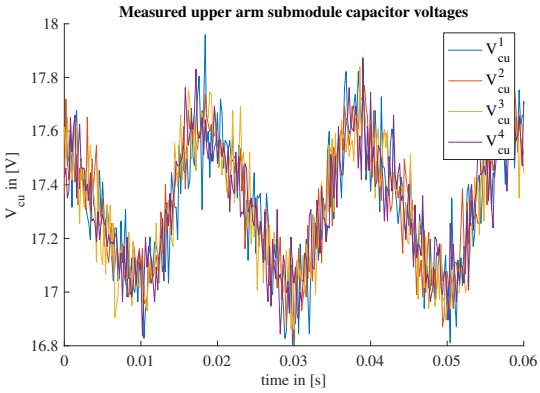


Figure 6.8: Measured SM capacitor voltages with SM balancing control.

Figure 6.7 shows the simulated SM capacitor voltages $v^{\mathrm{i}}_{\mathrm{cu}}$ of phase a, with an initial discrepancy. Till time point $t = 0.16s$, the SM balancing control is deactivated. It can be seen that the spread in the $v^{\mathrm{i}}_{\mathrm{cu}}$ is maintained over this period. After $t = 0.16$, when the SM balancing control is active, the SM capacitor voltages converge steadily to the arm average. The same behaviour is observed during experiments. Figure 6.8 shows the measured, steady-state behaviour of the Imperix MMC. The upper arm capacitors voltages of phase a refrain from any divergence when operated in steady-state. Note that the significant ripple in $v^{\mathrm{i}}_{\mathrm{cu}}$ is caused by the limited precision of the voltage sensors.

6.2.3 Output current control

Another important MMC quantity that must be controlled is the output current i_{s}. Section 3.3 elaborated on the structure of the vector output current controller. This controller defines output voltage reference v^*_{s} to force the measured output current i_{s} to the reference output current i^*_{s}. Figure 6.9 illustrates the output current control implementation for the Imperix MMC. This controller is a simplified version of Figure 3.7 as, following Appendix D, it does not require the vector saturation. As the vector output current control is designed in the dq-reference frame the abc-dq transformations are performed as in Figure 3.8.

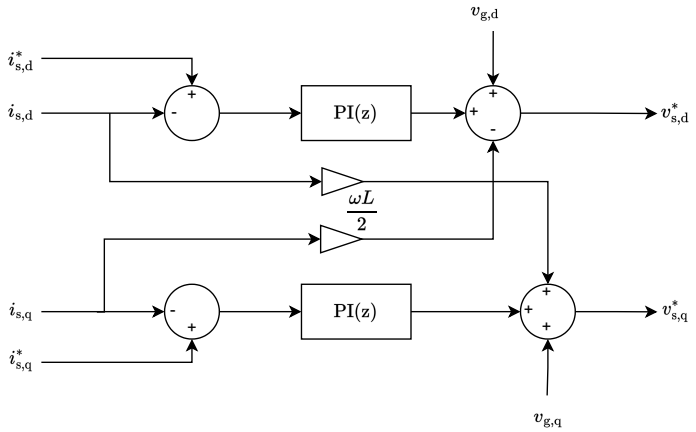


Figure 6.9: Imperix output current control implementation.

For the implementation of the output current control, discrete-time PI controllers are used. The transfer function of the PI controller, in forward Euler configuration, was provided in Equation (6.1). For the selection of the proportional and integral gain, the Magnitude Optimum (MO) tuning method is used. This PID tuning method concentrates on improving the closed-loop tracking performance of the system [33]. K_{p} and K_{i} are selected such that Equation (6.2) and (6.3) hold for the largest number of r possible.

$$G_{\mathrm{CL}}(s) = 1 \; at \; s = 0 \tag{6.2}$$

$$\frac{d^r |G_{\mathrm{CL}}(s = j\omega)|}{d\omega^r} = 0 \; at \; s = 0 \tag{6.3}$$

In Equation (6.2) and (6.3), $G_{\mathrm{CL}}(s)$ represents the closed loop transfer function of the system. The closed loop transfer is defined in Equation (6.4) as a function of the process transfer function $P(s)$ and controller transfer function $C(s)$. The complete closed loop system is presented in Figure 6.10, in which d represent the input disturbance.

$$G_{\mathrm{CL}}(s) = \frac{P(s)C(s)}{1 + P(s)C(s)} \tag{6.4}$$

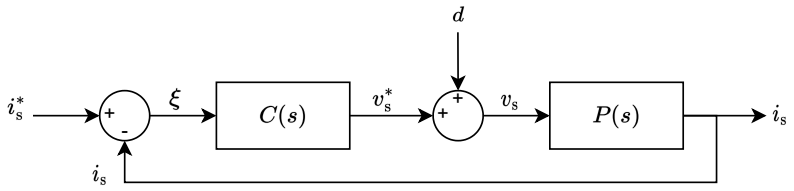


Figure 6.10: Output current control closed-loop system.

The process transfer function $P(s)$ can be deduced from the derived plant model in Equation (3.29). As the grid voltage v_{g} is measurable, the dependency on this quantity is suppressed using feedforward in the output current controller. This allows for a simplification of the plant model and results in the process transfer function as given in Equation (6.5). Note that Equation (6.5) contains an additional term $e^{-T_{\mathrm{d}}s}$, which prescribes the time delay of the control system. As the Imperix controller is implemented digitally, the system encounters a control delay and a modulator delay. A detailed review of the delays encountered in the Imperix MMC is provided in Appendix B.3.

$$P(s) = \frac{i_{\mathrm{s}}}{v_{\mathrm{s}}} = \frac{2}{sL + R} * e^{-T_{\mathrm{d}}s} \tag{6.5}$$

The controller transfer function $C(s)$ represents the input-output relation of PI controller and is given in Equation (6.6). Note that Equation (6.1), is the discrete time implementation of Equation (6.6) using the forward Euler method and given the sampling period T_{s} [34]. Following this discretisation method, the controller gains can by definition be preserved.

$$C(s) = \frac{v_{\mathrm{s}}^*}{\xi} = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s} \tag{6.6}$$

Using the MO tuning method, the proportional gain K_{p} and integral gain K_{i} can be found that comply with Equations (6.2) and (6.3) for the largest number of r possible. In accordance with [33], a process transfer function $P(s)$, that has a standard form as in the first part of Equation (6.7), can be developed into the infinite series as the second part of Equation (6.7). By which the transformation is performed using a infinite Pade series of $e^{-T_{\mathrm{d}}s}$ and A_0,A_1,... represent the characteristic areas.

$$P(s) = K_{\mathrm{M}} \frac{1 + b_1 s + b_2 s^2 + \cdots + b^m s^m}{1 + a_1 s + a_2 s^2 + \cdots + a^n s^n} e^{-T_{\mathrm{d}}s} = A_0 - A_1 s + A_2 s^2 - A_3 s^3 + \ldots \tag{6.7}$$

Then applying Equation (6.5) to the conversion in (6.7) results in the following characteristic areas:

- $A_0 = 2/R$

- $A_1 = 2/R(T_\mathrm{d} + L/R)$
- $A_2 = 2/R(T_\mathrm{d}^2/2) + A_1 L/R$
- $A_3 = 2/R(T_\mathrm{d}^3/6) + A_2 L/R$

Following the MO tuning method, the proportional gain K_p and integral gain K_i are then defined as a function of the characteristic areas indicated in Equation (6.8).

$$\begin{bmatrix} K_\mathrm{i} \\ K_\mathrm{p} \end{bmatrix} = \begin{bmatrix} -A_1 & A_0 \\ -A_3 & A_2 \end{bmatrix}^{-1} \begin{bmatrix} -0.5 \\ 0 \end{bmatrix} \tag{6.8}$$

Using the Imperix parameters of Appendix B.2 and the process delay of Appendix B.3, the characteristic areas are determined. Then with Equation (6.8) the gains are calculated at: $K_\mathrm{p} = 3.125$, $K_\mathrm{i} = 75$.

With these gains, the closed-loop behaviour of the output current controller can be analysed. Figures 6.11 and 6.12 show the performance of the closed-loop system in the frequency domain and time domain, respectively. Figure 6.11 provides the Bode plot of $G_\mathrm{CL}(j\omega)$. From this figure can be concluded that the closed-loop system has a cut-off frequency at $5.6 * 10^3 rad/s$, with a flat 0dB magnitude response up to the control system bandwidth. This result can be compared with the closed-loop bandwidth statement of Section 3.3. Equation (3.31) indicated that the closed-loop bandwidth $\alpha_c \leq \frac{\omega_s}{10} = 3.14 * 10^3 rad/s$ in order for the control to remain mostly unaffected by the switching behaviour. Note that the MO tuning method could extend this conservative limit by considering the actual process delay. This resulted in a larger output current control bandwidth, which equates to a faster control operation.

Figure 6.12 shows the step response of the closed-loop system. It can be concluded that the output current controller achieves a zero steady-state error with a settling time of less than $\tau_s = 2ms$. Besides, the overshoot of the step response is limited to 4% of the nominal value. To ensure a stable operation of the output current controller, the stability margins of the open-loop transfer function are determined. The gain margin $GM = 9.94$dB, the phase margin $PM = 61.3$deg. As both the gain margin and phase margin are significantly positive, the closed-loop system can be defined to be stable.

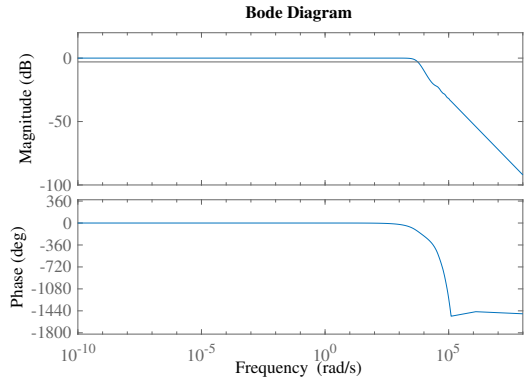


Figure 6.11: Bode plot of closed-loop transfer output current control.

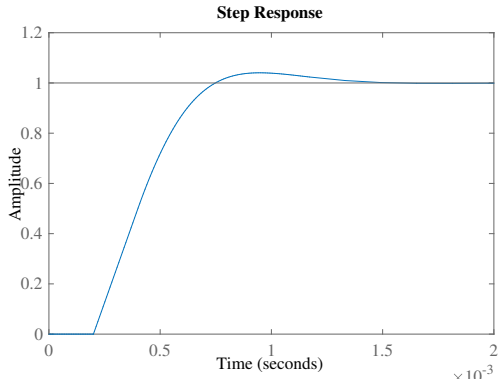


Figure 6.12: Step response of closed-loop transfer output current control.

To verify the workings of the output current controller, a Submodule-Level Averaged (SLA) simulation is performed. Figure 6.13 show the simulated step response of the d-axis component of the output current $i_\mathrm{s,d}$. It can be concluded that the $i_\mathrm{s,d}$ accurately follows the reference value in steady-state. The transient behaviour shows a steady increase of $i_\mathrm{s,d}$ without significant overshoot.

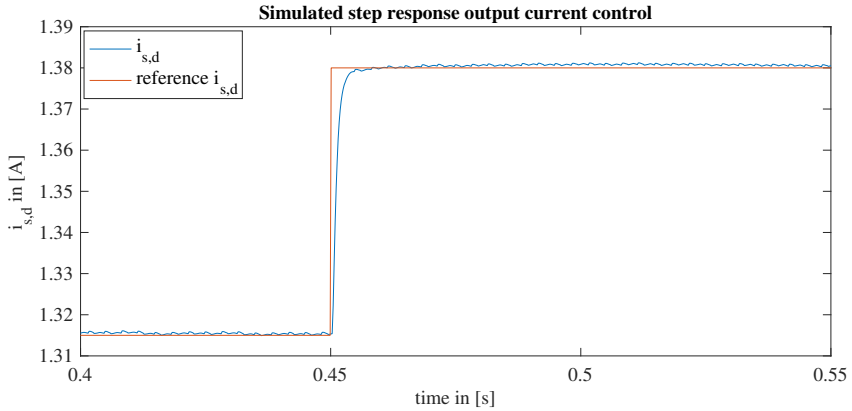


Figure 6.13: Simulated step response of output current control.

6.2.4 Energy balancing control

In Section 3.4 the energy balancing controller was introduced. This controller is required as the SM capacitors are inserted at different time points, thus encountering different operational conditions. This in turn leads to a deviation from the desired operation point for: the SM capacitor voltage $v^{\mathrm{i}}_{\mathrm{cu,l}}$, the arm average capacitor voltage $\bar{v}_{\mathrm{cu,l}}$ and the leg average capacitor voltage $\bar{v}_{\mathrm{c}}$. These deviations negatively impact the stability of the Imperix MMC and its output harmonic performance. Therefore, the energy balancing controller is implemented for the Imperix MMC to regulate the three quantities. Combined with the SM balancing controller, this controller can maintain the SM energies at the set-point.

Circulating current controller

As mentioned in Section 3.4.2, the energy balancing in the MMC is performed via alternating the circulating current. Therefore, the first part of the energy balancing control is the circulating current controller. The Imperix implementation of the circulating current controller is provided in Figure 6.14. This controller defines the internal voltage reference v^*_{c} to eliminate the error in circulating current $i^*_{\mathrm{c}} - i_{\mathrm{c}}$. The structure of the circulating current controller is similar to the one provided in Figure 3.9. Though, note that the Imperix implementation does provide feedback on the DC component in i_{c}. This was found to be vital for the control of the total energy, as is discussed later. Furthermore the PR controller in Figure 3.9 is replaced by a combination of a discrete-time PI controller and two discrete-time PR controllers, at the line frequency ω_1 and double-line frequency $2\omega_1$. In line with [15], the circulating current controller is directly implemented for the individual submodule, providing $v^*_{\mathrm{c}}/4$ instead of v^*_{c}.

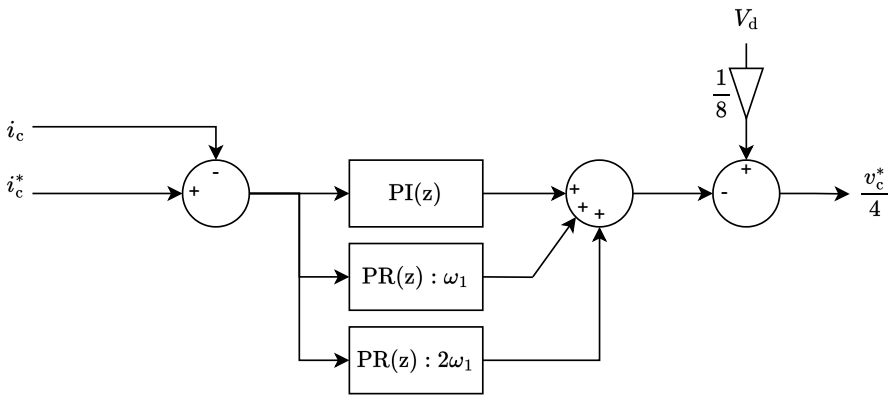


Figure 6.14: Imperix circulating current controller implementation.

Recall the transfer function of the discrete-time PI controller that was provided in Equation (6.1). This discrete-time implementation was found by performing the forward Euler method on the continuous-

time implementation in Equation (6.6). A similar conversion can be performed for the PR controller. As introduced in Section 3.4.1 the ideal PR controller has a continuous-time transfer as in Equation (6.9). However, as mentioned in [35], the ideal PR controller can cause stability issues when implemented digitally. Therefore, the non-ideal PR controller is proposed with a continuous-time transfer as in Equation (6.10).

$$PR(s) = K_\mathrm{p} + \frac{2K_\mathrm{r}s}{s^2 + \omega_0^2} \tag{6.9}$$

$$PR(s) = K_\mathrm{p} + \frac{2K_\mathrm{r}\omega_\mathrm{c}s}{s^2 + 2\omega_\mathrm{c}s + \omega_0^2} \tag{6.10}$$

In these equations ω_0 is the resonant frequency, and ω_c is the resonant cut-off frequency or the width of the resonant filter. Then applying the bilinear transform on Equation (6.10), the discrete-time transfer function is found as provided in Equation (6.11). For implementing the discrete-time PR controller in the Imperix MMC, the PR-controller block is used as part of the ACG SDK software. Which implements the PR controller transfer as defined in Equation (6.11).

$$\begin{aligned} PR(z) &= K_\mathrm{p} + \frac{b_0\left(z^{-1} - z^{-2}\right)}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \\ b_0 &= 4K_\mathrm{i}T_\mathrm{s}\omega_\mathrm{c} \\ a_0 &= T_\mathrm{s}^2\omega_0^2 + 4T_\mathrm{s}\omega_\mathrm{c} + 4 \\ a_1 &= 2T_\mathrm{s}^2\omega_0^2 - 8 \\ a_2 &= T_\mathrm{s}^2\omega_0^2 + 4T_\mathrm{s}\omega_\mathrm{c} + 4 \end{aligned} \tag{6.11}$$

For the implementation of the circulating current controller the proportional gain K_p, integral gain K_i and two resonant gains K_r1, K_r2 must be determined. As the control of the DC component of i_c can be seen as a separate task form the control of the ω_1, $2\omega_1$ components, the K_p and K_i are again tuned using the MO tuning method. The tuning is performed similar to the output current controller, with the main difference being a change in the process transfer function. The process transfer function $P(s)$ can be deduced from the derived plant model in Equation (3.35). As the DC link voltage v_d is measurable, the dependency on this quantify can be suppressed using feedforward in the circulating current controller. This allows for a simplification of the plant model and results in the process transfer function as given in Equation (6.12) where the $e^{-T_\mathrm{d}s}$ term models the system delay.

$$P(s) = \frac{i_\mathrm{c}}{v_\mathrm{c}} = \frac{1}{sL+R} * e^{-T_\mathrm{d}s} \tag{6.12}$$

Then using the controller function of Equation (6.6), the Imperix parameters of Appendix B.2 and the process delay of Appendix B.3, the MO tuning method can be applied to find the controller gains at: $K_\mathrm{p} = 8.33/4 = 2.1$, $K_\mathrm{i} = 200/4 = 50$. Note the division by 4 as the output of the circulating current controller is implemented for an individual submodule.

With these gains, the closed-loop behaviour of the circulating current controller can be analysed. Figures 6.15 and 6.16 show the performance of the closed-loop system in the frequency domain and time domain, respectively. Figure 6.11 provides the bode plot of the closed-loop transfer with a PI controller. It can be concluded that the system has a cut-off frequency at $7.4 * 10^3 rad/s$, with a flat 0dB magnitude response up to the control system bandwidth. Because of the MO tuning method, the circulating current controller has a large control bandwidth, which equates to a fast control operation. Figure 6.16 shows the step response of the closed-loop system. It can be concluded that the circulating current controller achieves a zero steady-state error with a settling time of less than $\tau_s = 1.4ms$. Besides, the overshoot of the step response is limited to 4% of the nominal value.

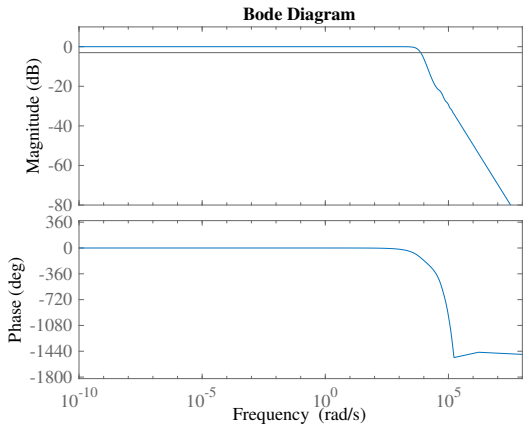


Figure 6.15: Bode plot of closed-loop transfer circulating current control.

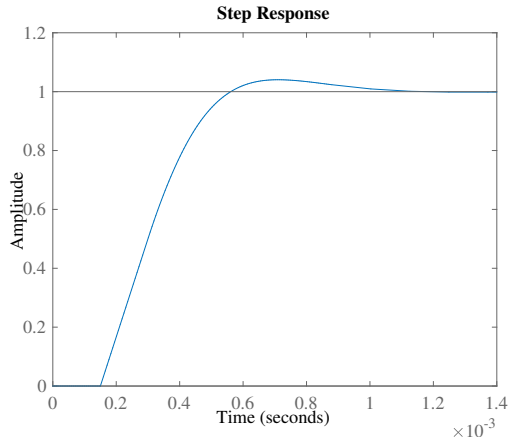


Figure 6.16: Step response of closed-loop transfer circulating current control.

For the control of the line frequency and double-line frequency components in i_c the two resonant controllers are set at resonant frequency $\omega_0 = \omega_1$ and $\omega_0 = 2\omega_1$ both with a resonant cut-off frequency of 15 rad/s, as proposed in [35]. The selection of the resonant gains is done via iterative tuning using the SLA simulated system response. After various iterations the gains were defined at: $K_{r1} = K_{r2} = 16$. In addition it was found that a slight increase in the integral gain was beneficial to the system response, resulting in $K_i = 80$. Note that, because of the design, the addition of the resonant controllers and change in integral gain does not effect the systems cut-off frequency.

To ensure a stable operation of the circulating current controller, the stability margins of the open-loop transfer function are determined. Figure 6.17 shows the gain margin $GM = 9.59$dB and the phase margin $PM = 52.4$deg of the complete system. As both the gain margin and phase margin are significantly positive, the closed-loop system can be defined to be stable.

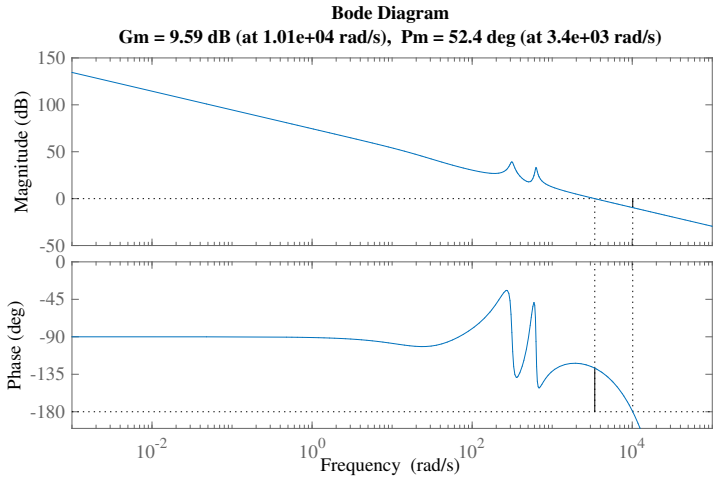


Figure 6.17: Bode plot of the open-loop transfer for the circulating current controller.

For the circulating current controller a reference i_c^* is required. This reference comprises three components as indicated in Figure 6.18. The first component is a feedforward of the DC side current reference $id^*/3$. It is obtained from the division of the active power reference and DC link voltage V_d. As the measured V_d contains high-frequency components, two filters are used to eliminate ripples. $H_1(z)$ is a 50Hz Notch filter, $H_2(z)$ is a 20Hz second-order Butterworth low-pass filter. Both are converted from continuous-time to discrete-time using the Zero-Order Hold (ZOH) method. The second and third com-

ponents, $\Delta i^*_{c,1}$ and $\Delta i^*_{c,2}$, are outputs of the leg energy balancing controller and decoupled arm energy balancing controller, respectively. There combined performance relates to Δi^*_c in Equation (3.42).

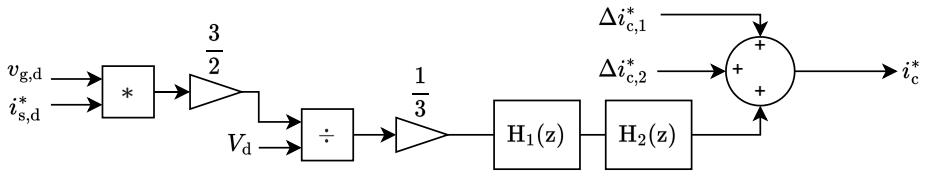


Figure 6.18: Imperix circulating current reference.

Leg energy balancing controller

The second part of the energy balancing control is the leg energy balancing controller [36]. This controller regulates the total energy W_Σ stored in an MMC leg. It can be conduced form Equations (3.38) and (3.39), that the control of W_Σ to its reference $W_{\Sigma 0}$ is equivalent to the control of $\bar{v}_c$ to $V^*_d/4$. Were $\bar{v}_c$ is the leg average capacitor voltage defined in Equation (6.13).

$$\bar{v}_c = \frac{v^\Sigma_{cu} + v^\Sigma_{cl}}{2N} \tag{6.13}$$

For the Imperix implementation of the leg energy balancing controller, a structure similar to the one proposed in [15] is used. The controller circuit is provided in Figure 6.19, defines the change in the circulating current reference $\Delta i^*_{c,1}$ such that the discrepancy between $\bar{v}_c$ and its reference $V^*_d/4$ is eliminated. Note that Figure 6.19, also contains three input filters. These filters are used to remove the double-line frequency ripple in on $\bar{v}_c$, as was shown to be present in Equation (4.6). This 100Hz component would otherwise be detrimental to the performance of the controller. Therefore, $H_3(z)$ is a 100Hz Notch filter, and $H_4(z)$ is a 50Hz second-order Butterworth low-pass filter. Both are converted from continuous-time to discrete-time using the ZOH method.

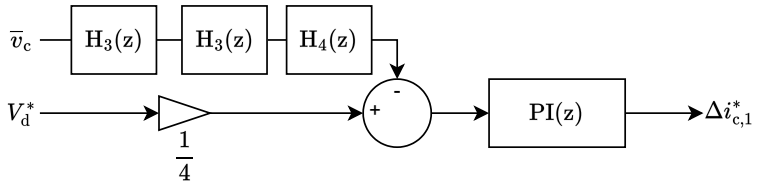


Figure 6.19: Imperix leg energy balancing controller implementation.

For the implementation of the leg energy balancing control a discrete-time PI controller is used. The selection of the proportional and integral gain is done via iterative tuning using the SLA simulated system response. After various iterations the proportional and integral gain were defined at: $K_p = 0.12$, $K_i = 0.93$.

Arm energy balancing controller

The final part of the energy balancing control is the arm energy balancing controller. This controller regulates the imbalance energy W_Δ that exists between the upper and lower arm of an MMC leg. Similar to the total energy, it can be conduced from Equations (3.38) and (3.39), that forcing W_Δ to 0 is equivalent to forcing $\bar{v}_{cu} - \bar{v}_{cl}$ to 0. Where $\bar{v}_{cu,l}$ is the upper/lower arm average capacitor voltage.

To actively reduce the discrepancy between the upper and lower arm average capacitor voltage, the arm energy balancing controller is implemented for the Imperix MMC. Figure 6.20, illustrates the implementation, were the change in circulating current reference $\Delta i^*_{c,2}$ is defined to make $\bar{v}_{cu} - \bar{v}_{cl}$ zero. Note that the difference in average arm capacitor voltage has a 50Hz ripple component, as was seen in Equation

(4.7). Therefore a double 50Hz Notch filter $H_1(z)$ is used in line with the input to remove the fundamental discrepancy ripple from the control.

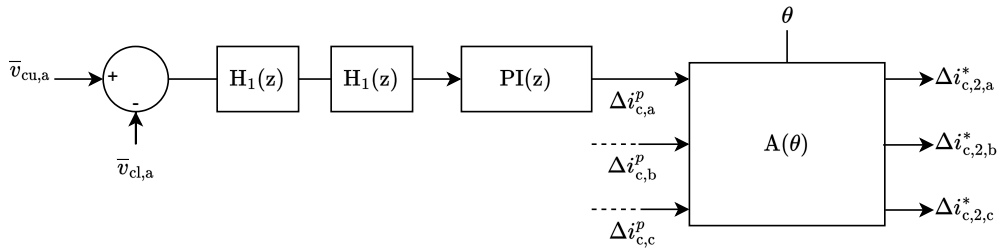


Figure 6.20: Imperix decoupled arm energy balancing controller implementation.

Recall from Section 3.4.2, that to reduce the imbalance energy W_Δ a fundamental frequency i_c component is needed that is in line with the output voltage V_s. Equation (3.40), showed that a constant i_c does provide no net contribution to the change in W_Δ. The output of the PI controllers $\Delta i^p_{\text{c,2}}$ thus give the amplitude of a 50Hz circulating current component. Though, one drawback of this control is the coupling of the three phases with each-other and the DC link current. If phase a has an arm imbalance, this 50Hz component would appear in i_d in case $i_{\text{c,b}}$ and $i_{\text{c,c}}$ are fixed. Or if i_d is fixed it causes a 50Hz ripple in $i_{\text{c,b}}$ and $i_{\text{c,c}}$, shifting the imbalance energies in the MMC. In [36] a decoupling strategy is proposed for a Static Synchronous Compensator (STATCOM), but this method can also be applied for DC link applications to improve the operational performance. Equation (6.14) shows the decoupling of $\Delta i_{\text{c,2}}$ among the three phases, completing the decoupled arm energy balancing controller. With $\theta = \omega_1 t$ being the grid phase angle.

$$\begin{bmatrix} \Delta i^*_{\text{c,2,a}} \\ \Delta i^*_{\text{c,2,b}} \\ \Delta i^*_{\text{c,2,c}} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \frac{1}{\sqrt{3}}\cos(\theta+\frac{1}{2}\pi) & \frac{1}{\sqrt{3}}\cos(\theta-\frac{1}{2}\pi) \\ \frac{1}{\sqrt{3}}\cos(\theta-\frac{7}{6}\pi) & \cos(\theta-\frac{2}{3}\pi) & \frac{1}{\sqrt{3}}\cos(\theta-\frac{1}{6}\pi) \\ \frac{1}{\sqrt{3}}\cos(\theta+\frac{7}{6}\pi) & \frac{1}{\sqrt{3}}\cos(\theta+\frac{1}{6}\pi) & \cos(\theta+\frac{2}{3}\pi) \end{bmatrix} \begin{bmatrix} \Delta i^p_{\text{c,a}} \\ \Delta i^p_{\text{c,b}} \\ \Delta i^p_{\text{c,c}} \end{bmatrix} \tag{6.14}$$

For the implementation of the arm energy balancing control discrete-time PI controllers are used. The selection of the proportional and integral gain is again done via iterative tuning using the SLA simulated system response. After various iterations the proportional and integral gain were defined at: $K_\text{p} = 0.35$, $K_\text{i} = 0.04$.

Simulation of the energy balancing controller

To verify the workings of the energy balancing controller, the complete system is simulated with the SLA model. The MMC is then initialised with unbalanced upper and lower arm average capacitor voltage $\bar{v}_{\text{cu,l}}$. Figure 6.21 shows the simulation results, indicating the arm average capacitor voltages of the MMC over time. The simulation is performed at a DC link voltage reference $V^*_\text{d} = 70V$ therefore the reference of $\bar{v}_{\text{cu,l}}$ is set at 17.5V. Note that at the start of the simulation, the upper arm capacitors have a higher voltage of +1V and the lower arm capacitors have a smaller voltage of -0.5V. There is thus an initial arm energy imbalance and leg energy imbalance. During the first 0.2s of the simulation, the energy balancing controller is disabled. After $t = 0.2s$ both the arm energy balancing and leg energy balancing are activated.

From Figure 6.21 it can be concluded that the initial divergence in average arm capacitor voltage is maintained during the first 0.2s of the simulation. This indicates that there is no inherent asymptotic stability of the capacitor voltages. After $t = 0.2s$ the energy balancing control is activated, which causes the arm capacitor voltages to converge to the reference of 17.5V. Note that both the initial leg imbalance $\bar{v}_\text{c} \neq 17.5V$ and initial arm imbalance$\bar{v}_{\text{cu,l}} \neq \bar{v}_{\text{cu,l}}$ is dissolved by the control, within a 0.6s time-span.

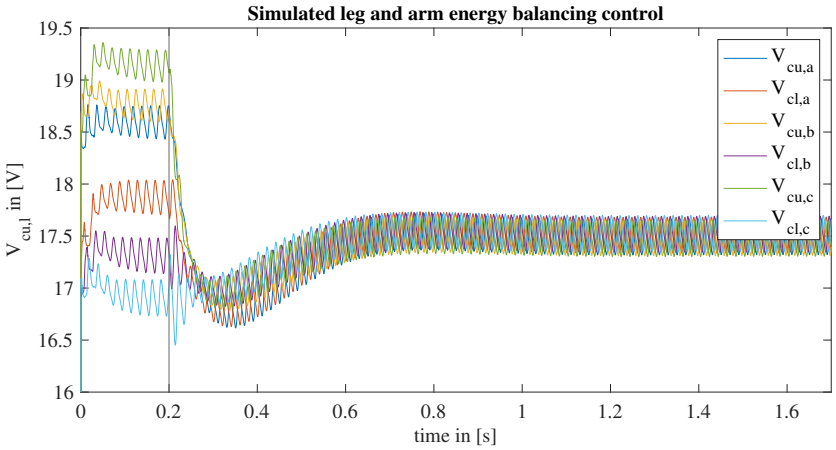


Figure 6.21: Simulated operation leg and arm energy balancing.

6.2.5 Higher-level control

The final part of the control implementation for the Imperix MMC is the higher-level control. As was discussed in Section 3.6, the higher-level control performs multiple tasks simultaneously using smaller controllers. It should be noted that the bandwidth and thus the speed of the higher-level control is small compared to the output current controller. This restriction is imposed to ensure control separation.

The phase-locked loop implementation of the Imperix is achieved using the PLL-block that is part of the ACG SDK software. The PLL is positioned in a feedback loop for the grid voltage v_g around the *abc* to *dq* transformation, similar to Figure 3.12. Note that the PI controller, that forces the quadrature component $v_{g,q}$ to zero, is implemented in the discrete domain. The proportional and integral gain of the PLL were defined at: $K_p = 5$, $K_i = 2$. The output of the PLL, the grid angle θ, is then used by the output current control and arm energy balancing control.

Besides the PLL, the higher-level control defines the output current reference i_s^*. The control circuit is provided in Figure 6.22 where i_s^* is defined such that both the DC link voltage and the reactive power are operated at the desired set-point. For the control of the reactive power Q, an open-loop structure is chosen. This is performed according to the control law of Equation (3.47). Note that the open-loop control design can cause a steady-state error in the output reactive power. Though, this error is justified for the DC distribution link application.

Figure 6.22 also contain the DC-link voltage control. As mentioned in Section 3.6.3, the DC link voltage control regulates the DC side voltage of the MMC. As can be concluded from [11, 14, 37–39] there are two commonly proposed DC link voltage control structures in literature. The first, uses the squared inputs: $v_d^2 - v_d^{*2}$ to define the active power reference P^*. This structure is based on alternation of the DC link energy as was explained in Section 3.6.3. For the Imperix MMC the second approach is implemented. This approach, that is proposed in [14] and uses the error in the DC link voltage $v_d - v_d^*$ to define the reference of the direct-axis output current component $i_{s,d}^*$. This provides a simplified DC link voltage controller implementation that is stable over a wide operational range of V_d.

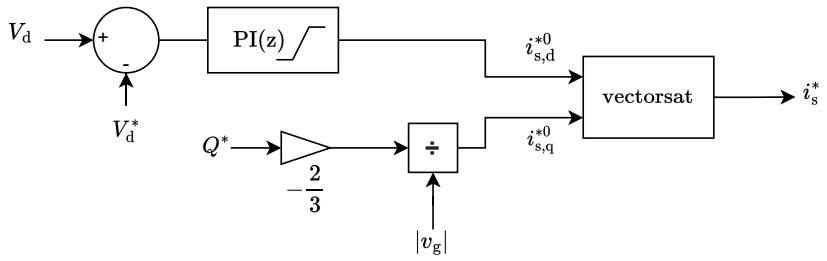


Figure 6.22: Imperix higher level control implementation.

For the implementation of the DC-link voltage control, a discrete-time PI controller is used. The selection of the proportional and integral gain is done via tuning using the SLA simulated system response. Figures 6.23 and 6.24 show the DC link voltage response of the MMC for a input reference step. Figure 6.23 shows the V_d step response for different proportional gains K_p. As was concluded in Chapter 4, the DC link voltage enhancement has a strict limit $k_{d,max}$. Any bypass of $k_{d,max}$ impacts the AC-side harmonic performance of the MMC. Therefore large overshoots in V_d over V_d^* should be limited as much as possible. Analysing Figure 6.23 with this constraint results in selection of $K_p = 0.03$. This proportional gain limits overshoot and results in a fast transition to steady state. Similarly, Figure 6.24 shows the V_d step response for different integral gains K_i. Analysing Figure 6.24 with the same constraint results in selection of $K_i = 1.25$. This integral gain limits overshoot without compromising on the fast transition to steady state, as would be the case with a lower K_i.

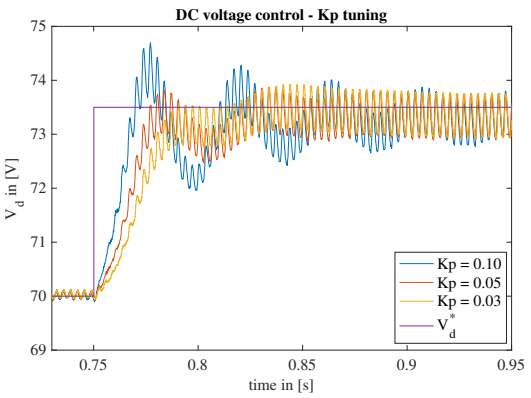


Figure 6.23: Simulated step response of DC link voltage controller for different K_d.

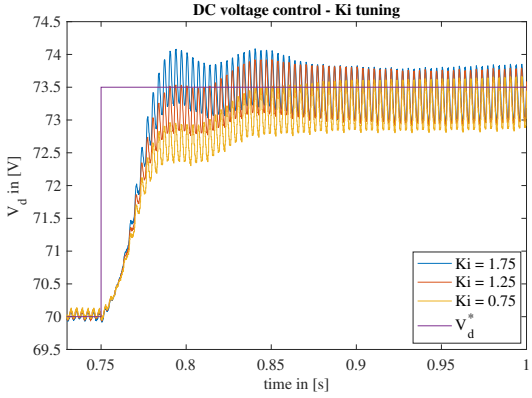


Figure 6.24: Simulated step response of DC link voltage controller for different K_i.

Besides the discrete-time PI control also saturation is performed in the controller. This saturation limits the direct axis output current reference to the maximum of $i_{s,d} = 5A$. This constrain is set by the DC-side load as mentioned in Appendix D.2. To constraint also the quadrature axis component of i_s a vector saturation is used to limit $|i_s| \leq 15A$ as was explained in Section 3.3.

To check the workings of the DC link voltage control, an experimental verification is performed. Figure 6.25, shows the measured DC link voltage response of the Imperix MMC when the input transitions from $V_d^* = 100V$ to $V_d^* = 105V$ at time-point $t = 3.2s$. It can be concluded from this figure that, the DC link voltage control can achieve accurate reference tracking during steady state conditions. In addition, the controller is able to alter the DC link voltage, following the reference step. This is achieved with limited overshoot and a settling time of 0.49s. From this can be concluded that the DC link voltage control performs as intended.

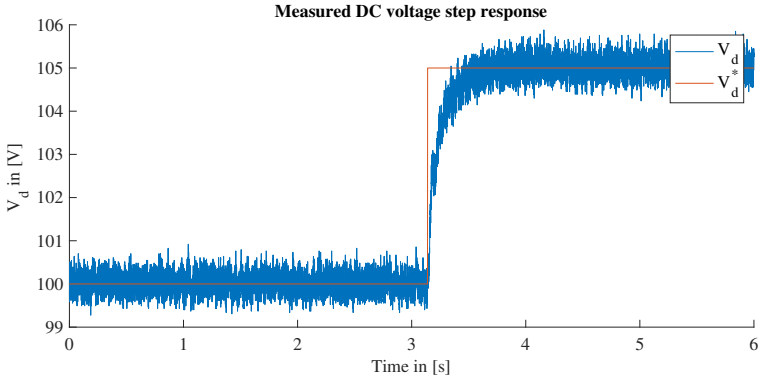


Figure 6.25: Measured step responses of DC link voltage control.

6.3 Dynamic DC link voltage control

The final implemented module for the Imperix MMC is the dynamic DC link voltage control. This controller, as discussed in Chapter 5, is used to dynamically alter the DC link voltage reference given the operational reactive power injected into the AC network. Two controllers were proposed to incorporate the dynamic DC link enhancement: the direct controller and open-loop controller. As was concluded from the simulations in Chapter 5, the direct controller injects harmonic components during system transients, which are detrimental to the performance of the MMC. Therefore the more robust open-loop controller is used to implement the dynamic DC link voltage control.

As discussed in Section 5.3, the open-loop DC link voltage control was designed using a finite state machine. The FSM is defined in Matlab using the Stateflow library, which has a structure similar to Figure 5.3. As the FSM requires to retain certain variables, memory blocks are used in the implementation. The overall positioning of the FSM is shown in Figure 6.26. Note that for the dynamic DC link voltage control the DC link voltage reference of the higher-level control in Figure 6.22 is defined as $V_{\mathrm{d}}^{*} = k_{d}^{*} V_{\mathrm{dr}}$. However, to maintain the average sum capacitor voltage, the DC link voltage reference of the leg energy balancing control in Figure 6.19 is defined as $V_{\mathrm{d}}^{*} = V_{\mathrm{dr}}$.

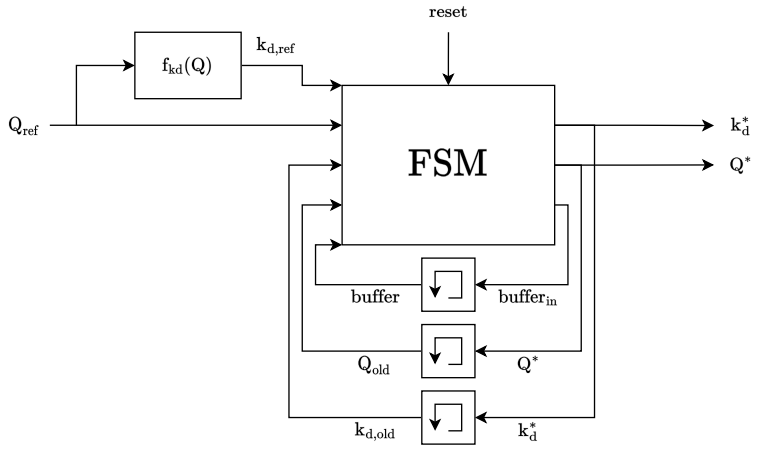


Figure 6.26: Implementation of open-loop DC link voltage control.

To verify the workings of the dynamic DC link voltage control, an experimental verification is performed. For this the parameters τ_{startup}, τ_{kd} and τ_{Q} are tuned for the Imperix MMC and are set at:

- $\tau_{\mathrm{startup}} = 2.0s$

- $\tau_{\text{kd}} = 0.5s$
- $\tau_{\text{Q}} = 0.25s$

Figure 6.27 provides the outcome of the experiment. The figure shows the state of the FSM, the input/output reactive power reference Q_{ref}, Q^* and the input/output enhancement factor $k_{\text{d,ref}}$, k_{d}^* as a function of time. Initially the reset is set high, by which the FSM machine maintains in the *safe steady state* and k_{d}^* is fixed at 1. Around $t = 2s$ the reset is turned low, and after $\tau_{\text{startup}} = 2.0s$ the FSM transitions to the *pre enhanced state*. k_{d}^* now matches the input reference $k_{\text{d,ref}}$. After $\tau_{\text{kd}} = 0.5s$ the FSM transitions to the *enhanced steady state*. Then sequentially, the open-loop controller transitions through an increase and decrease in Q_{ref} sequence, providing the appropriate outputs ans following the given timings $\tau_{\text{kd}} = 0.5s$ and $\tau_{\text{Q}} = 0.25s$. Finally, the controller returns safely to the *safe steady state* after the reset is set high. From this, it can be concluded that the open-loop DC link voltage control performs as specified [40].

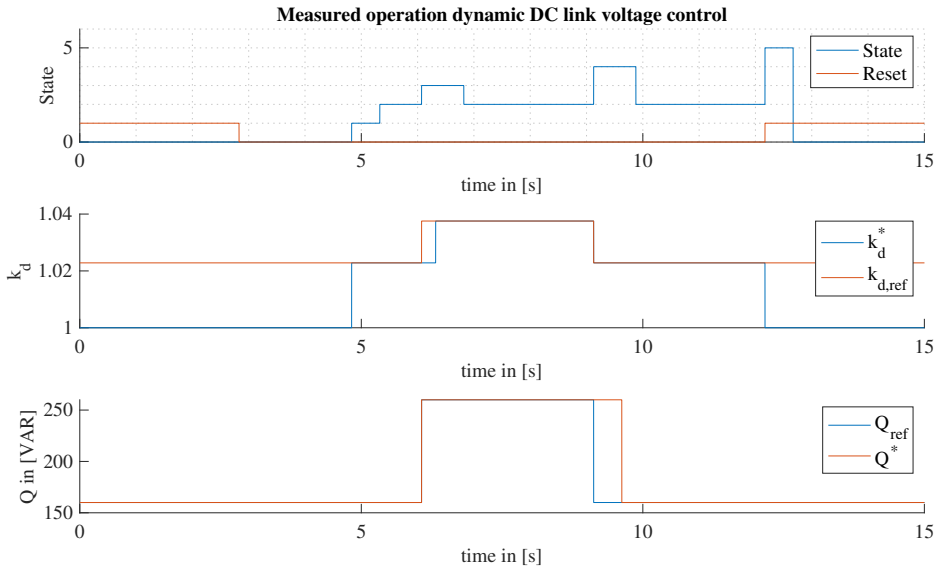


Figure 6.27: Measured operation of the open-loop DC link voltage control.

Chapter 7

Experimental Verification

In Chapter 4, the idea was proposed to operate a MMC-based MVDC distribution link at an enhanced DC voltage $V_{\mathrm{d}} > V_{\mathrm{dr}}$ while maintaining the same average energy stored in the MMCs. Following the analytical calculations, Equation (4.19) was constructed. This equation gave the boundary of the DC link voltage enhancement $k_{\mathrm{d,max}}$ as a function of the system and operating parameters. As the DC link voltage enhancement is proposed as a mathematical concept, experiments are used to back up the given claims. Therefore, this chapter examines the DC link voltage enhancement concept via experimental measurements. These measurements are used to demonstrate the working concept, verify the analytical enhancement boundary and show the performance of the dynamic DC link voltage control. Combined, this provides an experimental verification for the power transfer capacity increase achieved when operating an MVDC distribution link under dynamic DC link voltage control. For the experiments the lab-scale Imperix MMC is used, with the implemented control strategy defined in Chapter 6.

The first section of this chapter, Section 7.1, describes the measurement setup which is used during the experiments. Second, Section 7.2 experimentally demonstrates the workings of the DC link voltage enhancement. Then, in Section 7.3 the enhancement boundary is examined using steady-state measurements. Finally, Section 7.4 discusses the performance of the open-loop dynamic DC link voltage controller during system transients.

7.1 Measurement setup

For the execution of the experiments, a measurement setup is used. As discussed in Chapter 6, the setup contains the lab-scale Imperix MMC, for which a detailed overview is provided in Appendix D.1. The MMC, which is constructed in a double-star configuration, is shown in Figure 7.3. The figure shows the three MMC legs (a,b,c) that each contain $2N = 8$ submodules. These submodules are regulated by the three B-Box RCP controllers that acquire measurement data and run the control code. The submodules are operated in a half-bridge configuration and have a submodule capacitance of $C = 5.0mF$. The six MMC arms are connected to the arm inductors, each with an inductance of $L = 2.5mH$. Further information on the Imperix parameters can be found in Table B.2.

The Imperix MMC is connected to the measurement setup, which contains: three parallel DC loads, an AC power supply, a DC power supply and the measurement instruments. An overview of the complete measurement setup is provided in Figure 7.2 where the individual devices are defined as follows:

- DC loads: three variable power resistors: $[0\Omega, 65\Omega]$ and rated at $5A$.
- DC power supply: Delta Elektronika SM6000 Series: $[0V, 300V]$ and $[0A, 20A]$.
- AC power supply: Cinergia GE20: four-quadrant AC grid emulator and electronic load.
- Oscilloscope: Yokogawa DLM2034
- Voltage probes: Keysight Technologies N2791A / Testec TT-SI9101
- Current probe: Keysight Technologies N2782B

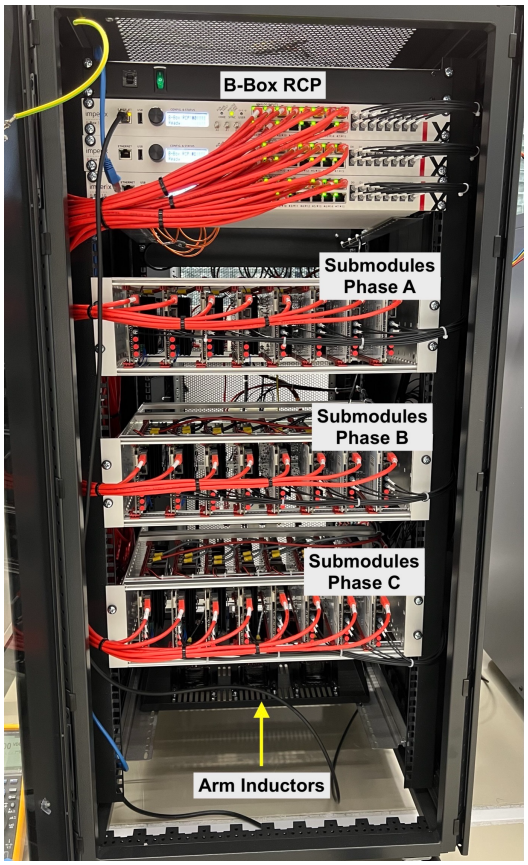


Figure 7.1: Internal configuration of the Imperix MMC.

Figure 7.2: Complete measurement setup with the Imperix MMC, DC loads, probes, DC and AC supply.

More information about the devices and measurement setup can be found in Appendix D. To further clarify the layout of the measurement setup in Figure 7.2, Figure 7.3 can be used. This figure provides a schematic overview of the measurement setup and indicates the probes placement. It becomes clear that the Imperix MMC is connected directly to the Cinergia GE20, which functions as an AC power supply. The Cinergia supplies the active power for, and absorbs the reactive power of, the converter ($P < 0$,$Q \geq 0$). The operating parameters of the AC power supply, which are used during measurements, are provided in Table 7.1.

In addition to the AC-side, Figure 7.3 indicates that the DC-side of the Imperix MMC is connected to the parallel load resistors R_{load}, the multimeter and the DC power supply. The DC power supply is used during the startup of the MMC and functions as a backup for the DC link voltage control. During normal operation, the output of the DC source $V_{\text{dc,source}}$ is fixed below the rated DC voltage V_{dr}, which makes the internal power diode operate in reverse bias. As a result, the DC-side of the MMC is solely characterised by the load resistance R_{load}. The operating parameters of the DC power supply, which are used during the experiments, are provided in Table 7.1.

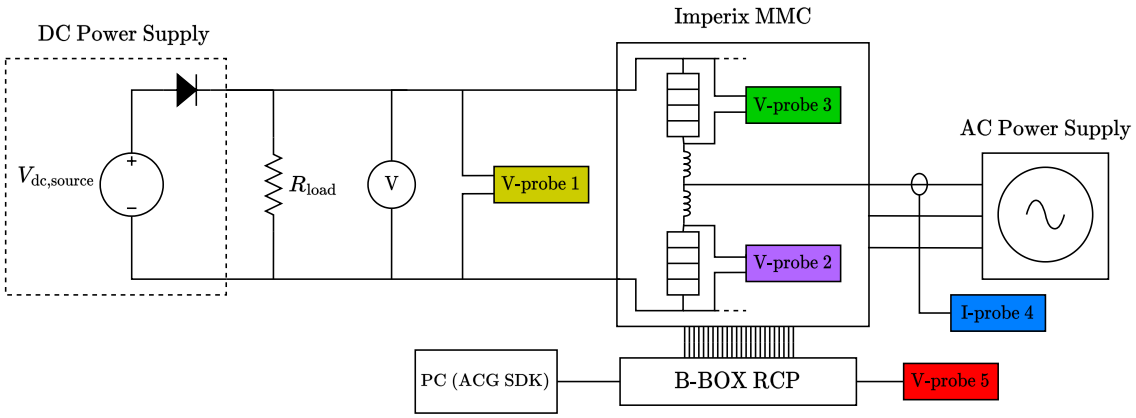


Figure 7.3: Schematic overview of the measurement setup.

Table 7.1: Operating parameters of the AC and DC side during experiments

Operating parameters		
AC grid:		
Grid frequency	ω_{l}	314.2 rad/s
Grid voltage L-N (rms)	v_{g}	33.7V
Phase current limit	$i_{\text{g,max}}$	8A
DC link:		
Rated DC link voltage	V_{dr}	100V
DC source voltage	$V_{\text{dc,source}}$	55V
DC side load	R_{load}	30Ω

Figure 1.1 showed the MMC-based MVDC distribution link which was composed of two back-to-back connected MMCs. The measurement setup in Figure 7.3 resembles the distribution link but uses only one modular multilevel converter. In the measurement setup, the other MMC of the distribution link is emulated by the power resistors. Note that the controller of the MMC is used to set the DC-link voltage V_{d}. Meanwhile, the power transfer of the link is defined through the load resistors. Although this setup limits the operating region of the distribution link, the measurement setup resembles the setup of two back-to-back configured MMCs.

In addition to the configuration of the AC and DC side of the MMC, Figure 7.3 shows the placement of the probes. The measurement instruments consist of four differential probes and one current probe, which are all connected to the Yokogawa DLM2034 oscilloscope. The probe configuration is defined as follows:

- V-probe 1: Measures the DC voltage across the power resistors V_d.
- V-probe 2: Measures the lower arm voltage v_l of phase a.
- V-probe 3: Measures the upper arm voltage v_u of phase a.
- I-probe 4: Measures the output current i_s of phase a.
- V-probe 5: Measures the sum capacitor voltage v_cu^Σ of the upper arm of phase a.

Note that using the upper and lower arm voltage measurements, the output voltage v_s can be calculated during post-processing. Besides, observe that the sum capacitor voltage measurement is obtained via the B-Box RCP. The B-Box RCP adds the measured SM capacitor voltages v_cu^i in the upper arm and provides the result at the analog output. Due to the internal processing time of the B-Box RCP, the output encounters a delay of 1 control cycle: $1/f_\mathrm{s}$. This delay is compensated during post-processing.

7.2 Workings of the DC link voltage enhancement

The first experiment is performed to verify the workings of the DC link voltage enhancement. The enhancement process was illustrated using Figure 4.1, which showed the sum capacitor voltage v_cu^Σ and upper arm voltage v_u as functions of time. The plot indicated that the ripple in the sum capacitor voltage, caused by the reactive arm current component, created a spacing between v_cu^Σ and v_u. This space was then used for biasing the arm voltage without violating constraint (4.1). An increment in the DC component of the arm voltage then directly appear at the DC terminal, increasing V_d above V_dr. To quantify the spacing between v_cu^Σ and v_u, consider the definition of the spacing voltage V_space. V_space is defined as the minimal distance between the sum capacitor voltage v_cu^Σ and the arm voltage v_u that is encountered over a fundamental period T_l as expressed in Equation (7.1).

$$V_\mathrm{space} = min\left(v_\mathrm{cu}^\Sigma(t) - v_\mathrm{u}(t)\right) \qquad with \quad t \in [(i-1)T_\mathrm{l}, iT_\mathrm{l}] \; and \; i \in \mathbb{Z} \tag{7.1}$$

To verify the workings of the DC link voltage enhancement, an experiment is performed to measure the sum capacitor voltage v_cu^Σ and upper arm voltage v_u similar to Figure 4.1. The result of the experiment is provided in Figure 7.4 and Figure 7.5.

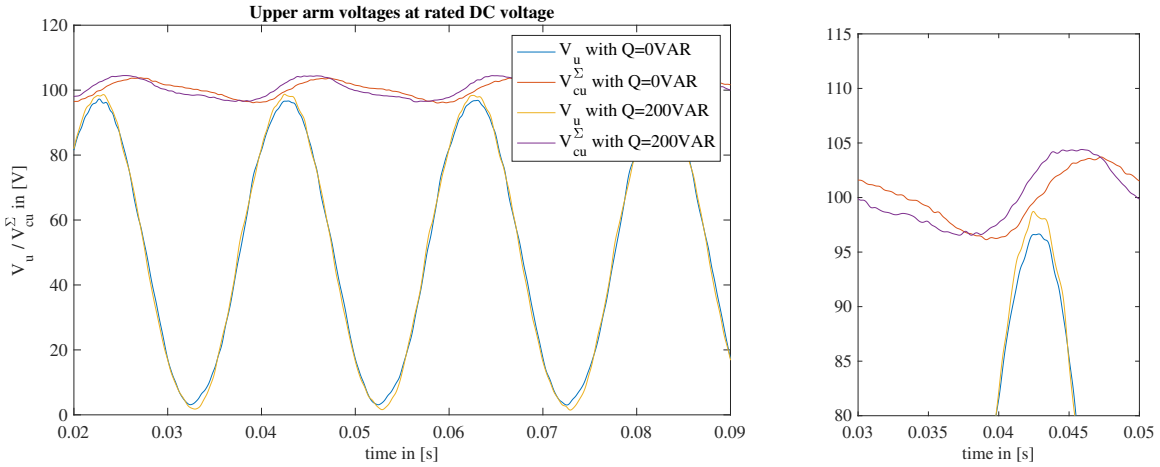


Figure 7.4: MMC arm voltage measurements when operated at the rated DC link voltage of 100V.

Figure 7.4 shows the arm voltages of the Imperix MMC when operated at the rated DC link voltage $V_d = V_{dr}$[1]. The measurements are performed for two values of reactive power $Q = 0VAR$ and $Q = 200VAR$ which, for the given setup, correspond to power factors $pf = 1.0$ and $pf = 0.86$, respectively.

When analysing Figure 7.4, multiple observations can be defined. At first, it is observed that the sum capacitor voltage v_{cu}^{Σ} of $Q = 200VAR$ is larger than $Q = 0VAR$ at the peak of v_u ($\omega_1 t = \pi$). This observation is expected as the larger ripple in the sum capacitor voltage is caused by the reactive arm current component. Second, it is noted that the spacing between v_{cu}^{Σ} and v_u increases for a larger value of Q. In Figure 7.4 the spacing voltage $V_{space} = 2.8V$ for $Q = 0VAR$ and $V_{space} = 3.3V$ for $Q = 200VAR$. This is again in line with the expectations. Though, note that the amplitude of the arm voltage v_u also increases with Q. This increase in the amplitude of v_u counteracts the impact of the ripple increase in v_{cu}^{Σ}. Overall, limiting the rise of the spacing voltage. This phenomenon was also observed during the simulations in Section 4.3, where mentioned that the grid injection of reactive power demanded a higher output voltage v_s. So $\hat{V}_s$ and thus the amplitude of v_u, increase with Q.

Figure 7.5 shows the arm voltages of the Imperix MMC when operated at an enhanced DC link voltage $V_d = 107V$[1]. The measurements are again performed for $Q = 0VAR$ and $Q = 200VAR$. By comparing Figure 7.4 with Figure 7.5, a set of observations can be defined. At first, it is observed that for both values of Q, the upper arm voltage v_u is biased while maintaining the same average sum capacitor voltage. This is an important process aspect, as the DC link voltage enhancement must be achieved while keeping the MMC energies within the rated limits. Second, it is observed that the spacing voltage in Figure 7.4 is zero $V_{space} = 0V$ for $Q = 0VAR$. Meanwhile, a positive spacing voltage of $V_{space} = 1.1V$ remains for $Q = 200VAR$, which shows that a further enhancement is feasible. This experiment thus indicates that for larger values of Q, a greater DC link voltage enhancement is possible when compiling constraint (4.1). This while maintaining the average sum capacitor voltage at V_{dr}.

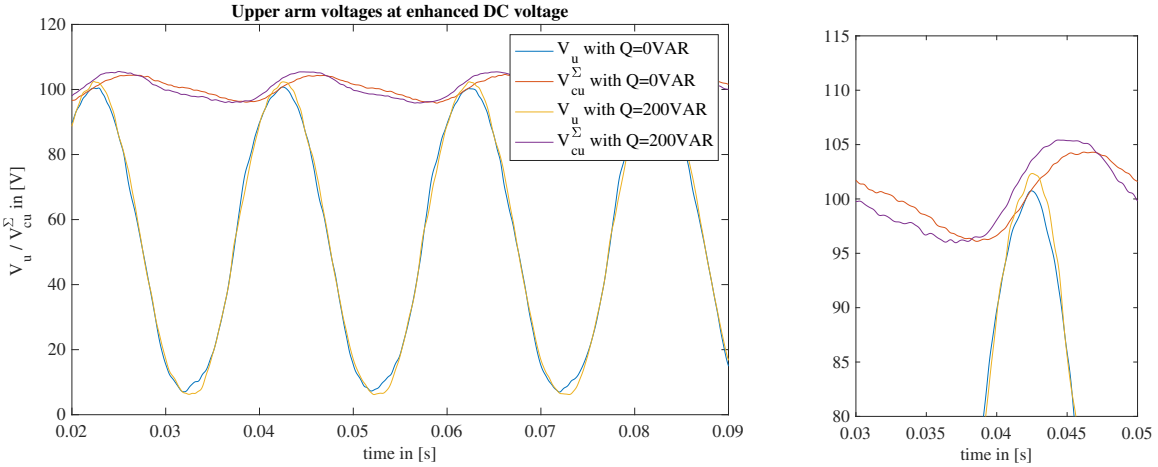


Figure 7.5: MMC arm voltage measurements when operated at an enhanced DC link voltage of 107V.

7.3 Steady state performance

Now that the workings of the DC link voltage enhancement has been demonstrated experimentally, the next step is to verify the enhancement boundary. Equation (4.19) gave the analytical expression of the DC link voltage enhancement limit $k_{d,max}$. As this equation is used by the dynamic DC link voltage control, it is important to analyse the expression's validity to ensure the controller's performance. Therefore, the

[1]The sum capacitor voltage v_{cu}^{Σ} and upper arm voltage v_u are sampled at 625kHz and filtered using a low-pass FIR-filter with a filter-order of 600 and a cutoff frequency of 1kHz. Unfiltered plots of the oscilloscope are provided in Appendix E.

second experiment measures the DC link voltage enhancement limit during steady-state operation and compares the result to the analytical boundary.

7.3.1 Harmonic distortion

The first attempt towards measuring the DC link voltage enhancement limit is via harmonic distortion. In this experiment the upper arm voltage v_u is measured for multiple values of the enhancement factor k_d. Afterwards, the Total Harmonic Distortion (THD) is calculated over 10 fundamental periods $T_1 = 1/f_1$ using the harmonic components up to the 50th order [41]. This experiment is then repeated for multiple values of the reactive power Q, each creating a k_d vs THD_v curve. In the ideal situation, these curves would have a hockey-stick shape, maintaining a small constant THD_v for $k_d < k_{d,max}$ and increasing linearly for $k_d > k_{d,max}$.

The results of the measurements are provided in Figure 7.6. This figure shows the measured THD_v as a function of the enhancement factor. The k_d vs THD_v curves are plotted for three values of reactive power $Q = 0VAR$, $Q = 75VAR$ and $Q = 150VAR$. For the given setup these correspond to power factors $pf = 1.0$, $pf = 0.98$ and $pf = 0.91$, respectively. In addition to the measured curves, Figure 7.6 contains linear approximations to emulate the hockey-stick shape.

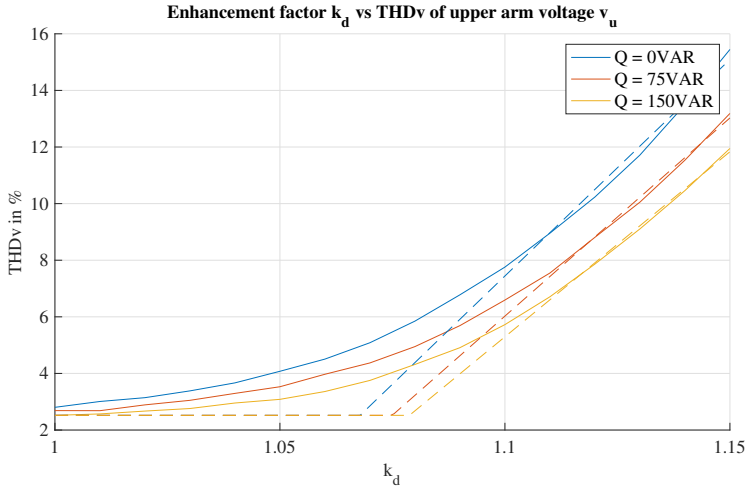


Figure 7.6: Measured THDv of the upper arm voltage as a function of the enhancement factor.

When analysing Figure 7.6, multiple observations can be made. At first, it is observed that, the THD_v is around 2.6% when operated at the rated DC link voltage ($k_d = 1$) for all three values of Q. Then for larger DC link voltages, the harmonic distortion increases faster for smaller values of Q: $THD_v(0) > THD_v(75) > THD_v(150)$. This phenomenon is in line with the expectations as no saturation should appear in the arm voltage v_u at the rated DC link voltage. Making a constant THD_v for $k_d = 1$. Then, when increasing k_d, the arm voltage becomes restricted by v_{cu}^{Σ}, effectively causing the sinusoid to clip. A larger value of Q should increase the spacing between v_{cu}^{Σ} and v_u and thus delay the saturation point in terms of k_d. This observation again demonstrates the workings of the DC link voltage enhancement, as operating at a lower power factor allows for a larger DC link voltage enhancement when fixing the harmonic performance.

Using the linear approximations in Figure 7.6, a second observation can be made. As mentioned in the ideal situation, the corner point of the THD_v curves gives the analytical enhancement boundary $k_{d,max}$. Therefore, the corner point of the linear approximation provides an empirical estimate of the enhancement limit. The resulting estimates of Figure 7.6 are provided in Table 7.2 together with the analytical enhancement boundary $k_{d,max}$ for the corresponding values of Q. Although the two limits exhibit the same trend, Table 7.2 shows a large discrepancy between the empirical and analytical boundaries. A

similar discrepancy was observed during the simulations in Section 4.3. The discrepancy is mainly caused by the analytical assumption stated in Section 4.1: that the output voltage amplitude $\hat{V}_s$ is fixed at $V_{dr}/2$. Following Table 7.1, the rated DC link voltage V_{dr} is set at 100V and the grid voltage amplitude $\hat{V}_g$ is fixed at 47.7V. As in the experiment, $V_{dr} > 2\hat{V}_g$ there is a 5% voltage spacing in which output voltage amplitude $\hat{V}_s$ can exceed the grid voltage amplitude $\hat{V}_g$. This spacing is required for the injection of active and reactive power into the grid. Therefore, during the measurements, the amplitude $\hat{V}_s$ is not constant at $V_{dr}/2$ but varies with both Q and P.

Table 7.2: Empirical and analytical DC link voltage enhancement limit for harmonic distortion method.

Reactive power:	**Empirical limit:**	**Analytical limit:**
$Q = 0VAR$	$k_{d,corner} = 1.067$	$k_{d,\,max} = 1.000$
$Q = 75VAR$	$k_{d,corner} = 1.075$	$k_{d,\,max} = 1.016$
$Q = 150VAR$	$k_{d,corner} = 1.079$	$k_{d,\,max} = 1.033$

This behaviour is observed during the experiment. Figure 7.7 shows the measured output voltage amplitude as a function of enhancement factor for multiple values of Q. It can be seen that for larger values of injected reactive power, the output voltage amplitude increases. In addition, for larger values of k_d, and thus smaller values of P, the output voltage amplitude decreases[1]. So in this experiment the output voltage amplitude increases with both Q and P.

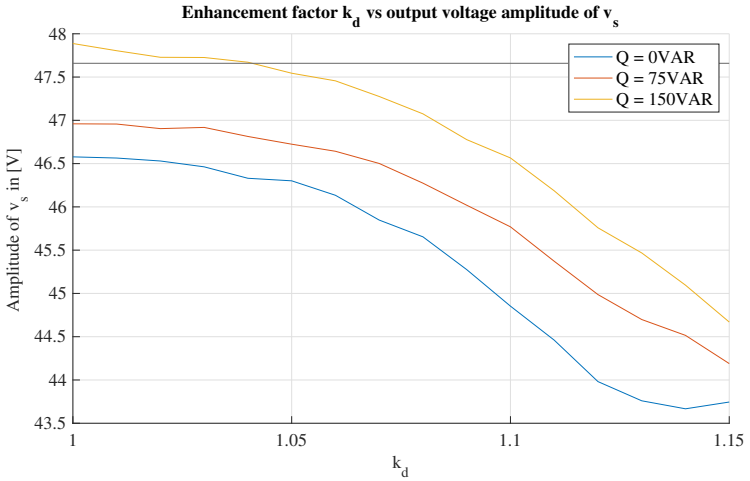


Figure 7.7: Measured output voltage amplitude as a function of the enhancement factor.

This conclusion explains the large discrepancies in Table 7.2. As the empirical estimate $k_{d,corner}$ includes both the enhancement caused by the injection of Q and the enhancement that is created when giving up the voltage spacing between $2\hat{V}_s$ and V_{dr}. Note that the initial 5% voltage spacing is need for the injection P and Q but the voltage spacing also varies with P and Q. Thus imposing a varying enhancement component that significantly influences the empirical estimate of $k_{d,max}$. This dependency compromises the accuracy of $k_{d,corner}$ in estimating $k_{d,max}$.

7.3.2 Enhancement voltage

An alternative attempt towards measuring the DC link voltage enhancement limit is via the enhancement voltage. In this experiment the upper arm voltage v_u, lower arm voltage v_l and sum capacitor voltage v_{cu}^{Σ} are measured for multiple values of the enhancement factor k_d. In contrast to the last method, this

[1] As the load resistance R_{load} is fixed during the measurement, the grid absorbed power "$-P$" increases with k_d. So the converter supplied power P decreases with k_d.

method accounts for the voltage spacing between V_{dr} and $2\hat{V}_s$ and its dependency on P and Q. To provide a description of the measurement method, first a framework has to be defined. Recall the definition of the spacing voltage V_{space} as the minimal distance between the sum capacitor voltage v_{cu}^{Σ} and the arm voltage v_u that is encountered over a fundamental period T_1 as expressed in Equation (7.1). Besides, consider the definition of the safely voltage V_{safety} as the distance between half the average sum capacitor voltage $\overline{v_{cu}^{\Sigma}}$ and the output voltage amplitude $\hat{V}_s$. Note that v_{cu}^{Σ} indicates the available voltage for creating v_u. As v_u is a sinusoid with amplitude $\hat{V}_s$, the output voltage amplitude must be below half of v_{cu}^{Σ}. The remaining spacing is then considered a safety region that accounts for ripples during transients or when more active/reactive power is required to be injected into the grid. V_{safety} is defined as in Equation (7.2).

$$V_{safety} = \frac{\overline{v_{cu}^{\Sigma}(t)}}{2} - \hat{V}_s \tag{7.2}$$

As mentioned in the introduction of this section, the DC link voltage enhancement must be achieved while maintaining the same average energy stored in the MMCs. The average sum capacitor voltage $\overline{v_{cu}^{\Sigma}}$ is therefore controlled to the rated DC link voltage V_{dr}. Now using the statement of Section 7.3.1, it can be seen that the spacing voltage includes two components. The first component is the minimal voltage spacing between $V_{dr}/2$ and $\hat{V}_s$, defined as the safely voltage V_{safety}. The second component is the voltage spacing created by the injection of Q, defined as the enhancement voltage V_{enh}. Both of which previously contributed to the empirical estimate $k_{d,corner}$. This concludes the second definition of V_{space} as in Equation (7.3).

$$V_{space} = V_{safety} + V_{enh} \tag{7.3}$$

Now, the proposed measurement method is based on Equation (7.3), which states that the enhancement voltage can be measured by subtracting the safely voltage from the spacing voltage. This enhancement voltage is of interest for estimating the analytical enhancement boundary. The measurement method based on the enhancement voltage, creates an estimate which includes the enhancement caused by the injection of Q but is independent of the variations in $\hat{V}_s$. The empirical enhancement factor can thus more accurately estimate $k_{d,max}$.

The result of the measurements are provided in Figure 7.8[1]. This figure shows the measured enhancement voltage V_{enh} as a function of the enhancement factor. The k_d vs V_{enh} curves are measured for five values of $Q = \{0, 75, 110, 150, 200\} VAR$ while maintaining the same active power $P = 333W$. The active power is kept constant by increasing the load resistance R_{load} with the enhancement factor k_d. This is done to make V_{safety} independent of k_d an solely a function of Q. As in the ideal situation the k_d vs V_{enh} curves are linear, a linear interpolation is fitted to the data points.

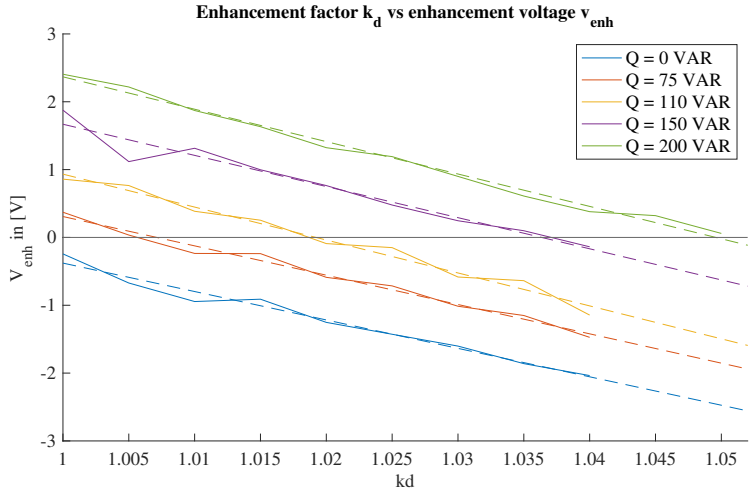


Figure 7.8: Measured enhancement voltage as a function of the enhancement factor.

From Figure 7.8 can be concluded that the enhancement voltage decreases with an increase in the enhancement factor. When V_{enh} becomes zero, any further increase of k_d sacrifices the safety voltage. Therefore, the intersection of the k_d vs V_{enh} curve with zero gives an empirical enhancement factor $k_{d,emp}$ that estimates $k_{d,max}$. The resulting values of $k_{d,emp}$ are plotted as a function of Q together with the analytical enhancement boundary. The result is provided in Figure 7.9.

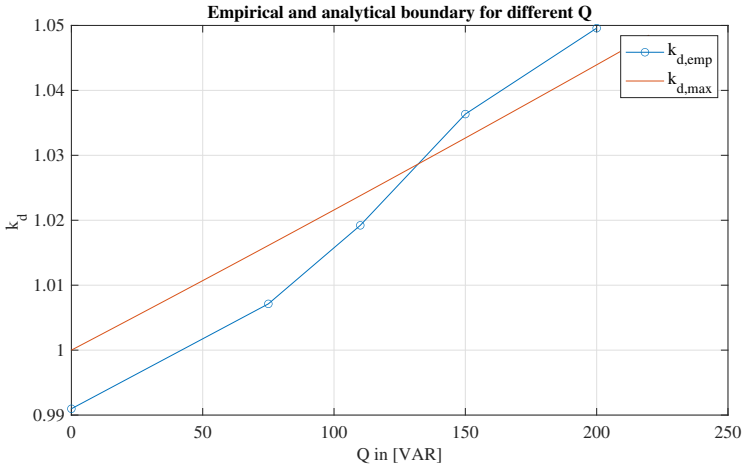


Figure 7.9: Empirical and analytical DC link voltage enhancement boundary for enhancement spacing method.

From Figure 7.9 can be concluded that both the empirical enhancement boundary and analytical enhancement boundary increases with the reactive energy Q. Although the curves follow the same trend, it is observed that for lower values of Q the analytical enhancement boundary overestimates the measured enhancement boundary. The opposite is seen for larger values of Q. The first observation can possibly be explained by considering the time-point assumption, discussed in Appendix C.2. During the analytical derivation of $k_{d,max}$, the assumption was made that the spacing between v_{cu}^{Σ} and v_u was most stringent near $\omega_1 t = \pi$. However, this assumption does not always hold for high power factors, as was illustrated in Figure 4.5. For $Q = 0$, the stringent time point is positioned to the right of the peak of v_u. This shows that operating at $k_d = 0$ with $Q = 0$ violates constraint (4.1). The measured enhancement boundary can thus be smaller than the analytical enhancement boundary for lower values of Q. A possible cause for the boundary deviations at larger values of Q is a measurements error like a small sensor offset for measuring V_d. Although a slight discrepancy is encountered, the analytical enhancement boundary preserves the trend of the empirical enhancement boundary with sufficient accuracy.

7.4 Transient performance

Having analysed the accuracy of the enhancement boundary in steady-state, the next step is to look at the transient performance of the MMC when it runs an enhanced operation. As was concluded in Section 7.3.2, the analytical boundary provides a sufficiently accurate enhancement factor limit for larger values of Q. So when using Equation (5.1) as the controller enhancement function, the enhanced operating steady-state does not violate constraint (4.1). However, as was denoted in Chapter 5, the dynamic behaviour between steady-states becomes crucial when running in an enhanced operation. Therefore the third experiment measures the transient performance of the dynamic DC link voltage control, to verify its workings between steady-states.

To measure the transient performance of the dynamic DC link voltage control, the upper arm voltage v_u, sum capacitor voltage v_{cu}^{Σ} and DC link voltage V_d are measured as a function of time. The dynamic

[1]The sum capacitor voltage v_{cu}^{Σ}, upper arm voltage v_u and lower arm voltage v_l are sampled at 625kHz and filtered using a low-pass FIR-filter with a filter-order of 600 and a cutoff frequency of 1kHz

DC link voltage control is implemented using the open-loop control strategy that is proposed in Section 5.3 and tuned in Section 6.3. This method is compared with the direct control method, explained in Section 5.1. During the measurements the reactive power reference Q_{ref} is reduced from 200VAR to 0VAR at time point $t = \text{t1}$. Using the controller enhancement function of Equation (5.1), this bring the enhancement factor down from $k_{\text{d}} = 1.042$ to $k_{\text{d}} = 1.000$. Figure 7.10 provides the results of the two measurements [1]. This figure contains the upper arm voltage, sum capacitor voltage and DC link voltage for the direct and open-loop control measurements. In addition, Figure 7.10 provides the spacing voltage V_{space} for the constraining time points.

For the direct control, both the output reactive power reference Q^* and the enhancement factor reference k_{d}^* decrease upon the change in Q_{ref} (at time point t = t1). As a result, the measured DC link voltage in Figure 7.10 directly reduces with the change of Q_{ref}. The simultaneous reduction of k_{d}^* and Q^* makes the spacing voltage V_{space} reduces from 2.11V to 0.27V at time point t = t1. Note that this would cause a violation of constraint (4.1) if the initial safety voltage were to be smaller than 5% or the change in Q_{ref} to be large than 200VAR. Therefore, the direct control method could cause significant output harmonics during system transients.

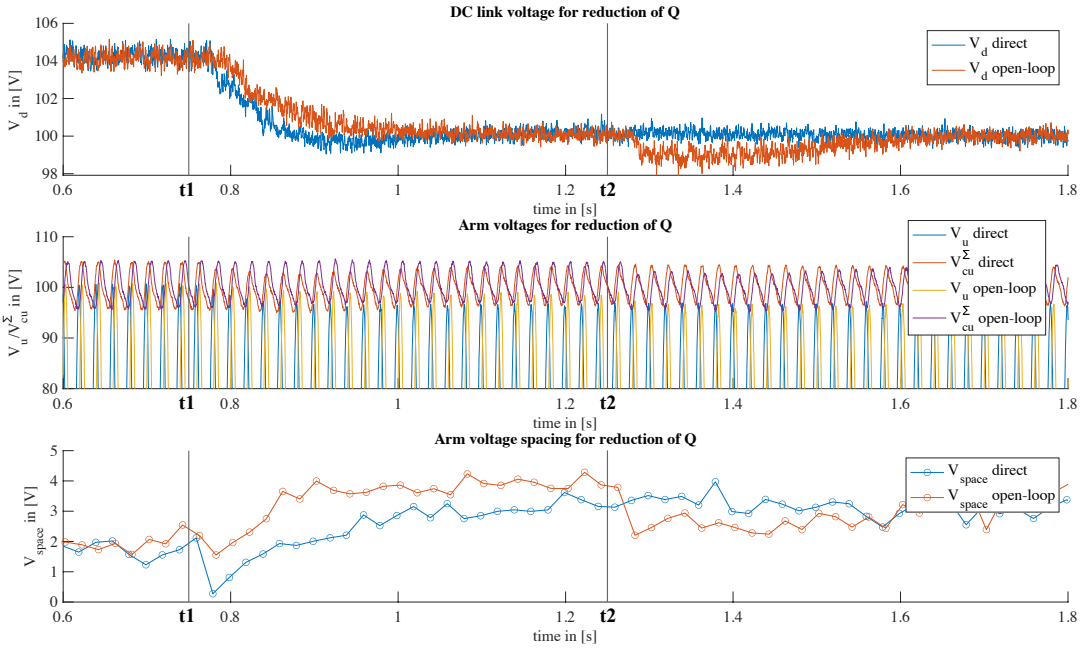


Figure 7.10: Voltage spacing for a reduction in the reactive power, with and without open-loop DC link voltage control.

For the open-loop control method, the output reactive power reference Q^* and the enhancement factor reference k_{d}^* decrease in stages upon the change in Q_{ref}. Following Section 5.3, k_{d}^* decreases from 1.042 to 1.000 upon the change of Q_{ref} (at time point t1). Then 0.5s later (at time point t2), when V_{d} has settled, the output reactive power reference Q^* is reduced to 0VAR. In Figure 7.10 it is observed that V_{d} directly reduces with the change of Q_{ref} while the spacing voltage V_{space} reduces from 2.19V to 1.55V. This drop in the spacing voltage is significantly less than the one observer during direct control. So, by using the open-loop control strategy, the MMC is able to maintain its safety voltage during system transient and thus prevent additional harmonic distortion. It can thus be concluded that the dynamic DC link voltage control, implemented with the open-loop control strategy, can accomplish a DC link voltage enhancement during steady-state and cope with the associated transient conditions.

[1] The sum capacitor voltage v_{cu}^{Σ} and upper arm voltage v_{u} are sampled at 62.5kHz and filtered using a low-pass FIR-filter with a filter-order of 50 and a cutoff frequency of 1kHz

Chapter 8

Third Harmonic Injection Improvement

The DC link voltage enhancement for an MMC-based distribution link was explored in Section 4.1, which resulted in the enhancement boundary provided in Equation (4.19). During this analysis, various assumptions were made, among which Equation (4.3). This equation implies that the generated output voltage v_s is a fundamental frequency sinusoid. However, this assumption does not apply to specific cases. As was introduced in Section 2.3.2, a third-order harmonic component can be added to the fundamental frequency reference signals of the three-phase legs. This concept is based on the fact that, under symmetric conditions, any odd-multiple third-order harmonic becomes a zero-sequence component [11]. In many three-phase grid applications the midpoint of the AC-side is not connected, which removes the impact of the zero-sequence component on the source/load. This as the third-order harmonic components cancel out in the line-to-line voltage. The process of adding a third-order harmonic component to the reference signal is called Third Harmonic Injection (THI), which is done to extend the converter's linear modulation range or improve its harmonic performance.

THI provides various benefits for the operation of the modular multilevel converter. Some of these benefits, discussed in [42], are as follows: lower power losses, reduced SM capacitance requirements, improved circulating currents and smaller DC fault currents. As an alternative to the know benefits, this chapter proposes the idea of using THI to improve the DC link voltage enhancement. First, in Section 8.1, the concept of THI is explained for the MMC model, and the impact on the DC link voltage enhancement boundary is investigated. Second, Section 8.2 verifies the impact of THI on the DC link voltage enhancement using measurements on the experimental setup.

8.1 THI concept

With the concept of THI, the three-phase output voltages are changed by adding a third-order harmonic component to the fundamental frequency references. As defined in [19], the optimal amplitude of the third harmonic component is 1/6 of the fundamental amplitude $\hat{V}_s$, which extends the linear modulation range by 15.5%. Rather than using this extended modulation range to increases $\hat{V}_s$, it is used for biasing v_u and thus increase V_d. As a result the output voltage reference of Equation (4.3) is altered to Equation (8.1).

$$v_s = \hat{V}_s \cdot \cos(\omega_1 t) - \frac{1}{6}\hat{V}_s \cdot \cos(3\omega_1 t) \tag{8.1}$$

Recall that the upper arm voltage caries both half of the DC link voltage and the sinusoidal output voltage. Therefore the change in the output voltage impacts v_u. The output voltage is redefined as in Equation (8.2).

$$v_u = \frac{1}{2}V_d - v_s = \frac{1}{2}V_d - \hat{V}_s \cdot \cos(\omega_1 t) + \frac{1}{6}\hat{V}_s \cdot \cos(3\omega_1 t) \tag{8.2}$$

Note that the added third harmonic component also affect the sum capacitor voltage v_{cu}^{Σ}. Equation (4.11) gave the simplified expression of the sum capacitor voltage as a function of the energy ripples. This equation is again provided in Equation (8.3).

$$v_{\mathrm{cu}}^{\Sigma} \approx V_{\mathrm{d}} + \frac{N}{2CV_{\mathrm{d}}}(\Delta W_{\Sigma} + \Delta W_{\Delta}) \tag{8.3}$$

From this equation follows that the sum capacitor voltage ripple depends on the total energy ripple ΔW_{Σ} and imbalance energy ripple ΔW_{Δ}. In turn, using Equation (4.2), it is observed that the energy ripples depend upon the output voltage v_{s}. Then using the assumptions of Equation (4.3) with the altered output voltage of Equation (8.1) and performing a time integration, provides the energy equations. The total energy W_{Σ} and imbalance energy W_{Δ} are defined in Equations (8.4) and (8.5), respectively.

$$W_{\Sigma} = W_{\Sigma 0} - \frac{\hat{V}_{\mathrm{s}}\hat{I}_{\mathrm{s}}}{4\omega_1}\sin(2\omega_1 t - \phi) + \frac{\hat{V}_{\mathrm{s}}\hat{I}_{\mathrm{s}}}{24\omega_1}\sin(2\omega_1 t + \phi) + \frac{\hat{V}_{\mathrm{s}}\hat{I}_{\mathrm{s}}}{48\omega_1}\sin(4\omega_1 t - \phi) = W_{\Sigma 0} + \Delta W_{\Sigma} \tag{8.4}$$

$$W_{\Delta} = W_{\Delta 0} + \frac{V_{\mathrm{d}}\hat{I}_{\mathrm{s}}}{2\omega_1}\sin(\omega_1 t - \phi) - \frac{2\hat{V}_{\mathrm{s}}i_{\mathrm{c}}}{\omega_1}\sin(\omega_1 t) + \frac{\hat{V}_{\mathrm{s}}i_{\mathrm{c}}}{9\omega_1}\sin(3\omega_1 t) = W_{\Sigma 0} + \Delta W_{\Delta} \tag{8.5}$$

Equations (8.4) and (8.5) are the altered versions of Equations (4.6) and (4.7), that include the impact of THI on the energy ripples. By combining Equation (8.3) with (8.4) and (8.5), the sum capacitor voltage expression is obtained for a THI output voltage.

To visualise the impact of THI on the enhancement process, Figure 8.1 can be used. This figure shows the upper arm voltage v_{u} and sum capacitor voltage v_{cu}^{Σ} with and without the injection of the third harmonic component. The arm voltages are plotted with no enhancement ($k_{\mathrm{d}} = 1$) and apply to the Imperix MMC with $X_{\mathrm{c}} = 2.55\Omega$ and $V_{\mathrm{dr}} = 100V$.

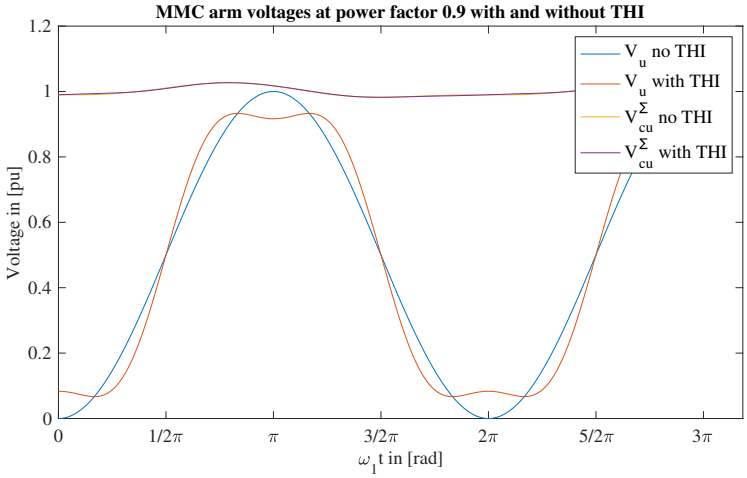


Figure 8.1: The sum capacitor voltage and upper arm voltage with and without THI.

In Figure 8.1 can be observed that the amplitude of upper arm voltage with THI is significantly smaller than the standard arm voltage amplitude. Meanwhile, the sum capacitor voltage with and without THI are reasonably similar. Therefore, the smaller value of $\hat{V}_{\mathrm{s}}$ develops a larger spacing between v_{cu}^{Σ} and v_{u} increasing the spacing voltage V_{space}. If the safety voltage V_{safety} is defined as a property of Q, then the enhancement voltage V_{enh} significantly increases with the injection of the third harmonic component. The increased enhancement voltage allows for a larger DC link voltage enhancement without violating the constrains. So the third harmonic injection progresses the DC link voltage enhancement.

To analyse the impact of THI on the enhancement boundary, an optimisation is performed. This optimisation is performed to maximise the enhancement factor k_{d} while compiling to constraint (4.1). Note that the equations of v_{u} and v_{cu}^{Σ} are known but highly nonlinear. As a result, the problem can be posed as an unconstrained nonlinear optimisation problem of the form:

$$min_{k_d \in \mathbb{R}} \left(|min_{t \in [0,T_1]} \{ v_{cu}^{\Sigma}(t) - v_u(t) \}| \right)$$

This problem is solved using the Levenberg-Marquardt algorithm for multiple values of the power factor [43]. The result of the optimisation is provided in Figure 8.2. This figure contains the DC link voltage enhancement boundary for the Imperix MMC when applying THI. For comparison also the analytical enhancement boundary $k_{d,max}$ is plotted. This figure shows that at unity power factor, the enhancement limit with THI is 1.108 while $k_{d,max} = 1.00$. Furthermore, when operating at smaller power factors, the enhancement limit whit THI is larger than the analytical enhancement limit. It is thus concluded that THI improves the DC link voltage enhancement for the Imperix MMC.

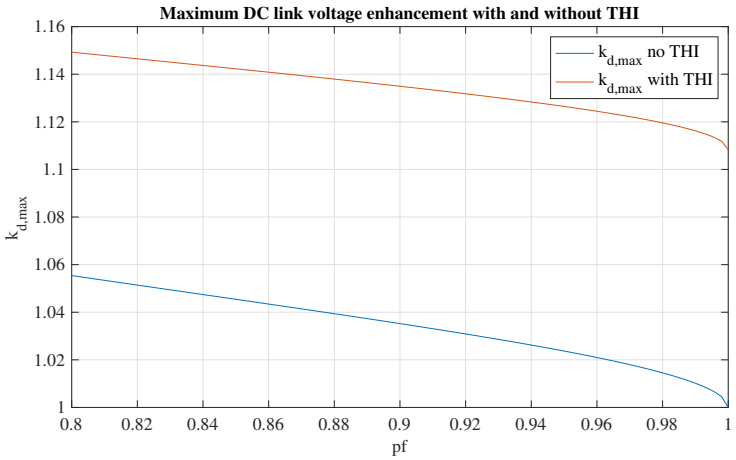


Figure 8.2: Impact of THI on output DC link voltage enhancement boundary for the Imperix MMC.

8.2 THI experimental results

After establishing the concept of THI for the MMC-based distribution link, the next step is to verify the DC link voltage enhancement extension by using measurements. The experiment is analogous to the one performed in Section 7.2. Similar to figure 7.5 the arm voltages v_{cu}^{Σ} and v_u of the Imperix MMC are measured when operated at an enhanced DC link voltage $V_d = 107V$. The measurement is performed with and without THI at a reactive power $Q = 100VAR$. The results of the measurements are provided in Figure 8.3.

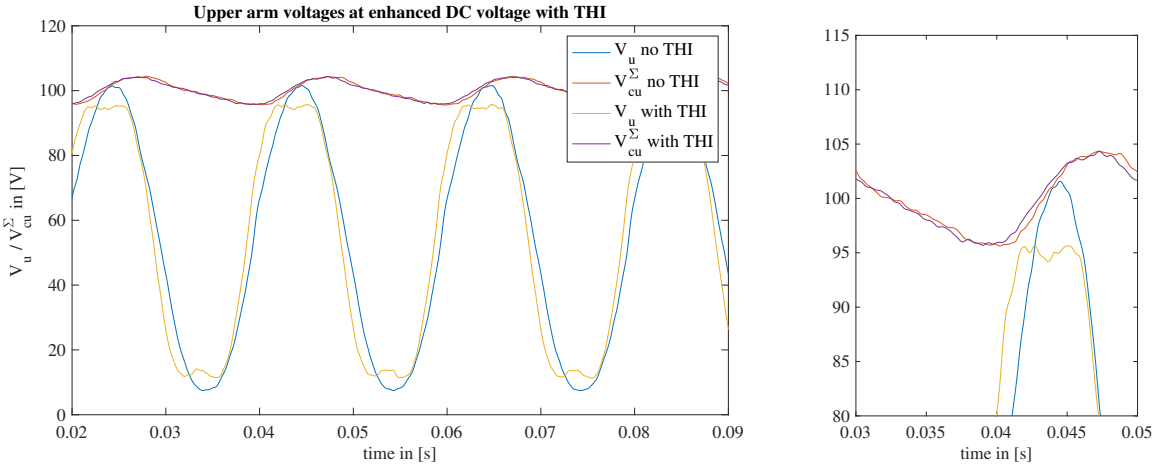


Figure 8.3: MMC arm voltage measurements with and without THI when operated at the enhanced DC link voltage of 107V.

Using Figure 8.3, a set of observations can be defined[1]. At first, it is observed that the sum capacitor voltage curves for the case with and without THI are very similar. This is in line with the expectations implied by Figure 8.1. Second, it is observed that the minimal spacing between v_{cu}^{Σ} and v_{u} is 0V for the operation without THI. Meanwhile, a positive spacing voltage of 2.4V remains for the operation with an injected third harmonic component. This indicates that the standard operation has reached its DC voltage enhancement limit. Whereas the injection of the third harmonic component makes a further enhancement possible. So from this experiment can be concluded that the application of THI in MMC can extend the DC link voltage enhancement.

[1]The sum capacitor voltage v_{cu}^{Σ} and upper arm voltage v_{u} are sampled at 625kHz and filtered using a low-pass FIR-filter with a filter-order of 600 and a cutoff frequency of 1kHz

Chapter 9

Conclusion and Future Work

This master thesis project explores the possibility of operating an MMC-based MVDC distribution link at a DC voltage higher than the nominal value. This is achieved while preserving the average energy stored in the MMC and maintaining the AC-side harmonic performance. The DC link voltage enhancement is performed to improve the power transfer capacity of an MVDC link, which can help to avoid grid congestions. Alternatively, the voltage enhancement can improve the efficiency of the DC link system for a given operating power. Throughout the report, a control strategy is developed and experimentally verified, which is used to achieve the transfer capacity enhancement for a dynamic operation of the MMC-based MVDC distribution link. To conclude the analysis, the four sub-research questions and main research question of Section 1.1 are used as references.

1. Which control strategy qualifies for the static operation of back-to-back configured MMCs?

To analyse the concept of the DC link voltage enhancement, first of all, a control strategy was derived that regulates the modular multilevel converter when it is back-to-back configured in an MVDC distribution link. Because of the MMC's complex internal dynamics and inherent instabilities, the control strategy becomes a fundamental part of the operation of the converter. It is concluded that the control strategy which qualifies for the static operation of the MMCs is composed of five sub-control modules: voltage controller, output current controller, circulating current controller, arm-leg energy balancing controller and a higher-level controller. The sub-control modules each regulate one or multiple circuit quantities using a closed-loop PI or closed-loop PR control strategy. These controllers have appropriate closed-loop bandwidths to prevent module interactions. This all to achieve the intended operating point of the MMC when situated in a distribution link.

2. What is the analytical limitation to the DC link voltage enhancement?

The DC link voltage enhancement was then examined analytically using the model equations of the MMC. It was concluded that the voltage enhancement is limited by the saturation of the arm voltage at the corresponding sum capacitor voltage. With this conclusion, the enhancement limitation could be posed as a mathematical optimisation problem which was solved using a set of assumptions. This concluded the enhancement boundary expression $k_{d,max}$ which posed the analytical limitation to the DC link voltage enhancement. As a result of this equation, a dependency was discovered between the enhancement factor limit and the reactive power injected into the AC grid. This showed that a greater DC link voltage enhancement was attainable with a larger injection of Q. For the considered 11MW MVDC link, a 9.1% DC link voltage enhancement was found when operating at a power factor of 0.95. Further interpretation of the enhancement limit introduced the reactive voltage, which related the MMC characteristics via the arm impedance X_c to the enhancement boundary. Finally, during the ALA simulations, the limitations of the enhancement boundary were discovered, which restricted the application power factor range of the equation to $pf \in [0.9, 1.0]$.

3. How can the MMC control strategy be adapted to incorporate the DC link voltage enhancement during dynamic operation?

With the enhancement boundary expression, the DC link voltage of an MVDC distribution link can be enhanced while preserving the AC-side harmonic performance. Though, this acquired limit is applicable to the steady-state operation of the MMC and does not concern system transient. First, the dynamic DC link behaviour was investigated using the original control strategy: direct DC link voltage control. It was concluded that by directly applying the controller enhancement function, derived from $k_{d,max}$, high-frequency components appeared in the arm voltages during transients. So the direct DC link voltage control compromises the AC-side harmonic performance to achieve the DC link enhancement. As a result of this observation, a set of requirements was defined to ensure a reliable operation of the dynamic controller. Following these requirements, it was concluded that the control strategy which qualifies to incorporate the DC link voltage enhancement for dynamic operation, is the open-loop DC link voltage control. This controller dynamically enhances the DC link voltage by solely using the reactive power reference as an input. The controller is implemented with a discrete control strategy by which the control logic is realised using a finite state machine. From the simulation can be concluded that the open-loop controller successfully limits the grid injection of harmonic elements during system transients and thus suffices as a correct implementation of the dynamic DC link voltage control.

4. To what extent can the dynamic DC link voltage control enhance the DC link voltage of the MVDC distribution link?

The dynamic DC link voltage control provides the ability to dynamically enhance the DC voltage of an MVDC distribution link. To consider the enhancement performance that would be obtained in a practical situation, the control strategy was implemented on the lab-scale Imperix MMC. The implemented control structure is based on the initially proposed control strategy, though it is altered to account for practical circumstances and uncertainties. This involved the addition of an Imperix modulator, a fault trigger module and a submodule balancing controller. Besides, the output current control, energy balancing control and higher level control are implemented using a closed-loop PI or PR control strategy. It was concluded that these controllers were optimally tuned using the MO tuning method, which improved the tracking performance. After experimental verification of the workings of the Imperix controller, measurements were performed to verify the DC link voltage enhancement. These experiments were performed to demonstrate the working concept, verify the analytical enhancement boundary and show the performance of the dynamic DC link voltage control. The first experiment concluded that the DC link voltage enhancement concept does occur in the Imperix MMC. The second experiment extended this statement by concluding that the empirical enhancement boundary approximates the analytical enhancement boundary with sufficient accuracy. This indicated the correctness of the $k_{d,max}$ expression. For the considered 600W MMC a 3.6% DC link voltage measured was when operating at a reactive power of 150VAR. Finally, the third experiment concluded that the dynamic DC link voltage control, implemented with the open-loop control strategy, can enhance DC link voltage during steady-state situations and cope with the associated transient conditions. These combined give experimental proof of the DC link voltage enhancement that is achieved when operating an MVDC distribution link under dynamic DC link voltage control.

To what extent can the power transfer capacity of an MVDC distribution link be enhanced by using dynamic DC link voltage control for the back-to-back operation of modular multilevel converters?

In line with the previous results, it can be concluded that the power transfer capacity of an MMC-based MVDC distribution link is enhanced by applying open-loop dynamic DC link voltage control. The enhancement is achieved while preserving the average stored energy in the MMC and maintaining the AC-side harmonic performance. When the DC current of the distribution link is fixed at the rated value, the power transfer capacity of the link increases linearly with the enhancement factor. This makes, for steady-state applications, the boundary $k_{d,max}$ the effective limit of power transfer capacity enhancement. In practice, the power transfer capacity enhancement is given by the controller enhancement function of the open-loop controller. This function is a conservative version of $k_{d,max}$ to ensure the steady-state

performance. For system transients, the dynamic DC link voltage controller contains smart control logic, which avoids the injection of harmonic elements into the grid. So combined this concludes that the open-loop dynamic DC link voltage control achieves a proper DC link voltage enhancement that meets the requirements for both steady state and dynamic conditions.

Further studies analysed the possibility of using THI to benefit the DC link voltage enhancement. It was proposed that by injecting a third harmonic component in the output voltage reference, the DC link voltage enhancement limit could be extended. During the analytical analysis, an enhancement factor gain of 10.8% was found for the Imperix MMC when operating at unity power factor. Besides, for smaller operational power factors the enhancement limit with THI was concluded to be larger than the analytical enhancement limit. This concept was then verified with an experiment. This concludes that the application of THI in a MMC can indeed improve the DC link voltage enhancement.

9.1 Future work

For the DC link capacity enhancement concept, several improvements can be made to enhance the accuracy of boundary expression or to widen the concept's applicability. Future research aimed at improving the DC link enhancement concept can be focused on the following topics:

- During the analytical analysis of Chapter 4, the assumption was made that the output voltage amplitude was fixed at half the rated DC link voltage. However, during simulations and experiments, it was observed that $\hat{V}_\mathrm{s}$ depends on the AC-side active and reactive power. The first improvement is, therefore, concerned with analysing the dependency between $\hat{V}_\mathrm{s}$ and P/Q. This dependency between $\hat{V}_\mathrm{s}$ and P/Q will involve the model parameters of the AC grid and the characteristics of the MMC. This relation could then be used to establish a more accurate analytical boundary expression $k_{d,max}$ that would apply to a more extensive operation power factor range.

- As already introduced in Chapter 8, third harmonic injection is an exciting concept that can significantly improve the DC link voltage enhancement. As a second improvement, a proper analytical analysis could be performed that reveals the extension of the enhancement boundary caused by THI. An essential aspect of this would involve the impact of the MMC arm impedance X_c on $k_{\mathrm{d,max}}$. During ALA simulation, it was observed that the impact of THI appeared more significantly for MMCs with a smaller X_c. This generally relates to MMCs with a low number of submodules and large submodule capacitance. Under the same conditions, these MMCs have a smaller sum of capacitor voltage ripples, which reduces the impact of Q on the enhancement voltage. Though, because of the shape of the altered arm voltage, the flatter sum capacitor voltage enables the maximum potential of the injected third harmonic component.

- The third possible improvement involves the circulating current i_c. During the analytical analysis of Chapter 4, the assumption was made that the circulating current is a constant DC component $I_\mathrm{dc}/3$. Though, as was observed in Section 6.2.4, a line frequency and double-line frequency component are intentionally added to the circulating current to achieve arm and leg energy balancing. Another example where a non-constant circulating current provides an advantage to the MMC operation, is discussed in [44]. Here the optimal shaping of the circulating currents is performed to prevent AC-side power oscillations. The third proposed improvement would be to pursue optimal circulating current shaping to benefit the DC link voltage enhancement. Were i_c could be used to alter the shape of v_cu^Σ to create a larger enhancement spacing.

- The fourth improvement proposal relates to the application of the DC link voltage enhancement. Till now, the enhancement concept has been applied to an MVDC distribution link, where two MMCs are connected back-to-back. This configuration is denoted as a symmetrical monopolar MMC-MVDC system, which has the drawback of limited redundancy. Therefore the idea is proposed to apply the DC link voltage enhancement concept to a multi-terminal MMC-based MVDC

system with a bipolar configuration. The bipolar aspect results in a more reliable and secure implementation. In addition, the multi-terminal aspect provides the opportunity to achieve an enhanced MVDC grid, with the benefits of better power distribution. The system can then be used to reconfigure an exciting MVAC architecture to an enhanced multi-terminal MVDC network.

- The final improvement proposal relates to the dynamic DC link voltage controller implementation. In Section 5.4, the open-loop dynamic DC link voltage control was derived. This controller was designed with a more stable and reliable design philosophy, favouring no constrain violation over dynamic performance. An alternative to this approach would be a closed-loop controller, where dynamic performance is defined as a higher priority. The closed-loop controller would use the reactive power reference Q_{ref}, the sum capacitor voltages v_{cu}^{Σ}, and arm voltages $v_{\text{u,l}}$ as an input to define the output enhancement factor reference k_{d}^{*}. An example of a closed-loop controller is provided in Figure 9.1. In this controller the spacing voltage V_{space} is calculated from the measured v_{cu}^{Σ} and $v_{\text{u,l}}$. This spacing voltage can be determined at three times the fundamental frequency: $3f_1$. Then a closed-loop PI control strategy is used to regulate V_{space} to the desired spacing voltage V_{space}^{*}. This reference is defined by a FSM which increases the spacing during system transients to improve stability and harmonic performance. Meanwhile, the FSM decreases the spacing voltage during steady-state conditions, maximising the DC link voltage enhancement. Note that this controller is also optimal when combined with THI, as it does not require an analytical expression for the enhancement boundary.

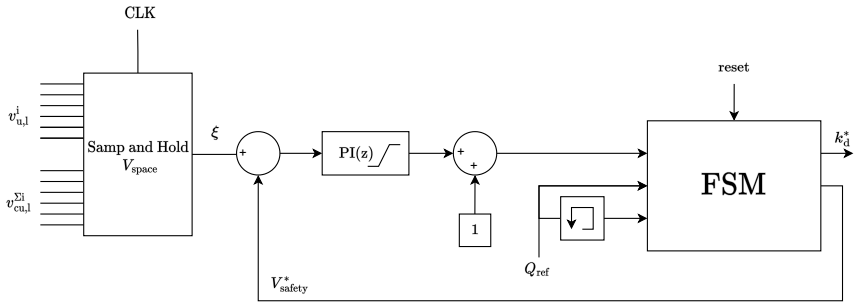


Figure 9.1: Proposed implementation of closed-loop dynamic DC link voltage control.

References

[1] European Commission, "Going climate-neutral by 2050 : a strategic long-term vision for a prosperous, modern, competitive and climate-neutral EU economy," tech. rep., Directorate-General for Climate Action, Publications Office, 2019.

[2] D. Fraile, A. Van den berghe, V. Klonari, and I. Pineda, "Getting fit for 55 and set for 2050 Electrifying Europe with wind energy AUTHORS," tech. rep., 2021.

[3] S. Coffey, V. Timmers, R. Li, G. Wu, and A. Egea-àlvarez, "Review of mvdc applications, technologies, and future prospects," 12 2021.

[4] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Modular multilevel converter for medium-voltage applications," in *2011 IEEE International Electric Machines and Drives Conference, IEMDC 2011*, pp. 1013–1018, 2011.

[5] A. Shekhar, L. Ramírez-Elizondo, Z. Qin, and P. Bauer, "Modular Multilevel Converter Performance withDynamic MVDC Distribution Link Voltage Rating," in *18TH International Conference on Power Electronics and Motion Control*, pp. 1000–1005, 2018.

[6] IEEE Power Electronics Society, "IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships," tech. rep., 2018.

[7] A. Giannakis and D. Peftitsis, "MVDC Distribution Grids and Potential Applications: Future Trends and Protection Challenges; MVDC Distribution Grids and Potential Applications: Future Trends and Protection Challenges," tech. rep., 2018.

[8] P. Schavemaker and L. van der Sluis, *Electrical Power System Essentials*, vol. 2. Delft: John Wiley & Sons, 8 2017.

[9] C. Long, J. Wu, K. Smith, A. Moon, R. Bryans, and J. Yu, "MVDC link in a 33 kV distribution network," in *CIRED - Open Access Proceedings Journal*, vol. 2017, pp. 1308–1312, Institution of Engineering and Technology, 10 2017.

[10] M. Lonkar and S. Ponnaluri, "An overview of DC microgrid operation and control," in *2015 6th International Renewable Energy Congress, IREC 2015*, Institute of Electrical and Electronics Engineers Inc., 5 2015.

[11] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*, vol. 1. Chichester: John Wiley & Sons, first edition ed., 2016.

[12] H.-J. Knaak, "Modular Multilevel Converters and HVDC/FACTS: a success story," tech. rep., 2011.

[13] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics Converters, Applications, and Design*, vol. 3. New York: John Wiley & Sons Inc, media enhanced ed., 11 2002.

[14] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular Multilevel Converters: Analysis, Control, and Applications*. Hoboken, NJ, USA: John Wiley & Sons, Inc., first edition ed., 2018.

[15] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[16] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, 2015.

[17] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, 2015.

[18] S. Ali, Z. Ling, K. Tian, and Z. Huang, "Recent Advancements in Submodule Topologies and Applications of MMC," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, pp. 3407–3435, 6 2021.

[19] F. Blaabjerg, *Control of Power Electronic Converters and Systems*, vol. 1. London: Academic Press, 1 2018.

[20] J. C. Colque, E. Ruppert, R. Z. Vargas CECS, J. L. Azcue CECS, and S. André, "Comparative analysis based on the switching frequency of modulation techniques for MMC applications; Comparative analysis based on the switching frequency of modulation techniques for MMC applications," tech. rep., 2019.

[21] A. António-Ferreira, C. Collados-Rodríguez, and O. Gomis-Bellmunt, "Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review," 2 2018.

[22] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna PowerTech - Conference Proceedings*, vol. 3, pp. 6–11, IEEE Computer Society, 2003.

[23] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450–462, 2015.

[24] A. Hassanpoor, A. Nami, and S. Norrga, "Tolerance Band Adaptation Method for Dynamic Operation of Grid-Connected Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 31, pp. 8172–8181, 12 2016.

[25] H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic averaged and simplified models for MMC-based HVDC transmission systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1723–1730, 2013.

[26] N. Ahmed, L. Angquist, S. Norrga, A. Antonopoulos, L. Harnefors, and H. P. Nee, "A computationally efficient continuous model for the modular multilevel converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, pp. 1139–1148, Institute of Electrical and Electronics Engineers Inc., 12 2014.

[27] J. Yang, J. O'reilly, and J. E. Fletcher, "An Overview of DC Cable Modelling for Fault Analysis of VSC-HVDC Transmission Systems," tech. rep., 2010.

[28] R. Murray and K. Aström, *Feedback Systems an Introduction for Scientists and Engineers*, vol. 2.11b. New Jersey: Princeton University Press, electronic edition ed., 9 2012.

[29] S. Isik, M. Alharbi, and S. Bhattacharya, "An Optimized Circulating Current Control Method Based on PR and PI Controller for MMC Applications," *IEEE Transactions on Industry Applications*, vol. 57, pp. 5074–5085, 9 2021.

[30] Y. Li, X. Shi, B. Liu, F. Wang, and W. Lei, "Maximum modulation index for modular multilevel converter with circulating current control," in *2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014*, pp. 491–498, Institute of Electrical and Electronics Engineers Inc., 11 2014.

[31] Y. Wang, A. Aksoz, T. Geury, S. B. Ozturk, O. C. Kivanc, and O. Hegazy, "A review of modular multilevel converters for stationary applications," 11 2020.

[32] S. Cui, J. Hu, and R. W. De Doncker, "Control and Experiment of a TLC-MMC Hybrid DC-DC Converter for the Interconnection of MVDC and HVDC Grids," *IEEE Transactions on Power Electronics*, vol. 35, pp. 2353–2362, 3 2020.

[33] D. Vrančić and S. Lumbar, "Improving PID Controller Disturbance Rejection by Means of Magnitude Optimum," tech. rep., 2004.

[34] B. N. Biswas, S. Chatterjee, S. P. Mukherjee, and S. Pal, "A discussion on Euler method: a review," Tech. Rep. 2, 2013.

[35] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings: Electric Power Applications*, vol. 153, no. 5, pp. 750–762, 2006.

[36] G. Tsolaridis, E. Kontos, S. K. Chaudhary, P. Bauer, and R. Teodorescu, "Internal balance during low-voltage-ride-through of the modular multilevel converter statcom," *Energies*, vol. 10, no. 7, 2017.

[37] S. Du, J. Liu, and T. Liu, "Modulation and closed-loop-based DC capacitor voltage control for MMC with fundamental switching frequency," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 327–338, 2015.

[38] S. Samimi, F. Gruson, X. Guillaud, and P. Delarue, "Control of DC bus voltage with a Modular Multilevel Converter," in *2015 IEEE Eindhoven PowerTech, PowerTech 2015*, Institute of Electrical and Electronics Engineers Inc., 8 2015.

[39] K. Shinoda, A. Benchaib, and J. Dai, "DC Voltage Control of MMC-based HVDC grid with Virtual CapacitorControl," pp. 1–10, 2017.

[40] Q. Zheng, J. Li, X. Ai, J. Wen, and J. Fang, "Overivew of grid codes for photovoltaic integration," in *2017 IEEE Conference on Energy Internet and Energy System Integration, EI2 2017 - Proceedings*, vol. 2018-January, pp. 1–6, Institute of Electrical and Electronics Engineers Inc., 6 2017.

[41] D. Committee of the IEEE Power and E. Society, "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems Sponsored by the Transmission and Distribution Committee IEEE Power and Energy Society," tech. rep., 2014.

[42] R. Li, J. E. Fletcher, and B. W. Williams, "Influence of third harmonic injection on modular multilevel converter-based highvoltage direct current transmission systems," *IET Generation, Transmission and Distribution*, vol. 10, pp. 2764–2770, 8 2016.

[43] T. van den Boom and B. de Schutter, *Optimization for Systems and Control*. TU Delft, 9 2021.

[44] G. Bergna-DIaz, J. A. Suul, E. Berne, J. C. Vannier, and M. Molinas, "Optimal Shaping of the MMC Circulating Currents for Preventing AC-Side Power Oscillations from Propagating into HVdc Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, pp. 1015–1030, 6 2019.

[45] J. Orsinger, "Discrete control delay identification," 3 2021.

[46] C. Wang, L. Xiao, H. Jiang, and T. Cai, "Analysis and Compensation of the System Time Delay in an MMC System," *IEEE Transactions on Power Electronics*, vol. 33, pp. 9923–9936, 11 2018.

Appendix A

MMC Technology and Modulation

A.1 Two level voltage source converter

Figure A.1 provides the circuit diagram of the two-level voltage source converter as introduced in Section 2.1.1. This converter is used to put the advantages and disadvantages of the MMC in MVDC into perceptive.

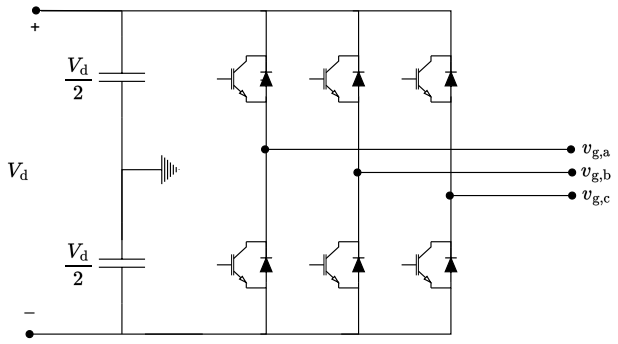


Figure A.1: Schematic diagram of the two-level voltage source converter.

A.2 MMC circuit configurations

In Section 2.2 the double-star configured MMC is discussed, which is most applicable for medium and high voltage DC applications. Though in addition to this configuration, the MMC can be star-configured, delta-configured and can be in Dual configuration. Figures A.2, A.3 and A.4 provided the structure of the star, delta and dual configuration of the MMC, respectively [15].

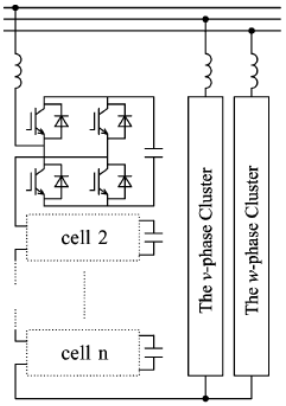


Figure A.2: Schematic diagram of the multilevel modular converter in star configuration.

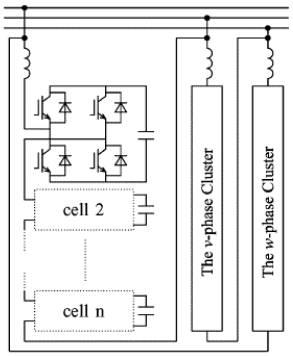


Figure A.3: Schematic diagram of the multilevel modular converter in delta configuration.

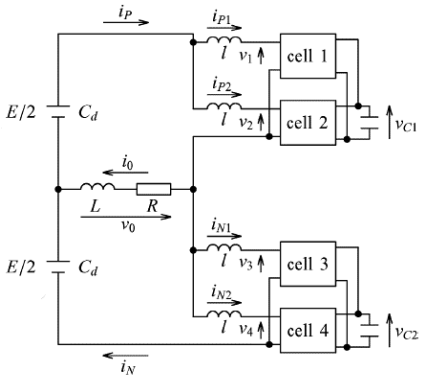


Figure A.4: Schematic diagram of the multilevel modular converter in Dual configuration.

A.3 Pulse width modulation waveforms

In section 2.3.3 the Pulse Width Modulation PWM stage is introduced. In the PWM stage, the reference insertion indices $n_{\mathrm{u,l}}$ are converted into appropriate submodule switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$. This conversion is performed such that the inserted arm voltages approximate their intended values. The PWM process is based on a comparison of the reference signal $n_{\mathrm{u,l}}$ with a triangular carrier signal n_{tri}. The output of this process it the submodule switching signals $s^{\mathrm{i}}_{\mathrm{abc}}$ as indicated in Figure A.5.

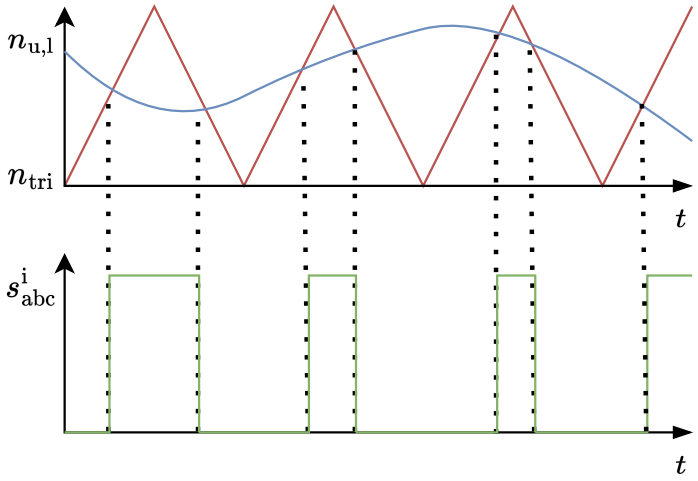


Figure A.5: Basic concept of pulse width modulation.

Following Figure 2.5, it can be concluded that there are multiple techniques for implementing PWM. These techniques differ in their positioning of the triangular carrier signal. Figure A.6 provides the schematic representation of the three types of LSC-PWM: Phase-disposition (PD), Phase-opposition-disposition (POD) and Alternate-Phase-opposition-disposition(APOD) [21].

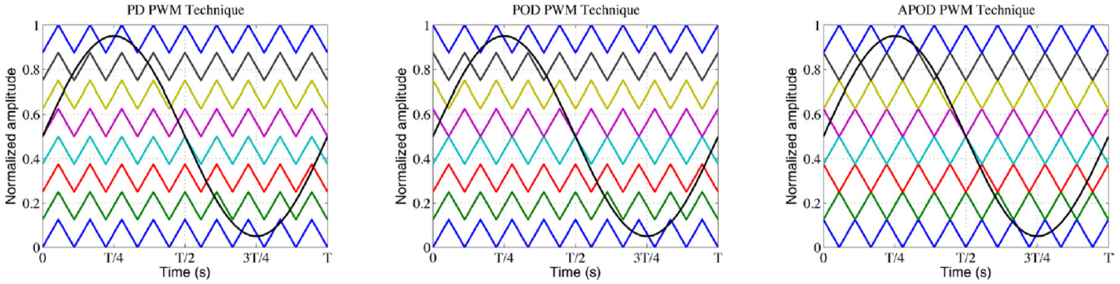


Figure A.6: Schematic representation of the LSC-PWM: PD, POD, APOD.

Figure A.7 provides the schematic representation of the Phase Shifted Carrier-PWM (LSC-PWM) technique [21]. As an alternative to pulse width modulation, Nearest Level Control (NLC) can be used. Figure A.8 provides a schematic representation of the NLC technique [21].

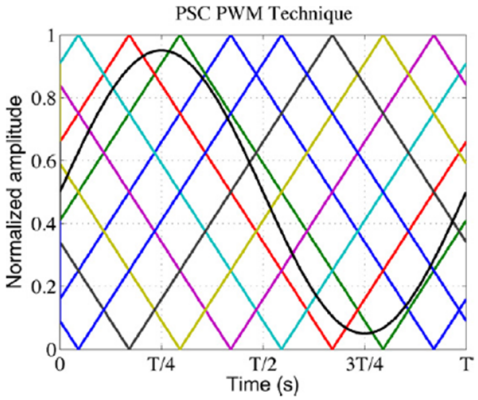


Figure A.7: Schematic representation of the PSC-PWM.

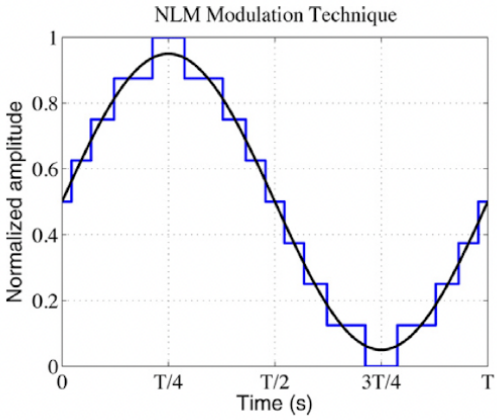


Figure A.8: Schematic representation of the NLC.

A.4 Submodule capacitor balancing

In Section 2.4 the submodule capacitor balancing is discussed. This stage is used to actively balances the arm submodule capacitor voltages to counteract any divergence. The SM capacitor balancing is performed using various methods. All methods use the output of the modulation stage: the switching signals s^{i}_{abc} and alter these accordingly. The submodule capacitor balancing methods discussed in Section 2.4 are presented as flowcharts. First, Figure A.9 represents the submodule sorting method [11]. Second, Figure A.10 represents the predictive sorting method [11]. Third, Figure A.11 represents the average submodule voltage tolerance band method [11]. Finally, Figure A.12 represents the individual submodule voltage tolerance band [11].

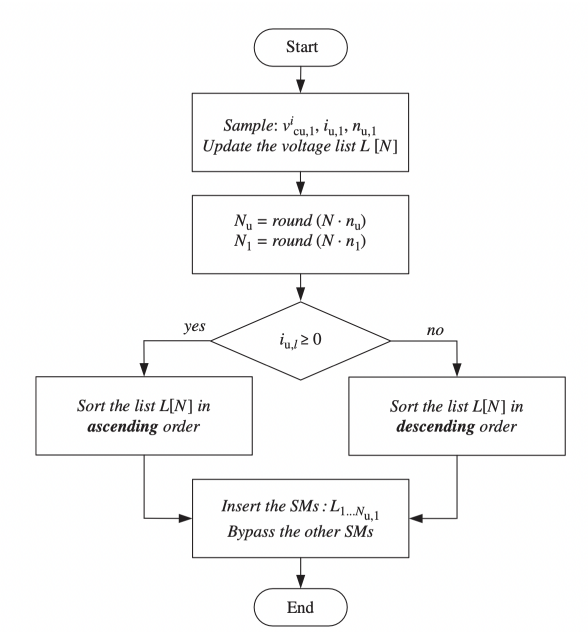


Figure A.9: Flowchart representation of the submodule sorting method.

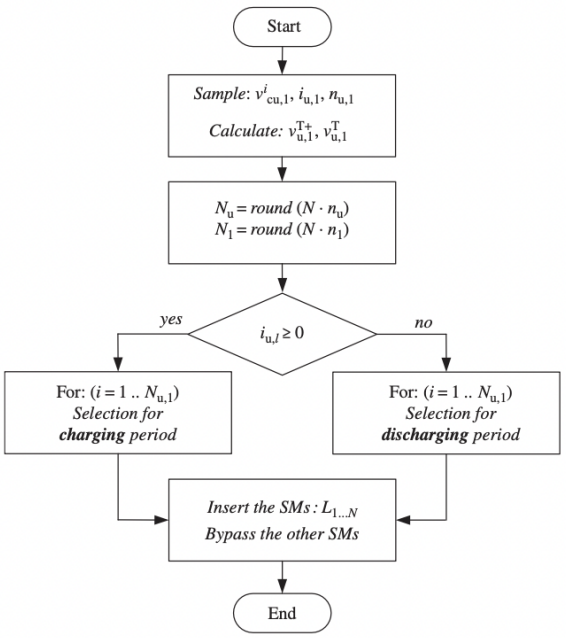


Figure A.10: Flowchart representation of the predictive sorting method.

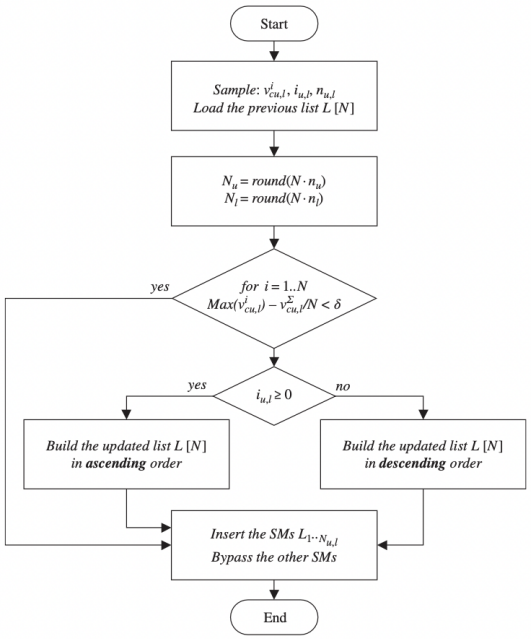


Figure A.11: Flowchart representation of the average submodule voltage tolerance band method.

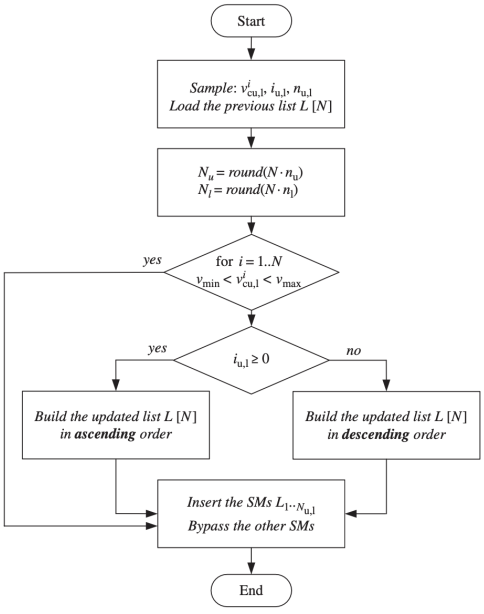


Figure A.12: Flowchart representation of the individual submodule voltage tolerance band method.

Appendix B

MMC Simulation Models and Parameters

Throughout the report, controller design and controller tuning is performed using simulation models. These simulation models are based on the dynamic models of the MMC, AC grids and DC link, which were elaborately discussed Chapter 3. This appendix provides a more detailed description of the two developed simulation models and the associated parameters. The two simulation models each have a unique approach toward accuracy and simplicity for testing the MMC controller. First, in Appendix B.1, the back-to-back MMC Arm-Level Averaged (ALA) simulation model is discussed. This model constrains two MMCs, which are connected via a DC link. In addition, both of them are connected to individual AC networks. Second, in Appendix B.2, the Imperix MMC Submodule-Level Averaged (SLA) simulation model is explained. This model contains a single MMC that is connected to a DC-side resistor and an AC-side network.

B.1 Back-to-back MMC ALA simulation model

The back-to-back MMC arm-level averaged model simulates the workings of an MMC-based DC link. This model makes use of two main assumptions. At first, it uses the assumption that the sum capacitor voltage is evenly distributed over the arm submodules. This assumption is provided in Equation (B.1) and applies to all six MMC arms.

$$v^{\mathrm{i}}_{\mathrm{cu,l}} = \frac{v^{\Sigma}_{\mathrm{cu,l}}}{N} \qquad with \;\; i \in [1,N] \tag{B.1}$$

By using this assumption, the concept of the individual capacitor voltages becomes redundant. So the ALA simulation model only stores the sum capacitor voltage to reflect the individual capacitor voltages. Second, the ALA simulation model assumes ideal semiconductor switching. Unlike a full physics-based model, the IGBTs are modelled as ideal switches, neglecting all switching transients. This allows for a further simplification of the simulation model where the MMC arms are to be represented as controllable voltage sources. The N submodules are simplified to a single arm voltage source, indicated in Equation (B.2). Following this simulation structure allows for a significant reduction in the computation time of the simulation, which enables the studies to investigate the power-system behaviour of the MMC.

$$v_{\mathrm{u,l}} = n_{\mathrm{u,l}} \cdot v^{\Sigma}_{\mathrm{cu,l}} \tag{B.2}$$

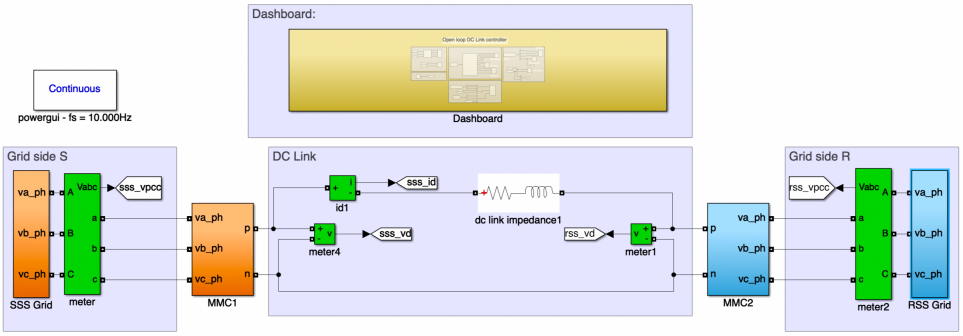


Figure B.1: Structure of the back-to-back MMC ALA simulation model in Simulink.

Figure B.1 contains an overview of the back-to-back MMC ALA simulation model implemented in Matlab Simulink. For this simulation the configuration parameters of the MMC and AC grid are provided in Table B.1.

Table B.1: Configuration parameters of the MMC ALA simulation model.

ALA-simulation parameters:		
Simulation parameters:		
Control frequency	f_c	10kHz
AC grid:		
Grid frequency	ω_1	314.2 rad/s
Grid voltage L-N (rms)	v_g	5.77kV
Grid inductance	L_g	287µH
Grid resistance	R_g	9mΩ
DC link:		
DC link resistance	R_l	0.1Ω
DC link inductance	L_l	100µH
Rated DC link voltage	V_{dr}	17.1kV
MMC:		
Rated apparent power	S_{max}	11MVA
Submodule capacitance	C	3.3mF
DC link capacitance	C_d	100µF
Number of arm submodules	N	9
Arm inductance	L	4mH
Arm resistance	R	0.1 Ω
Maximum output current	$i_{s,max}$	907A

B.2 Imperix MMC SLA simulation model

The Imperix MMC switch-level averaged model simulates the workings of the Imperix MMC when connected to a DC-load. This simulation model is related to the measurement approach of Chapter 7, which uses a DC load to emulate the second MMC of the distribution link. Similar to the ALA model, the SLA simulation model uses the assumption of ideal semiconductor switching. This allows for a simplification of the full physics-based model, by neglecting the switching transients. As a result, the MMC submodules in this model are simplified by replacing the IGBTs with ideal switches. In contrast to the ALA model, the SLA model does account for the spread in the submodule capacitor voltages. It, therefore, stores the individual capacitor voltages. This type of simulation allows for the verification of the SM balancing controller and the fault-trigger module, as explained in Chapter 7.

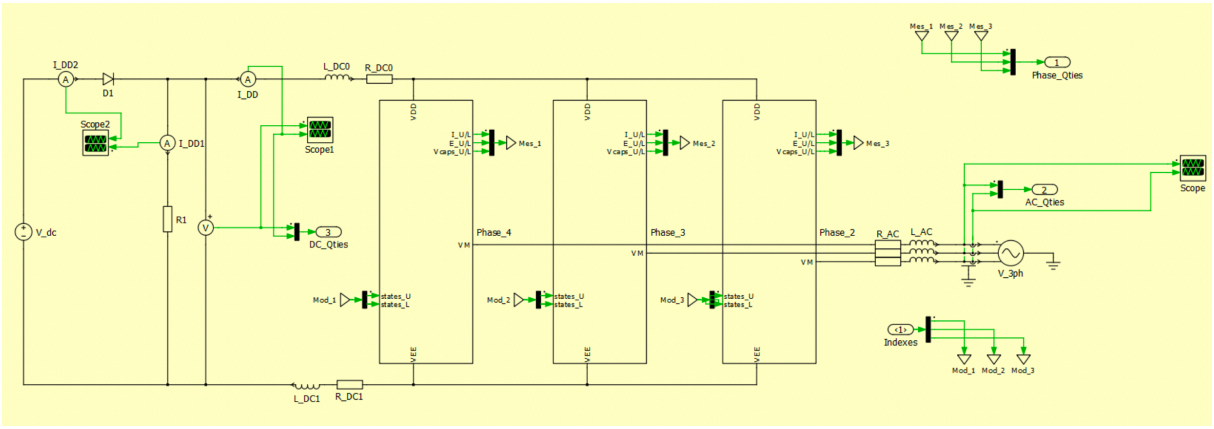


Figure B.2: Structure of the Imperix MMC SLA simulation model.

Figure B.2 contain an overview of the Imperix MMC SLA simulation model implemented in Plexim. For the simulation the configuration parameters of the MMC and AC grid are provided in Table B.2.

Table B.2: Configuration parameters of the Imperix MMC SLA simulation model.

SLA-simulation parameters:		
Simulation parameters:		
Control/switching frequency	f_c	5.0kHz
Sampling frequency	f_s	5.0kHz
AC grid:		
Grid frequency	ω_l	314.2 rad/s
Grid voltage L-N (rms)	v_g	23.6V
Grid inductance	L_g	2.0mH
Grid resistance	R_g	10mΩ
DC link:		
DC link resistance	R_l	50mΩ
DC link inductance	L_l	100µH
Rated DC link voltage	V_{dr}	70V
DC side load	R_{load}	100Ω
MMC:		
Submodule capacitance	C	5.0mF
DC link capacitance	C_d	0F
Number of arm submodules	N	4
Arm inductance	L	2.4mH
Arm resistance	R	60 mΩ
Maximum output current	$i_{s,max}$	15A

B.3 Imperix MMC delay identification

In Sections 6.2.3 and 6.2.4 the output current control and circulating current control were tuned, respectively. This tuning involved the determination of the proportional and integral gain of the PI controllers, which was achieved using the Magnitude Optimum (MO) tuning method. This method concentrated on improving the closed-loop tracking performance of the system. As part of the MO tuning method, a delay identification is performed to find the time delay involved with the control system: T_d. T_d is effectively the time needed to measure the state of the MMC, perform the control operation and generate the proper switching signals.

As the operation of a digital controller requires time for computations and measurement processing. The controller always introduces a delay along the control chain. This delay has an impact on closed-loop response time and thus reduces the achievable closed-loop control bandwidth [45]. For the delay identification in the Imperix controller Figure B.3 can be used.

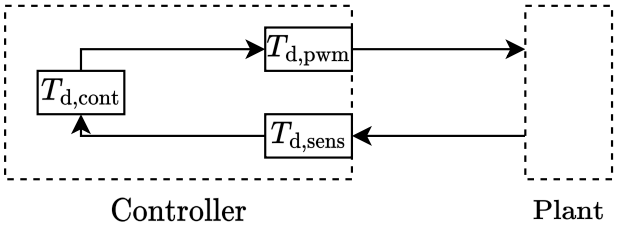


Figure B.3: Delay identification Imperix digital controller.

From this figure can be concluded that the total loop delay time T_{d} is composed of the sensing delay $T_{\text{d,sens}}$, the control delay $T_{\text{d,cont}}$, and the modulator delay $T_{\text{d,pwm}}$. Note that the control delay $T_{\text{d,cont}}$ can be fragmented into multiple sub delays, as indicated by Ehquation (B.3). In this equation $T_{\text{d,acq}}$ represents the acquisition delay, $T_{\text{d,pr}}$ the processing delay, and $T_{\text{d,wr}}$ the write delay. The ξ term is used for the controller synchronisation, as the output of the controller only updates at $\frac{T_{\text{s}}}{2} * (2n+1)$. So the ξ term increases $T_{\text{d,cont}}$ to its nearest update time-point.

$$T_{\text{d,cont}} = T_{\text{d,acq}} + T_{\text{d,pr}} + T_{\text{d,wr}} + \xi \tag{B.3}$$

For the Imperix B-Box RCP applies that: $T_{\text{d,acq}} = 2.072\mu s$, $T_{\text{d,pr}} = 3.9\mu s$, $T_{\text{d,wr}} = 0.1\mu s$ [45]. As the control period is quite large at $T_{\text{s}} = 1/5000 = 200\mu s$, only half the sampling period is needed $T_{\text{d,cont}} = \frac{T_{\text{s}}}{2}$.

Following [45], it can be concluded that the sensing delay of the B-Box RCP can be neglected as $T_{\text{d,sens}} \approx 800ns$. Furthermore, following [46] it can be concluded that the modulator delay of the MMC is $T_{\text{d,pwm}} = [0.25T_{\text{s}}, 0.5T_{\text{s}}]$ depending on the used sampling method. Then using these three defined delays, the total loop delay can be specified as: $T_{\text{d}} = [0.75T_{\text{s}}, T_{\text{s}}]$. Figure B.4 provides a further overview of the delay process.

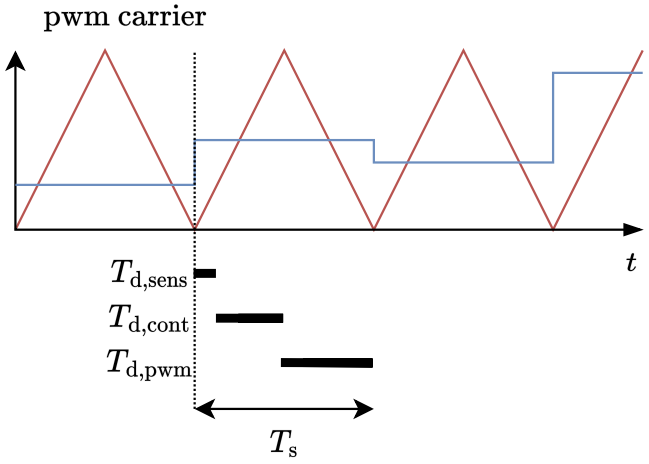


Figure B.4: Delay calculation Imperix digital controller.

Appendix C

MMC Analytical Assumptions

With the analytical derivation in Chapter 4 the DC link voltage enhancement boundary was derived. The boundary expression, provided in Equation (4.18), is obtained using a set of assumptions. These assumptions can cause a discrepancy between the analytical enhancement boundary $k_{\mathrm{d,max}}$ and the maximum enhancement observed in simulations/experiments. As a result, the practical operating range of Equation (4.18) was limited to higher power factors. In addition, the controller enhancement function of Equation (5.1) was proposed, to operate at a more conservative enhancement compared to $k_{d,max}$. In this appendix, some of the used assumptions are verified.

C.1 Linear approximation of square root

The first approximation that is encountered is the linear approximation of the sum capacitor voltage v_{cu}^{Σ}. This approximation is done in Equation (4.11) and is restate in Equation (C.1). In this equation the square root expression of the ripple energies W_{Σ},W_{Δ} is linearly approximated at zero.

$$V_{\mathrm{d}}\sqrt{1+\frac{N}{CV_{\mathrm{d}}^2}(\Delta W_{\Sigma}+\Delta W_{\Delta})} \approx V_{\mathrm{d}}+\frac{N}{2CV_{\mathrm{d}}}(\Delta W_{\Sigma}+\Delta W_{\Delta}) \tag{C.1}$$

If this equation is normalised with V_{d} and define $x=\frac{N}{CV_{\mathrm{d}}^2}(\Delta W_{\Sigma}+\Delta W_{\Delta})$ then Equation (C.1) becomes Equation (C.2). Both equations are plotted as a function of x in Figure C.1.

$$\sqrt{1+x} \approx 1+\frac{1}{2}x \tag{C.2}$$

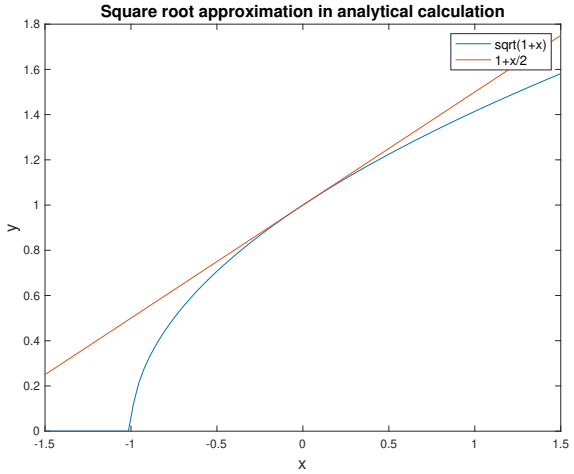


Figure C.1: Square root and linear approximation

From this figure can be concluded that the linear curve approximates the square root curve with significant accuracy for small norms of x: $|x| << 1$. Note that this conclusion corresponds to: $|\Delta W_{\Sigma}+\Delta W_{\Delta}| <<$

$\frac{CV_d^2}{N}$. This induces that the linear approximation of the sum capacitor voltage v_{cu}^{Σ} only holds for small values of the ripple energies W_{Σ},W_{Δ}. This result can also be observed by comparing Figure C.2 and Figure C.3. These two figures show the upper arm voltage v_u and sum capacitor voltage v_{cu}^{Σ} for a high ($pf = 0.95$) and low ($pf = 0.0$) power factor respectively. It can be seen that, at the time point of interest $\omega t = \pi$, for the higher power factor the linear approximation perfectly resembles the actual sum capacitor voltage. In contrast this approximation is compromised for the lower power factor. Furthermore, it should be noted that this discrepancy is accelerated at enhanced DC link voltage levels.

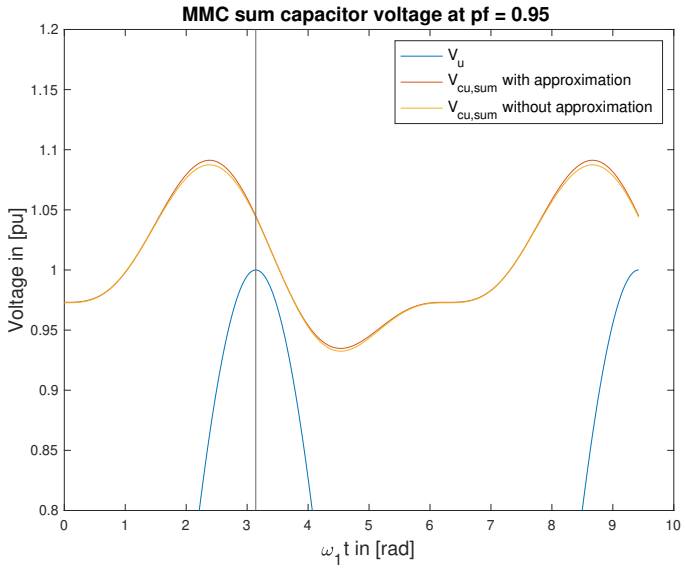


Figure C.2: The upper arm voltage and sum capacitor voltage decomposed for $pf = 0.95$.

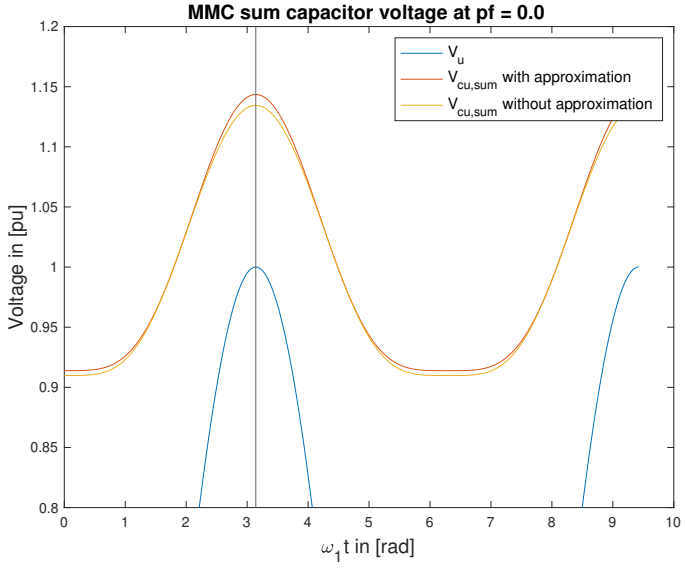


Figure C.3: The upper arm voltage and sum capacitor voltage decomposed for $pf = 0.0$.

It can however be concluded that for power factors close to 1.0 the linear approximation of the square root expression is of significant accuracy. This complies with the requirement of the MVDC distribution link. As the main task of the DC link is to transmit active power and thus only operated at high power factors.

C.2 Constraint time-point assumption

The second considered approximation is the constraint time-point assumption. During the analytical derivation of enhancement boundary, the assumption was made that spacing between v_{cu}^{Σ} and v_{u} is most stringent near $\omega_1 t = \pi$ independent of the power factor. This allows Equation (4.15) to be simplified to Equation (4.16). Though, note that this assumption provokes the neglect of the $\frac{2\hat{V}_s i_c}{\omega_1}\sin(\omega_1 t)$ term in (4.15). Therefore the active power P does not impact the enhancement boundary, even though it does affect the sum capacitor voltage v_{cu}^{Σ} ripple.

To investigate the impact of the constraint time-point assumption, Figure 4.5 can be used. This figure illustrates the arm voltage and sum capacitor voltage for three operating power factors. Note that Figure 4.5 does neglect the saturation of v_{u} at v_{cu}^{Σ} for illustration reasons. It can be observed that for $pf = 1.0$, the stringent time-point is positioned to the right of the peak of v_{u}. So the constraint time-point is $\omega_1 t > \pi$. This shows that operating at analytical enhancing factor $k_{\mathrm{d,max}} = 0$ with $Q = 0$ would violate constraint (4.1).

To analyse the constraint time-point assumption for different power factors, Figure C.4 is used. This figure shows the time points for which the spacing between v_{cu}^{Σ} and v_{u} is minimal, as a function of the operating power factor. Note that result of this figure relate to an MMC that is operating at the rated output current i_{s}, rated DC link voltage $V_{\mathrm{dr}} = 17.1kV$, and with an arm impedance $X_{\mathrm{c}} = 8.68\Omega$, all according to the properties proposed in Appendix B.1.

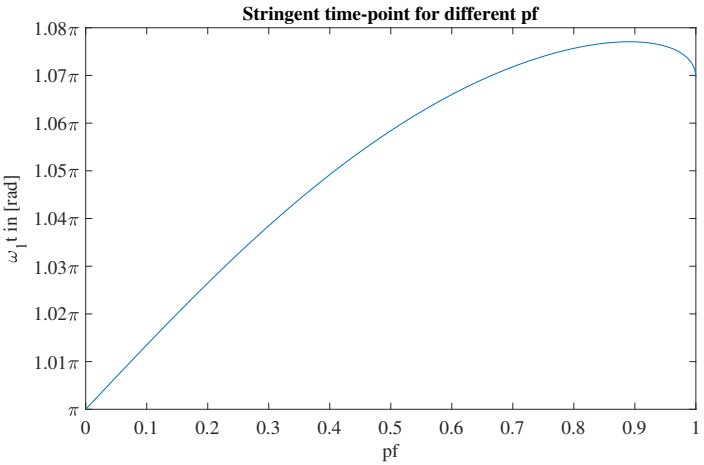


Figure C.4: Stringent time-point as a function of the power factor.

In Figure C.4 can be observed that the constraint time-point assumption is most relevant for lower power factors. Then the minimal spacing between v_{cu}^{Σ} and v_{u} is obtained close to $\omega_1 t = \pi$, in line with the assumption. Though for an operation at unity power factor, the restricting time-point is around $\omega_1 t = 1.07\pi$, which is larger than the assumed π. This causes an overestimation of the analytical enhancement boundary $k_{\mathrm{d,max}}$ compared to the actual enhancement limit observed in simulations/experiments. These observations are in line with the expectations, considering that the neglected $\frac{2\hat{V}_s i_c}{\omega_1}\sin(\omega_1 t)$ term would be zero when $P = 0$.

Appendix D

Experimental Setup and Devices

For the MMC controller implementation in Chapter 6 and experimental verification in Chapter 7, a lab-scale MMC is used. The lab-scale MMC prototype used in the experiments is the "MMC test bench" from Imperix, later denoted as the Imperix MMC. The Imperix MMC is connected to the measurement setup, which contains: three parallel DC loads, an AC grid emulator, a DC power supply, and measurement equipment. This appendix provides a detailed overview of the properties of the Imperix MMC and the characteristics of the measurement setup.

D.1 Imperix MMC test bench

One of the main devices used in the experimental setup is the Imperix MMC. This prototype MMC is shown in Figures D.1 and D.2, where it is constructed in the the double-star configuration with half-bridge submodules. The Imperix MMC is aimed at supporting research related to MMC control verification and operating behaviour validation. The converter is implemented for a 230/400V grid-tied operation with a rated power of 5-8 kVA. The main properties of the Imperix MMC can be summarised as follows:

- **Submodules**: 24 full bridge PEH2015 submodules
  - 4 Power switches, IGBTs
  - 5.04mF submodule capacitance
  - Capacitor voltage sensor and arm current sensor
  - Optical gate drivers inputs
  - 200V, 15A maximum rating
- **Gate drivers**: 3 B-Box RCP controllers
  - 500kHz sampling
  - Hardware protections
  - ACG SDK software
- **Arm inductors**: 6 inductors 2.5mH, 20A
- **Sensors**: Grid voltage and arm current sensors
  - 3 DIN 800V voltage sensors, sensitivity 2.46mV/V
  - 6 DIN 50A current sensors, sensitivity 99mV/A
- **Grid connection**: Grid connection panel
  - 16A circuit breaker
  - Bypass relay 230V, 63A
  - Precharge relay 230V, 63A

- Precharge resistors 47Ω

Most of these characteristic were used in the Imperix MMC SLA simulation model, as discussed in Appendix B.2. The associated model parameters of the Imperix MMC are defined in Table B.2.

Figure D.1: Imperix MMC test bench, front view

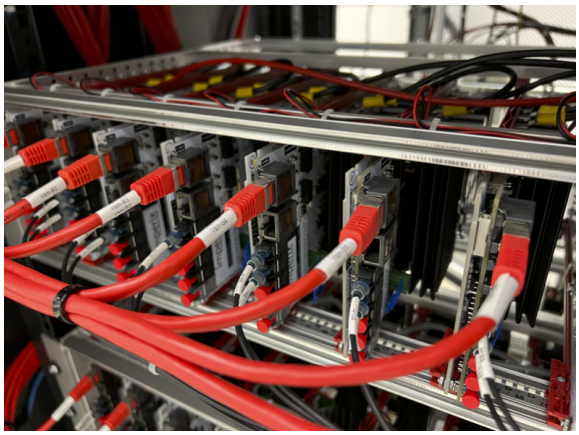


Figure D.2: Imperix MMC test bench, leg submodules

D.2 The measurement setup

In addition to the Imperix MMC, the experimental setup contains a set of devices connected to the AC and DC terminals. An overview of the complete measurement setup was provided in Figure 7.2. Where the individual devices are defined as follows:

- **DC loads**: three parallel variable power resistors
  - Albert van der Perk: A381
  - Variable resistance of $[0\Omega, 65\Omega]$
  - Current rating of $5A$
- **DC power supply**: Delta Elektronika SM6000 Series
  - Variable output voltage of $[0V, 300V]$
  - Output current rating of $20A$
  - Overload and short circuit protection
- **AC power supply**: Cinergia GE20
  - Four-quadrant 3 phase AC grid emulator and electronic load

  - Rated power 20 kVA
  - $\hat{v}_{\mathrm{g}} = \pm 400V$ phase-neutral
  - Set-point resolution of 10mVrms
  - Fundamental frequency range $f_1[10, 100]Hz$
  - Grid current $THD_{\mathrm{i}} < 3\%$
  - Modbus control protocol with Labview
- **Oscilloscope**: Yokogawa DLM2034
  - 4 analog input channels
  - Sampling frequency $f_{\mathrm{s}} = 350MHz$
  - External trigger functionality
- **Voltage probe**: Keysight Technologies N2791A
  - Input voltage range $\pm 700V$ common mode
  - input voltage range $\pm 700V$ differential mode
  - 25 MHz bandwidth
  - 100:1 attenuation ratio
- **Voltage probe**: Testec TT-SI9101
  - Input voltage range $\pm 700V$ common mode
  - input voltage range $\pm 700V$ differential mode
  - 100 MHz bandwidth
  - 100:1 attenuation ratio
- **Current probe**: Keysight Technologies N2782B
  - Input current range $\pm 30A$
  - 50 MHz bandwidth
  - 10:1 attenuation ratio

Figure D.3: Measurement setup with the Imperix MMC.

Appendix E

Oscilloscope Plots

In Chapters 7 and 8, the experimental measurement results are processed and provided in various figures. Plots like Figures 7.4 and 7.5 showed the measurement data of the Yokogawa oscilloscope. Though, recall from Chapter 6 that the output of the MMC is generated with PWM at a control/switching frequency of $f_c = 5kHz$. This implies that the measurement data contains high-frequency components related to the switching events. As this thesis is aimed at the power system behaviour of the MMC, the switching transients become noises in the analysis. Therefore, in Chapters 7 and 8, the measurement data is filtered before plotting/processing it in as experimental results. This filtering is performed using a low-pass FIR filter with a given filter-order and cutoff frequency. To better understand the measurement data, the unfiltered oscilloscope plots are provided in the following figures. Figures E.1 and E.2 show the MMC arm voltage measurements when operated at the rated DC link voltage of 100V. These relate to the measurements in Figure 7.4. Figures E.3 and E.4 show the MMC arm voltage measurements when operated at an enhanced DC link voltage of 107V. These relate to the measurements in Figure 7.5.

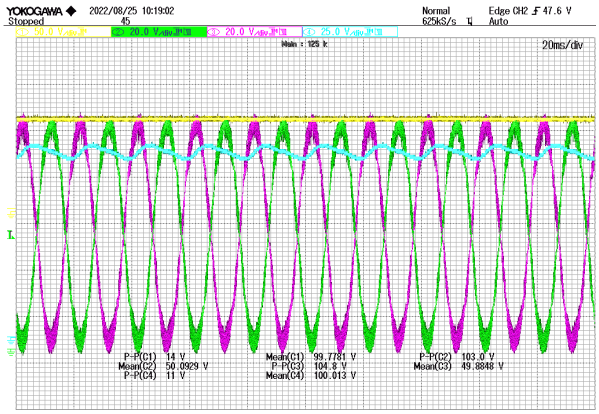


Figure E.1: Scope plot: Q = 0VAR, V_d = 100V

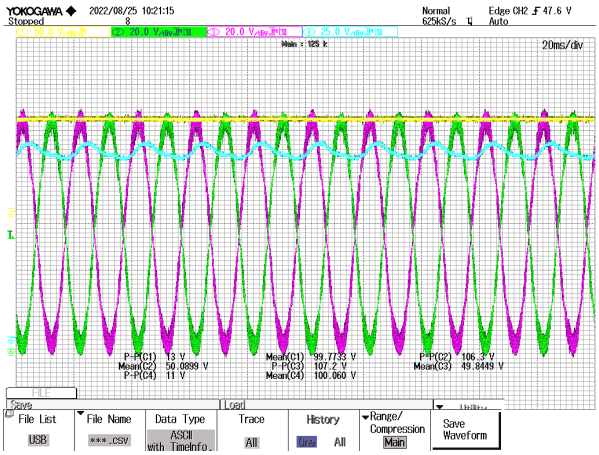


Figure E.2: Scope plot: Q = 200VAR,V_d = 100V

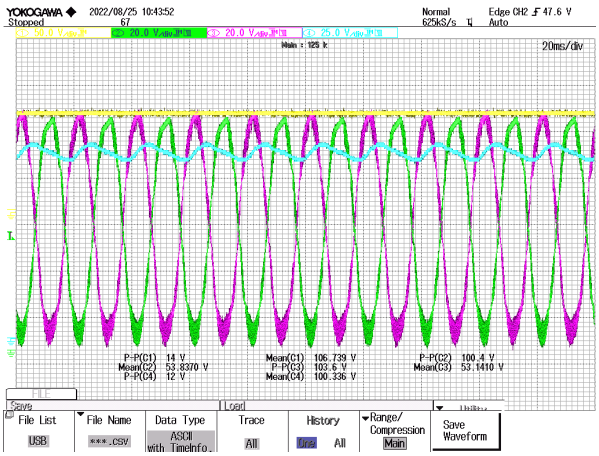


Figure E.3: Scope plot: Q = 0VAR,V_d = 107V

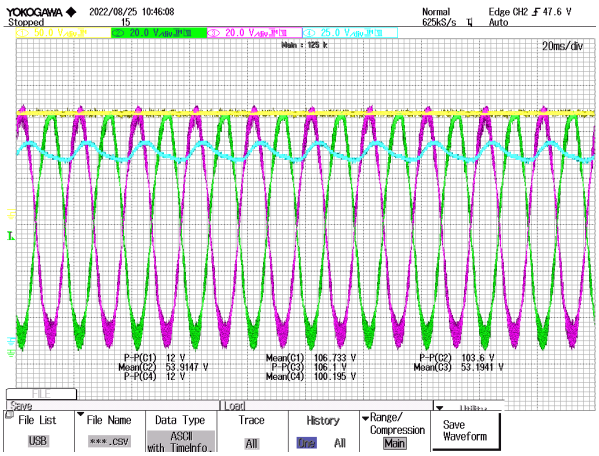


Figure E.4: Scope plot: Q = 200VAR,V_d = 107V