A High-Resolution Capacitance-to-Digital Converter based on Iterative Discharging

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Contents

1 Introduction

In this chapter, the background and the motivation of the thesis will be given. The performance of the previous state-of-art capacitor-to-digital converter (CDC) designs will be given. At the end of this chapter, the outline of the thesis will be given.

1.1 Background and motivation

Capacitive sensors are quite attractive for low power applications as they don't consume static power. The working principle of the capacitive sensors is based on the modulation of an electrical capacitance by a physical parameter of interest. Such principle is commonly used in in pressure sensors, humidity sensors, liquid-level gauges, accelerometers and capacitive touch screens (shown in figure 1) [1]. To read out the capacitance, an interface circuit is needed.

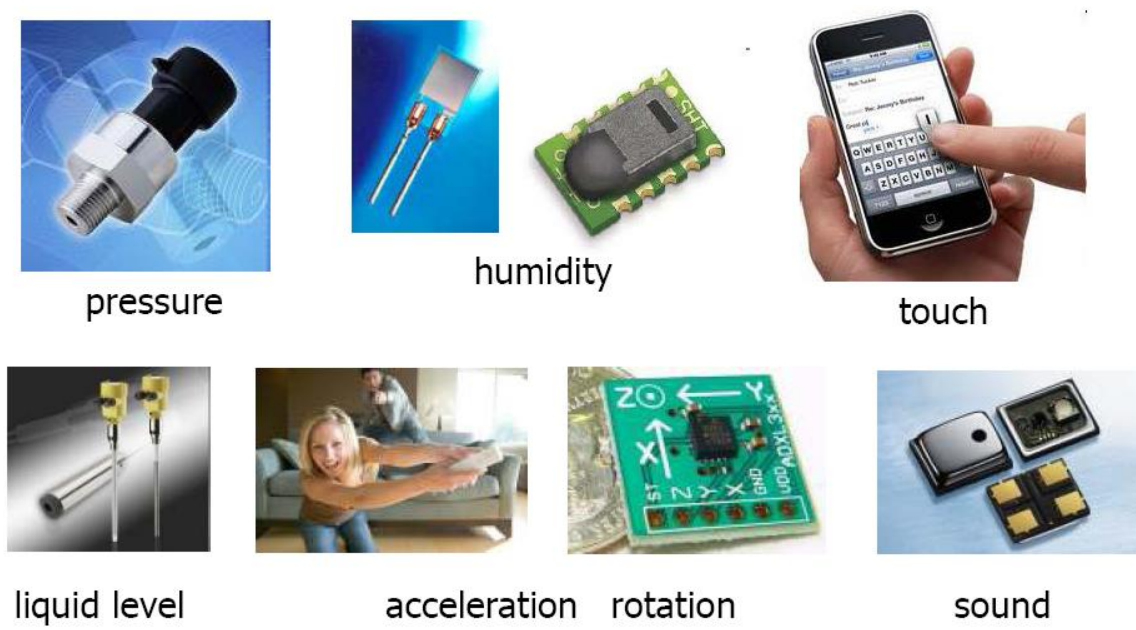

Figure 1 Capacitive sensors for different application [1]

One common method to measure capacitance is to use a charge amplifier and an analog-to-digital converter (ADC) (shown in figure 2).

However, it suffers from the requirement on the amplifier. To achieve a high resolution, a low noise amplifier is required, which means the amplifier will consume more power. Also, the feedback capacitor can be large. It should have similar size as the sensor capacitor.

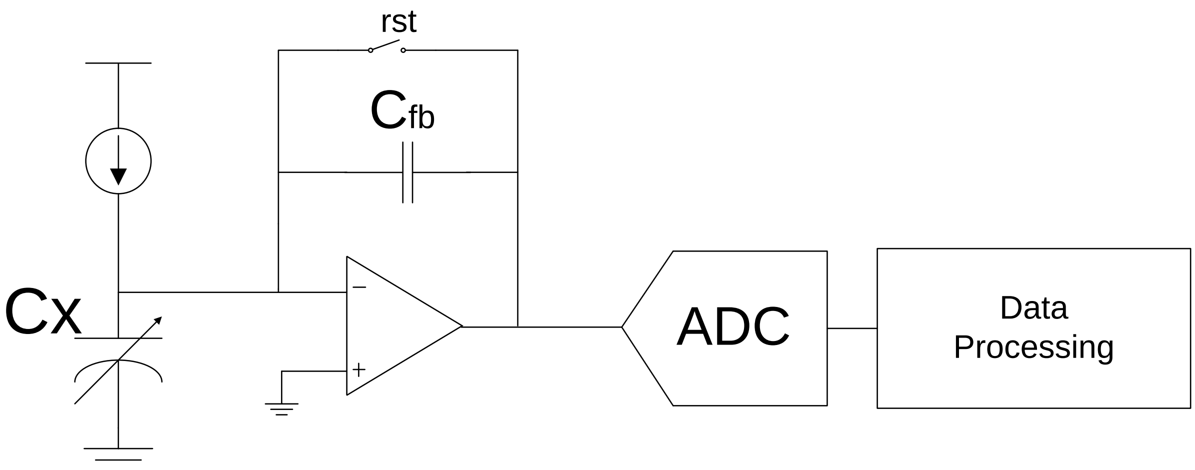

Figure 2 Traditional method of using a charge amplifier and an ADC

Compared with this method, a more attractive way is to convert the capacitance into the digital domain without using a voltage as an intermediate step. Such capacitive sensing system usually contains a capacitive sensor and an interface to convert the data into digital domain. We usually refer to it as capacitor-to-digital converter (CDC). There are many different CDC topologies, like SAR based CDCs [2] [3], sigma delta based CDCs [4].

Usually, the capacitive sensor hardly consumes static power, so the dominant power consumption in CDCs comes from the interface circuit. Therefore, the power in the interface circuit is critical for the whole application. SAR based topology is popular for low power applications [2] [3], but provides only moderate resolution (<=10bits). For application requiring higher resolution, a sigma-delta based topology is suitable [4]. Zoom-in CDC is another candidate which merges the SAR and sigma-delta together [5]. Also, there are many other topologies, like dual slope CDC [6], period-modulation (PM) CDC [7] and digital CDC, in which iterative discharge process is used [8]. Table 1 gives the parameters of the previous state-of-art design.

Table 1 Previous state-of –art design

	ISSCC 2014 [2]	VLSI 2016 [3]	JSSC 2013 [4]	VLSI 2014 [5]	JSSC 2015 [6]	ISSCC 2015 [7]	ISSCC 2015 [8]
Technology (nm)	180	180	160	180	180	160	40
Method	CDS+SAR	SAR	$\Sigma-\Delta$	Zoom-in	Dual slope	PM	Digital
Area (mm^2)	0.49	0.1	0.28	0.456	0.105	0.05	0.0017
Resolution (fFrms)	6	1.1	0.07	0.16	8.7	1.443	12.3
Conversion time(µs)	4000	16	800	230	6400	210	19
Power(µW)	0.16	7.25	10.32	33.7	0.11	14	1.84
FOM (pJ/Step)	1.3	0.035	1.4	0.175	5.3	1.87	0.141

For the industry, the cost of the interface is also critical. Compared with traditional mixed-signal interfaces, a more digital implementation is beneficial in terms of the ease of process migration and a relatively shorter time to market. The first fully digital CDC was presented by Wanyeong Jung, presented in ISSCC 2015 [8]. However, this design suffers from relative poor resolution. This thesis work will focus on improving the resolution while keeping the promising digital feature.

1.2 Thesis organization

The thesis is divided into the following chapters. Chapter 2 analyses the previous work and gives the system-level design of the proposed CDC. Chapter 3 discusses the circuit-level design. The system simulation results and the layout of the chip will be given in chapter 4. Chapter 5 will describe the setup of the test environment. In chapter 6, measurement results will be given. The last chapter gives the conclusion.

1.3 Conclusion

In this chapter, the background and the motivation of the CDC design. The arrangement of the thesis is also given.

2 System level design

In this chapter, the system level design of the proposed CDC will be given. The following section starts with the introduction of the working principle of the architecture proposed by Michigan University [8] we will refer this as 'Michigan design', which is the first implementation of the fully digital CDC. A brief introduction on the working principle and an analysis of the design will be given. Based on that design, an improved architecture will be given, which gives a higher resolution. The improvement is done through interpolation. An analysis of the performance limitations of the proposed design will also be presented.

2.1 Architecture introduction on previous work

The first trial of a fully digital implementation of a capacitance to digital converter was made by Wanyeong Jung, presented in ISSCC 2015 [8]. An iterative discharge process is applied on the sensor capacitor to give the fully digital implementation. Delays are compared instead of voltages which enable to perform the comparison using only digital logic cells. In this section, a brief introduction will be given on such work, including its working principle and performance limitation.

In Figure 3 [1][8], a behaviour model and the waveform of the Michigan's design is given. The sensor capacitor (C_{SENSE}) is first charged to a voltage V_{high} when switch ϕ1 is turned on. After the sensor capacitor has been fully charged, it is disconnected form the source and connected to a load through switch ϕ2. As a result, C_{SENSE} is discharged and a voltage decrease over the sensor capacitor can be observed. When the voltage across the sensor capacitor is lower thanV_{low}, the comparator is triggered, which will generate a pulse at its output. The pulse width is proportional to the capacitor value. A larger sensor capacitance gives a wider pulse. The C_{SENSE} value is then calculated by quantizing the pulse width, which is done by a counter. The discharge process gives a non-linear voltage decrease. However, this non-linear process can still give a linear function in the time domain of the pulse width. The slope of the curve can be represented as:

$$\frac{dV_{SENSE}}{dt} = \frac{I(V_{SENSE})}{C_{SENSE}} \tag{2.1}$$

We can also write it in another form:

$$dt = C_{SENSE}\frac{dV_{SENSE}}{I(V_{SENSE})} \tag{2.2}$$

By doing integration at both sides, we can find in the following expression that the pulse width is in proportional with capacitance value. Figure 4 shows this process.

$$T_{PULSE} = \int dt \propto C_{SENSE} \tag{2.3}$$

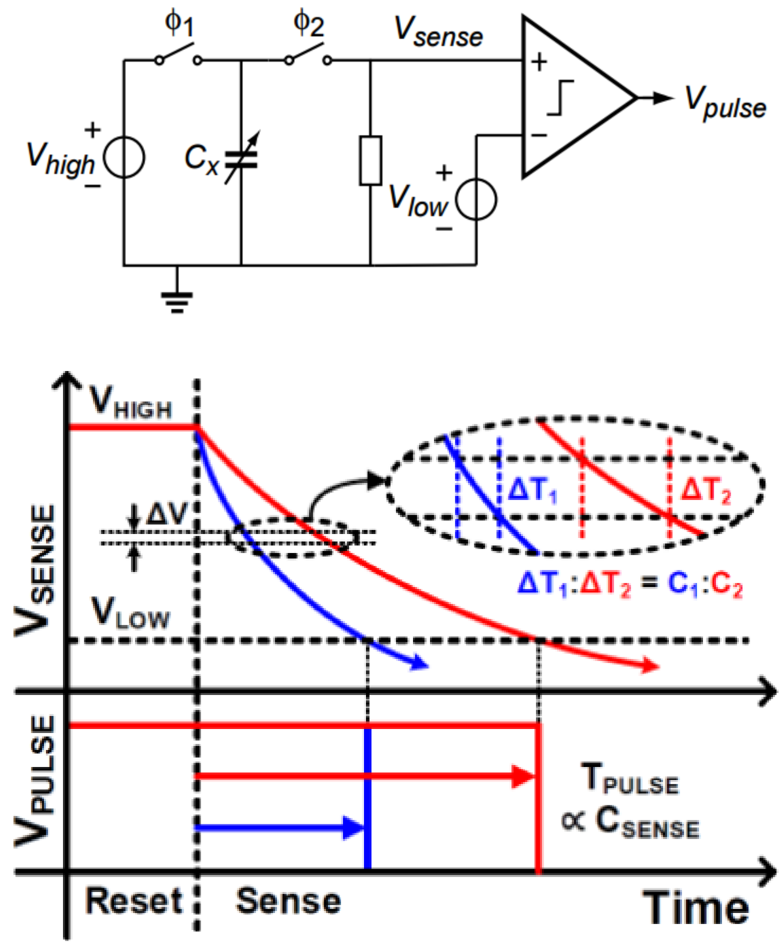

Figure 3 Behaviour model and the waveform of the Michigan's design [1][8]

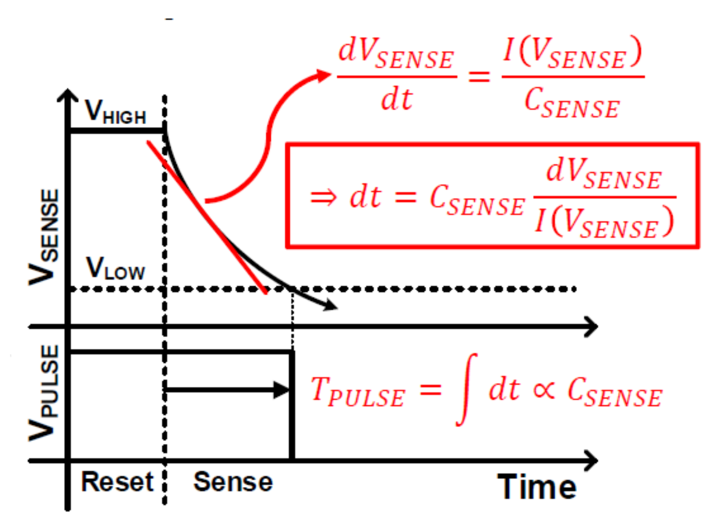

Figure 4 Linear behavior of the CDC [8]

The next step is to replace the load by a ring oscillator. In this way, the charge is reused and power is saved. The output of the ring oscillator is used to clock the comparator. Then the clocked output of the comparator can be used to drive the counter, which is shown in figure 5. This approach makes the system to work in discrete time domain. A sample and hold function is applied on it. So, it is still linear according to the previous expressions.

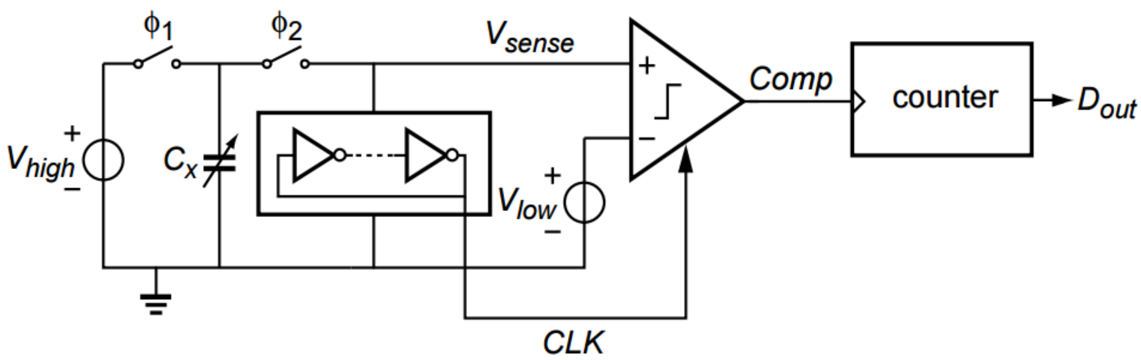

Figure 5 Replace the load by a ring oscillator [8]

However, the discrete-time comparator based system is still not completely digital. To further digitize the system, the voltage domain information is mapped into time domain and a time-domain comparator is used. Inverters (delay chain) are used to convert the time domain information from the voltage domain. And then the voltage comparator can be replaced by a time-domain comparator, which is simply a SR-latch. The time-domain system is shown in figure 6. Two delay chains are used here for V_{high} and V_{low}. This is the basic working principle of Michigan's Design.

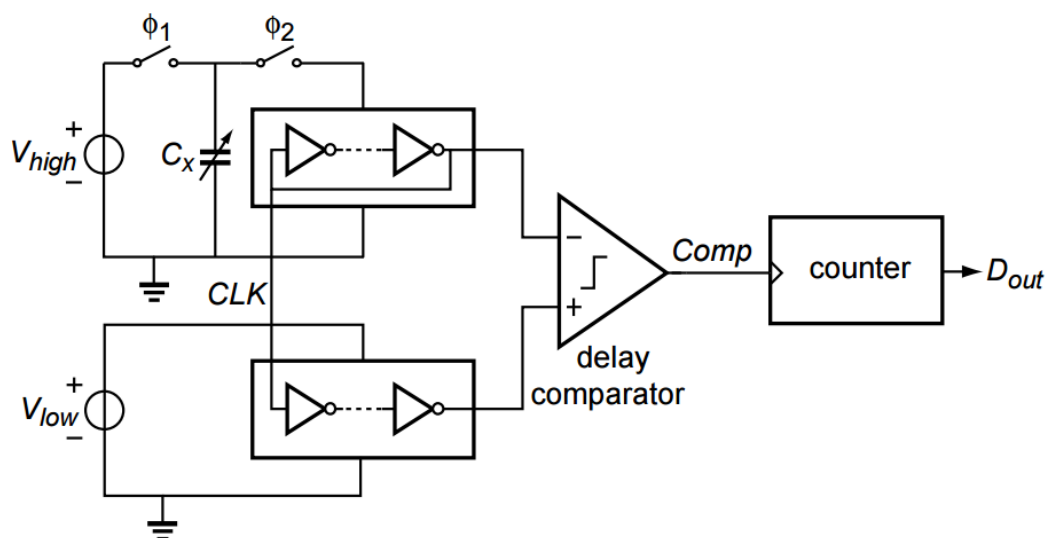

Figure 6 Time-domain system block diagram [1]

2.1.1 Performance limitation

The Michigan's design gives an appropriate solution to quantify very big capacitance. However, the discharge process is done through the parasitic capacitance, mainly coming from the gate source capacitance in the delay line. With that approach, the minimum capacitance resolution is determined by the parasitic capacitance. The process has a limitation on such parasitic capacitance. A better resolution can only be achieved by using newer technology. The improvement on the CDC is focussed on measuring capacitance with a better resolution.

2.1.2 Quantified analysis

The discharge process can be described by expression 2.4, which is basically a charge sharing process between $C_{load}$and C_x.

$$V_{low} = V_{high}\left(\frac{C_x}{C_x + C_{load}}\right)^n \tag{2.4}$$

WhereV_{low}, is the low voltage andV_{high}, is the high voltage, C_x is the sensor capacitor and $C_{load}$is the effective load capacitance for the delay chain, n is the number of clock cycles to discharge the voltage from $V_{high}$to V_{low},.

The value n can be represented by expression 2.5. n should be an integer number, so it is the minimum integer number larger than the calculated value.

$$n = \left\lceil \frac{In\left(\frac{V_{low}}{V_{high}}\right)}{In\left(\frac{C_x}{C_x + C_{load}}\right)} \right\rceil \tag{2.5}$$

The resolution of the Michigan's design can be defined as the minimum capacitor change in the sensor capacitor to make the number n increase by 1. Expression 2.4 can also be written as

$$\left(1 + \frac{C_{load}}{C_x}\right)^n = \frac{V_{high}}{V_{low}} \tag{2.6}$$

The resolution ΔC can be defined by the following two expressions.

$$\left(1 + \frac{C_{load}}{C_x}\right)^n = \frac{V_{high}}{V_{low}} \tag{2.7}$$

$$\left(1 + \frac{C_{load}}{C_x + \Delta C}\right)^{n+1} = \frac{V_{high}}{V_{low}} \tag{2.8}$$

Finally, the resolution is:

$$\Delta C = \frac{C_{load}}{\left(\frac{V_{high}}{V_{low}}\right)^{1/n+1} - 1} - \frac{C_{load}}{\left(\frac{V_{high}}{V_{low}}\right)^{1/n} - 1} \tag{2.9}$$

From expression 2.9, we can know that the ratio between the two voltages and C_x value is independent of the process, which means a higher resolution can only be achieved by using a better technology to reduce C_{load} without touching the voltages.

2.2 Improved architecture

2.2.1 Working principle introduction

The Michigan approach gives a good solution in terms of cost and technology migration. The following design aims at improving the resolution of the fully digital capacitance to digital converter.

The restriction of the previous design is the load capacitance, which is determined by the technology. This load capacitance determines the resolution, as the counter can only give integer numbers. To overcome this restriction, interpolation is applied at the edges of the crossing point. Figure 7 explains how it works.

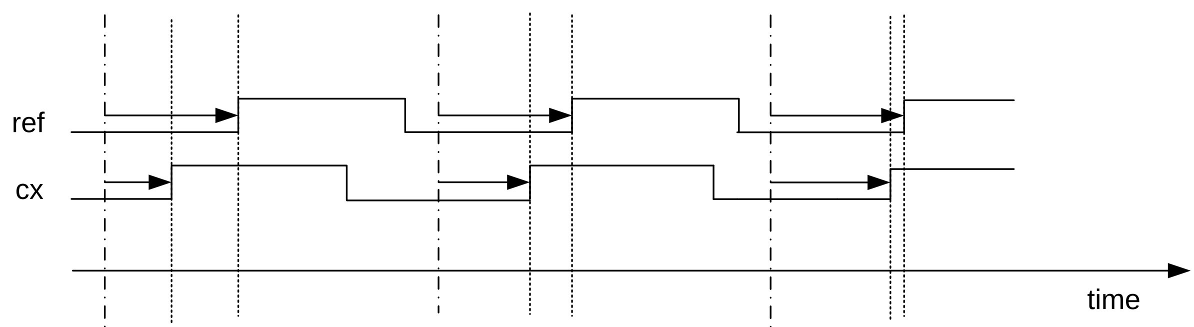

Figure 7 Waveform of working process

Each time, when the sensor capacitor is connected to the load, charge flows into the load capacitor. In this way, the supply voltage of the inverter goes lower as lower via iterative discharge process. As a result, the delay of the inverter is increased iteratively. So, in the waveform shown in figure 7, we can observe that the second rising edge of the sensor capacitor branch (cx) is shifted a step right relative to the rising edge of the reference branch (ref). This is the quantization step caused by the discharge process. With the discharge process, the edges will be closer and closer to each other. When the rising edge of the sensor capacitor branch comes after the one from the reference branch, the conversion is completed. And this gives a crossing point. Different sensor capacitor gives different relative distance at the crossing point. With only a counter, time of step-level shifting process cannot be measured at the end of the conversion. By using a TDC to quantify the time distance at the crossing point (shown in figure 8), we can do time domain interpolation.

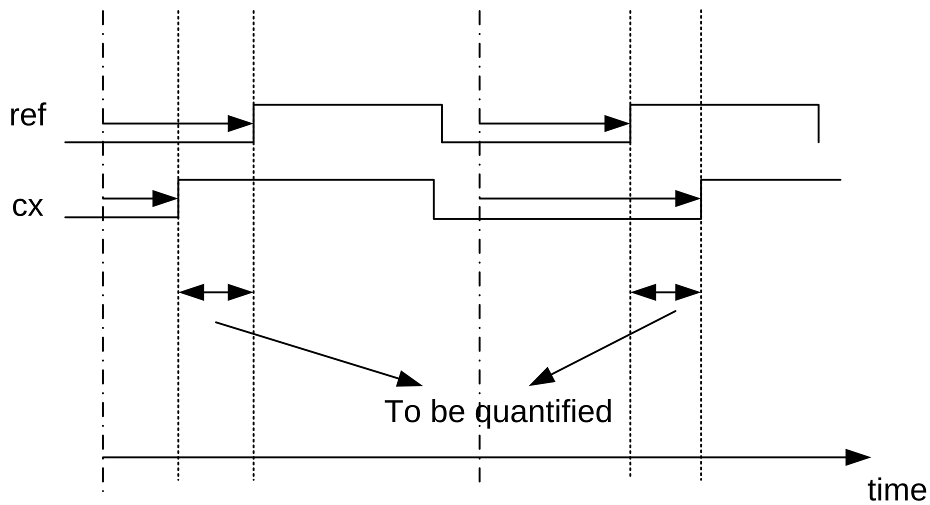

Figure 8 Time step to be quantified by TDC

However, having the TDC on during the whole conversion process is quite power hungry. The TDC only needs to be active at the crossing point and that is realized by using the early detection branch. When the delay of the signal branch is larger than the early detection branch (cx edge comes after the early edge), the TDC is on and starts measuring the time steps. Also, the early edge can be used as a common reference here, which helps to get rid of the influence of TDC offset. At this point, the time difference between reference branch and the cx branch is no longer directly measured. And the time differences between cx and the early edge, time difference a, and the reference and the early edge, time difference b, are measured. When the time difference between cx and the early edge is larger (a>b), the measurement is completed, shown in figure 9.

The early detection branch gives mismatch when the time differences are measured between this branch and two other branches (the reference branch and cx branch). So, the next step is to merge reference branch and cx branch together. So, the measurement is done in two phases by consecutively connecting cx and V_{ref} to the same inverter. The first operation phase measures the time difference between the reference branch and the early comparison branch. And after that, it is the measurement phase, which gives the final values. In figure 10, the architecture of the proposed CDC is shown.

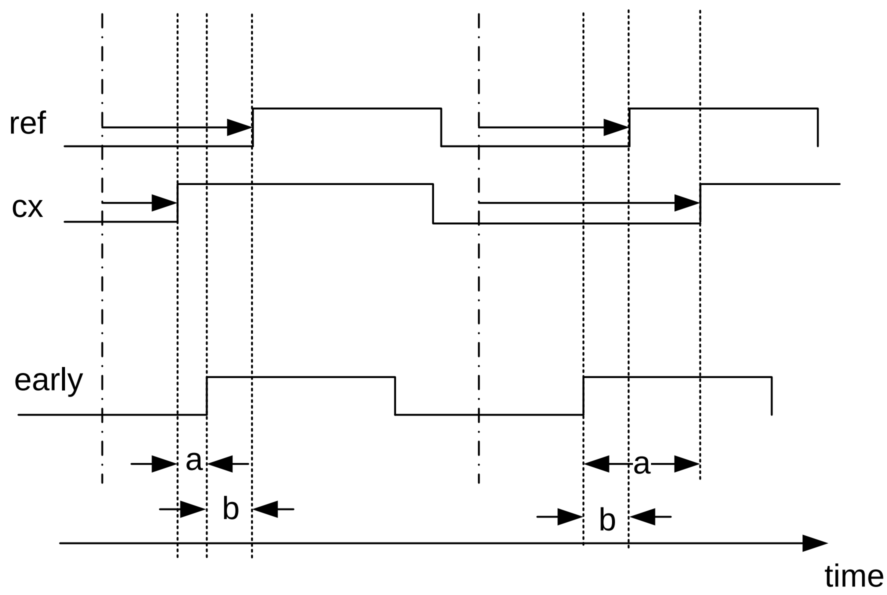

Figure 9 Early detection is used

2.2.2 Working process

The main idea here is to look at the relative location of the final edge compared with the reference edge. We are looking at where the signal edge is sitting relative to two reference edges. This is done by a TDC. As a result, the final output code is divided in two parts, the integer and the fraction. The integer number is given by the counter and the fractional part is calculated through the TDC output.

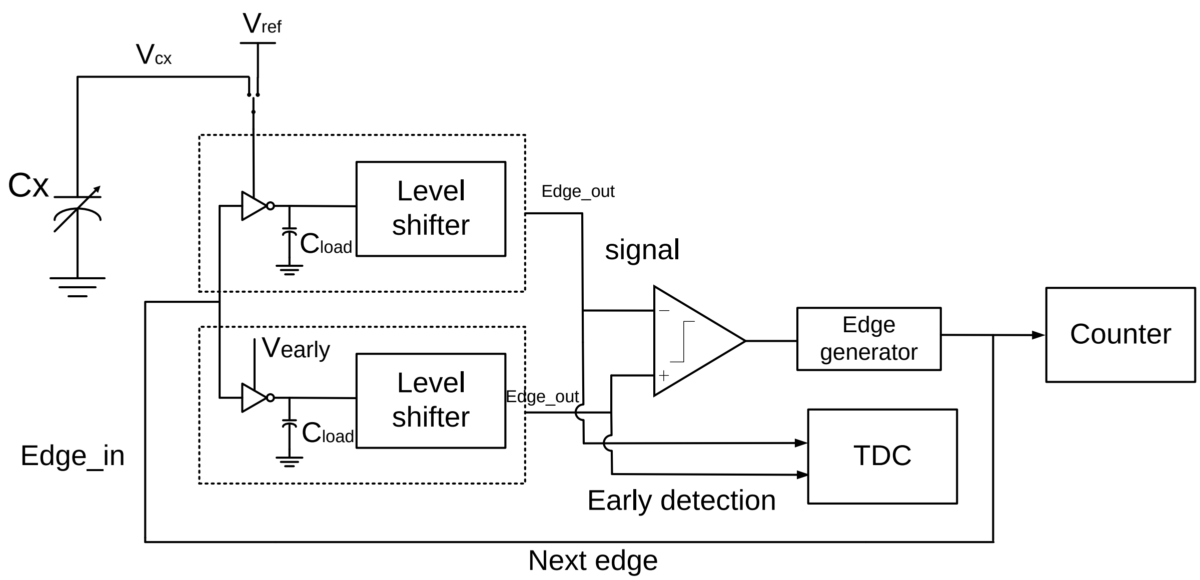

Figure 10 System architecture

In figure 10, the system diagram of the proposed design is given. It can be divided into the following parts: the inverter, which is used to discharge the sensor capacitor and generate the time domain signal; the level shifter, which is used to shift the voltage back to the 1.2 volt supply domain; the delay comparator(Delay CMP), which is used to compare the time difference; the edge generator, which is used to generate the edges for the discharge process; the counter, which is used to count the number of the cycles the sensor capacitor is discharged; the TDC, which is used for time interpolation.

The proposed CDC has two branches, the signal branch (for cx and ref function) and the early detection branch. In each branch, there is an inverter and a level shifter. The supply of the signal branch can be switched between the reference voltage, which is lower than the supply of the early detection branch, and the voltage across the sensor capacitor.

The operation process of the proposed CDC is divided into two phases, the calibration and the measurement phase, shown in figure 11. To make it easier for understanding, in figure 11 all the edge positions are relative to the reference edge. (Reference edge is periodical, so we can consider it is static in time domain)

In the calibration phase, the supply of the signal branch is connected to the reference voltage. The time difference of the reference (ref in figure 11) and the early detection branch will be measured (Out1 in figure 11) and used as the reference in the measurement phase. This is done by the TDC. Later, the measurement phase is started, with the decrease of the voltage across the sensor capacitor, the delay is also becoming larger and larger (cx in figure 11). The TDC will measure the time difference here. When the time difference is larger than the result from the measurement phase, the conversion is completed and the output data will be calculated.

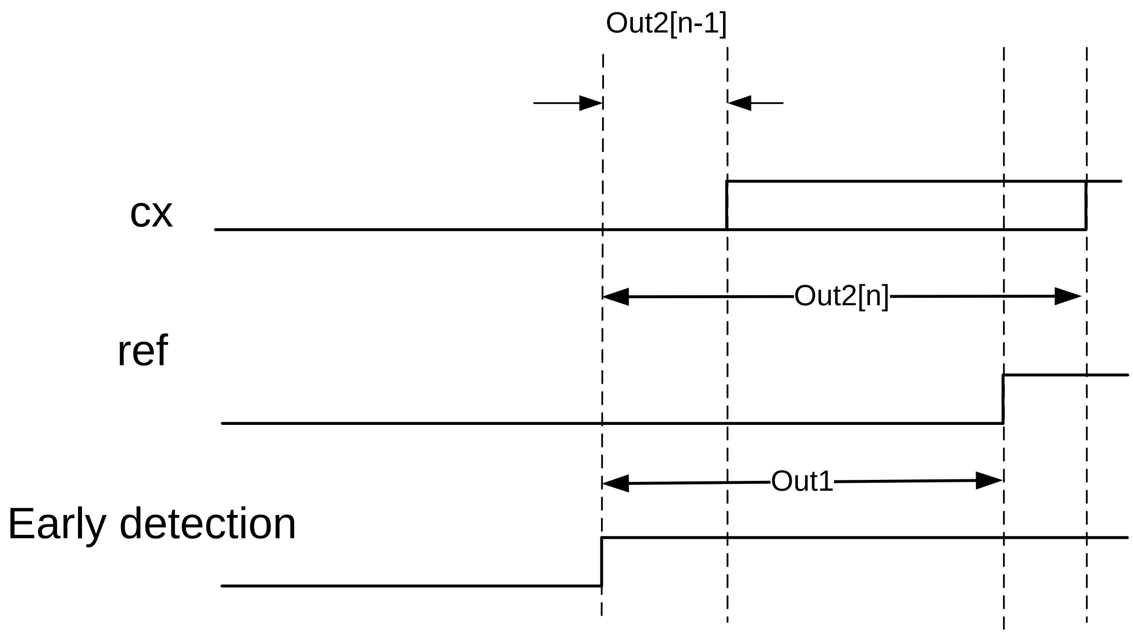

Figure 11 Operation process

The calculation has two parts, the calculation of the fractional part and the calculation of the final output code. For the fractional part, we want to know where the relative location of signal cx is according to the reference edge. The expression to calculate this final output code is shown in equation 2.10. The finally output is the sum of the fractional part and the number of the clock cycles which is used to discharge the voltage below the reference voltage.

$$fine\_code = \frac{out1 - out2[n-1]}{out2[n] - out2[n-1]} \tag{2.10}$$

In the expression, the early detection edge is used as a common reference signal, which is finally removed in the sustraction. The offset is also cancelled in this process. In the conversion process, a larger sensor capacitor will give a slightly higher voltage after the same amount of clock cycle. (We assume the same numbers in the counter.) This means that the delay of the signal branch is smaller, which will move the cx signal in figure 11 slightly to the left side. Then, according to the expression, a larger number will appear on the numerator. So, the fractional number is larger.

2.2.3 Signal to noise ratio

The signal-to-noise ratio of the fine conversion indicates how many times we can interpolate between the edges. Because of the jitters on the edges, the positions of the edges are not certain within some range. This is the noise here. The iterative discharge process generates change in the inverter delay, which is the signal here. The ratio between them is the signal-to-noise ratio, or interpolation factor, which tells us how many times we can interpolate.

Signal

In this interpolation method, the signal is defined by the time difference of two successive edges, which is the time step, and the noise is defined by the jitter of each edges. Here, for simplicity, we only analysis the SNR of the first stage, which is done by the single inverter, shown in figure 12.

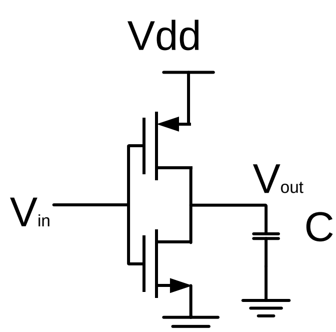

Figure 12 Inverter

The signal here can be recognized as the time step. The time step is caused by the voltage change of the iterative discharge process. Each time, when an edge appears at the input of the inverter, a certain amount of charge is removed from the sensor capacitor, resulting in a very tiny change in the supply voltage of the inverter which causes the change in the inverter delay. Here, we define half of the supply voltage as the point we are looking at, shown in figure 13. The time step is defined by the time difference in the rising edge of two successive voltages from the iterative discharge

In this design, the falling edge at the inverter input draws charges from the sensor capacitor, resulting in a rising edge at the output. And the rising edge at the input is used to clear the charge at the load capacitor. In the analysis of the SNR, only the rising edge at the output needs to be considered.

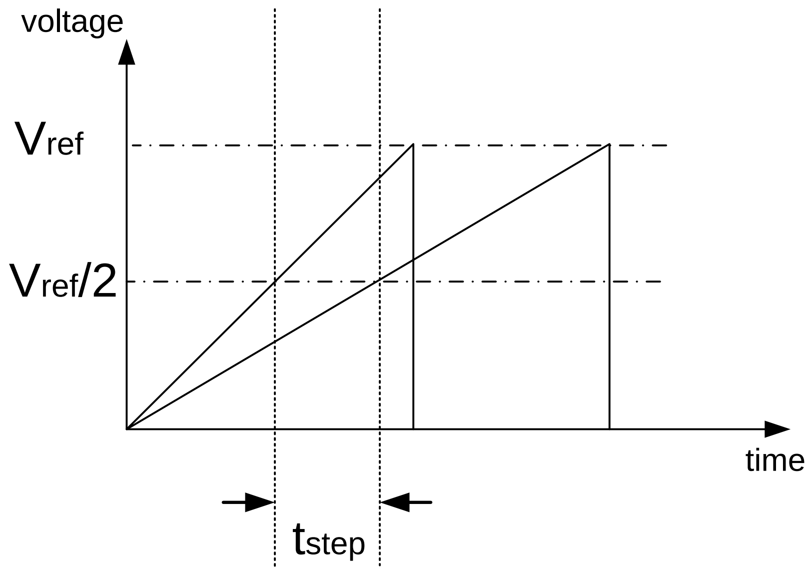

Figure 13 The time step is defined by the time difference in the rising edge of two successive voltages from the iterative discharge

The rising time of the edge at the output can be defined as the following.

$$t_p = \frac{C_L V_{ref}}{2I_{ds}} \tag{2.11}$$

By doing a differential calculation we can get the time step which is caused by the tiny change of the supply.

$$t_{step} = \frac{d(t_p)}{d(I_{ds})} g_m \Delta V = \frac{V_{ref} C_L}{2{I_{ds}}^2} g_m \Delta V = \frac{V_{ref} C_L}{2{I_{ds}}^2} g_m \frac{C_L}{C_X} V_{ref} \tag{2.12}$$

Where g_m is the transconductance of the MOSFET, V_{ref} is the reference supply, C_L is the load capacitor, I_{ds} is the drain current and Cx is the sensor capacitor. And this is the signal we will use in the later calculation.

Inverter jitter [9]

The inverter jitter can be understood as the integration of the noise current on the capacitor. This noise current causes the variation of the crossing time which finally gives the jitter. Figure 14 [9] shows how noise turns into jitter. The slope is the rising edge of the inverter. Due to the noise, the threshold voltage crossing point is changing up and down due to the noise integration on the inverter output capacitor, which makes the crossing time of each edge different. That's the cause of the jitter.

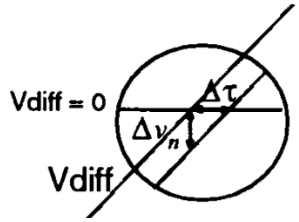

Figure 14 Cause of the jitter [9]

So, we can express the integrated noise by expression 2.13:

$$v_n(t) = \frac{1}{C_L}\int_0^{t_p} i_n dt \tag{2.13}$$

t_p is the rising time, which defines the upper limit of the integration. $C_L$is the load capacitor and $i_n$is the noise current. The integration can be expressed by a convolution. w_{tp} is a rectangular unit window with a width of t_p

$$v_n(t) = \frac{1}{C_L}\int_0^{\infty} i_n(x) \times w_{tp}(t-x)dt \tag{2.14}$$

In frequency domain, in terms of power spectral density:

$$S_{vn}(f) = \frac{1}{C_L{}^2} S_{in}(f)\,|W_{tp}(f)|^2 \tag{2.15}$$

The Laplace transform of a rectangular window:

$$W_{tp}(s) = \frac{1-e^{-st_p}}{s} = \frac{\sin(wt_p/2)}{wt_p/2} e^{-jwt_p s} \tag{2.16}$$

$$|W_{tp}(s)| = t_p \frac{\sin(\pi f t_p t)}{\pi f t_p} \tag{2.17}$$

So, the integrated voltage noise is:

$$v_n{}^2 = \int_0^{\infty} S_{vn}(f)df = \frac{1}{C_L{}^2}\int_0^{\infty} S_{in}(f)\,|W_{tp}(f)|^2 df \tag{2.18}$$

$$S_{in} = 4kT\gamma g_m \tag{2.19}$$

So, we can calculate the final noise voltage of the large signal behaviour:

$$v_n{}^2 = \frac{S_{in}}{2C_L{}^2} t_p = \frac{2kT\gamma g_m}{C_L{}^2} t_p \tag{2.20}$$

The jitter is the value of the noise divided by the slope, which is $slope = \frac{I_{ds}}{C_L}$

So, the jitter value is:

$$\sigma^2 = \frac{4kT\gamma t_p}{I_{ds}(V_{DD} - V_{th})} = \frac{2kT\gamma C_L V_{ref}}{I_{ds}{}^2 (V_{DD} - V_{th})} \tag{2.21}$$

Signal-to-noise ratio

After that, we can calculate the signal-to-noise ratio, which is

$$SNR = \frac{V_{ref} C_L \frac{g_m}{2I_{ds}{}^2} \Delta V}{2\sqrt{\frac{4kT\gamma g_m t_p}{2I_{ds}{}^2}}} = \frac{V_{ref}}{4\sqrt{kT\gamma / C_L}} \frac{C_L}{C_X} \sqrt{\frac{g_m}{I_{ds}} V_{ref}} \tag{2.22}$$

The jitters in the calibration phase do not dominate since they can be reduced by using multiple edges. So, finally, the TDC measurements before and after the crossing point are involved in the calculation. There are 4 edges in total. So, the jitter on the denominator should be multiplied by 4.

The final resolution can be estimated by expression 2.23. The final resolution is estimated by dividing the load capacitanceC_L by the SNR ratio, which defines the full scale of the fine conversion, by this SNR.

$$C_{final} = \frac{C_L}{\frac{V_{ref}}{4\sqrt{kT\gamma / C_L}} \frac{C_L}{C_X} \sqrt{\frac{g_m}{I_{ds}} V_{ref}}} = \frac{4\sqrt{kT\gamma / C_L}\, C_X}{V_{ref} \sqrt{\frac{g_m}{I_{ds}} V_{ref}}} \tag{2.23}$$

For example,If V_{ref}=0.65V, C_L=30fF, C_x=8pF, g_m/I_{ds}=10~20, we use 20 here, γ=1

We get a signal-to-noise ratio of 6, which means the interpolation factor is around 6, which further divides the LSB by 6. So, for this example, the equivalent load capacitor is 5fF. A higher resolution is achieved.

2.3 Conclusion

In this chapter, a working principle of Michigan's design is reviewed. The analysis on Michigan's design reveals its performance limitation, which is determined by the load capacitor. To break the limitation from the load capacitor, an interpolation based method is proposed. And analysis is done on its signal noise ratio. And a higher resolution can be achieved.

3. Circuit level design

In this chapter, the detailed schematic design of the main functional blocks in the system will be discussed. The blocks include the inverter and level shifter stage, the delay comparator, the edge generator, the counter and the time-to-digital converter (TDC). The layout of the custom design (TDC and inverter and level shifter stage) will be given. Simulation across different corners will be given on the TDC block. The layout of the digital logic has been done by automatic placement and routing. The technology used for the design is 0.16µm CMOS process.

3.1 Inverter and level shifter stage

The inverter and the level shifter stage is the block at the input. This block can be divided into two parts: the inverter and the level shifter, shown in figure 15. The inverter is used to discharge the sensor capacitor and generate the time domain delay signal based on the voltage of the sensor capacitor. In figure 15, the inverter stage (cells in the box) consists of M1, M2 andC_{load}. The inverter supply of the signal branch is connected to the sensor. The bulk of M1 is connected to supply for a higher threshold voltage. A small capacitor charge current can be achieved by doing this. As a result, the voltage across C_{load} is increasing slowly and a sufficiently large time step for the TDC to measure can be obtained by doing this.

Due to the decrease of the supply voltage, the output level of the inverter will also decrease, which could make the following transistors, not work in on/off mode. The level shifter is used to provide a buffer between them and move the voltage back to the chip supply domain. In figure 15, the transistors M3 to M6 form the level shifter stage.

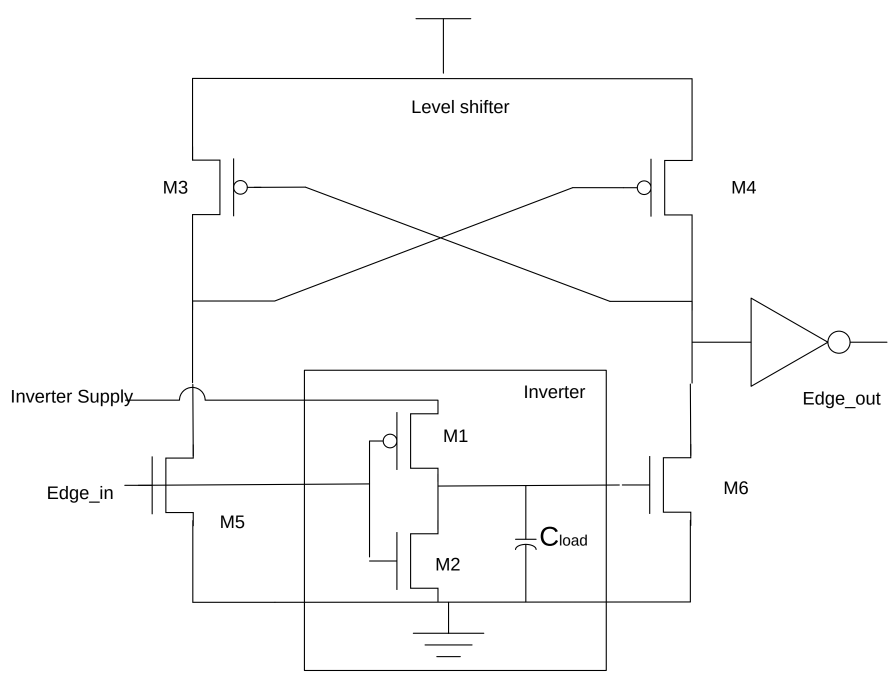

Figure 15 Inverter and level shifter stage

There are two such blocks in the system: one serves the early detection branch and the other as the signal branch. The connections between them and the supplies are shown in figure 16. In the early detection branch, the supply of the inverter is connected to an early detection voltage. In the signal branch, the supply of the inverter can be switched between the reference voltage V_{ref} and the voltage across the sensor capacitorV_x. The outputs of the level shifters are connected to the delay comparator. M1 is used to charge the sensor capacitor. M2, M3 and INV are the part to select the supply of the inverter of signal branch. SW is the selection signal.

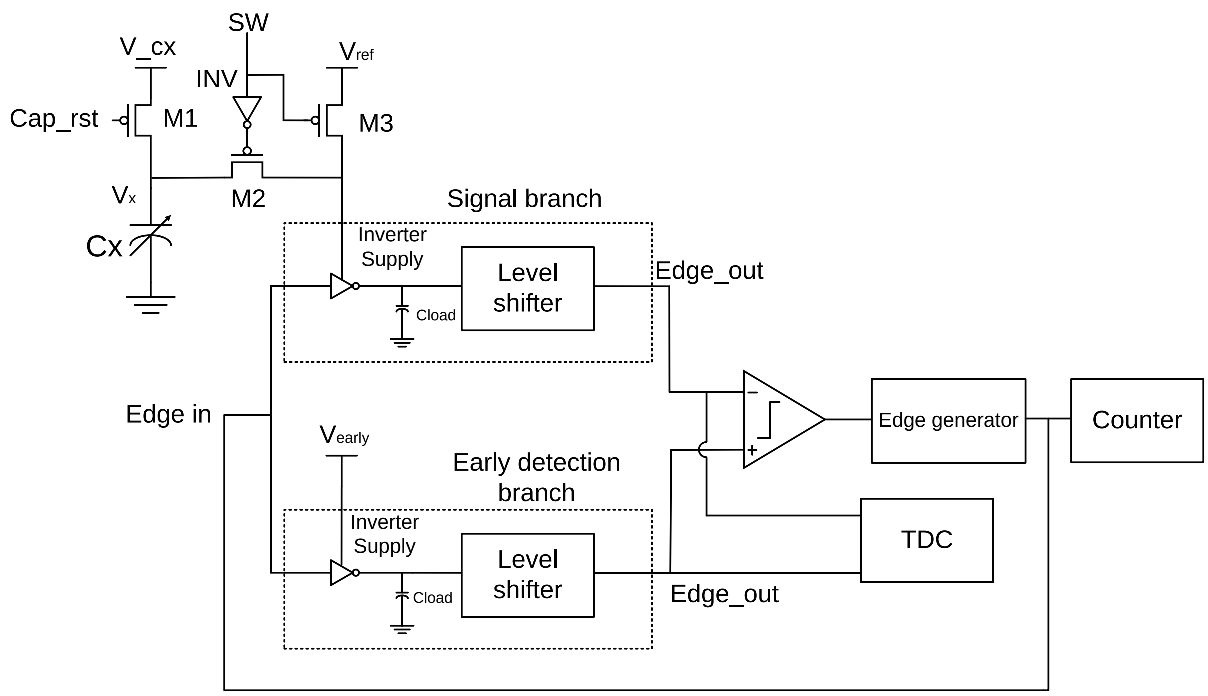

Figure 16 Connections between blocks

Device Sizing:

Inverter and load capacitor:

As derived in expression 2.22, the signal-to-noise ratio (SNR) of the fine conversion is:

$$SNR = \frac{V_{ref}}{4\sqrt{kT\gamma / C_L}} \frac{C_L}{C_X} \sqrt{\frac{g_m}{I_{ds}} V_{ref}} \tag{2.22}$$

The final capacitance resolution is derived in 2.23. Here, we write it again.

$$C_{final} = \frac{C_L}{\frac{V_{ref}}{4\sqrt{kT\gamma / C_L}} \frac{C_L}{C_X} \sqrt{\frac{g_m}{I_{ds}} V_{ref}}} = \frac{4\sqrt{kT\gamma / C_L} \bullet C_X}{V_{ref} \bullet \sqrt{\frac{g_m}{I_{ds}} V_{ref}}} \tag{2.23}$$

The size of the transistor and the sizing of the load capacitor are mainly designed based on expression 2.23 and the time step and jitter expressions 2.12 and 2.21 derived in section 2.

In figure 15, the NMOS (M2) of the inverter has its minimum size. It is only used to discharge the load capacitor. For the PMOS (M1), according to the expression 2.23, the final resolution has nothing to do with the length of the PMOS. The PMOS size mainly contributes to the absolute value of the jitter and the time step, which directly links it to the TDC design. With a small jitter, there is a smaller time step, which means the TDC has to have a high resolution and is harder to implement. A big jitter gives bigger time step, which relaxes the TDC design. But the jitter should not be much bigger than the TDC resolution; otherwise the TDC will be over designed.

From the expressions 2.23, a larger load capacitor is beneficial to the final resolution. But a larger load capacitor gives a larger absolute jitter value. In consequence, the upper limit of the load capacitor is determined by the jitter level and the TDC resolution. Finally, according to the designed TDC resolution, a 30fF capacitor is used as the load and the PMOS size is 0.768/0.4. In the layout, a fringe capacitor is used and it gives a capacitance of 32fF.The supply of the signal branch is 0.65V. In simulation, the supply of the early detection branch is 0.8V.

Level shifter:

For the size of the NMOS (M5 and M6 in figure 15), it should not make the level shifter dominate the jitter level, which means a sharp edge and a wide NMOS. But the width of the NMOS is related to kickback, which means a small NMOS is beneficial. As a compromise, the size of the NMOS is 4/0.16. The size of the PMOS is 0.768/0.5.

Layout:

Figure 17 shows the layout of this block.

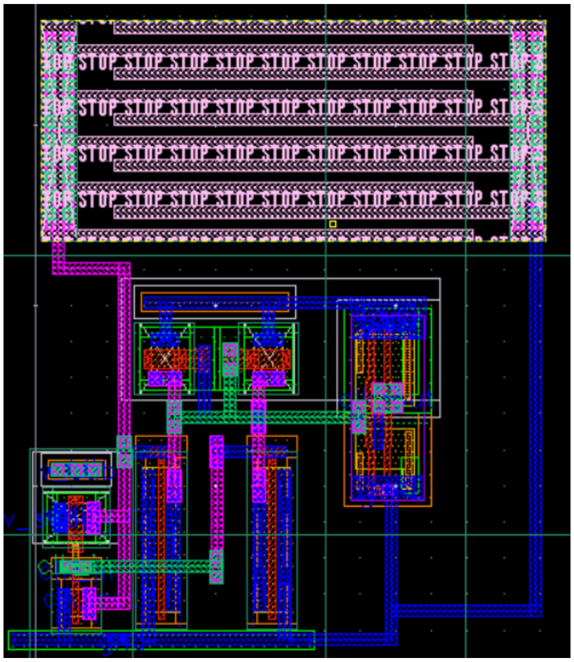

Figure 17 The layout of the inverter and level-shifter stage

3.2 Delay comparator

The delay comparator, or the time domain comparator, is the cell used to detect which edge comes first from the previous stages. It is shown in figure 18.

The delay comparator can be considered as a SR latch. When the inputs of the two nand gates are 0, both nand gates are disabled and the logic level at node a and node b are 1. So, the final outputs we get are: cmp_p=0, cmp_n=0.

When rising edge at the input 'fast' comes first, the input of the 'nand 1 is 1'. The other input of nand 1 is 1 due to the feedback. So, the value saved at node a is 0. Also, though the feedback path, the input of nand 2 is set to 0 from 1, which means that the nand is no longer sensitive to a rising edge at input 'slow'. So, finally, when a rising edge comes at input slow, through the cross-coupled structure, we get cmp_p=1, cmp_n=0.

When 'slow' is faster, the situation is similar, and we get cmp_n=1, cmp_p=0.

The outputs are gated so that both outputs are kept 0, when the comparator is reset by the falling edge. The buffer in cross coupled structure here is used to prevent glitch.

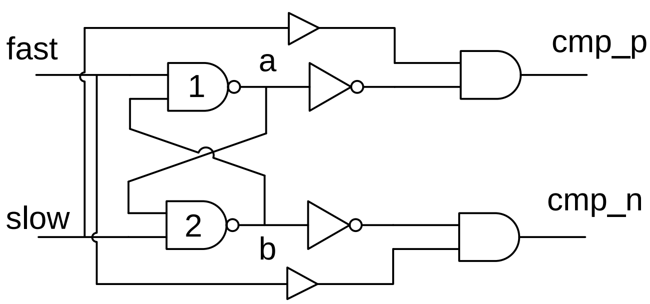

Figure 18 Delay comparator

Figure 19 shows a transient simulation result that illustrates this operation. The signal names are labelled in the figure.

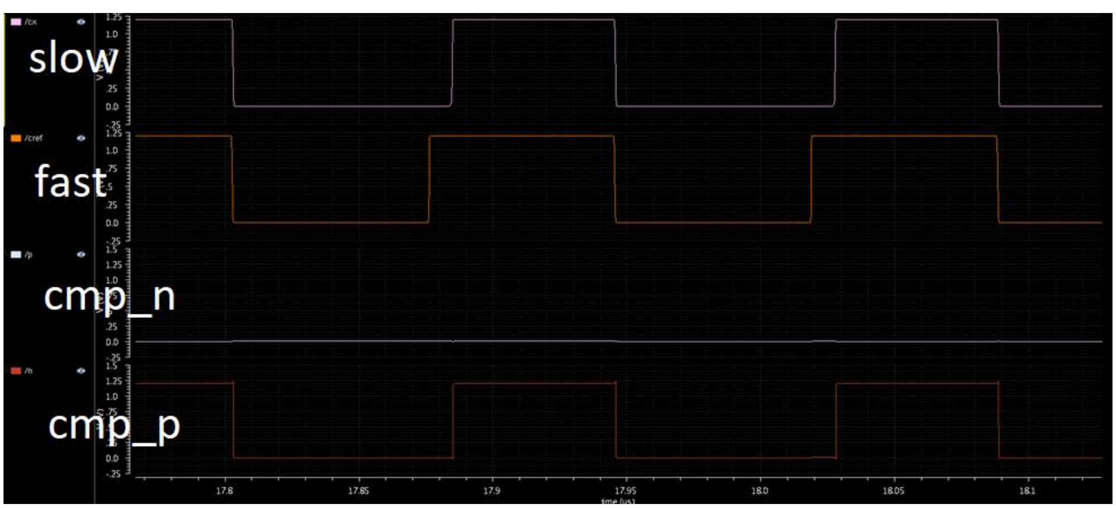

Figure 19 simulation of delay comparator

3.3 Edge generator

After each discharge cycle is completed, a new edge is needed to trigger a new discharge process. Such edges can be generated by an external clock. However, it is more elegant to make it a self-clocked system. The edge generator is such a block, which is used to generate the edges that are used to keep the self-clock system working. Basically, it is a cell toggling its output between 0 and 1, depending on its control signal.

The state machine of the edge generator has two states. The state 0 gives an output of 0 and the state 1 gives the output of 1. The stage machine can be considered as a SR-latch, which the output is controlled by set and reset signal. The set and reset signal are generated based on the outputs of the comparator, the TDC conversion finish signal (tdc_conv_fin) and the clock control signal.

The core of the state machine is shown in figure 20. When set=1 and reset=0, the output q goes from 0 to 1. When reset=1 and set=0, it goes from 1 to 0.

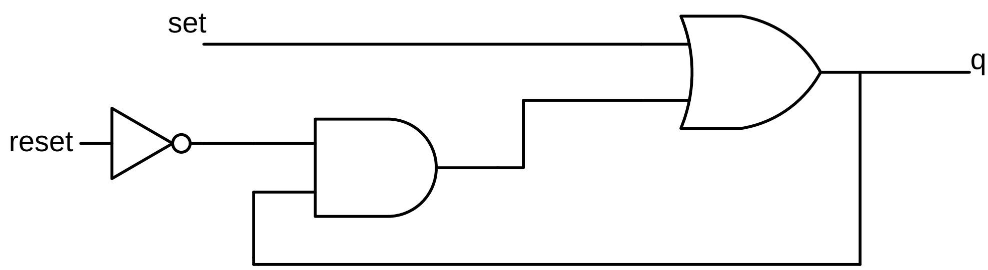

Figure 20 Core of the edge generator machine

In the state machine shown in figure 21, cmp_p, cmp_n are the outputs of the delay comparator; tdc_conv_fin is the signal to detect the tdc conversion completion; the clk_ctr is the on/off chip clock selection signal.

The generation of the set and the reset signal can be described by the following expressions.

$$set = (cmp\_p + cmp\_n) \bullet tdc\_conv\_fin \bullet clk\_ctr \tag{3.1}$$

$$reset = \overline{(cmp\_p + cmp\_n)} \bullet tdc\_conv\_fin \bullet clk\_ctr \tag{3.2}$$

From the expressions 3.1 and 3.2, we can know there are only two combination situations for set and reset signals: set=1, reset=0 and set=0, reset=1.

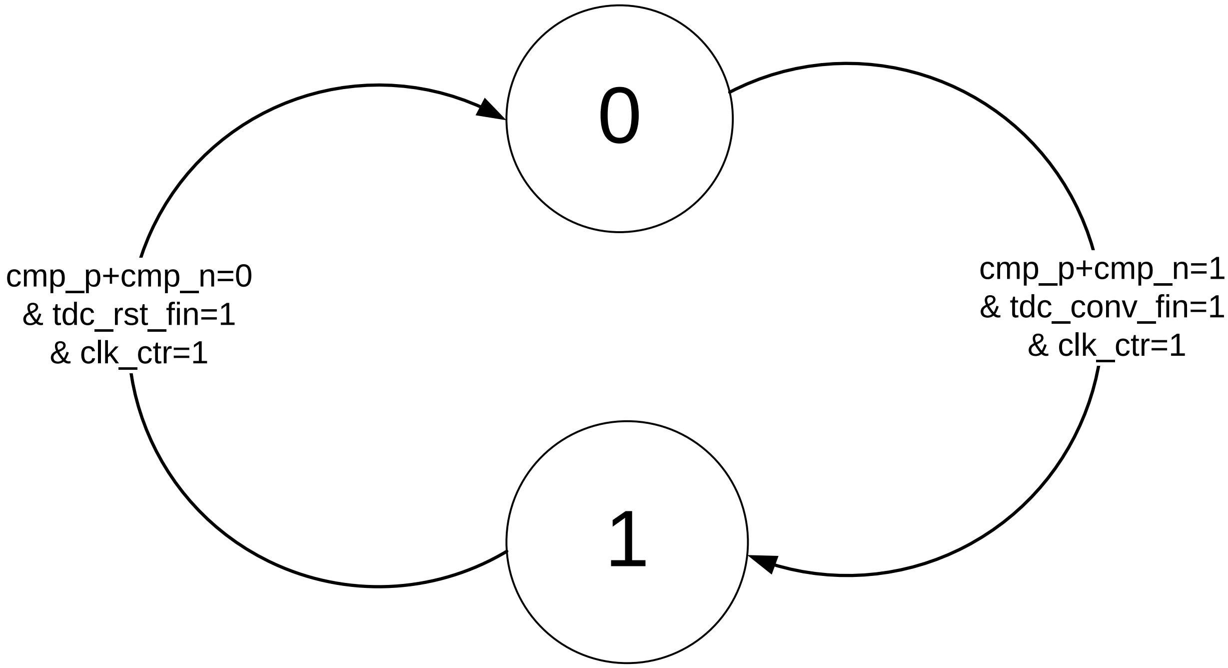

Figure 21 State machine diagram of the edge generator

The schematic implementation of the state machine is shown in figure 22. To prevent that the next edge is generated before completion of the charge transfer from $C_x$to C_L, a delay element is placed at its output, which gives a 70ns delay on rising edge and 20ns delay on falling edge.

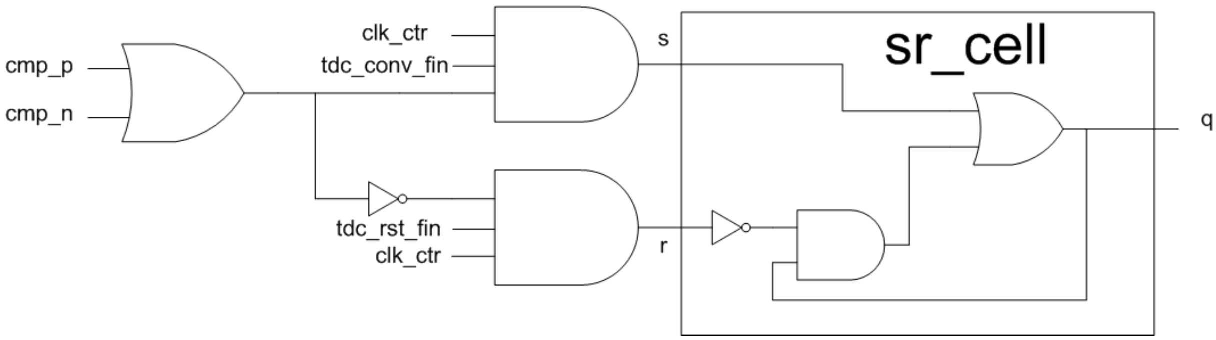

Figure 22 Schematic implementation of the state machine

3.4 Counter

The counter is an asynchronous counter, shown in figure 23. It has 10 bits.

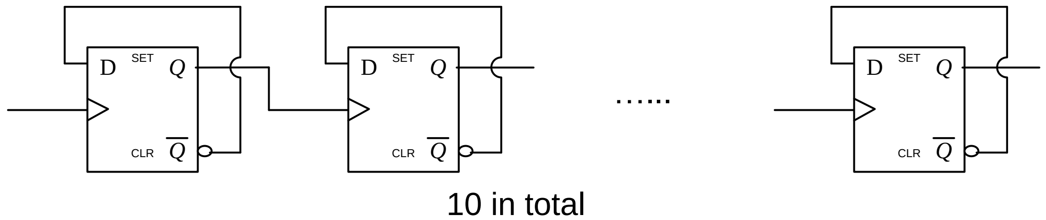

Figure 23 10-bit counter

3.5 Time-to-digital converter

3.5.1 TDC architecture

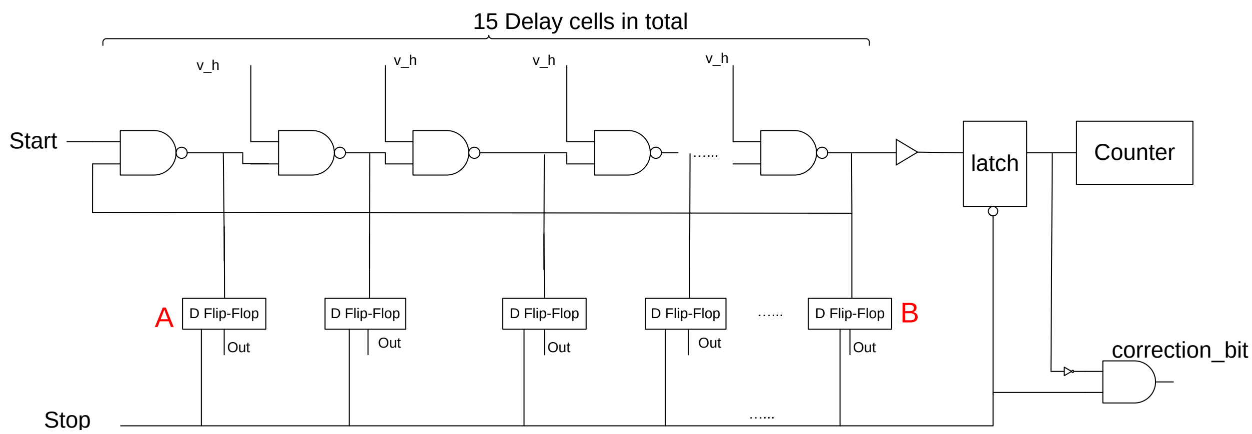

Figure 24 TDC architecture

The TDC is a coarse-fine TDC. The coarse conversion is done through the counter and the fine conversion is done through the ring oscillator. The coarse conversion is done through a 5-bit asynchronous counter, which is shown in figure 24. It is only sensitive to rising edges. The counter clock is the output of the ring oscillator, which serves as the fine TDC. The ring oscillator has 15 stages; each stage is implemented by a nand gate with a delay of 70ps, which makes the input of the counter less then 500MHz. One input of the nand gate is tied to the supply. To give a balanced delay in each stage, the PMOS and NMOS of the nand are a custom design. The size of the PMOS is 4.904/0.16, fold=4. The size of the NMOS is 0.768/0.16.

The ring oscillator is triggered by a rising edge at the input 'start'. The stop signal, which is also a rising edge, will be applied through input 'stop'. At the beginning, the first nand in the ring oscillator is disabled because of a low voltage level at the start input.

When a rising edge comes at the input, both inputs of the first nand are at high level. Then, it starts oscillating. The voltage level at each node inside will be toggled to its opposite value one after another. So, the pattern double 0 or double 1 determines the location of the time incident. When a stop signal comes, the D-Flip-flops (DFF) sample the nodes in the ring oscillator. The data in the ring oscillator is saved in the DFF and the pattern of double 0 and double 1 is where the signal is in the ring oscillator.

The decoder which will be discussed in detailed later will process the data from the ring oscillator to obtain a binary code from the fine TDC. The coarse TDC output is basically the output of the counter, since there are 15 delay cells and the counter is only sensitive to rising edges, the code in the counter has a radix of 30.

The latch at the output of the ring oscillator is used to regenerate the clock signal to the counter, which helps to solve the code error at the transition point. This will be discussed in this section later.

3.5.2 TDC decoder

The decoder of the TDC can be divided into three parts, the pattern detector, the one-hot code to binary code converter and a 4-bit adder.

Firstly, the location of double 0 and double 1 needs to be detected. This is done by means of detecting double 0 or double 1 through XOR gate. An OR gate is used to detect the output of the last and the first DFF, since at these two nodes, only double 0 needs to be detected. Double 1 at this node means a carry in the counter. Figure 25 shows the detector.

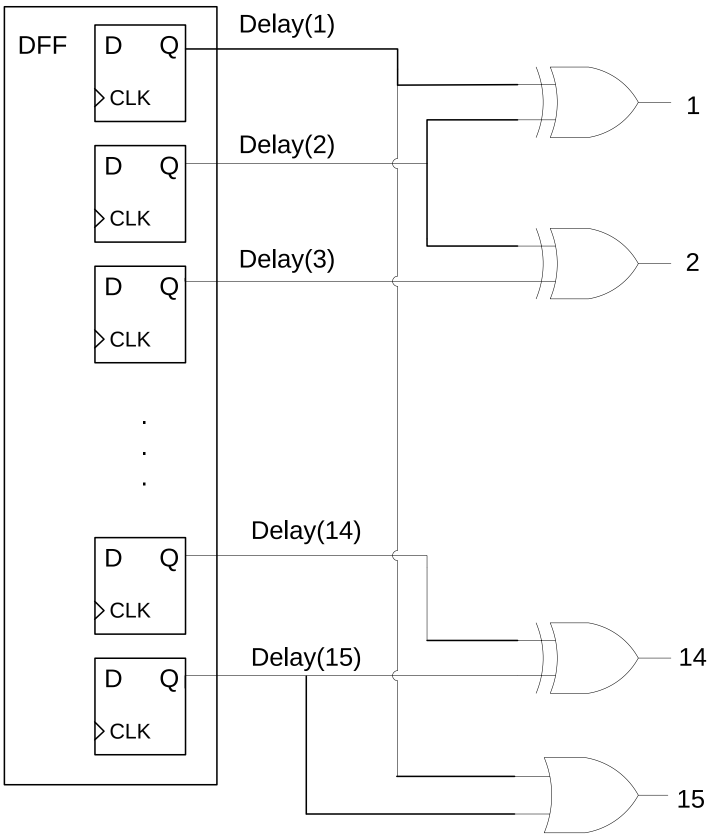

Figure 25 Detector

The output code of the detector is an inverted one-hot code, where 0 indicates the location of the signal.

The decoder for this inverted one-hot code to a binary code is based on the following expressions [10]. Figure 26 shows corresponding implementation.

$$B4=\overline{8}+\overline{9}+\overline{10}+\overline{11}+\overline{12}+\overline{13}+\overline{14}+\overline{15} \tag{3.3}$$

$$B3=\overline{4}+\overline{5}+\overline{6}+\overline{7}+\overline{12}+\overline{13}+\overline{14}+\overline{15} \tag{3.4}$$

$$B2=\overline{2}+\overline{3}+\overline{6}+\overline{7}+\overline{10}+\overline{11}+\overline{14}+\overline{15} \tag{3.5}$$

$$B1=\overline{1}+\overline{3}+\overline{5}+\overline{7}+\overline{9}+\overline{11}+\overline{13}+\overline{15} \tag{3.6}$$

By doing logic simplification, the following decoder can be obtained. Expression 3.7 is a simplification example for expression 3.3.

$$B1=\overline{\overline{\overline{1\bullet 3}+\overline{5\bullet 7}}\bullet\overline{\overline{9\bullet 11}+\overline{13\bullet 15}}}=\overline{\overline{\bar{1}+\bar{3}+\bar{5}+\bar{7}}\bullet\overline{\bar{9}+\overline{11}+\overline{13}+\overline{15}}}=\overline{1\bullet 3\bullet 5\bullet 7\bullet 9\bullet 11\bullet 13\bullet 15}$$
$$=\bar{1}+\bar{3}+\bar{5}+\bar{7}+\bar{9}+\overline{11}+\overline{13}+\overline{15} \tag{3.7}$$

As the counter is only sensitive to the rising edges and one rising edge means that the signal has travelled two cycles in the loop, we need to figure out whether the signal has travelled an odd or even number of cycles. Based on the value in the DFFs marked A and B in figure 24, this can be found out. If $A \times \bar{B} = 1$, the signal has travelled two cycles in the loop and the binary number 1110 will be added to the output via a 4-bit adder. The 4-bit adder is implemented by one 1-bit half adder (low bit) and three 1-bit full adders (high bits).

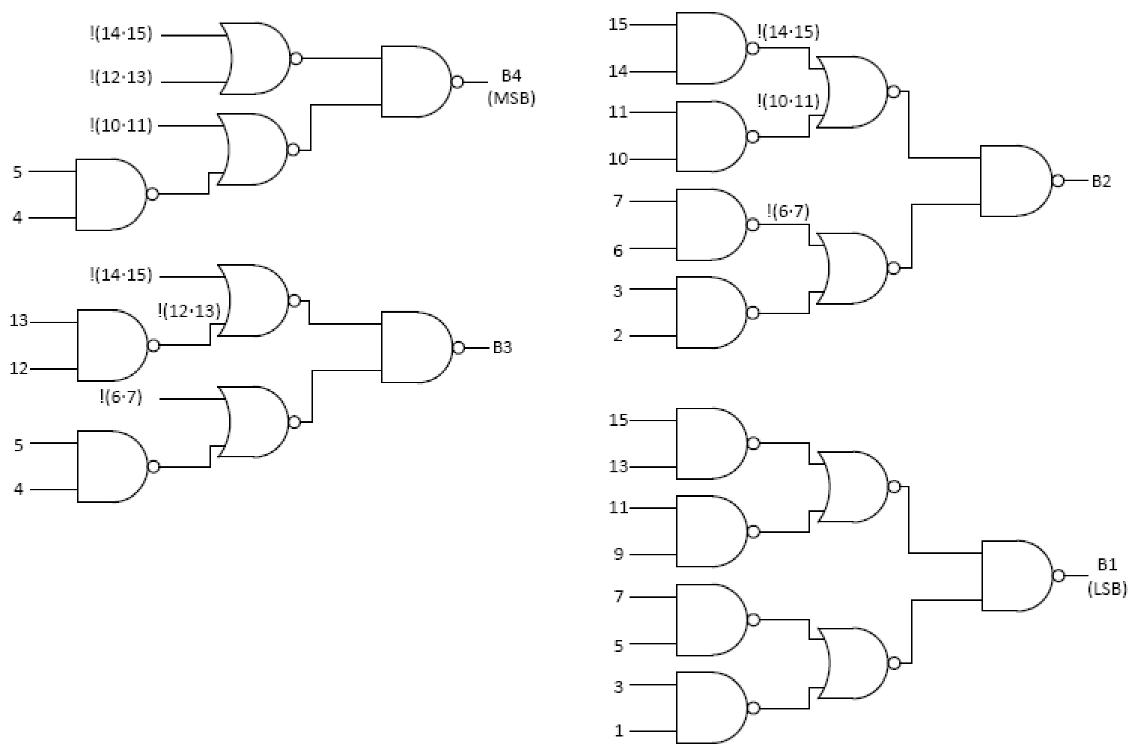

Figure 26 One-hot code to binary code decoder [10]

3.5.3 TDC correction

The TDC outputs can be divided into the coarse code from the counter and the fine code from the DFFs. But the counter and the DFFs are in different clock domains, they are asynchronous. The counter is driven by the ring oscillator output, while the clock of the DFF comes from the stop event, which means there is no guarantee to stop the counter and the ring oscillator at the same time.

The counter can be disabled if the timing event in the loop is far away from the counter. But when the timing event is very close the counter, the appropriate control signal for the counter cannot be generated at the correct time. The counter will either counts more or less, which causes non-monotonic issues at the transition points (shown in figure 27).

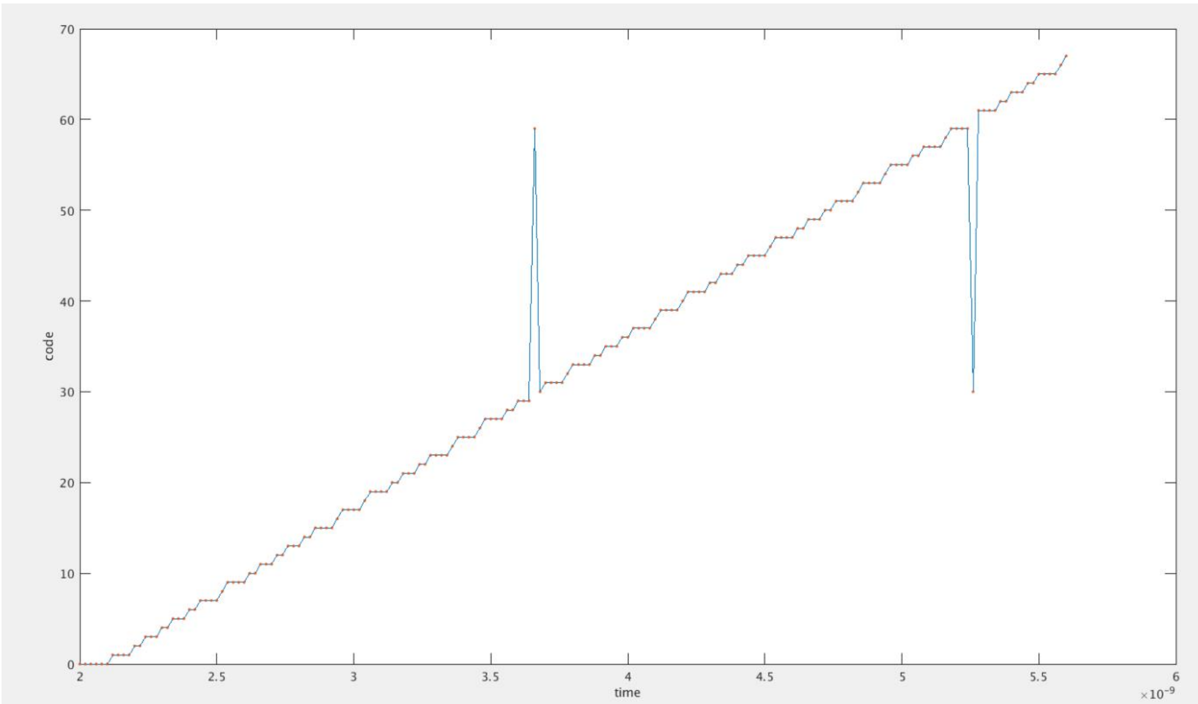

Figure 27 Non-monotonic behavior caused by the asynchronous behavior

To solve the problem, the counter is triggered slightly later by delaying its input and gating the clock with a latch. When a start signal appears at the input of the ring oscillator, the oscillator starts working and generating pulses for the counter. Also, the time event is travelling in a clockwise manner in the loop of the ring oscillator (Figure 24). Later, a stop signal comes. At this moment, let's assume that the time event is in the region where the counter cannot be stopped reliably without a delayed counter input. With the latch, the counter input status can be tracked. Also, the undesired pulse from the ring oscillator cannot enter the counter with a delayed counter input. Then, the problem can be solved. Extra delay is added before the latch to make it robust across corners. So, the code is always smaller than its original value at the transition point.

The next step is that we need to fix that pattern. Here, the latch in front of the counter is used. This latch is transparent when the TDC is operating. When the stop signal comes at the transition point, the data in the latch is saved. When the value in the latch is 0 and the value in DFF B is 1, the location of the time signal is in the nodes after DFF A. So, the counter value should be added by 1. A correction bit will be generated. Figure 28 shows how this works. For simplicity, a 3-stage ring oscillator is used.

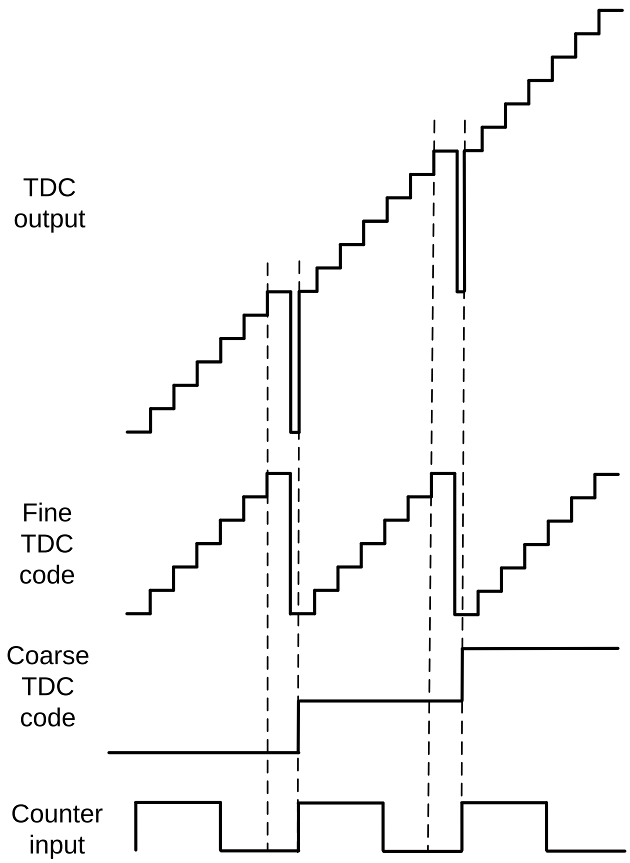

Figure 28 TDC correction example with a 3-stage ring oscillator

Post-layout simulation shows that a glitch may appear at the input of the counter due to the latch set up failure (shown in the red cycle in figure 29). This spike will make the counter number increase by one. A 20fF capacitor is applied at the output of the latch to filter out the glitch.

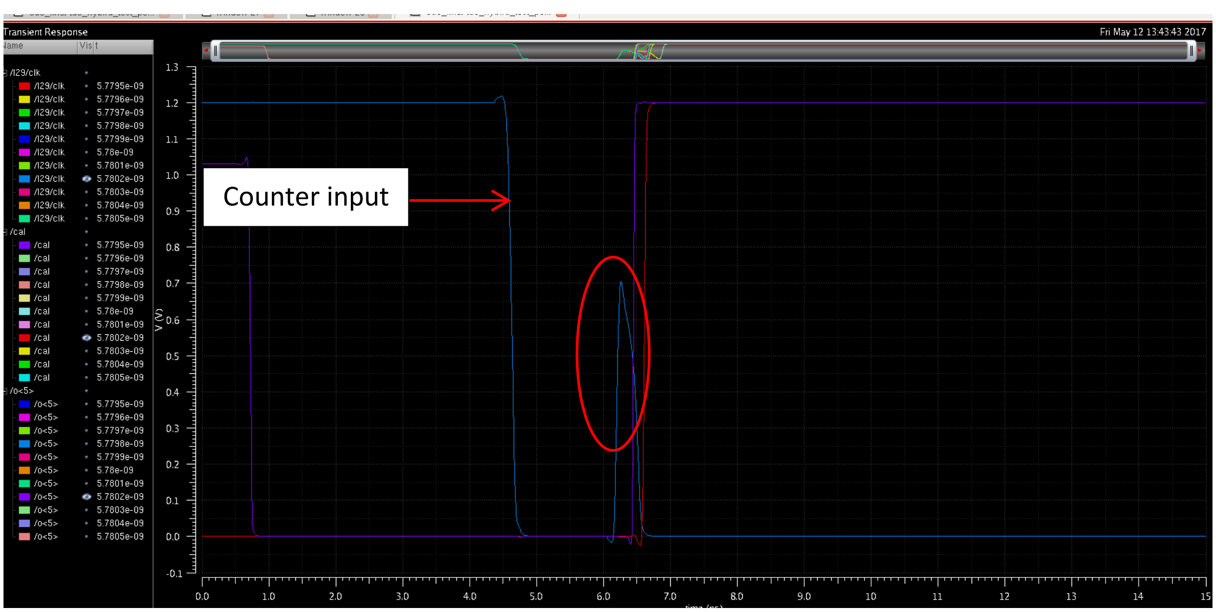

Figure 29 Post-layout simulation result with a glith

3.5.4 TDC trigger

The TDC trigger (shown in figure 30) turns on the three TDC inputs (start, stop, rst), when the voltage across the sensor capacitor is lower than the early detection voltage. The rst_n is used to reset the cell at the beginning. The trigger is set to 1 when an edge appears at cmp_n. Each input is gated by an and gate, shown in figure 31. The gate of the start signal uses an inverted stop signal to stop the ring oscillator to decrease power.

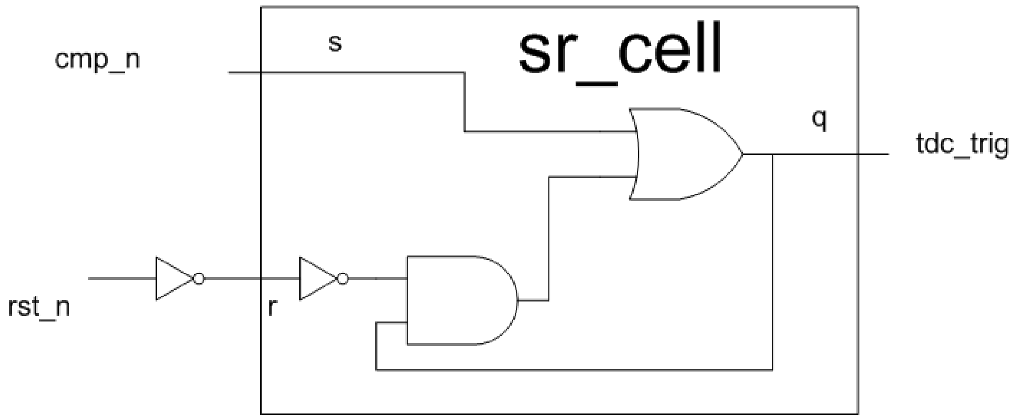

Figure 30 TDC trigger

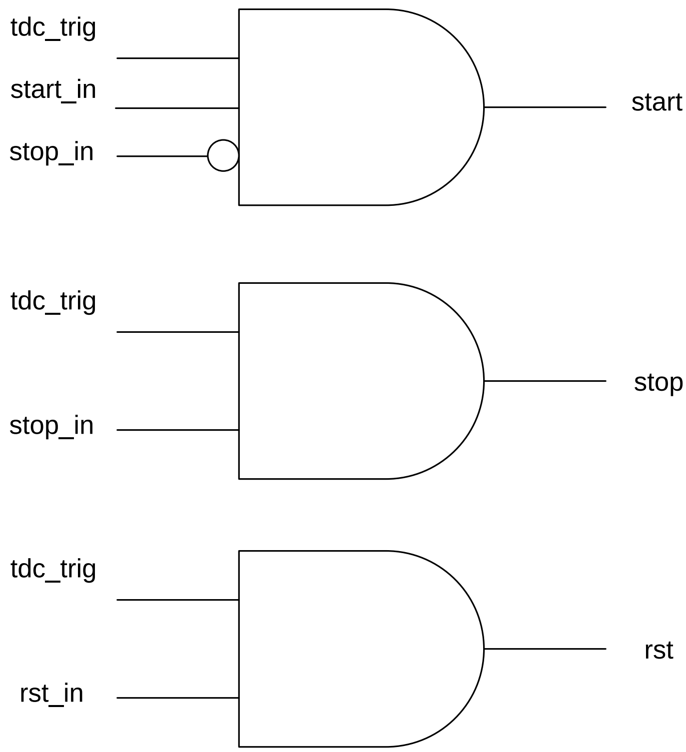

Figure 31 and gates

3.5.5 TDC layout

Figure 32 is the layout of the TDC core. The ring oscillator is the 16 nand gates in the middle. A dummy nand is placed at the up left corner of the ring oscillator. The cells at the top and the bottom are the D-flip-flops.

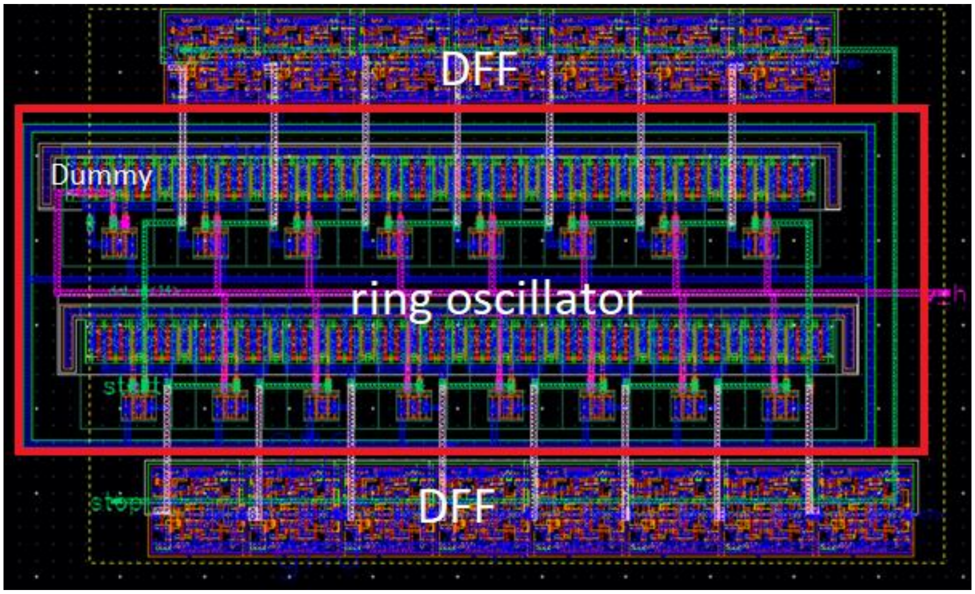

Figure 32 TDC layout

3.5.6 TDC simulation

A post layout simulation has been performed in which the time to be digitized is swept for each of the process corners, the FF, SS and TT. The DNL is calculated. The time step of the sweep is 5ps/step.

TT corner:

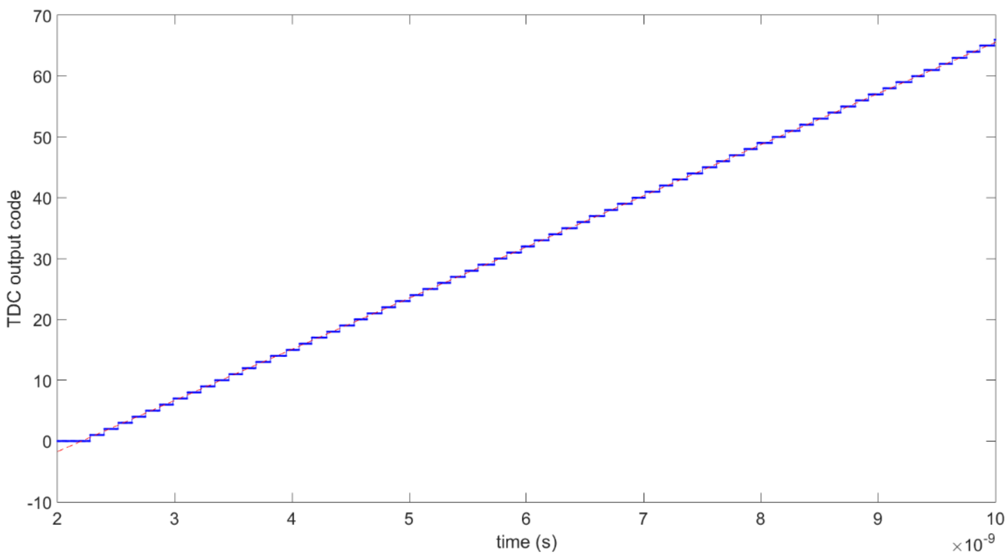

Figure 33 post-layout simulation in TT corner

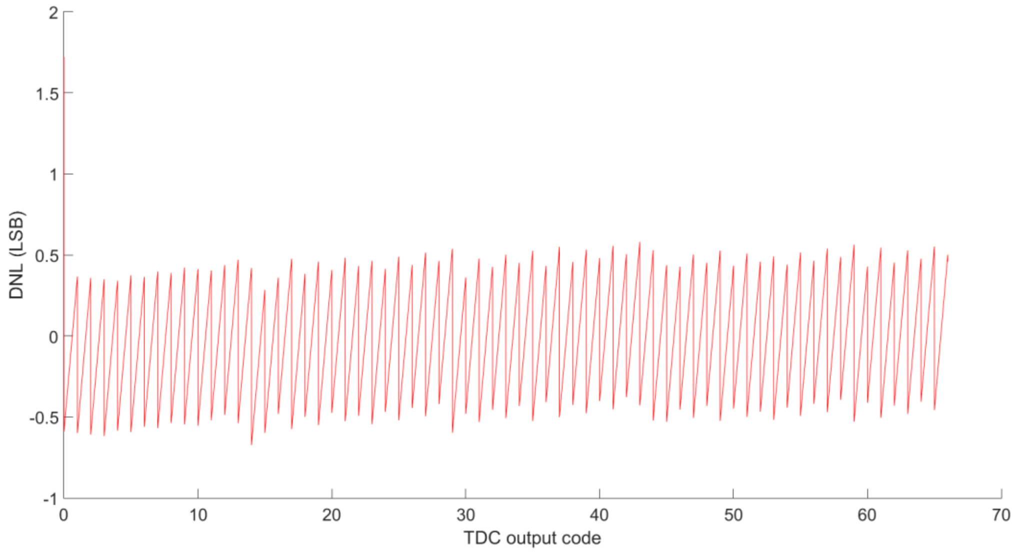

Figure 34 DNL in TT corner

FF corner:

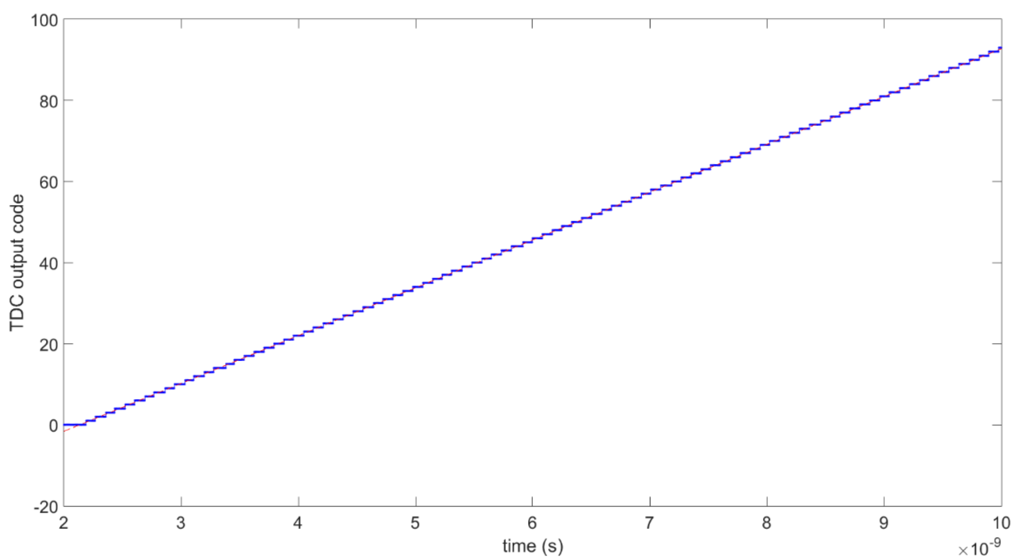

Figure 35 post-layout simulation in FF corner

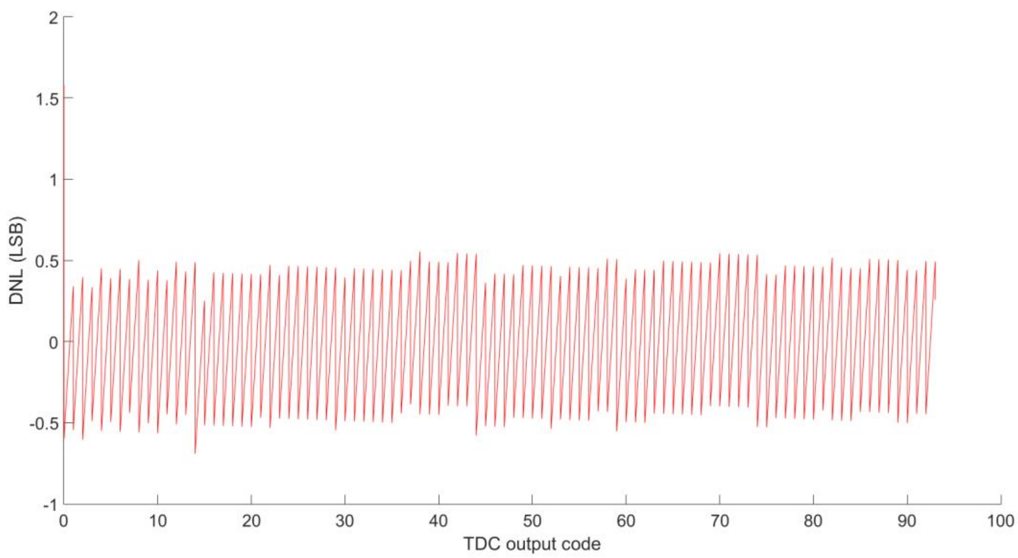

Figure 36 DNL in FF corner

SS corner:

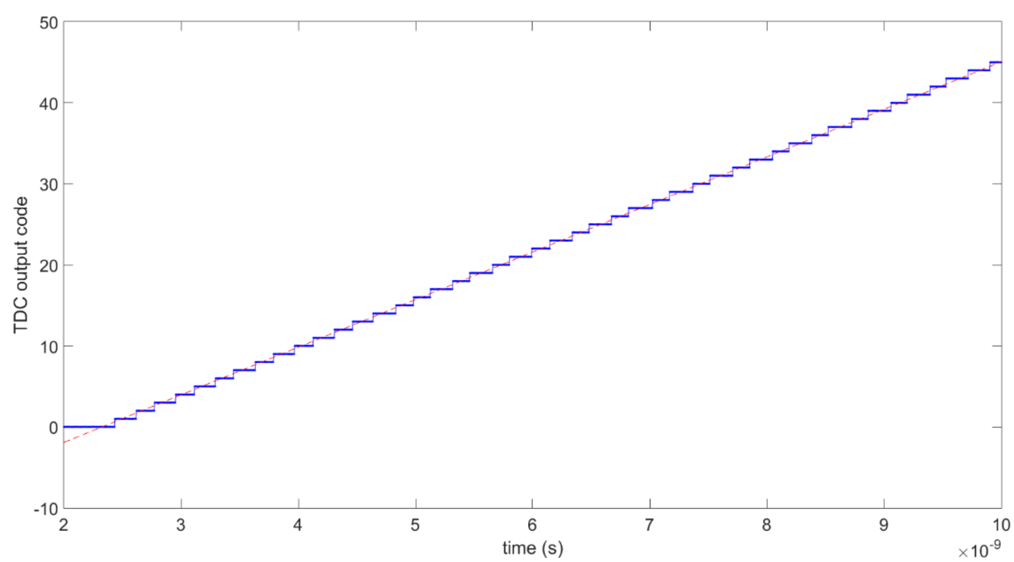

Figure 37 post-layout simulation in SS corner

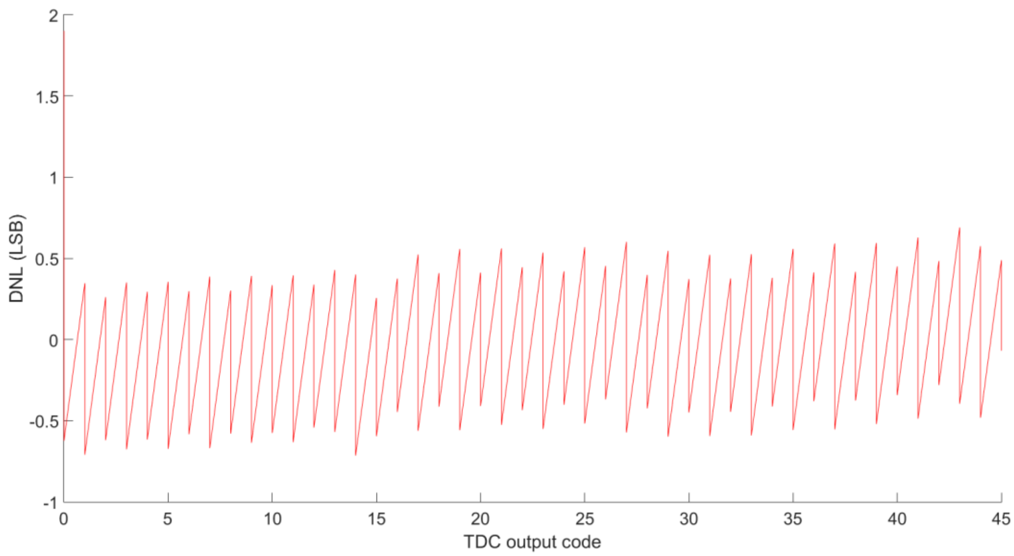

Figure 38 DNL in SS corner

From the simulation results we can see that the correction parts can perfectly fix the problem caused by the non-monotonicity.

Table 2 gives the simulated resolution of the TDC in different corners.

Table 2 Simulated resolution of the TDC in different corners

	TT	SS	FF
resolution	120ps	170ps	90ps

3.6 Conclusion

In this chapter, the detailed schematic design of the main blocks in the system has been given. The layout of the custom design has been shown. The corner analysis has been done on the TDC, which proves that the TDC is monotonic. The system is built based on the blocks discussed in this chapter.

4 System level simulation and layout

This chapter reports the system level simulation of the chip. First, the simulation waveform of the core of the chip will be shown. Then, the layout of the chip will be introduced. Finally, the system level post layout simulation of the chip will be shown. The simulated transfer curve of the whole chip will also be given.

4.1 System level simulation

Figure 39 shows the waveform of the voltage across the sensor capacitor during the operation process. The curve can be divided into 3 parts. In the first part, the voltage across the sensor capacitor is constant. At this moment, the CDC is in calibration phase. Then, it comes to the measurement phase. The sensor capacitor is firstly charged to the supply. Then, an iterative discharge process brings the voltage to the reference voltage, which corresponds to the steps down part in the curve. Finally, the voltage across the capacitor is lower than the reference voltage. The conversion is completed. In simulation, only several edges are used in the calibration phase, which corresponds to the flat region c_cx at the beginning in the figure. In practice, more edges are used to get an average as the time reference.

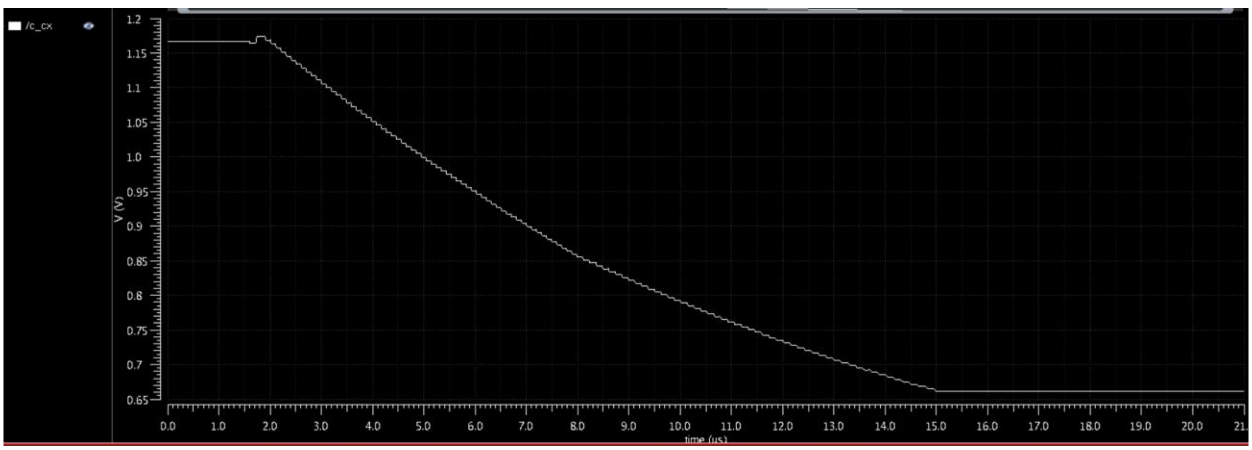

Figure 39 Voltage across the sensor capacitor during the operation process

4.2 Layout

Figure 40 shows the layout of the whole chip. Four 8pF decoupling capacitors are used for the supply. Digital I/Os are used for the inputs and outputs of the chip.

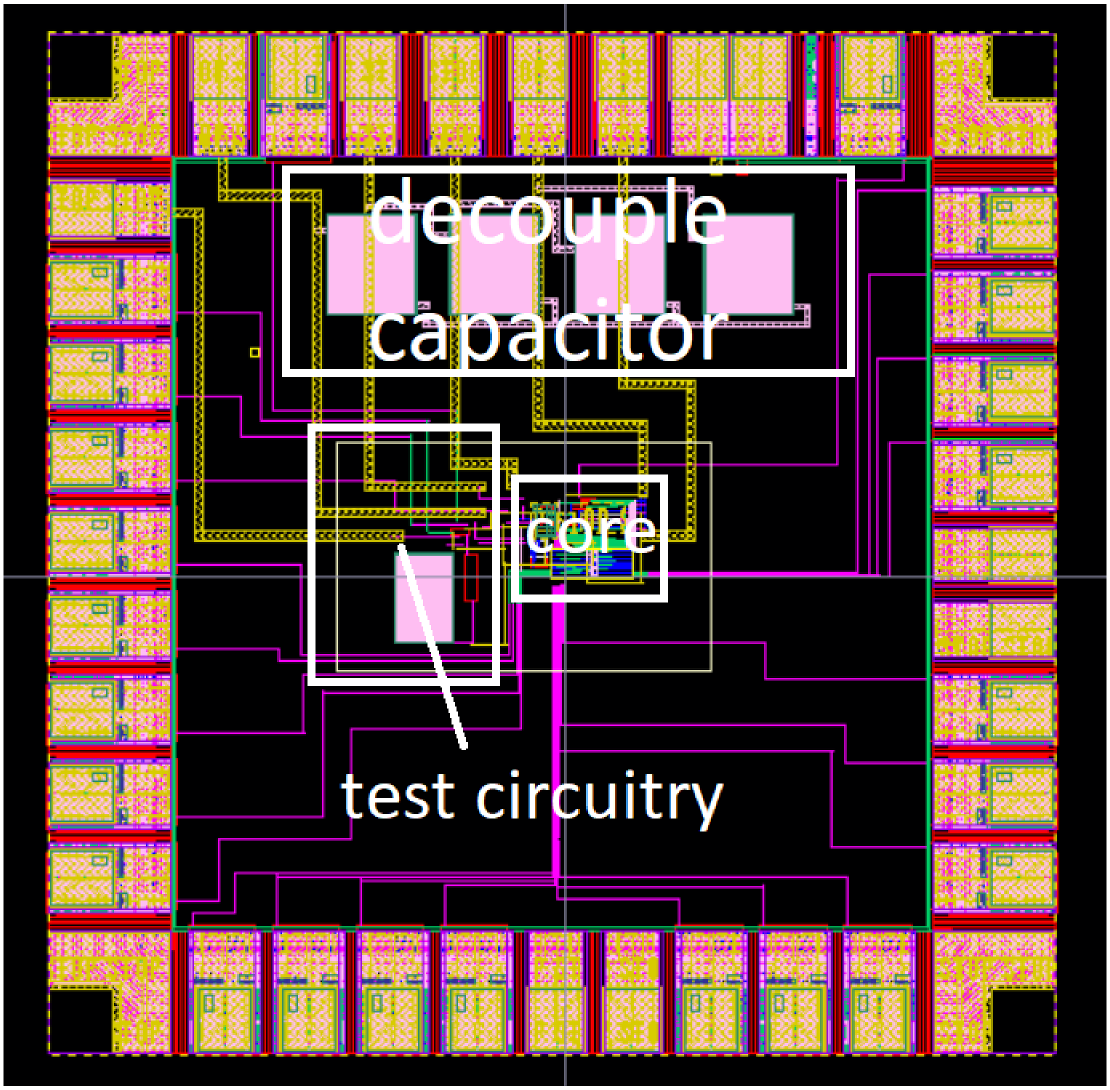

Figure 40 Chip layout

In figure 41, the core of the chip is shown. Its size is quite small, around 100µmx100µm, which is quite small. An element level CDC is possible with such area.

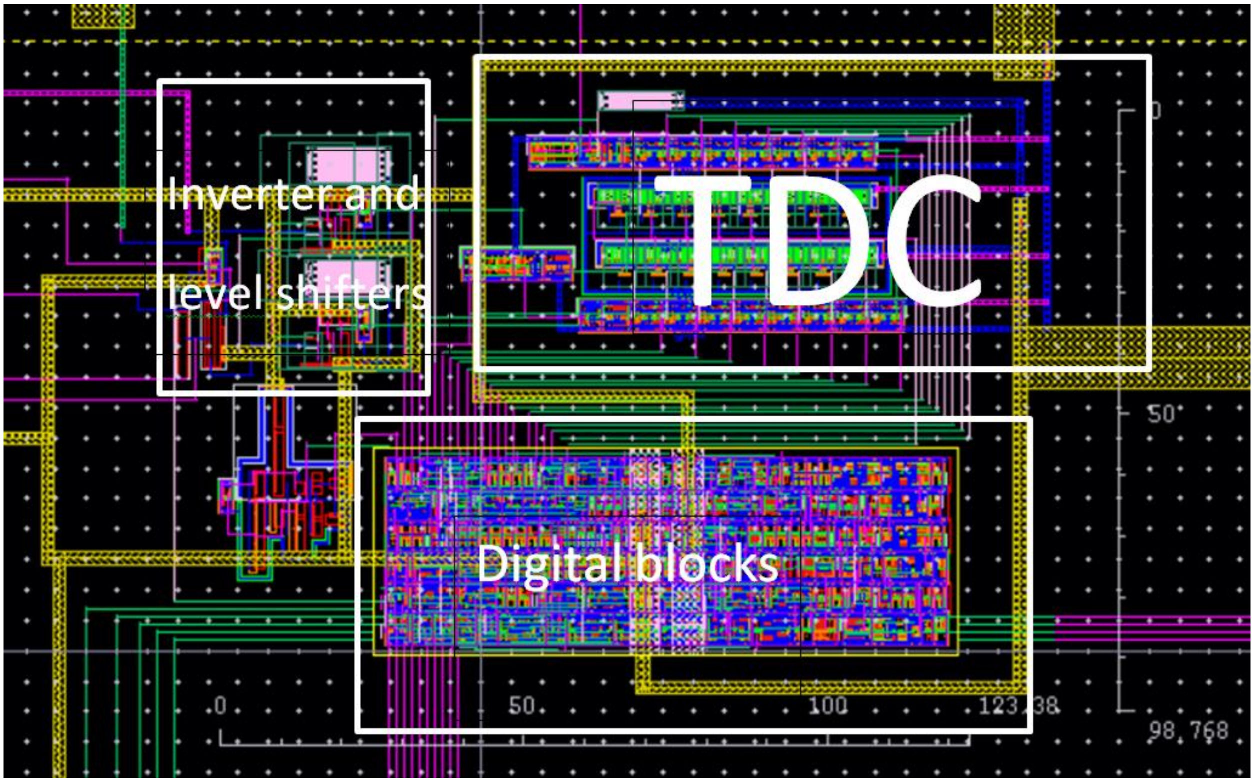

Figure 41 layout of the CDC core

4.3 System level post layout simulation results

In figure 42, the post layout simulation result of the whole chip is given (TT corner). A parametric sweep is done over sensor capacitance from 8pF to 8.05pF, where a transient simulation is performed for each capacitance. The step of the sweep is 1fF/step. The reference voltage ($\mathrm{V_{ref}}$) is 0.65V. Such voltage is determined by the lowest voltage to drive the inverter. A higher reference voltage gives less jitter but also less SNR for fine conversion. The early detection voltage is 0.8V, which is mainly a balance between jitter and power consumption. Large $\mathrm{V_{early}}$ gives lower jitter on early detection edges but the TDC is operated for a longer time, which means more power. Small $\mathrm{V_{early}}$ is good for power consumption but the jitter is bigger in the reference branch. This voltage can be changed to get the best performance in measurement.

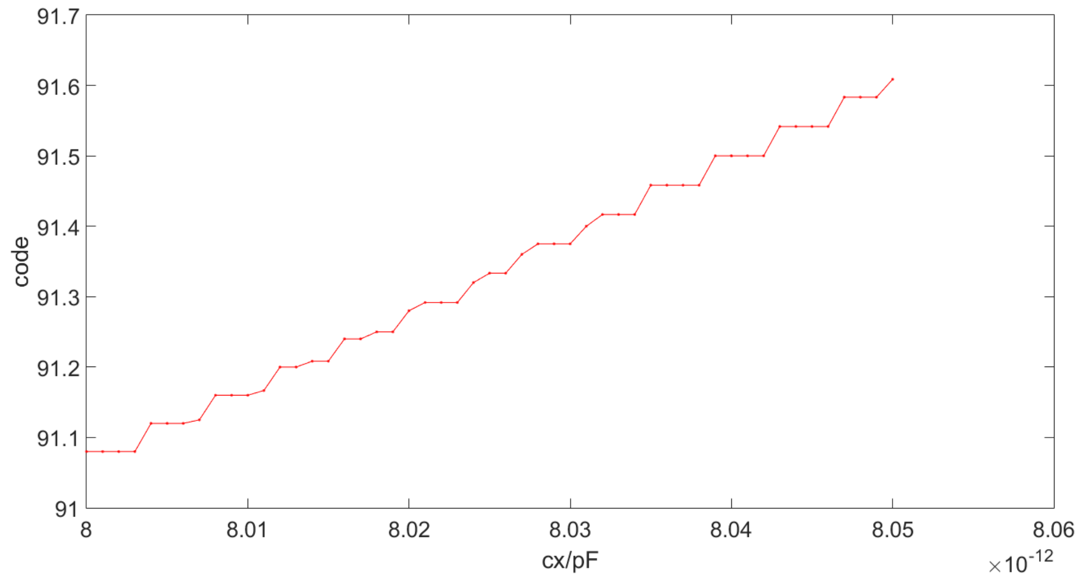

Figure 42 Transfer furve from 8pF to 8.05pF

In the transfer curve shown in figure 42, we can see quantization steps. According to the steps size, the resolution of the design is around 3fF at 8pF sensor capacitance. The simulation is done without thermal noise included.

In the transfer curve, we can also see some steps are not flat. The reason for such edges is explained in operation process by figure 43. In figure 43, there are 3 edges, the reference edge (V_ref), early detection edge (Early detection) and two edges in the discharge process (V_cx). A different sensor capacitor will make the edges in V_cx slightly different after the same discharge cycles. So, after the same discharge cycles, we will get a higher voltage with a slightly larger sensor capacitor, which reduces the inverter delay. As a result, the Out2[n] and Out2[n-1] are reduced. However, both Out2[n] and Out2[n-1] are not reduced with the same amount. So, Out2[n]-Out2[n-1] may be different depending the sensor capacitance.

For example, let's assume out2[n]-out2[n-1] is 10 and out1-out2[n-1] is 2. According to the expression 2.10, we get a fraction number of 0.2. With a larger capacitor (assume the same coarse code), out2[n] and out2[n-1] both change after the same discharge cycles. However, the change in out2[n] may be too small to cancel the change caused by out2[n-1], so we will get out2[n]-out2[n-1] =11. While, with the current out2[n-1], out1-out2[n-1] becomes 3, which means a fraction number of 3/11 .

$$fine\_code = \frac{out1 - out2[n-1]}{out2[n] - out2[n-1]} \qquad (2.10)$$

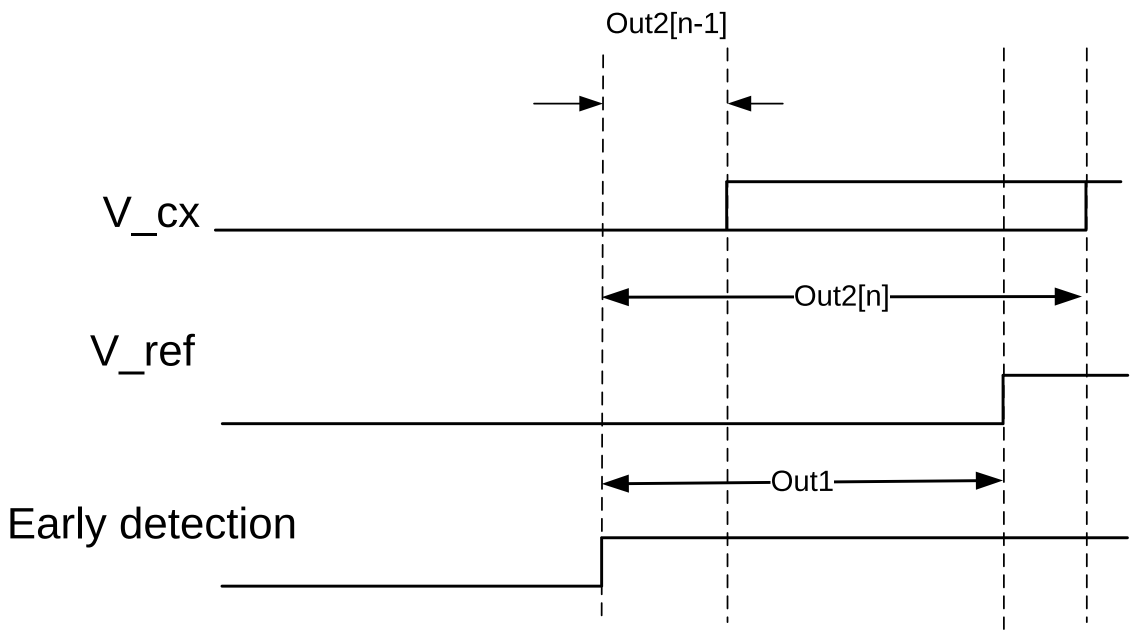

Figure 43 Operation process

The transient noise simulation (including thermal noise) has been done with the schematic of inverter and level shifter blocks and an ideal TDC, because the transient noise simulation of the complete circuit is too time-consuming. The result is shown in figure 44.

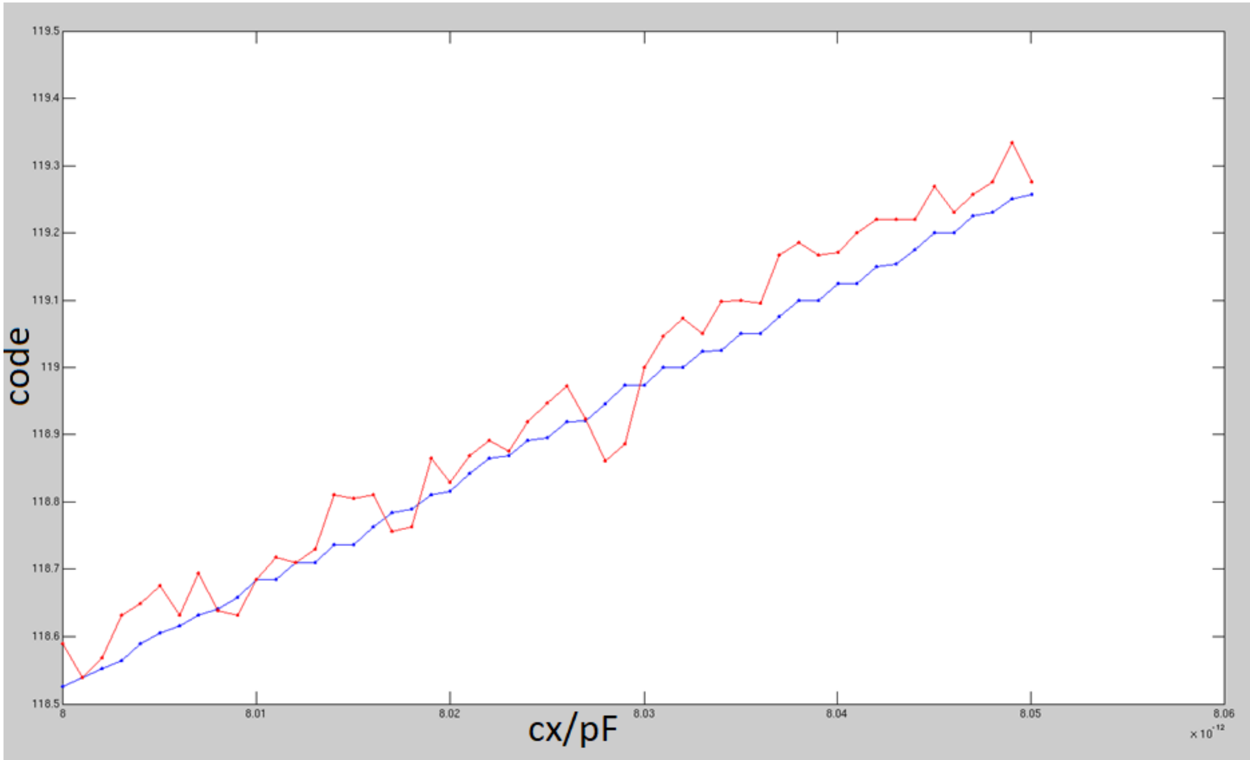

Figure 44 Code sweep results with noise (red) and without noise (blue)

In figure 44, the blue curve is the noise-free case and the red one is the result from transient noise simulation. The resolution is around 5fF.

The power of the CDC is mainly determined by the TDC operation time, which means a lower early detection voltage is helpful to decrease the voltage. In simulation, the averaged current is around 30uA. With a 1.2 V supply, the power consumption is 36µW. The conversion time of the CDC is 15µs, including the calibration and measurement phase. Those two results are simulated on an 8pF capacitor.

The capacitor range can be super big. Here we use 8pF as its full range, which corresponds to 5fF resolution.

The FOM of the CDC is 0.97pJ/step, which is calculated based on expressions 4.1 4.2 4.3.

$$FOM = \frac{Power \times Conv.Time}{2^{ENOB}} \tag{4.1}$$

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{4.2}$$

$$SNR = 20\log(\frac{Cap.range / 2\sqrt{2}}{rms\_resolution}) \tag{4.3}$$

The reference voltage, the early detection voltage and the number of the samples used in the calibration phase have influence on the resolution, power, conversion time and FOM. Based on the requirement, a higher resolution CDC can be achieved by changing the supply of the reference voltage. The early detection voltage determines the operation time of the TDC, which means that a lower early detection voltage benefits the power consumption.

4.4 Conclusion

In this chapter, the layout of the chip has been given and the system level simulation result have been reported. With a reference voltage of 0.65V and an early detection voltage of 0.8V, the estimated resolution of the CDC is 5fF. The power is 36uW. The conversion time is 15µs. The FOM is 0.97pJ/step

5 Experimental Setup

In this chapter, the test environment of the chip will be introduced as well as the on-chip test block. A PCB is designed to test the chip. The control of the chip is done through an FPGA. A serial port is used to transfer the data to the PC. Finally, the chip will be tested with a pressure sensor attached in a pressure chamber.

5.1 Chip Prototype

Figure 45 gives the block diagram of the chip. To reduce the number of required output pins, the CDC counter and the TDC outputs share the same pins (dout<9:0>) through a multiplexer. There are two on chip test capacitors, 0.5pF and 5pF. They are controlled by pins cap_ctr_0 and cap_ctr_1. In table 3, the pin names and their functions are given.

Table 3 Chip pin names and their functions

Pin name	Comment
v_cx	supply to charge sensor capacitor
vdd_early	Supply for early detector
vdd_ref	Supply for reference
vdd	Digital core supply
gnd	
vddd	Digital I/O driver logic supply
gndd	
vdde	Power supply, pad ring, 2 pairs
gnde	
c_cx	off-chip capacitor connection, which is used as the supply of the inverter in discharge process
cap_ctr<1:0>	Selection between on-chip capacitors and off-chip capacitor
cap_rst_n	on-chip capacitor reset
sw_ctr	Selection between calibration phase and measurement phase
start_n	start signal for the chip to work
rst_n	global reset signal
mux_ctr	Selection for the cdc counter and tdc code
clk	off-chip clock
clk_ctr	on-chip/off-chip clock selection
dout<9:0>	CDC counter output/ TDC output
correction	TDC correction bit
tdc_conv_fin	TDC conversion completion
cmp_p	comparator output (positive)
cmp_n	comparator output (negative)
clk_out	Output of edge generator

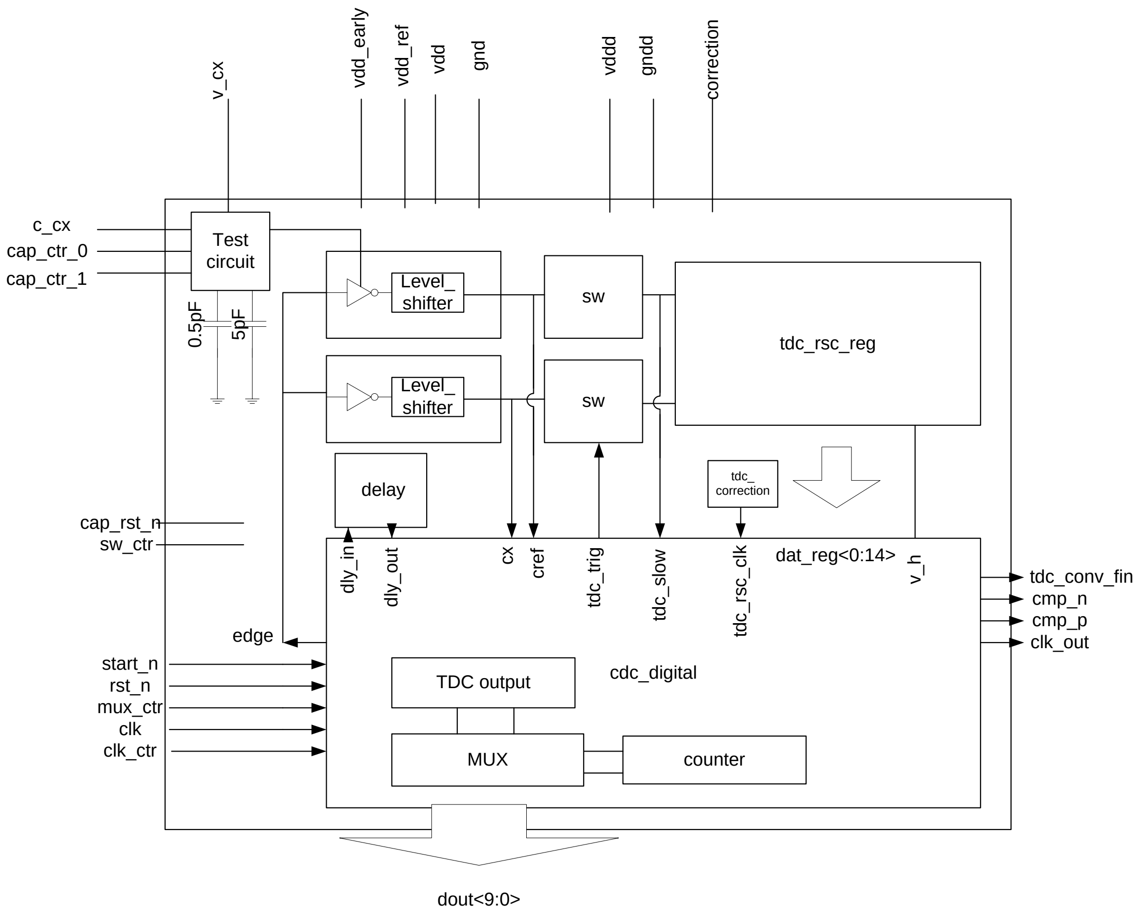

Figure 45 Block diagram of the chip

Through the test circuit shown in figure 46, three different test capacitor combinations (0.5fF, 5fF and 5.5fF) can be achieved. Linearity can be evaluated in this way. Another state in the switch block is used for an off-chip capacitor. Or it can be connected to a commercial pressure sensor [11].

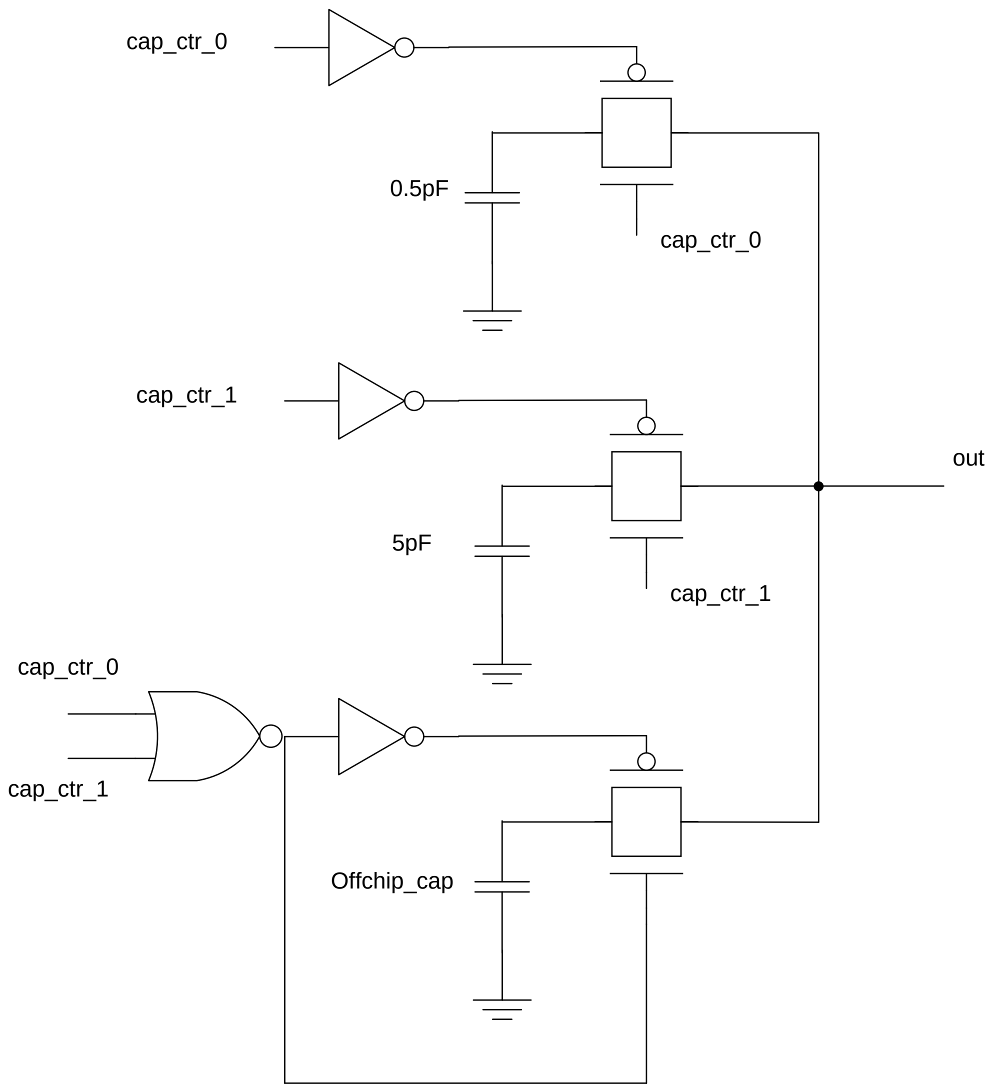

Figure 46 Test circuit

Bonding diagram

Figure 47 and Figure 48 are the bonding diagrams of the chip. The chip is bonded in a CLCC44 package. 24 samples have the pin Cx connected to the outside, which enables it to measure an off-chip capacitor. 8 samples have the pin Cx connected to a commercial pressure sensor (microFAB, Capacitive Pressure Sensor E1.3N) [11] (shown in figure 48). In figure 48, another side of the pressure sensor is connected the bottom of the package and uses conductive glue to connect to the ground pad.

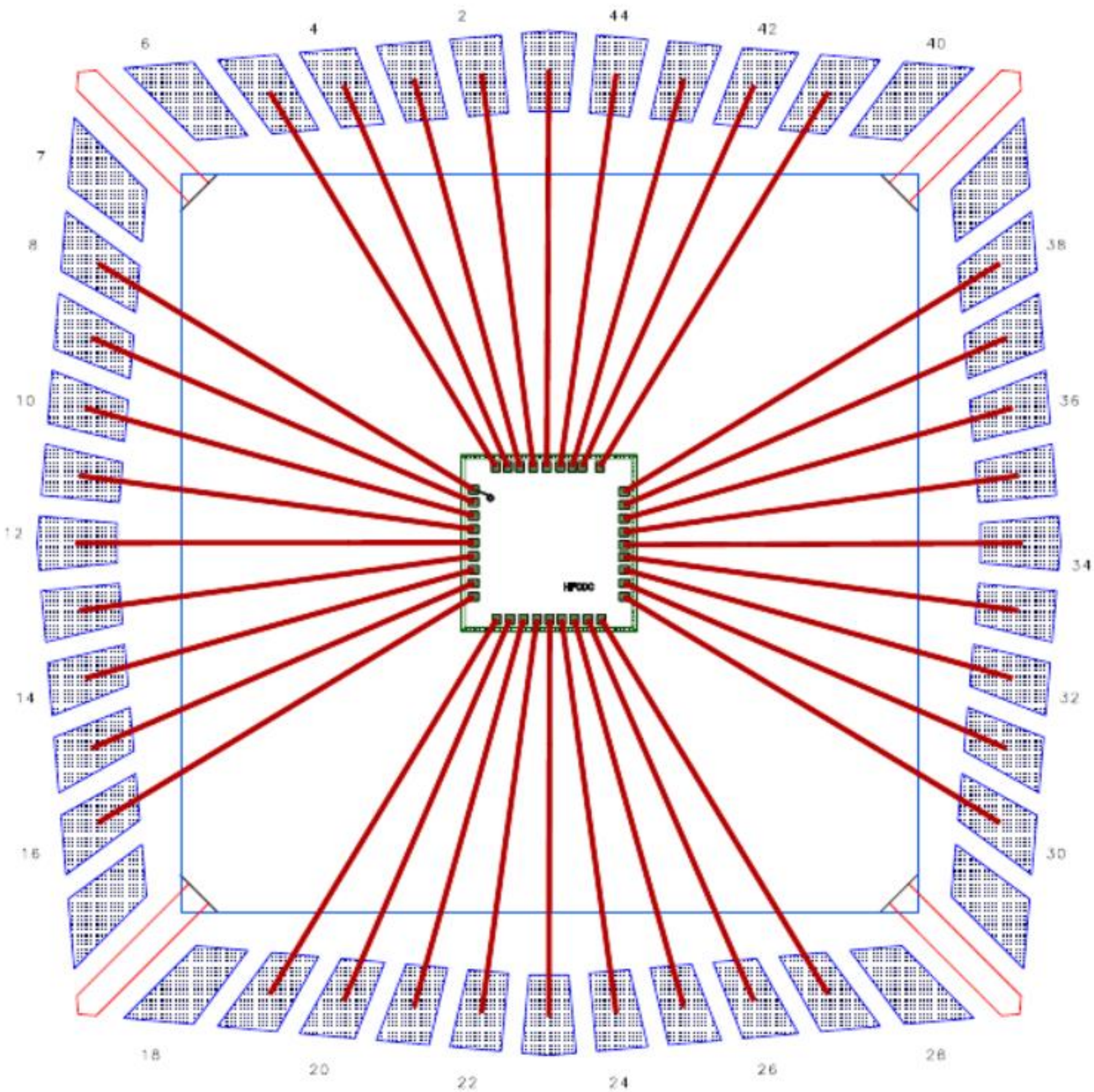

Figure 47 bonding diagram (without sensor)

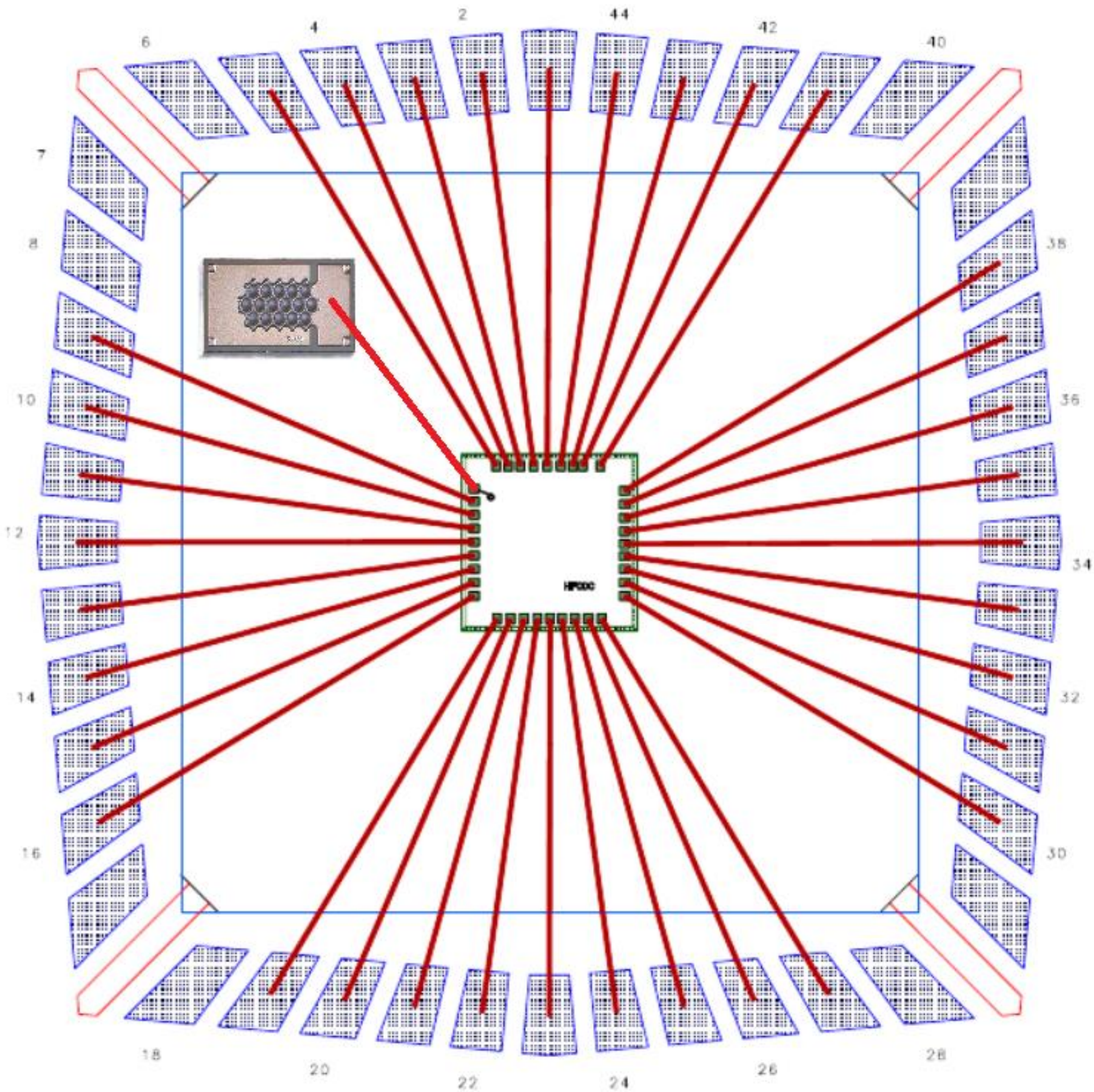

Figure 48 Bonding diagram (with sensor)

5.2 Test environment setup

The test can be divided into two steps. In the first step, the electrical parameters of the chip will be evaluated. In the second step, a bare die of a pressure sensor will be bonded to the chip and it will be measured in a pressure chamber. The first and the second steps share the same PCB board and control logics. Figure 49 gives a block diagram of the setup for the pressure measurements.

On the PCB, there are LDOs, level shifters and a chip socket. The chip core is powered through the LDOs. Level shifters are used to connect the chip outputs to the FPGA because of different supply domains. Some of the control signals (cap_ctr_0, cap_ctr_1, clk_ctr) will be set using jumpers because they are constant signals during each measurement. Level shifters are not needed on these signals. SMD capacitors can be clamped onto the PCB as a flexible way of connecting off-chip capacitors to the chip (shown in figure 50). The PCB is mounted on top of the FPGA board, shown in figure 51.

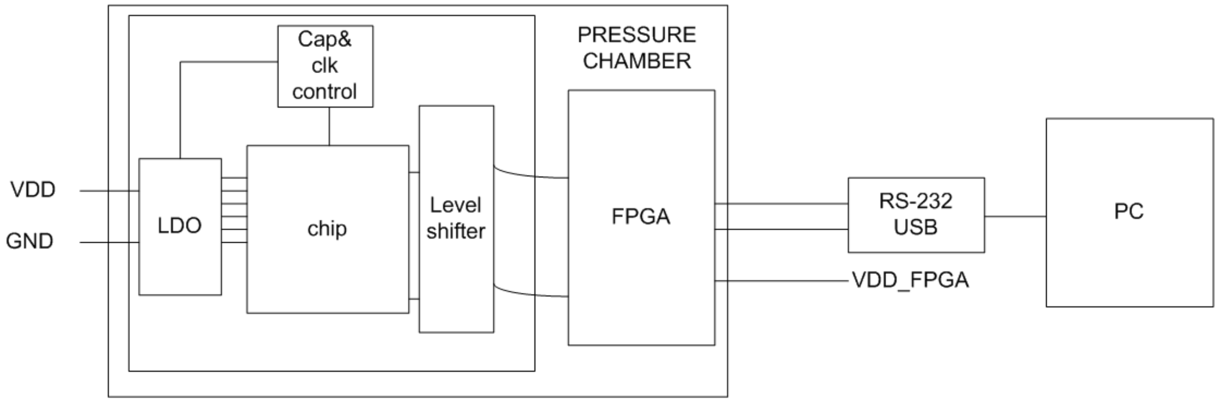

Figure 49 Block diagram of the pressure measurements

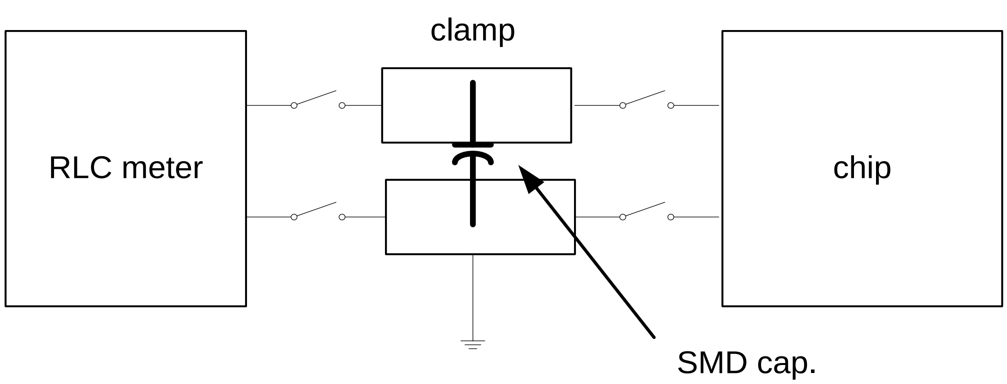

Figure 50 SMD capacitor clamp

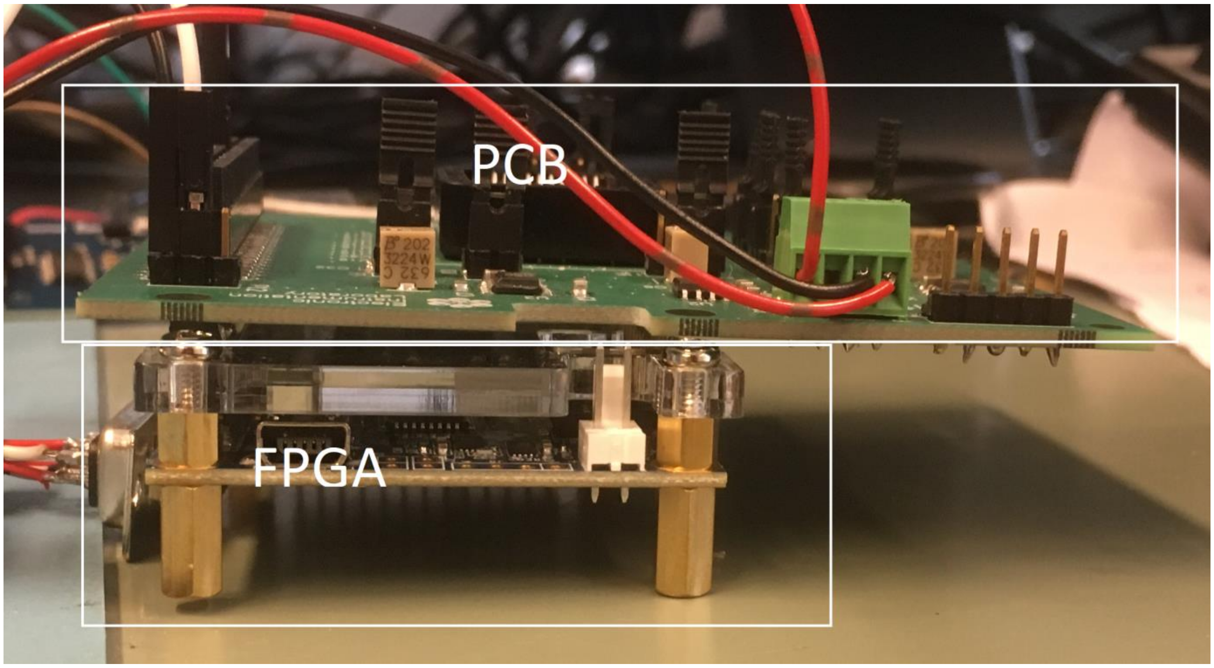

Figure 51 PCB and FPGA connection

5.2.1 PCB

In figure 52, the layout arrangement of the PCB is given.

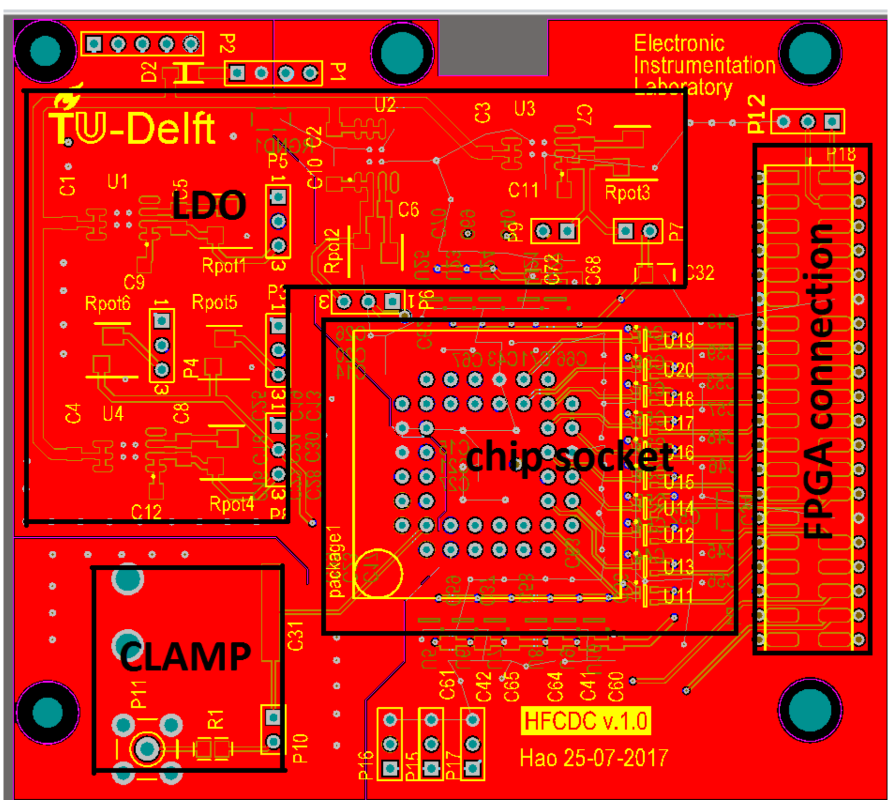

Figure 52 PCB

The PCB is restricted by the size of the pressure chamber, a cylinder which is 10cm in diameter and 12 cm in depth. Considering the size of the FPGA Board, 49mm*75.2mm in length and width and around 3 cm in height, the size of the PCB needs to be even smaller. The final size of the PCB is 91mm*81mm.

5.2.2 FPGA

Figure 53 gives the blocks on the FPGA. The FGPA can be divided into three parts, a FIFO part, a control blocks and a serial port. The FIFO is used to temporary saved the data from the chip because the data rate of the serial port is slow relative to the 5MHz chip output. The control block is mainly used to provide the operation signals for the chip. Also, it decides the time when the data goes to the FIFO or when the serial port starts to work.

The FIFO is built in the FPGA with its IP core. The calculation of the data will be processed by PC. The communication between the board and the PC is done through the serial port.

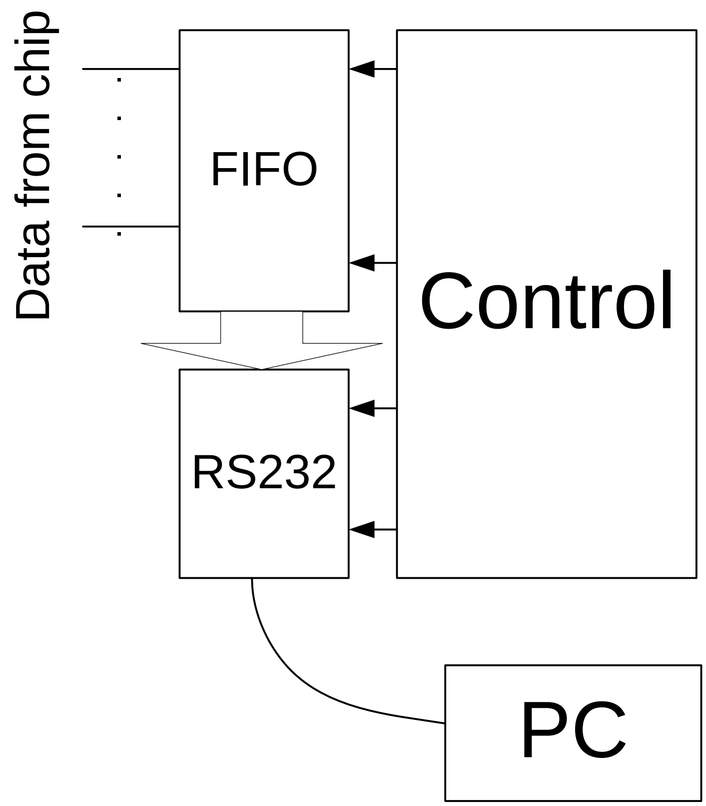

Figure 53 Blocks on FPGA

Control block

The control block mainly serves as the chip operation signal provider. It also decides the time of saving data into the FIFO and the communication between the PC and the FPGA board.

At the beginning, the system will be reset. Then, a system trigger signal comes in and it starts to operate. There are two operation phases, the calibration phase and the measurement phase. During the calibration phase, the supply of the signal branch is connected to a reference voltage. The TDC will keep working to measure the data to be used as the reference. 30 data points will be saved into the FIFO of the FPGA. And then, all those data points will be transferred into the PC and an average will be calculated via Matlab. This result will be used as the reference number, which will be transferred back into the FPGA.

After that, the measurement phase is started. The FIFO will keep sampling the output data from the chip. At the same time, the control block will also acquire the data and compare it with the reference number. In this way, a simultaneous control on the loop can be applied. When it detects a number larger than the reference, the conversion is stopped. At the end of the conversion, the switch of the MUX inside the chip will be togged and the number in the counter will be saved in the FIFO. So, through trace back, we can find the data we need to calculate the result.

Figure 54 gives the control flow of the FPGA.

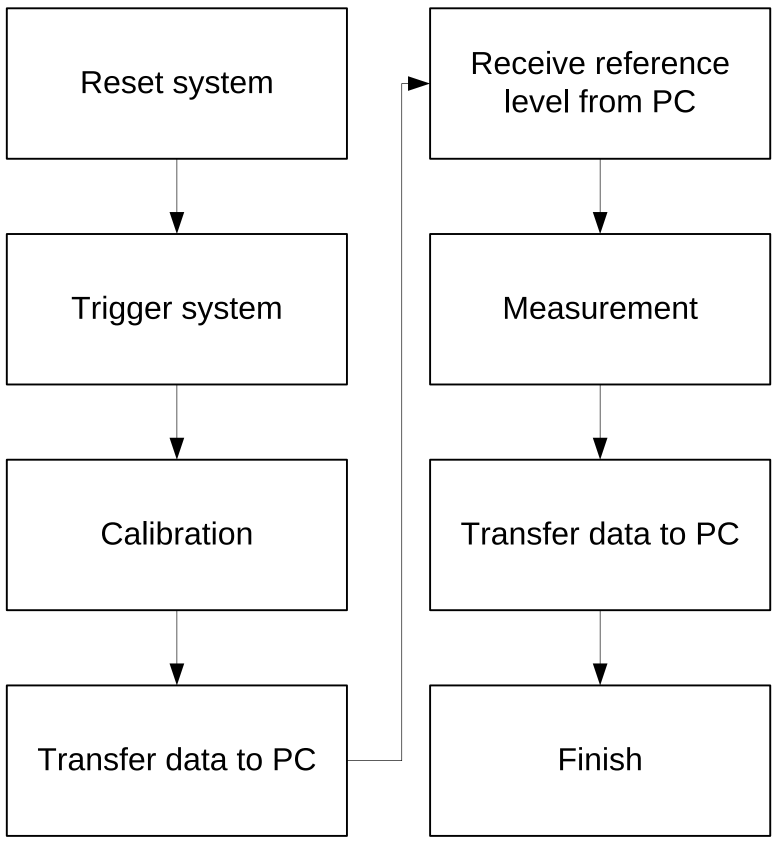

Figure 54 Control folw of FPGA

Serial port block

The control of the whole FPGA and the data communication between the PC and the FPGA is done through the serial port. It can be divided into two parts: FPGA to PC and PC to FPGA

FPGA to PC

This part of the block is used to transfer the data from the chip to the PC. The serial port can only transfer 8 bits at one time. But the data width of the chip is 11 bits (transfer data from FIFO to PC, a correction bit is included here). So, 2 bytes are used to transfer the data. What needs to be noticed is that when transfer data out, the clock that is applied on the FIFO needs to be half of the output clock of the serial port, since one data package needs two bytes to transfer. The control flow is shown in figure 55.

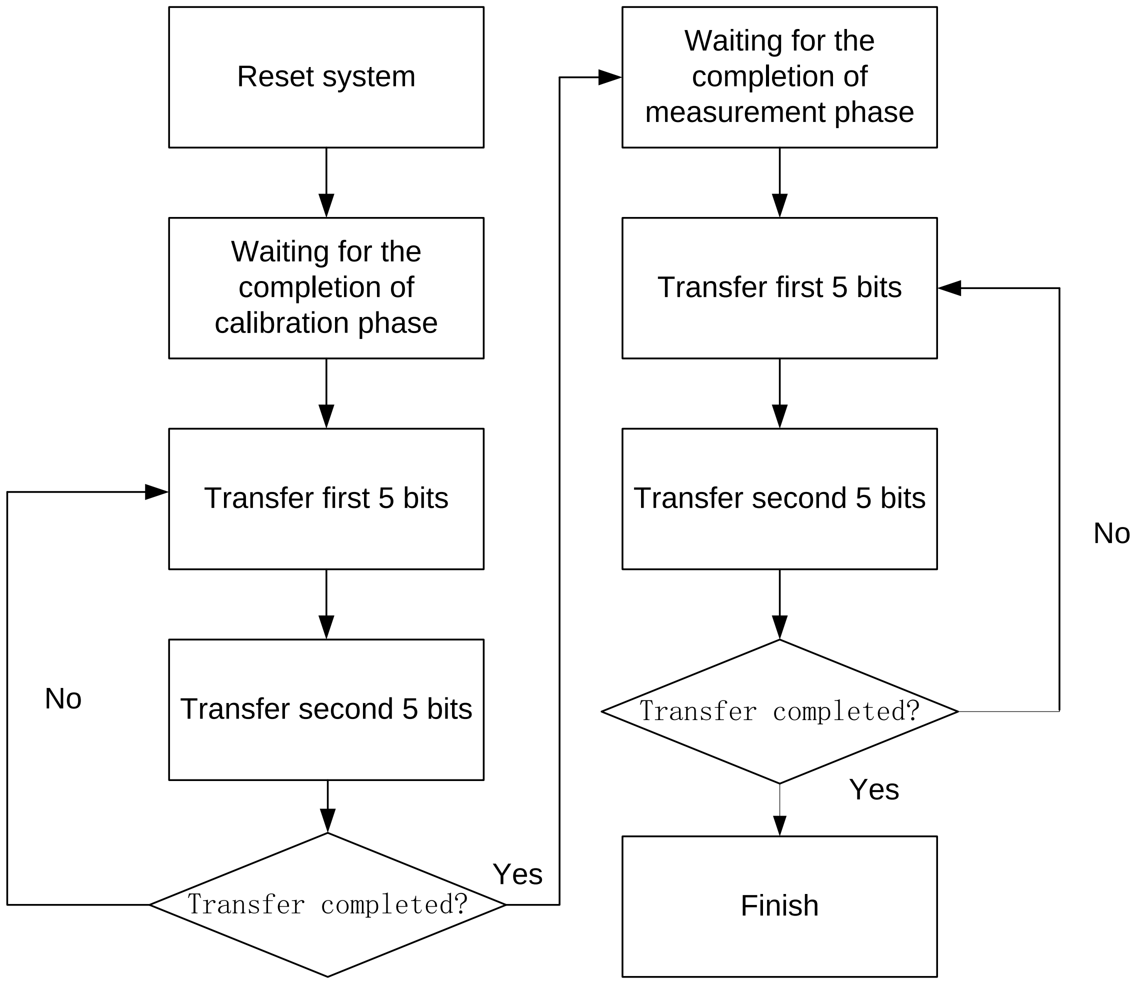

Figure 55 Control flow from FPGA to PC

PC to FPGA

This part is used to apply the control signal to the FPGA as well as transfer the calculated average back from PC. At the beginning, a global reset signal is applied to FPGA through control word '11111111'. Then, a control word of '00000000' is used to start the system. After the finish of the calibration phase, the PC transfers the calculated average to the FPGA. The PC will transfer 10 bits to the FPGA in total. They will be transferred two packets of 5 bits. So, there is still 3 empty bits in each transfer. Those 3 bits are reserved as signal symbols. '101' and '010' are the pattern used here to tell which half of those 5 bits is in the total 10 bits data. Finally, a control word of '11000000' is used to have the FPGA start the measurement phase. Figure 56 shows its control flow.

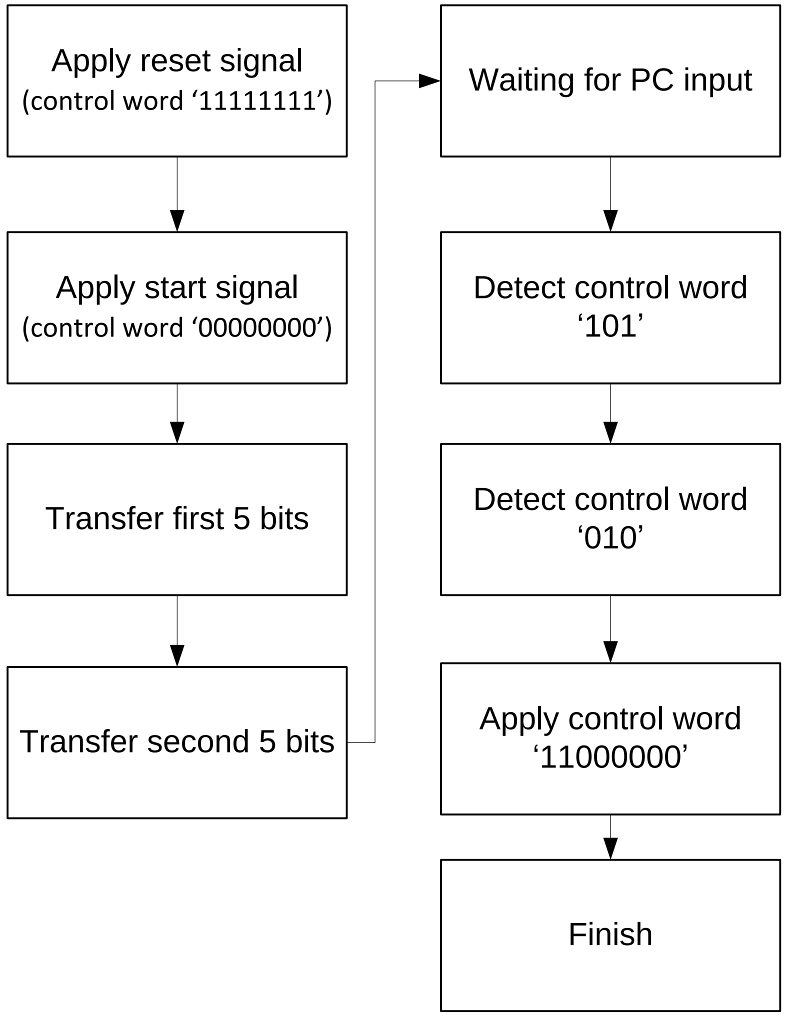

Figure 56 Control flow from PC to FPGA

5.3 Pressure Chamber test

Figure 57 shows the test environment setup of the chamber. A pressure pump and a vacuum pump enable that the pressure can be swept from below atmosphere to above atmosphere.

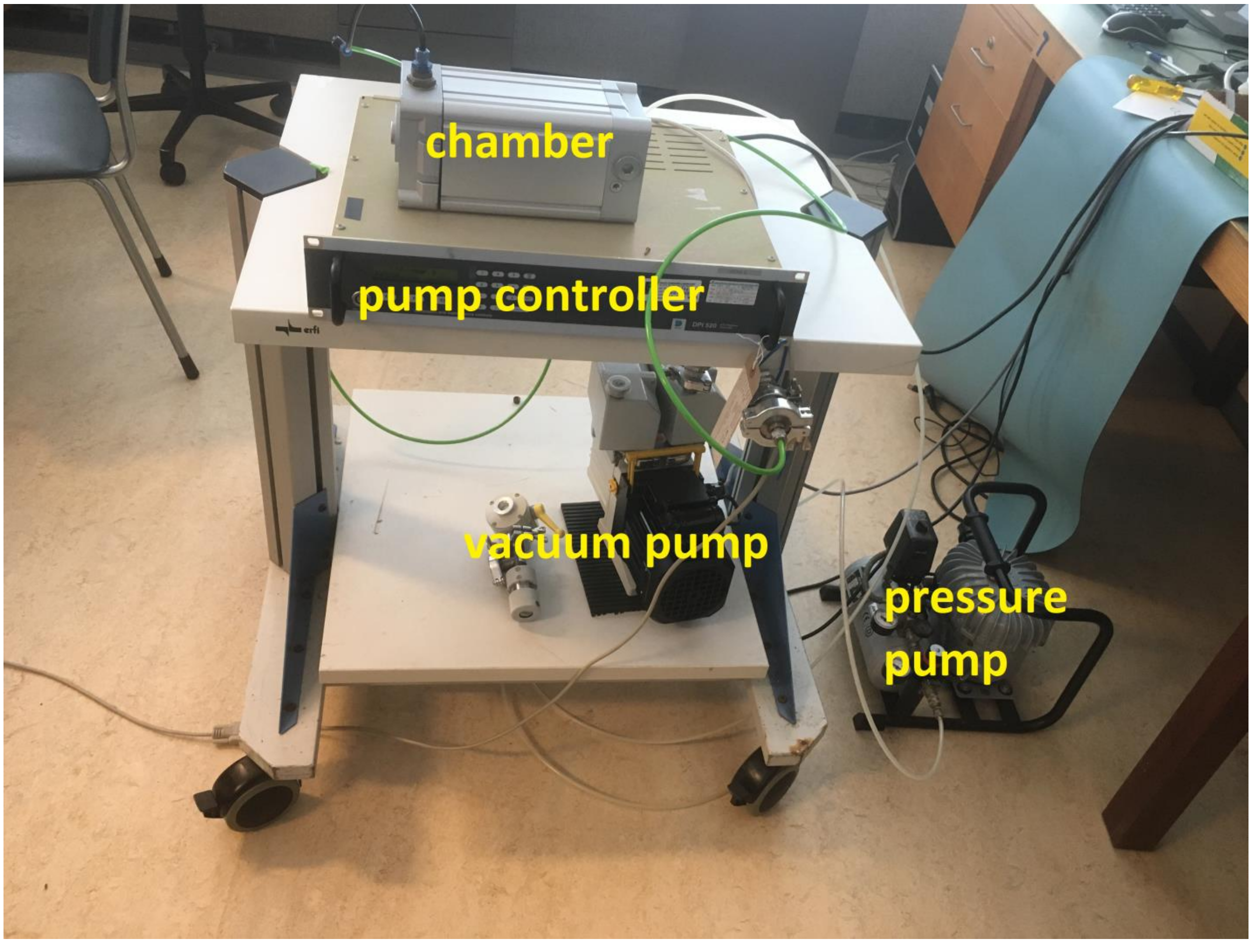

Figure 57 test environment

5.4 Conclusion

In this chapter, the test environment of the chip is introduced as well as the on-chip test block. A PCB is designed to test the chip and a FPGA is used for the control logic.

6 Measurement

In this chapter, the measurement results of the chip will be given. First, the electrical characteristics of the chip will be presented, including resolution, power consumption and conversion time. Then, the results of an experiment with a capacitive pressure sensor will be reported. For this, the chip has been placed in a pressure chamber with a MEMS pressure sensor bonded to it.

6.1 Measurement with on-chip capacitor

Figure 58 shows the chip micrograph.

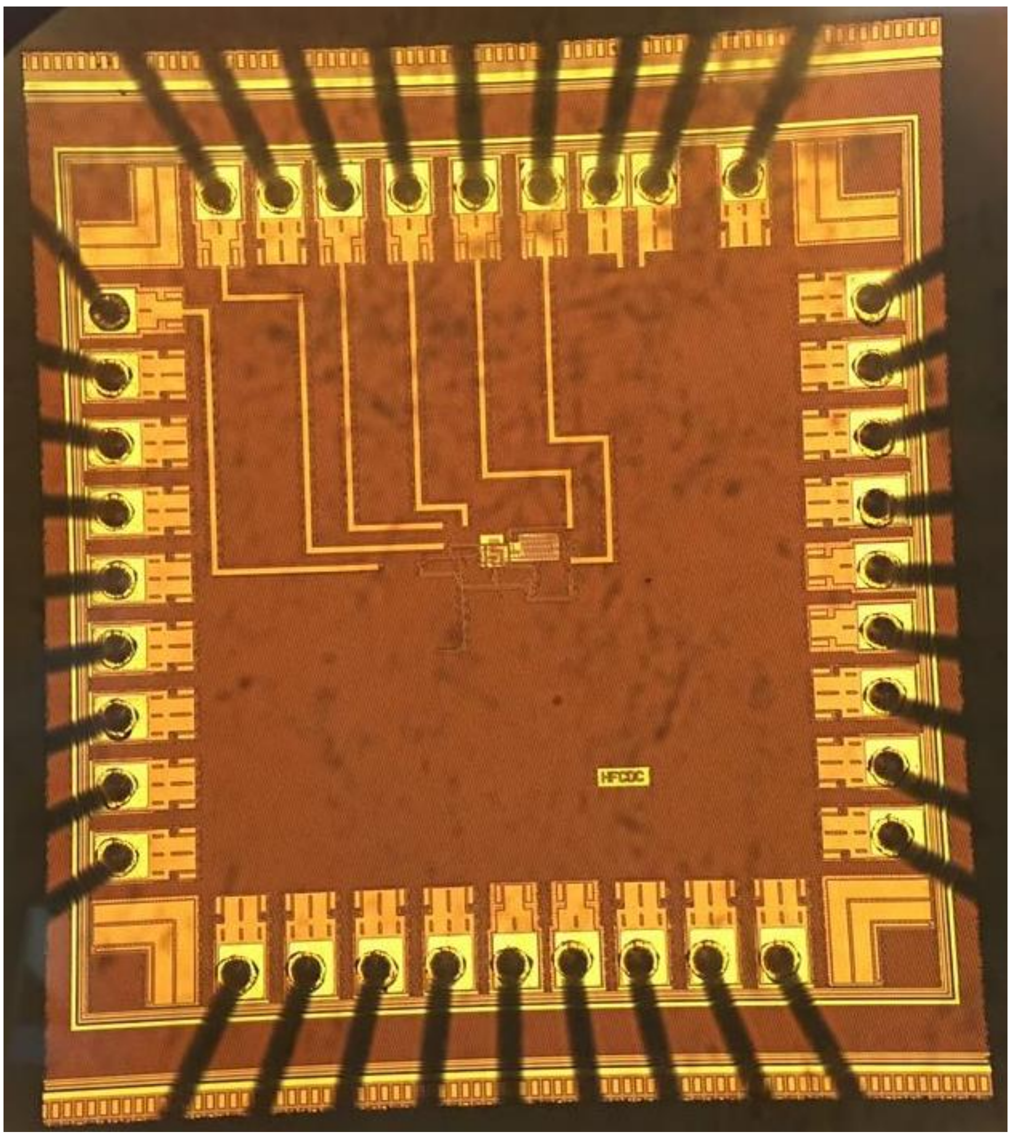

Figure 58 chip micrograph

Figure 59 shows the transfer curve of the chip (measured and simulated). Here, the measurement is done with V_{ref} =0.6585V, V_{early}=0.71V. Here, V_{ref} is close to the voltage used in simulation. The trimming resistor is sensitive; it is difficult to get 0.65V sharp. V_{early} is lower than the voltage used in simulation, since a low early detection voltage is beneficial for power consumption.

The output codes of 3 on-chip capacitors (0.5fF, 5fF, 5,5fF) are measured. The transfer curve is obtained through best linear fit.

$$code = 11.22\,pF^{-1} \bullet Cx + 1.3 \quad (6.1)$$

From expression 6.1, the slope of the transfer curve is $11.22pF^{-1}$, which means when the capacitance changes 1pF, there will be a change of 11.22 in the output code. The slope calculated from simulation is $11.10pF^{-1}$. The two results are quite close.

Based on the slope, the resolution of the CDC can be measured by using Monte Carlo method. Multiple measurements will be done. Their standard deviation σ will be translated into an equivalent capacitance resolution through the slope of the transfer curve.

$$resolution = \sigma / slope \quad (6.2)$$

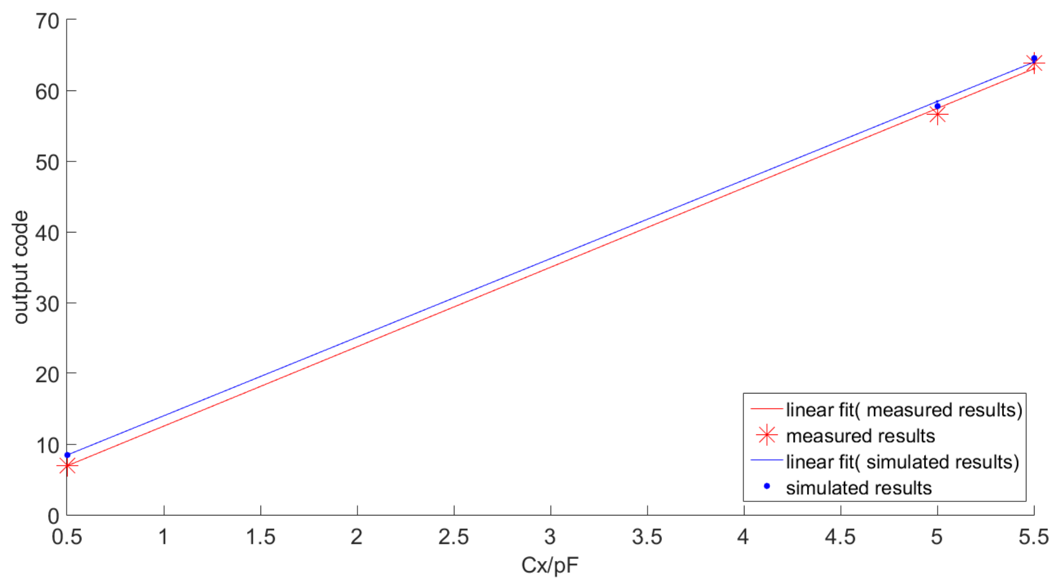

Figure 59 Transfer curve of the CDC

Figure 60 shows the results of 200 repeated measurements of the 5.5pF on-chip capacitor. The reference voltage is 0.6585V. The early detection voltage is 0.71V. The time between each two measurements is around 1s, which is almost totally consumed by the data communication through RS232 between PC and FPGA.

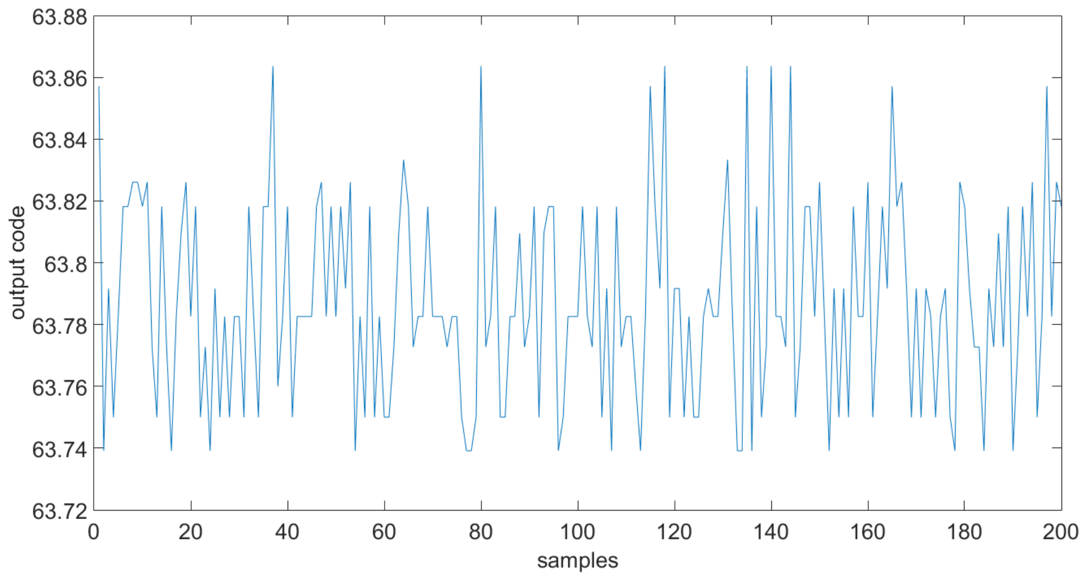

Figure 60 final output code of 5.5pF

Figure 61 shows a histogram of these measurements. The average of the measurement is 63.781. The standard deviation is 0.0318. Based on expression 6.2, the resolution is 2.8fF. In figure 62, the TDC outputs at the crossing point of each measurement are given. The time reference from the calibration phase is in orange (Out1). The blue curve is the TDC outputs with the Cx edge before time reference (Out2[n-1]). The red curve is the TDC outputs with the Cx edge after the time reference (Out2[n]) .

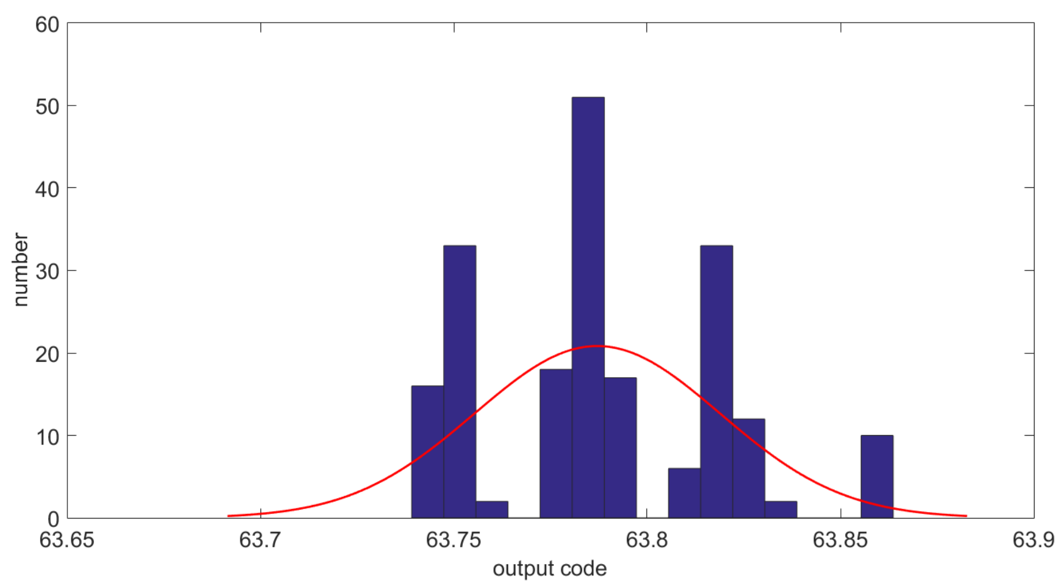

Figure 61 Histogram of the measurements on 5.5pF capacitor

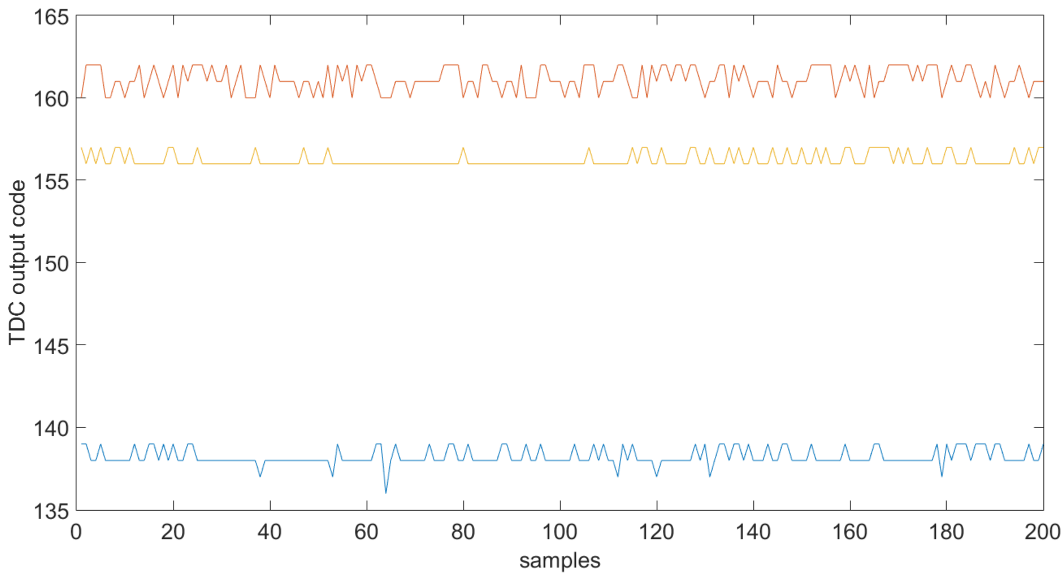

Figure 62 measured time steps for interpolation

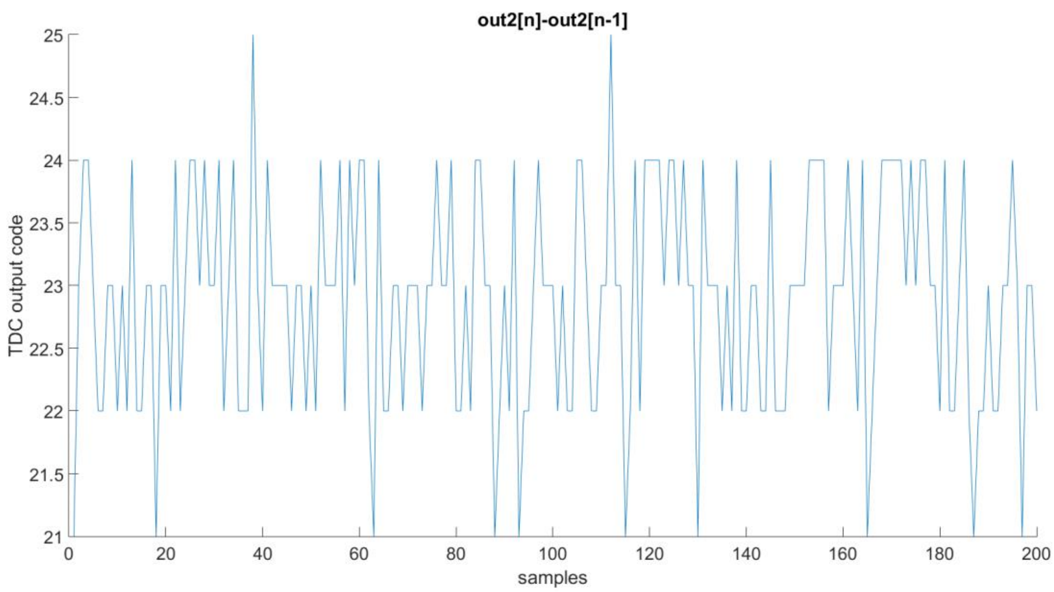

Figure 63 The results of out2[n]-out2[n-1] (time step)

In figure 63, the results of out2[n]-out2[n-1], are shown from which we can estimate the SNR. The time step is 23 TDC output code. Because of noise, the TDC output is toggling from 22 to 24. According to the result shown in figure 62, the SNR is around 10. The load capacitor is around 35fF, which means a resolution of around 3.5fF. So, the measurement result agrees with theory.

The simulation is done with an 8pF and the simulated resolution is 5fF. A large sensor capacitor will degrade the SNR of the fine conversion. According to the expression 2.23, we can estimate the new SNR from the current one by change the value of cx from 5.5 pF to 8 pF. The new SNR is 10*5.5/8, which is around 7. So, according to expression 2.24, the resolution will be around 5fF at an 8pF capacitor.

We can further improve the resolution through multiple measurements, which is done by calculating the average from every successive 5 measurements in the 200 measurements. The resolution can thus be improved to 1.18fF. The square root of 5 is around 2. So, the improvement from the average process agrees with theory.

The blue curve in figure 64 shows the ultimate resolution achieved with this CDC in a log-log scale plot. It includes around 4900 repeated measurements on 5.5pF capacitor. By averaging different numbers of successive samples and calculate the standard deviation, the improvement of the average process is shown. The resolution is improved by $\sqrt{\text{average times}}$. Also, such curve proves that the design is a thermal-noise-limited design. The ultimate resolution is around 0.6fF, which is 1/f noise or drift limited. The red curve in figure 64 shows the improvement of resolution by averaging in ideal case, which is used as comparison.

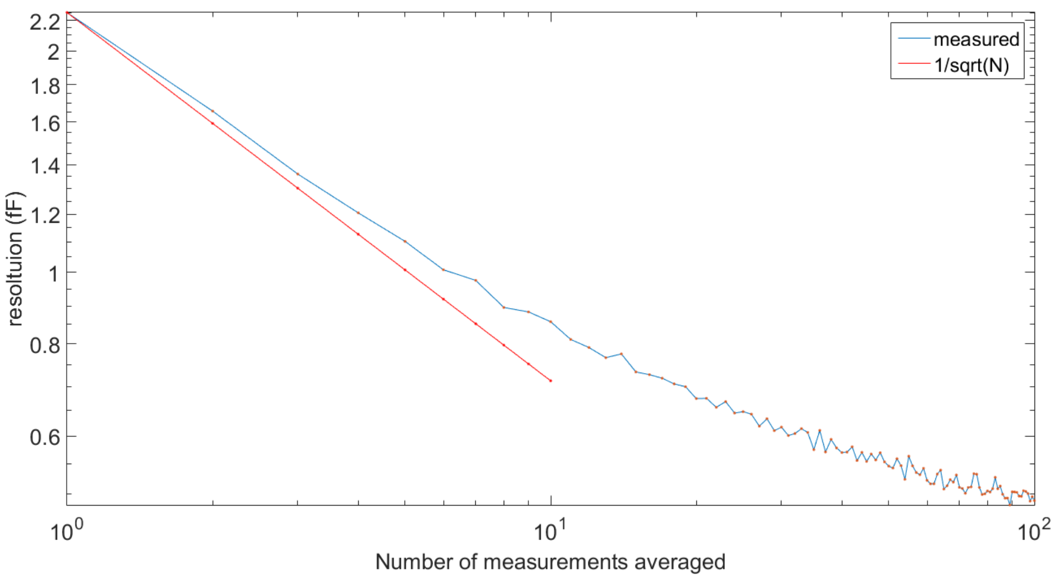

Figure 64 Ultimate resolution achievable with this CDC

The conversion time and the average current consumption have been measured by disabling the data transfer function in the test bench, since the transfer time of the serial port is much longer than the exact conversion time. The measurement of conversion time is done by measuring the output clock of the CDC(clk_out) using an oscilloscope. The power of the CDC is measured by operating the CDC continuously in a similar time as the conversion time. The conversion time is 25µs; including 6µs to fully charge the capacitor (can be reduced). The average current is 25µA. The supply is 1.2V. The FoM is 1.32pJ/step. The FoM is calculated based on expression 4.1, 4.2 and 4.3. Here, we write them down again. The capacitor range could be very big, but degraded with performance. So, 5pF is used as its range with a resolution of 2.8fF.

$$FOM = \frac{Power \times Conv.Time}{2^{ENOB}} \tag{4.1}$$

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{4.2}$$

$$SNR = 20\log(\frac{Cap.range / 2\sqrt{2}}{rms\_resolution}) \tag{4.3}$$

6.2 Measurement with a capacitive pressure sensor

After the electrical parameters are evaluated, the CDC is tested in a pressure chamber with a commercial chip-scale pressure sensor [11]. Figure 65 shows the specifications of the pressure sensor. Figure 66 shows the capacitance pressure dependency.

Physical Model		Value	Unit	Notes
Capacitance @ P_{ZS}	C_{ZS}	5.838	pF	@ 0 V_{DC}, T_{ref}
Capacitance @ P_{ref}	C_{ref}	6.026	pF	Sensor characteristics are 100%-tested on wafer-level. The number of data points can be chosen according to the appication's requirements.
Capacitance @ P_{FS}	C_{FS}	6.206	pF	
Full-scale sensitivity	S_{FS}	7.6	%	$(C_{FS}-C_{ZS})/C_{ref}$ x 100, @ T_{ref}
Average sensitivity	S	0.451	pF/bar	(S_{ref}=0.519 pf/bar @ Pref)
Capacitance @ P_{ZS}	C_{ZS}	5.822	pF	@ 50°C
Capacitance @ P_{ref}	C_{ref}	6.005	pF	@ 50°C
Capacitance @ P_{FS}	C_{FS}	6.183	pF	@ 50°C
Reference Temperature	T_{ref}	25	°C	
Hysteresis	ΔC_H	$<2\times10^{-2}$	%	Max. $(C_{Down}-C_{Up})/C_{FS}$ x 100

Figure 65 sensor specifications [11]

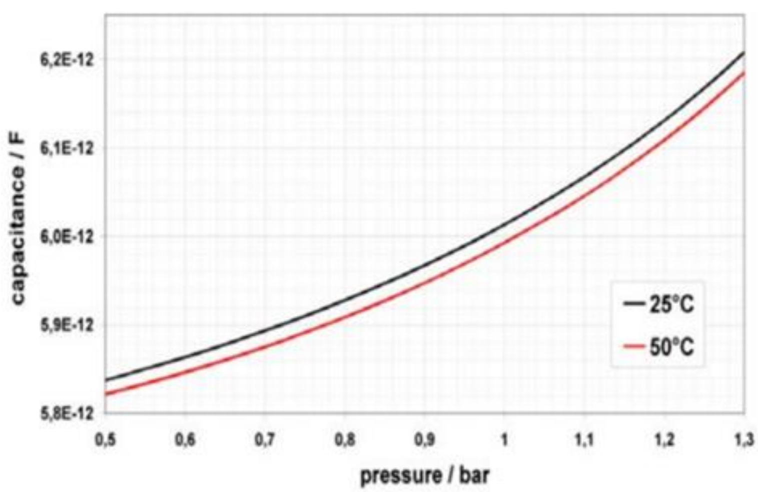

Figure 66 Capacitance pressure dependency [11]

The pressure sensor is wire-bonded to the CDC in package, shown in Figure 67.

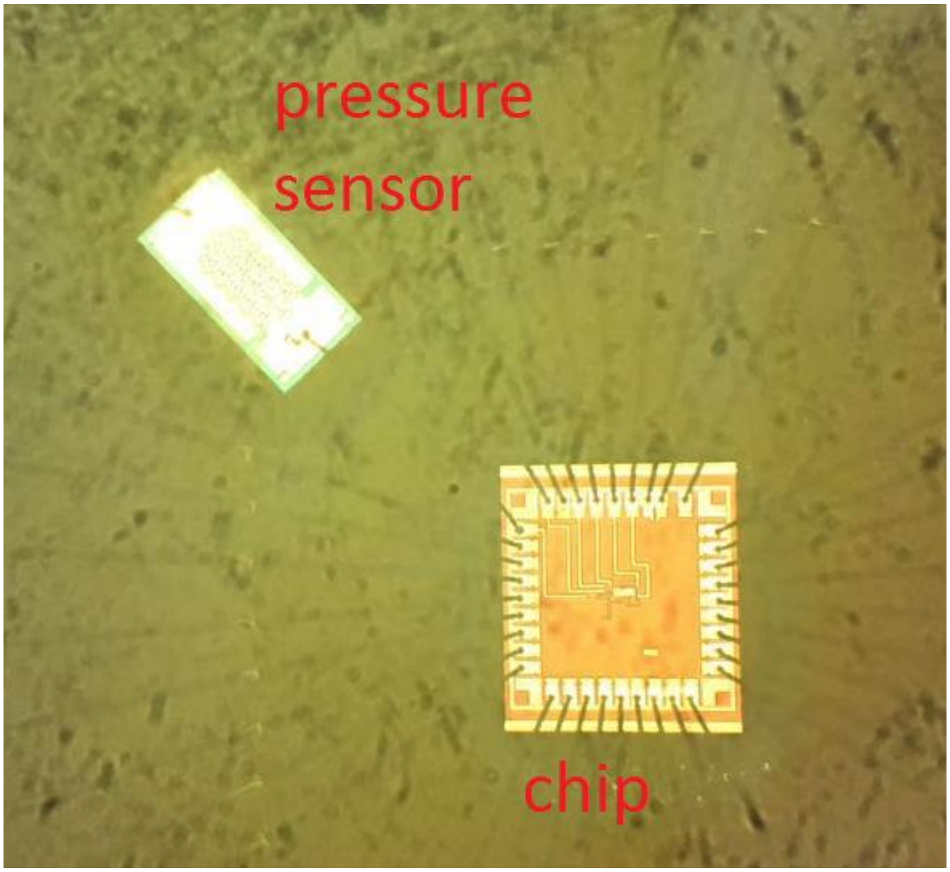

Figure 67 chip and pressure sensor

Figure 68 shows the PCB, the CDC and the pressure chamber. The pressure controller is programmed to control the pressure sweep.

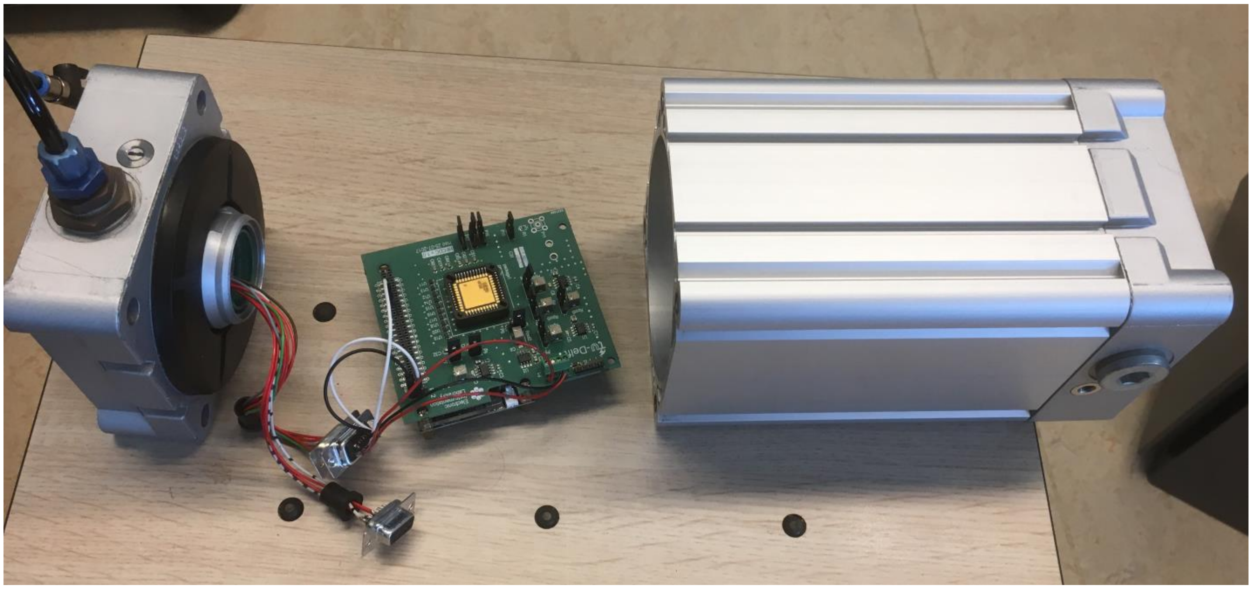

Figure 68 test chamber

Figure 69 is the measured output of the CDC as a function of the applied pressure from 820mbar to 1300mbar. The pressure sweep step is 20mbar/step (9.02fF/step). Each point is the average of around 200 measurements.

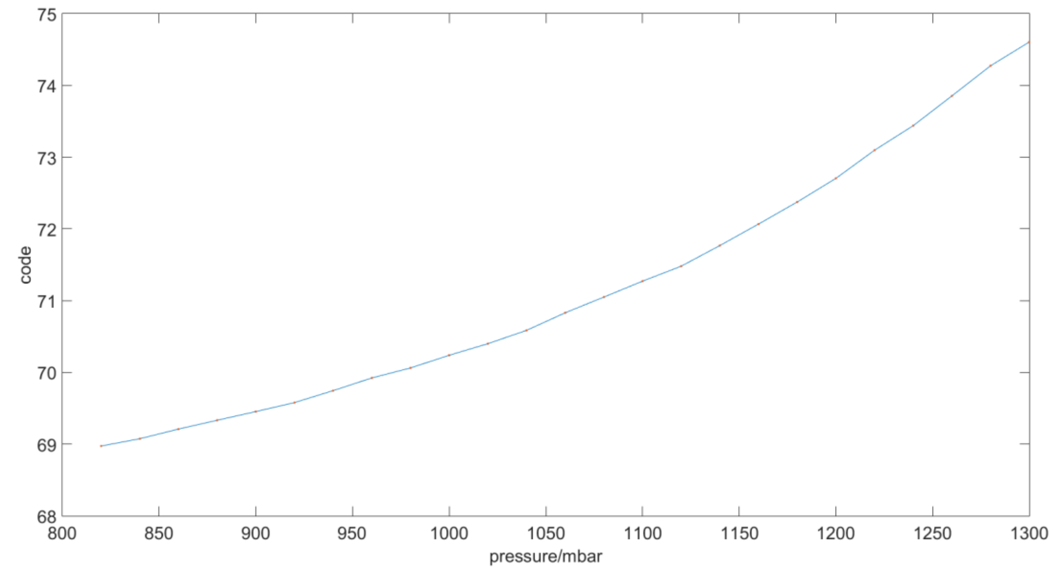

Figure 69 Transfer curve from 820mbar to 1300mbar

Figure 70 shows the standard deviation of the repeated measurements for each pressure level.

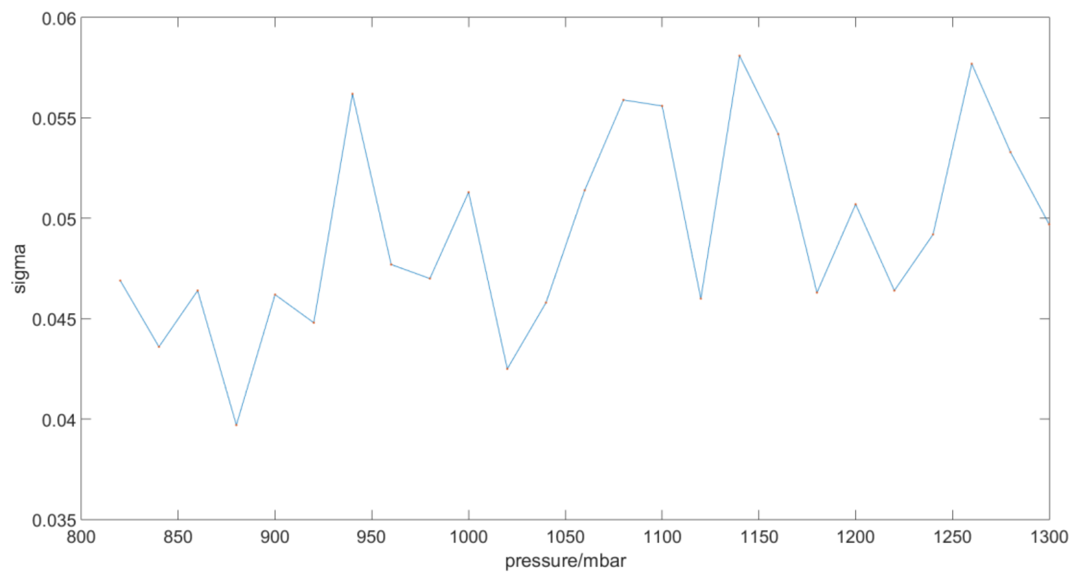

Figure 70 Standard deviation of the repeated measurements for each pressure level

Figure 71 is the measured output of the CDC as a function of the applied pressure from 500mbar to 810mbar in a smaller sweep step size, which also takes more time. The sweep step is 2mbar/step (0.9fF/step). Each point is the average of around 200 measurements.

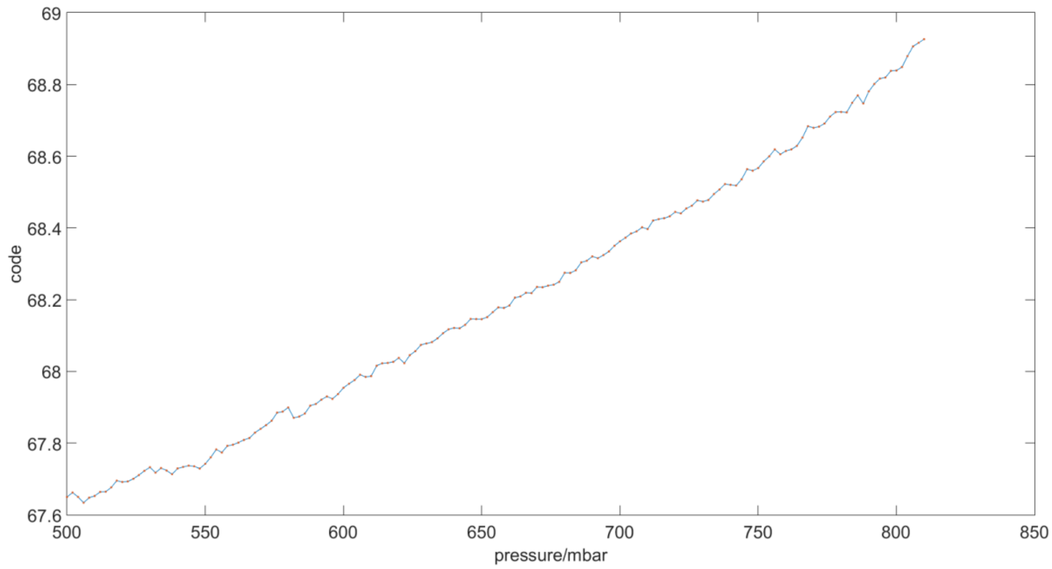

Figure 71 Transfer curve from 500mbar to 810mbar

Figure 72 shows the standard deviation of the repeated measurements for each pressure level. The blue curve shows the standard deviation of the repeated measurements for each pressure level. The red curve is obtained by averaging every 5 successive measurements. According to the datasheet shown in figure 65, the minimum capacitance of the sensor is 5.8 pF at 500mbar, which is slightly larger than the 5.5pF on-chip capacitor. The measurement result at 500mbar is around 67.65, slightly larger than the 63.8 of the on-chip capacitor. That's a reasonable result. In figure 73, the transfer curve from 500mbar to 1300mbar is given, which is similar to the datasheet plots.

The standard deviation from the on-chip capacitor is 0.0318, which is smaller than the standard deviations in pressure measurement (around 0.05). The main reason is that the pump keeps working during the measurement to maintain the pressure in the chamber. So, the noise of the pump is also added up to the standard deviation since the structure of the pressure sensor resembles to a microphone. Also, the small ripples shown in figure 71 are caused by that reason. To prove that the interpolation works without bringing in any discontinuity; further measurements are done with a turned-off pump.

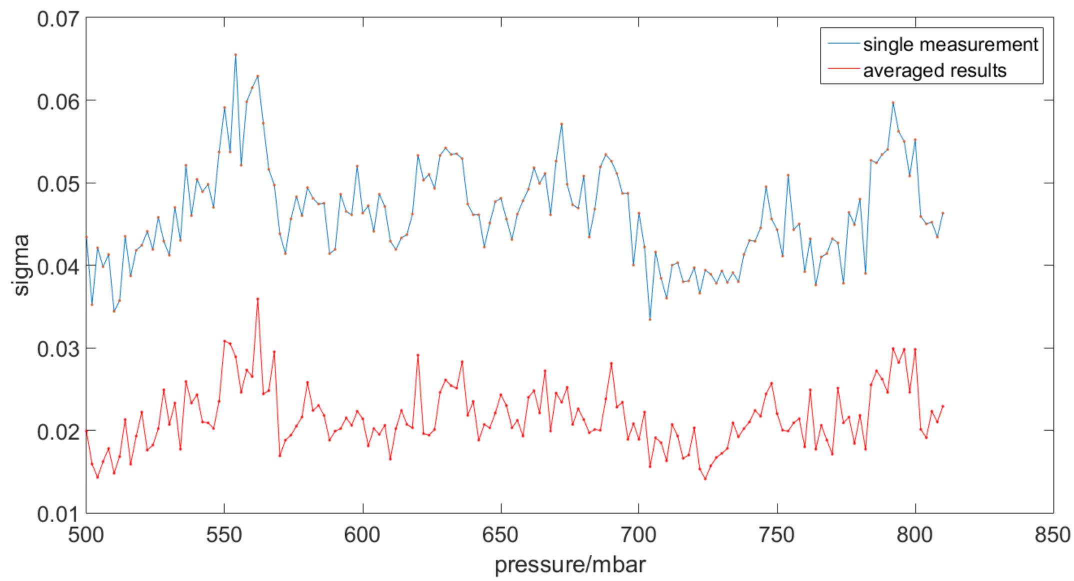

Figure 72 Standard deviation of the repeated measurements for each pressure level

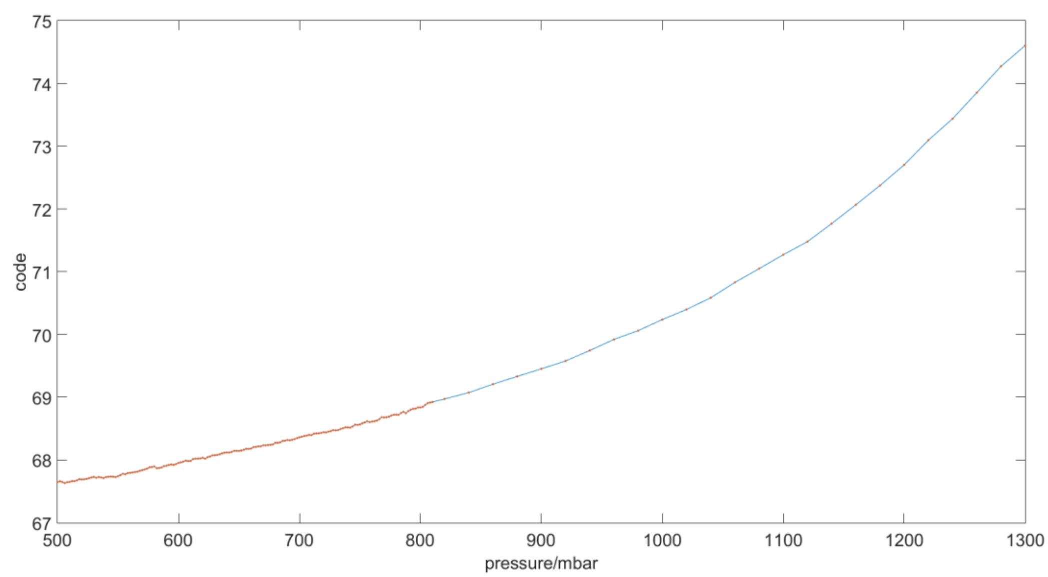

Figure 73 Transfer curve from 500mbar to 1300mbar

Figure 74 and figure 75 are measured with a turned-off the pump. For the measurements shown in figure 74, the pressure is first pumped to 500mbar. Then, the pump is closed. The air leaks very slowly into the chamber and brings it back to the atmospheric pressure. The measurement in figure 75 is also done in a similar way by first pumping the pressure to 1300mbar. Figure 74 and 75 shows that there are no such ripples. Only noise from the circuit itself is shown on the curve.

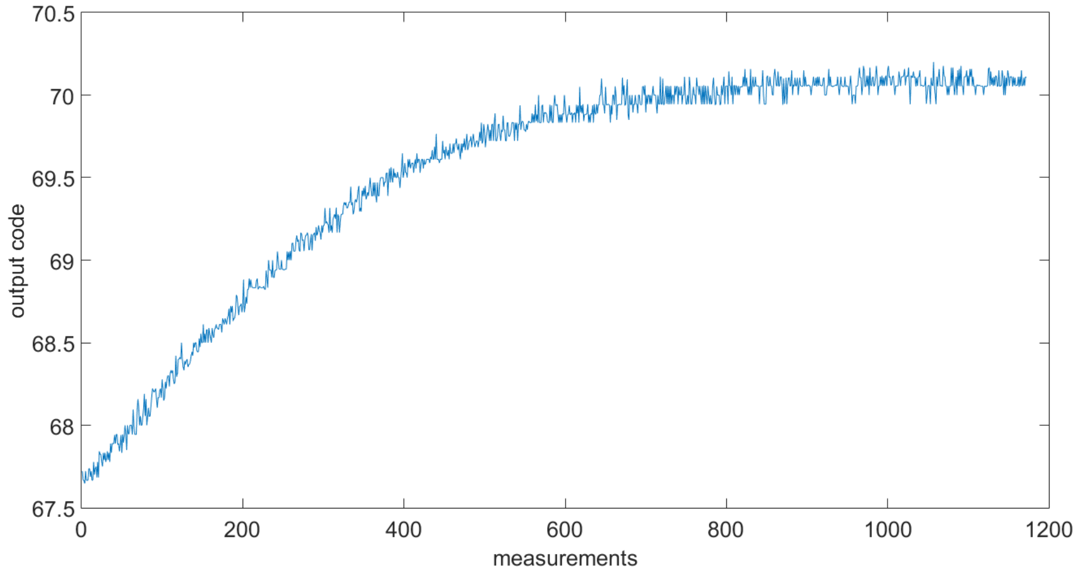

Figure 74 500mbar to atmosphere pressure

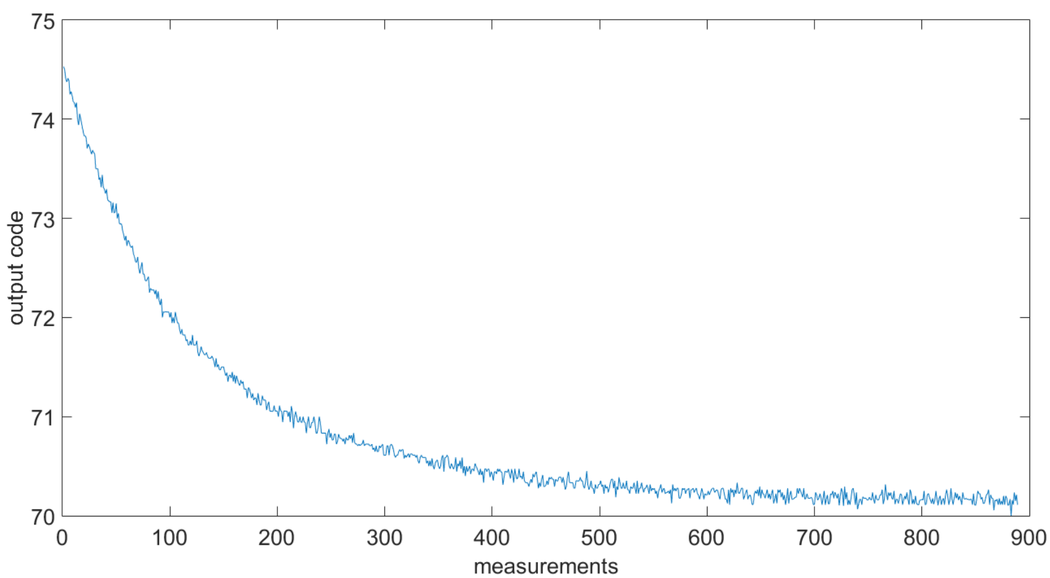

Figure 75 1300mbar to atmosphere pressure

6.3 Comparison with the state-of-the-art

Table 4 Comparison with the state-of-the-art

	This work	ISSCC 2015 [8]	ISSCC 2014 [2]	VLSI 2016 [3]	JSSC 2015 [6]	ISSCC 2015 [7]
Technology (nm)	160	40	180	180	180	160
Method	Digital	Digital	CDS+SAR	SAR	Dual slope	PM
Area (mm^2)	0.012	0.0017	0.49	0.1	0.105	0.05
Range (pF)	5^1	10.6^1	10^2	12.66	4^2	8
ENOB	9	8	8.9	11.7	7	10.6
Resolution (fFrms)	2.8	12.3	6	1.1	8.7	1.443
Conversion time(us)	25	19	4000	16	6400	210
Power(µW)	30	1.84	0.16	7.25	0.11	14
FoM (pJ/Step)	1.32 (@ 5.5pF)	0.141	1.3	0.035	5.3	1.87

1: The range can be very large, but with degraded performance

2: Range with a fixed reference capacitor.

Table 4 gives the comparison with current state-of-art designs. This work achieves the best resolution with a fully digital implementation. Also, the area is smaller compared with designs in similar technology. FoM is calculated based on expressions 4.1, 4.2 and 4.3

$$FOM = \frac{Power \times Conv.Time}{2^{ENOB}} \tag{4.1}$$

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{4.2}$$

$$SNR = 20\log(\frac{Cap.range / 2\sqrt{2}}{rms\_resolution}) \tag{4.3}$$

6.4 Conclusion

In this chapter, the measured function and the performance of the chip have been reported. The chip achieves a resolution of 2.8fF with power consumption of 30µW and a conversion time of 25µs at a 5.5pF capacitance. The FoM of the chip is 1.32pJ/step. A pressure sweep has also been done to check the output with varying capacitance. The comparison with the state-of-arts design is also done.

7 Conclusion

7.1 Summary

The presented work focuses on improving the resolution of the fully digital CDC. Based on Michigan's design [8], a coarse-fine fully digital CDC has been proposed. The coarse conversion is done through a counter. The fine conversion is based on time-domain interpolation, which is realized by a TDC. To know the signal-to-noise ratio of the fine conversion, the jitter and the time step have been analyzed. The TDC is a coarse-fine TDC, which consists of a ring oscillator and a counter. A novel correction circuit is used to fix the non-monotonic issue of such a type of TDC.

The design has been taped-out in a 160nm CMOS process technology. The measurement results show that the time-domain interpolation is functional to improve the resolution. Such interpolation successfully achieves a 1/f noise or drift limited design. By averaging, a sub-femtofarad resolution can be achieved. The resolution is improved from 12.3fF to 2.8fF, compared with Michigan's design in 40nm technology. The maximum measurement range of the proposed CDC is comparable to Michigan's design. The power consumption is 30µW and the conversion time is 25µs at a 5.5pF capacitance. The measured FoM of the chip is 1.32pJ/step. The active area of the chip is 0.012 mm^2. A chip-scale pressure sensor with a range from 500mbar to 1300mbar has been bonded to the chip. A pressure test has been done in a pressure chamber and the CDC is functioning properly in the sensor range.

The main finding of the thesis project is that time-domain interpolation can successfully improve the resolution of a CDC based on iterative discharging. By applying such technology, a high-resolution CDC can be achieved while its fully digital feature can be kept, which is advantageous for the cost and technology migration. The proposed CDC has been shown to be functional and achieves a performance that is in line with the state of the art.

7.2 Future work

For the further improvement of the work, one choice is to move all the digital back-end blocks on chip so that fewer external control signals are needed to operate the CDC. These signals are currently generated by an FPGA. After everything is on chip, since the digital back-end needs an external clock, the chip can also use that clock as the capacitor discharge function. By doing that, the FIFO in the Verilog can also be removed, which can save power and make the chip less complex. Then, the output data can be directly sampled into PC. Also, the waiting time between two measurements can be decreased greatly by doing this since the amount of data that needs to be transferred is reduced and a faster interface can be used than the serial link currently used between the FPGA and the PC.

This is helpful to have less influence from 1/f noise and drift in the final resolution. Also, as a test chip, the supply of the reference and the early detection branch is tunable. It is also good to have them fixed on chip.

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