Testing of Interconnect and Contact Defects in STT-MRAMs

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Testing of Interconnect and Contact Defects in STT-MRAMs

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Abstract

Spin-transfer-torque magnetic random access memory (STT-MRAM) is regarded as one of the most promising non-volatile memory (NVM) technologies, which has the potential to replace the traditional memories in the modern memory hierarchy. Due to some advantages such as non-volatility, fast access speed, low leakage power and high density, more and more research attention is being paid to STT-MRAM. To enable the mass production of STT-MRAM, high-quality and cost-efficient test solutions are the prerequisites. In this thesis, the comprehensive investigation for testing interconnect and contact defects in STT-MRAMs will be presented. The complete defect space for interconnect and contact defects in STT-MRAMs is systematically defined, which are modelled as linear resistors. All theoretically possible faults are defined in a fault space, followed by a methodology to validate these faults under inter-cell magnetic coupling in the presence of defined defects. In this way, accurate fault modelling is performed to guarantee the occurrence of realistic faults in STT-MRAMs. We observed the specific STT-MRAM fault model — passive neighborhood pattern sensitive fault (PNPSF). Based on the fault validation results, an effective march test algorithm(7N) is proposed for interconnect and contact defects in STT-MRAMs.

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1 Introduction

This chapter gives a brief introduction for the topic of this thesis. The motivation of this thesis is firstly provided by going through the rapid development and highlighting enormous potential of STT-MRAM, which brings out the significance of testing of interconnect and contact defects in STT-MRAMs. Next, the problem statement is presented followed by the contribution of this thesis. Finally, the organization of the remaining chapters is shown.

1.1. Motivation

In architecture of the modern computer system, memory unit is regarded as the indispensable component, which works with Central Processing Unit (CPU) to achieve desired function. With the enhancement of CPU's clock rate and the appearance of multi-core processors, the past few decades have seen the significantly improvement of CPU. However, regardless of lower production cost for memories, their performance has been left far behind that of CPU, which results in a huge performance gap between these two main components in computer systems as illustrated in Figure 1.1. The performance bottleneck in memories is called 'memory wall' [1].

In order to achieve better system performance, the memory is expected to be as fast as CPU. As a result of this, a traditional memory hierarchy is designed to make the trade-off between speed and cost per bit, which normally comprises three main stages: cache, main memory and mass storage. Cache is the closest stage to CPU, while mass storage is the farthest one. Cache is small, fast and expensive. On the contrary, mass storage has the highest volume, the lowest speed and the lowest cost per bit. Main memory is placed at the medium stage due to its medium performance and medium cost. In such a memory hierarchy, the trade-off between performance and cost per bit can be made.

Targeted on specific requirements for different stages, different memories have been employed respectively. Since the most recently used data is stored in cache, high access speed is the priority for this stage. Consequently cache is implemented by static random access memory (SRAM), the access latency of which is up to ~1ns [23]. By contrast, memory technology used for mass storage is hard drive disk or flash memory that owns larger volume and lower cost. As the medium stage, main memory is implemented by dynamic

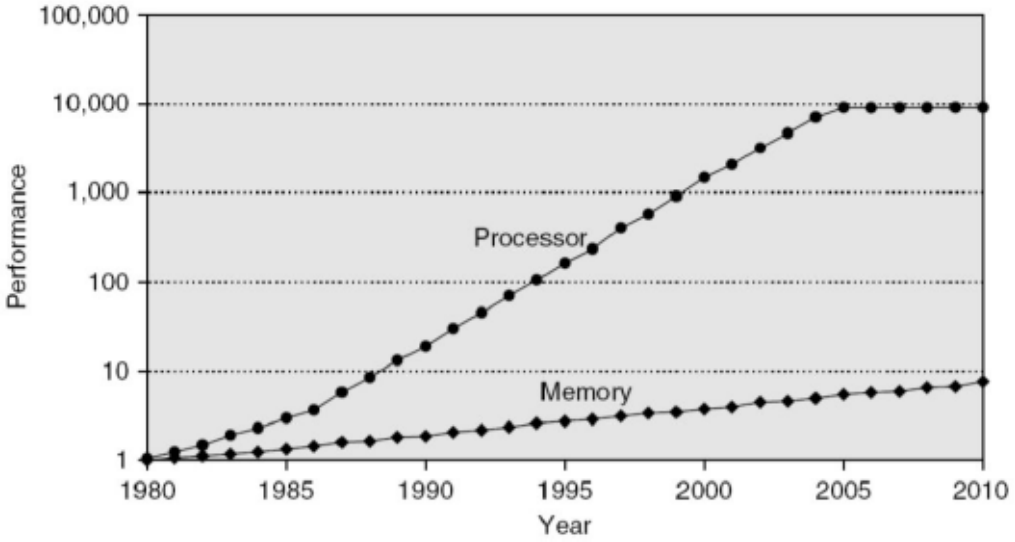


Figure 1.1: The memory wall [1]

random access memory (DRAM) with 50-100 ns access latency [24].

With the technology down-scaling, above mentioned existing memories including SRAM, DRAM, and flash memory gradually approach their limits and become increasingly power hungry, and less reliable [25], while the fabrication cost becomes more expensive due to manufacturing complexity [26]. As a consequence, several emerging non-volatile (NVM) memory technologies are expected to serve as the substitutes for those existing memories in the memory hierarchy. Among these memory technologies, magnetoresistive random access memory (MRAM) family attracts the most intensive R&D attention.

There are three variations in current MRAM family: Toggle MRAM, spin-transfer torque MRAM (STT-MRAM) and spin-orbit torque MRAM (SOT-MRAM). These three generations of MRAM can be utilized in a variety of applications. Compared with the first generation MRAM (Toggle MRAM), STT-MRAM provides larger density, low power consumption, and lower costs as the second generation MRAM. The capacity of scaling STT-MRAM chips to attain larger densities at the cheaper cost is the major benefit of STT-MRAM over Toggle MRAM [27]. As the third generation in the MRAM family, the SOT-MRAM technology is still in the exploratory stage and its potential application is not as wide as that of STT-MRAM due to its properties. Therefore, STT-MRAM is the most promising one of the current MRAM family in recent years. Everspin Technology announced the first STTMRAM chip of 64Mb in 2012 [28] and the industry's first 1Gb pMTJ-based STT-MRAM in 2016 [29]. In 2018, Intel and Samsung also showed off their embedded STT-MRAMs [30, 31]. The core element of STT-MRAM is magnetic tunnel junction (MTJ), the design of which primarily promotes the enhancement of the STT-MRAM technology. In 2011, Samsung developed perpendicular MTJ (pMTJ) that is a type of MTJ at 17 nm. By the end of the year 2016, IMEC researchers reported to develop world's smallest pMTJ at 8 nm [2].

As one of the most promising NVM technology, STT-MRAM has several advantages including non-volatility, high density, fast access speed, high endurance and low static power

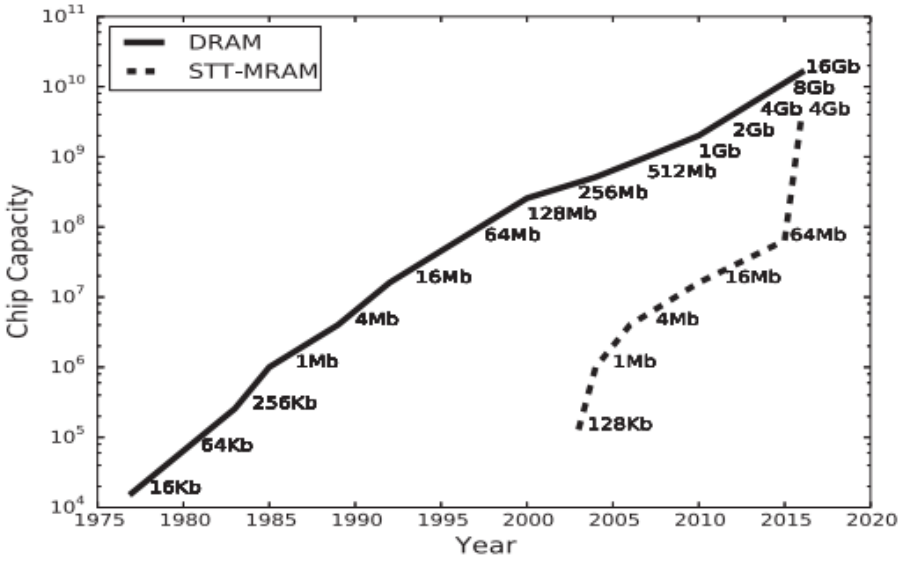


Figure 1.2: Chip capacity development of DRAM and STT-MRAM [2]

consumption compared with the existing memory technologies [6]. More detailed comparison among these memory technologies will be given later in section 2.2.2. Because of these superiorities, STT-MRAM is regarded as the potential universal memory technology in near future. More specifically, STT-MRAM has the potential to replace the mainstream memory technologies in different stages of the memory hierarchy. For example, STT-MRAM can serve as the main memory better than DRAM with comparable read/write latency, non-volatility and lower static power. In order to break the 'memory wall', STT-MRAM technology has been rapidly developing and catching up to the established DRAM technology since 2005 [2].

Figure 1.2 clearly demonstrates the closing gap between these two technologies by depicting an approximation of the chronology of DRAM and STT-MRAM chip capacity growth. With the announcement of 4Gb STT-MRAM chips[32], the capacity gap between STT-MRAM and DRAM dramatically decreases from 2000× in 2003 to only 4× in 2016 [2]. It is predicted that the market size of STT-MRAM is growing from $0.2 billion in 2020 to $2.57 billion in 2028 [33] and the annual shipped capacity will increase to 84PB by 2028 [34]. Therefore, it can be expected that STT-MRAM possibly becomes the real universal memory with maturer technology in near future. At that time, this would unquestionably boost the mass production of STT-MRAM.

During the whole manufacturing process, there possibly exist a variety of physical defects. Since there are large amounts of cells in the memory array, the most common defects are interconnect and contact defects, which can interfere with the internal circuit connections in a printed circuit board (PCB) leading to undesired faults [35]. Faults are the abstract representation of defects [1]. Interconnect and contact defects are randomly occurring regions of extra or missing material in, or between the layers used in the fabrication process [36]. For STT-MRAMs, interconnect and contact defects have not been compre-

hensively investigated, especially under consideration of magnetic coupling, which is the novel property of STT-MRAM. Under this circumstance, the goal of this thesis is to generate the high-quality ensured test solutions for interconnect and contact defects under magnetic coupling in STT-MRAMs.

1.2. Problem Statement

Before the memory chips shipped to customers, the products should be tested to guarantee the good quality. However, the test programs are not able to detect all the chips with defects, which causes test escapes. In other words, it is possible that the defective chips will be delivered to the clients mixed with defect-free chips. When these imperfect products flow into the market, they likely result in a series of problems. After finishing the tasks for a short period of time, the defective chips may break down and will be returned to the manufacturer by customers. The sudden failure of products may cause extremely catastrophic consequences. For example, life losses can be caused by serious car accidents resulted from the test escape chips. Simultaneously, the poor quality of the products has a profound negative impact on the reputation of companies, which may be faced with bankruptcy in this case. Therefore, the defective chips that escape the tests are expected to be weeded out with more effective test programs.

As introduced in section 1.1, STT-MRAM is remarked as one of the most prospective NVM technologies. When the capacity of STT-MRAM chips becomes increasingly larger, the number of the memory cells will show a sharp rise. In this case, the appearance possibility of interconnect and contact defects increases consistently. These defects contribute to diverse faults. If the used test program is able to detect the caused faults as much as possible, more defective chips can be filtered out. Therefore ,in order to reduce test escapes and avoid aforementioned worst consequences, it is of much significance to develop the high-quality and cost-efficient test solutions for STT-MRAMs. Only with test solutions that can reach higher fault coverage, the mass production of STT-MRAMs can be achieved and its huge potential can be unlocked. It is worth noting that the impact of inter-cell magnetic coupling should be taken into account to get realistic fault models, when we investigate interconnect and contact defects in STT-MRAMs. More details will be presented in corresponding chapters of this thesis.

The above gives rise to the problem statement of this thesis: *investigate the fault models in the presence of all possible interconnect and contact defects in STT-MRAMs under inter-cell magnetic coupling and develop the high-quality and cost-efficient test solution.*

1.3. Contributions

The main goal of this thesis is to investigate the fault models attributed to interconnect and contact defects under inter-cell magnetic coupling in STT-MRAMs and develop the effective test solution capable of detecting all the observed faults. The key contribution of this thesis' work is listed as follows:

- **Definition of a complete defect space**: As the most common physical defects, interconnect and contact defects can cause intensive damage for STT-MRAM chips. How-

ever, this type of defects has not been comprehensively investigated. In this thesis, all possible interconnect and contact defects are defined as shorts, opens, bridges in a general manner, in order to promote the accurate fault modelling.

- **Accurate fault modelling**: With the defined complete defect space in STT-MRAMs, the accurate fault modelling will be processed. Firstly, a complete fault space is built up, in which all possible STT-MRAM faults are defined. Next, the realistic faults are validated based on SPICE-based circuit simulation in the presence of defined defects. In order to observe realistic faults, inter-cell magnetic coupling are considered during the simulations. Due to the influence of magnetic coupling, specific STT-MRAM faults are sensitized, which is passive neighborhood pattern sensitive fault (PNPSF).

- **Effective test solution development**: Targeted on the fault validation results from fault modelling, the effective march test algorithm is developed with DBs-based ILP method and sequence-based ILP method. With the proposed algorithm, all EtD faults can be detected. In other words, this test solution is able to weed out the most STT-MRAM chips with interconnect and contact defects. Therefore, the high quality of STT-MRAM chips can be guaranteed.

1.4. Organization

The rest of this thesis is organized as follows:

- **Chapter 2** of this thesis gives a background for our work. Firstly, VLSI test is introduced followed by presenting the evolved memory hierarchy and comparison among memory technologies. Next, we elaborate on the core element (MTJ) of STT-MRAM and the electrical model of STT-MRAM circuits. Finally, an overview of STT-MRAM test development is given.

- **Chapter 3** of thesis illustrates how to define all possible interconnect and contact defects in STT-MRAMs. These defects are classified into three groups: shorts, opens and bridges, all of which are modeled as linear resistors.

- **Chapter 4** of this thesis firstly defines the complete memory fault space for STT-MRAMs. Then we explain the used test circuit and how we consider the inter-cell magnetic coupling in circuit simulation setups. Finally the methodology of fault validation is presented.

- **Chapter 5** of this thesis firstly shows the results of fault validation. Then we did some analysis for these results to reveal the influence of inter-cell magnetic coupling on the faults caused by the predefined defects in chapter 3. Some specific STT-MRAM faults are observed. Lastly, a simple comparison is made between the realistic faults in our work and the existing fault models caused by interconnect and contact defects in previous works.

- **Chapter 6** of this thesis generates the test solution aimed for all detected EtD faults based on DBs-based ILP method and sequence-based ILP method. Then the pro-

posed march test algorithm is verified by applying it to the test circuit. Finally, a simple comparison is made between our proposed algorithm and the existing algorithms for interconnect and contact defects in STT-MRAMs.

- **Chapter 7** draws the conclusion of the thesis project followed by some potential points that can be investigated more deeply as the future work.

2

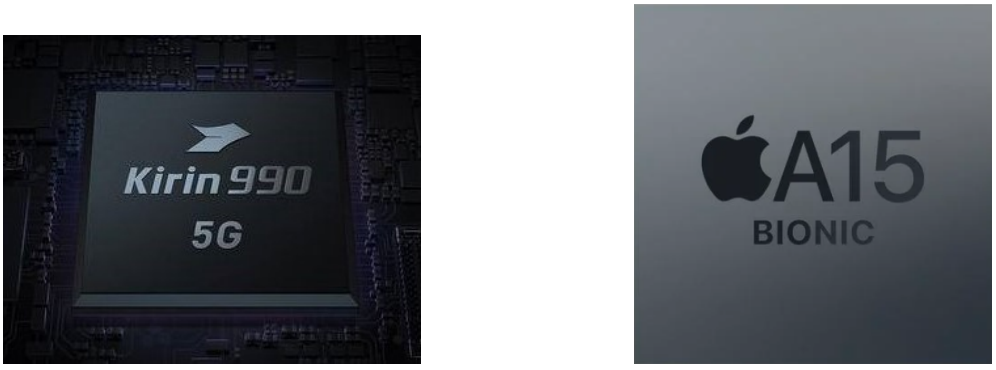
Background

This chapter gives a background of the work for this thesis. It starts with introducing the basic conceptions of VLSI test and emphasizing its significance. Next, we present the modern memory hierarchy, after which a variety of memory technologies are compared together. Then, the core element of STT-MRAM named Magntic Tunnel Junction (MTJ) is discussed in detail, followed by the introduction for the used electrical STT-MRAM model in this thesis. Finally, an overview of STT-MRAM test development is presented from three aspects: defects, fault models and test algorithms.

2.1. VLSI Test Philosophy

This section firstly highlights the indispensable role of the VLSI test for complicated electronic components and systems in their lifetime. Thereafter, some key conceptions in tests such as test escapes are explained in detail.

2.1.1. Role of VLSI Test



(a) (b)

Figure 2.1: Illustrations of the state of art SoC: (a) Kirin 990 5G processor [3], and (b) A15 processor [4]

In the past several decades, very large scale integration (VLSI) has been rapidly devel-

oped, which contributes to the growing practical complication of electronic components and systems [37]. In these complex components and systems, semiconductor chips play an important role in functionality achievement. As one of the most well-known and the most popular electronic systems in the modern society, smartphones comprise a variety of semiconductor chips, the most significant one of which is system-on-chip (SoC). A SoC is an integrated circuit that includes all or most components of electronic systems [38]. On SoC of the smartphones, there exist the central processing unit (CPU), on-chip memories, the neural processing unit(NPU), radio modems and the graphics processing unit (GPU) etc., – all on a single substrate or microchip [39].

Figure 2.1a and 2.1b shows two mainstream SoC chips in smartphones, respectively. Kirin 990 5G processor is a 64-bit high-performance mobile ARM 5G SoC designed by HiSilicon introduced in September 2019 [40], which is built with 10.3 billion transistors in a single chip of 113.31mm^2 using TSMC's 7nm process [41]. A15 chip is a 64-bit ARM-based SoC designed by Apple Inc, which integrates 15 billion transistors using TSMC's 5nm process [42]. Obviously, it is likely that defects will happen during the manufacturing process of such a intricate chip. As a result of this, in order to guarantee the quality and reliability of semiconductor chips, it is essential to rigorously test them in different effective methods at different phases of their lifetime [5].

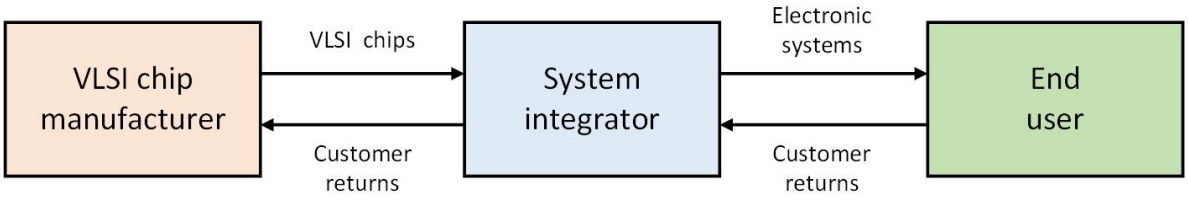


Figure 2.2: Supply chain of VLSI chips

The typical supply chain of VLSI chips is illustrated in Figure 2.2, which comprises three key phases. VLSI chip manufacturers are involved in the first phase, where various specifications for chips are specified followed by the chip design and fabrication. The second phase is about the integration of a variety of components in the electronic systems including SoC chips etc.. The most commonly used digital products are produced in this phase such as smartphones, laptops and tablets etc.. In the final phase, the products are delivered to the customers to execute desired functions until breakdown.

During all of these three key phases of chips' supply chain, different types of tests for the products are carried out. The most critical test process is carried out in the first phase, in order to detect the defective chips in the earlier phase. In this way, most defective parts can be weeded out and the outgoing parts shipped to customers can be guarantee to perform desired functions [5]. System test and on-line test are respectively carried out in the second and third phase. If the defective products are identified, they will be delivered back for repair and analysis.

Although tests in last two phases are much of significance as well, the quality of chips are expected to be ensured by chip manufacturers. The first reason is the test cost. A widely accepted rule of thumb in test economics in the electronics industry is the rule of ten [43]. It

suggests that if a defective chip is not detected by chip level testing, finding it at the printed circuit board level costs ten times more than at the chip level [6]. Another reason is about the reputation of companies. The defective products may cause a devastating blow to the manufacturers' reputation. Therefore, VLSI test in the first phase attracts the most intensive R&D attention and the work in this thesis focuses on the chip test in this phase.

2.1.2. Key Concepts of VLSI Test

By the end of the first phase in the supply chain of VLSI chips. the manufactured chips will be divided into four sets based on two conditions. The first condition is the outcomes of the production test: **pass** or **fail**. The production test is a short and go/no-go decision-making process targeted on each chip after the manufacturing process, in order to guarantee high quality of chips shipped to the customers. **Pass** means the manufactured chips pass the production test, while **fail** means the products do not meet the requirements. Although the results of the production test ensure that the most defective chips will be weeded out, some chips with defects can still escape with the tests. Therefore, the second condition is used to point if the chips are actually defective or not after manufacturing process: **OK** and $\overline{\textbf{OK}}$. **OK** stands for the defect-free chips, while $\overline{\textbf{OK}}$ represents those with physical defects. Therefore, the four sets of manufactured chips are listed as shown in Figure 2.3:

① **Pass** & **OK**: the set of defect-free chips, which pass the production test.

② **Pass** & $\overline{\textbf{OK}}$: the set of defective chips, which pass the production test.

③ **Fail** & $\overline{\textbf{OK}}$: the set of defective chips, which fail the production test.

④ **Fail** & **OK**: the set of defect-free chips, which fail the production test.

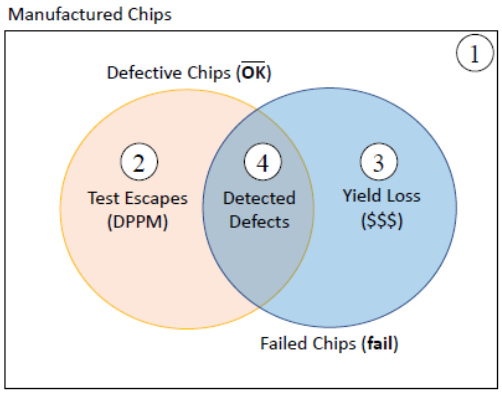


Figure 2.3: Four sets of manufactured chips [5]

Set ② and Set ③ express two crucial concepts of VLSI test: test escapes and yield loss. Set ② involves the chips that are indeed with defects, but are missed out by the test program. The possible reason for test escapes is the incompleteness of the test program. More

specifically, not all defects that happen in the chips are represented by the existing fault models covered by the test program. Fault models are the representation of certain physical defects at the abstracted function level [43]. These chips escaping the test are delivered to the customers along with those in set **1** that are indeed qualified products without defects. Due to the undetected defects, chips in set ② may wear out and will be returned from the users, which is called customers returns. Therefore, test escapes not only increase the manufacturing costs, but also have a negative impact on the reputation of companies.

Set ③ contains the indeed defect-free chips that fail the tests, which corresponds to the definition of yield loss. This is because some tests are excessively rigorous to eliminate a couple of good chips. For example, some defect-free chips are possibly discarded as defective ones by I_{DDQ} test due to inaccurate identification of mounted leakage current, which is recognized as defects [43]. It is obvious that yield loss increases the manufacturing cost as well.

Compared with above two sets (test escapes & yield loss), set ① and set ④ are actually the desired sets for manufacturers under ideal conditions. In other words, manufacturers expect that all chips labeled with **OK** will pass the tests, while those labeled with $\overline{\mathbf{OK}}$ will be weeded out. Therefore, reducing the test escapes and yield loss are the goals of R&D investment all the time.

2.2. Memory Technologies

As briefly mentioned in section 1.1, the existing memories such as SRAM, DRAM, and flash memory have encountered some challenges with technology down-scaling. For example, the issues with row hammer have a negative impact on the DRAM devices [44], if the feature sizes are continuously shrunk. For flash memories, string current will be undoubtedly influenced with the further scaling-down, making the implementation of sense operations more challenging [44]. Therefore, the emerging memory technologies attract increasingly intensive R&D attention. It is expected that some of them have enormous potential to take the place of the existing memory technologies to break the memory bottleneck.

In this section, the present memory hierarchy is firstly presented, followed by the comparison among various memory technologies.

2.2.1. Present Memory Hierarchy

As the indispensable component of modern computer systems, semiconductor memories are being paid attention increasingly. In section 1.1, the traditional memory hierarchy has been introduced, which is composed of three stages: cache, main memory and mass storage. The goal of this hierarchy is to break the 'memory wall', which is the huge performance gap between CPU and memory.

In the traditional memory hierarchy, SRAM is responsible for the implementation of cache and DRAM is utilized to serve as main memory. Mass storage is implemented by hard drive disk that has high volume and low cost per bit. With this type of hierarchy, the performance gap between CPU and memory becomes not so wide to some extent. However, the performance difference is still one of the bottlenecks in modern computer systems.

Consequently, it is necessary to update this memory hierarchy further to reach better

performance from various aspects. For instance, the more suitable memory technologies are expected to be discovered for each stage in the memory hierarchy. For cache, the high access speed is the most significant property. Therefore, the memory technology can be considered as the substitutes for SRAM, if its access latency is lower than that of SRAM or it owns comparable access speed as SRAM, but with lower cost per bit. The emerging memory technologies make this direction possible.

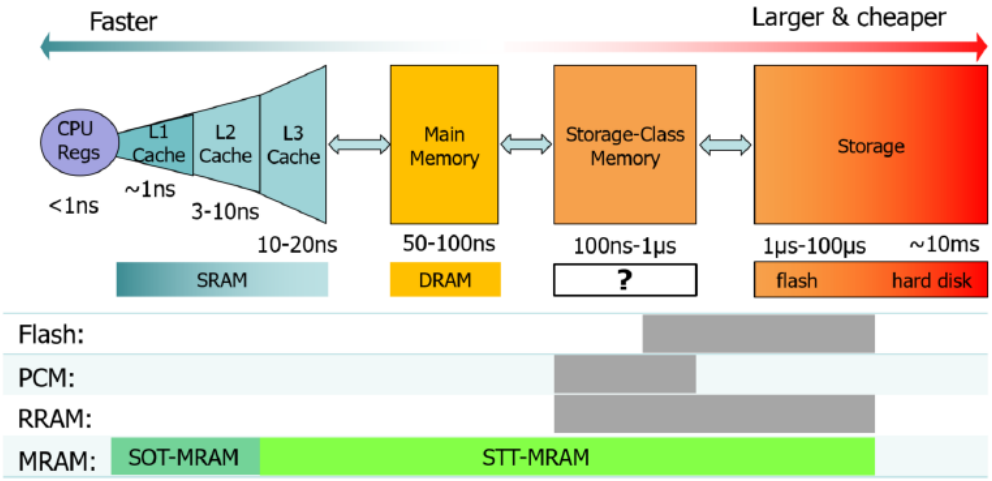


Figure 2.4: Present memory hierarchy [6]

Adapted with emerging memory technologies in the past years, traditional memory hierarchy is gradually stepping towards evolution as well as illustrated in Figure 2.4. The stage of Cache is divided into three levels: L1 cache, L2 cache and L3 cache. The main differences among these three levels of caches are access speed and volume. For example, L1 cache is faster than L2 cache, while the volume of L2 cache is larger than that of L1 cache [45]. Apart from the optimization in cache, the performance of mass storage has been considerably improved due to the presence of flash memory. Compared with hard disk driver, the access latency is significantly reduced in flash memory [46]. It is worth noting that an extra stage named storage-class memory (SCM) [47] is proposed for further improvement. The existence of SCM narrows down the performance gap between main memory and mass storage. For this stage, one of the solutions is hybridizing flash memory with DRAM [48].

As alternatives for the SCM, several emerging NVM technologies are predicted to be promising and attract comprehensive R&D attention. In Figure 2.4, the suitable stages of the memory hierarchy are clearly illustrated for several NVM technologies. Phase-change memory (PCM) is anticipated to be candidates for SCM stage, while resistive random access memory (RRAM) is able to serve as SCM and mass storage [49]. Compared with PCM and RRAM, magnetic random access memory (MRAM) is predicted to cover more stages in memory hierarchy, which means MRAM family including sub-classes with different flavors has the potential to be the true universal memory technology in the future [50]. Spin-orbit torque MRAM (SOT-MRAM) owns the potential to replace SRAM in first two levels of caches, while STT-MRAM is suitable for L3 cache and below. Next, the comparison among

all above mentioned memory technologies is made aimed at various metrics.

2.2.2. Comparison among Memory Technologies

As shown in Figure 2.5, memory technologies can be categorized into different types base on different standards of classifications. Volatile and Non-volatile memory technologies can be distinguished by the necessity of constant power supply when keeping the stored data [49]. Volatile memories are able to maintain the stored, only when the power is on. By contrast, non-volatile memories are capable of retaining the data without power supply. Both SRAM and DRAM belong to volatile memories. Non-volatile memories include flash memory, PCM, RRAM and MRAM.

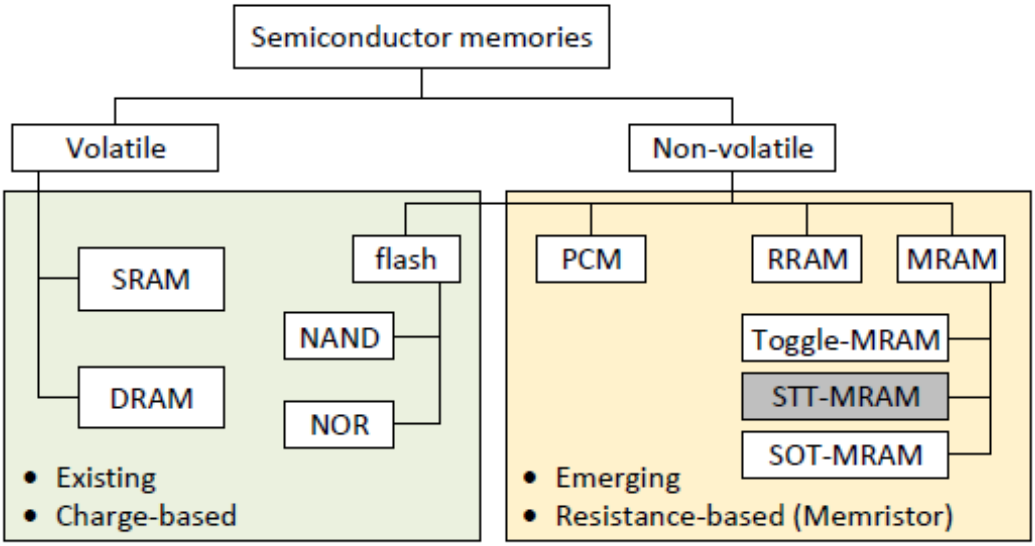


Figure 2.5: Classification of memory technologies [6]

Besides, memory technologies are classified into two groups: charge-based memories and resistance-based memories according to general working principles. The main existing memories are charged-based memories including SRAM, DRAM and flash memory, in which the electric charge is used to represent binary logic value in computer systems. By contrast, the representation of logic '0' and '1' in resistance-based memories relies on the resistance value of the device. Several emerging memories including PCM, RRAM and MRAM belong to this category. Note that there are three generations in MRAM family: Toggle-MRAM, STT-MRAM and SOT-MRAM. The focus of this thesis is STT-MRAM, which has been promoted into commercialization with a small scale by worldwide semiconductor companies such as Intel, Samsung, Globalfoundries, and Everspin in recent years [51, 52].

In Table 2.1, various metrics of aforementioned memories are presented. SRAM has the fastest access speed among the existing memory technologies, while SOT-MRAM has comparable access latency as the emerging NVM technology. Compared with SOT-MRAM, the large cell size and volatility are disadvantages of SRAM. However, manufacturing technologies of SOT-MRAM is still not mature, the possible solutions of which were first demon-

Table 2.1: Comparison among various memory technologies [6, 20–22]

Metrics \ Memory	SRAM	DRAM	NOR FLASH	NAND FLASH	PCM	RRAM	Toggle MRAM	STT MRAM	SOT MRAM
Cell Size (F^2)	~150	~8	10	5	6-12	6-10	20-30	6-10	10
Non-Volatility	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Write time	~1ns	~30ns	~500us	~200us	100ns-10us	10ns-100us	~35ns	5-100ns	~1ns
Read time	~1ns	~30ns	~5us	~50us	20-50ns	10-50ns	~35ns	~5ns	~1ns
Endurance	10^{15}	10^{15}	10^5	10^5	10^6-10^9	10^5-10^9	10^{15}	10^{15}	10^{12}

strated by IMEC until 2019 [53].

The second-generation MRAM: STT-MRAM owns low write time (5-100ns) and read time (~5us) that nearly approach the speed of SRAM and has better performance than DRAM. Apart from this, the static power of STT-MRAM is sufficiently lower than that of SRAM and DRAM, which respectively result from leakage current and continuous refreshing. Besides, non-volatility of STT-MRAM makes it more competitive than those existing memories. Based on these merits, STT-MRAM is predicted to serve as main memory and the last level cache. Compared with the second and the third generation in the MRAM family, the performance of the first generation (Toggle-MRAM) is not outstanding enough, the cell size and access speed of which is marginally lager than other sub-classes in MRAM.

As mentioned in section 2.2.1, PCM and RRAM are expected to take the responsibility for the SCM stage in the updated memory hierarchy to compensate for the wide gap between the main memory and mass storage. Corresponded with this anticipated position in memory hierarchy, the access speed of PCM and RRAM is higher than that of flash memory that serves as mass storage, but lower than that of DRAM that is the core element of main memory. The drawback of PCM and RRAM is the slightly larger cell size than NAND flash. Although there already exist some solutions to enlarge the density of PCM and RRAM such as 3D stacking and novel architecture (1D1R-1R1D) [54, 55], more techniques are still needed to further improve this merit for these two NVM technologies.

After the comparison among the memory technologies listed in Table 2.1, it can be concluded that STT-MRAM is well qualified for various stages in the present memory hierarchy. Compared with other memory technologies, STT-MRAM possesses a couple of superiorities: non-volatility, high access speed, high density, high endurance and low power consumption [25], which makes it one of the most promising memory technologies. It is predicted that the market size of STT-MRAM is growing from $0.2 billion in 2020 to $2.57 billion in 2028 [33] and the annual shipped capacity will increase to 84PB by 2028 [34]. STT-MRAM is still unable to take the place of DRAM and SRAM, since the manufacturing technology are not as mature as that of the existing memories. In spite of this, STT-MRAM has the enormous potential to improve the performance of memory units in the near future. Therefore, we aim to generate high-quality and cost-efficient test solutions for STT-MRAM in this thesis.

2.3. MTJ Technologies

In this section, we elaborate on the cole element of STT-MRAM: magnetic tunnel junction (MTJ). Firstly, the structure of MTJ is presented. Next, the working principles of this device

is explained in detail.

2.3.1. MTJ Structure

MTJ is the core element of STT-MRAM, which is responsible for storing data in the form of resistance. As illustrate in Figure 2.6, the simplest structure of MTJ only consists of free layer (FL), tunnel barrier (TB) and reference layer (RL). However, this simple design causes undesired magnetostatic interactions between the RL and the FL, which possibly makes the magnetization of the RL biased in the inverse direction with the FL [7].

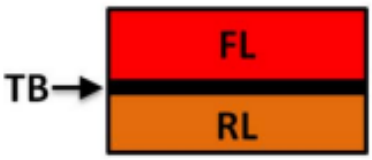


Figure 2.6: Simplest design of MTJ [7]

Therefore, the design of MTJ is expected to be improved further to get rid of the undesired interlayer magnetic coupling. There are two types of optimized MTJ structures: in-plane magnetic anisotropy (IMA) MTJ and perpendicular magnetic anisotropy (PMA) MTJ, which are distinguished by the direction of easy axis. The easy axis of the former lies in the thin film (i.e, horizontal direction) [56], while that of the latter lies along the perpendicular direction of FL. There exists synthetic antiferromagnet (SAF) structure in both of them to provide the stable reference magnetic direction for FL and eliminate the undesired interlayer coupling [57]. Since PMA-MTJ is more superior than IMA-MTJ with much more advantages such as better scalability to smaller sizes and smaller switching current [7], we only focus on PMA-MTJ in this thesis and present more detail next.

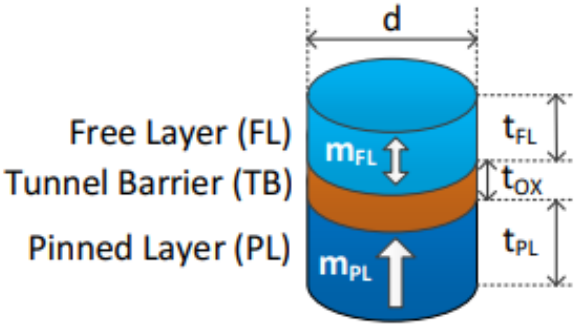


Figure 2.7: Simplified schematic of PMA-MTJ [8]

As shown in figure 2.7, the structure of PMA-MTJ comprises of three layers [56]: FL, TB and pinned Layer (PL). FL is the top ferromagnetic layer usually made of CoFeB material, the role of which is to store data based on the relative magnetization direction with PL. Compared with FL, the structure of PL is more complicated. It contains reference layer (RL)

and hard layer (HL). The former is usually formed by Co/spacer/CoFeB multilayers, while the latter is made of $[Co/Pt]_x$ [19]. These two layers constitute the SAF structure, where the magnetization of RL is fixed by HL. The typical thickness of FL and PL are respectively ~ 1.5nm and ~ 2.5nm [58].

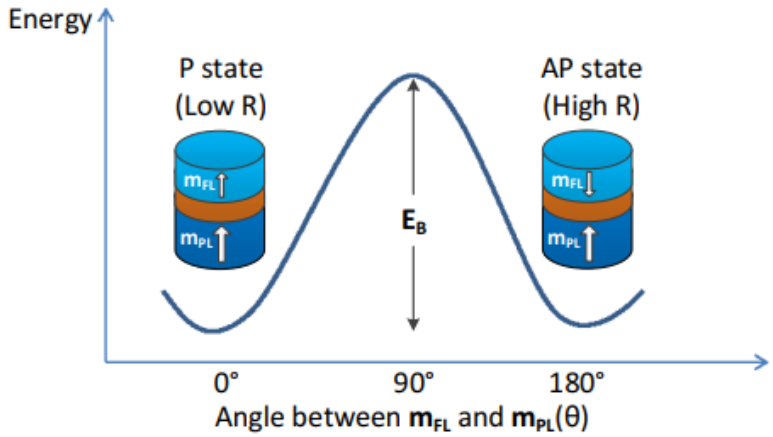


Figure 2.8: Two states of MTJ: AP and P state [9]

In Figure 2.7, m_{FL} and m_{PL} respectively represent the magnetization of FL and PL. The middle non-magnetic insulating MgO layer is TB that is ultra-thin(~ 1nm) [58]. The characteristics of the MTJ device are similar to those of a tunneling resistor with electrons overcoming the potential barrier height $\overline{\varphi}$ to tunnel through the TB [9]. The resistance-area (RA) product [56] is employed to present the difference of sheet resistance of various MTJ devices regardless of device sizes. In the MRAM community, electrical critical diameter (eCD) is used to stand for critical diameter (CD) with consistent qualities throughout the device, since slight difference exists between the edge and the internal area of MTJ devices.

As aforementioned, the data-storing capability of MTJ is attributed to relative magnetization configurations between FL and PL. More specifically, when magnetization direction of FL is parallel to that of PL, the resistance of MTJ is low and it holds in parallel (P) state as shown in figure 2.8. Oppositely, anti-paralell (AP) state stands for high resistance of MTJ with the same magnetization directions of FL and PL. These two states P and AP respectively correspond to logic '0' and '1'. The resistance difference between P and AP states results from tunneling magneto-resistance effect (TMR) [59], which will be explained in more detail in 2.3.2. To switch from one state to another, electrons need to overcome the energy barrier (E_B) with the applied current as illustrated in Figure 2.8.

2.3.2. Working Principles

As the promising memory technology, STT-MRAM is capable of retaining data, reading data and writing data. These three functionalities are achieved relied on MTJ devices that are the core element of STT-MRAM. Next, We shall go into further depth about them and explain the corresponding physical mechanisms behind them in detail.

data retaining
Data retaining means that the data stored in the memory shall be kept stable for the required time named retention time. The retention time of MTJ depends on thermal stability (Δ). Δ is defined as follows [7]:

$$\Delta = \frac{E_B}{k_B T} = \frac{\mu_0 M_s V H_k}{2 k_B T} \tag{2.1}$$

where E_B is the energy barrier between AP and P states as shown in Figure 2.8, k_B the Boltzmann constant, μ_0 the vacuum permeability, M_s the saturation magnetization, V the volume of FL and H_k the magnetic anisotropy field. The expression of retention time is given in [60] as follows:

$$t_{ret} = \tau_0 exp(\Delta) \times \frac{1}{1 - P_{ret}} \tag{2.2}$$

where τ_0 is the inverse of the attempt frequency and P_{ret} is switching probability attributed to thermal fluctuation after retention time. As presented in equation 2.2, the higher the thermal stability is, the longer the retention time will be. For example, when Δ is 80, the retention time will be longer than 10 years [7]. By contrast, if Δ of a MTJ device is around 40, the associated retention time is only approximately 7.4 years[60]. Although the larger Δ contributes to longer retention time, it can not be neglected that larger thermal stability imposes a negative impact on write latency of memory. As a result of this, the specification of thermal stability is customized aimed at the need of diverse applications.

data reading
Apart from data retaining, the functionality of data reading is indispensable for memory cells as well. For MTJ devices, the ability of reading out value in memory cells is attributed to TMR effect. TMR effect means that different relative magnetization direction between FL and PL results in different value of MTJ resistance [61]. As illustrated in Figure 2.8, when m_{FL} and m_{PL} are in the same direction, the resistance of MTJ will be low corresponded to P state. Oppositely, MTJ in AP state has high resistance, when the magnetization of FL and PL are relatively inverse. The following equation [25] defines TMR ratio in order to express it qualitatively:

$$TMR = \frac{R_{AP} - R_P}{R_P} \times 100\% \tag{2.3}$$

where R_P and R_{AP} respectively present MTJ resistances of P and AP state. It is obvious that when difference value between R_P and R_{AP} is larger, TMR ratio will be larger. In other words, P and AP state can be more easily distinguished with larger TMR ratio. A minimum TMR ratio of 150 % is needed for MTJ devices to be economically viable [7].

To go further depth into TMR effect, we firstly introduce the distribution of electrons' spin states in MTJ. For electrons, there are two spin states: up-spin and down-spin. In normal metal, the number of up-spin electrons and down-spin electrons are equal, while there exists difference between them in ferromagnetic (FM) material due to impact of magnetization. In FM material, the number of electrons, whose spin direction is same with FM's magnetization, is much greater than that of those with inverse spin direction. The spin

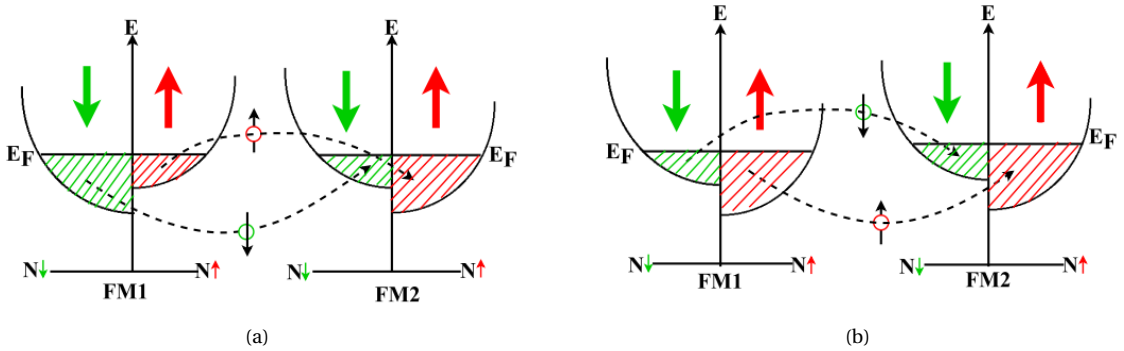


Figure 2.9: Band structure model for interpretation of TMR effect [10]: (a) AP state, and (b) P state

polarization of FM is expressed with the following equation [62]:

$$P = \frac{N_\uparrow - N_\downarrow}{N_\uparrow + N_\downarrow} \tag{2.4}$$

where $N_\uparrow$ and $N_\downarrow$ respectively represent the number of up-spin electrons and down-spin electrons. Spin-dependent tunneling, in which down-spin electrons can only tunnel into down-spin states and up-spin electrons can only tunnel into up-spin states, is the underlying mechanism of the TMR effect [63].

As illustrated in Figure 2.9a, MTJ devices are kept in P state. FM1 and FM2 correspond to FL and PL respectively. The magnetization directions of FL and PL are completely inverse, which means majority spin states in FL and PL are opposite. Therefore, after tunneling through TB layer, the majority spin states of outgoing electrons from PL are unable to fill in majority states of FL, which contributes to poor conducting ability. This is the reason why AP state of MTJ devices has high resistance. By contrast, the majority spin states of FM1 can fill in the majority spin states of FM2, while the minority spin states of FM1 can fill in the minority spin states of FM2 under P state of MTJ devices in Figure 2.9b. Consequently, there will be higher current passing through MTJ devices.

data writing

The functionality of data writing is that the desired data such as logic '0' or '1' can be written into the addressed memory cells, which is achieved by spin-transfer torque (STT) effect [7]. The free-electron model shown in Figure 2.10 is used to interpret the mechanism of STT effect.

As aforementioned, electrons possibly have different spin directions. Therefore, the incoming current contains large amounts of electrons with diverse spin states, when the voltage is applied to MTJ devices. When these electrons arrive at RL, all of them will be polarized to the same direction with magnetization of RL. These repolarized electrons constitute the spin-polarized current in Figure 2.10. After passing through TB layer, spin-polarized current enters the FL, magnetization of which may be not identical with that of RL. Therefore, the polarized electrons by RL will be polarized by FL again to produce the outgoing spin-polarized current. Since the momentum is conserved, the magnetization of FL will be

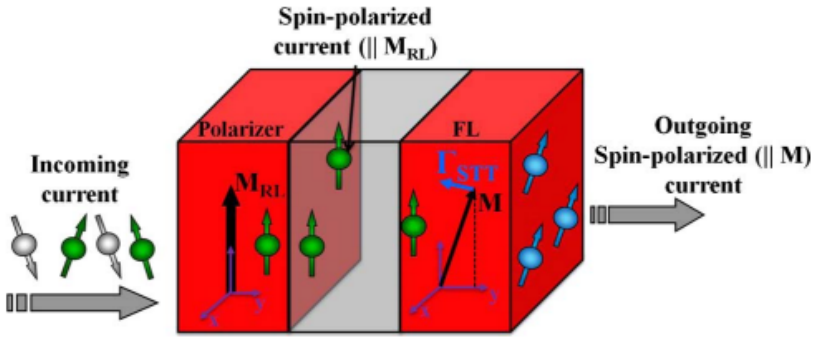


Figure 2.10: Free-electron model for spin transfer torque [7]

inversely influenced by the torque induced by the change between incoming current and outgoing current. With this torque, FL magnetization may change to the inverse direction compared with the initial direction. In this way, the switching process of AP to P or P to AP will be successfully carried out. Figure 2.10 presents AP to P switching process.

For switching process in MTJ, there are two significant parameters: I_c and t_w. I_c is critical switching current of MTJ, which is the required minimal current to flip device's state over an endlessly long period of time [56]. t_w is the switching time [9], which is the time required for the switching process. The expression derived in [62] for switching current (I_c) is given here as follows:

$$I_c = 2\alpha \frac{\gamma e}{\mu_B \cdot g} E_B \tag{2.5}$$

$$g = \frac{\sqrt{TMR \cdot (TMR+2)}}{2\,(TMR+1)} \tag{2.6}$$

where α is the Gilbert damping, e the electron charge, γ the the gyro-magnetic ratio, μ_B the Bohr magneton and g the spin polarization efficiency factor calculated by TMR ratio.

In order to facilitate the switching process, the current is expected to be applied on MTJ. The switching process will be faster with higher applied current. Apart from magnitude of the applied current, the pulse width (t_p) of the current plays a significant role in the switching process as well [64]. In [65–67], two types of switching process are distinguished by t_p of the applied current: precessional regime and thermal activation regime. In the precessional regime ($t_p < 40ns$), STT effect contributes to the flip of FL magnetization to realize the switching process and the magnitude of the applied current must be higher than I_c. Sun's model [68] is used to evaluate the switching time (t_w) in this regime as following equation:

$$\frac{1}{t_w} = \frac{2}{C + \ln\left(\frac{\pi^2 \Delta}{4}\right)} \cdot \frac{\mu_B P}{e \cdot m\left(1+P^2\right)} \cdot (I - I_c) \tag{2.7}$$

where C is the Euler's constant, P the spin polarization, m the magnetization of FL and I the applied current. It obvious that t_w is inversely proportional to the applied write current on MTJ in the precessional regime. More specifically, larger applied current induces shorter t_w, while smaller current makes the switching process slower.

Different from STT effect induced switching process, the switching process depends on the thermal fluctuation in the thermal activation regime ($t_p > 40ns$). With thermal fluctuation, FL magnetization reversal can take place under the condition $I < I_c$. The switching time t_w is expressed with the Neel-Brown model [69] as the following equation:

$$t_w = \tau_0 exp(\Delta\left(1 - \frac{I}{I_c}\right)) \tag{2.8}$$

where τ_0 is the attempt period ($\sim$ 1ns). Other than inverse proportional relationship between t_w and I_c, the more complicated relationship involving exponential calculation is demonstrated by equation 2.8. When the applied current is closer to I_c, t_w wiil be shorter.

2.4. Electrical STT-MRAM Model

As one of the most promising NVM, STT-MRAM is expected to play a more important role in future's semiconductor market with increasingly mature manufacturing technology. In this section, we firstly introduce the STT-MRAM modelling hierarchy based on the abstraction levels. Next, the electrical STT-MRAM model is discussed in more details, since the main focus of our work is on electrical-level simulations of STT-MRAM circuits, which are based on SPICE.

2.4.1. Hierarchy of STT-MRAM Modelling

As before introduced in section 2.1.1, semiconductor chips consist of various modules, each of which comprises large amounts of transistors. Therefore, cooperation among different worldwide companies is necessary in the industry of semiconductor memories. In order to make the whole production process sufficiently seamless and efficient, a hierarchy of chip modelling is built up, each level of which is focused by the responsible designers.

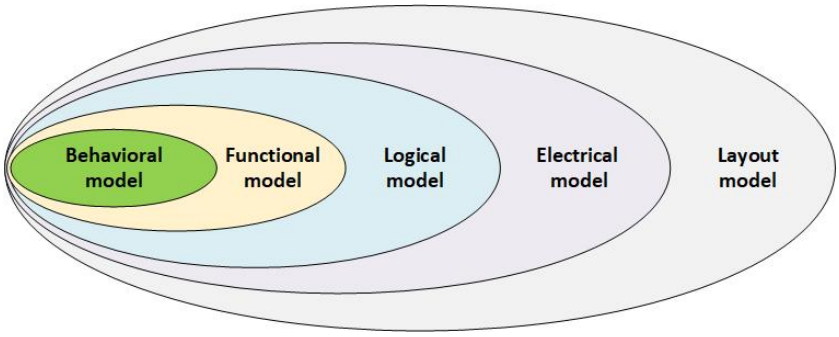


Figure 2.11: Different levels of chip modelling

Figure 2.11 illustrates the general hierarchy of chip modelling based on the abstraction level. From behavioral model to layout model, the abstraction level becomes gradually lower. The behavioral model is the highest level, while the layout model is the lowest level. The higher the abstraction level is, more physical implementation details are included. Almost no detailed information is provided related to the internal structure or operations of the designed systems in the behavioral model. Regarded as a black box, the behavioral

model only reveals the relationship between input and output signals [70] as illustrated in Figure 2.12, which presents the behavioral model of Everspin's 1Gb ST-DDR4 STT-MRAM. By contrast, the layout model incorporates the most detailed system implementation information including the location, dimensions, and other characteristics of the real physical structure [6] as shown in Figure 2.13. Figure 2.13 displays the layout model of a STT-MRAM cell in Intel's test chip.

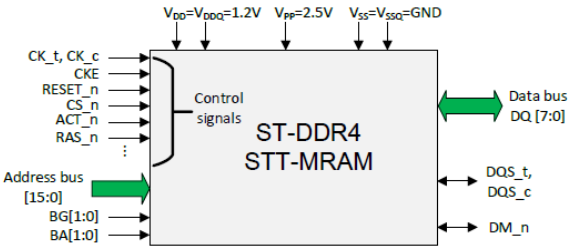


Figure 2.12: Behavioral model of Everspin's 1Gb ST-DDR4 STT-MRAM [11]

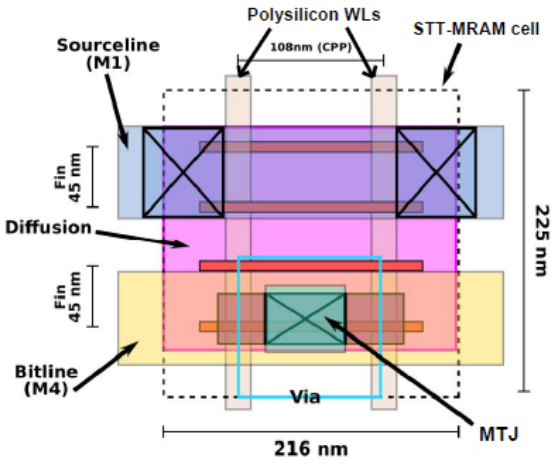


Figure 2.13: Layout model of a STT-MRAM cell in Intel's test chip [12]

As the next level for behavioral model, functional model is regraded as a set of smaller black boxes, which represent different modules of the whole circuit. Each of them has corresponding functionality. Logical model is expressed by a large amount of logic gates. This type of model is not typical for memory chips, which is due to the fact that logic gates only take a small portion of the whole chip circuit [6].

In this thesis, we focus on the electrical model, which is built up with various components. Figure 2.14 presents the typical electrical model of STT-MRAM circuit including two main parts: a memory cell array and peripheral circuits. In our work, the similar circuits are utilized for circuit simulations, which will be explained in section 4.2.1. In architecture of memory cell array shown in Figure 2.14, there are numerous memory bit cells. The selected bit cell design is 1T-1MTJ in our work, which comprises a NMOS transistor and a MTJ [71] and is the most widely adopted STT-MRAM bit cell design [25]. Additionally,

the peripheral circuit includes three parts: address decoders (row/column decoder), write drivers and sense amplifiers. Next, we will elaborate on these components separately.

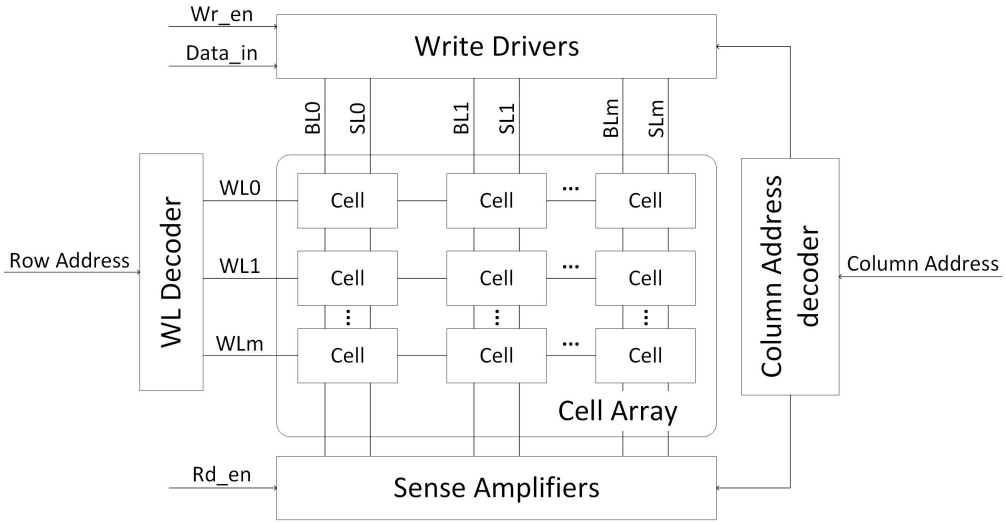


Figure 2.14: Electrical model of STT-MRAM circuit

2.4.2. STT-MRAM Bit Cell

As the typical STT-MRAM design, the architecture of 1T-1MTJ bit cell is illustrated in Figure 2.15a. The MTJ device that is the core element of STT-MRAM is serially connected with a single NMOS transistor that serves as a selector. The bit line (BL) is connected to MTJ's FL and the source line (SL) is connected to the source or drain of NMOS. The word line(WL) connected to the gate of the NMOS transistor selects which row of cells in the memory cell array is accessible according to the memory address provided by the address decoder.

Three basic operations of STT-MRAM respectively shown in Figures 2.15b, 2.15c and 2.15d are write '0' operation, write '1' operation and read '0'/'1' operation. When logic '0' is being written into the selected cell, the applied current (I_{W0}) flows from BL to SL. On the contrary, I_{W1} flows in reverse direction from SL to BL. It is worth noting that I_{W0} is marginally higher than I_{W1} due to source degeneration of NMOS [72, 73].

For read '0'/'1' operations, the applied current has same direction as that of write '0' operation. BL is pulled up to V_{read}, while SL is pulled down to ground. The process of reading out cell's value is equivalent to the discharging process. During the implementation of the read operation, the current state of the memory cell is expected to keep unchanged. Only with the stable state, the stored binary data can be truly read out by sense amplifier. Therefore, the reading current I_{rd} must be sufficiently weaker than the critical switching current. When thermal stability (Δ) is 60, I_{rd} should be the half of I_c at most [74]. In Figures 2.15b, 2.15c and 2.15d, the magnitude of the applied current for three operations is presented by arrow's width, respectively.

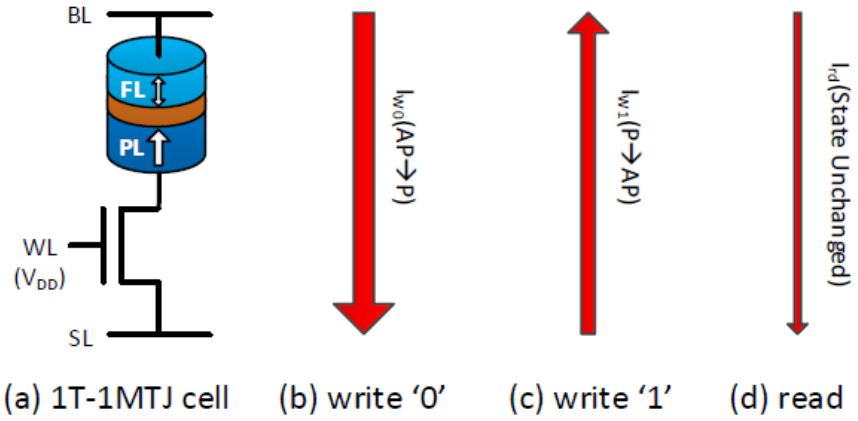


Figure 2.15: 1T-1MTJ bit cell and write/read operations [13]

2.4.3. Peripheral Circuits

As shown in Figure 2.14, peripheral circuits are regarded as one of the important parts in STT-MRAM circuits. Peripheral circuits consist of address decoders, write drivers and sense amplifiers. Next, we separately elaborate on these sub-circuits. Note that these circuits are used for SPICE-based simulations in our work.

address decoder

In the organization of STT-MRAM circuit illustrated in Figure 2.14, there are numerous memory cells. Address decoders are utilized to choose specific memory cells. In order to locate the desired memory cells accurately, there are row address decoder and column address decoder. Row address decoder is used to determine the row address of the desired cell, while column address decoder is utilized to select the column address of the targeted cell. In other words, the voltage of WL is provided by the row address decoder and the voltage of BL/SL is provided by the column address decoder. Here we take the row address decoder for example.

Figure 2.16 presents the typical row address decoder in a small STT-MRAM circuit that is not larger than 4x4. The whole circuit is formed by NOT and NAND gates. There are two inputs: A1 and A2 that will be decoded into four outputs, each of them corresponds to each of word lines that sever as the switches in each row of the cell array.

Table 2.2 presents the logic relationship between the inputs and outputs of the row address decoder. For instance, when 'A1A0' is '01', the word line for the second row (WL_1) will be applied high level voltage. By contrast, the voltage on other word lines will be low.

write driver

Write driver is utilized to perform write operations on the selected cell. The design of the used write driver in this thesis is illustrated in Figure 2.17. Based on the functions, it can be divided into two sub-circuits. The sub-circuit in blue region is called control logic part, while the part of driving circuit is within the orange region. The whole control logic part consists of three NOT gates and two NAND gates. This part is utilized to provide the inputs

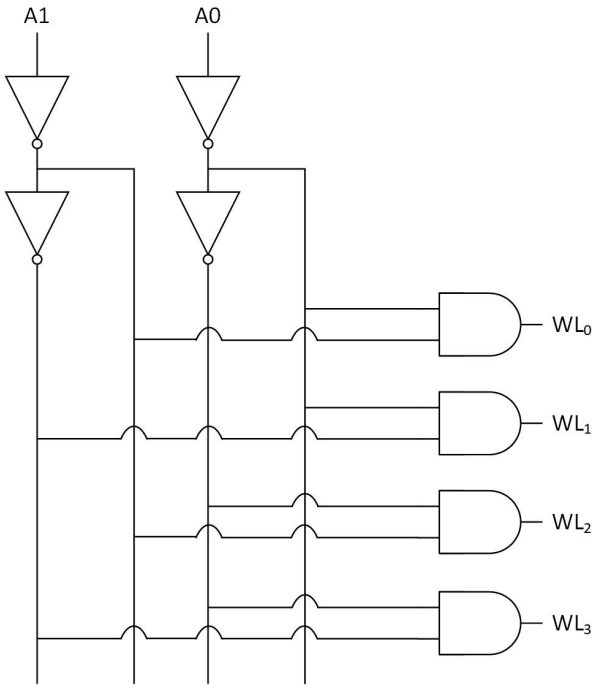


Figure 2.16: Row address decoder

Table 2.2: Truth table of row address decoder

A1	A0	WL_3	WL_2	WL_1	WL_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

for the driving circuit based on two inputs: Data_in and Wr_en. Data_in represents the data to be written into cells and Wr_en is the enable signal for write operations. Four outputs of the control logic part are IN1, IN2, IN3 and IN4, the logic value of which respectively determines the switch-off/on of P1, N1, P2 and N2 transistors. In this way, the voltage is applied on BL and SL of bit cells to perform the desired write operations. When w0 operation is performed, the current flows from BL to SL as shown in Figure 2.17. Oppositely, the current direction is from SL to BL under w1 operation.

Table 2.3 gives the truth table of the control logic part. For example, when Wr_en is '1' and Data_in is '0', IN1, IN2, IN3 and IN4 will be '0011'. Therefore, P1 and N2 will be switched on, while P2 and N1 will be kept off. Write '0' operation is performed with I_{W0} flowing through the MTJ device. When Wr_en is '1' and Data_in is '1', write '1' operation is carried out in the similar way.

The waveform of several signals related to the sequence 0w1w0 is illustrated in Figure

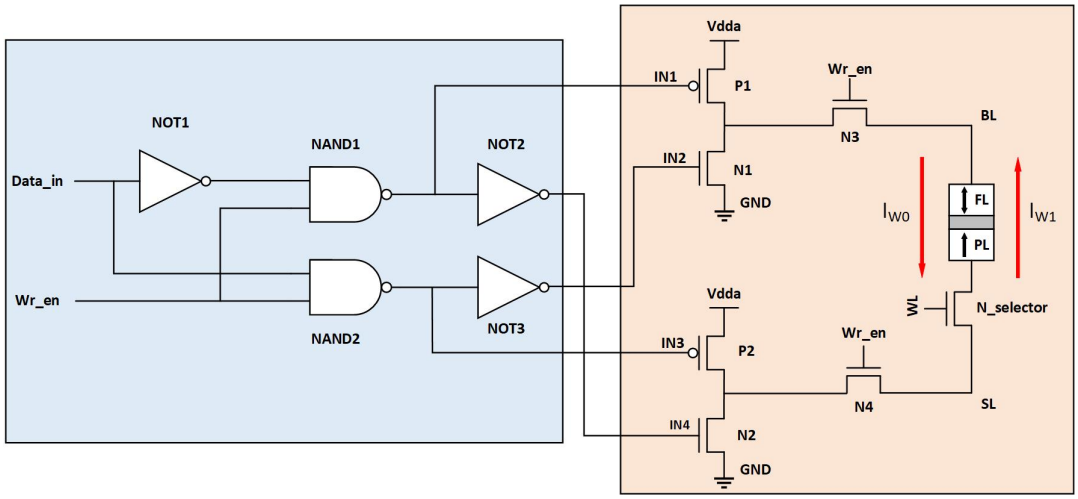


Figure 2.17: Write driver for STT-MRAM cells

Table 2.3: Truth table of the control logic part

Wr_en	Data_in	IN1	IN2	IN3	IN4	Operation
0	0	1	0	1	0	None
0	1	1	0	1	0	None
1	0	0	0	1	1	W0
1	1	1	1	0	0	W1

2.18. V_{WL}, V_{Wr_en} and V_{Data_in} are respectively the voltage of the word line, write enable and input data. V_{WL} and V_{Wr_en} are set to high level voltage during the write operations. Due to source degeneration issue [9], V_{WL} is slightly larger than 2V to promote the switching current, while V_{Wr_en} is set to 2V. During write '1' operation, 2V is assigned to V_{Data_in}. By contrast, V_{Data_in} is 0V under write '0' operation. As shown in Figure 2.18, the pulse width (t_p) of the voltage on STT-MRAM is around 7 ns. The switching time ($t_w\,(P \rightarrow AP)$) of P to AP state is around 3.5 ns, while the opposite switching process lasts about 5.4 ns. For the circuit simulations in this thesis, a Verilog-A MTJ compact model is utilized. More detail about this model can be found in [6]. The 90nm predictive technology model (PTM) is employed for all used transistors in our circuits.

sense amplifier

The functionality of sense amplifier is to read out the logic data stored in the selected cell. The logic value '0' or '1' in the MTJ device is stored in the form of resistance. In other words, there is a wide gap between the current flowing through the MTJ device under P and AP states. In the sense amplifier, the current difference is translated into the voltage difference using two cross-coupled inverters. When the output voltage is high, the read-out value will be '1'. By contrast, '0' is read out with the low output voltage. The output is Q shown in Figure 2.19.

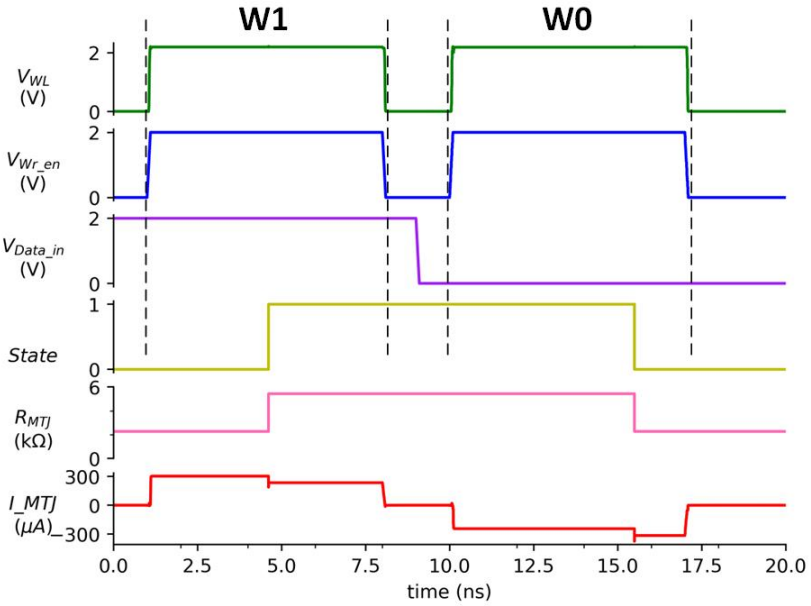


Figure 2.18: SPICE-based simulation waveform of 0w1w0

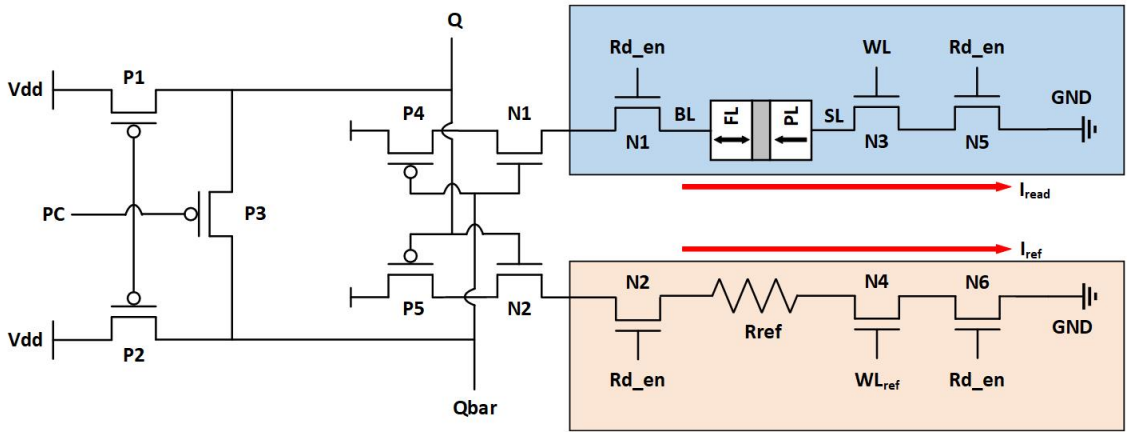


Figure 2.19: Pre-charge based sense amplifier for STT-MRAM cells

Figure 2.19 presents the circuit design of pre-charge based sense amplifier used for circuit simulations in our work. This type of sense amplifier consists of three parts: a voltage equalizer, two cross-coupled inverters and two discharge circuits including the paths of the memory cell and the reference cell. The period of read operations can be divided into 3 phases: pre-charge, voltage development and voltage amplification [6]. Different parts of the sense amplifier play the different roles in different phases. Next, we elaborate on each part and each phase respectively.

- **Pre-charge**: The voltage equalizer consisting of three PMOS transistors (P1, P2, P3) provides the identical voltage for Q and Qbar. More specifically, when PC node is connected to the ground, all of these three PMOS transistors are switched on. Therefore,

the voltage of both Q and Qbar will be pulled up to Vdd during this phase. It is worth noting that WL and WL_{ref} signals are pulled down to the ground to guarantee no current generated in two discharge paths, respectively. Rd_en signal is connected to voltage supply (Vdd) during the whole read operation.

- **Voltage development**: In this phase, PC signal is firstly pulled up to Vdd to turn off P1, P2 and P3. WL and WL_{ref} are connected to Vdd at the same time. As a result, the discharging process starts in both paths. As shown in Figure 2.18, I_{read} passes through the selected memory cell, while I_{ref} is the discharge current in the reference circuit path. The reference resistor (Rref) is $\frac{1}{2}(R_P + R_{AP})$. When the memory cell is in AP state, I_{read} is smaller than I_{ref}. With the difference of discharging speed, the potential of Q falls slower than Qbar. On the contrary, Q has the lower potential than Qbar, when the state of the memory cell is P state.

- **Voltage amplification**: In this phase, the potential difference between Q and Qbar will be further enlarged. If one of these two nodes reaches the certain threshold, the corresponded inverter will be switched on and another will be switched off. In this way, the potential of Q and Qbar will be constantly kept at Vdd or gnd at the end of this phase. For instance, if the stored data in the memory cell is '1', the cross-coupled inverters guarantee that the voltage on Q will be Vdd, while the voltage on Qbar will be gnd. Similarly the logic value '0' can be read out with the low potential of Q.

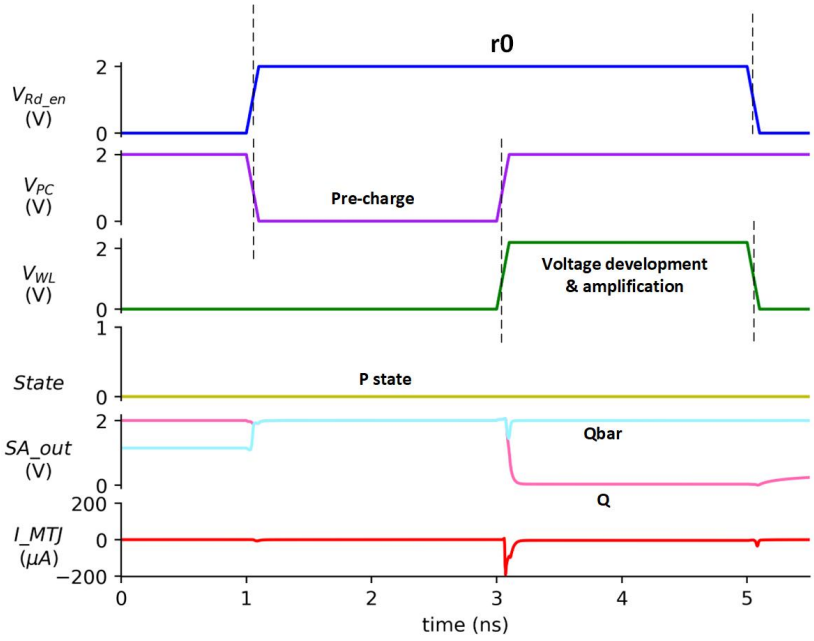


Figure 2.20: SPICE-based simulation waveform of 0r0

Figure 2.20 illustrates the waveform of several signals related to the read operation 0r0. The r0 operation takes 4 ns. The phase of pre-charge takes place from 1 ns to 3 ns, while Voltage development and amplification are within 3-5 ns. It can be observed that these

three phases do not take such a long time. The actual time for them is around 400 ps. In other words, the read latency may be reduced to sub-nm levels using this sense amplifier. After three phases, the voltage Q is pulled down to gnd, while Qbar is hold at Vdd. This is consistent with the above discussion. The design of this pre-charge based sense amplifier is similar with the work in [75]. There are also other types of sense amplifiers for STT-MRAM. If interested, readers can find more related work in [76–78].

2.5. Overview of STT-MRAM Test Development

As one of the most important component in modern computer systems, memory has been attracting intensive R&D attention. In order to ensure high quality of manufactured memory chips, memory testing is crucially significant. The constant development of memory testing has been seen in the past few decades. Before 1980, ad-hoc tests are used in memory testing, which are only capable of detecting the limited defects and consume a lot of time [79]. In order to overcome these shortcomings, a number of fault models are introduced such as stuck-at faults [80]. With the assistance of these fault models, higher fault coverage can be guaranteed and the test time drastically decreases compared with the early ad-hoc tests.

In the late 1990s, the methodology of building fault models becomes increasingly formal, which is based on SPICE simulation under various defects injected. Nowadays, cell-aware test (CAT) approach is the mainstream of memory testing methodology, which is carried out by the injection of linear resistors as well. However, different from the earlier test method, CAT focuses on the cell-internal defects with further technology scaling down. CAT has proven its capability of detecting resistive defects such as opens, shorts and bridges happening at contact or interconnect of devices [81]. The work in this thesis is exactly based on the CAT approach. CAT approach has three main steps: defect modelling, fault modelling and test development. In defect modelling, the targeted defects will be modelled as linear resistors. Next, all possible faults will be defined in a complete fault space and they will be validated in the presence of the predefined defects. The final step is to develop effective test solutions for targeted defects. These steps will be elaborated in next sections. Note that if the test solutions target on some device-internal defects caused by novel failure mechanisms or novel materials, device-aware tests (DAT) is expected to be utilized. Since this is out of the scope of this thesis, more details will not be given here. If interested, more details can be found in [82].

As aforementioned in section 2.2.2, STT-MRAM is the potential substitutes for DRAM, even for SRAM in L3 caches. In order to reduce the test escape and yield loss of manufactured STT-MRAM chips, effective STT-MRAM testing is indispensable. In this section, the development of STT-MRAM testing will be introduced from three aspects: defects, fault models and test solutions.

2.5.1. Defects

Defect modelling is the first step of the memory testing. In order to obtain accurate defect models, the physical mechanism of STT-MRAM's possible defects is expected to be deeply investigated. On the basis of different phases in the manufacturing process, STT-MRAM

defects can be classified into two categories: front-end-of-line (FEOL) and back-end-of-line (BEOL) defects [25]. Next, these two types of defects will be respectively introduced in more details.

Defects in FEOL

The FEOL process of STT-MRAM manufacturing includes transistor fabrication and M1-4 metallization [15]. Semiconductor impurities, crystal imperfections and pinholes in gate oxides are the typical FEOL defects possibly happening within FEOL process [83]. All of these defects are regarded as the resistive defects and are modelled as linear resistors in defect modelling. Figure 2.21 shows the schematic of pinhole defects in a NMOS gate. A short circuit appears between the gate and transistor channel or between the gate and drain or source diffusion zones [14]. Therefore, this type of defects can be modelled as a short resistor.

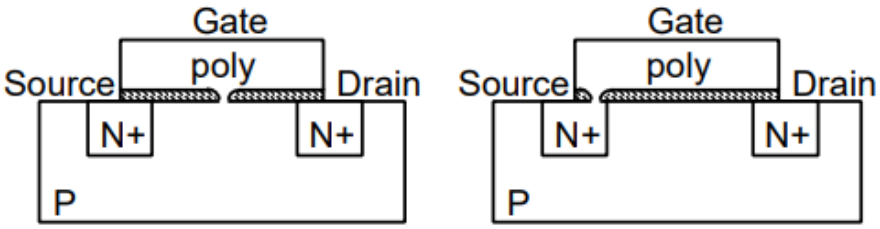


Figure 2.21: Schematic of gate-to-channel and gate-to-source(drain) pinhole defects in a NMOS gate [14]

Defects in BEOL

After FEOL steps, all other STT-MRAM manufacturing steps belong to BEOL steps. Among BEOL steps, bottom electrode contact (BEC) and top electrode contact (TEC) are the two phases, where resistive defects may occur with high possibility. During these two phases, interconnect defects may take place such as open vias/contacts, irregular shapes and big bubbles [84]. These interconnect defects will be modelled as open, short or bridge resistors as well. For instance, Figure 2.22 gives the TEM image of an open contact defect caused by polymer leftovers [15]. This defect occurs between the BEC layer and the underlying Cu layer during BEC step following the M1-4 metallization.

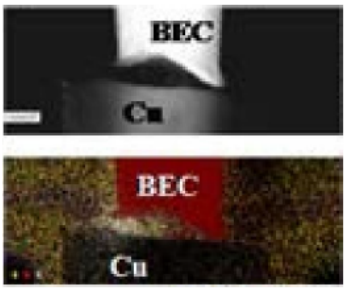


Figure 2.22: An open contact defect between the BEC and the underlying Cu layer [15]

Apart from in BEC and TEC steps, defects may also take place in other FEOL steps. Since most of these steps are STT-MRAM unique manufacturing steps compared with the traditional CMOS manufacturing, some MTJ related defects occur more easily during these phases. For example, Figure 2.23(a) illustrates the schematic of a pinhole defect in tunnel barrier (TB). It is the unintended penetration of CoFeB free layer into Mgo tunnel barrier. With the pinhole defect in TB, a conductive path forms between two ferromagnetic layers [9]. This type of defects can not be modelled as linear resistor directly, since it belongs to device-internal defects. If interested, more details about this defect can be found in [9].

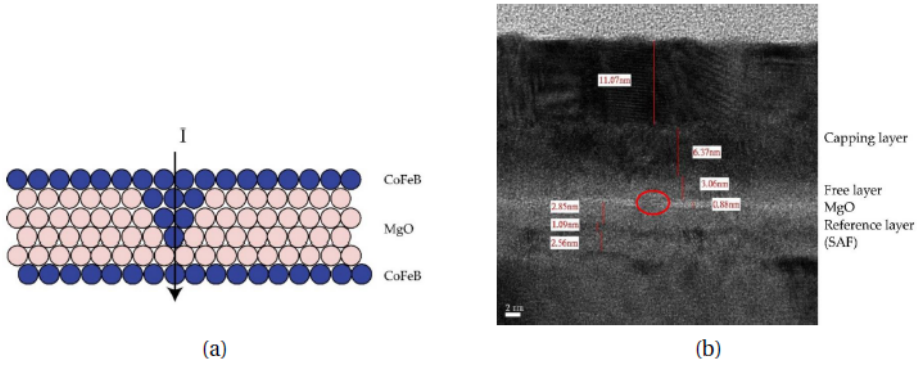


Figure 2.23: A pinhole defect in TB layer of MTJ[16]: (a) Schematic, and (b) Cross sectional TEM

2.5.2. Fault Models

After defect modelling, next step is fault modelling, which transfers the effect of physical defects into the functional level, in order to sweep out defective chips in a more efficient way. Faults are the representation for physical defects in the abstraction level [80]. Therefore, accurate fault models are necessary for STT-MRAM testing. Faults are usually denoted in the form of fault primitives, the general expression of which is $\langle S/F/R\rangle$ if only one cell is involved [85]. S means the sensitizing sequences, while F is the faulty behavior and R stands for read-out value. When two cells or more than two cells are involved in the faults, $\langle S_a; S_v/F/R\rangle$ and $\langle S_{a_0}; ...; S_{a_{m-2}}; S_v/F/R\rangle$ will be respectively used. S_a is the sensitizing sequence of the aggressor cell, while that of the victim cell is S_v. More detail about the definition of fault primitives will be elaborated in section 4.1. Next, We will introduce some typical fault models caused by interconnect and contact defects in STT-MRAMs.

Transition Fault

Transition fault (TF) means the failed transition between P state and AP state. It can be described with fault primitive ($\langle x w \overline{x}/x/-\rangle$), where $x \in \{0,1\}$ and $\overline{x}$ represents the inverse state of x. There are two types of TF: TF1 ($\langle 1w0/1/-\rangle$) and TF0 ($\langle 0w1/0/-\rangle$). In [17, 86], TFs are validated with simulations under various resistive defects such as open defects at BL, SL or WL. In other words, TFs will take place with defects contributing to the dramatic reduction of write current. Figure 2.24 presents the occurrence of TFs under various injected defects. when the write time is above the red horizontal line, TFs will happen. Apart from resistive

open defects, process variation can cause TFs [17]. For different specific thermal stability (Δ), different write time is required to finish the switching process. When switching time produced by process variation is longer than the applied write pulse, TFs occur as well even without resistive defects.

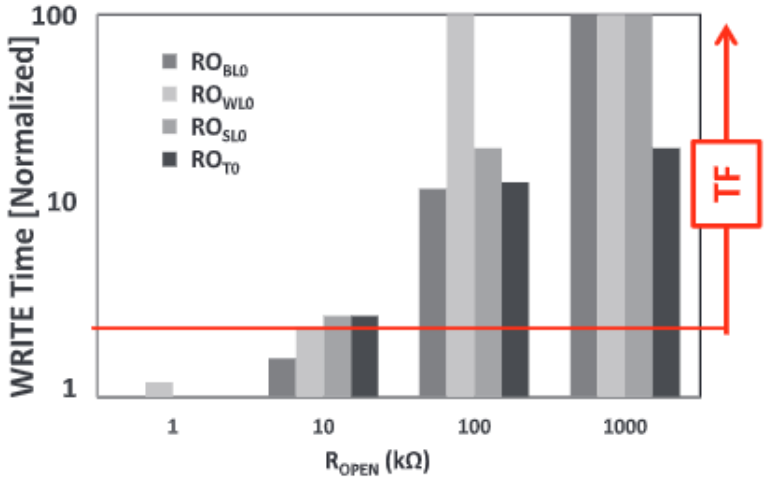


Figure 2.24: Occurrence of TFs with various open defects at different defect strengths [17]

Incorrect Read Fault

The fault primitives of incorrect read fault (IRF) are $\langle 1r1/1/0\rangle$ and $\langle 0r0/0/1\rangle$, which respectively correspond to IRF1 and IRF0. IRF means the state of cell keeps stable with wrong read-out value after the read operation.

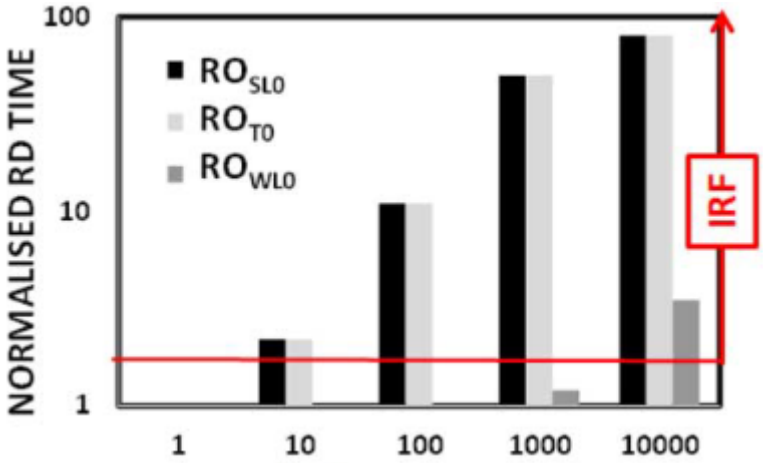


Figure 2.25: Occurrence of IRF0 with various open defects at different defect strengths [17]

As explained in section 2.4.3, the read-out value depends on the current difference between the memory cell path and the reference circuit path. As a result, the appearance of

IRFs may be attributed to the change of read current in the presence of resistive defects, which are observed in [17]. Defects such as open defects at SL or WL cause IRF0, since large read current is drastically reduced to less than that of the reference path. By contrast, when read current is pulled up due to some bridge defects, IRF1 possibly takes place as well. Figure 2.25 illustrates the appearance of IRF0 with different open defects. The horizontal red line defines the critical point of IRF0, which arises above this line. Similar with TF, the occurrence of IRFs is affected by process variation as well. More details can be found in [17, 86].

Read Destructive Fault
Read destructive fault (RDF) refers to the unintended reversal of magnetization direction in the free layer of the selected bit cell after the read operation. $\langle 0r0/1/1\rangle$ and $\langle 1r1/0/0\rangle$ respectively correspond to RDF0 and RDF1. It is worth noting that only RDF1 possibly arises in STT-MRAM cell arrays, since read current (I_{rd}) passes along with the same direction as write '0' current (I_{W0}) as shown in Figure 2.15. Consequently, only the inadvertent flip from AP state to P state can take place during a read operation. Some resistive bridge or short defects cause RDF1 in [17].

Write Disturb Coupling Fault
Different from above introduced fault models, two bit cells are involved in write disturb coupling fault (CFwd). The two involved cells are classified into two types: aggressor cell and victim cell. The operations or state of the aggressor cell cause the faulty behavior in the victim cell. The denotation of CFwd is $\langle xwx; y/\overline{y}/-\rangle$ or $\langle xw\overline{x}; y/\overline{y}/-\rangle$, where $x, y \in \{0,1\}$ and operations are applied on the aggressor cells. By contrast, CFwd is expressed by $\langle x;1w1/0/-\rangle$ and $\langle x;0w0/1/-\rangle$, when states of the aggressor cell contribute to the unintended fault during non-transition write operations of the victim cell. This type of fault possibly arises between the adjacent bit cells that share the common bit line and source line in the presence of inter-cell bridge defects [17, 86]. For example, CFwd is reported when the word lines in two columns are inadvertently connected [86].

2.5.3. Test Solutions

The final step of memory testing is to develop efficient test solutions to detect realistic fault models caused by physical defects.

Figure 2.26 presents the fault classification based on the testability. If the memory faults can be described by fault primitives, they will be regarded as strong faults. Otherwise, the faults belong to the group of weak faults. According to the testability of memory faults, they can be classified into two types further as shown in Figure 2.26: Easy-to-detect (EtD) and Hard-to-detect (HtD) faults. Different types of test solutions are respectively applied to EtD and HtD faults.

EtD faults are those that can be detected by march tests [80], while design-for-testability (DfT) techniques or stress tests are used to detect HtD faults. In this section, some developed march tests for STT-MRAM are introduced followed by DfT techniques and stress tests.

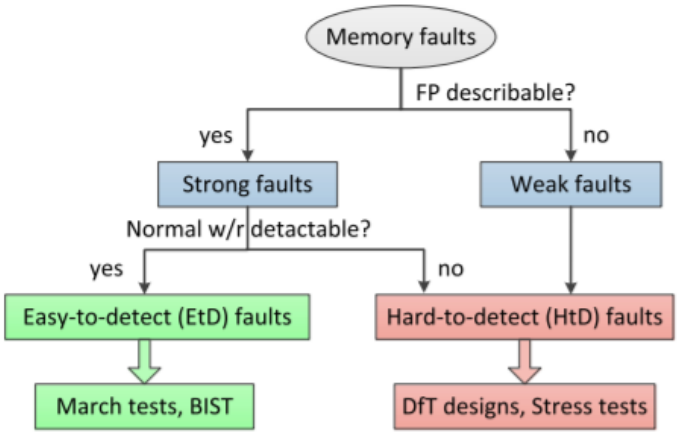


Figure 2.26: Fault classification based on the testability [8]

March Tests

A march test is a set of finite march elements, which consists of read or write operation sequences [8]. This kind of test algorithms can be used to detect EtD faults. For instance, transition fault ($\langle 0w1/0/-\rangle$) caused by certain defects can be detected by $\Updownarrow(...,0,w1,r1,...)$, where $\Updownarrow$ means that the march test is implemented regardless of the addressing direction of memory array cells [8]. Other two denotations of addressing directions are $\Uparrow$ and $\Downarrow$, which respectively stands for up addressing order and down addressing order. For $\Updownarrow(...,0,w1,r1,...)$, the selected memory bit cell is firstly fixed to '0' state. Then a write '1' operation and a read '1' operation are sequentially applied to the current cell. Above process is repeated until this operation sequence has been applied to each bit cell in the targeted memory array. If the result of the read operation is not '1', this fault is detected and the corresponding defective chips are to be swept out.

In [87], a Word Oriented March (WOM) test [88] targeted for several fault models in STT-MRAMs is constructed as follows:

$$\Updownarrow(w00);\Uparrow(r00,w11,r11);\Downarrow(r11,w00,r00);$$
$$\Downarrow(r00,w11,r11);\Downarrow(r11,w00);\Updownarrow(r00);$$
$$\Uparrow(r00,w01,r01);\Uparrow(r01,w10,r10);\Downarrow(r01,w10,r10);$$
$$\Downarrow(r10,w11,r11);\Updownarrow(r11)$$

This march test algorithm (26N) comprises of 11 march elements, which are able to sensitize and detect various discussed fault models in [87] including stuck-at faults, transition faults, incorrect read faults and coupling faults in the presence of the predefined physical defects. Each parenthesis represents a march element to be applied on each cell in the specified addressing order. It is worth noting that the word size is 2. For example, $\Updownarrow(w00)$ means '0' will be written into two bit cells of a word cell and this sequence will be carried out in each word cell regardless of address order. If interested in the generation of WOM test, more details can be found in [88].

In [86], various fault models are observed in STT-MRAMs as well. Different from the results in [87], some STT-MRAM specific fault models are recorded such as dynamic incorrect

read fault (dIRF-n), where n means the number of read operations required for sensitizing this fault. For different classes of STT-MRAM faults, different march test sequences will be generated in [86]. The test algorithm for dIRF-8 in [86] is taken as an example here and is constructed as follows:

$$\Uparrow (w0);$$
$$\Uparrow (r0, w1, r1, r1, r1, r1, r1, r1, r1, r1);$$
$$\Downarrow (r1, w0, r0, r0, r0, r0, r0, r0, r0, r0);$$
$$\Downarrow (r0)$$

This test sequence contains 4 march elements and 22 operations in total. It is clearly seen that there are 8 sequential read '1' operations in the second march element, which is utilized to sensitize dIRF-8 fault. The first read '1' operation in the third march element is used to detect this fault model. Not limited to detection of dIRF-n, this test sequence can also cover other STT-MRAM faults. If interested, readers can refer to [86].

DfT Techniques/Stress Tests

Since the normal write or read operation sequences are unable to detect HtD faults, DfT techniques or stress tests are implemented to achieve the coverage of these more complicated faults. For instance, within defect strength $(0.32, 0.35]$, the TB pinhole defect contributes to the appearance of the fault expressed by $\langle 1r1/U/? \rangle$, where 'U' means the faulty state is between '0' and '1' state, and '?' means the read-out value is random ('0' or '1'). It is obvious that the normal march test is unable to detect this type of faults. Since when the pinhole defect strength sufficiently increases, the caused faults will be transformed to detectable fault models by march tests. Therefore, stress test is expected to combine with march tests to detect this fault [6]. More specifically, one possible solution is to subject the STT-MRAM to a hammering write '1' operation sequence with elevated voltage or prolonged pulse width to deliberately speedup the growth of the TB pinhole defect, so as to transform HtD faults to EtD faults [6]. After transformation, march tests can be used to detect the defective chip successfully.

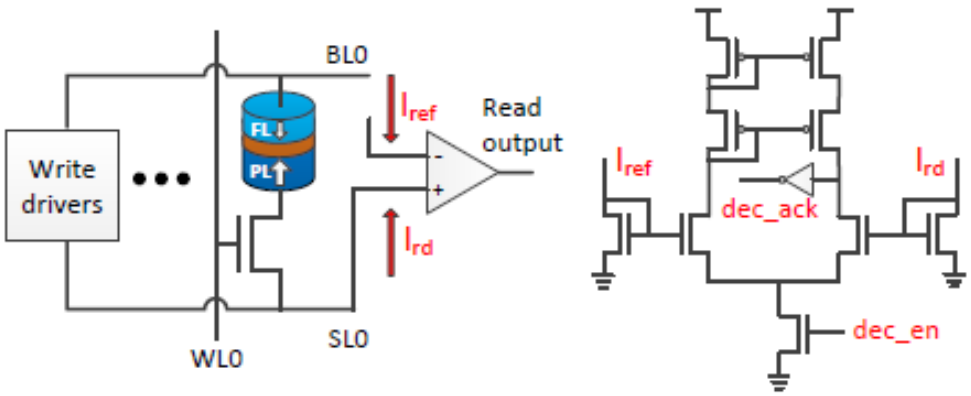


Figure 2.27: DfT circuit for TRDF detection[18]

Apart from the proposed stress tests for small pinhole defects, various DfT techniques are also utilized for detecting some specific fault models in STT-MRAMs. In [18, 89], DfT techniques targeted for transient read disturb faults (TRDF) are developed. Since the occurrence possibility of TRDF varies from cycle to cycle, march tests can not guarantee detection of this fault. TRDF means when a weak read current is applied to the addressed memory cell, original state of MTJ device will be inadvertently switched to the inverse state. Under this circumstance, the applied read current will increase in turn due to the change of cell's resistance. The proposal in [18, 89] is exactly based on this principle. The designed DfT circuit is illustrated in Figure 2.27. Since the current direction of read operations is same with that of write '0' operation, TRDF only take places during read '0' operation. As a result, only when the read '0' operation is implemented, dec_en will be set to high voltage level to enable the TRDF detection. I_{ref} and I_{rd} are respectively current flowing through the reference circuit in the sense amplifier and the addressed memory cell. In the proposed DfT ciruit, these two currents will be copied with two current mirrors and the comparison will be made. Signal dec_ack presents whether TRDF is detected or not. When MTJ is in AP state, I_{ref} is smaller than I_{rd} and dec_ack will be '0'. If dec_ack switches from '0' to '1', that means I_{ref} becomes larger than I_{rd} and TRDF is successfully detected.

3

Defect Space

This chapter discusses the defined space of interconnect and contact defects in STT-MRAMs. Firstly, we presents how to build accurate models for interconnect and contact defects, which are the prerequisites for the accurate fault modelling. Next, all possible defects are elaborated in terms of three types: opens, shorts and bridges.

3.1. Modelling of Interconnect and Contact Defects

As the first step in the memory testing, defect modelling is of much significance in the manufacturing test process. During the defect modelling, all possible physical defects are modelled at the electrical level, since the electrical simulation will be performed in fault modelling [36]. SPICE-based circuit simulation will be used in this work. Defect modelling serves as the critical bridge between physical defects and fault models that are the representation of defects at the abstraction level [80]. If the focused defects are not modelled in an appropriate way, the obtained fault models are not realistic. Therefore, the best method to narrow the gap between the defects and faults is to build an accurate model for targeted defects. Next, we will discuss how to model interconnect and contact defects in STT-MRAMs.

Interconnect and contact defects are essentially the spot defects attributed to undesired particles in electronic circuits [90]. Spot defects occur during the manufacturing process and are not defined by the original integrated circuit layout [91]. More specifically, there exists the missing or extra material in or between the layers of the fabricated devices [90]. Interconnect and contact defects are modelled as the linear resistors, the value of which signifies the defect strength [80, 86, 87]. The defect models for them can be classified into three groups based on different electrical manifestation as follows [80, 92].

- Open: An extra resistance within a connection, which is denoted as R_{op}. The value of R_{op} is from 0 Ω to infinity ($0\Omega < R_{op} \leq \infty\Omega$).
- Short: An undesired resistive path between a node and power supply (V_{DD} or GND), which is denoted as R_{sh}. The value of R_{sh} is from 0 Ω to infinity ($0\Omega < R_{sh} \leq \infty\Omega$).

- Bridge: An extra parallel resistance between two different nodes, both of which are not V_{DD} or GND. It is denoted as R_{br}. The value of R_{br} is from 0 Ω to infinity ($0\Omega < R_{br} \leq \infty\Omega$).

According to the above definition, interconnect and contact defects are modelled as linear resistors. Although the defect models are seemingly concise, they are able to imitate the realistic impact of the most spot defects on the electrical simulation. Apart from spot defects, there are also other STT-MRAM specific defects caused by some novel mechanisms such as synthetic anti-ferromagnet flip (SAFF) defect [93] and intermediate (IM) state defect [94]. The behavior of these defects can not be represented by linear resistors. Interested readers can refer to [8] for more details about defect modelling of these defects, since the targeted defects of this work are interconnect and contact defects.

As introduced in section 2.4, the used electrical model of STT-MRAM in this thesis consists of two main parts: memory cell array and peripheral circuits. Contact/interconnect defects possibly occur in any part of the whole memory circuit such as the memory cell array, write drivers and sense amplifiers. In this thesis, we only focus on the defects in the memory cell array, neglecting those anywhere else. Figure 3.1 illustrates the classification of the targeted defects in this chapter. Opens, shorts and bridges are discussed in section 3.2, section 3.3 and section 3.4 later, respectively.

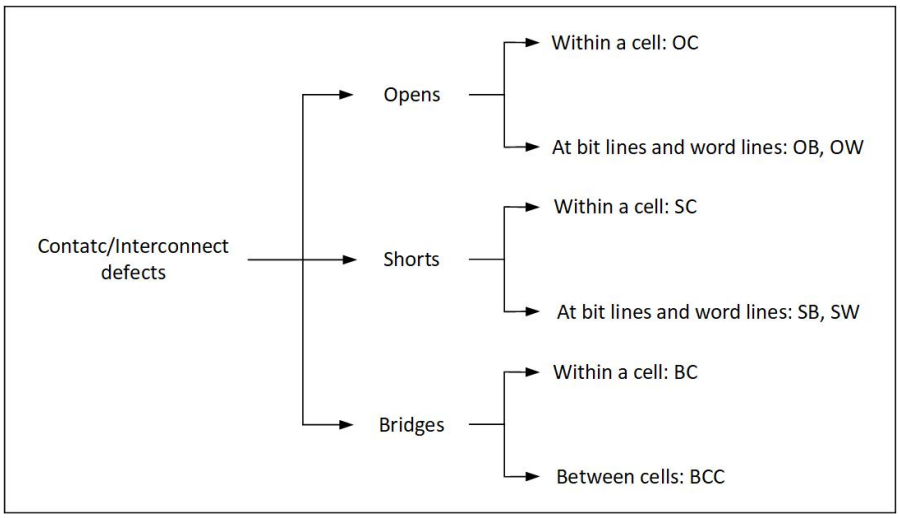


Figure 3.1: Classification of contact/interconnect defects

Figure 3.2 shows the structure of the selected STT-MRAM cell: 1T-1MTJ bit cell as introduced in section 2.4.2. One bit of data is stored in this design, which comprises a PMTJ and a NMOS selector. There are other types of designs for STT-MRAM bit cell such as multi-level cell (MLC) design in [95], which stores one bit of data with two complementary 1T-1MTJ cells. Compared with other designs, the selected design has the advantage of higher density. As a result, it is universally adopted in the industry. It is worth noting that a 1T-1MTJ bit cell has four nodes: WL, BL, SL and int. WL, BL, SL respectively correspond to word line, bit line and source line, while int represents the internal node between MTJ device and NMOS selector. All possible defects occur within or between these nodes.

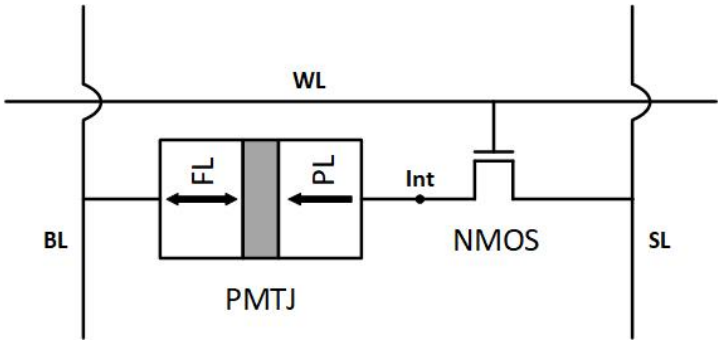


Figure 3.2: A selected 1T-1MTJ bit cell

3.2. Definition and Location of Opens

Based on locations, opens can be categorized into four groups: opens within a cell, opens at bit lines, opens at source lines and opens at word lines. All possible open defects are shown in Figure 3.3. It is worth noting that since similar faulty behavior in cells are caused by opens at different bit lines, source lines or word lines, only defects at one of these lines will be considered. This principle will be applied to the discussion of shorts in section 3.3 as well. Next, we will discuss different types of opens respectively.

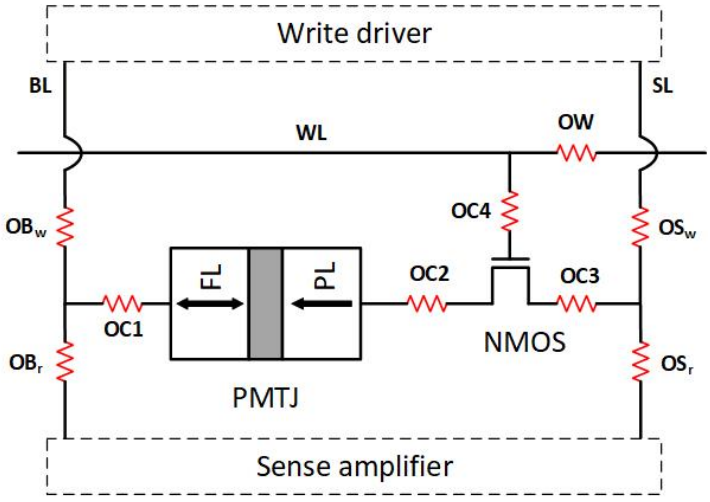


Figure 3.3: Opens within a cell, at BLs, SLs and WLs

3.2.1. Opens within a Cell

When we consider the opens within a cell, only the connections within the device will be taken in account. The denotation of opens within a cell is OC. As illustrated in Figure 3.3, there are four opens within a cell: OC1, OC2, OC3, OC4, since a memory bit cell has four internal connections. For example, OC2 represents the open defect occurring between PMTJ device and the NMOS transistor. The descriptions of all these opens within a cell are given in the first block of Table 3.1.

Table 3.1: List of opens

Open	Description	Type
OC1	An open between the bit line and the MTJ device	Opens within a cell
OC2	An open between the NMOS selector and the MTJ device	
OC3	An open between the source line and the MTJ device	
OC4	An open between the word line and the NMOS selector	
OB_w	An open at the bit line and at the write driver side	Opens at bit lines
OB_r	An open at the bit line and at the sense amplifier side	
OS_w	An open at the source line and at the write driver side	Opens at source lines
OS_r	An open at the source line and at the sense amplifier side	
OW	An open at the word line	Opens at word lines

3.2.2. Opens at Bit Lines, Source Lines and Word Lines

As shown in Figure 2.14, the bit cells in the same column share the common bit line and source line, while those in the same row are controlled by the common word line. Therefore, the behavior of memory cells in the same column or row may all be affected, when an open occurs at bit lines, source lines or word lines. Next, we discuss them one after another in details.

Opens at bit lines or source lines

A memory cell is not only connected to other cells, but also to the write drive and sense amplifier through bit lines and source lines. Therefore, the relative locations of opens to these peripheral circuits should be considered, when we define the locations of defects. Due to symmetry between bit lines and source lines, opens at bit lines and source lines will be elaborated together here, the denotations of which are respectively OB and OS. As shown in Figure 3.3, there are two possible locations for opens at bit lines as follows:

- OB_w: disconnection within the bit line at the write driver side.
- OB_r: disconnection within the bit line at the sense amplifier side.

Since the bit line is symmetric with the source line, the locations of opens at source lines are similar with that of opens at bit lines. OS_w represents the broken bit line at write side, while OS_r is an open disconnecting the bit cell with the sense amplifier. In Table 3.1, the definitions of opens at bit lines and source lines are given in the second and third block.

Opens at word lines

Different from the bit lines and source lines, the word lines is only connected to one subcircuit — row address decoder. In this way, the word lines provide the voltage for the NMOS selectors to switch on/off the bit cells in the same row. Therefore, only one possible location of opens at word lines are discovered, which is denoted as OW as illustrated in Figure 3.3. It is given in the last block of Table 3.1.

3.3. Definition and Location of Shorts

Similar with the definition of opens, there are also four groups of shorts in the memory cell array: shorts within a cell, shorts at bit lines, shorts at source lines and shorts at word lines.

A short means an undesired connection arises between a node and power supply (VDD or GND). Figure 3.4 presents the locations of all possible shorts in the memory array. Shorts within a cell will be discussed firstly followed by shorts at bit lines, short lines and word lines.

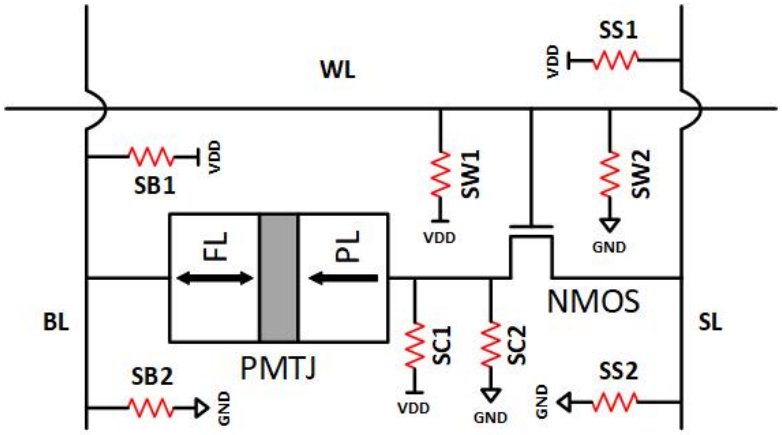


Figure 3.4: Shorts within a cell, at BLs, SLs and WLs

3.3.1. Shorts within a Cell

When we investigate the locations of shorts within a cell, only internal node between the MTJ device and the NMOS selector will be considered. Therefore, there are only two short defects within a cell that are SC1 and SC2. The descriptions for them are given in the first block of Table 3.2.

Table 3.2: List of shorts

Short	Description	Type
SC1	A short between the internal node and VDD	Shorts within a cell
SC2	A short between the internal node and GND	
SB1	A short between the bit line and VDD	Shorts at bit lines
SB2	A short between the bit line and GND	
SS1	A short between the source line and VDD	Shorts at source lines
SS2	A short between the source line and GND	
SW1	A short between the word line and VDD	Shorts at word lines
SW2	A short between the word line and GND	

3.3.2. Shorts at Bit Lines, Source Lines and Word Lines

Similar with opens, shorts at bit lines, source lines and word lines influence write or read operations on cells in the same columns or rows. For example, when write '0' operation is performed, BL is pulled up to high voltage level and SL is pulled down to the ground. If SB2 occurs during this operation, the switching process of '1' to '0' possibly fails. By contrast, the occurrence of SB1 contributes to the failure of write '1' operation with the

similar mechanism. The second, third and fourth block of Table 3.2 respectively gives the descriptions of shorts at bin lines, source lines and word lines.

3.4. Definition and Location of Bridges

The targeted bridges are the undesired connections between two different nodes in the memory array, both of which can not be VDD or GND. It is worth noting that the discussion about the locations of bridges are based on two assumptions. One is that the number of involved memory cells are two at most, when we consider the bridge defects. Another is that only defects in a cell itself or between adjacent memory cells are taken into account. This is because bridges with three or more involved cells have sufficiently low occurrence possibility (3.4 % on the average) [96, 97] and the nodes of nonadjacent cells are too far to reach each other in terms of the layout. Bridges are classified into two groups:

- Bridges within a cell: Both nodes of the undesired connections belong to nodes of the same memory cell. The denotation is BCs.
- Bridges between cells: Two nodes of the desired connections are from two adjacent memory cells. This kind of defects are denoted by BCCs. According to different relative positions of involved cells, BCCs are further divided into three types: bridges between the diagonal cells, bridges between cells in the same column and bridges between cells in the same row, which are respectively denoted by dBCCs, cBCCs and rBCCs.

In this section, these two groups of bridges will be separately discussed.

3.4.1. Bridges within a Cell

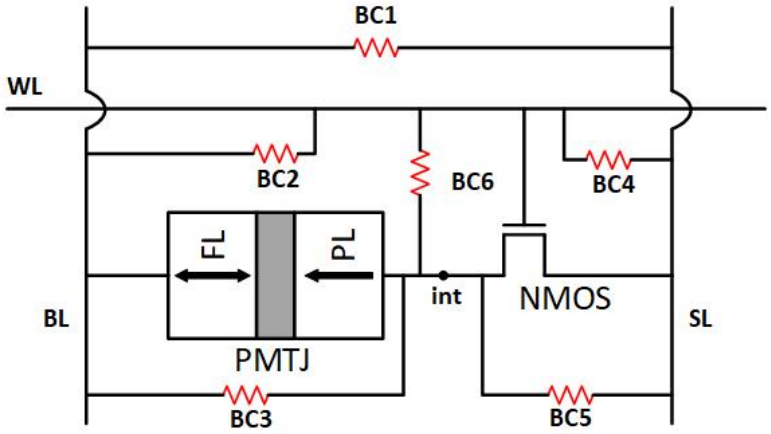


Figure 3.5: Bridges within a cell

A STT-MRAM cell has four different nodes including BL, SL, WL and int, two OF which form a bridge defect. Therefore, locating all possible BCs is equal to solving the problem of permutation and combination. The number of BCs is generally C_n^2, where n is the number of nodes in a bit cell. For the selected STT-MRAM design, the number of BCs should be

$C_6^2 = 6$. Figure 3.5 presents all possible bridges within a cell. For example, BC2 means an undesired connection arises between the bit line and word line of the cell, which may prevent the operations on this cell. More details about BCs are given in Table 3.3.

3.4.2. Bridges between Cells

For bridges between cells, there are three types: dBCCs, cBCCs and rBCCs. In other words, when we determine a bit cell as the selected central cell, other three cells should be considered. We build up a 3x3 memory array used for circuit simulations as shown in Figure 3.6. For the central cell C4, there are four diagonal cells (C0, C2, C6, C8), two cells in the same column (C1, C7) and two cells in the same row (C3, C5). Due to the symmetry of position, we only need to consider bridge defects between C0 and C4 or C1 and C4 or C3 and c4. In other words, only defects in red-box circled region are investigated in this thesis. Other bridge defects have symmetric one in this region. Therefore, we can simplify the process of location for BCCs. Next, we will explain how to locate dBCCs, cBCCs and rBCCs respectively.

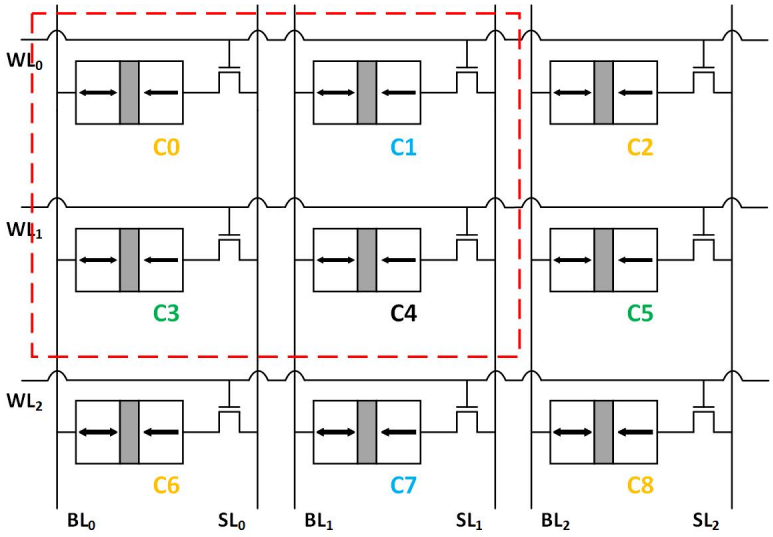


Figure 3.6: 3x3 memory array

Bridges between the diagonal cells

For the central cell C4, the diagonal cell is C0. Therefore, C0 and C4 will be considered when we focus on all possible dBCCs. Here we develop a equation $(n-k)^2$ to find all possible dBCCs, where n is the number of cells' nodes and k is the number of common nodes of involved cells. After this, the bridges that have been found previously should be removed in order to avoid repetition of defects. Both C0 and C4 have four nodes: BL_0, SL_0, WL_0, int_0 for C0 and BL_1, SL_1, WL_1, int_4 for C4. Therefore, n is 4 and k is 0. All possible dBCCs are shown in Figure 3.7 after removal of repeated defects, descriptions of which are given in the second block of Table 3.3. This method is also applied to finding possible cBCCs and rBCCs.

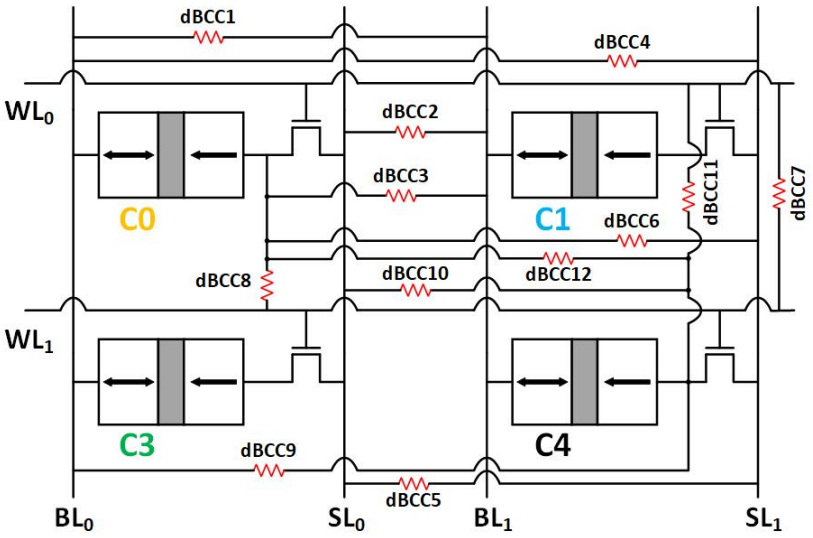


Figure 3.7: Bridges between the diagonal cells

Bridges between cells in the same column

Only C1 and C4 are considered for locating all possible cBCCs. The nodes of C1 are BL_1, SL_1, WL_0 and int_1. BL_1/SL_1 is shared by C0 and C4. Therefore, n is 4 and k is 2 for calculation of cBCCs. All possible cBCCs are shown in Figure 3.8 after removal of repeated defects, descriptions of which are given in the third block of Table3.3.

Bridges between cells in the same row

Similar with finding dBCCs and cBCCs, the common nodes between C4 and C3 is WL_1. Consequently, n is 4 and k is 1. All possible rBCCs are shown in Figure 3.8 after removal of repeated bridge defects, descriptions of which are given in the last block of Table 3.3.

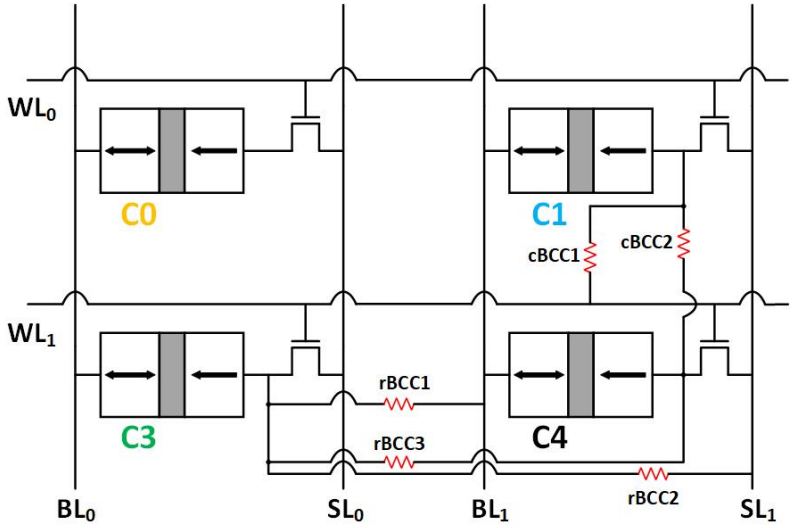


Figure 3.8: Bridges between the cells in the same column and row

8

Table 3.3: List of bridges

Bridge	Description	Type
BC1	A bridge between the bit line and source line	Bridges with a cell
BC2	A bridge between the bit line and word line	
BC3	A bridge between the bit line and internal node	
BC4	A bridge between the source line and word line	
BC5	A bridge between the source line and internal node	
BC6	A bridge between the word line and internal node	
dBCC1	A bridge between the bit lines of C0 and C4	Bridges between diagonal cells
dBCC2	A bridge between the bit line of C0 and source line of C4	
dBCC3	A bridge between the bit line of C0 and internal node of C4	
dBCC4	A bridge between the source line of C0 and bit line of C4	
dBCC5	A bridge between the source lines of C0 and C4	
dBCC6	A bridge between the source line of C0 and internal node of C4	
dBCC7	A bridge between the word lines of C0 and C4	
dBCC8	A bridge between the word line of C0 and internal node of C4	
dBCC9	A bridge between the internal node of C0 and bit line of C4	
dBCC10	A bridge between the internal node of C0 and source line of C4	
dBCC11	A bridge between the internal node of C0 and word line of C4	
dBCC12	A bridge between the internal nodes of C0 and C4	
cBCC1	A bridge between the word line of C4 and internal node of C1	Bridges between cells in the same column
cBCC2	A bridge between the internal nodes of C4 and C1	
rBCC1	A bridge between the bit line of C4 and internal node of C3	Bridges between cells in the same row
rBCC2	A bridge between the source line of C4 and internal node of C3	
rBCC3	A bridge between the internal nodes of C4 and C3	

4

Fault Modelling

This chapter discusses the second step of the memory testing — fault modelling, which consists of two sub-steps: fault space definition and fault space validation. The former is presented by explaining fault classification and defining the complete fault space, while the methodology of fault space validation is introduced in the latter. Next, we will elaborate on these two sub-steps respectively.

4.1. Fault Space Definition

A fault is the abstraction of a defect in terms of the function level [80]. With predefined defect models in chapter 3, the accurate fault modelling can be implemented, whose targets are faults caused by defects. In fault modelling, there are two sub-steps: fault space definition and fault space validation. The former is to abstract the predefined defects at the functional level and define the complete fault space including all possible faults, while the latter detects all the realistic faults in the presence of the predefined defects with Spice simulations. Here we will explain fault space definition firstly. Then fault space validation will be discussed in section 4.2.

4.1.1. Fault Classification

Based on different standard of classification, faults can be divided into various groups. For example, faults can be classified into EtD and HtD faults based on testability as shown in Figure 2.26. EtD faults can be detected by applying normal read or write operations. By contrast, it is only effective to recognize HtD faults with DfT techniques or stress tests. Apart from this, faults can also be classified based on the number of involved memory cells m and the number of operations n applied on the addressed cells [98], since faults can be influenced by the combination of multiple cells' states or operations and multiple sequential operations can be utilized to sensitize specific faults. For the number of involved of memory cells, the fault is a single-cell fault (SCF), if there is only one involved cell. If m = 2, the fault is categorized into 2-cell coupling fault (2-CF). If the number of the involved cells is more than 2, the fault is regarded as neighborhood pattern sensitive fault (NPSF). On the basis of the number of sequential operations, the fault is a static fault, if n = 1. The fault

is regarded as a dynamic fault, if more than one operations are needed for fault sensitization. It is worth noting that the fault possibly belongs to these two groups. For instance, the fault is static 2-CF, which means two cells are involved and one operation is performed. We discuss the complete fault space in the next section.

4.1.2. Complete Fault Space

The complete memory fault space consists of single-cell fault (SCF), 2-cell coupling fault(2-CF) and neighborhood pattern sensitive fault (NPSF). As introduced in section 2.5.2, these faults can be described in the form of fault primitive (FP) [36], which presents the applied operations on the cells and realistic state of the targeted cell. Figure 4.1 illustrates the composition of the complete fault. We will discuss them, respectively.

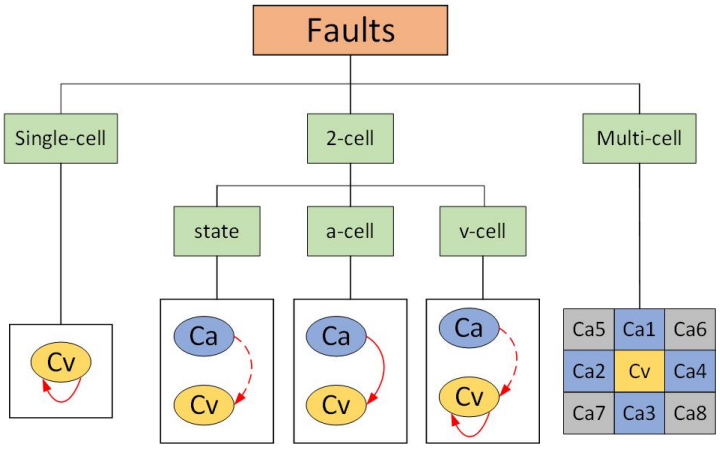


Figure 4.1: Complete fault space

Single-cell faults

A fault is a single-cell fault (SCF), when there is only one involved cell. As shown in Figure 4.1, the sensitizing operations are directly applied on the selected cell and other cells have no impact on it. The FP notation of SCF is $\langle S/F/R \rangle$, where

- S(sensitizing sequence) describes the operation sequences that are able to sensitize the corresponding fault. It is denoted in the form of $x_0O_1x_1...O_nx_n$, where $x \in \{0,1\}$ represents the stored logic value in the addressed cell, $O \in \{r,w\}$ represents the performed operations and n represents the number of the performed operations. If n > 1, the fault is dynamic, otherwise it is static. For example, $S = 1r1$ describes that a read operation is performed on a selected cell, the logic value of which is '1'. $S = 0w1r1$ describes that '1' are expected to be written into the addressed cell containing '0' followed by a read operation.

- F(faulty effect) describes the realistic state after performing the sensitizing sequence, where $F \in \{0,1,U,L,H\}$. Normally the states of memory cells are either '0' or '1'. However, the resistance of MTJ devices that represent the state of STT-MRAM can be out-

side the predefined resistance ranges for '0' and '1'. Extra states are expected to describe the states of these devices. Therefore, 'U', 'L' and 'H' are respectively defined for the undefined state, the extremely low state and the extremely high state. Figure 4.2 shows the resistance ranges for 5 states in STT-MRAMs.

Figure 4.2: STT-MRAM resistance ranges

- R(readout value) describes the output of a read operation, where $R \in \{0, 1, ?, -\}$. '0' and '1' correspond to normal logic readout value. '?' means that the readout value is random, which can not be determined by sense amplifier. '-' occurs when the last operation is not read operation. Under this circumstance, there will not be any output of the read operation. Note that R is '0' when the state of the targeted cell is 'L' and R is '1' when the state of the targeted cell is 'H'.

Table 4.1 lists all possible single-cell faults. Note that these faults can be divided into various fault models. A fault model consists of faults that have similar properties. For example, faults from #1 to #8 are belong to state fault (SF). When the number of performed operations is larger than 1, the fault will be single-cell dynamic fault. Since the methodology of presenting them is similar with that of static fault, we do not list them here.

Table 4.1: Single-cell static fault primitives

#	S	F	R	Notation	Fault model	#	S	F	R	Notation	Fault model
1	0	1	-	<0/1/->	State Fault	27	1r1	1	0	<1r1/1/0>	Read Non-destructive Fault
2	0	L	-	<0/L/->		28	1r1	1	?	<1r1/1/?>	
3	0	U	-	<0/U/->		29	0r0	1	0	<0r0/1/0>	Read Destructive Fault
4	0	H	-	<0/H/->		30	0r0	1	?	<0r0/1/?>	
5	1	0	-	<1/0/->		31	0r0	1	1	<0r0/1/1>	
6	1	L	-	<1/L/->		32	0r0	L	0	<0r0/L/1>	
7	1	U	-	<1/U/->		33	0r0	L	?	<0r0/L/?>	
8	1	H	-	<1/H/->		34	0r0	L	1	<0r0/L/1>	
9	0w1	0	-	<0w1/0/->	Write Transition Fault	35	0r0	U	0	<0r0/U/0>	
10	0w1	L	-	<0w1/L/->		36	0r0	U	?	<0r0/U/?>	
11	0w1	U	-	<0w1/U/->		37	0r0	U	1	<0r0/U/1>	
12	0w1	H	-	<0w1/H/->		38	0r0	H	0	<0r0/H/0>	
13	1w0	1	-	<1w0/1/->		39	0r0	H	?	<0r0/H/?>	
14	1w0	L	-	<1w0/L/->		40	0r0	H	1	<0r0/H/1>	
15	1w0	U	-	<1w0/U/->		41	1r1	0	0	<1r1/0/0>	
16	1w0	H	-	<1w0/H/->	Write Destructive Fault	42	1r1	0	?	<1r1/0/?>	
17	0w0	1	-	<0w0/1/->		43	1r1	0	1	<1r1/0/1>	
18	0w0	L	-	<0w0/L/->		44	1r1	L	0	<1r1/L/0>	
19	0w0	U	-	<0w0/U/->		45	1r1	L	?	<1r1/L/?>	
20	0w0	H	-	<0w0/H/->		46	1r1	L	1	<1r1/L/1>	
21	1w1	0	-	<1w1/0/->		47	1r1	U	0	<1r1/U/0>	
22	1w1	L	-	<1w1/L/->		48	1r1	U	?	<1r1/U/?>	
23	1w1	U	-	<1w1/U/->		49	1r1	U	1	<1r1/U/1>	
24	1w1	H	-	<1w1/H/->		50	1r1	H	0	<1r1/H/0>	
25	0r0	0	?	<0r0/0/?>	Read Non-destructive Fault	51	1r1	H	?	<1r1/H/?>	
26	0r0	0	1	<0r0/0/1>		52	1r1	H	1	<1r1/H/1>	

2-cell coupling faults

As introduced before, a 2-cell coupling fault (2-CF) involves two memory cells, the denotation of which is $\langle S_a; S_v/F/R\rangle$, where S_a and S_v are respectively the sensitizing sequences of the aggressor cell and the victim cell, F is the final value of the victim cell and R is the read-out value of the victim cell. Their definitions are similar with that for SCF. For 2-CF, there are three groups as shown in Figure 4.2: state CF, a-cell accessed CF and v-cell accessed CF.

State CF means that the state ('0' or '1') of the aggressor cell (Ca) affects the state of the victim cell (Cv). Table 4.2 lists all possible state CF. All of them belong to the fault model called state coupling fault.

Table 4.2: state coupling faults

#	Sa	Sv	F	R	Sa;Sv/F/R	Fault model
1	x	0	1	-	<x;0/1/->	State Coupling Fault
2	x	0	L	-	<x;0/L/->	
3	x	0	U	-	<x;0/U/->	
4	x	0	H	-	<x;0/H/->	
5	x	1	0	-	<x;0/0/->	
6	x	1	L	-	<x;0/L/->	
7	x	1	U	-	<x;0/U/->	
8	x	1	H	-	<x;0/H/->	

Note: x can be 0 or 1

when the state of Cv is influenced by the operations performed on Ca, this fault will be regarded as a-cell accessed CF. Table 4.3 lists all possible a-cell accessed CF. A fault model named disturb coupling fault contains all these listed faults.

Table 4.3: A-cell accessed coupling faults

#	Sa	Sv	F	R	Sa;Sv/F/R	Fault model	#	Sa	Sv	F	R	Sa;Sv/F/R	Fault model
1	$xw\bar{x}$	0	1	-	<$xw\bar{x}$;0/1/−>	Disturb Coupling Fault	13	xwx	1	0	-	<xwx;1/0/->	Disturb Coupling Fault
2	$xw\bar{x}$	0	L	-	<$xw\bar{x}$;0/L/−>		14	xwx	1	L	-	<xwx;1/L/->	
3	$xw\bar{x}$	0	U	-	<$xw\bar{x}$;0/U/−>		15	xwx	1	U	-	<xwx;1/U/->	
4	$xw\bar{x}$	0	H	-	<$xw\bar{x}$;0/H/−>		16	xwx	1	H	-	<xwx;1/H/->	
5	$xw\bar{x}$	1	0	-	<$xw\bar{x}$;1/0/−>		17	xrx	0	1	-	<xrx;0/1/->	
6	$xw\bar{x}$	1	L	-	<$xw\bar{x}$;1/L/−>		18	xrx	0	L	-	<xrx;0/L/->	
7	$xw\bar{x}$	1	U	-	<$xw\bar{x}$;1/U/−>		19	xrx	0	U	-	<xrx;0/U/->	
8	$xw\bar{x}$	1	H	-	<$xw\bar{x}$;1/H/−>		20	xrx	0	H	-	<xrx;0/H/->	
9	xwx	0	1		<xwx;0/1/->		21	xrx	1	0	-	<xrx;1/0/->	
10	xwx	0	L		<xwx;0/L/->		22	xrx	1	L	-	<xrx;1/L/->	
11	xwx	0	U		<xwx;0/U/->		23	xrx	1	U	-	<xrx;1/U/->	
12	xwx	0	H		<xwx;0/H/->		24	xrx	1	H	-	<xrx;1/H/->	

Note: x can be 0 or 1

The fault belongs to v-cell accessed CF if the state of Ca has impact on the operations on Cv. Table 4.4 lists all possible v-cell accessed CF. For v-cell accessed CF, there are five fault models including write disturb coupling fault, transition coupling fault, incorrect read coupling fault, read destructive coupling fault and deceptive read coupling fault.

Neighborhood pattern sensitive faults

A Neighborhood pattern sensitive fault (NPSF) involves more than 2 cells. It is denoted as $\langle S_{a_0}; ...; S_{a_{m-2}}; S_v/F/R\rangle$ (m>2), where S_{a_i} is one of the aggressor cells ($i \in \{0,1...m-2\}$), m

Table 4.4: V-cell accessed coupling faults

#	Sa	Sv	F	R	Sa;Sv/F/R	Fault model	#	Sa	Sv	F	R	Sa;Sv/F/R	Fault model
1	*x*	0w0	1	-	<*x*;0w0/1/->		21	*x*	0r0	L	1	<*x*;0r0/L/1>	
2	*x*	0w0	L	-	<*x*;0w0/L/->		22	*x*	0r0	L	?	<*x*;0r0/L/?>	
3	*x*	0w0	U	-	<*x*;0w0/U/->		23	*x*	0r0	U	1	<*x*;0r0/U/1>	
4	*x*	0w0	H	-	<*x*;0w0/H/->	Write Disturb	24	*x*	0r0	U	?	<*x*;0r0/U/?>	
5	*x*	1w1	0	-	<*x*;1w1/0/->	Coupling Fault	25	*x*	0r0	H	1	<*x*;0r0/H/1>	
6	*x*	1w1	L	-	<*x*;1w1/L/->		26	*x*	0r0	H	?	<*x*;0r0/H/?>	
7	*x*	1w1	U	-	<*x*;1w1/U/->		27	*x*	1r1	0	0	<*x*;1r1/0/0>	Read Destructive
8	*x*	1w1	H	-	<*x*;1w1/H/->		28	*x*	1r1	0	?	<*x*;1r1/0/?>	Coupling Fault
9	*x*	0w1	0	-	<*x*;0w1/0/->		29	*x*	1r1	L	0	<*x*;1r1/L/0>	
10	*x*	0w1	L	-	<*x*;0w1/L/->		30	*x*	1r1	L	?	<*x*;1r1/L/?>	
11	*x*	0w1	U	-	<*x*;0w1/U/->		31	*x*	1r1	U	0	<*x*;1r1/U/0>	
12	*x*	0w1	H	-	<*x*;0w1/H/->	Transition	32	*x*	1r1	U	?	<*x*;1r1/U/?>	
13	*x*	1w0	1	-	<*x*;1w0/1/->	Coupling Fault	33	*x*	1r1	H	0	<*x*;1r1/H/0>	
14	*x*	1w0	L	-	<*x*;1w0/L/->		34	*x*	1r1	H	?	<*x*;1r1/H/?>	
15	*x*	1w0	U	-	<*x*;1w0/U/->		35	*x*	0r0	1	0	<*x*;0r0/1/0>	
16	*x*	1w0	H	-	<*x*;1w0/H/->		36	*x*	0r0	L	0	<*x*;0r0/L/0>	
17	*x*	0r0	0	1	<*x*;0r0/0/1>		37	*x*	0r0	U	0	<*x*;0r0/U/0>	
18	*x*	0r0	0	?	<*x*;0r0/0/?>	Incorrect Read	38	*x*	0r0	H	0	<*x*;0r0/H/0>	Deceptive Read
19	*x*	1r1	1	0	<*x*;1r1/1/0>	Coupling Fault	39	*x*	1r1	0	1	<*x*;1r1/0/1>	Coupling Fault
20	*x*	1r1	1	?	<*x*;1r1/1/?>		40	*x*	1r1	L	1	<*x*;1r1/L/1>	
21	*x*	0r0	1	1	<*x*;0r0/1/1>	Read Destructive	41	*x*	1r1	U	1	<*x*;1r1/U/1>	
22	*x*	0r0	1	?	<*x*;0r0/1/?>	Coupling Fault	42	*x*	1r1	H	1	<*x*;1r1/H/1>	

Note: *x* can be 0 or 1

is the number of involved cells, F is the final value of the victim cell and R is the readout value of the victim cell. With m involved cells, the fault is regarded as m-NPSF. Note that m-NPSF is also called as m-cell coupling fault (m-CF). Most commonly, only neighbor cells are normally considered relative to the selected central cell. As illustrated in Figure 4.1, the central victim cell (Cv) is coupled with eight neighbor cells, which consist of four direct neighbor cells (Ca1-Ca4) and four diagonal neighbor cells (Ca5-Ca8). Here possible NPSFs will not be listed, since the methodology to present them is similar with single cell faults and 2-cell coupling faults.

4.2. Fault Space Validation Methodology

After defining the complete memory fault space, SPICE-based circuit simulations will be performed to detect the realistic faults in the presence of predefined defects in section **??**. Next, the setups for circuit simulations will be firstly explained. Then the methodology of fault space validation will be given.

4.2.1. Circuit Simulation Setup

Figure 4.3 illustrates the architecture of STT-MRAM simulation circuit used in our work. It comprises two parts: a 3x3 memory cell array and peripheral circuits. The former consists of nine 1T-1MTJ bit cells (C0-C8), which are the most commonly adopted STT-MRAM bit cell design as introduced in section 2.4.2, the latter includes address decoders, write drivers and sense amplifiers as same as those introduced in section 2.4.3. As shown in Figure 4.3, the common word line is shared by memory cells in the common row, while memory cells in the common column share the same bit line and source line. The address decoder is

able to switch on the word line to select cells in a row. The write drivers are responsible for driving the voltage on the bit lines and source lines to perform write operations by enabling **Wr_en** and assigning desired values to **Data_in**. For example, when '1' is written into C4, $\mathbf{WL_1}$ is pulled to VDD by the address decoder, while $\mathbf{BL_1}$ is pulled down to GND and $\mathbf{SL_1}$ is pulled up to VDD by write drive 1. Other idle signals are switched off by pulling down to GND. By contrast, read operations are performed with sense amplifiers by enabling **Rd_en**. For the circuit simulations, a Verilog-A MTJ compact model is used for the MTJ devices, which is built up in [6]. Both NMOS selectors in STT-MRAM cells and peripheral circuits are built up using the predictive technology model (PTM) [99] on 45nm node.

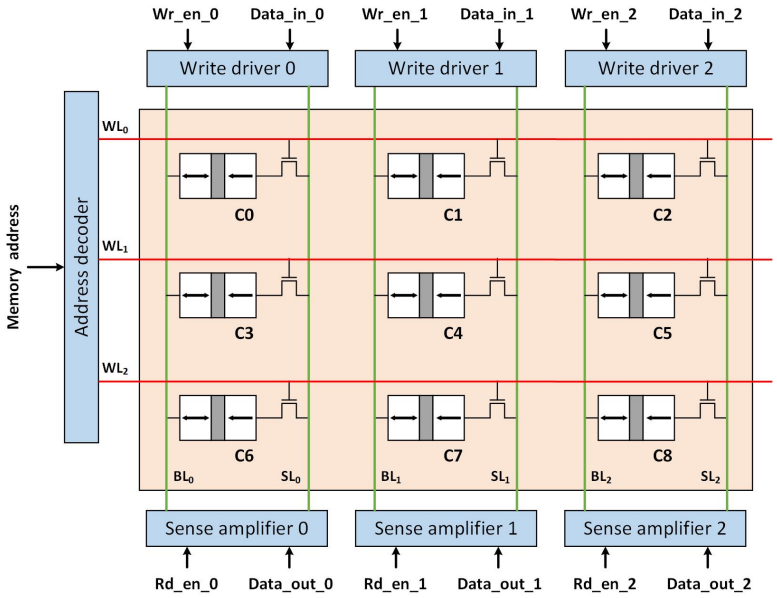


Figure 4.3: STT-MRAM simulation circuit architecture

In this thesis, we aim to investigate interconnect and contact defects in STT-MRAMs as comprehensively as possible. As discussed in chapter 3, we only need to consider four memory cells due to symmetric position, in order to define interconnect and contact defects within a cell or between cells accurately. There are eight neighbor cells relative to the selected central cell (C4) including four diagonal cells (C0, C2, C6, C8), two cells in the same column (C1, C7) and two cells in the same row (C3, C5) as shown in Figure 4.3. It is easily observed that position symmetry exists between the cells with similar relative position to the selected central cell. For example, we select C4 as the central cell in figure 4.3, C0, C2, C6 and C8 demonstrate the same location relative to C4. As a result of this, C0 is able to represent other three diagonal cells, when defects between diagonal cells are investigated. Due to the same reason, C1 and C3 are respectively able to represent all the cells in the same column and same row for the central cell C4. For our circuit simulation, we only consider the defects arising within or between C0, C1, C3 and C4.

It is worth noting that we will take data backgrounds (DBs) into account, when we run the SPICE-based circuit simulations for the predefined defects. Data backgrounds (DBs) are the combinations of neighbor cells' states, which are also well-known as neighborhood

patterns (NPs). In [100], neighborhood pattern sensitive faults (NPSFs) are theoretically investigated for random access memories. For STT-MRAM cell arrays, DBs are also expected to be considered to ensure the occurrence of the realistic fault models in the presence of interconnect ad contact defects. However, Unlike existing memory technologies such as SRAM or DRAM, there exists magnetic coupling within and between STT-MRAM bit cells, which can affect the operations on cells, possibly leading to some specific STT-MRAM faults. Therefore, it is necessary for us to consider the influence from magnetic coupling on the occurrence of faults during circuit simulations. In other words, we need to integrate the influence of magnetic coupling into our simulations reasonably. Next, we will firstly explain mechanism and influence of magnetic coupling. Then, the simulation setup with magnetic coupling will be explained.

Magnetic coupling

As the core element of STT-MRAM, MTJ devices reveal both charge and spin properties [19], different from MOSFET devices. Therefore, the performance of MTJ devices is also influenced by the magnetic field. According to the work in [19], there are three sources of magnetic field in STT-MRAMs including intra-cell magnetic coupling, inter-cell magnetic coupling and external fields, which are able to affect the performed operations on STT-MRAM bit cells. For our work, external field will not be taken into account. Therefore, we only explain intra-cell magnetic coupling and inter-cell magnetic coupling. Intra-cell stray field ($\mathbf{H}_{s\_intra}$) and inter-cell stray field ($\mathbf{H}_{s\_inter}$) are respectively the real resources of intra-cell and inter-cell magnetic coupling. The direction and value of stray field reflects the impact of magnetic coupling qualitatively and quantitatively.

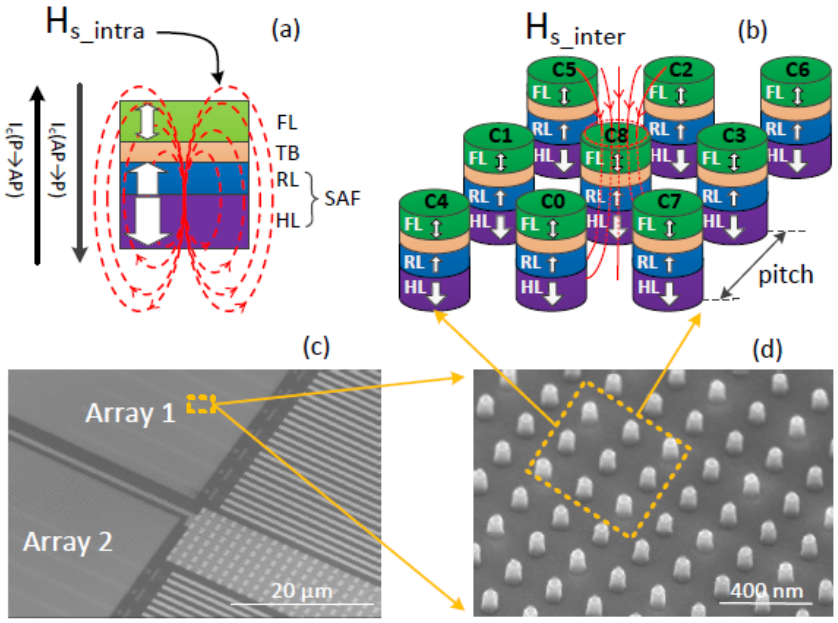


Figure 4.4: (a) Intral-cell stray field, (b) Inter-cell stray field, (c) SEM image of 0T1R wafer floor plan and (d) SEM image of MTJ array [19]

Figure 4.4(a) illustrates the mechanism of $\mathbf{H}_{\text{s\_intra}}$. There are four layers in the MTJ device: free layer (FL), tunnel barrier (TB), reference layer (RL) and hard layer (HL). FL, RL and HL are all ferromagnetic layers, each of which can generate the magnetic stray field, while TB layer is nonmagnetic insulating layer normally formed by MgO. RL and HL constitute synthetic anti-ferromagnetic (SAF) structure, which gives a strong fixed reference magnetization for FL [6]. $\mathbf{H}_{\text{s\_intra}}$ shown in Figure 4.4(a) are generated by RL and FL. It is able to impose inverse impact on the state switching processes of MTJ devices. More specifically, the switching process AP→P will be hindered by $\mathbf{H}_{\text{s\_intra}}$, if $\mathbf{H}_{\text{s\_intra}}$ has same direction with the magnetization of FL in AP state. Oppositely, the switching process P→AP will be promoted, when $\mathbf{H}_{\text{s\_intra}}$ is parallel with the magnetization of FL in AP state. The essence of this phenomena is attributed to the difference caused by $\mathbf{H}_{\text{s\_intra}}$ between E_B(AP→P) and E_B(P→AP), which respectively correspond to energy barrier from AP to P state and from P to AP state. In our work, the direction of $\mathbf{H}_{\text{s\_intra}}$ is set to be same with the magnetization of FL in AP state in accordance with the work in [19]. Note we only consider the component of $\mathbf{H}_{\text{s\_intra}}$ along with the magnetization of ferromagnetic layers, since other components nearly have no impact on the performance of MTJ devices.

$\mathbf{H}_{\text{s\_intra}}$ exists in each STT-MRAM bit cell. Unlike $\mathbf{H}_{\text{s\_intra}}$, $\mathbf{H}_{\text{s\_inter}}$ becomes increasingly nonnegligible, when the STT-MRAM array achieves sufficiently high density. In other words, the narrower the distance between memory cells is, the more evident the influence of inter-cell magnetic will be. Figure 4.4(b) illustrates the effect of $\mathbf{H}_{\text{s\_inter}}$ from eight neighbor cells (C0-C7) on the central cell C8. Pitch represents the spacing between adjacent cells. Eight neighbor cells include four direct neighbor cells and four diagonal neighbor cells, while unneighbor cells are not considered due to negligible influence. Figure 4.4(c) and (d) respectively show the SEM image of 0T1R wafer floor plan and MTJ array [19].

Compared with $\mathbf{H}_{\text{s\_intra}}$, the impact of $\mathbf{H}_{\text{s\_inter}}$ is much more complicated, since this involves multiple memory cells. In [19], $\mathbf{H}_{\text{s\_inter}}$ was investigated based on a 3X3 MTJ array as shown in Figure 4.4(b). Each neighbor cell imposes their own $\mathbf{H}_{\text{s\_inter}}$ on the central cell. The magnitude of $\mathbf{H}_{\text{s\_inter}}$ is dependent on the spacing between cells, while the direction of $\mathbf{H}_{\text{s\_inter}}$ relies on the state of the bit cell. For example, $\mathbf{H}_{\text{s\_inter}}$ from cell in AP state generates totally opposite effect compared with the cell in P state. Therefore, there are 256 combinations of neighbor cells' states to represent the influence of $\mathbf{H}_{\text{s\_inter}}$ on the central cell. Neighborhood patterns (NP_8) are used as the denotation for these 256 combinations. NP_8 is in the form of $\{S_0S_1S_2S_3S_4S_5S_6S_7\}$, where S_i is '1' or '0' representing the state of neighbor cells. For instance, NP_8 = 11111111(255) means that all neighbor cells are in AP state, while NP8 = 00000000(0) means that all neighbor cells are in P state. Note that the inter-cell magnetic coupling from diagonal neighbor cells is weaker than that from direct neighbor cells.

Figure 4.5 gives the quantitative illustration of $\mathbf{H}_{\text{s\_inter}}$ imposed on the central cell in the 3x3 memory array under various combinations of neighbor cells' states. The vertical axis represents the value of $\mathbf{H}_{\text{s\_inter}}$, while other two horizontal axes respectively stand for the number of direct neighbor cells and diagonal neighbor cells in '1' state. The positive direction of the $\mathbf{H}_{\text{s\_inter}}$ axis is parallel to the magnetization of the central cell's FL in P state, while the negative one corresponds to AP state. As a result of this, when the number of 1s in neighbor cells increases, the processes of P→AP and AP→P respectively need

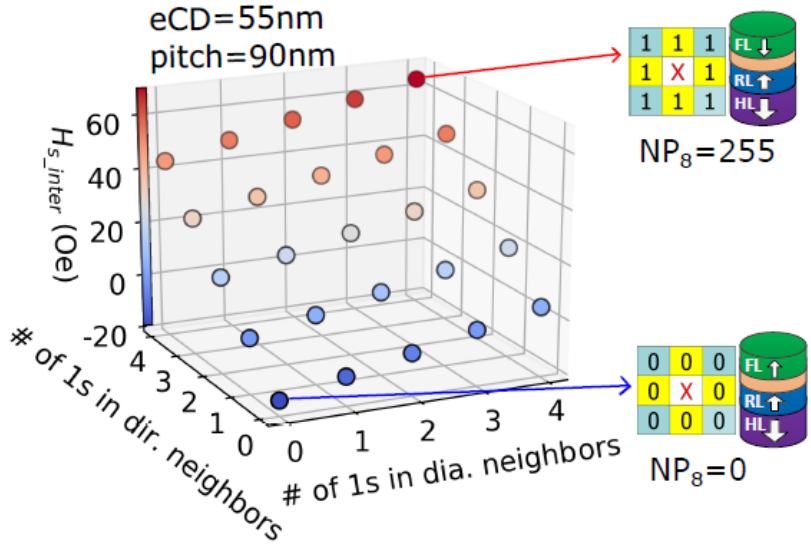


Figure 4.5: $\mathbf{H}_{s\_inter}$ at the FL of the central cell under various combinations of the number of 1s in direct neighbors and diagonal neighbors. [19]

higher and lower switching current to overcome the higher and lower energy barrier for the central cell. If more and more neighbor cells are in '0' state, the generated $\mathbf{H}_{s\_inter}$ demonstrates completely opposite influence. In Figure 4.5, there are only 25 points to represent $\mathbf{H}_{s\_inter}$ under 256 neighborhood patterns (NP_8). This is because all the direct neighbor cells generate same $\mathbf{H}_{s\_inter}$ for the central cell and the same rule applies to all the diagonal cells. From Figure 4.5, it is easily observed that $\mathbf{H}_{s\_inter}$ reaches the maximal positive value with NP_8 = 11111111(255), while the influence of $\mathbf{H}_{s\_inter}$ is negatively maximal under NP_8 = 00000000(0). Based on the analysis before, the highest switching current is needed for the process P→AP with NP_8 = 255, By contrast, the process of AP→P the highest switching current with NP_8 = 0. Therefore, we regard NP_8 = 11111111 and NP_8 = 00000000 as two worst cases for switching processes in STT-MRAMs.

Simulation setup with data backgrounds

Since we investigate the defects in the memory cell array, we focus most on the influence of inter-cell magnetic coupling. Note that we will use data backgrounds(DBs) to represent inter-cell magnetic coupling. Figure 4.6 illustrates the circuit simulation setup in our work. Note that only defects between or within C0, C1, C3 and C4 are considered as explained in chapter 3. All eight neighbor cells generate inter-cell stray field for the central cell as shown in Figure 4.6. $\mathbf{H}_{dir}$ represents the stray field from direct neighbor cells, while $\mathbf{H}_{dia}$ is for diagonal neighbor cells. For our circuit simulation, we only consider two worst cases among all the data backgrounds(DBs). It is clear that all of neighbor cells are set to '1' or '0' as shown in the right part of Figure 4.6. We do not need to do simulations under all data backgrounds, since faults occur most easily under the worst cases and all sensitized faults will be covered by these two cases. In this way, not only the simulation time can be saved, but also the realistic fault models can be detected in benefice of developing the effective

test solutions for interconnect and contact defects in STT-MRAMs. Note that we will use ↑ and ↓ to represent two worst cases in this thesis. ↑ means states of all neighbor cells are '1', while ↓ indicates all neighbor cells are in '0'.

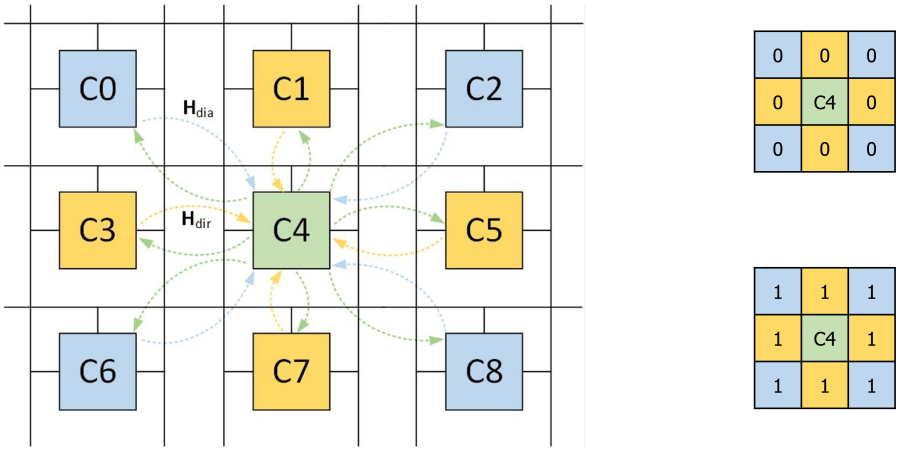


Figure 4.6: Circuit simulation setup

Note that we need to verify the correctness of the circuit simulation in the defect-free case before injecting the predefined defects. Figure 4.7 and 4.8 give the waveform of the defect-free case simulation for sequences 1w0r0w1r1 under ↓ and ↑ setups respectively. It can be clearly seen that both write and read operations are performed normally under both ↓ and ↑ setups. After this, the circuit simulations in the presence of defects can be implemented further.

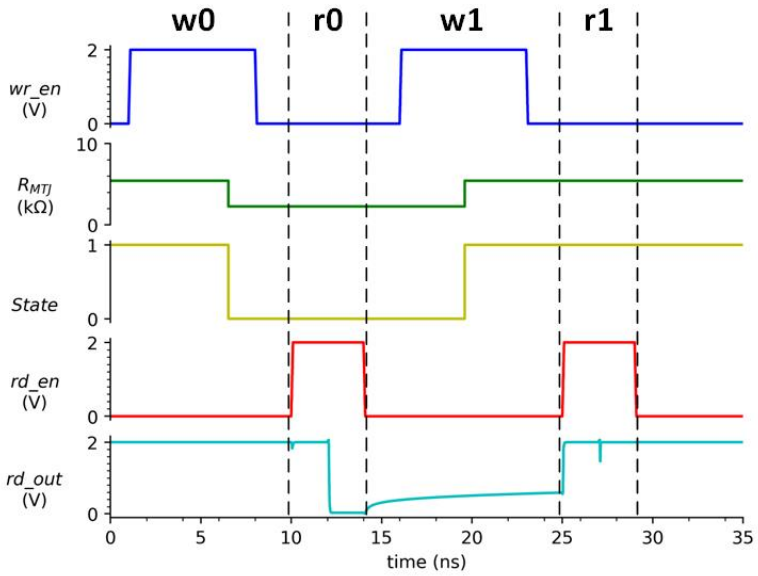


Figure 4.7: Defect-free simulation for 1w0r0w1r1 under ↓ setup (pitch=90nm)

In this thesis, electrical critical diameter (eCD) of the MTJ device is 60nm, which is con-

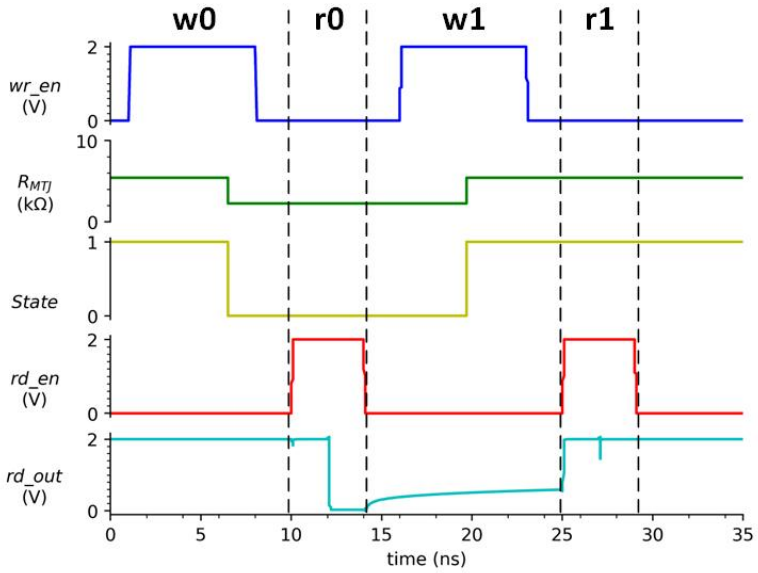


Figure 4.8: Defect-free simulation for 1w0r0w1r1 under ↑ setup (pitch=90nm)

sistent with the work in [6]. The pitch between memory cells in the test circuit will be set to 1.5eCD (90nm) based on the work in [101]. In order to investigate the influence of inter-cell magnetic coupling on fault models separately, the circuit simulation under pitch=200nm is also implemented, where the impact of inter-cell stray field can be neglected [6].

4.2.2. Methodology

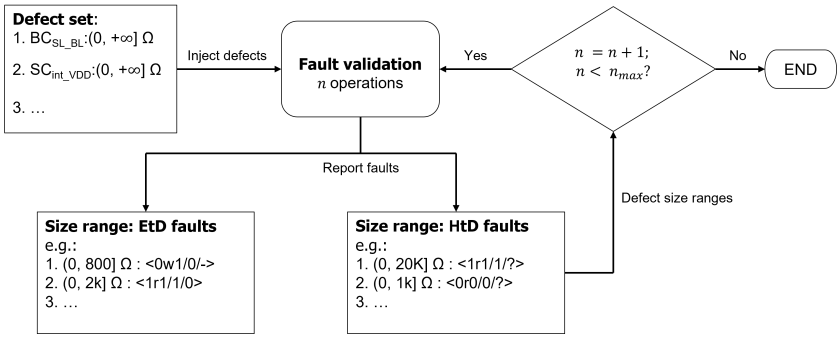


Figure 4.9: Fault space validation methodology

After explaining the circuit simulation setup, the predefined fault space will be validated on a Python-based simulation platform that controls simulations automatically. Figure 4.9 illustrates the fault space validation methodology. Targeted on the predefined defects and defects size ranges for simulations, fault validation will be processed repeatedly. The sensitized faults are reported as EtD faults or HtD faults in the form of {Size range : faults}. When all defect size ranges are swept for n operations, the fault validation will be further implemented for n+1 operations. For example, dynamic faults (n ≥ 2) will be analysed af-

ter validating all the static faults. When the maximal n is reached, the fault validation is finished. Note that although we limit the focus point to static faults, our python-based simulation platform can be applied to the analysis for dynamic faults.

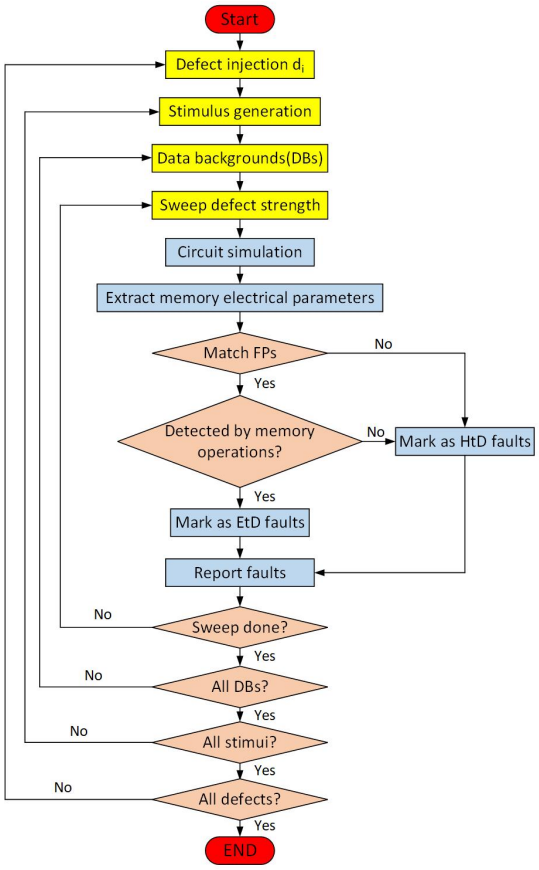


Figure 4.10: Flow chart of fault space validation

Figure 4.10 shows the steps of fault space validation in more detail. Firstly one of the predefined defects in chapter 3 is injected as a linear resistor into the netlist of the shown STT-MRAM test circuit in Figure 4.3, followed by generating all possible stimulus such as 0w0 and 0r0. Since we only investigate static faults, stimulus belong to {0, 1, 0w0, 1w1, 0w1, 1w0, 0r0, 1r1}. Each time one of these operations will be performed on the central cell C4 in Figure 4.3 under two considered data backgrounds (DBs) : ↑ and ↓. The value of the modeled linear resistance is swept from 1Ω to 100MΩ, which is regarded as the defect size and is logarithmically distributed with 81 defect size points in our simulations. Each time the simulation is finished, the desired electrical parameters of C0, C1, C3 and C4 such as resistance of MTJ devices are extracted from the measurement files to determine whether any faults in the fault space occur or not. If the sensitized faults can not be described by fault primitives (FPs), they belong to weak faults and will be marked as HtD faults. If yes and the faults can be detected by normal read/write operations, they will be reported as EtD faults. Otherwise the faults are still labeled with HtD faults. This fault classification is consistent with Figure 2.26 All the simulation steps are repeated for each injected defect

until everything is down.

5

Fault Modelling Results & Analysis

This chapter discusses the results of fault space validation under various circuit simulation setups. Firstly, fault validation results are given in the form of fault maps, which clearly reflect the defect strength ranges, where faults occur with specific operations. Then the detected fault models are analyzed by comparing the results under different setups. Finally, validated faults in our work are simply compared with the existing fault models caused by interconnect and contact defects in STT-MRAMs.

5.1. Fault Validation Results

Based on the proposed fault validation methodology in section 4.2, SPICE-based circuit simulations are implemented to investigate the realistic faults in the presence of the predefined defects in section 3. The simulation results are shown in the form of the fault maps as illustrated in Table 5.1. We take one defect (BC6) as an example to explain the delivered information from the fault map. Note that results for all defects are placed in appendix A.

Table 5.1: Fault map for BC6 defect. Fault-free EtD HtD

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	251.1	794.3	1k	2k	3.2k	10k	100k	251.2k	1M	10M	100M
BC6	no	1w0													
		0r0													
		1r1													
	↑	1w0													
		0r0													
		1r1													
	↓	1w0													
		0r0													
		1r1													

Table 5.1 shows the fault validation results for BC6 defect, which is a bridge defect between the internal node and the word line within a cell as shown in Figure 3.5. As discussed in section 4.2.1, we consider two worst cases ↑ and ↓ for inter-cell magnetic coupling as depicted in Figure 4.6 under pitch=90nm. Apart from these two setups, we also run the circuit simulation under pitch=200nm, in order to investigate the influence of inter-cell stray

field on the faults caused by interconnect and contact defects. Note that the inter-cell stray field can be neglected under pitch=200nm, while ↑ and ↓ respectively means that all neighbor cells are set to '1' (DB=11111111) and '0' (DB=00000000). Therefore, we obtained three group of results, which correspond to three blocks for 'no', '↑' and '↓' in the fault map respectively. Targeted on each setup, the fault map gives the defect strength ranges, where EtD or HtD faults are sensitized by specific sequences. If EtD faults occur at specific defect strength, it will be labeled with green color. By contrast, yellow color means only HtD faults are detected. From this fault map, it can be seen that under no inter-cell magnetic coupling, when 1w0 is performed on the central cell C4 in our test circuit, EtD faults are detected within defect strength range $[1\Omega, 10k\Omega)$. Within $[1\Omega, 794.3\Omega)$, 0r0 sensitizes EtD faults, while this sequence sensitizes HtD faults in $[794.3\Omega, 3.2k\Omega)$. For 1r1 operation, HtD faults arise in $[1k\Omega, 3.2k\Omega)$ before the occurrence of EtD faults in $[3.2k\Omega, 251.2k\Omega)$. It is easily observed that the covered defect strength ranges are completely identical for these three $\mathbf{H}_{\text{s\_inter}}$ setups. However, more details about fault results can not be reflected by fault maps. For example, it is not revealed that what faults are sensitized by 1w0 sequence under no $\mathbf{H}_{\text{s\_inter}}$. In section 4.1.2, diverse 0w1 sensitized faults are defined in complete fault space. As a result of this, we generate fault tables such as Table 5.2 to present the fault space validation results in more detail. Here we still take BC6 as an example case to explain the table.

Table 5.2: Sensitized faults for BC6 defect

Defect	Inter-cell magnetic coupling	Defect strength	S	F	R
BC6	no & ↑ & ↓	(0, 794.3)	1w0	1	-
			0r0	0	1
		[794.3, 1k)	1w0	1	-
			0r0	0	?
		[1k, 3.2k)	1w0	1	-
			0r0	0	?
			1r1	1	?
		[3.2k, 10k)	1w0	1	-
			1r1	1	0
		[10k, 251.2k)	1r1	1	0

As a supplement for the fault map, Table 5.2 gives more details for fault validation results under three setups. For BC6 defect, same faults are sensitized in the same defect strength ranges under all three setups as demonstrated in Table 5.2. Corresponded to the results in fault map, <1w0/1/-> is sensitized in $[0\Omega, 10k\Omega)$, which belongs to EtD faults. <0r0/0/1> occurs in $[0\Omega, 794.3\Omega)$, while <0r0/0/?> is detected in $[794.3\Omega, 3.2k\Omega)$. Note that <0r0/0/?> is regarded as the HtD fault, since the read-out value is random. Similarly <1r1/1/?> and <1r1/1/0> arise in different defect strength ranges respectively as HtD and EtD faults. For BC6 defect, inter-cell magnetic coupling are not strong enough to affect the sensitized faults. Actually we found that fault validation results for some other predefined defects are not identical under no, ↑ and ↓ after checking all the results, which is an attractive phenomena. In this section we only explain how the results are presented. In

next section, we will analyse the possible reasons behind this phenomena and investigate it further.

5.2. Fault Models Analysis

In this section, we do some analysis for the validated faults. Figure 5.1 shows the relationship between faults under three setups. Red circle represents all the faults sensitized under ↑ setup, while green circle is for the detected faults under ↓ setup. Blue one with dash lines corresponds to the results under no inter-cell magnetic coupling (pitch=200nm). The faults under three setups are divided into five regions: A, B, C, D, E. The faults in region A are those sensitized under all of no, ↑ and ↓ magnetic coupling. Region B includes the detected faults only under no and ↑ magnetic coupling, while the faults only under ↓ and no magnetic coupling forms the region C. Faults in region D can only be sensitized by setting all neighbor cells in '1'. Oppositely, holding all neighbor cells in '0' is the requirement for sensitizing the faults in region E. After checking results, we found that faults in region A are single-cell faults, while most faults in region B and C are a-cell accessed coupling faults. Compared with those, the faults in region D and E seem to be specific STT-MRAM faults and demonstrate the greatest influence of $\mathbf{H}_{s\_inter}$. Therefore, we focus on these two regions next, in order to find some novel faults.

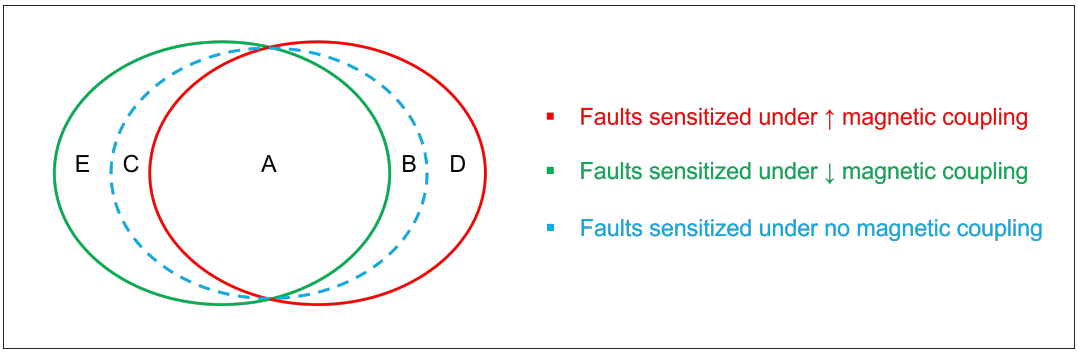


Figure 5.1: Relationship between sensitized faults under three setups

Region D consists of some faults in the presence of SS2 and SB1 defect, while region E comprises certain faults caused by OS_w and SC2 defect. The locations and descriptions for these four defects are given in chapter 3. Here we take one defect from each region as example cases to illustrate what are exactly in these two regions.

Table 5.3 and 5.4 show the fault maps for SS2 and OS_w respectively. It is easily observed that 0w1 sensitized EtD faults in $[793.4\Omega, 1k\Omega)$ occur only under ↑ setup and other faults cover the same defect strength ranges under all three setups in the presence of SS2 defect. In other words, the covered defect strength ranges are extended for 0w1 operations, if all neighbor cells are in logic '1'. This is possibly attributed to the explained mechanism of inter-cell magnetic coupling in section 4.2.1. When all neighbor cells are kept in AP state (DB=11111111), $\mathbf{H}_{s\_inter}$ imposed on the central cell is positively maximal. The positive direction of $\mathbf{H}_{s\_inter}$ is same with FL's magnetization in P state. Therefore, the switching process of P→AP is discouraged to an extreme extend by $\mathbf{H}_{s\_inter}$ generated by neighbor

cells. SS2 is a short defect, which easily causes faults at low defect strength. When the defect strength becomes high enough, the influence of $\mathbf{H}_{s\_inter}$ dominates the fault sensitization. As a result of this, longer defect strength ranges with faults are covered by ↑ compared with no and ↓ magnetic coupling, if 0w1 operations (P→AP) are performed. For SB1 defect included in region D, some faults are also sensitized by 0w1 operations at higher defect strength, only when DB is 11111111.

Table 5.3: Fault map for SS2 defect. Fault-free EtD HtD

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	794.3	1k	1.6k	2k	10k	100k	1M	10M	100M
SS2	no	0w1														
		1r1														
	↑	0w1														
		1r1														
	↓	0w1														
		1r1														

Different from the fault result for SS2 defect, ↓ setup lengthens the defect strength ranges covered by 1w0 sensitized faults in the presence of OS_w defect. The faults in $[501.2\Omega, 631\Omega)$ can only be sensitized by 1w0 operations under all neighbor cells in P state, which is consistent with the analysis for inter-cell stray field in section 4.2.1 as well. When data background is 00000000, the generated $\mathbf{H}_{s\_inter}$ reaches the negative peak, the direction of which is same with the magnetization of FL in AP state. That means the switching process of AP→P (1w0) is hindered most under ↓ setup. Note that unlike SS2 defect, OS_w is a open defect that easily contributes to faults at high defect strength. The lower defect strength is, the more evident the effect of $\mathbf{H}_{s\_inter}$ for OS_w defect is. Therefore, within $[251.1\Omega, 501.2\Omega)$, extended defect strength ranges occur under ↓ setup. For another defect (SC2 defect) in region E, some 1w0 faults are only detected under ↓ setup as well.

Table 5.4: Fault map for OS_w defect. Fault-free EtD HtD

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	631	1k	1.6k	2.5k	10k	100k	1M	10M	100M
OS_w	no	0w1														
		1w0														
	↑	0w1														
		1w0														
	↓	0w1														
		1w0														

Based on the above analysis for region D and E in Figure 5.1, it can be seen that $\mathbf{H}_{s\_inter}$ under ↑ setup promotes the occurrence of 0w1 sensitized faults, while 1w0 operations are discouraged by $\mathbf{H}_{s\_inter}$ under ↓ setup. In order to verify the influence of inter-cell magnetic coupling on the faults caused by interconnect and contact defects, we decided to run circuit simulation under various spacing between cells, which are represented by the value of pitch. In this thesis, we only take SS2 defect for this to demonstrate the impact of $\mathbf{H}_{s\_inter}$ further. Note that the before shown faults for ↑ and ↓ are validated under pitch=1.5eCD (90nm) and the simulations for no magnetic coupling are run under pitch=200nm. Now we set the minimal pitch to 1.1eCD(66nm) and set the maximal pitch as 200nm. Figure

5.2 shows the percentage of the extended defect strength ranges relative to results under pitch=200nm, where $\mathbf{H}_{s\_inter}$ can be neglected. For example, the maximal covered defect strength by 0w1 operations is extended from 794.3Ω to 1kΩ under ↑ setup, when pitch is 90nm. We regard the extended defect strength ranges as the undetected faults under no magnetic coupling. Therefore, the percentage of the missing 0w1 sensitized faults will be around 25 % , if we ignore the inter-cell magnetic coupling. When the STT-MRAM array has higher density, the missing part has higher percentage, even over 30%. By contrast, the wider spacing between cells is, the less missing faults are. Therefore, the inter-cell magnetic coupling must be taken into account, in order to detect all the faults caused by interconnect and contact defects.

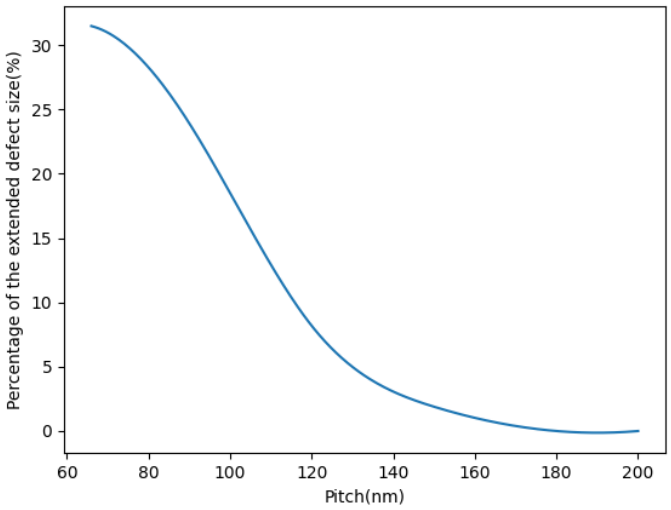


Figure 5.2: Percentage of extended defect strength ranges for SS2 defect under various pitches

According to the above analysis for the influence of $\mathbf{H}_{s\_inter}$, both ↑ and ↓ magnetic coupling cause uncovered faults compared with no magnetic coupling. As discussed in section 4.1.2, the complete fault space consists of single-cell faults (SCFs), 2-cell coupling faults (2-CFs) and neighborhood pattern sensitive faults(NPSFs). For our work, it is easily observed that the faults covered in region A belong to SCFs, since they are sensitized under both ↑ and ↓, which are two worst cases. In other words, these faults only involve one cell. By contrast, faults in region B, C, D and E involve more than one cell and are 2-CFs or NPSFs. Because we do not run the circuit simulation for all 256 data backgrounds(DBs) as introduced in section 4.2.1, the number of involved cells for these faults can not be accurately decided. Therefore, we determined to focus on the faults in region D and E, where specific STT-MRAM faults occur with higher possibility due to the dominant influence of $\mathbf{H}_{s\_inter}$.

Here we take SS2 for example to explain how to investigate the targeted regions. In the presence of SS2, the faults in $[794.3\Omega, 1k\Omega)$ are sensitized by 0w1 operation only under ↑ setup. ↑ means DB=11111111 with pitch=90nm in our work. As illustrated in Figure 3.4, DB=11111110 is the data background, $\mathbf{H}_{s\_inter}$ of which is closest to that of DB=11111111.

Note that the only cell in '0' belongs to one of the four diagonal cells, since $\mathbf{H}_{s\_inter}$ generated by the diagonal cell is smaller than the direct neighbor cell. Therefore, we decided to implement fault space validation under DB=11111110 as well, where one diagonal cell is in '0'. The fault results are same with that under no and $\downarrow \mathbf{H}_{s\_inter}$ shown in Table 5.3. The 0w1 sensitized faults in $[794.3\Omega, 1k\Omega)$ under DB=11111111 do not occur under DB=11111110. That means all of the neighbor cells are involved for the faults in $[794.3\Omega, 1k\Omega)$. Therefore, these faults can be denoted as <1;1;1;1;1;1;1;1;0w1/0/->. They belong to passive neighborhood pattern sensitive faults (PNPSFs) [80], which involve all the neighbor cells. The same method is applied to another defect (SB1) in region D. <1;1;1;1;1;1;1;1;0w1/0/-> is also observed. For defects in region E, circuit simulation under DB=00000001 is run and <0;0;0;0;0;0;0;0;1w0/1/-> is observed. Therefore, the observed specific STT-MRAM faults are <1;1;1;1;1;1;1;1;0w1/0/-> and <0;0;0;0;0;0;0;0;1w0/1/-> in our work. The classification of faults in region B and C can be investigated as the future work.

5.3. Comparison between Fault Models

In section 2.5.2, we introduce some existing fault models in STT-MRAMs such as transition fault (TF) and incorrect read fault (IRF). All of these faults are observed in the presence of interconnect and contact defects in [17, 86], but inter-cell magnetic coupling is not considered in these works, which leads to difference between the observed faults and realistic faults. In our work, the influence of $\mathbf{H}_{s\_inter}$ is taken into account, when we investigate interconnect and contact defects in STT-MRAMs. Figure 5.3 illustrates the general difference between the observed faults in our work and the existing fault models caused by interconnect and contact defects in STT-MRAMs.

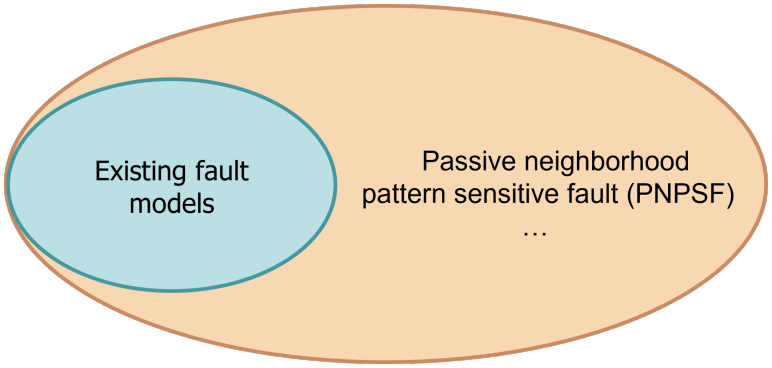


Figure 5.3: Comparison between fault models caused by interconnect and contact defects

In our work, the existing fault models in previous works are all sensitized. Apart from these faults, we observed <0;0;0;0;0;0;0;0;1w0/1/-> and <1;1;1;1;1;1;1;1;0w1/0/-> under inter-cell magnetic coupling in region D and E as shown in Figure 5.1. We regard these two faults as one fault model: passive neighborhood pattern sensitive fault (PNPSF), which involves all of the neighbor cells in the memory array and occurs during state switching process. This fault model is not observed in previous work for interconnect and contact defects in STT-MRAMs due to not considering $\mathbf{H}_{s\_inter}$. In other words, our work presents realistic fault models more comprehensively compared with previous work. Note that since we did

not run simulation under all 256 data backgrounds(DBs), the faults in region B and C in Figure 5.1 can not be classified based on the number of involved cells. As a result of this, '...' appears in Figure 5.1, which means that there are possibly still other specific faults in need of further investigation in the future.

Table 5.5: Observed fault models in previous work and our work

Fault models	Observed in previous work	Observed in our work
TF	Y	Y
IRF	Y	Y
RDF	Y	Y
CFwd	Y	Y
PNPSF	N	Y
...	N	P

Table 5.5 gives more detail about the observed fault models in previous work and our work. In this table, for the listed fault models, "Y" denotes that the fault model is observed, while "N" denotes that the fault model is not observed and "P" denotes that the fault model is possibly observed in need of further investigations.

In the previous work [17, 86], transition fault (TF) is observed in the presence of resistive defects such as opens at BL, SL or WL. In our work, TF is also caused by various defects like bridges within the cell. IRF means the stored data keeps stable during read operations, but read-out value is wrong. This type of faults is caused by open defects at SL or WL in [17, 86], which is validated in this thesis under most of the predefined defects in chapter 3. Read destructive fault (RDF) is also observed both in previous work and our work. Compared with the first three fault models, Write disturb coupling fault (CFwd) is more complicated and involves two cells. When write operations are performed on one cell, the state of another cell will be forced to the inverse state. This is what CFwd means. From Table 5.5, we can see that this type of fault models is observed both in the previous work and our wrok. For example, CFwd is reported in [86] when the word lines in two columns are inadvertently connected. In our work, CFwd is caused by some bridge defects such as dBCC11, which is a undesired connection between the internal node of C4 and the word line of C1.

Apart from these existing fault models, the most evident difference between the works in [17, 86] and our work is the observation for passive neighborhood pattern sensitive fault (PNPSF). In our work, the influence of inter-cell magnetic coupling is considered compared with works in [17, 86]. This specific property of STT-MRAM dominates the fault sensitization at some specific defect strength. For example, <1;1;1;1;1;1;1;1;0w1/0/-> is caused by SS2 defect only within $[794.3\Omega, 1k\Omega)$. In [17, 86], this specific fault model is missed out due to ignoring magnetic coupling.

In Table 5.5, '...' can be seen in the last row for the listed fault models. That indicates that there are possibly still some other types of fault models in STT-MRAMs such as the faults that may involves 3 cells or more. In [17, 86], these possible faults can not be verified because of neglection for magnetic coupling. However, these faults are possibly observed in our work, if we perform simulations under more DBs targeted for the faults in region B and C shown in Figure 5.1. In conclusion, our work is able to observe more realistic fault

models compared with the previous works.

6

Test Solution Development & Verification

This chapter illustrates how we develop the effective test solution for the validated faults in chapter 5, Firstly we explain data backgrounds(DBs)-based ILP method used for selecting optimized DBs. Then similar method named sequence-based ILP method is discussed and we present the chosen sequences under optimized DBs to detect all realistic faults in the presence of predefined interconnect and contact defects in STT-MRAMs. Next the proposed test solution is verified by applying it to the test circuit to compare the fault coverage with validation results in chapter 5. Finally we simply compare the proposed test algorithm in our work with existing test solutions for interconnect and contact defects in STT-MRAMs.

6.1. Test Solution Generation

In order to detect the faults in previous chapter, we need to develop the effective test solution. Figure 6.1 shows the whole procedure of test solution generation in our work. For fault space validation results, we firstly utilized data backgrounds(DBs)-based ILP method to select the optimized DBs, since we considered two worst cases for inter-cell magnetic coupling. Then, sequence-based ILP method is made of use to choose optimized sequences under the optimized DBs. Finally effective march test algorithm is generated to cover all EtD faults. The procedure of test solution generation is integrated into our Python-based simulation platform. Note that since all HtD faults are either <0r0/0/?> or <1r1/1/?>, for which the specific DfT techniques are needed, we only discuss the test solution for EtD faults in this section. The test solution for HtD faults can be investigated as the future work.

6.1.1. Data Backgrounds(DBs)-based ILP Method

In our work, we consider DB=11111111 and DB=00000000 for the circuit simulations under pitch=90nm. It is obvious that the increased number of DBs increases the complexity and time cost for the testing procedure. As a result, we decided to select the minimal number of DBs, which are able to cover all EtD faults. The used method is called DBs-based ILP method, which is learned from the work in [102]. The key idea of this method is to transfer

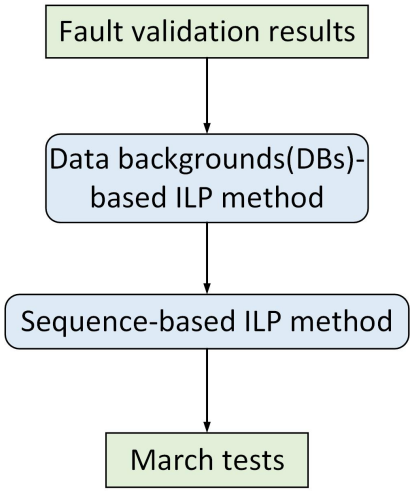


Figure 6.1: Procedure of test solution generation

the selection for DBs into solving the integer linear programming(ILP) problem. In other words, the desired DBs are being selected under various constraints. Figure 6.2 illustrates the general process of this method. The selected DBs must meet the requirements for the minimal number and highest fault coverage. Here we take Table 6.1 as an example case to explain the principles of this method.

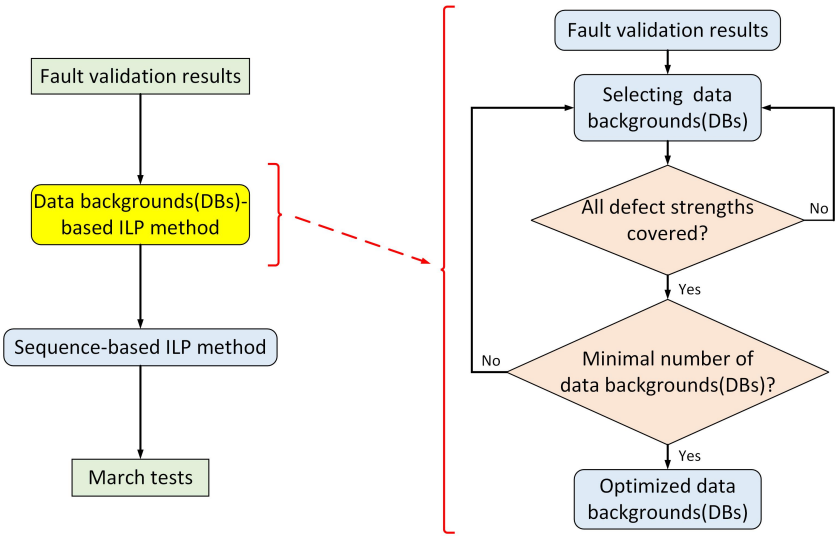


Figure 6.2: Data backgrounds(DBs)-based ILP method

In Table 6.1, two defects and two DBs are considered. It is a binary matrix consisting of n rows and m columns. Each row corresponds to each defect strength that sensitizes a fault at least, while each column demonstrates the fault results under each data backgrounds(DBs). If a fault is detected at jth defect strength under ith DB, the corresponding element $a_{j,i}$ will be '1'. Otherwise, the value is '0' that means no faults are sensitized. The last column lists the sum of element value for each defect strength. For example, faults

occur both under ↑ and ↓ at 1Ω, $\sum_{i=1}^{m} a_{j,i}$ will be 2. The last row ($S_{selected}$) indicates which DBs will be selected to meet the given constraints. '1' represents that ith DB will be selected, while '0' means it is not the desired one. Therefore, how to select the optimized DBs is equal to solving the ILP problem. The problem can be mathematically described as follows:

$$min \sum_{i=1}^{m} c_i \cdot S_{selected,i} \quad \text{subject to: } \sum_{i=1}^{m} a_{j,i} \cdot S_{selected,i} \geq 1 \text{ for all rows } j \tag{6.1}$$

where $S_{selected,i} \in \{0,1\}$ and c_i is element of the weight matrix for each data background. In our work, all of c_i is set to '1', since we regard ↑ and ↓ as totally same. In formula 6.1, the first part guarantees that the number of the selected data backgrounds is minimal, while the second part ensures that each listed defect strength is covered by the selected DBs. With this method, the optimized DBs can be obtained for further selection for sequences. In Table 6.1, ↑ and ↓ are both selected for the example case. For our realistic fault results, the selected DB is 00000000(↓), under which all defect strength can be covered. In next section, we will utilize similar method to select the optimized sequences for ↓.

Table 6.1: Example to illustrate DBs-based ILP method

			Data backgrounds(DBs)		$\sum_{i=1}^{m} a_{j,i}$
			1	2	
			11111111(↑)	00000000(↓)	
Defect 1	1	1Ω	1	1	2
	2	10Ω	1	1	2
	⋮	⋮	⋮	⋮	⋮
	j	10MΩ	1	0	1
	j+1	100MΩ	1	0	1
Defect 2	j+2	1Ω	1	1	2
	j+3	10Ω	1	1	2
	⋮	⋮	⋮	⋮	⋮
	n-1	10MΩ	0	1	1
	n	100MΩ	0	1	1
$S_{selected}$			1	1	

6.1.2. Sequence-based ILP Method

After determining the optimized DBs, the next step is to choose the optimized sequences. Figure 6.3 shows the key idea of sequence-based ILP method, which is similar with the method in the previous section. For validated faults under selected DBs in last step, the desired sequences are expected to cover all the sensitized faults and the total number of sequences should be minimized. To explain this step more clearly, example in Table 6.2 is given. Unlike the example in Table 6.1, we focus on different sequences such as 0w1(↓) or 1w0(↑) in Table 6.2. For this given example, we assume that the optimized data background is 00000000(↓). Since we are limited to static faults in this thesis, the considered sequences are 0w0, 1w1, 0w1, 1w0, 0r0 and 1r1. Based on formula 6.1, the selected sequences are 0w1(↓) and 1w0(↓) for the given example. For results in our work, the selected sequences are 1w0(↓), 0r0(↓) and 1r1(↓), which can be used to develop the effective test solution for interconnect and contact defects in STT-MRAMs.

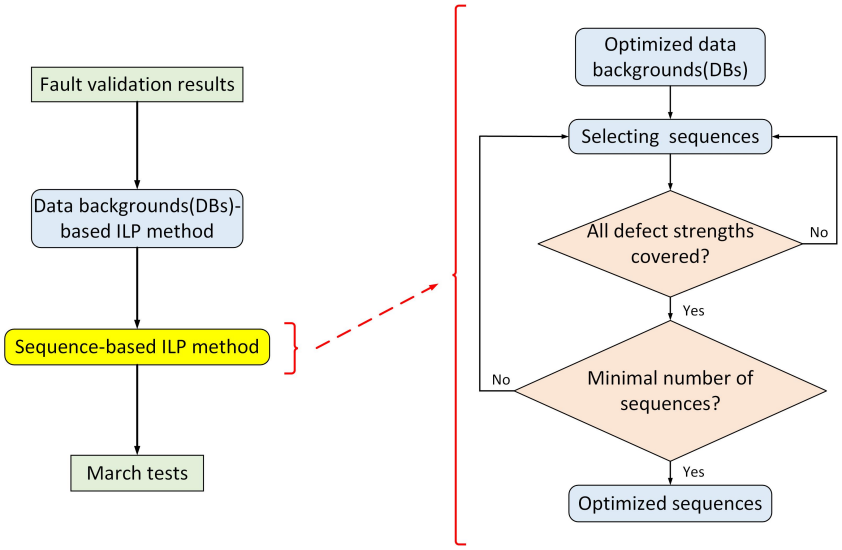


Figure 6.3: Sequence-based ILP method

Table 6.2: Example to illustrate Sequence-based ILP method

			Sequences						$\sum_{i=1}^{m} a_{j,i}$
			1	2	3	4	5	6	
			0w0(↓)	1w1(↓)	0w1(↓)	1w0(↓)	0r0(↓)	1r1(↓)	
Defect 1	1	1Ω	0	0	1	1	1	1	4
	2	10Ω	0	0	1	1	1	1	4
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	j	10MΩ	0	0	1	1	0	0	2
	j+1	100MΩ	0	0	1	0	0	0	1
Defect 2	j+2	1Ω	0	0	0	1	1	1	3
	j+3	10Ω	0	0	0	1	1	1	2
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	n-1	10MΩ	0	0	0	1	1	1	3
	n	100MΩ	0	0	0	1	0	0	1
$S_{selected}$			0	0	1	1	0	0	

6.1.3. Test Solution

After applying DBs-based ILP method and sequence-based ILP method to the fault space validation results, we obtained the optimized sequences that are able to cover all EtD faults. These sequences are shown as follows:

$$S_{EtD} \in \{1w0(\downarrow), 0r0(\downarrow), 1r1(\downarrow)\}$$

Above sequences are used to develop the march test for the realistic faults. The March test algorithm for detecting all EtD faults is given as follows:

$$\text{March-EtD} = \{\Updownarrow(w0); \Updownarrow(r0, w1, r1, w0, r0); \Updownarrow(r0)\}$$

where $\Updownarrow$ is the denotation of the random addressing orders. This march test algorithm (7N) consists of three march elements, each of which corresponds to the set of opera-

tions in parenthesis. The set of operations in one march element is applied to each bit cell in defined addressing order, after which the operations in next march element will be performed. In the proposed march test algorithm, the first march element ⇳ (w0) is used to write '0' into all bit cells in the memory array to make the initial data background as 00000000(↓). Compared with the first march element, the second one is more complex. In the second march element, the last four operations (w1,r1,w0,r0) correspond to the selected sequences S_{EtD}. The first operation is for detecting the a-cell accessed coupling faults, which are observed in our results. The last march element ⇳ (r0) is also for detecting the a-cell accessed coupling faults. With this algorithm, all EtD faults in the presence of predefined interconnect and connect defects in the STT-MRAM array can be detected effectively. Note that the test time for this march test algorithm can be assessed as 3Nw + 4Nr, where Nw and Nr respectively represent the consumed time for writing and reading the whole targeted memory array. As explained at the beginning of this chapter, all HtD faults in our work are either <0r0/0/?> or <1r1/1/?>, which are difficult to detect. Therefore, the work for this type of HtD faults can be done as the future work.

6.2. Test Solution Verification

After generating the test solution for all EtD faults, its effectiveness is expected to be verified. Therefore, we performed all the operations of the march test algorithm on bit cells of the test circuit in the addressing order. Firstly, we generate the desired stimulus and perform them in the defect-free test circuit, in order to guarantee the correctness of operations. After successfully being checked, the sequences of the proposed march test algorithm will be applied on the cells in the memory array in the similar process shown in Figure 4.10. By extracting the output of the read operations, we are able to judge whether any faults are sensitized at each defect strength. There are four read operations in the proposed March-EtD. As long as the output for one of them is not consistent with the expected value, faults will be recorded at current defect strength. Note that the procedure of test solution verification is also integrated into our Python-based simulation platform. When we compare the test verification results with fault space validation results, we find that most of them are identical. Here we take SS2 defect and OS_w defect as examples to illustrate the results of test solution verification.

Table 6.3: Comparison between the results of test verification and fault validation for SS2 defect

Defect	Type of results	1	50.1	100	251.1	501.2	1k	2k	10k	100k	1M	10M	100M
SS2	Fault space validation												
	Test solution verification												

Table 6.3 and 6.4 show the comparison between the results of fault validation and test verification respectively for SS2 and OS_w defect. Green color represents the covered defect strength ranges in faults space validation, while blue is for test solution verification. Grey means defect strength is fault-free. The fault validation results of these two defects are extracted from the fault maps depicted in Table 5.3 and 5.4. The covered defect strength

Table 6.4: Comparison between the results of test verification and fault validation for OS_w defect

Defect	Type of results	1	50.1	100	251.1	501.2	631	1k	1.6k	2.5k	10k	100k	1M	10M	100M
OSw	Fault space validation														
	Test solution verfication														

ranges are $[1\Omega, 2k\Omega)$ and $[501.2\Omega, 100M\Omega)$ respectively for SS2 and OS_w defect. It is obvious that the same results are obtained with the proposed march test algorithm. Therefore, the correctness of March-EtD is successfully verified.

6.3. Comparison between Test Solutions

In this section, we will simply compare our proposed march test algorithm with some existing march test algorithms.

Firstly, we take our proposed test solution and March C- [103] that is made for mainstream memory technologies to make a simple comparison. March C- is expressed as follows:

$$\Updownarrow (w0); \Uparrow (r0,w1); \Uparrow (r1,w0);$$
$$\Downarrow (r0,w1); \Downarrow (r1,w0); \Uparrow (r0)$$

This march test test consists of 5 write operations and 5 read operations, the cost time of which can be evaluated as 5Nw + 5Nr. This algorithm is able to detect stuck-at fault (SAF) and transition fault (TF). If March test is used for detecting the realistic fault models in our work, write disturb coupling fault (CFwd) and passive neighborhood pattern sensitive fault (PNPSF) wiil be missed. Whats' more, March-EtD in this thesis takes only 3NW + 4Nr. Therefore, our proposed march test algorithm appears more effective and more efficiently for detecting the defects in STT-MRAMs than March C-. Next, we will take the algorithm in [87] that is also targeted for STT-MRAMs to compare with our proposed algorithm.

In [87], the developed march test algorithm is 26N, which consists of 9 write operations and 16 read operations. It is expressed as follows:

$$\Updownarrow (w00); \Uparrow (r00,w11,r11); \Downarrow (r11,w00,r00);$$
$$\Downarrow (r00,w11,r11); \Downarrow (r11,w00); \Updownarrow (r00);$$
$$\Uparrow (r00,w01,r01); \Uparrow (r01,w10,r10); \Downarrow (r01,w10,r10);$$
$$\Downarrow (r10,w11,r11); \Updownarrow (r11)$$

The time cost will be evaluated as 9Nw + 16Nr. This algorithm is updated from March C- to detect transition fault (TF), in order to cover write disturb coupling fault (CFwd), which involves two cells. This algorithm is a 2-bit word oriented march (WOM) test [88]. Compared with this algorithm, the proposed test solution in our work only takes 3Nw + 4Nr, which saves much test time. Another point is that the 26N algorithm is not able to cover all

the faults detected by our solution. The most significant reason why this gap occurs is that inter-cell magnetic coupling is not considered in [87]. In this case, the observed specific STT-MRAM faults such as <1;1;1;1;1;1;1;1;0w1/0/-> are not validated in [87]. Due to the the demand for memory array with high density, the influence of $\mathbf{H}_{s\_inter}$ become increasingly evident. Therefore, our proposed march test algorithm is able to detect more realistic faults in STT-MRAMs and has higher fault coverage than that 26N algorithm. Secondly, short defects and open defects are not investigated in [87], which possibly leads to missing some faults. For example, <1;1;1;1;1;1;1;1;0w1/0/-> are exactly sensitized in the presence of a open defect.

Note that since we do not consider the dynamic faults in our work, some improvement is still needed for our test solution. As introduced in section 2.5.3, test sequences are developed for dynamic incorrect read faults (dIRF-n) as follows:

$$\begin{aligned}
&\Uparrow (w0);\\
&\Uparrow (r0,w1,r1,r1,r1,r1,r1,r1,r1,r1);\\
&\Downarrow (r1,w0,r0,r0,r0,r0,r0,r0,r0,r0);\\
&\Downarrow (r0)
\end{aligned}$$

Since only static faults are focused in our work, our proposed algorithm is not able to detect dynamic faults like dIRF-n. We can take this to improve the algorithm in the future work, in order to cover dynamic faults as well.

7

Conclusion & Future Work

This chapter firstly restates the purpose of the work in this thesis. Then conclusions are drawn for each steps in testing of interconnect and contact defects in STT-MRAMs. Finally, some possible future work will be revealed, in order to promote the STT-MRAM testing further.

7.1. Conclusion

As one of the most promising emerging memory technologies, STT-MRAM has enormous potential to replace DRAM. even SRAM of L3 cache in the memory hierarchy due to some advantages including low power consumption, high access time and non-volatility. It is of much significance to guarantee the high quality of STT-MRAM products, when the mass production starts. Therefore, in order to sweep out the defective STT-MRAM chips, effective test solutions are expected, which are able to detect the defects in STT-MRAMs as much as possible. In this thesis, the targeted defects are interconnect and contact defects in STT-MRAMs. The classical memory testing approach is utilized to generate the effective test solution to avoid test escapes during manufacturing. It consists of three steps: defect modelling, fault modelling and test development, which are discussed in different chapters respectively.

In chapter 3, all possible interconnect and contact defects are defined as three categories: shorts, opens and bridges, all of which are modeled as linear resistors.

In chapter 4 and 5, the complete fault space is firstly defined. Then, the circuit simulations are controlled by our Python-based simulation platform to validate the defined fault space in the presence of predefined defects. Note that inter-cell magnetic coupling is considered in our work. Based on the comparison between results under various setups including no $\mathbf{H}_{\text{s\_inter}}$, $\uparrow \mathbf{H}_{\text{s\_inter}}$ and $\downarrow \mathbf{H}_{\text{s\_inter}}$. we found that 0w1 operations are discouraged by $\uparrow \mathbf{H}_{\text{s\_inter}}$, while $\downarrow \mathbf{H}_{\text{s\_inter}}$ contributes to more 1w0 sensitized faults. The smaller the spacing between cells is, the evident the influence of $\mathbf{H}_{\text{s\_inter}}$ will be. Under $\uparrow$, the extended defect strength ranges are observed for SS2 and SB1, while $\downarrow$ causes extended defect strength ranges in the presence of OS_w and SC2. In these ranges, passive neighborhood pattern sensitive fault (PNPSF) is validated, FPs of which are <0;0;0;0;0;0;0;0;1w0/1/-> and <1;1;1;1;1;1;1;1;0w1/0/->. Compared with the existing fault models caused by interconnect

and contact defects, this type of fault are newly observed.

In chapter 6, DBs-based ILP method and sequence-based ILP method are utilized to develop the effective test solution for all validated EtD faults. The optimized data background is 00000000(↓), under which the optimized sequences are $S_{EtD} = \{1w0(\downarrow), 0r0(\downarrow), 1r1(\downarrow)\}$. The generated march test algorithm is March-EtD = $\{\Updownarrow (w0); \Updownarrow (r0, w1, r1, w0, r0); \Updownarrow (r0)\}$. The test time is evaluated as 3Nw + 4Nr, where Nw and Nr respectively represent the consumed time for writing and reading the whole targeted memory array. With the proposed algorithm, all EtD faults caused by predefined defects in STT-MRAMs can be detected. As a result of this, defective STT-MRAM chips will be effectively swept out and test escapes can be avoided.

7.2. Future Work

In this thesis, specific STT-MRAM fault model (PNPSF) is observed and an effective march test algorithm is generated to cover all EtD faults. However, there are still some points needed for further investigation. Firstly, more simulations need to be done to classify the faults in region B and C of Figure 5.1, since only two worst cases are considered in our work. In this way, more fault models are possibly discovered. Secondly, the generated march test algorithm can be only applied to sensitizing all EtD faults. Special DfT techniques should be designed to cover all HtD faults to improve the fault coverage further. Lastly, dynamic faults are expected to be focused as well. Dynamic faults are sensitized by multiple operations, which possibly extend the covered defects strength ranges. Therefore, if we generate test solutions that are able to detect both static and dynamic faults, it is more effectively to recognize the defects in STT-MRAMs.

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A

Fault Maps for All Defects

In this appendix, the fault maps for all considered defects are given. Table A.1–A.9 illustrate the fault maps for considered open defects in section 3.2. Table A.10–A.17 show the fault maps for all short defects discussed in section 3.3. Finally. Table A.18–A.40 give the fault maps for all bridge defects defined in section 3.4. In the fault maps, the following colour encoding is used:

- Gray : no sensitized faults
- Green : sensitized EtD faults
- Yellow : sensitized HtD faults

Note that we only list sequences that successfully sensitize faults in the fault maps.

A.1. Results for Open Defects

In this thesis, we considered 9 open defects: OC1, OC2, OC3, OC4, OS_w, OS_r, OB_w, OB_r, OW defect as illustrated in Figure 3.3, which correspond to Table A.1–A.9.

Table A.1: Fault map for OC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	631	1.6k	2.5k	10k	100k	1M	10M	100M
OC1	no	0w1													
		1w0													
		0r0													
	↑	0w1													
		1w0													
		0r0													
	↓	0w1													
		1w0													
		0r0													

Table A.2: Fault map for OC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	631	1.6k	2.5k	10k	100k	1M	10M	100M
OC1	no	0w1													
		1w0													
		0r0													
	↑	0w1													
		1w0													
		0r0													
	↓	0w1													
		1w0													
		0r0													

Table A.3: Fault map for OC3 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	316.2	501.2	631	1.6k	2.5k	10k	100k	1M	10M	100M
OC3	no	0w1													
		1w0													
		0r0													
	↑	0w1													
		1w0													
		0r0													
	↓	0w1													
		1w0													
		0r0													

Table A.4: Fault map for OC4 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	316.2	1k	3.2k	10k	100k	1M	10M	50.1M	79.4M	100M
OC4	no	0w1												
		1w0												
		0r0												
	↑	0w1												
		1w0												
		0r0												
	↓	0w1												
		1w0												
		0r0												

Table A.5: Fault map for OS_w defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	631	1k	1.6k	2.5k	10k	100k	1M	10M	100M
OS_w	no	0w1														
		1w0														
	↑	0w1														
		1w0														
	↓	0w1														
		1w0														

A.2. Results for Short Defects

In this thesis, we considered 8 open defects: SC1, SC2, SS1, SS2, SB1, SB2, SW1, SW2 defect as illustrated in Figure 3.3, which correspond to Table A.10–A.17.

Table A.6: Fault map for OS_r defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	1k	10k	100k	1M	10M	100M
0Sr	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.7: Fault map for OB_w defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	251.2	631	1k	2.5k	3.2k	10k	100k	1M	10M	100M
OBw	no	0w1												
		1w0												
	↑	0w1												
		1w0												
	↓	0w1												
		1w0												

Table A.8: Fault map for OB_r defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	631	794.3	1k	10k	100k	1M	10M	100M
0Sr	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.9: Fault map for OW defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	1k	2.5k	3.2k	10k	100k	1M	31.6M	39.8M	100M
OW	no	0w1											
		1w0											
		0r0											
	↑	0w1											
		1w0											
		0r0											
	↓	0w1											
		1w0											
		0r0											

Table A.10: Fault map for SC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	1k	2.5K	6.3k	10k	100k	1M	15.8M	100M
SC1	no	1w0											
		0r0											
		1w1											
	↑	1w0											
		0r0											
	↓	1w0											
		0r0											
		1w1											

Table A.11: Fault map for SC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	631	1.3k	2K	2.5k	10k	100k	3.2M	15.8M	100M
SC2	no	1w0												
		0w1												
		1r1												
		0w0												
	yes up	1w0												
		0w1												
		1r1												
		0w0												
	yes down	1w0												
		0w1												
		1r1												

Table A.12: Fault map for SS1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	7.9k	50.1k	100k	1M	10M	100M
SS1	no	1w0											
		0r0											
	↑	1w0											
		0r0											
	↓	1w0											
		0r0											

Table A.13: Fault map for SS2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	251.1	501.2	794.3	1k	1.6k	2k	10k	100k	1M	10M	100M
SS2	no	0w1														
		1r1														
	↑	0w1														
		1r1														
	↓	0w1														
		1r1														

Table A.14: Fault map for SB1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	2.5k	7.9k	50.1k	100k	1M	20M	100M
SB1	no	0w1											
		0r0											
	↑	0w1											
		0r0											
	↓	0w1											
		0r0											

Table A.15: Fault map for SB2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	501.2	3.2k	4k	10k	50.1k	100k	3.2M	20M	100M
SB2	no	1w0											
		1r1											
	↑	1w0											
		1r1											
	↓	1w0											
		1r1											

Table A.16: Fault map for SW1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	501.2	1.6k	4k	10k	39.8k	100k	1M	10M	100M
SW1	no	1r1											
		1w1											
		0w1											
	↑	1r1											
	↑	1r1											
		1w1											
		0w1											

Table A.17: Fault map for SW2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	501.2	1.6k	4k	7.9k	15.9k	100k	1M	10M	100M
SW2	no	0w1											
		1w0											
		0r0											
	↑	0w1											
		1w0											
		0r0											
	↓	0w1											
		1w0											
		0r0											

A.3. Results for Bridge Defects

In this thesis, we defined 6 bridges within a cell and 17 bridges between cells, results of which correspond to Table A.18– A.40.

Table A.18: Fault map for BC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	501.2	1.3k	6.3k	10k	15.9k	100k	3.2M	10M	100M
BC1	no	0w1											
		1w0											
		1r1											
	↑	0w1											
		1w0											
		1r1											
	↓	0w1											
		1w0											
		1r1											

Table A.19: Fault map for BC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	125.9	631	1.6k	7.9k	10k	12.5k	20k	100k	3.2M	10M	100M
BC2	no	0w1													
		1w0													
		0r0													
		1r1													
	↑	0w1													
		1w0													
		0r0													
		1r1													
	↓	0w1													
		1w0													
		0r0													
		1r1													

Table A.20: Fault map for BC3 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	251.2	631	1.6k	7.9k	10k	100k	1M	10M	100M
BC3	no	0w1											
		1w0											
		1r1											
	↑	0w1											
		1w0											
		1r1											
	↓	0w1											
		1w0											
		1r1											

Table A.21: Fault map for BC4 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	1k	2.5K	6.3k	10k	39.8k	1M	10M	100M
BC4	no	0w1											
		1w0											
		0r0											
	↑	0w1											
		1w0											
		0r0											
	↓	0w1											
		1w0											
		0r0											

Table A.22: Fault map for BC5 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	251.2	631	1.3k	7.9k	10k	100k	2.5M	10M	100M
BC5	no	1w1											
		0w1											
		1r1											
	↑	1r1											
	↓	1w1											
		0w1											
		1r1											

Table A.23: Fault map for BC6 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	251.1	794.3	1k	2k	3.2k	10k	100k	251.2k	1M	10M	100M
BC6	no	1w0													
		0r0													
		1r1													
	↑	1w0													
		0r0													
		1r1													
	↓	1w0													
		0r0													
		1r1													

Table A.24: Fault map for dBCC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	1k	7.9k	10k	100k	1M	10M	100M
dBCC1	no	0r0										
	↑	0r0										
	↓	0r0										

Table A.25: Fault map for dBCC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	1k	1.6k	2k	10k	100k	1M	10M	100M
dBCC2	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.26: Fault map for dBCC3 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	251.2	501.2	1k	7.9k	10k	100k	1M	10M	100M
dBCC3	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.27: Fault map for dBCC4 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	251.2	501.2	1k	7.9k	12.6k	100k	1M	10M	100M
dBCC4	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.28: Fault map for dBCC5 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	794.3	1k	10k	100k	1M	10M	100M
dBCC5	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.29: Fault map for dBCC6 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	251.2	501.2	1k	7.9k	10k	100k	1M	10M	100M
dBCC6	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.30: Fault map for dBCC7 defect

Defect	Inter-cell magnetic coupling	Sequence	1	100	501.2	1k	1.6K	5k	10k	15.8k	1M	10M	100M
dBCC7	no	0w1											
		1w0											
		0r0											
	↑	0w1											
		1w0											
		0r0											
	↓	0w1											
		1w0											
		0r0											

Table A.31: Fault map for dBCC8 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	631	2.5k	6.3k	12.6k	20k	100k	2.5M	10M	100M
dBCC8	no	0w1											
		0r0											
		1r1											
		1w1											
	↑	0w1											
		0r0											
		1r1											
	↓	0w1											
		0r0											
		1r1											
		1w1											

Table A.32: Fault map for dBCC9 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	6.3k	7.9k	100k	1M	10M	100M
dBCC9	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.33: Fault map for dBCC10 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	6.3k	10k	100k	1M	10M	100M
dBCC10	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.34: Fault map for dBCC11 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	631	3.2k	6.3k	10k	20k	100k	3.2M	10M	100M
dBCC11	no	0w1											
		1r1											
		0r0											
		1w1											
	↑	0w1											
		1r1											
		0r0											
	↓	0w1											
		1r1											
		0r0											
		1w1											

Table A.35: Fault map for dBCC12 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	6.3k	10k	100k	1M	10M	100M
dBCC12	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.36: Fault map for cBCC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	631	3.2k	6.3k	10k	20k	100k	3.2M	10M	100M
cBCC1	no	0w1											
		1r1											
		0r0											
		1w1											
	↑	0w1											
		1r1											
		0r0											
	↓	0w1											
		1r1											
		0r0											
		1w1											

Table A.37: Fault map for cBCC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	251.2	794.3	1k	6.3k	10k	100k	1M	10M	100M
cBCC2	no	1w0											
		1r1											
		1w1											
		0w1											
	↑	1w0											
		1r1											
	↓	1w0											
		1r1											
		1w1											
		0w1											

Table A.38: Fault map for rBCC1 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	7..9k	10k	100k	1M	10M	100M
rBCC1	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.39: Fault map for rBCC2 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	7.9k	10k	100k	1M	10M	100M
rBCC2	no	0r0											
	↑	0r0											
	↓	0r0											

Table A.40: Fault map for rBCC3 defect

Defect	Inter-cell magnetic coupling	Sequence	1	50.1	100	501.2	1k	6.3k	10k	100k	1M	10M	100M
rBCC3	no	0r0											
	↑	0r0											
	↓	0r0											