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Thermal-mechanical-electrical Co-design of Fan-Out Panel-Level SiC MOSFET Packaging with a Multi-objective Optimization Algorithm

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Abstract— **As the next generation of semiconductor devices, SiC MOSFETs have demonstrated significant performance improvements in switching loss, switching frequency, and high-temperature operation compared to Si-based MOSFETs. However, the long-term reliability of such devices and their packaging continues to be a major concern. Towards addressing this challenge, this study proposes a multi-objective optimization design method for parasitic inductance (*L*), thermal strain (*ε*), and thermal resistance (*R*) of SiC MOSFETs with Fan-Out Panel-Level Packaging (FOPLP). First, the orthogonal experimental design was employed to investigate the thickness effects of baseplate, solder, die and redistribution layer (RDL) on *L*, *ε,* and *R*. Then, the multi-objective optimization was developed to simultaneously reduce *L*, *ε,* and *R*. Finally, the fatigue lifetimes of the optimized and initial SiC MOSFET FOPLP structures were compared to verify the optimization's accuracy. Study findings include: (1) Solder thickness was the most significant influence factor for *L*, *ε* and *R* of SiC MOSFET FOPLP, *L* and *R* increased, and *ε* decreased with increasing solder thickness; (2) The proposed multi-objective optimization method coupled with a genetic algorithm achieved 14.79, 8.96, and 9.28% reduction of *L, ε,* and *R,* respectively; (3) The fatigue lifetime of solder (SAC305) was evaluated using the Coffin-Manson model, with predicted lifetimes before and after optimization being 6786 and 7085 cycles, respectively, demonstrating that the proposed approach significantly enhanced the designed SiC MOSFET FOPLP's long-term thermal cycling reliability.**

Keywords- SiC MOSFET; FOPLP; Genetic algorithms; Orthogonal experimental design; Reliability optimization

I. INTRODUCTION

Silicon carbide (SiC) exhibits excellent properties, such as high critical breakdown field strength, high thermal conductivity, and high electron saturation velocity compared to Si material [1, 2]. Thus, SiC MOSFET has comparative advantages over Si-MOSFET in terms of switching speed, junction temperature operation, and energy loss enabling a significant improvement in energy density and reduced weight and the volumetric ratio [3-6].

As such, the market of SiC power devices is fast growing. According to the Yole Group [7], the global market for SiC power devices was valued at $1.09 billion in 2021. It is expected to grow beyond $6 billion by 2027 at a compound annual growth rate of 34%. The application of SiC MOSFETs has spread throughout major industries such as automotive, locomotives, and energy. However, compared to Si-based power devices, their long-term reliability has not been well established, which limits their potential market growth and applications.

A key component of improving the reliability of devices is the development of better packaging technology. In our previous work [8, 9], we proposed Fan-Out Panel-Level packaging (FOPLP) uses the redistribution layer (RDL) to replace bonding wire, achieving low thermal strain, thermal resistance, and parasitic inductance. Most recent studies [10-12] focus on improving the packaging process of SiC MOSFET FOPLP to enhance thermal, mechanical, and electromagnetic parameters separately. . However, little attention has been paid to simultaneously improve these crucial factors. In this study, a multi-objective optimization design method for parasitic inductance (*L*), thermal strain (*ε*), and thermal resistance (*R*) of SiC MOSFET FOPLP were proposed, and thermal cycling fatigue lifetimes were used to evaluate and verify the method.

The remainder of the paper was organized as follows: Section II introduced the test samples, experiments designed, and simulations. Section III discusses orthogonal experimental results analysis, multi-objective optimization method, and fatigue lifetime prediction. Finally, section IV proposed the concluding remarks.

II. DESIGN OF EXPERIMENTS

This section described the structure of the SiC MOSFET FOPLP, followed by an experimental scheme designed using the orthogonal experiment method. Finally, the different FE simulations and material parameters were illustrated.

A. SiC MOSFET FOPLP

Fig. 1 displays the structure of SiC MOSFET FOPLP. The device is composed of the baseplate (lead frame), solder, SiC MOSFET die (1200V/136A/12mΩ, size of 5*5*0.15mm, from ROHM SEMICONDUCTOR), RDL, epoxy molding compound (EMC), and top heatsink pad. The material of the baseplate and RDL is copper. The wireless packaging device

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uses RDL to replace bonding wire. A double-sided cooling mechanism is achieved by releasing heat from the top heatsink pad and solder pad to the ambient temperature.

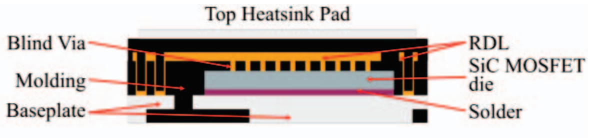

Fig. 1.The cross-section of SiC MOSFET FOPLP.

B. Orthogonal experimental design

The effect of the thickness of different layers in SiC MOSFET FOPLP on its performance was evaluated using an orthogonal experiment. The thicknesses of the baseplate (x_1), solder(x_2), die (x_3), and RDL (x_4) were selected in four types, resulting in 256 combinations. Orthogonal table L16 (4^4) was designed to reduce experiment quantity, and only 16 sets of experiments were necessary, as shown in TABLE 1.

TABLE 1. The orthogonal table L16 (4^4)

Scenario No.	x_1 (mm)	x_2 (mm)	x_3 (mm)	x_4 (mm)
1	0.25	0.05	0.1	0.2
2	0.25	0.1	0.15	0.3
3	0.25	0.15	0.2	0.4
4	0.25	0.2	0.25	0.5
5	0.3	0.05	0.15	0.4
6	0.3	0.1	0.1	0.5
7	0.3	0.15	0.25	0.2
8	0.3	0.2	0.2	0.3
9	0.35	0.05	0.2	0.5
10	0.35	0.1	0.25	0.4
11	0.35	0.15	0.1	0.3
12	0.35	0.2	0.15	0.2
13	0.4	0.05	0.25	0.3
14	0.4	0.1	0.2	0.2
15	0.4	0.15	0.15	0.5
16	0.4	0.2	0.1	0.4

TABLE 2. The material parameters used in thermal and mechanical simulations [8, 9, 13]

Component	Material	K (W/m·°C)	CTE (ppm/°C)	E (GPa)	v
RDL, Baseplate, Heatsink pad	copper	401	18	110	0.34
die	SiC	58.6	5.1	400	0.14
Solder	SAC305	70	31	49	0.38
Molding	EMC	1.5	9	15	0.38

TABLE 3. The material parameters used in electromagnetic simulation [13]

Component	Material	e	μ	σ (S/m)
RDL, baseplate, Heatsink Pad	copper	1	0.999991	5.8e7
die	SiC	9.7	1	0
Solder	SAC305	1	1	7e6
Molding	EMC	3.6	1	0

C. Simulations

Performances such as parasitic inductance (L), thermal strain (ε), and thermal resistance (R) significantly affect the operational capability and reliability of SiC MOSFET FOPOP. The parasitic inductance was extracted using the finite/boundary element (F/BE) method. The thermal strain and thermal resistance were simulated using finite element (FE) method. In the thermal resistance simulation, the thermal power generated in die was set as 58.5W with the on-state current/resistance was 70A/12mΩ. The material parameters used in thermal and mechanical simulations include thermal conductivity (k), coefficient of thermal expansion (CTE), Young's modulus (E), and Poisson's ratio (v), as listed in TABLE 2. The material parameters used in electromagnetic simulation include relative permittivity (e), relative permeability (μ), and conductivity (σ) as listed in TABLE 3.

III. RESULTS AND DISCUSSIONS

In this part, the effects of x_1, x_2, x_3, and x_4 on L, ε, and R were explored by analyzing the orthogonal experimental results. By resolving the extreme point of regression equation using a genetic algorithm, the multi-objective optimization method was developed to simultaneously reduce L, ε, and R. Last, the thermal cycling fatigue lifetimes of SiC MOSFET FOPLP before and after optimization was calculated with the Coffin-Manson model.

A. Orthogonal experimental results

Each scenario's L, ε, and R in orthogonal table L16 were simulated. The effect of x_1, x_2, x_3, and x_4 on L, ε, and R was analyzed using statistical software, and the results is shown in Fig. 2.

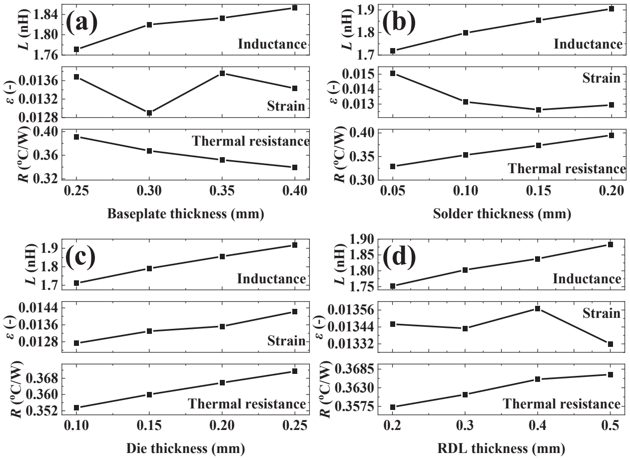

Fig. 2. The simulated parasitic inductance, thermal strain and thermal resistance results with the effect of (a) baseplate thicknesses, (b) solder thicknesses, (c) die thicknesses, and (d) RDL thicknesses.

Due to the extension of the conductive path, increases in baseplate thicknesses, solder thicknesses, die thicknesses or RDL thicknesses all cause an increase in parasitic inductance. With increasing solder thickness, thermal strain decreases. Thermal strain, however, was positively correlated with die thickness. Minimum thermal strain values appeared at baseplate thickness = 0.30 mm and RDL thickness = 0.50 mm. Increasing the solder thickness, die thickness or RDL thickness would prolong the heat dissipation path resulting in an increase in thermal resistance. Conversely, thermal resistance decreased with increasing baseplate thickness. The area of the die was larger than that of the drain solder pad. Therefore, the heat generated at the edge of the die needs to be transmitted laterally to the drain solder pad. Fig. 3 shows lateral heat conduction was limited in thin baseplates, while thicker baseplates would increase efficiency.

The influence degrees of x_1, x_2, x_3, and x_4 on L, ε, and R of SiC MOSFET FOPLP are illustrated in TABLE 4. Die thickness, solder thickness, and solder thickness significantly affected the parasitic inductance, thermal strain, and thermal resistance performances, respectively. The integrated influence degrees are listed in the order: solder thickness, die thickness, baseplate thickness, and RDL thickness.

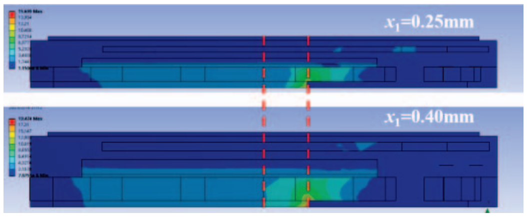

Fig. 3. Comparison of lateral heat conduction effect at baseplates with different thicknesses.

TABLE 4. The influence degree of baseplate thickness, solder thickness, die thickness, and RDL thickness for the performance of SiC MOSFET FOPLP

degree of influence	x_1	x_2	x_3	x_4
L	4	2	1	3
ε	2	1	3	4
R	2	1	4	3
Integrated	3	1	2	4

B. Multi-objective optimization

All three parameters (L, ε, and R) significantly affect the SiC MOSFET FOPLP. Therefore, we proposed a multi-objective optimization method to improve the three performances simultaneously using regression curves and genetic algorithms.

In this study, we assumed that L, ε, and R have the same degree of importance, though a significant difference existed in L, ε and R values, as shown in Fig. 2. Therefore, L, ε and R values needed to be normalized. Each of the normalized L, ε, and R were modeled as a function of x_1, x_2, x_3 and x_4. According to Equation (1), a quaternion quadratic polynomial function was proposed as a regression curve to relate the three performances with four factors.

Quaternion quadratic polynomial function:

$$\begin{aligned} z(x_1,x_2,x_3,x_4) &= a_1x_1+a_2x_2+a_3x_3+a_4x_4+a_5x_1x_2 \\ &+a_6x_1x_3+a_7x_1x_4+a_8x_2x_3+a_9x_2x_4+a_{10}x_3x_4+a_{11}x_1^2 \\ &+a_{12}x_2^2+a_{13}x_3^2+a_{14}x_4^2 \end{aligned} \tag{1}$$

Where z denotes each normalized L, ε or R, and a_1 to a_{14} are the fitting parameters relevant to the normalized performance. The fitting parameters value (a_1 to a_{14}) of each normalized performance was obtained after fitting. The fitted results of normalized L, ε, and R are listed in TABLE 5. It can be noted that high R^2 values over 0.99 were achieved for each normalized performance fitting.

Fig. 4 compares the actual and predicted normalized values for L, ε, and R. The predicted values agreed well with the actual value from orthogonal experimental results. Therefore, the proposed quaternion quadratic polynomial function is suitable for describing dynamically how normalized performance changes with the factors.

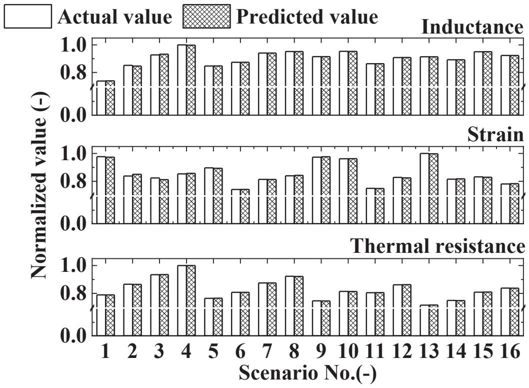

Fig. 4. Comparison between the actual and predicted normalized values.

The sum of three regression functions [$L(x_1, x_2, x_3, x_4)$, $\varepsilon(x_1, x_2, x_3, x_4)$, $R(x_1, x_2, x_3, x_4)$] was set as the integrated regression function $I(x_1, x_2, x_3, x_4)$ that considers the L, ε and R simultaneously. The following Equation calculates the integrated regression function:

$$\begin{aligned} &I(x_1, x_2, x_3, x_4)= \\ &L(x_1, x_2, x_3, x_4)+\varepsilon(x_1, x_2, x_3, x_4)+R(x_1, x_2, x_3, x_4) \end{aligned} \tag{2}$$

The parameters of $I(x_1, x_2, x_3, x_4)$ are listed in TABLE 5. The multi-objective optimization for L, ε, and R was realized by calculating the extreme point of the curve. The multi-objective optimization mathematical model is expressed as follows:

$$\begin{cases} 0.25 \le x_1 \le 0.40 \\ 0.05 \le x_2 \le 0.20 \\ 0.10 \le x_3 \le 0.25 \\ 0.20 \le x_4 \le 0.5 \\ Minimum\ \ I(x_1, x_2, x_3, x_4) \end{cases} \tag{3}$$

The genetic algorithm was used to solve Equation (3). The parameters of the genetic algorithm were set as follows: code base = 10, decimal places = 4, population size = 100, aberration rate = 0.01, uniform crossover with crossover rate = 0.85, and adopting absolute top mate selection. The optimal solution calculated by genetic algorithm was achieved when x_1, x_2, x_3, and x_4 were 0.4, 0.17, 0.1, and 0.2mm, respectively.

TABLE 6 compares the performances of SiC MOSFET FOPLP before and after multi-objective optimization. The results reveal that the optimized structure parameters are obtained when L, ε, and R are optimal. After optimization, the L, ε, and R were decreased by 14.79, 8.96, and 9.28%, respectively. Fig. 5 illustrates the simulated mechanical and thermal performances of the SiC MOSFET FOPLP. The maximum strain and maximum temperature points were located at the corner of the solder layer and the die, respectively, and the distribution trends of strain and temperature did not change due to optimization.

TABLE 5. The fitting results of normalized performances with the quaternion quadratic polynomial function

parameters	L	ε	R	Integrated
a_1	3.262	10.720	5.222	19.204
a_2	1.068	-5.275	0.377	-3.83
a_3	2.643	3.778	4.020	10.441
a_4	-0.250	4.648	-1.544	2.854
a_5	-0.434	6.203	1.533	7.302
a_6	-0.110	9.494	0.909	10.293
a_7	-0.015	2.674	-0.188	2.471
a_8	-5.002	-23.923	-11.879	-40.804
a_9	1.938	12.064	6.545	20.547
a_{10}	-0.899	3.060	-0.363	1.798
a_{11}	-4.843	-22.757	-10.325	-37.925
a_{12}	-0.501	11.276	-0.186	10.589
a_{13}	-2.886	-11.306	-6.771	-20.963
a_{14}	0.542	2.636	1.348	4.526
R^2	0.999	0.995	0.999	/

TABLE 6. Comparison of the performances before and after optimization

Condition	Structure parameters	L	ε	R
Before Optimization	x_1: 0.35mm, x_2: 0.15mm x_3: 0.25mm, x_4: 0.45mm	1.995	0.015	0.381
After Optimization	x_1: 0.40mm, x_2: 0.17mm x_3: 0.10mm, x_4: 0.20mm	1.700	0.014	0.345
Decrease percentage (%)		14.79	8.96	9.28

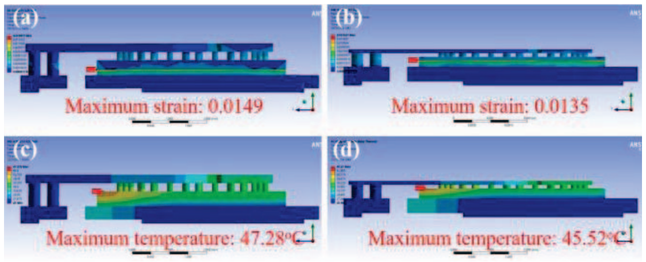

Fig. 5. The simulated mechanical and thermal performances of SiC MOSFET FOPLP: (a) strain distribution before optimization; (b) strain distribution after optimization; (c) temperature distribution before optimization; (d) temperature distribution after optimization.

C. *Fatigue lifetime enhancement*

Anand constitutive model explains visco-plastic materials' stress - strain relationship in high-temperature environments. The Coffin-Mason model is mainly used to predict the fatigue lifetime of visco-plastic material under thermal cycling conditions. FE simulation can be used to calculate parameters of the Coffin-Mason model, such as plastic strain amplitude. In this part, the fatigue lifetimes of SiC FOPLP before and after optimization were calculated and compared, which validated the effectiveness of the multi-objective optimization method.

The thermal cycling test for SiC MOSFET FOPLP was simulated using FE simulation software. According to JEDEC JESD22-A106B, the thermal cycling temperature range was set to -38 to 152 ºC. Fig. 6 illustrates the temperature profile. The solder (SAC305) in SiC MOSFET FOPLP is a visco-plastic material; Anand constitutive model was used in the simulation to describe the visco-plastic performance of SAC305. The Anand model parameters of SAC305 are listed in TABLE 7.

Fig. 6 illustrates the changes in the plastic strain of SAC305 in SiC MOSFET FOPLP during the thermal cycle. The maximum plastic strain and the amplitude of plastic strain have significantly decreased by an average of 6.74 and 4.10% respectively after optimization.

TABLE 7. The Anand model parameters of SAC305[14]

Anand constant	Units	Value	Description
S_0	MPa	45.9	Initial value of deformation resistance
Q/R	1/K	7460	Q=Activation energy R=Universal gas constant
A	S^{-1}	5.87E6	Pre-exponential factor
ξ	-	2	Stress multiplier
m	-	0.0942	Strain rate sensitivity of stress
h_0	MPa	9350	Hardening/softening constant
$\hat{s}$	MPa	58.3	Coefficient for deformation resistance saturation value
n	-	0.015	Strain rate sensitivity of saturation (deformation resistance) value
a	-	1.5	Strain rate sensitivity of hardening/softening

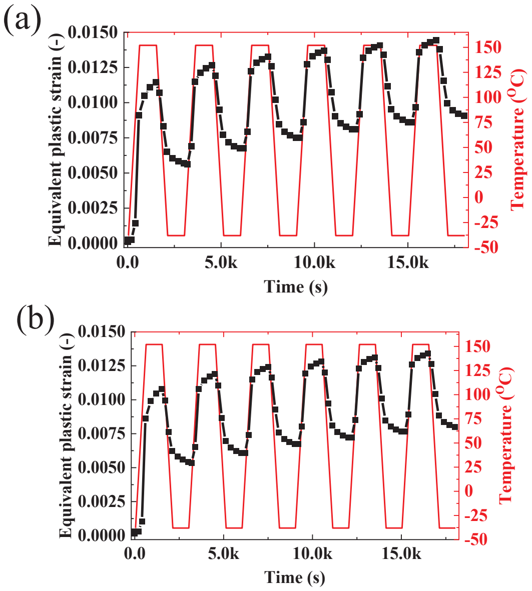

Fig. 6. The changes of plastic strain of SAC305 in SiC MOSFET FOPLP with the thermal cycle: (a) before optimization; (b) after optimization

Coffin-Manson equation [15] is expressed as follows:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon'_f}\right)^{\frac{1}{c}} \tag{4}$$

where N_f is the failure lifetime; ε'_f, c, and $\Delta\gamma$ are the fatigue ductility coefficient, fatigue ductility index, and shear strain amplitude, respectively.

c and $\Delta\gamma$ can be calculated by follow equations:

$$\Delta\gamma = \sqrt{3}\Delta\varepsilon \qquad (5)$$

$$c = -0.442 - 0.0006T_s + 0.017\,ln(1+f) \qquad (6)$$

$\Delta\varepsilon$ is the plastic strain amplitude, T_S and f are the average temperature and cycles for thermal cycling per day. Refer to [16], ε'_f of SAC305 was set as 0.24. TABLE 8 presents the fatigue lifetime predictions for SAC305 in SiC MOSFET FOPLP. The fatigue lifetime of SAC305 before and after optimization was 6786 and 7085 cycles, respectively, demonstrating that the proposed method can result in a 4.2% improvement.

TABLE 8. The predicted fatigue lifetime based on Coffin-Manson model

Condition	c	ε'_f	$\Delta\varepsilon$	N_f
Before Optimization	-0.407	0.24	0.005700	6786
After Optimization	-0.407	0.24	0.005601	7085

IV. CONCLUDING REMARKS

The study investigates the effect of the thicknesses of baseplate, solder, die, and RDL on the parasitic inductance, thermal strain, and thermal resistance of SiC MOSFET FOPLP. A genetic algorithm-based multi-objective optimization method was proposed to lower parasitic inductance, thermal strain, and thermal resistance. Furthermore, the thermal cycling reliability of the designed packaging was improved. The following conclusions can be drawn from the study: (1) The most significant influence factor is solder thickness according to its degree of integrated influence for L, ε and R; (2) The optimal L, ε, and R performance of SiC MOSFET FOPLP were obtained when the x_1, x_2, x_3, x_4 were 0.4, 0.17, 0.1 and 0.2mm, respectively; (3) After optimization, the L, ε, and R decreased by 14.79, 8.96 and 9.28% respectively, and the fatigue lifetime (N_f) improved 4.2%. Therefore, the proposed multi-objective optimization method is valuable in designing and fabricating the SiC MOSFET FOPLP, which will improve the package's initial performance and long-term reliability.

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REFERENCES

[1] L. Yang *et al.*, "Gate Oxide Instability of 4H-SiC p-Channel MOSFET Induced by AC Stress at 200 °C," *IEEE Transactions on Electron Devices,* vol. 70, no. 1, pp. 379-382, 2023. doi: 10.1109/TED.2022.3224638.

[2] S. Liang *et al.*, "Modeling Irradiation-Induced Degradation for 4H-SiC Power MOSFETs," *IEEE Transactions on Electron Devices,* pp. 1-5, 2023. doi: 10.1109/TED.2023.3234039.

[3] L. F. S. Alves, P. Lefranc, P. O. Jeannin, and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, 2018, pp. 824-829. doi: 10.1109/ICIT.2018.8352284

[4] T. Kimoto *et al.*, "Progress and future challenges of SiC power devices and process technology," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 9.5.1-9.5.4. doi: 10.1109/IEDM.2017.8268360

[5] X. Wang, H. Wen, and Y. Zhu, "Review of SiC Power Devices for Electrical Power Systems: Characteristics, Protection, and Application," in *2021 6th Asia Conference on Power and Electrical Engineering (ACPEE)*, 2021, pp. 1-5. doi: 10.1109/ACPEE51499.2021.9437108

[6] X. She, A. Q. Huang, L. Ó, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 10, pp. 8193-8205, 2017. doi: 10.1109/TIE.2017.2652401.

[7] *https://www.yolegroup.com/product/report/power-sic-2022/?cn-reloaded=1*.

[8] J. Fan *et al.*, "Genetic Algorithm-Assisted Design of Redistribution Layer Vias for a Fan-Out Panel-Level SiC MOSFET Power Module Packaging," in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, 2022, pp. 260-265. doi: 10.1109/ECTC51906.2022.00049

[9] Y. Qian, F. Hou, J. Fan, Q. Lv, X. Fan, and G. Zhang, "Design of a Fan-Out Panel-Level SiC MOSFET Power Module Using Ant Colony Optimization-Back Propagation Neural Network," *IEEE Transactions on Electron Devices,* vol. 68, no. 7, pp. 3460-3467, 2021. doi: 10.1109/TED.2021.3077209.

[10] J. Li, D. Shao, and K. Ding, "Optimizing RDS(on) of Dual-Chip Power MOSFET by Fan-out Panel Level Packaging (FOPLP)," in *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*, 2022, pp. 1-3. doi: 10.1109/ICEPT56209.2022.9872647

[11] J. Jiang *et al.*, "Research On FOPLP Package of multi-chip Power Module," in *2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC)*, 2020, pp. 1-6. doi: 10.1109/ESTC48849.2020.9229816

[12] J. Jiang *et al.*, "Research on Diode Product Reliability of FOPLP Based on PCB Process," in *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*, 2022, pp. 1-5. doi: 10.1109/ICEPT56209.2022.9873112

[13] F. Hou *et al.*, "Fan-Out Panel-Level PCB-Embedded SiC Power MOSFETs Packaging," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 1, pp. 367-380, 2020. doi: 10.1109/JESTPE.2019.2952238.

[14] J. Ting-biao, D. Chao, and X. Long-hui, "Finite Element Analysis and Fatigue Life Prediction of BGA Mixed Solder Joints," in *2007 International Symposium on High Density packaging and Microsystem Integration*, 2007, pp. 1-6. doi: 10.1109/HDP.2007.4283611

[15] L. Jiang, W. Zhu, and H. He, "Comparison of Darveaux model and Coffin-Manson model for fatigue life prediction of BGA solder joints," in *2017 18th International Conference on Electronic Packaging Technology (ICEPT)*, 2017, pp. 1474-1477. doi: 10.1109/ICEPT.2017.8046714

[16] P. Chauhan, M. Osterman, S. W. R. Lee, and M. Pecht, "Critical Review of the Engelmaier Model for Solder Joint Creep Fatigue Reliability," *IEEE Transactions on Components and Packaging Technologies,* vol. 32, no. 3, pp. 693-700, 2009. doi: 10.1109/TCAPT.2009.2030983.