Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application

Martin, Henry; Reintjes, Marcia; Reijs, Dave; Dorrestein, Sander; Kengen, Martien; Libon, Sebastien; Smits, Edsger; Tang, Xiao; Koelink, Marco; Poelma, Rene

DOI
10.1109/ECTC51909.2023.00029

Publication date
2023

Document Version
Final published version

Published in
Proceedings - IEEE 73rd Electronic Components and Technology Conference, ECTC 2023

Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application

Henry Martin[1,2]
h.a.martin@tudelft.nl
henry.martin@citc.org

Marcia Reintjes[3]
marcia.reintjes@mintres.com

Dave Reijs[2]
dave.Reijs@citc.org

Sander Dorrestein[2]
sander.dorrestein@citc.org

Martien Kengen[2]
martien.kengen@citc.org

Sebastien Libon[2]
sebastien.libon@citc.org

Edsger Smits[2]
edsger.smits@citc.org

Xiao Tang[3]
xiao.tang@mintres.com

Marco Koelink[2]
marco.koelink@citc.org

Rene Poelma[1]
R.H.Poelma@tudelft.nl

Willem van Driel[1]
W.D.vanDriel-1@tudelft.nl

GuoQi Zhang[1]
G.Q.Zhang@tudelft.nl

[1] *Delft University of Technology, Department of Microelectronics, Mekelweg 4, 2628 CD Delft, The Netherlands*
[2] *Chip Integration Technology Center (CITC), Transistorweg 5T, 6534 AT Nijmegen, The Netherlands*
[3] *Mintres B.V., De Nieuwe Erven 8, 5431 NT Cuijk, The Netherlands*

***Abstract* — Integrated Circuits and Electronic Modules experience concentrated thermal hot spots, which require advanced thermal solutions for effective distribution and dissipation of heat. The superior thermal properties of diamonds are long known, and it is an ideal material for heat-spreading applications. However, growing diamond films to the electronic substrate require complex processing at high temperatures. This research investigates a heterogeneous method of integrating diamond heat spreaders during the back-end packaging process. The semiconductor substrate and the heat spreader thicknesses were optimized based on simulations to realize a thermally enhanced Power Quad-Flat No-Lead package. The performance of the thermally enhanced PQFN was assessed by monitoring the temperature distribution across the active device surface and compared to a standard PQFN (without a heat spreader). Firstly, the thermally enhanced PQFN indicated a ∼9.6% reduction in junction temperature for an input power of 6.6W with a reduced thermal gradient on the active device surface. Furthermore, the diamond heat spreader's efficiency was observed to increase with increasing power input. Besides, the reliability of the thermally enhanced PQFN was tested by thermal cycling from –55°C to 150°C, which resulted in less than 2% thermal degradation over two-hundred cycles. Such choreographed thermal solutions are proven to enhance the packaged device's performance, and the superior thermal properties of the diamond are beneficial to suffice the increasing demand for high power.**

***Keywords* — Advanced thermal solutions, Advanced packaging, CVD Diamonds, Thermal Test Chips**

I. Introduction

Advances in the semiconductor lithography process, heterogeneous integration, and advanced electronic packaging is the driving factor for electrification [1; 2]. For instance, the transportation sector has experienced a paradigm shift due to carbon-neutral commitments. The percentage cost of electronics in automobiles was less than 10% in 1980, which surpassed ∼35% in 2010, and it is expected to reach 50% by 2030 [3]. The incremental growth also led to increased power density, i.e., the chip heat flux in today's modern devices is around 300 times higher than the flux density in 1980 (0.5 W/cm^2) [4; 5]. The increasing demand for high power in electronics emphasizes the need for thermal management. Device failure due to thermal breakdown is significantly higher than vibrations, humidity, and dust [5; 6].

Device heating is an undesirable side-effect during operation, thereby limiting its performance. With miniaturization and increasing chip density, the heat generation is concentrated within a small area, leading to thermal hot spots. For instance, the gate-to-gate spacing in Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) is typically less than 50μm, which creates concentrated thermal regions [7]. Heat sinks alone are insufficient to dissipate highly concentrated heat flux. Consequently, thermal barriers in power electronics are becoming inevitable. An overview of various materials and their thermal conductivity is shown in figure **1** [8; 9]. Thermal conductivity is the ability of a material to conduct heat, and diamonds are known for their excellent thermal conductivity. Diamond also has a relatively low thermal capacity, which makes it an ideal candidate as a heat spreader. Several researchers have focused on incorporating diamonds in power electronics as either active semiconductors or passive heat spreaders [7; 10–12]. Despite considerable research interests, incorporating diamonds in power electronics suffers from complex processing, high temperatures, and cost. Recent advancements in fabricating diamonds through Chemical Vapor Deposition (CVD) process have reduced the cost to ∼\$1/mm^2 [7].

2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) | 979-8-3503-3498-2/23/$31.00 ©2023 IEEE | DOI: 10.1109/ECTC51909.2023.00029

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00029

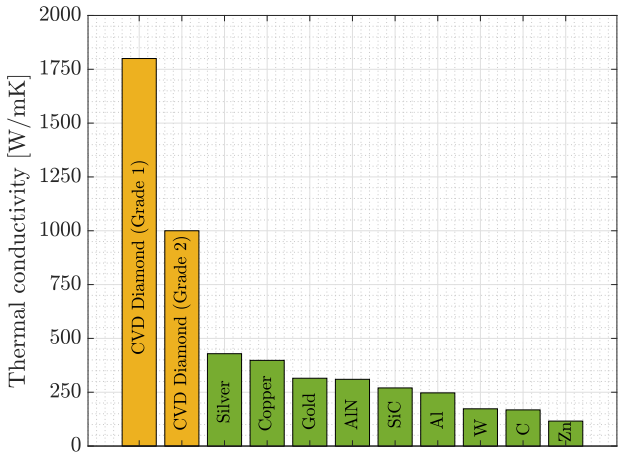


Fig. 1: The thermal conductivity of CVD diamond outperforms other materials such as silver, copper, and gold [8; 9]. CVD diamonds come in two grades; Grade 1 and 2 with thermal conductivity ranging from 1800 to 1000W/mK

The most common method of creating passive heat spreaders on active devices is growing synthetic diamond films on silicon substrates. However, these processes typically yield micro-crystalline structures resulting in higher thermal resistance between the Diamond-Silicon interface [12]. Besides, implementing such a complex process on wafer-level fabrication comes at a higher risk due to high processing temperatures. This study investigates a heterogeneous integration process of incorporating diamond heat spreaders to the backside of a thin silicon device during package assembly. A double sintering process using pressureless nano-silver sinter material was adapted for integration. Commercial Thermal Test Chips (TTCs) [13] were used as a test vehicle to characterize the heat spreading effect.

Firstly, the Silicon and Diamond layer thicknesses were optimized based on parametric transient thermal simulations. The heterogeneous integration process of realizing the thermally enhanced packages is then discussed along with the package integrity evaluation. Subsequently, the experimental evidence on the heat spreading effect is demonstrated by comparing standard packages (without a heat spreader) with thermally enhanced packages. Finally, the thermo-mechanical reliability of a thermally enhanced package was assessed for two-hundred thermal cycles from -55^{o}C to 150^{o}C. This paper concludes by summarising the empirical results and emphasizing the need for advanced thermal solutions.

II. Experimental Methods: Optimization and Assembly

Multiple heating and temperature-sensing elements within a single chip are needed to quantify the effect of heat spreading, which makes Thermal Test Chips (TTC) best suited for this

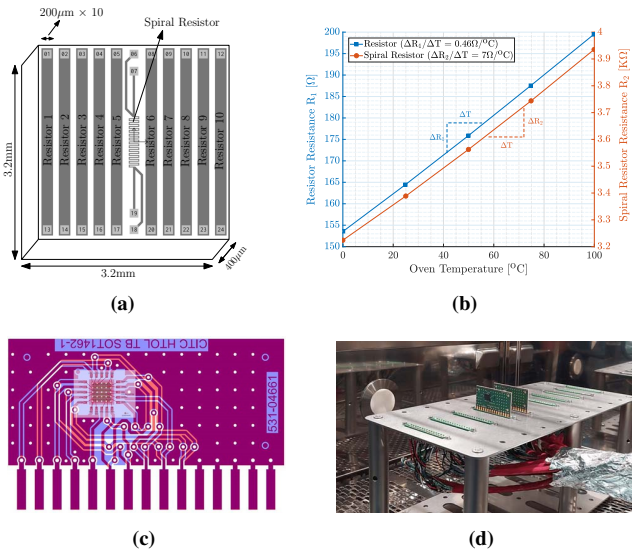


Fig. 2: **(a)** A schematic layout of the Thermal Test Chip (TTC) from [13]. The TTC has 10 Resistors with a resistance of $\sim$165Ω and a spiral resistor with a resistance of $\sim$3.4KΩ (typical at 25°C). **(b)** Calibration of the device resistance from 0°C and 100°C. The device shows a perfectly linear response with temperature. **(c)** A test board layout with double-side metallic tracks for electrical connection from the device to the equipment. **(d)** A test setup accommodating test boards inside thermal cycling (TMCL) oven for temperature-dependent electrical measurements.

application. Several research activities focus primarily on developing test chips [14–16]. Application of TTC for package-level reliability assessment have been previously investigated [17; 18]. A commercial TTC [13] is used in this research, and a schematic of the TTC is shown in figure **2a**. The resistive heating and sensing elements highlighted in figure **2a** have a linear temperature dependency. The resistance sensitivity of Resistors 1-10 is 0.46Ω/°C, and the resistance sensitivity of the spiral resistor is 7Ω/°C (figure **2b**). The differences in the resistance sensitivity of the various elements in the test chip are due to their geometrical differences. Normalizing the resistance sensitivity with the base resistance results in its material's Temperature Coefficient Resistance (TCR).

A Printed Circuit Board (PCB) was designed with 4-point kelvin connections (figure **2c**) to measure the resistance of the elements in the test chip (figure **2a**). The front side of the PCB was patterned for connections to a Power Quad Flat No-Lead (PQFN) surface mount package, and the backside has a copper ground plane for Electromagnetic Interference reduction. A test setup for accommodating the test boards were built inside a temperature-cycling (TMCL) industrial oven (figure **2d**). The test boards were connected to a source unit and a digital multi-meter via a switch matrix.

Material optimization is required to realize a thermally enhanced electronic package. Despite the diamond's superior thermal conductivity, the substrate thickness of the TTC (Sil-

icon) also influences thermal dissipation. Hence, a parametric numerical simulation study was conducted using Finite Element Methods (FEM) to identify optimal Silicon and Diamond layer thicknesses. The design of a complete PQFN package with the test board (figure **2c**) was simulated to represent the experimental conditions. A 3D Hexahedron mesh of the PQFN package materials with the test board is shown in figure **3**. The Von-Neumann stability criterion for thermal diffusivity needs to be satisfied to ensure a numerical convergence of the transient thermal simulation. To briefly explain the stability criterion, let us assume that the heat transfer through the system happens only through Conduction (i.e., ignoring the effect of Convection and Radiation). Accordingly, a one-dimensional temperature distribution equation can be expressed (equation 1), where x denotes the spatial coordinates, T denotes the temperature, t denotes the time, and α denotes the thermal diffusivity. Discretizing the one-dimensional equation results in the critical mesh ratio $r_c = \frac{\alpha \Delta t}{\Delta x^2}$, which must be less than or equal to 0.5. More details on the discretization and stability criterion are given in [18; 19].

$$\frac{\partial^2 T}{\partial x^2} = \left(\frac{1}{\alpha}\right) \cdot \frac{\partial T}{\partial t} \tag{1}$$

The geometrical inputs for the simulation are given in table **1**, and the material properties at room temperature are provided in table **2**. The thickness parameter of the die (Silicon) $\boldsymbol{a}$ is varied from 50μm to 400μm, and the heat spreader (Diamond) $\boldsymbol{b}$ is varied from 0μm to 400μm. The contact resistances between the Die-Heat spreader and the Heat spreader-Leadframe were chosen based on the thermal conductivity of Silver [23]. Likewise, the contact resistance between the Leadframe-PCB was chosen based on the thermal conductivity of the SAC305 solder paste. Glued contacts were assumed for all other contact points in the simulation.

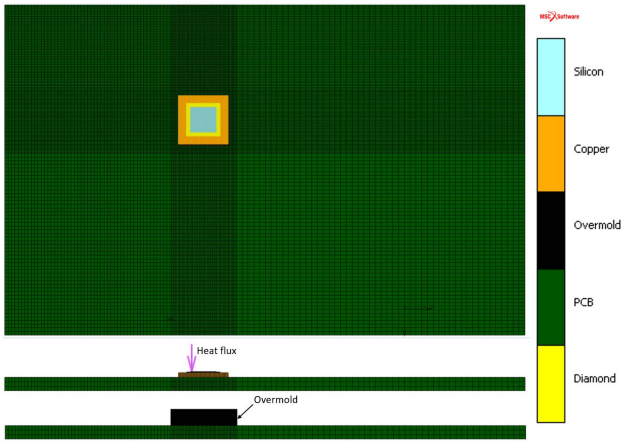


Fig. 3: A finite element Hexahedron mesh for transient thermal simulations with different layers (indicated in colors). The Von-Neumann stability criterion for thermal diffusivity was satisfied by limiting the mesh ratio of all layers to be less than the critical mesh ratio r_c.

Table 1: Geometrical dimensions of different layers (figure 3) is provided. The thickness of the TTC and the heat spreader are kept parametric. The overall thickness of the molding compound remains the same. However, the thickness of the molding compound above the die varies according to the defined parameters ($\boldsymbol{a}$ and $\boldsymbol{b}$).

Material	Width [mm]	Length [mm]	Thickness [mm]
Die	3.2	3.2	$\boldsymbol{a}$ = [0.05 - 0.4]
Heat spreader	4	4	$\boldsymbol{b}$ = [0 - 0.4]
Leadframe	6	6	0.55
PCB laminate	40	63	1.65
Overmold	8	8	2

Table 2: Silicon and copper thermal properties at room temperature were obtained from [20–22]. The properties of CVD Diamond were obtained from the supplier. The PCB design was simplified by assuming the properties of Polyimide (PCB laminate core). The Epoxy Molding Compound properties were taken from the datasheet of Sumitomo EME-G700LA.

Material	Density (ρ)$[g/mm^3]$	Conductivity (k) [W/mmK]	Specific heat (c_p) [J/gK]
Silicon	$2.32e^{-3}$	0.148	0.7
Diamond	$3.52e^{-3}$	1.8	0.5
Copper	$8.96e^{-3}$	0.401	0.385
Polyimide	$1.88e^{-3}$	0.00173	1.13
Epoxy	$0.95e^{-3}$	0.00096	1.9

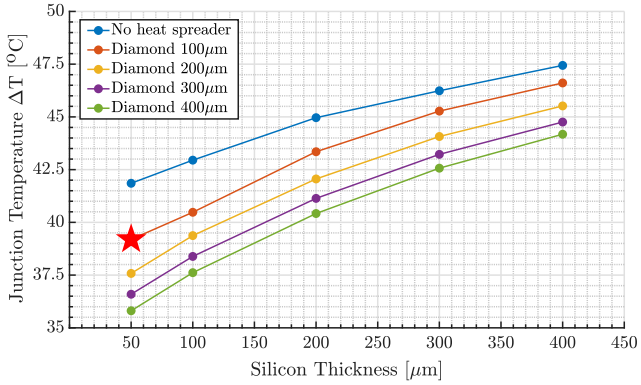


Fig. 4: Parametric transient thermal simulation results with input power of 6.6W (~10.5W/mm^2) applied at Resistor 1 location (figure **2a**) for a duration of 1 second. The Junction temperature recorded from simulations is the ΔT caused due to the applied input power at the end of 1 second. 50μm TTC thickness with 100μm Diamond heat spreader was chosen as an optimal point for this experimental study (highlighted in red).

An input power of 6.6W is applied at the Resistor 1 location (figure **2a**) for a duration of 1 second, which is equivalent to the input heat flux of ~10.5W/mm^2. The input power and heating time were chosen according to the experimental limitations (max. 40V restriction with the source unit). The Junction temperature was chosen as a metric to compare the effect of reducing the chip thickness (parameter $\boldsymbol{a}$) and increasing

the heat spreader thickness (parameter ***b***). The simulation results shown in figure **4** highlights the influence of the silicon and the heat spreader thicknesses on thermal dissipation. Reducing silicon thickness is favorable for achieving improved thermal performance, and adding a diamond heat spreader further reduces the junction temperature (figure **4**). However, it can be observed that the junction temperature reduction doesn't scale linearly with the Diamond thickness for 50μm Silicon. In other words, the maximum percentage difference for 50μm Silicon is observed between 0μm and 100μm Diamond. Hence, 50μm TTC thickness with 100μm Diamond heat spreader was chosen for this experimental study.

To realize a thermally enhanced packaged product (based on simulation results) requires a series of assembly processes to be carried out as depicted in schematics (figure **5**). The first step is to thin down the substrate thickness of the TTC. Since the lithographically defined active layers are at the top of the die, the back side of the TTC was polished to reduce the substrate thickness from 400μm to 50μm. The polished TTCs were cleaned with an ultra-sonic bath, and the chip was electrically probed to test its functionality. The polishing process removed the backside metallization, which is needed to promote its adhesion with the interconnect material. Hence, the polished backside of the test chips was sputter coated with Ti/Pt/Au of 100/200/600nm. Subsequently, the CVD diamond wafer of 110μm thickness was diced in the size of 4mm $\times$ 4mm and sputter coated with Ti/Pt/Au of 100/200/600nm. Nano-Silver sinter paste was dispensed on the metalized diamond slab using a time/pressure-controlled dispensing machine. The metalized thinned TTC was wet mounted to the diamond substrate using a die-bonder. Post wet-mounting, the die-diamond stack was sintered by a pressureless sintering process under Nitrogen. The sintering process happens in multiple stages; The first stage is the pre-sintering stage, during which the solvent evaporates, leaving behind nano-Ag particles. The second stage is the sintering stage, during

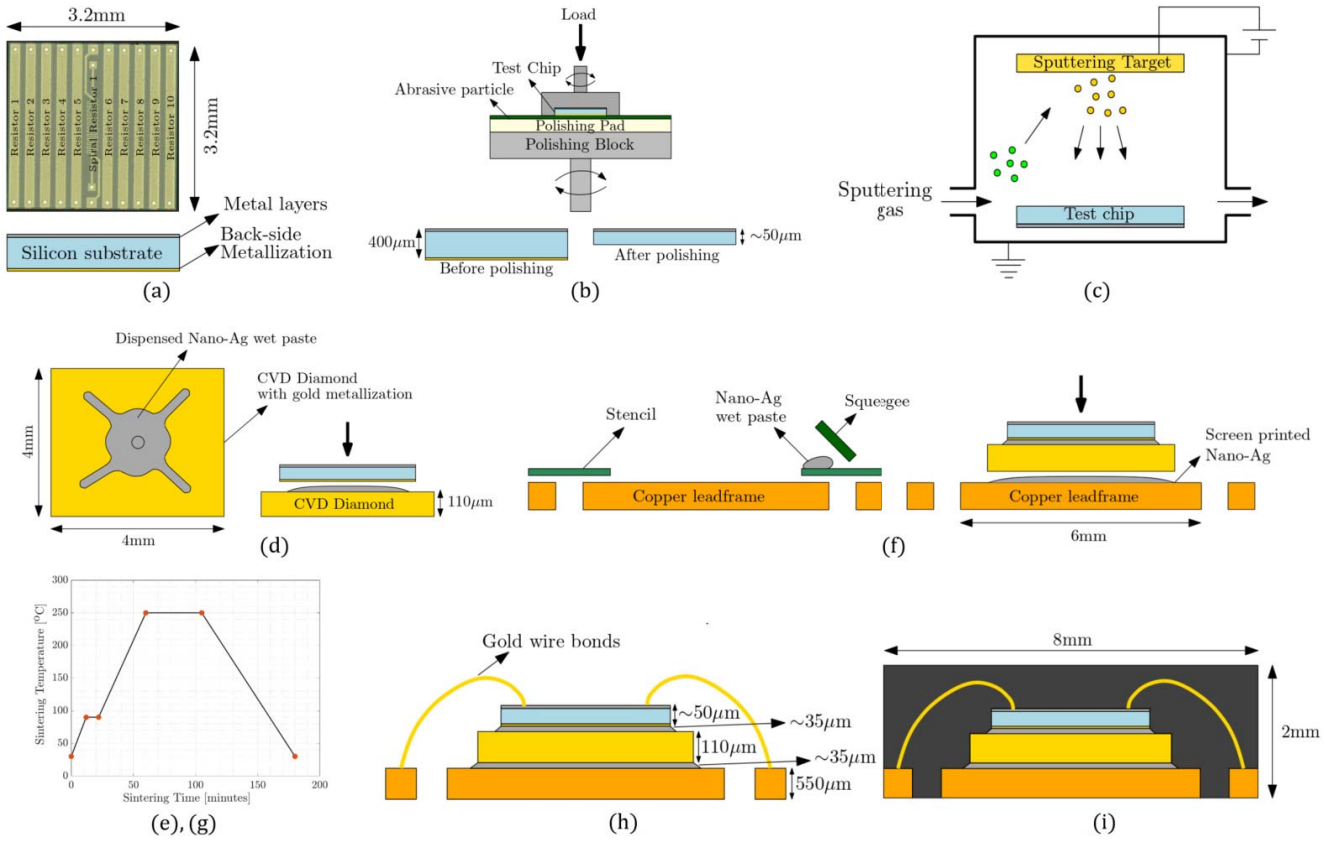
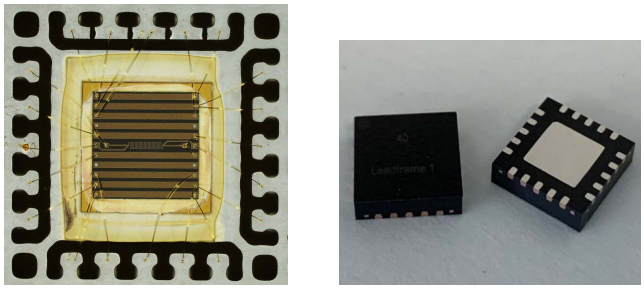


Fig. 5: **(a)** A Schematic of a TTC's geometry and different layers. **(b)** The thickness of the TTCs were reduced from 400μm to 50μm by back-side polishing process. **(c)** The backside of the test chip was metalized with Ti/Pt/Au of 100/200/600nm by sputtering. **(d)** Nano-Ag paste was dispensed on the Diamond slabs (also coated with Ti/Pt/Au of 100/200/600nm), and the metalized TTCs were placed using a die-bonder. **(e)** The wet-mounted TTC with the Diamond is sintered using a pressureless sintering process in a nitrogen-filled chamber of a sintering oven. **(f)** The Sintered Die-Diamond stack is then assembled on a lead frame with a nano-Ag paste screen printed on it. **(g)** The complete stack is sintered again by a pressureless sintering process. The sintered layer thicknesses are in the range of ~35μm. **(h)** The sintered samples are then wire-bonded with a 99.99% pure gold wire-bonds of 25μm thickness with a bond bump of 50μm. **(i)** The final stage of the assembly process involves transfer molding with an epoxy molding compound.



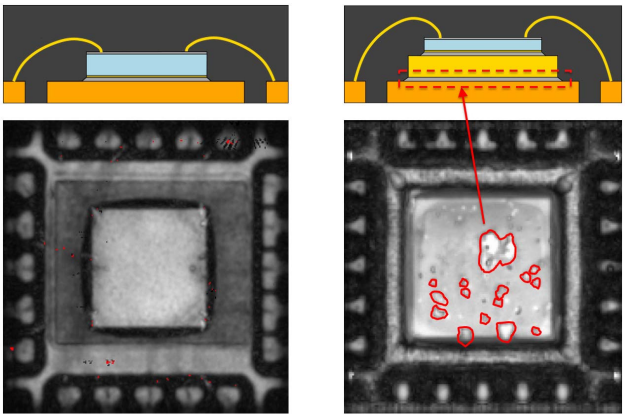
(a) **(b)**

Fig. 6: (a) An optical micrograph of the TTC with a Diamond heat spreader sintered to the die-pad of the lead frame. Electrical connections to the chip are established by wire bonds connecting the chip to the package bond pads. **(b)** Final optimized thermally enhanced PQFN packages are over-molded and singluated.

which the particles agglomerate. The matching CTE of the Die-Diamond favors sintering with lower thermo-mechanical stresses on the interface. The subsequent step involves screen printing of the nano-Ag paste to the die pad of the copper lead frame, and the sintered die-diamond stack is wet mounted. The complete stack is sintered again with a similar pressureless sintering process under Nitrogen. The sintered interface thicknesses are in the range of $\sim$35μm, which is based on the dispensed volume, the stencil thickness, and the material shrinkage.

After sintering, the electrical connections to the test chips are established using 99.99% pure gold wire bonds with 25μm bond wire and 50μm bond bump. An optical micrograph of the complete stack with wire bonds is shown in figure **6a**. Due to the limitation of the bond pads of the lead frame (20 pads), only resistors (1-3, 5-6, 8-10) and the spiral resistor (figure **2a**) are electrically connected. The resistors 2, 9, and the spiral resistor are connected with 4-point connections up to the TTC. The resistors 1, 3-8, and 10 are connected with 4-point Kelvin contacts until the bond pad of the lead frame. Once wire-bonded, the complete stack with the wire bonds is transfer molded with an epoxy molding compound and singulated into separate PQFN packages as shown in figure **6b**. The singulated packages are then soldered to a test board (figure **2c**) using a SAC305 solder paste.

To quantitatively analyze the heat spreading effects, standard PQFN packages (chip thickness 400μm without heat spreader) were also made in a similar processing condition. Confocal Scanning Acoustic Microscopy (CSAM) analysis was conducted on standard PQFN and thermally enhanced PQFN to evaluate the package integrity (figure **7**). Comparing the CSAM results of the standard PQFN (figure **7a**) and thermally enhanced PQFN (figure **7b**), it can be observed that the latter has voids (highlighted in red) in the interface material, i.e., in the nano-Ag sinter layer. From CSAM analysis, the location of voids was found to be in the Diamond-Leadframe interface. The presence of voids can be avoided by improving the sintering process. Nevertheless, the performance of the thermally enhanced PQFN can be assessed and compared against the standard PQFN despite the inhomogeneity in the interface layer.

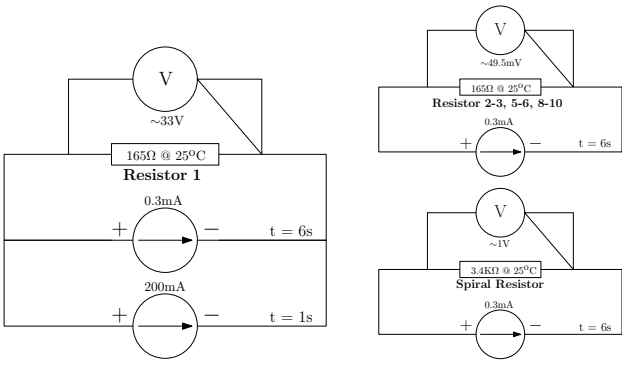


(a) CSAM - Standard PQFN **(b)** CSAM - Thermally Enhanced PQFN

Fig. 7: (a) CSAM imaging of the standard PQFN (400μm TTC without heat spreader) indicates a homogeneous interface. **(b)** CSAM imaging of the thermally enhanced PQFN (50μm TTC with 110μm heat spreader) highlights the presence of voids in the Diamond-Lead frame interface (highlighted in red).

III. Experimental Results

The standard PQFN and the thermally enhanced PQFN packages were tested inside the temperature-cycling oven, and the testing conditions are the same as explained in the simulations. An input power of 6.6W is applied at Resistor 1 (figure **2a**) for a duration of 1 second, which corresponds to $\sim$10.5W/mm^2 heat flux, and the device temperature was measured at 9 locations for a duration of 10 seconds. Multiple sourcing units are



(a) **(b)**

Fig. 8: (a) The electrical circuit of Resistor 1 is connected to two source units for simultaneous heating and sensing. **(b)** The electrical circuit of Resistor 2-3, 5-6, 8-10 (top), and spiral resistor (bottom) is connected to a single source unit for sensing application only. **(a)** and **(b)** The measurement current (0.3mA) was chosen accordingly to avoid self-heating effects.

connected to Resistor 1 for simultaneous heating and measuring as depicted in figure **8a**, whereas the Resistors 2-3, 5-6, 8-10, and the spiral resistor are connected with a single source for sensing application (figure **8b**). The electrical resistance measurements were translated into thermal readings based on the temperature dependency shown in figure **2b**.

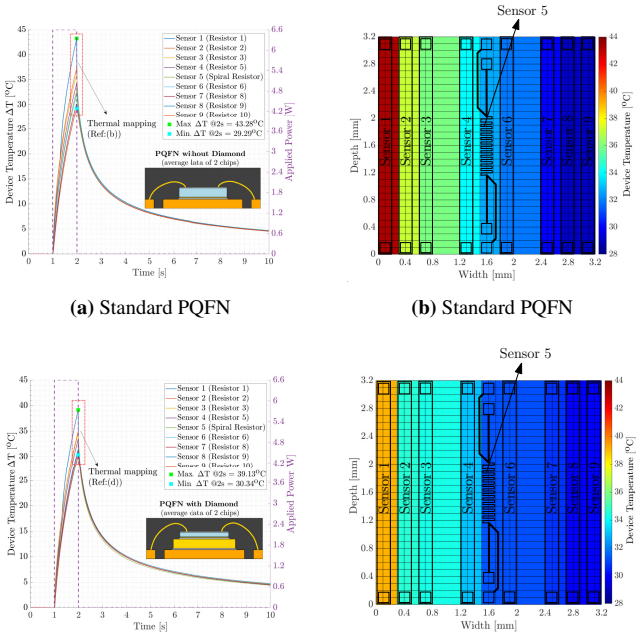
The heat spreading effect is demonstrated by measuring the device temperature at ambient room conditions (25°C), and the experimental results are shown in figure **9**. The results (figure **9**) shown is an average of two devices per package type. The maximum device junction temperature and the minimum temperature are highlighted in figures **9a** & **9c**. Comparing the standard PQFN against the thermally enhanced PQFN, the following are the significant differences observed:

- The maximum device junction temperature (figure **9a** & **9c**) shows a ∼9.6% reduction with the thermally enhanced PQFN samples as compared to the standard PQFN.

- Likewise, the minimum device temperature (figure **9a** & **9c**) indicates that the heat spreader redistributes the heat along the device surface, resulting in a lower thermal gradient. The same can be visually seen in figure **9b** & **9d**.

Subsequently, the thermal performance of the regular PQFN and the thermally enhanced PQFN were measured at different input power from 1.65W to 6.6W. The percentage reduction in the device junction temperature was chosen as a metric to compare the heat-spreading effect as a function of the input power (figure **10a**). The experimental measurements highlight that the percentage reduction in the junction temperature has a strong dependence on the applied heat input. An increase in the percentage from 3.57% to 9.6% was observed for the input power range from 1.65W to 6.6W (figure **10a**). Similar dependence was also observed from simulations. However, the semiconductor materials such as Silicon and Diamond have non-negligible temperature-dependent thermal properties, which need to be taken into consideration. Hence, the dependence of the percentage reduction in the junction temperature to its input power was simulated by considering the temperature-dependent properties of Silicon and Diamond. The effect of convective heat transfer to the environment was also included for the Overmold and the PCB. The simulation results are shown in figure **10b** with a tabulation of the temperature-dependent properties and the convective heat transfer coefficient used in the simulation.

The transient thermal simulation results (figure **10b**) indicate an increasing trend in the percentage reduction of the junction temperature as a function of input power (1.65W to 10W) as observed from the experiments. However, simulation results depict a much higher percentage reduction in junction temperatures (figure **10b**) than the experimental measurements (especially at a low power range). The primary reason



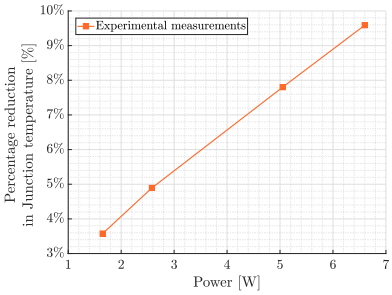
(a) Standard PQFN **(b)** Standard PQFN

(c) Thermally Enhanced PQFN **(d)** Thermally Enhanced PQFN

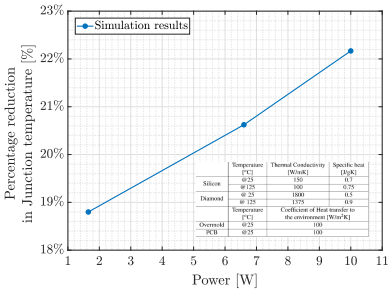
Fig. 9: (a) & (c) The device temperature ΔT measured (@25°C) at nine locations are shown (left axis) along with the power input (right axis). A maximum junction temperature (Max. ΔT) of 43.28°C is recorded for the standard PQFN, which is reduced to 39.13°C (∼9.6% lower) for the thermally enhanced PQFN. Likewise, the standard PQFN records a minimum temperature (Min. ΔT @t = 2s) of 29.29°C, as compared to 30.34°C with the thermally enhanced PQFN. This shows that the standard PQFN concentrates the heat and the thermally enhanced PQFN redistributes the heat. **(b) & (d)** The device temperature measured at t = 2s is mapped along the surface of the device for visual representation.

for the mismatch between the simulation and experimental results is the overestimation of the contact thermal resistances in the simulation. CSAM imaging of the thermally enhanced PQFN (figure **7b**) indicated the presence of voids, which results in higher thermal resistance. To evaluate the influence of the contact thermal resistance, the junction temperature of the thermally enhanced PQFN was simulated as a function of Die-Diamond and Diamond-Leadframe interface thermal conductivity. The simulation results are shown in figure **10c** and it is evident that there is a significant influence of the contact heat transfer coefficient parameter, especially for conductivity values lower than 100W/mK. Poor interface contacts decreases the efficiency of the heat spreader, which emphasizes the need for more research on interface materials in power packaging applications.

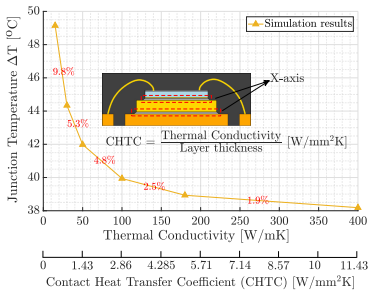
Furthermore, the thermally enhanced package reliability was assessed by thermal cycling from −55°C to 150°C for two-hundred cycles. During every cycle, the Junction temperature of the thermally enhanced PQFN was in-situ measured at 25°C (figure **11**). The experimental measurements are plotted with a 5-cycle Simple Moving Average and signs of



(a) Percentage reduction in Junction temperature as a function of applied heat input was experimentally measured for four different power inputs from 1W to 7W range. The efficiency of the heat spreader is observed to increase with increasing power input. Hence, the cost of developing thermally enhanced packages is truly beneficial for high-power applications.



(b) Percentage reduction in Junction temperature as a function of applied heat input was simulated from 1W to 10W power range. The transient thermal results were simulated with temperature-dependent material properties of Silicon and Diamond. The effect of convective heat transfer to the environment was also included in the simulation. The simulation results validate the claim from the experimental measurements on the effect of heat spreader efficiency increases with increasing power.



(c) The influence of the interface contact resistance was simulated by varying the contact heat transfer coefficient between the Die-Diamond and the Diamond-Leadframe interface. It can be observed that there is a significant difference in the device junction temperature for interface thermal conductivity less than 100W/mK. The simulation included the temperature-dependent properties and the convective heat transfer coefficient shown in **(b)**.

Fig. 10: **(a)**-experimental and **(b)**-simulation explains the influence of the applied power input on the heat spreading effect. **(c)** highlights the influence of interface resistance as a barrier to transport heat. It is evident that simulated results depict similar responses to the experimental results. However, the absolute values in the simulations don't match the experiments due to the overestimation of the interface resistance in the simulation and the mismatch in the thermal properties between the simulation and experiments.

degradation due to continuous stress testing can be observed. The junction temperature has increased by ∼1.95% after two-hundred thermal cycles as compared to its initial state. Yet the Junction temperature of the thermally enhanced package after two-hundred cycles is ∼7.25% lower than the junction temperature of the standard package at 0-cycle (figure **9a**).

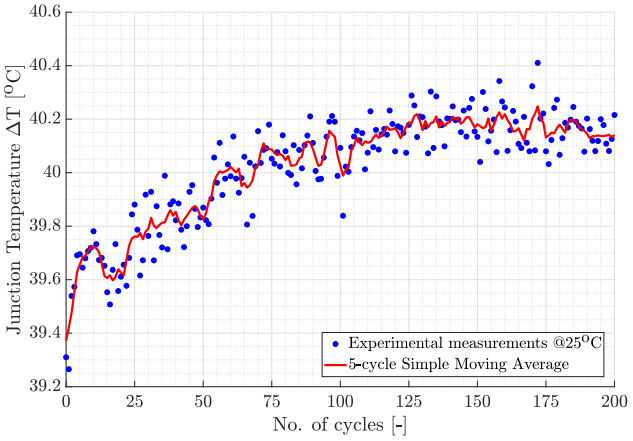


Fig. 11: The reliability of a thermally enhanced PQFN was tested by thermal cycling from −55°C to 150°C. The resolution of the measuring equipment is 10μV for measurements ranging from 10V to 100V. The measurement accuracy was calculated to be $\Delta V = \pm 12$mV. The repeatability of the measurements stays within the accuracy of the measuring equipment, which translates to ± 0.1°C as observed from the experimental data. Regardless, the devices were first calibrated to the measurement conditions, and the experimental data is averaged using Simple Moving Average 'μ'. The percentage of thermal degradation after two hundred cycles is observed to be less than 2%.

IV. Conclusion

The effect of the diamond heat spreader in high-power applications and the importance of tuning the semiconductor substrate and the heat spreader thicknesses are empirically analyzed in this research. A thermal test chip was substituted to characterize the heat-spreading effect. A heterogeneous integration approach was adapted for developing passive heat spreaders on thinned-down active devices. Accordingly, a thermally enhanced PQFN package was realized, and its performance was experimentally measured and compared against a standard PQFN package (without a heat spreader).

- For an applied input power of 6.6W, the thermally enhanced PQFN provides ∼9.6% reduction in Junction temperature as compared to a standard PQFN.
- More uniform distribution of heat is observed with the thermally enhanced PQFN due to the presence of a heat spreader. Whereas, the standard PQFN has concentrated heat sources.
- The percentage reduction in the junction temperature has a strong dependence on the applied heat input. Hence, the efficiency of a diamond heat spreader scales with the input power.
- Package degradation is inevitable. The thermally enhanced PQFN shows around 2% thermal degradation due to temperature cycling from −55°C to 150°C over two-hundred cycles. Yet, the Junction temperature measured after two hundred cycles is ∼7.25% lower than the junction temperature of the standard package at 0-cycle.

Advanced thermal solutions are needed to enhance the packaged device's performance, and the superior properties of the diamond are proven to be beneficial. Besides, the cost of manufacturing CVD diamonds is decreasing due to technological advancements, whereas the thermal issues in high-power electronics are increasing especially in harsh applications. Hence, the benefits of incorporating diamonds in high-power electronics are evident despite its cost. Furthermore, the beneficial properties of diamonds attract future research toward multi-chip high-power packaging applications.

V. Acknowledgment

This research was a collaborative work of the Delft University of Technology, Chip Integration Technology Center, and Mintres B.V. The author expresses his gratitude to Mintres B.V. for their support. Special thanks to Mohammed Achour - Engineer Material Analysis at NXP Semiconductors, for CSAM imaging.

References

[1] K. Leahy, G. Oster, "The Evolution of Electronic Systems Technology and Its Impact on Methods of Innovation," Journal: Regent Global Business Review, Issue: 2, Volume 5, 2012.

[2] T. G. Wilson, "The evolution of power electronics," in IEEE Transactions on Power Electronics, vol. 15, no. 3, pp. 439-446, May 2000, doi: 10.1109/63.844503.

[3] Deloitte, Semiconductors - the Next Wave. (April, 2019), Automotive electronics cost as a percentage of total car cost worldwide from 1970 to 2030. In *Statista*. Retrieved from https://www.statista.com/statistics/277931/automotive-electronics-cost-as-a-share-of-total-car-cost-worldwide/

[4] M. J. Ellsworth, "Chip power density and module cooling technology projections for the current decade," The Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems (IEEE Cat. No.04CH37543), 2004, pp. 707-708 Vol.2, doi: 10.1109/ITHERM.2004.1318362.

[5] A. Sundaram, R. Velraj, (2008). Thermal management of electronics: A review of literature. Thermal Science - THERM SCI. 12. 5-26. 10.2298/TSCI0802005A.

[6] F. Blaabjerg, H. Wang, I. Vernica, B. Liu and P. Davari, "Reliability of Power Electronic Systems for EV/HEV Applications," in Proceedings of the IEEE, vol. 109, no. 6, pp. 1060-1076, June 2021, doi: 10.1109/JPROC.2020.3031041.

[7] T. Obeloer, B. Bolliger, "Application of Diamond Heat Spreaders for the Thermal Management of GaN Devices," April 2016. Retrieved from Electronics Cooling magazine - https://www.electronics-cooling.com/2016/04/application-of-diamond-heat-spreaders-for-the-thermal-management-of-gan-devices/

[8] Thermtest Materials Database. Retrieved from https://thermtest.com/materials-database

[9] Mokhena, T. C., Mochane, M. J., Sefadi, J. S., Motloung, S. V., & Andala, D. M. (2018). Thermal Conductivity of Graphite-Based Polymer Composites. Impact of Thermal Conductivity on Energy Technologies. doi:10.5772/intechopen.75676

[10] N. Donato, N. Rouger, J. Pernot, G. Longobardi, & F. Udrea, (2019). Diamond power devices: State of the art, modelling and figures of merit. Journal of Physics D: Applied Physics. 53. 10.1088/1361-6463/ab4eab.

[11] G. Perez, M. Aurelien, C. Gauthier, L. Pierre, J. Pierre-Olivier, E. David, & R. Nicolas. "Diamond semiconductor performances in power electronics applications." Diamond and Related Materials, Volume 110, 2020, 108154, ISSN 0925-935, https://doi.org/10.1016/j.diamond.2020.108154.

[12] Guillemet, T., "Diamond-based heat spreaders for power electronic packaging applications", ProQuest Dissertations And Theses; Thesis (Ph.D.)–The University of Nebraska - Lincoln, 2013.; Publication Number: AAT 3591531; ISBN: 9781303321276; Source: Dissertation Abstracts International, Volume: 74-12(E), Section: B.; 285 p.

[13] Nanotest NT16-3k-WB, Technical Data Sheet, rev.13, https://nanotest.eu/ttc, 2018.

[14] Siegal, Bernie Galloway, Jesse. (2008). Thermal Test Chip Design and Performance Considerations. 59 - 62. 10.1109/STHERM.2008.4509367.

[15] B. Frostholm, (August 2014), Thermal test chips streamline system development. Retrieved from https://www.edn.com/thermal-test-chips-streamline-system-development/

[16] R. Sattari, H. van Zeijl and Q. Zhang, "Design and Fabrication of a Multi-Functional Programmable Thermal Test Chip," 2021 IEEE European Microelectronics and Packaging Conference (EMPC), 2021 (in press).

[17] R. Sattari, D. Hu, X. Liu, H. van Zeijl, S. Vollebregt, G. Q. Zhang, "Transient thermal measurement on nano-metallic sintered die-attach joints using a thermal test chip," Applied Thermal Engineering, Volume 221, 2023, 119503, ISSN 1359-4311, https://doi.org/10.1016/j.applthermaleng.2022.119503.

[18] H. A. Martin, R. Sattari, E. C. P. Smits, H. W. van Zeijl, W.D. van Driel and G. Q. Zhang, "In-situ reliability monitoring of power packages using a Thermal Test Chip," 2022 23rd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2022, pp. 1-10, doi: 10.1109/EuroSimE54907.2022.9758913.

[19] S. B. Yuste, L. Acedo, (2005). An Explicit Finite Difference Method and a New von Neumann-Type Stability Analysis for Fractional Diffusion Equations. SIAM J. Numerical Analysis. 42. 1862-1874. 10.1137/030602666.

[20] Glassbrenner, C. J. and G. A. Slack, Phys. Rev. 134, 4A (1964) A1058-A1069.

[21] Okhotin, A. S., A. S. Pushkarskii, and V. V. Gorbachev, Thermophysical Properties of Semiconductors, Moscow, "Atom" Publ. House, 1972, (in Russian).

[22] Simon, N. Drexler, Elizabeth Reed, R.. (1992). Properties of Copper and Copper Alloys at Cryogenic Temperatures. NIST Monograph. 177.

[23] Andrew A. Wereszczak, Dainel J. Vuono, Hsin Wang, and Mattison K. Ferber, Properties of Bulk Sintered Silver as a function of porosity, Oak Ridge National Laboratory (ORNL/TM-2012/130)