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A Single-Supply Balun-First Three-Way mm-Wave Doherty PA

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***Abstract*— This article introduces a single-supply balun-first three-way parallel Doherty power amplifier (PA) tailored for millimeter-wave (mm-wave) fifth-generation (5G) applications. It incorporates a bandwidth enhancement technique that widens the operational frequency range, enhances broadband power back-off (PBO) efficiency, and reduces impedance mismatch between differential PAs. Realized in 40-nm CMOS bulk technology with a core area of 0.77 mm^2, the prototype delivers a saturated power/peak gain surpassing 20 dBm/16 dB, and it demonstrates a drain efficiency (DE) exceeding 15%/22%/33% at 9.5 dB/6 dB/0 dB PBO across a 24–30 GHz band. The proposed mm-wave PA achieves EVM/ACLR values of −24.3 dB/−30.1 dBc for a 1-GHz 64-QAM OFDM signal, operating at an average output power (Pout) of 9.4 dBm with an average DE of 15%. For a 50-MHz 1024-QAM OFDM signal, it achieves an average Pout/DE of 8.6 dBm/12% with EVM/ACLR of −30 dB/−36.3 dBc.**

***Index Terms*— Compact, Doherty, lumped components, millimeter wave, Norton transformation, power amplifier (PA), three-stage.**

I. Introduction

THE millimeter-wave (mm-wave) spectrum finds application in various emerging fields like radar sensors and fifth-generation (5G) cellular networks. In the context of 5G networks, advanced techniques like phased arrays and spectrally efficient complex modulation are employed for multi-Gbit/s data transmission and low-latency line-of-sight links [1], [2], [3], [4]. As Table I outlines, exploiting higher-order modulation schemes such as quadrature-amplitude modulations (QAMs) and orthogonal frequency-division multiplexing (OFDM) presents uncompromising challenges due to their high peak-to-average power ratios (PAPRs). These challenges place stringent demands on power amplifiers (PAs), requiring considerations for output power (Pout), average efficiency, error vector magnitude (EVM) for in-band linearity, and adjacent channel leakage ratios (ACLRs) for out-of-band spectral purity [5], [6]. Likewise, the push for high integration, cost-effectiveness, compact size, and efficiency drives the exploration of nanoscale CMOS technologies for 5G mm-wave transmitters (TXs). However, limited supply voltage and maximum oscillation frequency ($f_{\max}$) pose difficulties in meeting the power specifications of 5G TXs. The average and peak power requirements for various 5G scenarios are detailed in Table I.

TABLE I

5G System Requirements [5], [6]

PAPR for various modulations (Filter roll-off factor = 0.25)						
Modulation	QPSK SC	16 QAM SC	64 QAM SC	QPSK OFDM	16 QAM OFDM	64 QAM OFDM
PAPR (dB)	5	6.9	7.1	9.7	10.4	11

3GPP minimum EVM requirement					
Modulation	BPSK	QPSK	16 QAM	64 QAM	256 QAM
Required EVM (dB)	-10.5	-15	-18	-21.9	-29.1

5G 28/39 GHz application scenarios and estimated requirements				
Scenario	Handset	Access point	Base station	Backhaul
$EIRP_{avg}$ (dBm)	30	45	55	60
N_{ant}	4-6	32	64	256
P_{avg}/PA (dBm)	11-15	12	16	9
P_{peak}/PA (dBm) (PAPR = 12 dB)	23-27	24	28	21
Average Efficiency (%)	20	20	20	20
DC power (W)	0.4-0.6	2.5	12	10

For instance, under certain assumptions, the backhaul link budget necessitates an average/peak TX power exceeding 9/21 dBm. These assumptions include a 12 dB PAPR, 5 dB antenna gain, 2 dB connection loss between PA and antenna, and a 16×16 phased-array antenna configuration to counteract free space path loss at mm-wave frequencies. The PAs play a crucial role in determining Pout, average efficiency (which impacts thermal management) and overall reliability of the TX system. Additionally, these mm-wave 5G front-ends need to offer substantial power gain to relax design constraints for the preceding upconversion stages [5], [7].

While recent mm-wave linear PA designs have addressed EVM and ACLR requirements of 5G systems, achieving high average efficiency remains largely unresolved [8], [9], [10], [11], [12], [13], [14], [15]. To overcome the average efficiency

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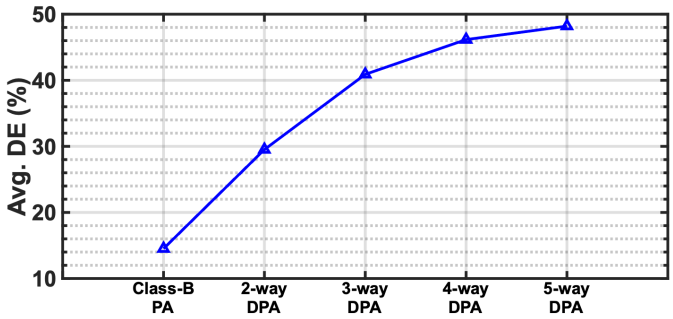


Fig. 1. OFDM signal's average DE with PAPR = 11.6 dB for Class B and N-way Doherty PAs.

and Pout issues in TXs, techniques like outphasing [16], [17], [18], [19], load-modulated balanced amplifiers (LMBAs) [20], [21], and N-way Doherty architectures [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36] have been explored. Outphasing PA demands significant baseband resources for generating outphasing signals and extensive digital predistortion (DPD). LMBA supports wideband modulation, but its power combiner introduces substantial die area, resulting in high insertion loss and reduced peak efficiency.

Among the various N-way Doherty configurations, a two-way Doherty PA is often realized [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33]. Nonetheless, this configuration does not completely tackle the issue of enhancing average efficiency for signals with high PAPRs, approximately 12 dB. Additionally, generating more than 21 dBm Pout utilizing only two power devices using CMOS technology is challenging. N-way Doherty architectures also tend to be inherently narrowband due to the quarter-wave transmission line (TLs) impedance inverter utilized for load modulation. Besides, their bandwidth decreases as the order of Doherty architecture increases.

The average drain efficiency (DE), as shown in Fig. 1, is calculated by combining the probability distribution function (pdf) of the orthogonal frequency division multiplexing (OFDM) signal with the DE of the PA. The graph displays the average DE for different PA architectures: ideal class B, two-, three-, four-, and five-way Doherty, all for an OFDM signal with a PAPR of 11.6 dB. Notably, the average DE has no substantial enhancement beyond the three-way Doherty architecture. Consequently, considering practical constraints and losses in an N-way combiner at mm-wave frequencies, thorough analysis indicates that the three-way Doherty PA stands out as a strong candidate. Its performance at 12 dB PAPR is comparable to four-/five-way Doherty architectures while featuring a more compact combiner and reduced design complexity [37]. Recently implemented three-way [35], [36] and four-way [34] architectures are also narrowband, particularly at deep PAPR levels. Furthermore, they commonly rely on two supply voltages in cascode PA structure and complex power management systems in their front-end stages to achieve the required power gain and radiated power. Thus, realizing a compact mm-wavefront-end with high average efficiency across a wide frequency range, using a single supply while adhering to the tight element-to-element $\lambda/2$ lattice spacing requirement of phased arrays remains a significant challenge.

An alternative approach has recently been realized that features a compact single-supply three-stage mm-wave three-way Doherty PA that employs a technique to enhance bandwidth (EBW) for broader operational frequency coverage [38]. This article elaborates on its architecture analysis, circuit-level design considerations, and extensive measurement results, organized as follows: Section II delves into the analysis of different three-way Doherty topologies, focusing on their operational bandwidth. Enhanced bandwidth (EBW) technique is detailed in Section III. Following the design methodology presented in Section IV, a compact power combiner comprising three identical balanced-to-unbalanced (balun) transformers, an inductor, and three capacitors is synthesized. Section V provides insights into the circuit implementation of the proposed Doherty PA prototype fabricated using the 40 nm bulk CMOS technology. Experimental results are discussed in Section VI, and the article concludes in Section VII.

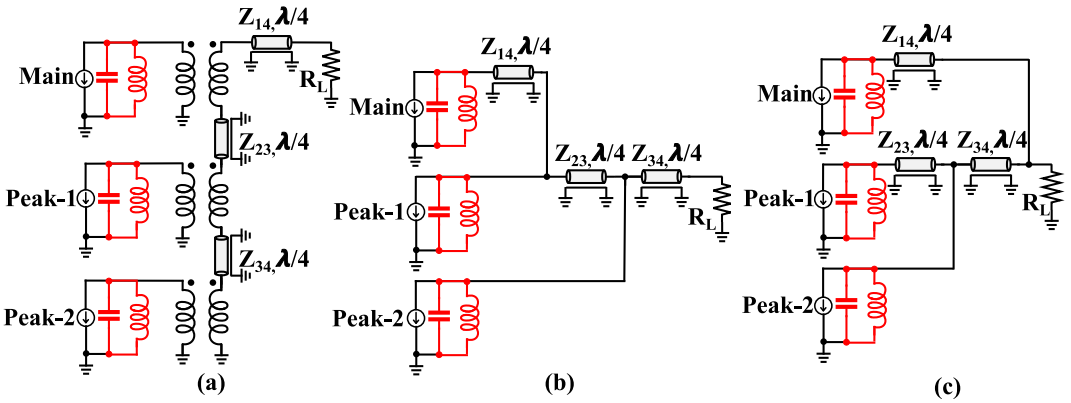
II. Three-Way Doherty Variants

The three-way Doherty architecture can be deployed in a series configuration or a parallel configuration. Various iterations of the three-way Doherty architecture are illustrated in Fig. 2. The design equation for the proposed three-way Doherty structure is detailed in [37]. An inductor is employed to counteract the parasitic drain–source capacitance of the PA, as indicated by the red color in all three schematics.

The key advantages of the proposed three-way parallel Doherty combiner are as follows.

1) Among the different configurations, the three-way series Doherty configuration exhibits superior performance in terms of DE and Pout across the frequency spectrum (as shown in Fig. 3). However, this configuration necessitates three transformers for the main, peak-1, and -2 devices. In contrast, the parallel Doherty configuration only requires a balun for differential operation. Using three transformers in the series configuration leads to significant DE and Pout degradation compared to the parallel Doherty setup.
2) Traditional parallel Doherty demands the current of the main device to increase linearly with the input RF voltage up to the first back-off point and then to maintain a constant level up to full power. Executing this feature is challenging in analog PAs and can lead to nonlinearity issues [39].
3) During deep power back-off (PBO), the proposed combiner operates with only the main PA active, establishing a direct signal path between the main PA output and the overall Doherty PA output. This results in minimal power loss. The OFF-state impedance of the peak-1 PA primarily influences the efficiency of the proposed combiner.

The symmetrical Doherty configuration offers the advantage of employing the same chain for the main, peak-1, and -2. Consequently, the proposed parallel Doherty architecture is designed symmetrically (with $K1 = 0.5$ and $K2 = 0.33$). However, Fig. 3 highlights that the proposed three-way Doherty configuration has limitations regarding its operational bandwidth.



Transmission line (TLs)	Conventional 3-way series Doherty (a)	Conventional 3-way parallel Doherty (b)	Proposed 3-way parallel Doherty (c)
Z_{14}	$\frac{\sqrt{R_L * R_{opt\_max}}}{K2}$	$\frac{R_{opt\_max}}{K1 * K2}$	$\frac{\sqrt{R_L * R_{opt\_max}}}{K2}$
Z_{23}	$\frac{R_L * K2}{K1}$	$\frac{R_{opt\_max}}{K1}$	$\frac{\sqrt{R_L * R_{opt\_max}}}{1-K2}$
Z_{34}	$\frac{R_L * K2^2}{K1 * (1-K2)}$	$\sqrt{R_{opt} R_L}$	$\frac{R_{opt\_max}}{K1 * (1-K2)}$

(d)

Fig. 2. (a) Conventional three-way series Doherty, (b) conventional three-way parallel Doherty, (c) proposed three-way parallel Doherty [38], and (d) equations for calculating characteristic impedance (Z_0) of each TL for each design.

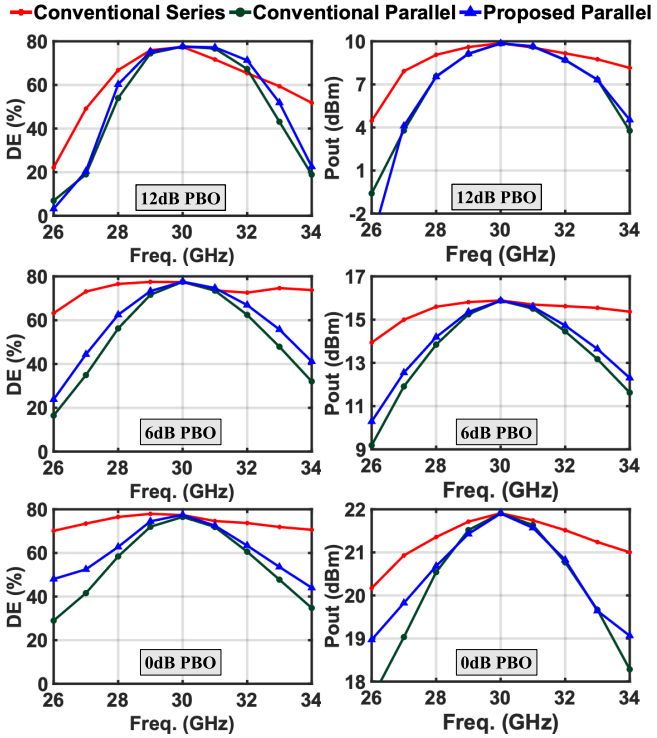


Fig. 3. DE and Pout across frequency at 12/6/0 dB PBO for $K1 = 0.5$ and $K2 = 0.25$.

III. Bandwidth Analysis

Due to its impractical size for on-chip implementation at mm-wave frequencies, the TL can be substituted with either a high-pass (HP) configuration [depicted in Fig. 4(a)] or a low-pass (LP) counterpart [illustrated in Fig. 4(b)] using lumped element models. The HP model is chosen because it incorporates shunt inductors acting as a dc feed and provides inherent transformation into a differential circuit. Upon replacing each of the TL components (Z_{14}, Z_{23}, and Z_{34}) with the HP model, the parallel elements are consolidated, resulting in the schematic depicted in Fig. 4(c). The values of the inductor and capacitor in the lumped element model are computed based on the characteristic impedance (Z_0) of the TL [refer Fig. 4(a) and (b)]. Z_{14}, Z_{23}, and Z_{34} correspond to Z_0 of each respective TL.

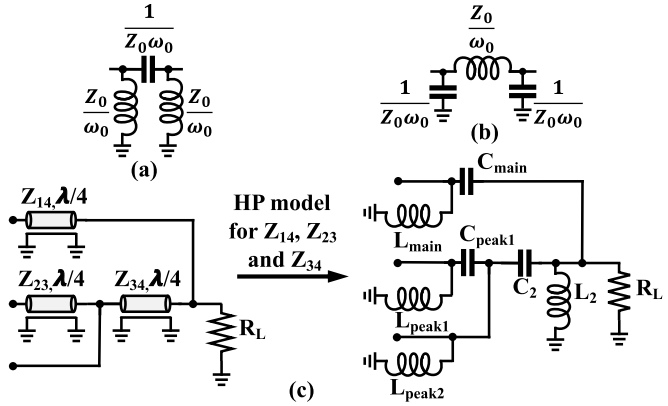


Fig. 4. (a) HP lumped element model, (b) LP lumped element model, and (c) proposed three-way parallel Doherty using lumped elements.

A. Bandwidth Enhancement Technique

Fig. 5 depicts a step-by-step design procedure for the proposed EBW onto the suggested three-way parallel Doherty network. This technique is applied to the main PA's path,

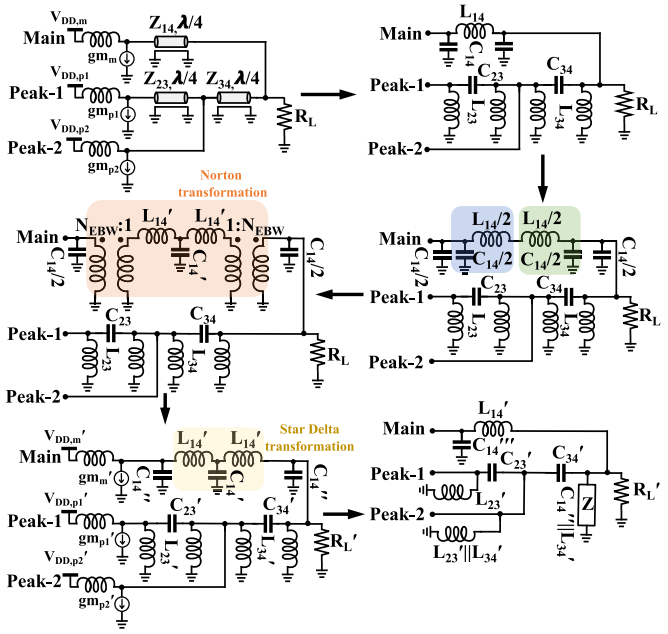
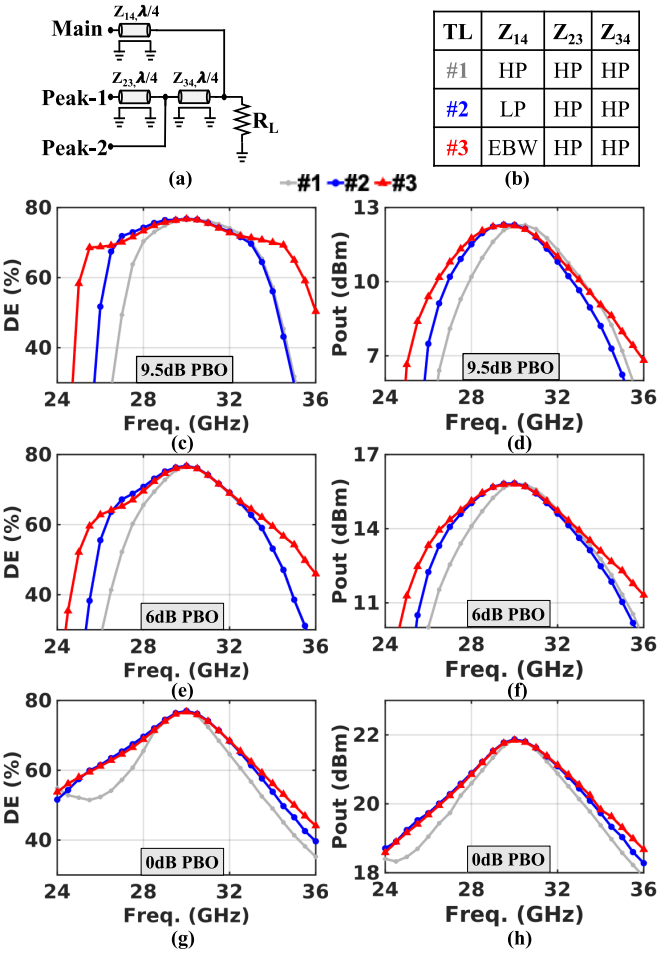


Fig. 5. Proposed compact EWB technique on a three-way Doherty combiner.

which experiences the most prominent power losses. The process starts by substituting the Z_{14} TL with its LP lumped element equivalents. Subsequently, the capacitors and the inductor within the main path are divided, accompanied by a Norton transformation [40]. This transformation then leads to replacing the obtained transformer with the following adjustments: reducing the main supply source (V_{DD}) by N_{EBW}, increasing the transconductance of the power device (gm) by N_{EBW}, augmenting capacitors by N_{EBW}^2, and decreasing inductors and impedance seen at the drain node by N_{EBW}^2, as shown in (1). Finally, a more compact three-way combiner configuration is achieved through the utilization of a star-to-delta transformation

$$\begin{aligned} V'_{\mathrm{DD}} &= \frac{V_{\mathrm{DD}}}{N_{\mathrm{EBW}}} \\ gm' &= gm \times N_{\mathrm{EBW}} \\ C' &= C \times N_{\mathrm{EBW}}^2 \\ L' &= \frac{L}{N_{\mathrm{EBW}}^2} \\ R' &= \frac{R}{N_{\mathrm{EBW}}^2}. \end{aligned} \tag{1}$$

Fig. 6 displays three versions of the concept. In version 1, the HP model is applied to all the TLs alongside the lumped element equivalence illustrated in Fig. 4(c). Version 2 employs the LP model, replacing the Z_{14} TL. In version 3, the EBW technique is employed on the Z_{14} TL, incorporating the final lumped-element circuit shown in Fig. 5. Each version is simulated using an ideal current source and ideal components with an infinite quality factor (QF). Fig. 6 reveals that version 3 exhibits enhanced bandwidth for DE, particularly noticeable at deep PBO levels. Considering a QF of 15 for the inductors and 25 for capacitors, all three cases are simulated [37], [41]. Fig. 7 presents the enhancement in DE and P_{out} at 0/6/9.5 dB



TL	Z_{14}	Z_{23}	Z_{34}
#1	HP	HP	HP
#2	LP	HP	HP
#3	EBW	HP	HP

Fig. 6. (a) Three-way Doherty structure, (b) variations in the three-way Doherty architecture, (c) DE versus frequency at 9.5 dB PBO, (d) Pout versus frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) Pout versus frequency at 6 dB PBO, (g) DE versus frequency at 0 dB PBO, and (h) Pout versus frequency at 0 dB PBO using the ideal inductor and capacitor.

PBO levels across the bandwidth for the proposed three-way Doherty structure integrated with EBW.

Variations in the three-way Doherty architecture can be achieved by alternating between the LP and HP models for the Z_{23} and Z_{34} TLs, as illustrated in Fig. 8(a). All simulations are carried out with an ideal PA model and a QF of 25/15 for the capacitors and inductors. The results indicate that alternative 4 in Fig. 8(a) outperforms its counterparts across frequencies at 9.5/6/0 dB PBO. The observed improvement in performance can be comprehended through an analysis of the HP and LP models of the TLs. Discrepancies in Pouts, as shown in Figs. 7 and 8, stem from variations in passive losses, given that the HP model of the TL incorporates two inductors compared to the LP model, thereby increasing passive losses.

B. Analysis of HP and LP Models of RLs

Fig. 9(a)–(d) presents the magnitude and phase profiles of S_{21} for the LP and HP lumped element models [as illustrated in Fig. 4(a) and (b)] of the TL over various characteristic impedance (Z_0) settings spanning the frequency range of 24–36 GHz. After applying the EBW technique, the new value of the inductors and capacitors can be calculated using (1).

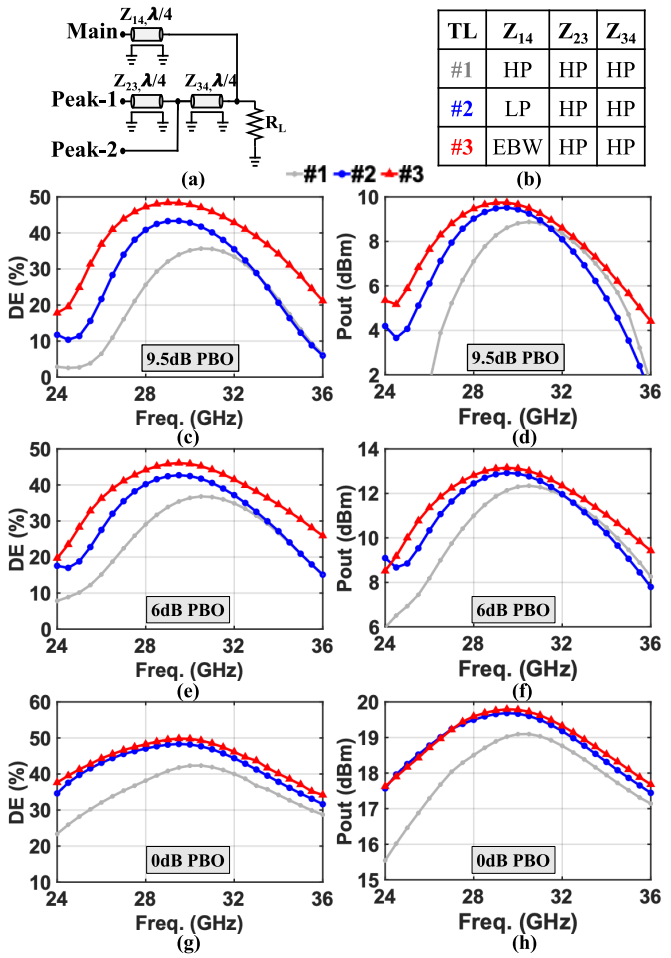


Fig. 7. (a) Three-way Doherty structure, (b) variations in the three-way Doherty architecture, (c) DE versus frequency at 9.5 dB PBO, (d) Pout versus frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) Pout versus frequency at 6 dB PBO, (g) DE versus frequency at 0 dB PBO, and (h) Pout versus frequency at 0 dB PBO using QF of 25/15 for capacitors and inductors.

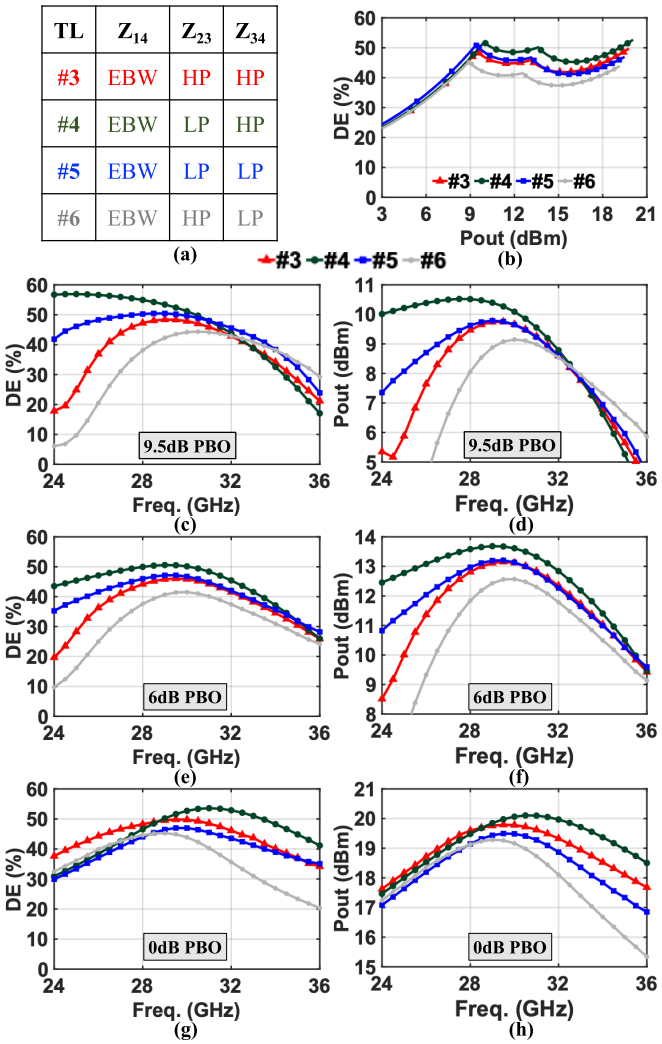


Fig. 8. (a) Variations in the three-way Doherty architecture, (b) DE versus Pout, (c) DE across frequency at 9.5 dB PBO, (d) Pout across frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) Pout across frequency at 6 dB PBO, (g) DE across frequency at 0 dB PBO, and (h) Pout across frequency at 0 dB PBO using QF of 25/15 for capacitors and inductors.

Then, Z_0 EBW in Fig. 9(a)–(d) can be calculated. Z_0 and Z_0 EBW can be related as Z_0 EBW $= Z_0/N_{\text{EBW}}^2$. Additionally, Fig. 9(e) exhibits the variations in magnitude and phase of TL's S_{21} within the frequency range of 24–36 GHz, relative to different Z_0 values. These visualizations reveal a noteworthy trend: as Z_0 of the TL decreases, phase variation diminishes, while the reverse is observed for magnitude variation. Furthermore, the LP model of the TL exhibits lower phase and magnitude variations compared to the HP model. In Fig. 9(f), the phase variation of S_{21} is presented against frequency, examining cases where lumped element models of the TLs (with $Z_0 = 50\ \Omega$) are arranged in distinct configurations, such as HP-LP, LP-HP, HP-HP, and LP-LP. This analysis suggests that both HP-LP and LP-HP configurations exhibit relatively flat phase responses across frequencies when contrasted with the other configurations.

Among all considered versions, version 4 (depicted in Fig. 10) demonstrates superior performance in terms of bandwidth. This feature can be attributed to its integration of two LP models for the TLs and the application of EBW, which consequently reduces Z_0 of each TL. Furthermore, version 4 incorporates a hybrid of LP and HP circuits within the peak PAs, leading to diminished phase variation in the equivalent passive network when compared to version 5. The adjacency of an LP structure to the active power devices contributes to the absorption of parasitic drain–source capacitance. Additionally, the utilization of EBW results in reduced inductor values, facilitating smoother layout implementation and less susceptibility to QF influences. Finally, the proposed three-way Doherty architecture resembles an inverted two-way Doherty PA [26], enhancing its operational bandwidth.

IV. Proposed Balun-First Three-Way Doherty Power Combiner

Mm-wave PA implementations commonly adopt push-pull PAs to enhance stability and increase Pout. Moreover, these push–pull PAs typically integrate a balun transformer at their end, catering to single-ended antenna configurations. Fig. 11(a) displays the schematic of version 4, presented in a push–pull configuration, while its corresponding layout is

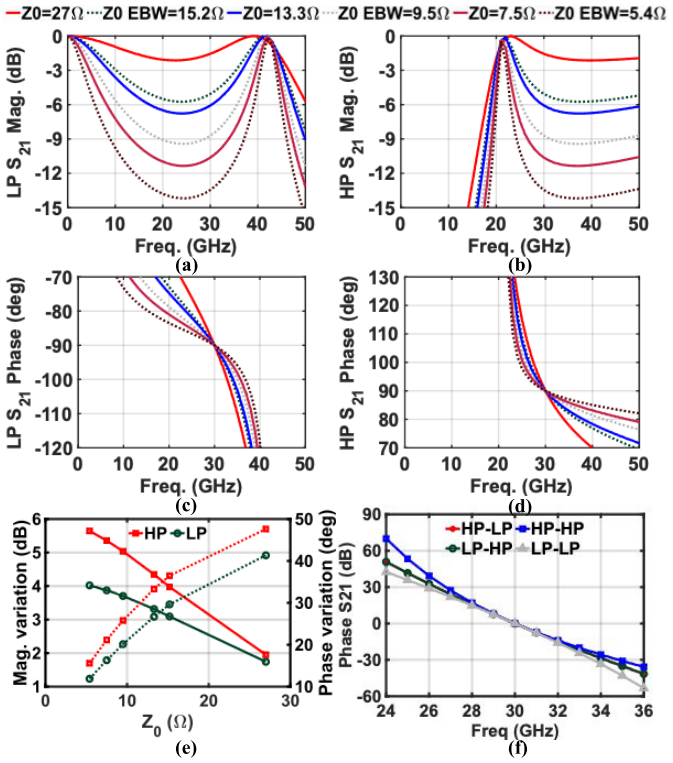


Fig. 9. Magnitude of TL for different characteristic impedance for (a) LP, (b) HP, phase of TL for different characteristic impedance for (c) LP, (d) HP, (e) magnitude variation and phase variation versus characteristic impedance of TL across the frequency 24–36 GHz, and (f) phase variation of S_{21} of the cascaded lumped element models of the TLs with $Z_0 = 50\ \Omega$ versus frequency.

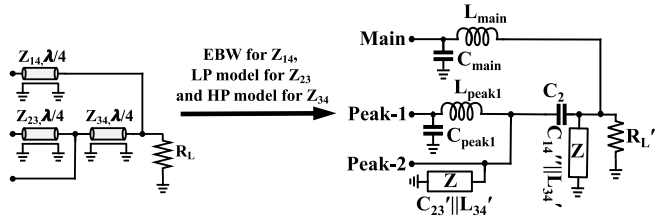


Fig. 10. Version 4 schematics, which uses EBW for Z_{14}, LP for Z_{23}, and HP for Z_{34}.

realized in 40 nm bulk CMOS, as depicted in Fig. 11(b). Fig. 11(c) and (d) reveals that push–pull PAs encounter varied impedances, particularly during PBO, due to unintended coupling among traces within the layout. Furthermore, the final circuit in Fig. 11(a) necessitates extra RF chokes to provide dc voltages to the main, peak-1, and -2 PAs, adding to the circuit's intricacy. These challenges can be addressed by splitting the output balun into three separate baluns and strategically relocating them to the drain terminals of the respective PAs [42].

A. Design Methodology

Fig. 12 outlines the stepwise progression involved in the design of a balun-first three-way Doherty combiner. The balun's turn ratio (NT) is derived using (2), where n signifies the ratio between secondary inductance (L_s) and primary

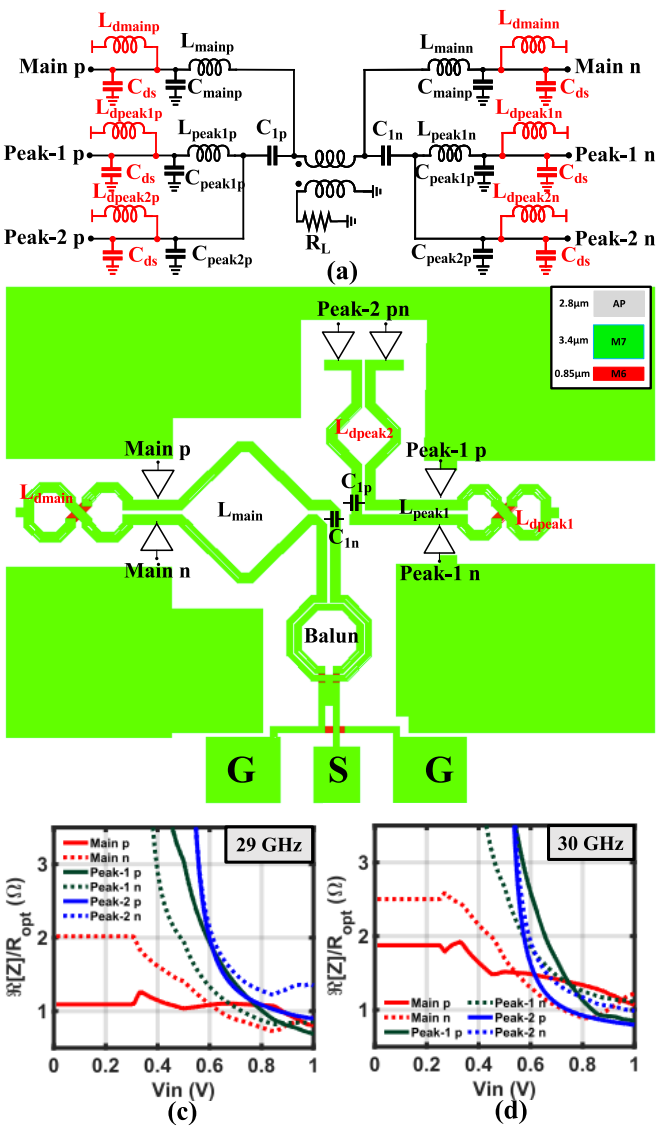


Fig. 11. Version 4 push–pull (a) schematic, (b) layout, and (c) normalized impedance of main, peak-1 and -2 PA versus input voltage (Vin) at 29 GHz, and (d) 30 GHz.

inductance L_p ($n = ((L_s/L_p))^{1/2}$), and k_m represents the balun's coupling factor

$$\mathrm{NT} = n \times k_m. \tag{2}$$

First, L_2 is repositioned to the main path, followed by the relocation of C_m, L_m, and L_2 to the drain side of the main PA through the following equation:

$$L_{k\_m} = L_m \times \mathrm{NT}_m^2 \tag{3}$$

$$L_{m\_m} = L_2 \times \mathrm{NT}_m^2 \tag{4}$$

$$C_m' = \frac{C_m}{\mathrm{NT}_m^2}. \tag{5}$$

The main balun's design parameters (L_{p_m}, L_{s_m}, and $k_{m,m}$) are then computed using (6)–(8) [43]. NT_m can be flexibly chosen, making n equal to 1. Consequently, the primary and secondary inductances can match sizewise, resulting in a single-turn balun. This type exhibits higher self-resonance than

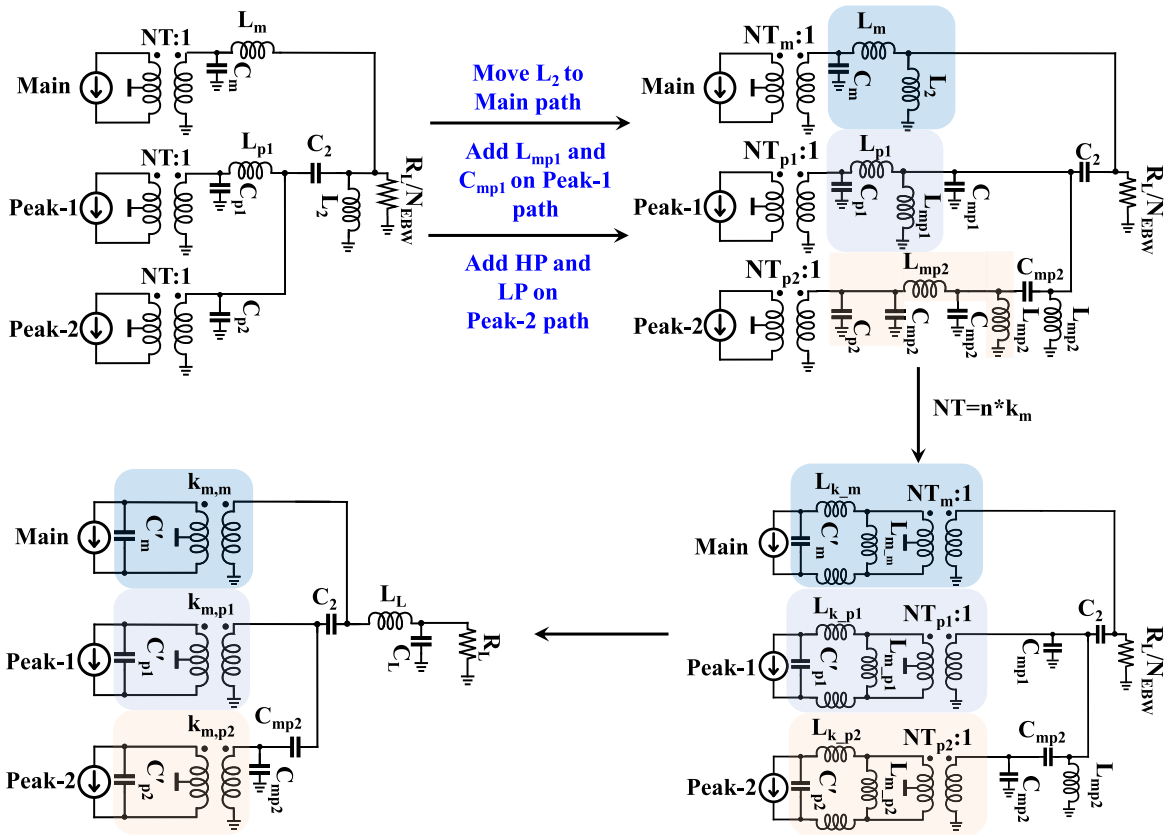


Fig. 12. Procedure to design the proposed balun-first three-way Doherty.

multiturn baluns. NT_m and $k_{m,m}$ within the range of 0.6–0.7 is easier to implement in the layout at mm-wave. Next, practical balun transformers with L_{p_m}, L_{s_m}, and $k_{m,m}$ replace the ideal transformer, magnetizing inductance (L_m), and leakage inductance (L_k) in the main path

$$L_{k\_m} = (1 - k_{m,m}^2) \times L_{s\_m} \tag{6}$$

$$L_{m\_m} = k_{m,m}^2 \times L_{s\_m} \tag{7}$$

$$n \times k_{m,m} = \mathrm{NT}_m. \tag{8}$$

Subsequently, L_{mp1}/C_{mp1} are introduced to the peak-1 path. C_{p1}, L_{p1}, and L_{mp1} are also shifted to the drain side of the peak-1 PA using (3)–(5). The peak-1 balun is fashioned similar to the main balun employing (6)–(8). The LP/HP models of the TL are then incorporated into the peak-2 path. Analogous to the main and peak-1 PA paths, C_{p2}, C_{mp2}, and L_{mp2} can be relocated to the drain side of the peak-2 PA using (3)–(5). The ideal transformer in the peak-2 PA path is replaced with practical balun transformers bearing L_{p_p2}, L_{s_p2}, and $k_{m,p2}$.

Finally, using the following equations, an L-match (L_L and C_L) is harnessed to convert R_L/N_{EBW} to R_L. The L-match proves advantageous by incorporating pad capacitance into C_L, and the trace connecting the Doherty output and pad is utilized for L_L design, thereby minimizing additional component losses in comparison to a C-match (refer to the following equations):

$$\Re\{Z_L'\} = \frac{R_L}{N_{\mathrm{EBW}}} = \frac{R_L}{1 + \omega^2 C_L^2 R_L^2} \tag{9}$$

$$\Im\{Z_L'\} = 0 \implies L_L = \frac{C_L R_L^2}{1 + \omega^2 C_L^2 R_L^2}. \tag{10}$$

The final circuit depicted in Fig. 12 features a compact network, incorporating only one inductor, four capacitors, and three baluns. The baluns' turn ratio (NT), C_{mp1}, and L_{mp2} are design parameters adaptable to achieve optimized values for layout synthesis. In this regard, C_{mp1} and L_{mp2} are selected to resonate at the desired operational frequency (30 GHz). C_m', C_{p1}', and C_{p2}' can be used to absorb the parasitic drain–source capacitance (C_{ds}) of the main, peak-1, and -2 PA.

In summary, with a specified Pout, supply voltage, and load, a balun-first three-way Doherty with bandwidth enhancement can be designed using the equations outlined in Fig. 2(d), coupled with the closed-loop equations above. These equations furnish initial values for the design parameters. Ultimately, the balun-first three-way Doherty configuration is realized within the available technology and optimized through electromagnetic (EM) simulations.

B. Layout and EM Simulation Results

The implementation of the proposed balun-first three-way Doherty layout is carried out using 40 nm CMOS bulk technology, as depicted in Fig. 13(a). This layout comprises three baluns, with coupling factors of 0.7, 0.64, and 0.7 assigned to the main, peak-1, and -2, respectively. The QF of the spiral/slab inductors is increased more than twofold using parallel slot lines of minimum width than utilizing one thick line of the required width, as shown in Fig. 13(a). The rationale

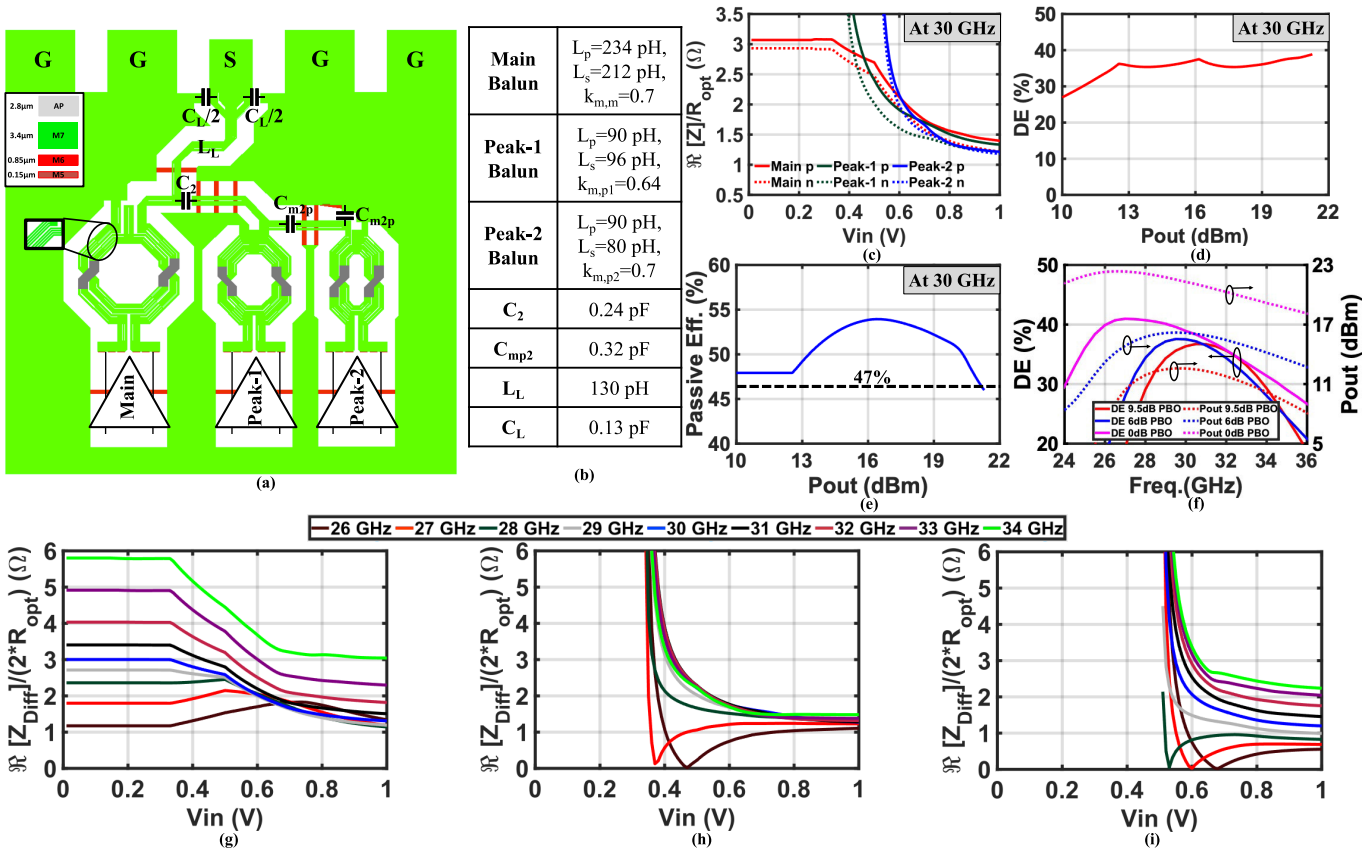


Fig. 13. (a) Layout of the proposed balun first three-way Doherty, (b) components' value, (c) impedance of main, peak-1 and -2 PA versus input voltage (Vin) at 30 GHz which is normalized to R_{opt}, (d) DE versus Pout at 30 GHz, (e) passive efficiency of the proposed balun first three-way Doherty combiner at 30 GHz, and (f) DE and Pout across frequency at 0/6/9.5 dB PBO, (g) impedance of main PA, (h) peak-1 PA, and (i) peak-2 PA versus input voltage (Vin) which is normalized to $2 \times R_{opt}$.

behind this choice lies in the signal's surface travel due to the skin effect, where splitting the lines increases the surface area, thereby reducing resistance and augmenting the QF [44]. This QF enhancement is particularly noticeable in slab and single-turn inductors/baluns, highlighting the preference for single-turn baluns in the proposed output network. Through optimization of component values based on the initial calculations presented in the preceding section, improved performance is achieved, and these updated values are displayed in Fig. 13(b).

All simulation results depicted in Fig. 13(c)–(f) are executed utilizing the EM model of the proposed output network [depicted in Fig. 13(a)] generated using momentum, capacitors possessing a QF of 25, and ideal PA models. In Fig. 13(c), the impedance encountered by the main, peak-1, and -2 push–pull PAs is illustrated when employing the EM model of the proposed balun-first technique, which is normalized to R_{opt}. The mismatch in impedance experienced by the push–pull counterparts remains below 0.5. The relationship between DE and P_{out} exhibited in Fig. 13(d) confirms the desired three-way Doherty operation at 30 GHz. Furthermore, the proposed output network achieves a passive efficiency surpassing 47% at 30 GHz. Ultimately, the proposed three-way Doherty combiner demonstrates a DE exceeding 20%/25%/30% at PBO levels of 9.5/6/0 dB across the 27–34 GHz frequency band [as depicted in Fig. 13(f)]. Fig. 13(g)–(i) shows the normalized impedance of the main, peak-1 and -2 PA versus input voltage across frequency. Z_{Diff} is the differential impedance seen by the main, peak-1 and -2 PA. It is normalized to $2 \times R_{opt}$, where R_{opt} is the single-ended optimum impedance to achieve the required Pout.

V. Circuit Implementation

Fig. 14(a) illustrates a detailed diagram of the proposed PA configuration. The initial component is an input splitter [Fig. 15(a)] consisting of three quadrature hybrid couplers (QHCs). Subsequently, each branch, namely the main, peak-1, and -2 paths, includes an input balun [Fig. 15(b)], predriver (PDRV), interstage matching [Fig. 15(c)], driver (DRV), interstage matching [Fig. 15(d)], and the PA itself.

The arrangement of the input splitter, shown in Fig. 15(a), consists of three transformer-based single-ended QHCs [45] designed to generate phase shifts of 90° and 180°. The unused (port 5) and isolation ports are properly terminated at 50 Ω. The type of resistor used is P+ polyresistor without salicide. The S-parameters and phase response of the main, peak-1, and -2 paths are depicted in Fig. 15(f) and (g), utilizing an EM simulated model of the input splitter. Notably, the input matching (S_{11}) exceeds −16 dB, and the isolation between the main and peak-1/peak-2 paths surpasses −21 dB within the 24–30 GHz frequency range, as indicated in Fig. 15(f).

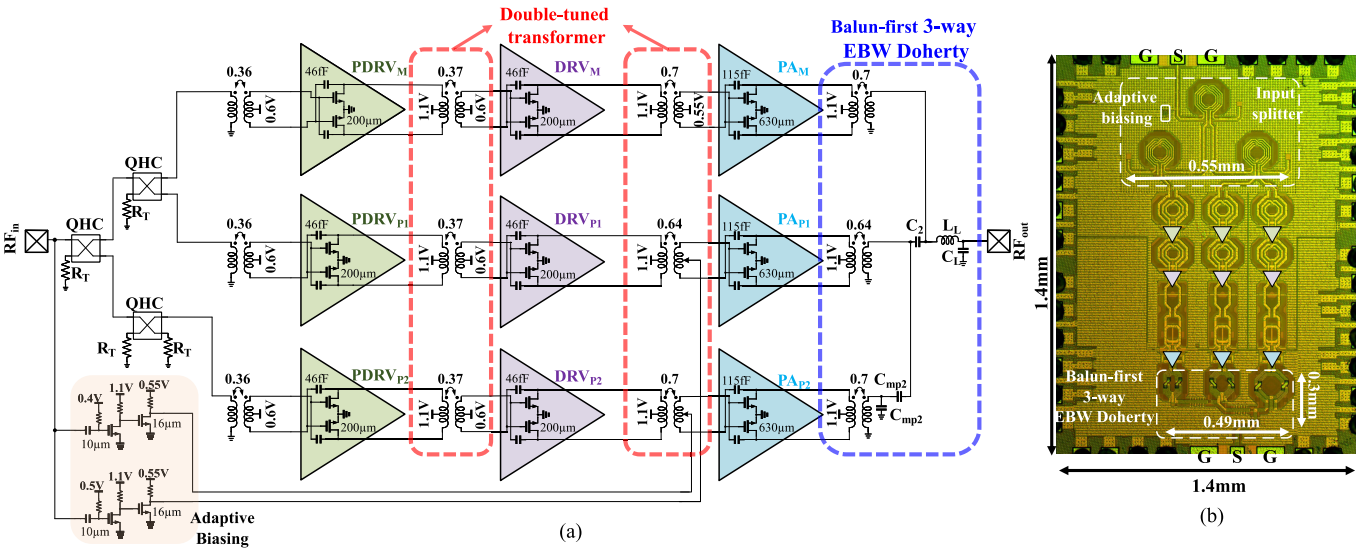


Fig. 14. (a) Top-level and (b) die micrograph of the proposed PA.

The magnitude and phase characteristics of signals in these paths are presented in Fig. 15(f) and (g), with the phase difference remaining below 5° within the specified frequency band. Although using three QHCs improves S_{11} variations and phase differences compared to using two, there is a tradeoff with an increased insertion loss of 1.8 dB [46].

After the input splitter, a balun is utilized to transform the single-ended signal into a differential signal. This balun employs a double-tuned transformer approach [47], [48] to achieve wide-ranging matching, resulting in a passive efficiency of 71% [as shown in Fig. 15(b)]. Alternatively, it is possible to use a balun at the input in combination with a differential input splitter. However, this arrangement necessitates the inclusion of an interstage component for proper matching between the input splitter and PDRV, potentially leading to increased passive losses. In this scenario, the balun serves the dual purpose of converting the signal from single-ended to differential and providing interstage matching. The necessary power gain is achieved by integrating two additional stages, each employing a neutralized common-source transistor with 50 fingers and a width of 1 μm [refer to Fig. 14(a)]. A bias of 0.6 V is applied to PDRVs and DRVs. However, this architectural choice negatively impacts power-added efficiency (PAE). The interstage matching connecting PDRV and DRV utilizes a double-tuned transformer network [47], [48] to achieve wide matching, with its parameter values shown in Fig. 15(c). It provides a passive efficiency of 75%, calculated using the equation from [49].

The PA utilizes common-source transistors and neutralization capacitors set at a bias of 0.55 V. To optimize the cut-off frequency (f_T) and maximize the highest oscillation frequency ($F_{\max}$), the PA design incorporates seven unit cells, each consisting of 50 fingers with a width of 1.8 μm. Fig. 16(a) and (b) illustrates two variations of the unit cell layout within the PA. The second iteration reduces side wall capacitance (C_{sw}) by eliminating metal one ($m1$) and contacts (CO) on both sides of the drain, as shown in Fig. 16(b). Additionally, the metal five ($m5$) trace is made thinner to reduce overlap capacitance (C_{ov}). These modifications collectively minimize the parasitic drain–source capacitance (C_{ds}). Version 2 accomplishes a C_{ds} of 57 fF, marking an enhancement compared to the 69 fF in version 1, while simultaneously improving $F_{\max}$.

The intermediary stage connecting the DRV and PA employs a double-tuned transformer technique to achieve wideband matching. The schematic of this double-tuned transformer is depicted in Fig. 15(e), and the impedance experienced by the DRV (Zd_{DRV}) is computed using (11), as shown at the bottom of the page, [50]. Notably, Cin_{OS} and Rin_{OS} correspond to the input capacitance and resistance of the PA, measured at approximately 250 fF and 6 kΩ, respectively. Additionally, R_{SEC} is the resistance in parallel with the PA, and $\mathrm{Cds}_{\mathrm{DRV}}$ accounts for the parasitic drain–source capacitance of

$$Zd_{\mathrm{DRV}} = \frac{-\omega\left(-\mathrm{Cin}_{OS} R_P T\omega^2 + jT\omega - L_P R_P\right)}{\left(jT R_P \mathrm{Cds}_{\mathrm{DRV}} \mathrm{Cin}_{OS}\omega^4 + \mathrm{Cds}_{\mathrm{DRV}} T\omega^3 + j(\mathrm{Cds}_{\mathrm{DRV}} L_P + \mathrm{Cin}_{OS} L_S) R_P\omega^2 + L_S\omega - jR_p\right)}$$

where,

$$T = -L_P L_S + M^2$$
$$M = k_m\sqrt{L_P L_S}$$
$$R_p = R_{\mathrm{SEC}} \| \mathrm{Rin}_{OS} \tag{11}$$

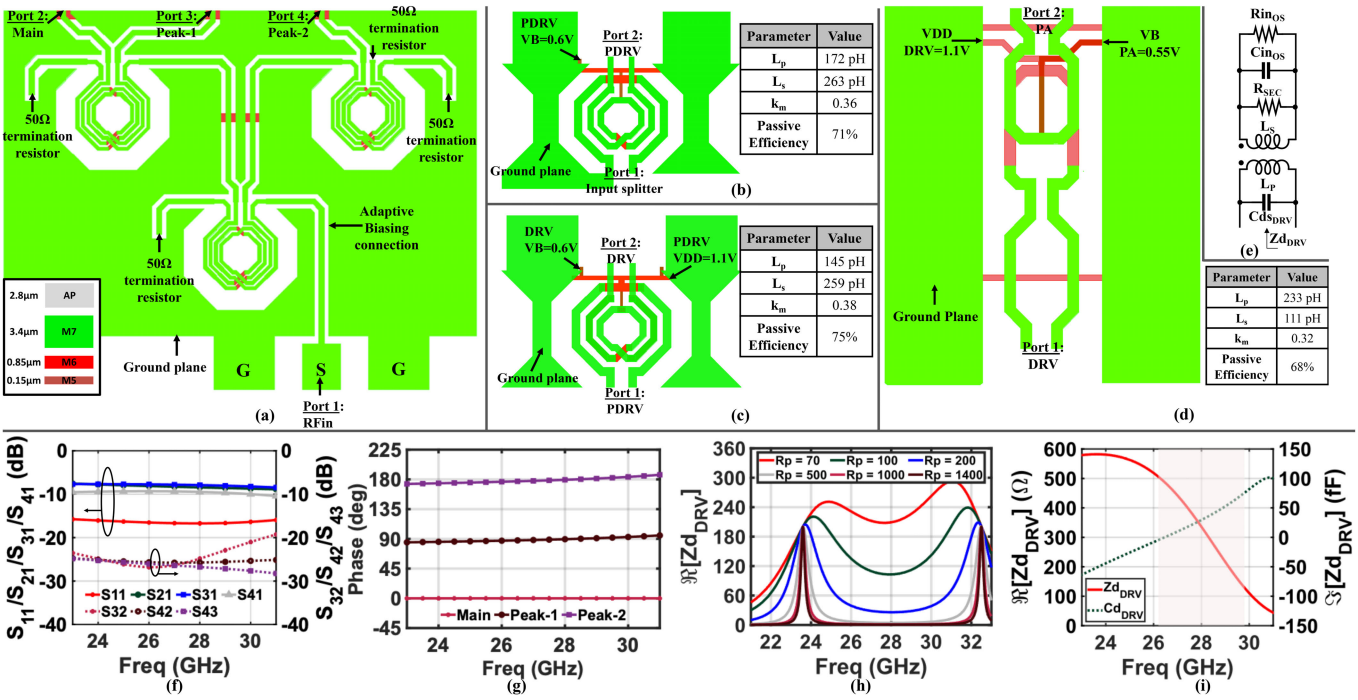


Fig. 15. (a) Layout of the input splitter, (b) input balun, (c) PDRV and DRV interstage matching transformer, (d) DRV and PA interstage matching transformers, (e) schematic of double-tuned interstage between DRV and PA, (f) S-parameters (S_{11}, S_{21}, S_{31}, S_{41}, S_{32}, S_{42}, and S_{43}) across frequency, (g) phase of main, peak-1 and -2 across frequency, (h) impedance plotted using (11) across frequency, and (i) impedance of the EM model across frequency.

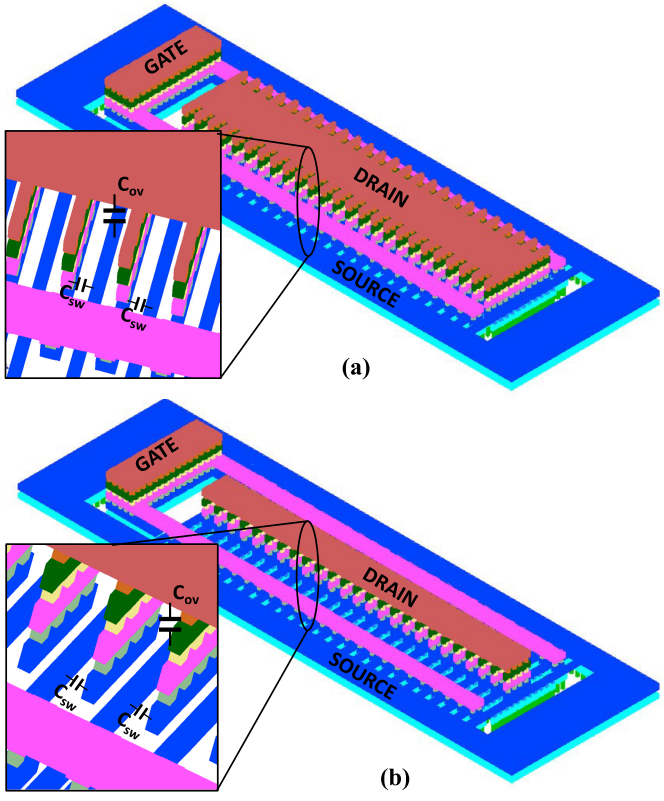


Fig. 16. (a) Version 1 and (b) version 2 of the PA unit cell.

the DRV, respectively. M is the mutual inductance between the primary (L_p) and secondary (L_s) windings.

Fig. 15(h) visually illustrates the real part of impedance across varying frequencies as the parameter R_p changes. Most importantly, higher R_p values result in a dip in the center frequency, thereby compromising the matching. Conversely, lower R_p values lead to a reduced voltage swing at the gate of the PA, preventing the PA from entering saturation. It is worth highlighting that the PA's substantial dimensions contribute to an increased Cin_{OS}, making wideband matching challenging. The layout of the interstage and specific component values are provided in Fig. 15(d). Fig. 15(i) employs the EM model of the interstage to present both the real and imaginary parts of the impedance observed by the DRV. Significantly, the interstage's 3 dB bandwidth is constrained to a mere 3 GHz, limiting the operational bandwidth despite the wideband capabilities of the output network.

An adaptive biasing circuit depicted in Fig. 14 is employed to implement Doherty load modulation. Adapted from [51], this circuit includes an envelope detector with an RF input and a turn-on voltage, placed as shown in Fig. 15(a). The specified turn-on voltage activates the peak PAs, set at 0.5 V and 0.4 V for peak-1 and -2 PAs, respectively. The adaptive biasing circuit offers a 3 dB bandwidth of 2.5 GHz.

VI. Measurement Results

The proposed PA is fabricated in 40 nm bulk CMOS technology [Fig. 14(b)]. The core area of the proposed balun-first three-way Doherty is 1.4×0.55 mm^2. All measurements are performed using a high-frequency probe station. The dc supplies, bias voltages, and turn-on voltage for adaptive biasing are wire-bonded directly to an FR4 printed circuit board (PCB). This work uses the 1.1 V supply voltage for the PAs, DRV, and PDRV amplifiers. Fig. 17(a) and (b) shows the continuous-wave (CW) and modulated measurement

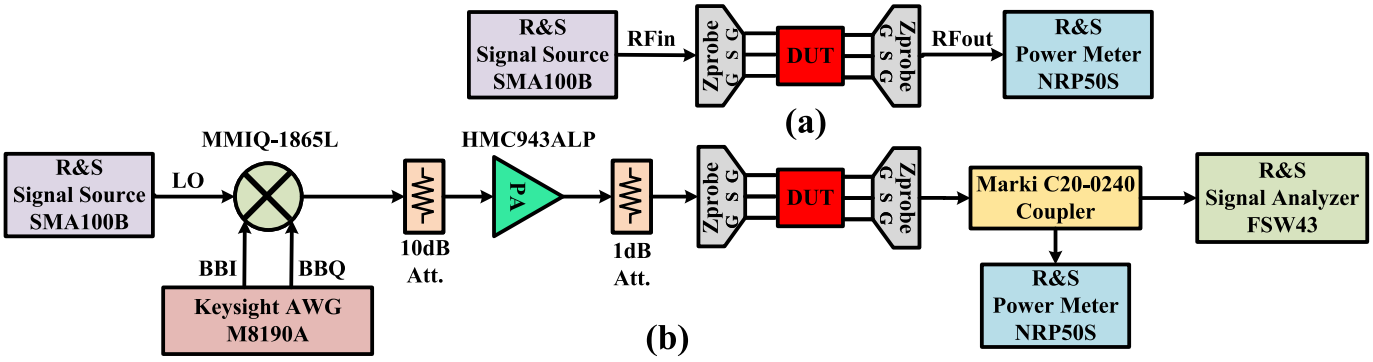


Fig. 17. Simplified (a) continuous-wave and (b) modulation measurement setups.

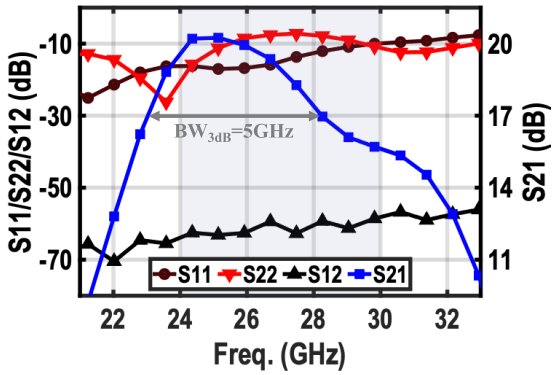


Fig. 18. S-parameter measurement results of the proposed balun-first three-way Doherty PA.

setup. The insertion loss of the probes (Z-probe), cables, and directional couplers are measured and de-embedded.

A. Continuous-Wave Measurement Results

The small-signal S-parameter performance is measured using the Keysight HP8753D vector network analyzer. As Fig. 18 demonstrates, the proposed PA achieves more than 5 GHz small-signal $BW_{3\,\mathrm{dB}}$ where its S_{11}/S_{12} are less than −10/−50 dB over a 24–28 GHz band. At 26 GHz, PA's S_{22} is −8.5 dB, while its input matching is −16.8 dB. The PA offers 19.9 dB small-signal gain at 26 GHz.

The large-signal CW measurement results are reported in Fig. 19 for various operational frequencies. At 25 GHz, $P_{1\,\mathrm{dB}}$ and P_{SAT} are 19.4 and 20.1 dBm, respectively. Its DE at P_{SAT}, 6 dB PBO, and 9.5 dB PBO are 33%, 25%, and 15%, respectively. Likewise, Fig. 19 indicates active load modulation only materializes over the 24–26 GHz band. So, the PBO efficiency enhancement bandwidth is 2 GHz. The efficiency at deep PBO is lower due to the smaller channel resistance of the device and finite QF of C_{ds}, especially of the main PA (refer to the Appendix). Note that the bandwidth is limited due to the high impedance transformation ratio required by the interstage between DRV and PA, as discussed in the earlier section. PAE is degraded since adaptive biasing is applied only to peak PAs and not the DRV and PDRV.

Fig. 20 shows P_{out} and DE across frequency at 12 dB PBO, 9.5 dB PBO, 6 dB PBO, and full power. It can be seen that the proposed PA achieves more than 20 dBm peak Pout and a DE of better than 10%/15%/22%/33% at 12 dB/9.5 dB/6 dB/0 dB across the 24–30 GHz band. The

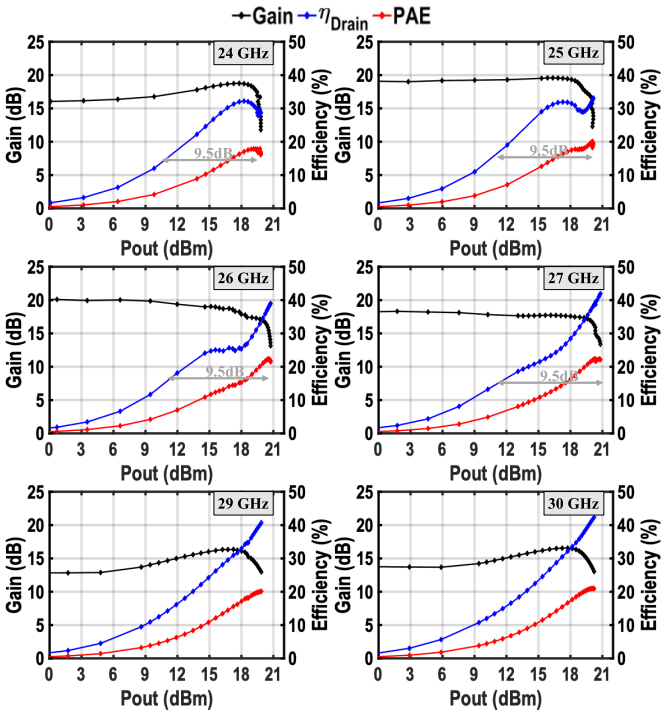


Fig. 19. Measured gain, last-stage DE, and PAE versus Pout at various frequencies.

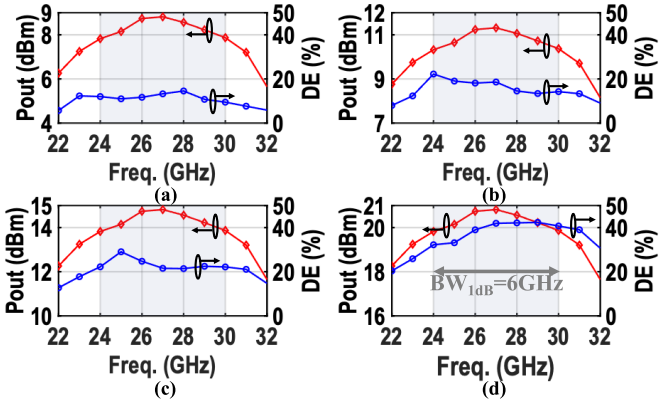


Fig. 20. Pout and DE across frequency at (a) 12 dB PBO, (b) 9.5 dB PBO, (c) 6 dB PBO, and (d) full power.

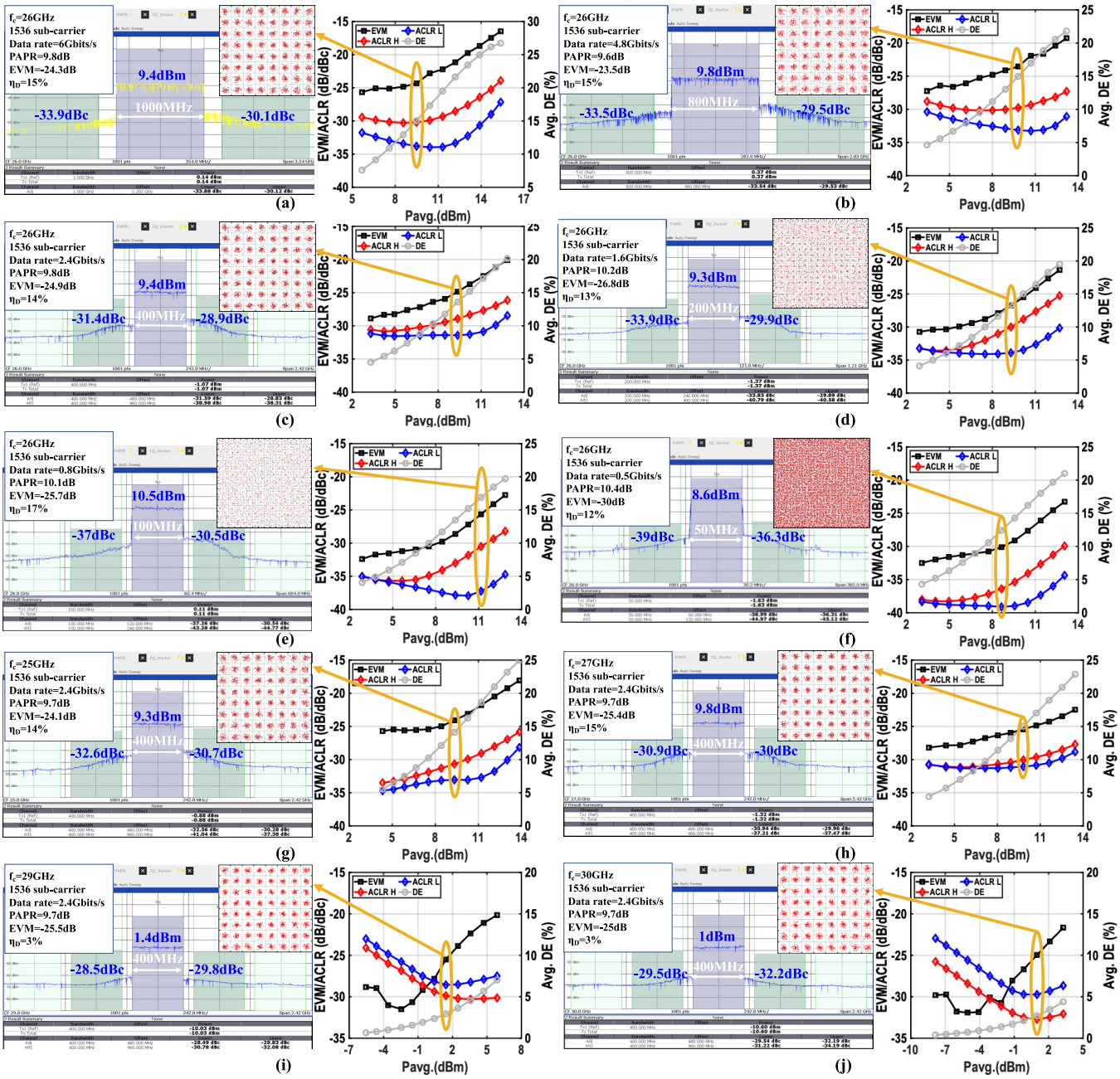


Fig. 21. (a) OFDM 1000 MHz 64-QAM, (b) OFDM 800 MHz 64-QAM, (c) OFDM 400 MHz 64-QAM, (d) OFDM 200 MHz 256-QAM, (e) OFDM 100 MHz 256-QAM, (f) OFDM 50 MHz 1024-QAM at 26 GHz, (g) OFDM 400 MHz 64-QAM at 25 GHz, (h) 27 GHz, (i) 29 GHz, and (j) 30 GHz measurement results.

PA achieves a 1 dB bandwidth of 6 GHz with respect to the P_{sat}.

B. Modulated Signal Measurement Results

The PA dynamic performance is verified by wideband modulated signals such as "64-QAM OFDM," "256-QAM OFDM," and "1024-QAM OFDM" signals. As demonstrated in Fig. 17(b), the baseband I/Q modulated signals are generated with an arbitrary waveform generator (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer (MMIQ-1865L). A directional coupler (Marki C20-0240) is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the Pout.

Fig. 21(a) exhibits 9.4 dBm/15% average Pout/DE measured for a 6 Gb/s OFDM 64-QAM signal at 26 GHz with 9.8 dB PAPR. Its EVM/ACLR are −24.3 dB/−30.1 dBc, respectively. Similarly, the proposed PA achieves 9.8 dBm/15% average Pout/DE for a 4.8 Gb/s OFDM 64-QAM signal with EVM/ACLR of −23.5 dB/−29.5 dBc, respectively [Fig. 21(b)]. For a 1.6 and 0.8 Gb/s OFDM 256-QAM signal with 10.2 dB PAPR, the proposed PA achieves an EVM/ACLR of −26.8 dB/−29.9 dBc and −25.7 dB/−30.5 dBc [Fig. 21(d) and (e)]. The proposed PA is tested with 0.5 Gb/s OFDM 1024-QAM signal and results are shown in Fig. 21(f). Furthermore, the spectral purity and constellation of

TABLE II

PERFORMANCE SUMMARY AND COMPARISON TO DOHERTY mm-WAVE PAs

Specifications	This Work	Z.Ma ISSCC'22 [36]	X.Zhang RFIC'22 [35]	Mortazavi JSSC'22 [34]	Pashaeifar JSSC'22 [33]	Huang ISSCC'21 [30]	Kim RFIC'21 [29]	Mannem JSSC'21 [28]	Wang ISSCC'19 [25]
Architecture	Balun-first 3-way Parallel Doherty PA	3-way Parallel Series Doherty PA	Coupled-inductor based 3-way Doherty PA	Digital polar series 4-way Doherty PA	2-step impedance inversion series Doherty PA	Continuous Coupler Doherty PA	Parallel-series Doherty PA	Role-exchange Doherty PA	Mixed-signal Doherty PA
PA structure	3-stage PAs	2-stage PAs	2-stage PAs	NA	2-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs
Technology	40 nm CMOS	55 nm CMOS	45 nm SOI	40 nm CMOS	40 nm CMOS	45 nm SOI	28 nm CMOS	45 nm SOI	45 nm SOI
Supply (V)	1.1	2.4, 1.2[+]	1.8, 1	2 V, 1 V	1.8, 0.9	2, 1	0.9, 1.8	2, 1	2, 1
Oper. Freq. (GHz)	24-30	28	38	29.5	24-32	26-60	27	26-60	27
PBO Eff. Enh. BW (GHz)	24-26	28	38	29.5	24-28[a]	26-60[b]	27	26-60[b]	27
Core Area (mm^2)	0.77	0.54	1.4	1.1	0.37	0.62	0.16	0.67	0.37
Gain (dB)	20 (26 GHz)	16.1	15	NA	17.4	15.5[*]	16.5	16[*]	19.1
P_{sat} (dBm)	20.7 (26 GHz)	25.5	18.9	18.7	20.4	22	18.8	22.6 (32 GHz)	23.3
DE_{sat}/PAE_{sat} (%)	39/22.3 (26 GHz)	32.5/25.2	31[*]/23.3	36/24	46[*]/38.2	NA/40.5	36[*]/30	46.7/41.9	NA/40.1
DE_{6dB}/PAE_{6dB} (%)	24.7/11.7 (26 GHz)	25.4/20.4	20[*]/17.1	33/15	39[*]/34	NA/32.5	26[*]/22	35.1/31.5	NA/33.1
$DE_{9.5dB}/PAE_{9.5dB}$ (%)	18.1/7 (26 GHz)	21[*]/17	17[*]/ 13.7	26[*]/10[*]	25[*]/20[*]	NA/15[*]	17[*]/12[*]	22[*]/20[*]	NA/20[*]
DE_{12dB}/PAE_{12dB} (%)	11.7/4.2 (26 GHz)	18.2/14.2	15[*]/10[*]	22/10	10[*]/10[*]	NA/10[*]	13[*]/10[*]	15[*]/11[*]	NA/12[*]
Modulation Scheme	64/64/64/256/1024 QAM OFDM (26 GHz)	64 QAM	64 QAM OFDM	64 QAM OFDM	64 QAM OFDM	64 QAM	64 QAM OFDM	64 QAM (28 GHz)	64 QAM
Data rate (Gb/s)	6/4.8/2.4/1.6/0.5	1.5[#]	0.6	1.8	2.4	3	4.8	3	6
Modulation BW (MHz)	1000/800/400/200/50	250	100	300	400	500	800	500	1000
EVM_{rms} (dB)	-24.3/-23.5/-24.9/-26.8/-30	-25.2	-25	-27.58	-24.5	-25	-25	-24	-25.3
ACLR (dBc)	-30.1/-29.5/-28.9/-29.9/-36	-27	-26.5[*]	-27.5	-28.2	-28.8	-25.9	-28.8	-29.6
P_{avg} (dBm)	9.4/9.8/9.4/9.3/8.6	17.7	11.3	7.9	8.8	13.4	11.4	10.7	15.9
PAE_{avg} (%)	15/15/14/13/12 (DE)	17.5	14.7	18	15	24.8	18.1	14.5	29.1 (27.6[++])
DPD	No	No	No	Yes	No	No	No	No	No

[#]limited by equipment. [*]Graphically estimated. [+]Nominal voltage of the technology. [++]Efficiency with digital circuits. [a]6 dB PAE>29 %. [b]6 dB PBO efficiency wrt class B PA>1.

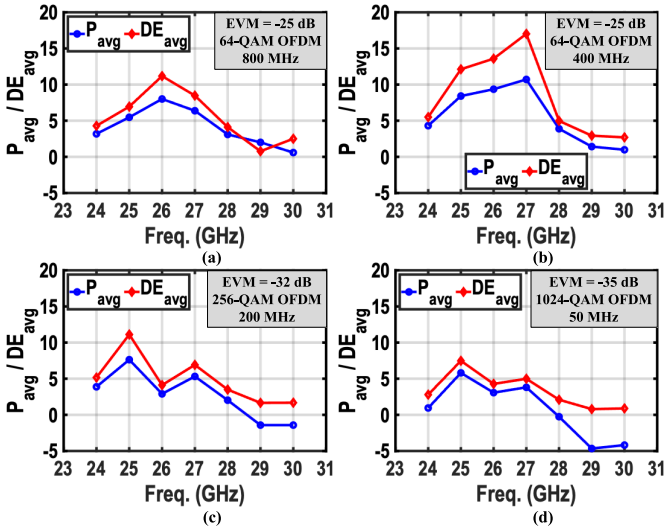


Fig. 22. Average power and DE for (a) OFDM 800 MHz 64-QAM, (b) OFDM 400 MHz 64-QAM, (c) OFDM 200 MHz 256-QAM, and (d) OFDM 50 MHz 1024-QAM across frequency to achieve certain EVM.

a 400 MHz OFDM 64-QAM signal is measured at 26, 25, 27, 29, and 30 GHz with EVM/ACLR of −24.9 dB/−28.9 dBc, −24.1 dB/−30.7 dBc, −25.4 dB/−30 dBc, −25.5 dB/−28.5 dBc, and −25 dB/−29.5 dBc which are illustrated in Fig. 21(c) and (g)–(j).

Fig. 22 illustrates the average P_{out} and DE for an OFDM signal with different bandwidths (800/400/200/50 MHz) and modulation schemes (64/256/1024) within the 24–30 GHz frequency band, aiming to meet specific EVM requirements. To elaborate, considering the minimum EVM requirement for a 64-QAM signal as −21.9 dB (Table I) and providing a 3 dB margin, we present the average P_{out}/DE for an EVM of −25 dB. The proposed PA achieves an average P_{out}/DE performance surpassing 5.5 dBm/7% in the 24–27 GHz band, as shown in Fig. 22(a). Additionally, Fig. 22(b)–(d) exhibits

TABLE III

COMPARISON OF EFFICIENCY TO LINEAR mm-WAVE PAs

Specifications	This Work	F.Wang JSSC'21 [13]	M.Pashaeifar MWCL'22 [14]	W.Zeng ISSCC'23 [15]
Technology	40 nm CMOS	45 nm SOI CMOS	40 nm CMOS	28 nm CMOS
Supply (V)	1.1	2	1	1.8/0.9
Freq. (GHz)	26	28	28	28
Psat (dBm)	20.7	20.4	20.1	20.3
DE_{sat}/PAE_{sat} (%)	39/22.3	50[*]/45	40.6/-	34.7/33.6
DE_{6dB}/PAE_{6dB} (%)	24.7/11.7	26[*]/25[*]	19[*]/-	15[*]/15[*]
$DE_{9.5dB}/PAE_{9.5dB}$ (%)	18.1/7	16[*]/15[*]	11[*]/-	8[*]/8[*]
DE_{12dB}/PAE_{12dB} (%)	11.7/4.2	10[*]/9[*]	7[*]/-	5[*]/5[*]

[*]Graphically estimated.

corresponding results for OFDM signals with bandwidths of 400 MHz, utilizing 64-QAM, 200 MHz with 256-QAM and 50 MHz with 1024-QAM modulation schemes, respectively.

C. Comparison With State-of-the-Art

The performance evaluation of the balun-first three-way Doherty PA is summarized in Table II and compared to that of previous designs. The results highlight that even with a supply voltage as low as 1.1 V, our compact single-supply three-stage mm-wavefront-end achieves reasonable P_{sat} and power gain characteristics. Furthermore, its core area is the second best among three-/four-way Doherty PAs. Across the 24–30 GHz frequency range, the proposed PA delivers relatively high peak Pout, power gain, and efficiency, with respective values exceeding 20 dBm/16 dB/33%. Notably, at 12 dB/9.5 dB/6 dB PBO, the DE maintains superiority over 10%/15%/22% across the same frequency spectrum. The DE primarily drops at 6/9.5 dB PBO due to the lossy C_{ds} of the main PA (see the Appendix) [52]. The lower DE/PAE at the deep PBO is not an inherent limitation of the proposed architecture. Enhancements can be made through improved design choices to reduce C_{ds} of the main PA, such

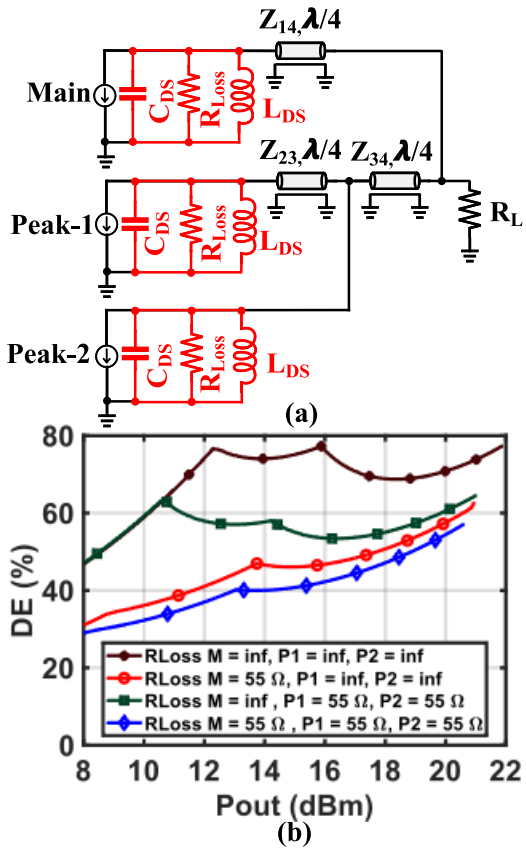


Fig. 23. (a) Proposed three-way parallel Doherty with R_{Loss} and (b) DE versus Pout with R_{loss} = 55 Ω/∞ for the main, peak-1 and -2 PA.

as: 1) utilizing advanced technology to reduce parasitics; 2) employing a higher voltage supply to reduce device size; and 3) implementing asymmetrical three-way Doherty.

It manages complex signals with a data rate of 4.8 Gb/s while demonstrating EVM/ACLR of −23.5 dB/−29.5 dBc, respectively. Notably, these achievements are attained without employing any DPD, which aligns with state-of-the-art standards.

Table III compares class B/AB PAs having a similar peak Pout and frequency of operation with our proposed three-way Doherty design. The table reveals that our proposed three-way Doherty surpasses the other three linear PAs in terms of DE at 9.5 dB PBO. Moreover, at 6-dB PBO compared to [14] and [15], our proposed PA exhibits better performance. However, the PAE is not as competitive compared to other models.

VII. Conclusion

A mm-wave three-way Doherty PA has been implemented that features an EBW to expand its operational bandwidth. A step-by-step design procedure for a balun-first configuration has been thoroughly explained. The proposed PA is fabricated using 40 nm CMOS technology, occupying a core area of 0.77 mm^2. The realized front-end operating at 26 GHz demonstrates a power gain of 20 dB, a peak power of 20.7 dBm, and a DE of 39%/24.7%/18.1% at PBO levels of 0 dB/6 dB/9.5 dB. It attains an EVM and ACLR of −24.9 dB/−28.9 dBc for a 400 MHz 64-OFDM signal with an average Pout of 9.4 dBm and a 14% average DE. For a 100 MHz 256-QAM OFDM signal, the proposed PA achieves EVM/ACLR of −25.7 dB/−30.5 dBc with an average Pout/DE of 10.5 dBm/17%. These results make it a promising choice for adoption in 5G mm-wave TXs.

Appendix

Fig. 23(a) illustrates the proposed three-way Doherty configuration, where C_{ds} represents the drain–source capacitance of the device, and L_{ds} is the inductor used for resonating out the C_{ds}. In practical implementations, the device has a channel resistance and C_{ds} possesses a finite QF. These can be represented by an R_{Loss}, as depicted in Fig. 23(a), although ideally, it should be infinite.

Fig. 23(b) introduces R_{Loss} to all three PAs (main, peak-1, and -2). All other aspects of the simulation are considered ideal. The degradation in DE is less significant when $R_{\text{Loss}} =$ 55 Ω is added to all three PAs (blue curve) compared to when R_{Loss} is added only to the main PA (red curve). This emphasizes the dominant impact of the main PA's R_{Loss} on deep PBO efficiency compared to that of peak-1 and -2 PAs.

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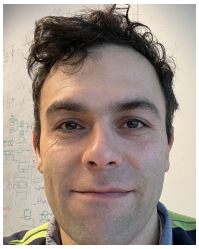

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