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A Reconfigurable Cold-Startup SSHI Rectifier with 4X Lower Input Amplitude Requirement for Piezoelectric Energy Harvesting

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***Abstract*—Synchronized switch harvesting on inductor (SSHI) is an efficient active rectifier to extract energy generated from piezoelectric transducer in piezoelectric energy harvesting system. Unlike passive rectifiers, SSHI rectifiers require a power supply to drive synchronized switches. Unfortunately, there is no stable supply when the system starts from the cold state. Most designs let the system work as a passive full bridge rectifier (FBR) to charge power capacitor until a supply is available. However, a FBR requires high open-circuit voltage (V_{OC}) and the FBR's output voltage cannot go over V_{OC}. This prevents the system from starting the SSHI rectifier if V_{OC} is low. This paper proposes a new transducer reconfiguration design to lower the required V_{OC} by 4× to start up the SSHI system from the cold state. The proposed system is designed in a 0.18-μm BCD process and post-layout simulations show that the successful cold-startup under low V_{OC} voltage.**

***Index Terms*—Cold-startup, energy harvesting, full bridge rectifier, open-circuit voltage, piezoelectric transducer, SSHI rectifier**

I. Introduction

Wireless sensors require batteries to operate, which are typically large in size and limited in lifetime. Extra costs would be introduced due to battery replacements. Piezoelectric energy harvesting (PEH) is a technique to harvest kinetic energy from the environment and generate electricity as an output. This technique is a promising way to untether from conventional batteries and achieve self-powered autonomy. In order to extract AC energy from piezoelectric transducer (PT) and convert it to DC energy, a rectifier is generally required. A Full bridge rectifier (FBR) is a widely used rectifier, but the output power and conversion efficiency of a FBR is relatively low. Some active designs like synchronous electric charge extraction (SECE) [1], [2], and synchronized switch harvesting (SSH) rectifiers [3]–[9] are all exploited to improve the output power extracted from the PT.

FBR results in low power conversion efficiency when PT voltage is flipped from positive to negative or vice versa. A SSHI rectifier helps to flip PT voltage to improve the power extraction with an inductor by forming a RLC oscillation loop. However, all active rectifiers require a stable DC supply (V_{DD}) to operate. In some cases, before V_{DD} is prepared, the interface circuits are out of charge and performed as a passive rectifier to build up the power supply. In [10], [11], high-efficiency SSHI rectifiers were proposed. However, these papers did not give more details realising cold-startup when the open-circuit voltage amplitude (V_{OC}) from the PT is lower than required power supply. The tricky thing is that when V_{OC} is lower than the required V_{DD}, the FBR is unable to build up a ready-use V_{DD} to power the SSHI rectifier; As a result, the SSHI rectifier would not start operating and flipping the voltage, which indicates the cold-start failure.

This paper proposes a new PT configuration design associated with a reconfigurable SSHI rectifier to realize cold-startup when the input V_{OC} is much smaller than the required V_{DD}. The post-layout simulations show that the system can be started from the cold state when V_{OC} is only $0.5\,\mathrm{V}$.

This paper is organised as follows: Analysis of the proposed design is given in Section II. Section III presents the system architecture. Circuit implementations are displayed in Section IV. Post-layout simulation results are shown in Section V to outline the effectiveness of the proposed design. Finally, Section VI summarises the work.

II. Proposed Design Analysis

A. Conventional Cold-Startup

Typically, during the cold state, a SSHI rectifier simply works as a passive FBR. Fig. 1 shows the equivalent circuit diagram during the cold-startup. The PT is modeled as an AC current source, I_P, in paralleled with a capacitor, C_P. A FBR is used to rectify the AC energy. The harvested energy is stored in a storage capacitor, C_S. A LDO is employed to generate a stable supply, V_{DD}, from V_S. When the cold state finishes, the proposed active rectifier would start operating with a stable V_{DD}. For a FBR, the maximum output voltage V_S is limited by V_{OC} and V_D as expressed below

$$V_S(max) = V_{OC} - 2V_D \tag{1}$$

where V_D is the voltage drop of the diode used in a FBR. However, for low excitation when $V_{OC} < V_{DD}$, the maximum output voltage V_S is also lower than V_{DD}. A desired V_{DD} would never be ready; hence, the cold state would not end and the designed active rectifier would not start operating.

B. Proposed Cold-Startup

In the proposed cold-startup circuit, the PT is divided into 4 equal sub-PTs as shown in Fig. 2. Because these sub-PTs

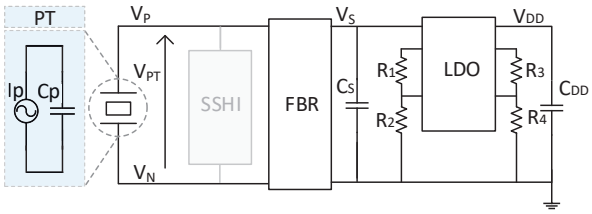


Fig. 1: Conventional cold-startup circuit – FBR

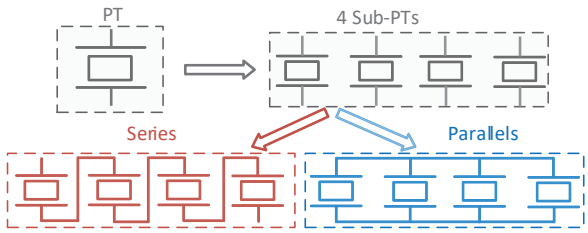


Fig. 2: PTs configurable

are fixed on the same substrate, they have the same frequency and amplitude when vibrating. Therefore, these PTs can be connected in series or parallel which are displayed at the bottom of Fig. 2. The parallel-connected output V_{OC} is the same as that of the monolithic PT; hence, is not able to build up a high V_S to generate a valid V_{DD} under low extraction levels. However, if the 4 sub-PTs are connected in series in cold state, the resulting output $V_{OC-series}$ is expressed as

$$V_{OC-series} = 4 \times V_{OC} \tag{2}$$

The maximum achievable ouput power of the FBR can be rewritten as

$$V_S(max) = V_{OC-series} - 2V_D = 4V_{OC} - 2V_D \tag{3}$$

Since the effective V_{OC} from the series-connected PT is increased by $4\times$, the new maximum output voltage V_S is also increased by approximately $4\times$. Assuming that the V_{OC} is $0.5\,\mathrm{V}$ and V_D is around $50\,\mathrm{mV}$, the series PTs would be able to build up 1.9-V V_S; as a result, up to 1.9-V V_{DD} can also be generated to start active rectification. However, for conventional cold-startup, the V_S can only be charged to $0.4\,\mathrm{V}$ ($= 0.5\,\mathrm{V} - 2 \times 0.05\,\mathrm{V}$), which is too low to start active rectification. Hence, in our proposed design, the 4 sub-PTs are connected in series by default during the cold state to ensure successful cold-startup even at low V_{OC} levels.

C. PTs Connections Selection - After Cold-Startup

When cold-startup ends, it is important to find a suitable connection for these sub-PTs. Output power comparisons between series and parallel configurations are analyzed to find which connection is better for normal active rectification. When the active SSHI rectifier begins to work, according to [12], the extracted power from the SSHI rectifier is written as

$$P_{SSHI} = 2f_P C_P V_S(2V_{OC} - (V_S + 2V_D)\eta_L) \tag{4}$$

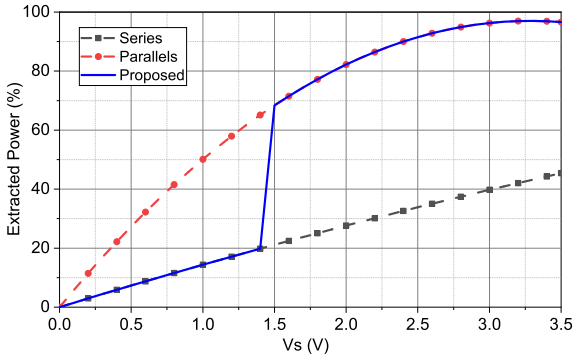


Fig. 3: Extracted power in different PT connections

where $\eta_L = 1 - \eta_F$, η_F is the flip efficiency of the SSHI rectifier and f_P is the vibrating frequency of PT. The above equation shows that when $V_S = \frac{V_{OC}}{\eta_L} - V_D$, the maximum power is written as

$$P_{SSHI}(max) = 2C_P f_P \eta_L (\frac{V_{OC}}{\eta_L} - V_D)^2 \tag{5}$$

The corresponding extracted power simulation results from PT are shown in Fig. 3 with the conditions: V_{OC} = $0.5\,\mathrm{V}$, $\eta_L = 15\%$, $V_D = 50\,\mathrm{mV}$. When the PTs are connected in series, corresponding output efficiency with changing V_S is in grey dash line. It shows that the series-connected power is always lower than the red one representing the parallel connection. However, paralleled output 0.5-V V_{OC} is too low to build up required 1.8-V V_{DD} in cold state. Therefore, 4 sub-PTs are connected in series by default to increase V_{OC} at the beginning to build up V_{DD} during startup period. Then, the connection changes to parallel for extracting more power. Thus, in Fig. 3, the output power follows the grey one until startup ends and changes to red line, so the system output power follows the blue solid line.

III. System Architecture

Fig. 4 shows the system architecture. There are mainly six blocks in this system: a PT array with 4 sub-PTs, a switch control block, a charge-up block, a SSHI rectifier, a FBR and active diode block, a LDO. On the leftmost side, the output amplitude from each of the sub-PTs is $0.5\,\mathrm{V}$. These sub-PTs can be configured between parallel and series connections depending on whether the cold sate is ended. They are connected in series by default during the cold state, so that $4\times$ higher output V_{OC} is generated from the series-connected sub-PTs to build up a 1.8-V V_{DD}.

A FBR and active diode block is used to rectify the generated AC energy. A LDO is employed to regulate V_{DD} through C_{DD1} and C_{DD2} in cold state. When the cold state finishes and V_{DD} is built up, a RDY signal from a LDO generates a rising edge. Then, the switch control block changes the connection of the 4PTs to parallel for the purpose of extracting more power. And the charge-up block connects

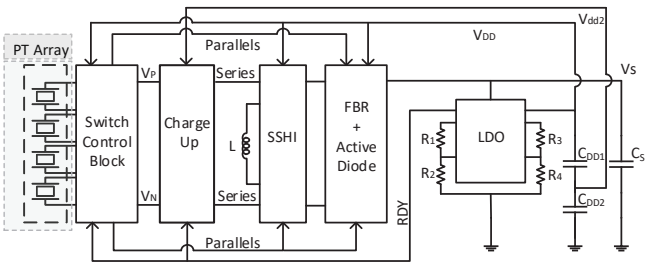


Fig. 4: System block diagram

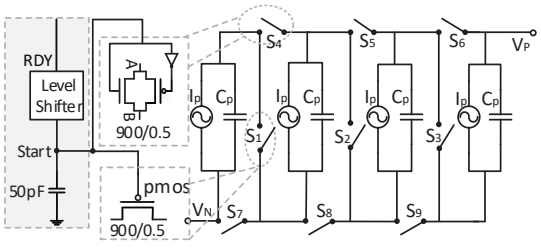


Fig. 5: Switches used in different PTs connections

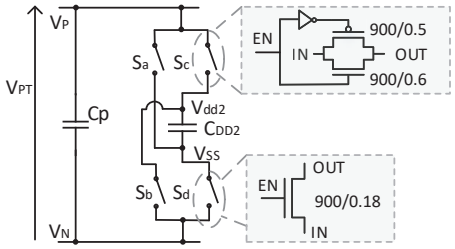


Fig. 6: Charge-up circuit

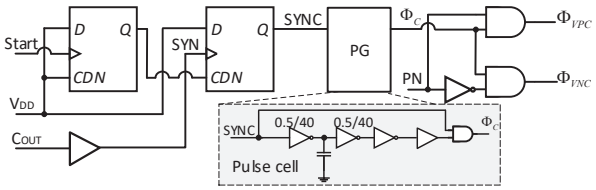


Fig. 7: Charge-up control signals generation

C_{DD2} to V_P or V_N in one flip cycle to help SSHI rectifier to work normally. Finally, a SSHI rectifier is started to increase the output power efficiency with the stable V_{DD} supply by flipping PT voltage. Circuit implementations of key blocks are presented in the following section.

IV. Circuit Implementation

A. Switch Control Block

As introduced in Section III, 4 PTs are connected in series by default to increase V_{OC} during cold-startup period. The switch control block is shown in Fig. 5. S_1, S_2 and S_3 are PMOS switches and S_4 to S_9 are transmission gate (TG) switches. The RDY signal is generated from a LDO. Through a level shifter, a 'Start' signal is generated. The RDY and 'Start' signal keep at low during cold state to turn on PMOS switches and turn off TG switches to keep 4 PTs connected in series. When required V_{DD} is attained, the RDY and 'Start' become high to turn off PMOS switches and turn on TG switches to change the connection to parallel.

However, since power supply is very small and unstable at the beginning, some ripples may exist in 'Start'. Additionally, due to the large width of the connection switches, MOSFET parasitic capacitors always affect the 'Start' signal. These effects prevent firmly turning on/off MOSFET switches, resulting in some current leakage. To address this issue, a on-chip $50\,\mathrm{pF}$ capacitor is added to stabilize the voltage and to eliminate undesired fluctuations in 'Start' signal in Fig. 5.

B. Charge-up Block

When the connection of the PTs changes from series to parallel after the cold-start stage finishes, the SSHI circuit would not work directly, because the PT voltage is decreased by $4\times$ at this moment due to the resulting parallel connection. Additionally, the small resulting V_{OC} ($4\times$ lower compared to series connection) is impossible to charge V_{PT} to overcome the threshold voltage. As a result, the SSHI rectifier would not operate properly, and the system would go back to the cold state gradually since parallel-connected PTs cannot transfer any energy through a passive FBR to a high V_S voltage. Thus, a charge-up block is required to help charge V_{PT} to a certain voltage to help SSHI start. The charge block only works for one flip cycle.

The diagram of the charge up block is shown in Fig. 6; 4 switches are used to charge C_P by connecting it to C_{DD2}. S_b and S_c are TG switches used for charging. S_a and S_d are NMOS switches connected to ground. S_a and S_b are controlled by Φ_{VNC}. S_c and S_d are controlled by Φ_{VPC}. These two phases are generated by the circuit shown in Fig. 7. The 'Start' signal is the same as in Fig. 5. The C_{OUT} is a synchronized signal indicating the moment when the voltage across the PT starts flipping which will be presented in the following sub-section. Through a buffer, the SYN signal is generated. When the SYN generates a rising edge, pulse generation block generates a pulse, Φ_C. The PN indicates the current polarity of V_P and V_N to determine the charging direction.

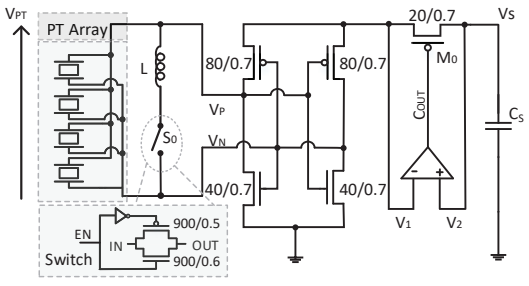


Fig. 8: SSHI rectifier

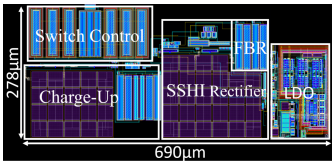
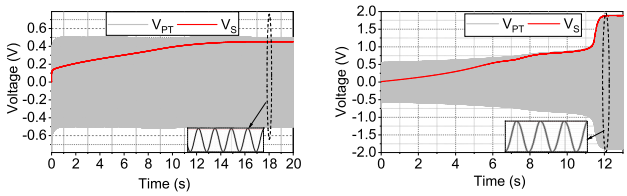


Fig. 9: Proposed layout diagram



(a) Conventional cold-startup (b) Proposed cold-startup

Fig. 10: Comparison of conventional and proposed cold-startup

C. SSHI Rectifier Block

When the charge-up finishes, the PT voltage is flipped to a certain voltage. And through automatically charging by the generated energy, the PT voltage would be high enough to overcome the threshold to charge C_S. In the next flip cycle, the SSHI rectifier begins to work. A SSHI rectifier is presented in Fig. 9. When $V_1 < V_2$, the output C_{OUT} of the comparator generates a rising edge and M_0 is turned off to prevent the current going out of C_S. This rising edge means the ending time of charging and the starting time to flip V_{PT}. So, it is also employed to generate a pulse to control S_0. The SSHI rectifier employs an inductor temporarily connected into a RLC loop by turning on S_0 to flip V_{PT} to improve output power.

V. Post-Layout Simulation Analysis

This system is designed in a 0.18-μm BCD process with the parameters: $V_{OC} = 0.5\,\text{V}$, $C_P = 30\,\text{nF}$, $f_P = 200\,\text{Hz}$, $C_S = 2\,\mu\text{F}$, required $V_{DD} = 1.8\,\text{V}$. A monolithic PT is divided into 4 equal sub-PTs. Fig. 8 displays the layout of the system and the active area is $0.19\,\text{mm}^2$. The corresponding post-layout simulation results are presented as follows. Fig. 10, shows the simulation results of the conventional cold-startup design and the proposed cold-startup design. For the conventional cold-startup circuit, when the input V_{OC} is $0.5\,\text{V}$, the maximum grey V_{PT} is bounded by $0.5\,\text{V}$ while the maximum output red voltage V_S is $0.4\,\text{V}$ in Fig. $10(a)$. $0.4\,\text{V}$ is impossible to build up 1.8-V V_{DD}. In comparison, Fig. $10(b)$ shows the proposed cold-startup simulation result, where the maximum grey V_{PT} is close to $1.9\,\text{V}$. The resulting maximum red V_S is also very close to $1.9\,\text{V}$ which is high enough to build 1.8-V V_{DD}.

Some key signals in the proposed design are shown in Fig. 11. The V_S voltage, is simulated to be charged from $0\,\text{V}$ to $3.5\,\text{V}$. The voltage V_{DD}, is gradually built up to $1.8\,\text{V}$. During startup period, the red 'Start' signal is hold at low to turn on PMOS switches and turn off TG switches in Fig. 5 to keep PTs connect in series. When V_{DD} attains $1.8\,\text{V}$, the cold state is finished and the RDY signal generates a rising edge. At the same time, the 'Start' turns to the high level to follow the V_S to make the PTs connected in parallel by turning off PMOS switches and turning on TG switches.

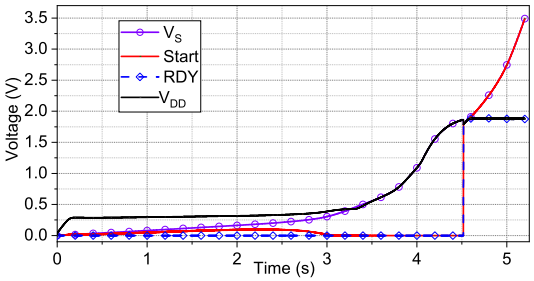


Fig. 11: Output signals of proposed design

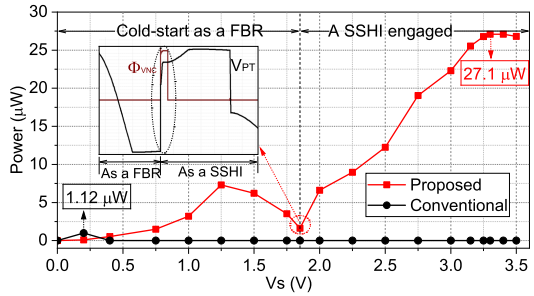


Fig. 12: Output power of proposed design and FBR

Fig. 12 shows the simulated output power related to V_S. Before V_S attains $1.8\,\text{V}$, the system works as a passive FBR and then works as a SSHI rectifier after startup. The maximum output power of the conventional design is $1.12\,\mu\text{W}$, and the corresponding output V_S is limited by $0.4\,\text{V}$. The red line is the output power of the proposed design. When V_S attains $1.8\,\text{V}$ to provide stable 1.8-V V_{DD}, the PTs connection is configured to parallel and the charge-up block generates a phase, Φ_{VNC}, to flip V_{PT} from negative to positive. After the SSHI rectifier starts operating, the output power is significantly increased and V_S can be charged to higher voltage. As a result, the output power becomes higher and attains $27.1\,\mu\text{W}$ when $V_S = 3.3\,\text{V}$.

VI. Conclusion

This paper proposes a cold-startup circuit for 0.5-V V_{OC}. The 4 series-connected sub-PTs are used to generate a $4\times$ V_{OC} to build up V_{DD} and change to parallel for the purpose of extracting more power. A LDO is used to generate 1.8-V V_{DD}. A charge-up block is used to help V_{PT} overcome the threshold voltage after cold-startup. A SSHI rectifier is used to improve the output power efficiency by flipping V_{PT}. Corresponding post-layout simulation results show that 1.8-V V_{DD} can be built up even with 0.5-V V_{OC}. The simulated maximum output power is $27.1\,\mu\text{W}$ which is $24\times$ larger than the maximum output power of the FBR.

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