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# TOWARDS A SCALABLE SUN POSITION SENSOR WITH MONOLITHIC INTEGRATION OF THE 3D OPTICS FOR MINIATURIZED SATELLITE ATTITUDE CONTROL

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## ABSTRACT

In this paper we present a sun position sensor platform with a scalable approach for the 3D integration of the sensor optics. This would facilitate the sun position sensor miniaturization, reduces fabrication cost and mitigates the need for sensor calibration. The sun position sensor platform is implemented in a seven mask BICMOS technology with optical windows between the light masking layer and CMOS image sensor implemented by adhesively bonded glass windows. The CMOS sensor functionality is experimentally verified by modulation of a light spot using a laser. The proposed approach enables wafer-scale fabrication of the 3D optics that includes the wafer stepper accurate overlay alignment of the apertures. This mitigates the need for cumbersome alignment of the apertures at die or package level and facilitates further miniaturization, accuracy and sensor cost.

## KEYWORDS

3D integrated optics; sun position sensor; CMOS image sensor; adhesive bonding.

## INTRODUCTION

Sun position sensors are vital attitude sensors that allow for determination of the direction vector towards the sun, which is commonly used in satellite attitude control. The amount of satellites and their application in orbit and outer space is ever increasing and developing. It is essential to follow these development with the vital components, such as the sun position sensor, to tailor suitable and compatible devices for future missions.

Similarly to the semiconductor industry, the trend for satellites is miniaturization [1]. Smaller and simpler satellites are favored for an increasing amount of applications as they are cheaper more versatile and can operate in robust constellations. A popular format is the CubeSat [2], whose size is comparable to a carton of milk. To facilitate this trend from the perspective of the sun position sensor, this sensor dimensions, weight and fabrication cost need to decrease.

The current fabrication approach is to integrate the aperture discretely in the sensor housing, which demands larger devices, an elaborate and expensive fabrication step and calibration of each device. In order to decrease the sensor size and cost, we propose a scalable approach for complete fabrication of the sensor and the 3D integrated optics on wafer level using advanced packaging techniques. Optical windows are aligned on the individual chips by use of a selective and aligned placement technique followed by adhesively bonding to the CMOS device wafer, on top of which the light masking layer is then implemented. Using the accurate lithography alignment for the aperture definition in future implementations, the need for sensor calibration due to misalignment of the aperture and image sensor is mitigated.

This work incorporates a sun position sensor testing platform in a seven mask 1 µm BICMOS technology. Here, the optical window is of glass and is adhesively bonded using spin coated SU-8, which is a standard MEMS capping technology. The SU-8 can be patterned using lithography, to selectively place glue outlines around the CMOS image sensor. This cost-effective platform enables rapid prototyping using different optical window geometries and materials.

## EXPERIMENTAL

### Sun Position Sensor Architecture

Various different sun position sensor sensors exist, which can be classified in the collimating, sun-pointing, tilted-mount and hybrid types [3]. The collimating sun position sensor type is typically implemented using stacked layers on which planar fabrication technologies implement the photodetectors and light masking layer. This is more compatible with microfabrication technologies than the other types and is therefore considered in this work.

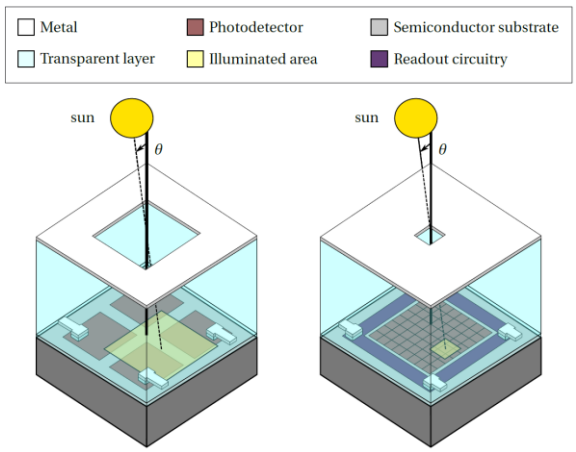


*Figure 1: Schematic illustration of the collimating sun position sensor architectures present in the platform design, including the quadrant sun sensor (left) [4-5] and pixel array sun sensor (right) [6].*

The operating principles of the two collimating position sensor architectures are illustrated in Figure 1. The quadrant sun sensor compares generated photocurrents of four photodetectors, to extract information on the direction

vector towards the sun. The pixel array sun sensor uses the array to pinpoint a much smaller light spot, which uses the outputs in a centroid algorithm to determine the direction vector of the sun. To reduce off-chip connections, the digital centroid sun sensor incorporates readout circuitry for selective pixel readout. Both architectures benefit from on-chip signal conditioning.

**The BICMOS7 Technology**

The seven core fabrication steps of the BICMOS7 technology [7-8] are schematically illustrated in Figure 2. The front-end-of-line (FEOL) fabrication entails the doped regions implementation and consists of the n-well (NW, $P^+$) in a p-type substrate, shallow n-type (SN, As+) and shallow p-type (SP, $B^+$) steps. The FEOL ends with 100 nm thermally grown silicon dioxide ($SiO_2$), used for the gate dielectric and field oxide.

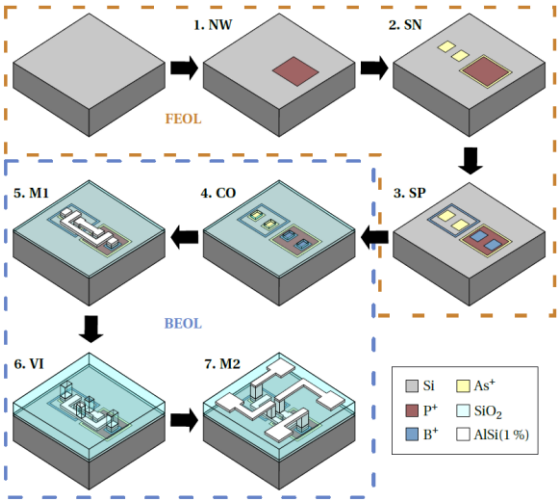


*Figure 2: Schematic illustration of the fabrication of a CMOS inverter in the BICMOS7 technology [7-8]. The starting material is a p-type four inch silicon wafer with a highly uniform dopant concentration determined by an epi-layer. The FEOL includes the NW, SN and SP steps and the BEOL includes the CO, M1, V1 and M2 steps. Each of the steps requires a lithography mask.*

The back-end-of-line (BEOL) starts with formation of contact openings (CO) to the doped regions, followed by the 1st metal interconnect layer (M1) in Al(1%Si). Subsequently tetraethyl orthosilicate (TEOS) plasma-enhanced chemical vapor deposition is used to form another $SiO_2$ layer. Via openings (VI) are etched and the fabrication is finalized by the second metal interconnect layer (M2) in Al(1%Si).

**Radiometry Considerations**

The sensor response time depends on the stored electric charge decrease rate through generated photocurrent. The photodetector photocurrent generation is calculated by the multiplication of the photodetector responsivity $R(\lambda)$ and incident optical power $P(\lambda)$ spectra, as depicted in Figure 3.

Since the spectra are only available for discrete wavelengths, the generated photocurrent can be estimated through a uniform midpoint Riemann sum, given by

$$I_0 \approx A_{tot} \sum_{i=1}^{N} T_{add}(\lambda_i^*) P_{opt}(\lambda_i^*) R(\lambda_i^*) \Delta\lambda. \quad (1)$$

The transparent window transmission $T_{add}(\lambda)$ is neglected, as it is >90% in the visual range [9]. The designed photodetector area in each pixel is ~0.25mm$^2$, resulting in <40μA generation.

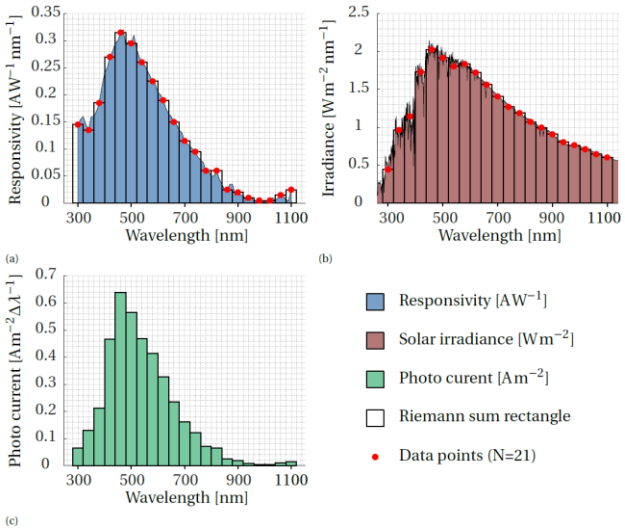


*Figure 3: Spectra used for photocurrent generation estimation, with (a) the responsivity $R(\lambda)$ of a reported VIS photodetector in the BICMOS7 technology [10], (b) the solar irradiance $P_{opt}(\lambda)$ data [11] in the same range and (c) the multiplication result $P_{opt}(\lambda)R(\lambda)$ that gives the photocurrent. The uniform midpoint Riemann sum (N=21) is depicted in each plot.*

**Functional Design**

The functional design of the 8x8 pixel array sensor is depicted in Figure 4. The sensor is implemented by three-transistor active pixel sensors (3T APS), which store electric charge after a reset pulse. The stored charge leaks away when photocurrent is generated in the pixel photodetector, allowing differentiation between illuminated and dark pixels.

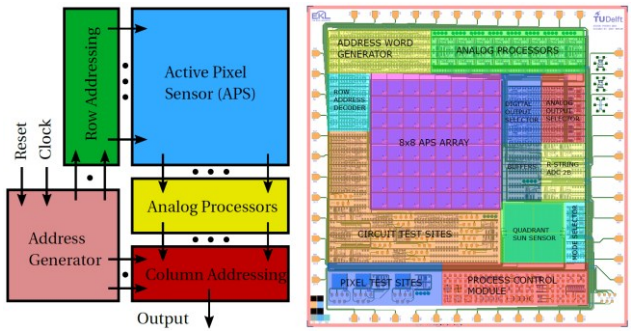


*Figure 4: Functional design overview of the 8x8 pixel array with readout circuitry block diagram (left) and highlighted functional blocks in the layout hardware design of the 10x10mm chip (right).*

To address an individual pixel, a unique address word is generated in the *address word generator*. Half of this

word is used to decode the pixel row in the *row address decoder* and the other half to decode the pixel column in the *digital/analog output selector*. Each column in the array is connected to an *analog processor*, which conditions the raw pixel output. The other annotated functional blocks are not discussed in this work, but allow for process control and the testing of individual design layers, circuit blocks or intermediate signals.

Using a clock signal, the sensor cycles through all its 3T APS pixels and serially communicates each pixel output off-chip. For the 8x8 pixel array this results in a sensor output of 64 bits (8 bytes). The pixel array readout principle is not limited to the current array size and is therefore scalable in potential future implementations in effort to increase the sensor accuracy. The four inch device wafer and single die after fabrication are depicted in Figure 5.

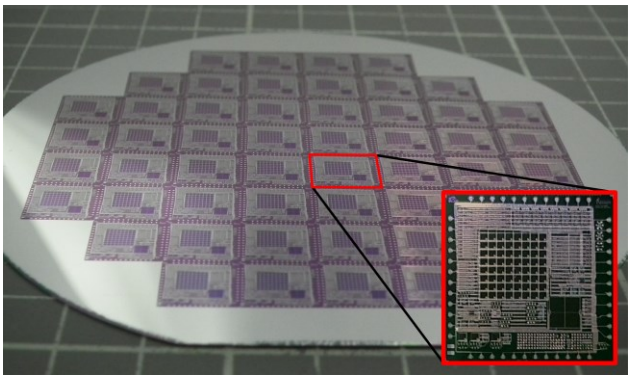

*Figure 5: BICMOS7 four inch device wafer, containing 52 identical 10x10mm dies. The picture inset shows a single die photograph, depicting the layout design from Figure 4.*

## RESULTS AND DISCUSSION

### Transparent Spacer Integration

The transparent spacer integration is implemented by adhesive bonding of 8x8mm glass windows to the CMOS device chips before conventional packaging. This bonding technique is favored over direct bonding or anodic bonding, as these techniques are considered not compatible with CMOS device wafers [12]. The final result of the packaged chip is depicted in Figure 7.

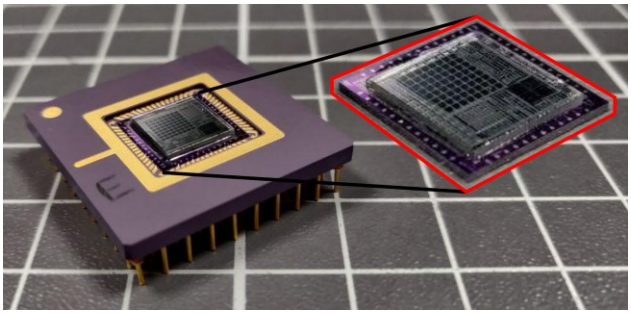

Figure 7: Packaged device after adhesive bonding of the transparent spacer. The inset shows the bare chip after adhesive bonding and before packaging.

### Circuit Characterization

To verify correct operation of the integrated system, the functional blocks are probed individually. Measurement results of the *address word generator* and *row address decoder* are given in Figure 6 and show correct operation of these blocks. The *address word generator* is a 6-bit counter with LSB *Q0* and MSB *Q5* that counts on clock rising edges. The *row address decoder* cycles through the 8 rows in the pixel array. During row selection, 8 counts pass to cycle through the 8 columns in the pixel array. For this reason, the *row address decoder* is only connected to *Q3-5*. The circuits are measured on wafer-scale (~37% yield) and after bonding of the transparent spacer without any observable difference.

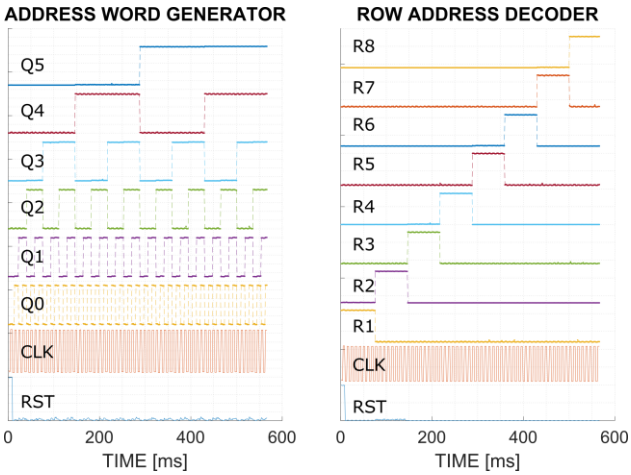


*Figure 6: Measurement results of the address word generator and row address decoder circuits. The address word (Q0-Q5) and row selection signals (R1-8) are probed to verify correct operation. The global clock (CLK) and reset (RST) input signals are also probed and included.*

### Light Spot Emulation

A microscope with a 633 nm laser source was used to emulate a light spot before aperture integration. The interfacing circuitry includes input and output level-shifters and is powered by an Arduino MEGA, connected to a laptop to control the measurements.

The light spot cast on the pixel array through an aperture is emulated by illuminating single pixels through the integrated optical transparent window. The measurement results of the illumination of a single pixel are listed in Figure 8. The laser illuminates the pixel in row two and column four. The raw sensor output is low for a single clock cycle and corresponds to a single pixel, according to the conditioned pixel response. Visualizing the array image clearly shows the illuminated pixel.

### Technology Outlook

The demonstrated approach for the integrated 3D optics of a sun position sensor enable a wafer-scale technology. Such a wafer-scale technology could be implemented using a pick-and-place tool or an accurate holder to position the optical windows on the device wafer. The patternable SU-8 adhesive is compatible with CMOS and MEMS fabrication and allows selective bonding areas to avoid interference with sensors or circuits. The technology is not limited to fixed optical window geometries or materials, enabling a versatile approach to tailor the 3D optics to the sensor requirements.

Future additions to the technology are required, to create light masking layers, filters or even sensors on top of the optical window. This benefits the optical sensors greatly and allows fabrication on wafer-scale.

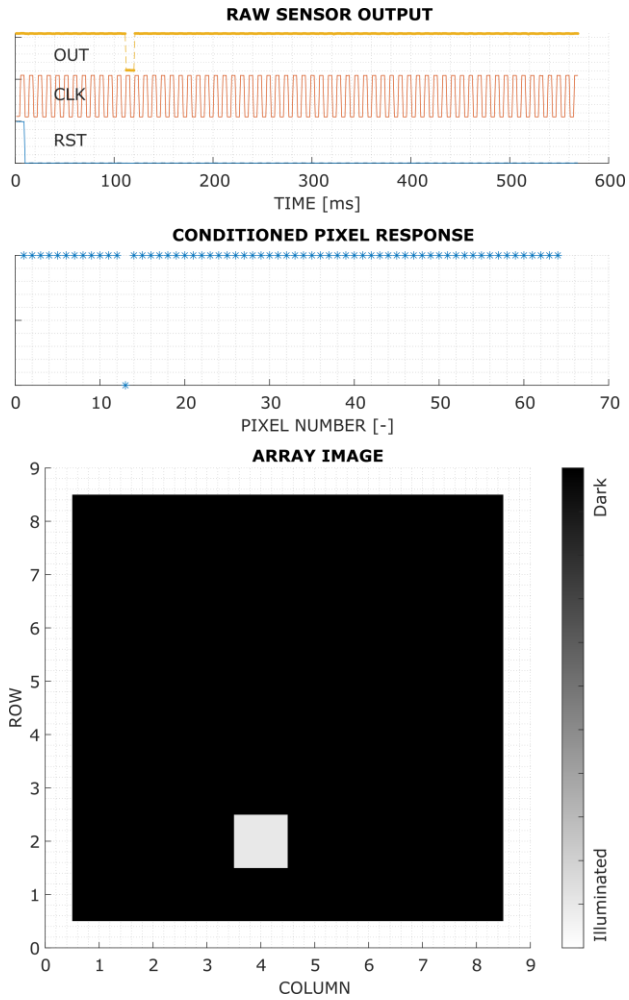


*Figure 8: Measurement results of single pixel illumination. The raw sensor output (OUT) is oversampled to probe the output stability, the conditioned pixel response is the result of averaging all measured points during the clock cycle and the visualized array image shows which pixels are illuminated and which are dark.*

## CONCLUSIONS

A scalable fabrication approach for the 3D optics of a sun position sensor was demonstrated. This technology enables implementations that allow further miniaturization and cost reduction of the devices, to facilitate the trend of satellite miniaturization. Selective adhesive bonding using SU-8 was used to bond the optical windows to the CMOS sensor substrates, which is compatible with CMOS and MEMS fabrication technologies.

The test platform includes an 8x8 active pixel array with integrated CMOS electronics in a facile in-house fabrication technology. The sensor operates as intended and no performance difference is observed before and after the adhesive bonding of an optical window on top of the sensor. The test platform is scalable, such that larger arrays can be implemented by following the same operating principle.

Future work should focus on the inclusion of the placement of the optical windows on wafer-level and the addition of layers on top of the optical window. This enables a versatile technology for sun position sensors that is compatible with wafer-scale fabrication and does not need sensor calibration due to the accurate overlay alignment in stepper lithography.

## ACKNOWLEDGEMENT

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