Live Transitioning of two Series-Parallel-Output Dual Active Bridge Converters

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by

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Koen Linders
Den Haag, July 2023

Abstract

The transportation sector is moving towards a green future with a rapidly growing EV market and consequently, the demand for EV chargers is rising too. With the increased interest in 800V batteries and the current presence of 400V and 600V batteries, the voltage range for EV chargers is wide (150V-1000V). In this thesis, a wide-output EV charger based on two DAB converters with series-parallel output is proposed. A novel method of reconfiguration is introduced to allow live transitioning between series and parallel mode. The circuit of a 25kW is optimized to achieve optimal efficiency during a charging cycle. A comparison between advanced DAB modulation strategies is made and Triple Phase Shift (TPS) modulation in combination with Minimum Current Stress Optimization (MCSO) improves the efficiency of the DAB at low voltage and low power operation. The converter operates at >97.6% efficiency in the full range of 150V-1000V with a peak efficiency of 98.8%. A 25kW converter is modeled and simulated in PLECS, and a 200W hardware prototype is built to verify the new method for live transitioning.

Samenvatting

Met de snelle groei aan elektrische auto's is de transport sector onderweg naar een groenere toekomst. Door de groei aan elektrische auto's groeit de vraag naar laders mee. Het spanningsbereik van deze laders wordt aldoor groter doordat EV batterijen op verschillende spanningen werken, waaronder 400V, 600V en 800V. In dit rapport wordt een lader ontworpen voor een brede uitgangsspanning van 150V-1000V. De lader bestaat uit twee Dual Active Bridge (DAB) omzetters met een serie-parallel uitgang. Een nieuwe methode is ontwikkeld om vloeiend over te schakelen van serie naar parallel zonder vermindering van de uitgangsstroom. Het ontwerp van een 25kW lader is geoptimaliseerd voor optimale efficiëntie tijdens het laden. Verschillende modulatie technieken voor de DAB zijn vergeleken en Triple Phase Shift (TPS) met Minimum Current Stress Optimization (MCSO) bleek het meest efficiënt. De geoptimaliseerde 25kW omzetter heeft een piek efficiëntie van 98.8% en een efficiëntie van >97.6% in het gehele spanningsbereik van 150V-1000V. Een 200W prototype is gebouwd om de theorie van het overschakelen te testen. Het ontwerp van de 25kW lader is gesimuleerd in PLECS en Matlab.

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Introduction

The market for electric cars is growing at a high pace and lately, the interest in 800V battery technology is growing too. By increasing the conventional 400V battery voltage to 600V or 800V, both the system efficiency and charging rate can be increased [1], [2]. Until now, several high-end cars and trucks have been equipped with 800V batteries while electric buses are charged with 600V. Prospects are that 800V batteries will be available in mass-market EVs around 2025 when the technology becomes inexpensive enough [2]. With 400V, 600V, and 800V EVs entering the market, the need for chargers that are capable of supplying a wide output voltage range will increase.

This project will be part of the FlexiNet Project at the Delft University of Technology. The FlexiNet project aims at reducing the reliance on energy import for households and increasing the flexibility of electricity supplies by creating an intelligent and integrated system for hybrid energy storage (Flexinet Project). Within the FlexiNet Project, a hybrid storage solution will be designed. Part of this storage solution is the temporary storage of energy in Electric Vehicles (EVs) using chargers featuring bidirectional Vehicle to Grid (V2G) capabilities. This thesis will tie into the FlexiNet project by exploring a future-proof Bidirectional charger for 400V, 600V, and 800V EVs.

Only a few EV chargers with wide output voltage (150V-1000V) have been reported in recent research. In Figure 1.1, a selection of converters with wide output voltages is shown. Three converters stand out in their output capabilities; [3], [4], [5], [9], and [14]. The authors make use of a reconfigurable output, each with a different converter topology like LLC[3], [4] or Phase Shifted Full Bridge (PSFB)[9]. The presented converters all have the same drawback. They can not transition from series to parallel while charging. The converters all transition between series and parallel before the power transfer starts. When the converters can not transition between series and parallel during charging, they are potentially operating in a suboptimal configuration for a part of the charging cycle. When a transition is needed, the converters need to reduce the output current to change from series to parallel. To operate the converter in the most efficient configuration 100% of the time, a transition between series and parallel under live power flow is necessary.

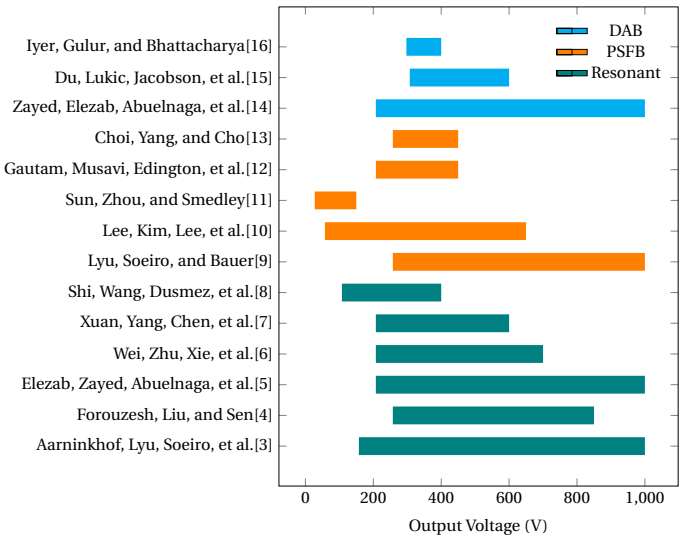


Figure 1.1: Output voltage range of converters in recent research

In this thesis, a reconfigurable Dual Active Bridge (DAB) converter will be proposed for an extremely wide output voltage range of 150V to 1000V. The converter will allow bidirectional power flow and a smooth tran-

sition between series and parallel without reducing the output power. To do this, a new method for smooth transitioning between series and parallel will be proposed. The topology and control will be optimized for high efficiency in the full operating range.

The following research question will be answered:

Can two DAB converters in series-parallel-output configuration extend the efficiency over a very wide voltage and power range?

- What topology and control methods can ensure smooth transitions, from series to parallel and vice versa, for two series-parallel output DAB converters under live bidirectional power flow?
- Can advanced range-enlarging modulation schemes like DPS, EPS or TPS increase the efficiency over a wide output and power range?
- How can the operating point of the series-parallel-output DAB converter be optimized to ensure maximum efficiency in all operating conditions?

In Chapter 2, previous work on wide output chargers is examined. Then, The design of the DAB is discussed and different modulation strategies are compared. In Chapter 4, a novel method for smooth transitioning is introduced. In Chapter 5, the newly developed smooth transitioning method is then integrated with the advanced modulation from Chapter 3. Then, in Chapter 6, the circuit design is optimized for the highest efficiency over the full operating range and finally, the smooth transitioning method is tested on a hardware prototype in Chapter 7.

2

Literature Review

The transportation sector is responsible for 29% of the total energy demand in the EU and electrification is happening in the whole transportation industry. Commercial cars are forced to be zero emission by 2035 and the emissions on freight and public transport are also tightly regulated. The increase in EV demand will surely increase the demand for EV chargers too. All EVs have different charging voltages. Currently, most Electric Cars are charged with 400V. Busses and some alternatively powered vehicles operate at a charging voltage of 600V while trucks are charging at 800V with high power. Since the introduction of the Porche Taycan in 2019, the market share of 800V cars is growing too. By doubling the voltage of the battery to 800V, the charging losses are reduced and maximum charging power can be increased, eventually reducing the total charging time [2]. All EVs are charging at different charging voltages and different charging power. In an effort to generalize the charger plugs for all EV types, some charging protocols like CHAdeMO and CCS increased the output voltage capabilities to 200V-1000V [17]. This calls for converters with a very wide output voltage capability. In this chapter, an overview of the current solutions is given in the form of a literature review. In Figure 1.1, a selection of wide output voltage converters is presented with their output voltage range. In this figure, three main converter topologies can be identified. These three topologies will be discussed in the next sections. Then, the techniques for reconfiguration are discussed.

Table 2.1: Summary of all the wide output solutions in recent research

Ref.	Topology	V_{min}	V_{max}	Bidirectional	Author	Year
[3]	LLC	150V	1000V	No	Aarninkhof, Lyu, Soeiro, et al.	2023
[4]	LLC	250V	850V	No	Forouzesh, Liu, and Sen	2022
[5]	LLC	200V	1000V	No	Elezab, Zayed, Abuelnaga, et al.	2023
[18]	LLC	200V	1000V	No	Mallik, Jain, and Kapat	2023
[10]	LLC + Buck	50V	650V	No	Lee, Kim, Lee, et al.	2019
[6]	CLLC	200V	700V	Yes	Wei, Zhu, Xie, et al.	2020
[9]	PSFB	250V	1000V	No	Lyu, Soeiro, and Bauer	2023
[14]	DAB	200V	1000V	Yes	Zayed, Elezab, Abuelnaga, et al.	2022
-	DAB	150V	1000V	Yes	This work	2023

LLC Converter

The LLC converter is a popular choice for low-loss unidirectional converters. The LLC converter can provide isolated power conversion with soft switching and high power density. The circuit of the converter is shown in Figure 2.1.

The LLC converter consists generally of a Full-Bridge (FB) or Half-Bridge (HB) inverter on the primary side with a resonant tank based around the transformer. On the secondary side, another FB or HB rectifier is used to rectify the output current. The advantage of the LLC converter is that it provides a ZVS condition for the primary bridge and a ZCS condition for the secondary diodes in a wide operating range [19]. Due to the soft switching, the switching frequency can be increased to high values allowing the converter to be very power-dense. The LLC converter is controlled by using variable frequency modulation (FM). The output voltage

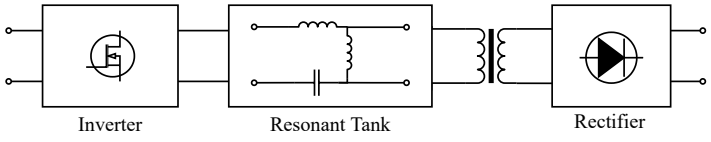


Figure 2.1: Circuit layout of an LLC Resonant converter

gain is changed by adjusting the switching frequency of the primary bridge. When the converter operates in a wide output voltage range, the switching frequency is far from the resonant frequency of the resonant tank. In these conditions the converter losses efficiency due to the loss of ZCS condition in the output diodes and the increased current when the primary Mosfets turn off. This makes the converter less efficient in a wide voltage range. Next to the efficiency losses in wide voltage applications, the power density is also decreased when the switching frequency has a wide operating region. This is due to the increased size of the transformer core to prevent saturation of the core [19]. In the next sections, some methods for increasing the output voltage range of the LLC converter are presented.

Resonant Tank Adjustments

With reconfiguration of the resonant tank, either the resonant tank is adjusted to obtain a new resonant frequency or the transformer is adjusted to alter the turns ratio. This way the output voltage can be extended without increasing the switching frequency range. In [19], a review of converters with resonant tank adjustments is given. Most proposed designs add passive components like capacitors or inductors. The components are added statically or can be included dynamically with the use of switches. For wide output converters, this is not the preferred method because it adds complexity to the resonant tank design [19]. Mallik, Jain, and Kapat present an LLC converter with a center-tapped transformer. The center tap of the transformer is connected to the output of the converter allowing the converter to operate in Full bridge mode and Center Tapped mode with different turn ratios. When the switch S1 is closed and the S2 is opened, the converter can supply a voltage range of 500V-100V. When the switch S2 is closed and S1 is opened, the converter can supply 200V-500V. The authors achieve an increased efficiency of 2% in the extreme frequency regions with an output voltage range of 200V-1000V.

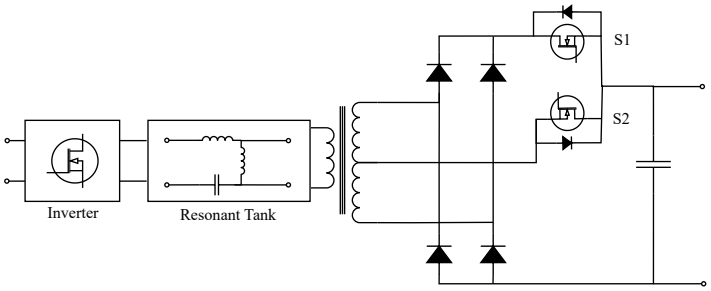


Figure 2.2: Circuit layout of the proposed converter by Mallik, Jain, and Kapat[18]

The disadvantage of adjusting the resonant tank is that the design of the converter becomes more complex. Furthermore, when adjustments are made to the resonant tank, often more passive components are included, reducing the power density of the converter [19].

Two Stage Converter

The second method is to use a two-stage converter where the LLC resonant converter is one of the two stages. In [10] and [3] the authors use an unregulated LLC converter that is operating at the resonant frequency for optimal efficiency. After the LLC converter, the voltage is stepped down by an unisolated buck converter. With this method the isolation is provided by the LLC converter and the buck converter is used to step down the voltage. The converter reaches an output voltage range of 50V-650V. An efficiency of 97.3% is reached. The disadvantage of this method is that the efficiency and power density will be limited. The addition of an extra stage will unavoidably reduce the efficiency of the total converter due to losses in the extra components for the second stage. Furthermore, the added components will reduce the converter power density and increase

the total converter cost.

Control Adjustments

The third method uses alternative control methods without adjustments to the circuit. Some of those methods include asymmetric PWM (APWM), Full Bridge/Half Bridge (FB/HB) operation, and Fixed Frequency Phase Shift (FFPS) [19]. With asymmetric PWM operation, the on and off time of the PWM signal are not symmetric as with a regular LLC converter. By using a hybrid APWM and FM combination the output gain can be increased [20]. By implementing an asymmetric PWM, the inductor current is also offset, causing saturation issues in the magnetic components. This reduces the power density of the device as the magnetics need to be oversized to avoid saturation [19]. FB/HB transition can increase the voltage gain by transitioning between Full Bridge and Half Bridge switching. Nevertheless, this method created high oscillations during the transition which is not desirable in charging converters. The last option is FFPS which introduces a phase shift in combination with regular FM. The method can enlarge the range of operations. In [21] the method is used to increase the range to low voltages to accommodate Battery Recovery. All of the methods mentioned are options for enlarging the converter range but most of them increase complexity significantly.

Output Circuit Adjustments

The last method is to alter the configuration of the secondary side circuit. This method is most often used when a wide output voltage is required. Forouzesh, Liu, and Sen present an EV charger for a wide output voltage. The authors use three rectifiers to rectify a three-phase AC input and use one single LLC converter for each phase. The outputs of the three converters are connected to the output using relays to choose between a series or parallel connection. This method ensures that the converters can operate in a more efficient frequency range with simple control. The converter reaches an efficiency of 96% but the efficiency over a wide voltage range is not discussed.

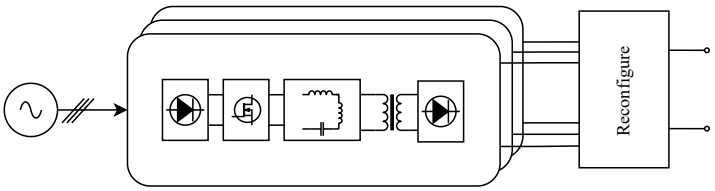


Figure 2.3: Circuit layout of the proposed converter by Forouzesh, Liu, and Sen[4]

Aarninkhof, Lyu, Soeiro, et al.[3] was already mentioned in the previous section on two-stage converters. The authors proposed a two-stage converter with reconfigurable outputs. The LLC converter is built with two secondary side windings, each connected to a buck converter. The buck converters are interleaved and used to step down the output voltage of the LLC converter. The circuit of the proposed converter is shown in Figure 2.4. The converter can achieve high efficiency of >95% in the whole operating range between 150V and 1000V. The authors use IGBT switches to switch the converter outputs between series and parallel. Whenever the middle IGBT is closed and the top and bottom IGBT are open, the outputs are in series. If the middle IGBT is opened and the top and bottom are closed, the outputs are in parallel. The authors reduce the conduction losses of the IGBTs by adding relays over the IGBTs. The disadvantage is already mentioned above, the efficiency of the full converter is still limited by the efficiency of the buck stage. Since there are two converters in the conduction path, the efficiency will inherently be lower. Furthermore, the design costs will be high and the power density will be lower due to the added components.

Elezab, Zayed, Abuelnaga, et al. propse an LLC converter with two outputs in [5]. The authors use two separate transformers. The two transformers help with reducing transformer losses. The two transformers are connected to a rectifier and a switchover circuit on the output. By switching between parallel and series. The converters will be operating in a smaller frequency range and the design of the converter is simplified. The converter has a peak efficiency of 98.7% and a minimum efficiency of 92%. In contrast to [3], the authors use frequency modulation on the LLC converter to control the output voltage. The advantage of this approach is that the extra buck stage is omitted. The disadvantage of the approach is that the two transformers reduce the overall power density.

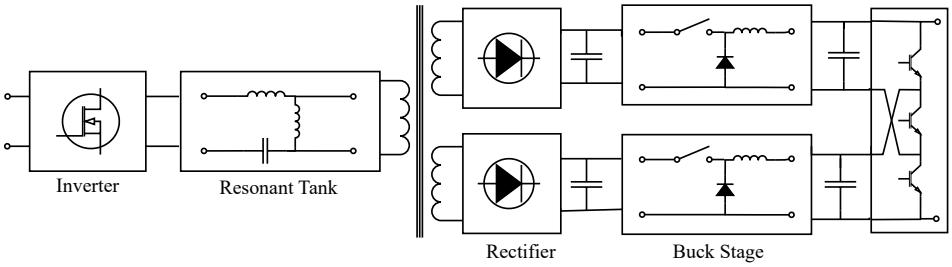


Figure 2.4: Circuit layout of the proposed converter by Aarninkhof, Lyu, Soeiro, et al.[3]

Bidirectional Current

The LLC converter has many advantages like isolation and high efficiency. Efforts in enlarging the output voltage range make it a viable solution for EV chargers [3]–[5], [22]. The LLC converter is a popular choice for unidirectional converters but is less suitable for bi-directional due to its asymmetric nature. All aforementioned LLC converters are unidirectional. Some authors propose an LLC converter where the output rectifier is replaced by a full bridge [23]. In [23], the authors propose an LLC+C converter where they make use of two smaller transformers and a center-connected capacitor to the secondary side to change the topology for reverse power flow. This way, the converter can be used in full bridge mode for charging from Grid to Vehicle (G2V). When the current is reversed to Vehicle to Grid (V2G) the converter can switch to half-bridge mode to increase the efficiency. The converter has an efficiency of >95% in G2V mode and >92% in V2G mode. Unfortunately, the converter is complex in design and can only operate in a voltage range from 300V-420V. The lack of good bidirectional power flow is one of the main disadvantages of the LLC converter. Other topologies can be considered to overcome this.

CLLC Converter

The CLLC resonant converter has gained more attention in recent research. Due to the symmetric topology, the CLLC converter is very suited for bidirectional power flow. The CLLC converter operates using two full bridges or half bridges connected through a CLLC resonant tank. The circuit is shown in Figure 2.5.

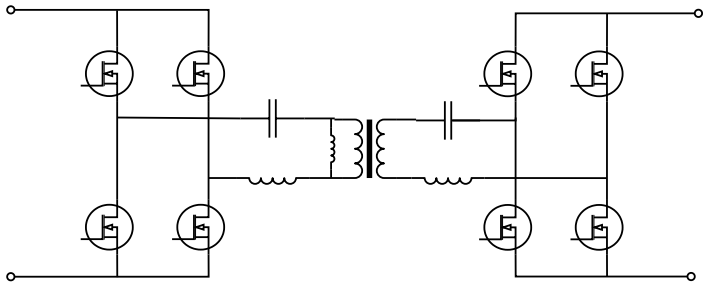


Figure 2.5: Circuit layout of the CLLC resonant converter

Like with the LLC resonant converter, the converter is controlled by adjusting the switching frequency of the bridges. The efficiency of the CLLC is also dependent on the switching frequency and is most efficient at the resonant frequency. There is not much research done on wide-output CLLC converters. Wei, Zhu, Xie, et al. propose a CLLC EV charger with an output voltage of 200V-700V [6]. The authors use a hybrid control scheme to control the CLLC converter in FB and HB modes. This increases the efficiency of the converter at low voltages. The proposed converter reaches an efficiency of 98.5% with a minimum efficiency of 91%. The CLLC converter is an interesting topology due to its high efficiency with bidirectional power transfer. To the best of my knowledge, a research gap remains for wide-output CLLC converters.

PSFB Converter

The Phase Shifted Full Bridge (PSFB) Converter is a unidirectional converter based around a FB inverter on the primary side and a FB or HB rectifier on the secondary side. The PSFB is controlled by adjusting the phase

shift between the two phases of the primary side inverter. The converter is often used in EV applications due to its high efficiency, easy control and galvanic isolation. Like the converters presented above, the PSFB suffers from decreasing efficiency in wide output voltage situations. Lyu, Soeiro, and Bauer compare three designs for increased output operation; r-PSFB, t-PSFB, and i-PSFB [9]. The authors compare the converters to assess which is best suitable for wide-output operation. The r-PSFB converter implements two secondary windings each connected to a FB rectifier an output filter and an RCD snubber network. The two outputs are connected to a reconfiguration circuit which can be used to place the outputs in series or parallel. The t-PSFB uses a center-tapped transformer which is used to connect the secondary side either in FB mode or in center-tapped HB mode. This method is similar to the method used in [18] but applied to a PSFB. The last converter, the i-PSFB, makes use of two primary bridges that are connected in parallel. The input bridges are interleaved with a phase difference ϕ, by adjusting this phase shift the output circuits will be in series or parallel due to the placement of the output diodes. Eventually, the r-PSFB turned out to be the best option when comparing costs and efficiency. The authors build an 11kW prototype to verify the converter efficiency in a wide output range. The peak efficiency of the converter is 97.76% and with maximum output current, the converter efficiency is >96% in the full output voltage range.

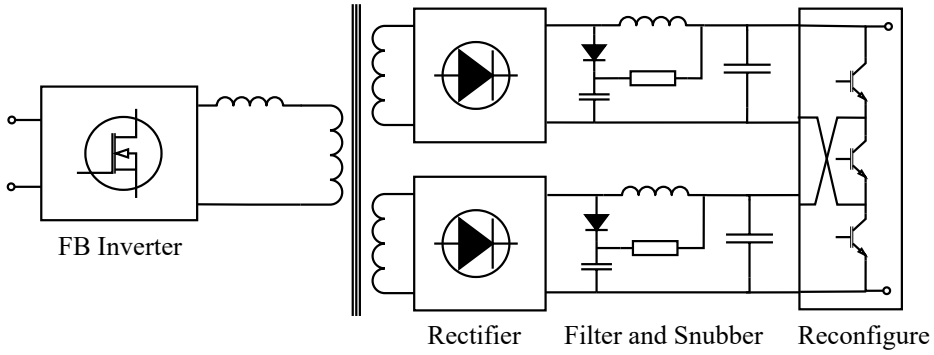


Figure 2.6: r-PSFB converter proposed by Lyu, Soeiro, and Bauer [9]

The proposed r-PSFB converter is a good solution since the converter can reach high efficiency in a wide output voltage range with a reasonable power density of 6.56 kW/L. Unfortunately, the r-PSFB can not provide bidirectional power flow.

DAB Converter

The last converter that will be covered in this review is the Dual Active Bridge (DAB). The DAB converter consists of two bridges with an inductor and transformer. The circuit is shown in Figure 2.7. The two bridges generate an alternating voltage on the primary and secondary sides and by shifting the two voltages the output current can be controlled. The DAB converter is considered to be a good solution for bidirectional EV chargers because of the inherent ZVS condition on all switches, high power density, simple control, and galvanic isolation. The DAB converter is most efficient when the voltage ratio from the input to the output is equal to the transformer turns ratio. In wide voltage operation, the efficiency of the DAB converter drops due to the loss of ZVS in the switches and due to the increase of backflow power.

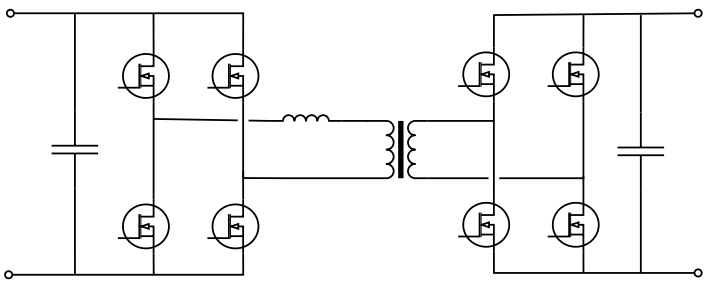


Figure 2.7: Circuit of the Dual Active Bridge Converter

In [14], Zayed, Elezab, Abuelnaga, et al. present a 10kW EV charger for wide battery voltages (200V-1000V). The authors use a reconfigurable output with a three winding transformer as shown in Figure 2.8. The converter has an output voltage range of 200V-1000V with a maximum efficiency of 98.9%. The efficiency of the converter is >90.1% in all operating conditions, including low voltage and low power (0.1 p.u.) situations. The efficiency during one full charging cycle is 97.9% and 97.5% for 400V and 800V batteries respectively.

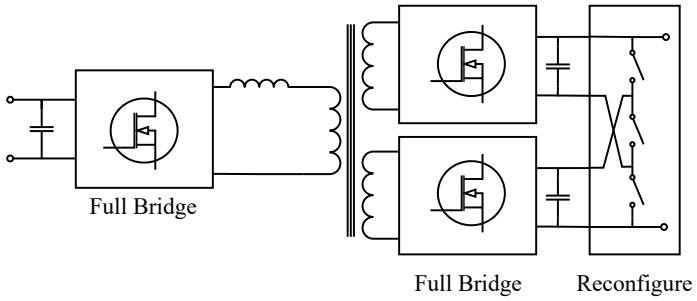


Figure 2.8: Proposed converter by Zayed, Elezab, Abuelnaga, et al. [14]

Review of Range Enlarging Solutions

In the sections above, a selection of topologies is presented for wide-output EV charging. From these topologies, three different range-enlarging solutions can be identified. Those solutions are not dependent on the used converter topology and can thus be compared separately.

Cascaded Converters

One of the methods for increasing the output voltage range is by cascading multiple converters. In [3] and [10] the authors used a two-stage converter with an LLC and a Buck converter as the first and second stages respectively. With this method, the LLC converter provides the isolation — and possibly a step up/down with the transformer turn ratio — and the buck converter provides the control in output voltage. Ensuring that the resonant converter is always operating in the most efficient operating point. The method of cascading is not limited to the LLC converter and is often used with other topologies too. The main advantage of cascading is the simplicity of the design and control. Especially in the case of the buck converter, the added design effort is low and the control is simple. However, when an extra converter is added, the losses at the most efficient operating point are reduced. The extra buck stage will add costs to the converter and the power density will be reduced compared to a single converter.

Topology Reconfiguration

The second method that is often used for increasing the voltage range is an adjustment of the used topology. In the case of a resonant converter, this is often done by rearranging passive components using switches [19]. By rearranging passive components the resonant frequency changes and the converter can operate at a more efficient operating point. An example of this method is used in [18]. Aside from resonant converters, many converters implement this strategy. As an example, in [24] the authors propose an interleaved half-bridge converter with a cascaded voltage doubler. By rearranging switches in the converter, it can operate in four different modes: Interleaved Boost, Single-boost, Cascaded buck-boost, and Single-buck allowing the converter to operate in a voltage range of 20V-1000V. The disadvantage of this kind of topology reconfiguration is the added components and design complexity [19]. In the case of reconfigurable resonant converters, the resonant tank needs to be carefully designed to stably operate in two regions. Designing the passives to operate in multiple operating points, will sometimes lead to larger passive components.

Output Reconfiguration

The last method of enlarging the output range is output reconfiguration. By reconfiguring the output of a converter between series and parallel, the range of a converter can be easily increased. [3]–[5], [9], [14] all use reconfiguration on the output side. The converters either, consist of multiple separate converters [4], use multiple transformers to create two outputs [5], or use a multi-winding transformer to create two outputs [3], [9], [14]. The advantage of reconfiguring the output is that the design and control methods remain relatively

simple. Furthermore, by reconfiguring the output, the converter outputs can be repurposed to increase the output voltage or the output current depending on the state of the output switches. This reduces oversizing of the converter and increases the power density at low voltages. The disadvantage is that the output circuit adds conduction losses during operation. [3] and [9] reduce the conduction losses by using relays in parallel with the IGBT switches on the output.

Live Transitioning

As discussed in the introduction, the output voltage range of EV chargers has become large since the increased capabilities of CCS and CHAdeMO. In Table 2.2 the ranges of EV batteries are shown. All EVs shown in the table are compatible with CCS and thus the charger needs to supply all of these voltages.

Table 2.2: Battary voltage range of different Electric Vehicles on the market.

Vehicle Type	Model	Min	Max
Hatchback	Nissan Leaf	288V	403V
Sedan	Tesla Model S	-	340V*
Bus	Volvo 7900 Electric	500V	700V
Bus	Mercedes eCitaro	486V	660V
Sedan	Porsche Tycan 4S	520V	720V
Sedan	Hyundai IONIQ 6	-	697V*

* Only nominal value available

During a charging cycle, the terminal voltage of the battery pack will rise. During V2G operation the battery voltage will decrease. It is therefore important that the converter can supply the whole voltage range continuously without interruption of the charging process. The proposed LLC+Buck converter in [10] is capable of supplying the full range without interruption by adjusting the output voltage of the buck converter. The CLLC converter in [6] is also capable of supplying the full range but the range of the CLLC converter is limited to 700V. All converters with reconfiguration on the output are not capable of supplying the full voltage range without interruption because the converters can not change configuration during operation. Aarninkhof, Lyu, Soeiro, et al. propose to use a communication period before the charging starts. During this period the converter determined the charging voltage range and reconfigures the output appropriately. Whenever the output voltage crosses the transition border of 500V, the converter will initiate a shutdown-reconfiguration-restart sequence. With this method, the charging time will be increased. To overcome the shutdown procedure, a live transition method is necessary. With a live transition, the converter can transition between series and parallel without shutting down the charging process. This reduces the charging time and the control complexity by eliminating the shutdown-reconfigure-restart sequence. With a live transition, the benefits of reconfigurable outputs can be combined with full-range capabilities.

To the best of my knowledge, there has been no EV charger with reconfiguration and live transitioning yet. In Table 2.3 a list of converters with some form of live transitioning is presented.

Table 2.3: Summary of converters with Live transitioning

Ref.	Topology	V_{min}	V_{max}	Bidirectional	Live Transition	Author
[11]	PSFB	20V	150V	No	Sun, Zhou, and Smedley	2010
[25]	LLC	200V	400V	No	Rathore, Reddy, and Rajashekara	2022
[26]	PSFB	20V	150V	No	Sun, Zhou, and Smedley	2011
-	DAB	150V	1000V	Yes	This work	2023

[11], [25] and [26] all use a reconfiguration method like presented in Figure 2.9. The authors use two diodes and one switch to connect the two outputs of the converters. In this figure 'Output 1' and 'Output 2' are different converters for each source. Whenever the switch S is opened, the output will be connected directly to V_{out} through diodes D_1 and D_2. The converter outputs are then in a parallel configuration. When the auxiliary switch S is closed, the converters are in series and the diodes will be reverse-biased. In 2010, Sun, Zhou, and Smedley presented a similar reconfigurable PSFB converter but for a lower output voltage of 20V-150V. Although the output voltage range is not impressive, the authors used an interesting way of reconfiguration. The authors change the state of the switch S from closed to open during operation. This

changeover causes the output current to increase by 200% which is not desirable. In [26], Sun, Zhou, and Smedley address this issue by stepping down the duty ratio at the same instance as S changes state. This way, the output current remains stable at the reference value without large overshoots. Rathore, Reddy, and Rajashekara go even further with the integration of the switch S and present a multilevel converter with hybrid resonant switching. The authors make use of the auxiliary switch by integrating it into the modulation. This causes the output circuit to be in series for part of the modulation period and in the other period, the output is in parallel. By switching S in the right part of the modulation, the switch acts as a voltage doubler for the resonant circuit. The converter is capable of supplying 200V-400V.

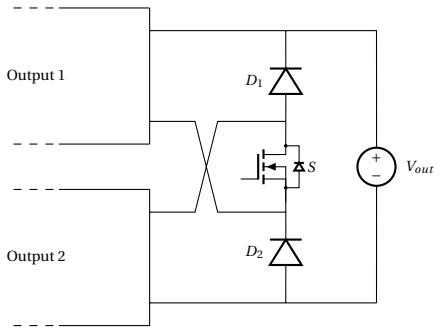


Figure 2.9: Switchover circuits used in [11], [25], [26] where 'Output 1' and 'Output 2' are the outputs of the used converter topology in the literature

Research Gap

EV chargers for 200V-1000V range are just recently starting to be developed and not much research has been done in this field. Especially wide range bi-directional chargers remain underexplored until this day. Out of the 10 wide-range chargers in this review, only two feature bidirectional power. When examining the proposed solutions for enlarging the output voltage range, output reconfiguration is a strong candidate. An EV charger with reconfigurable output can provide high efficiency over a wide output range without compromising on power density. With reconfigurable outputs the circuit design and control are kept simple compared to other range enlarging methods. The biggest downside of reconfigurable output is the restriction in live reconfiguration. The presented converters can not reconfigure during charging which can be necessary when voltages change during charging/discharging of the EV battery.

In this thesis, a bidirectional charger with a wide output voltage and live transitioning is presented. The converter will provide high efficiency in a very wide voltage range and is capable of transitioning without interrupting the charging process. In the reviewed literature two converter topologies proved to be suitable for bidirectional power. The CLLC converter and the DAB converter. Both converters provide high efficiency with inherent ZVS and galvanic isolation. In this thesis, the DAB converter is chosen.

3

The Dual Active Bridge

Eventually, the goal of this report is to design a converter with extremely high efficiency in a very wide operating range. To do this, the converter will be split up into two submodules that can be placed in series or parallel. In this chapter, the theory for the Dual Active Bridge (DAB) is introduced and range-enlarging modulation strategies are explored. Finally, the losses in the DAB are modeled analytically for each component. The full loss model is made in Matlab.

3.1. Single Phase Shift

The Dual Active bridge consists of two full bridges coupled by an inductor or transformer. The circuit of the DAB converter is presented in Figure 3.1. The primary and secondary side bridges can both generate an alternating voltage. The alternating square wave voltages are shown in Figure 3.2. By introducing a phase shift between the primary and secondary sides of the transformer, the current can be controlled. This modulation method is called Single Phase Shift (SPS). SPS is the simplest form of modulation and controlling the output current with this modulation is straightforward.

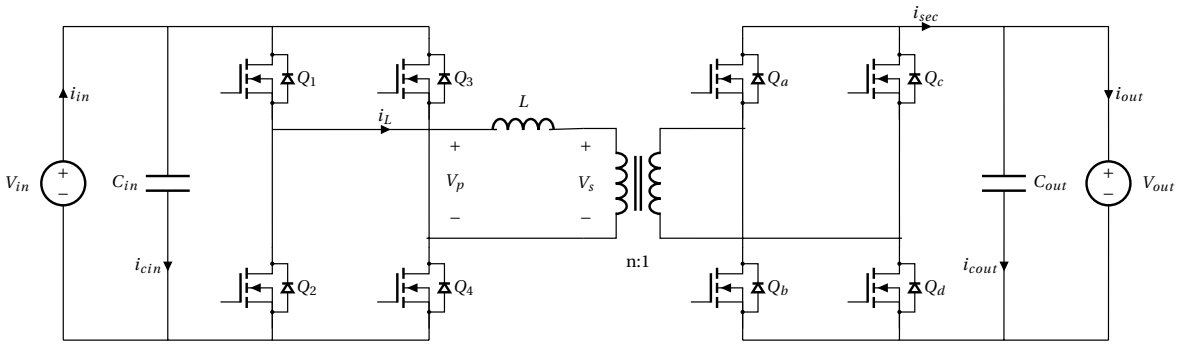


Figure 3.1: Circuit Diagram of the Dual Active Bridge Converter

In this report, D is defined as the relative phase shift between Q_1 and Q_a. Where $D = 1$ corresponds to a phase shift of a half period. When considering a period of 2π, the phase angle of the secondary bridge can now be determined by $\phi = D\pi$. Or in other words, the time t_1 is determined by $D(T_s/2) = Dt_h$. Where T_s is the period and t_h is half the period.

The inductor current is calculated by using Figure 3.2, and solving the inductor current for each linear period. This method can easily be extended to other modulation methods. The inductor current is obtained by applying KVL for Figure 3.3, resulting in Equation 3.1.

$$V_p - V_s = L\frac{dI}{dt} \tag{3.1}$$

When Equation 3.1 is substituted for each section in Figure 3.2, a system of equations results. Since the currents in the second half period are the inverse of the first half period, only the currents at t_0 and t_1 need

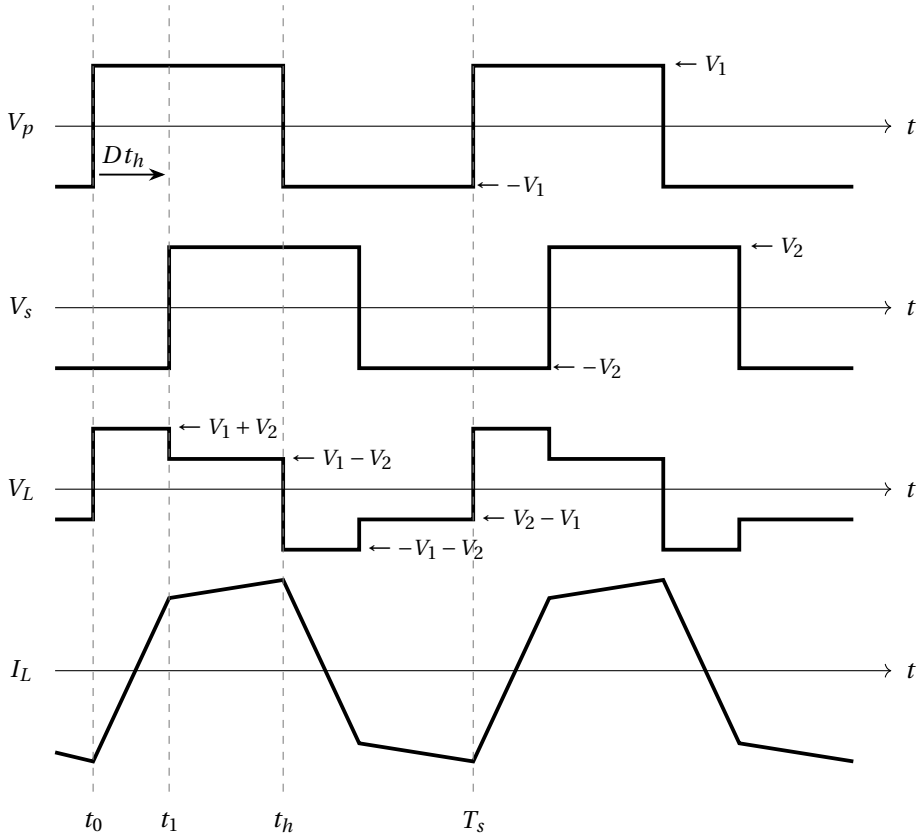


Figure 3.2: Switching patterns and inductor current for Single Phase Shift Modulation. Where the following applies:$V_L = V_p - V_s$, $V_1 = V_{in}$, $V_2 = nV_{out}$ and $t_h = 1/(2f_s)$

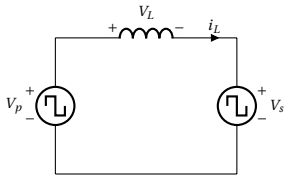


Figure 3.3: Equivalent circuit of primary and secondary bridges

to be calculated. The time instances can be calculated from the phase shift values as shown in Equation 3.2. The currents at t_0 and t_1 can be derived by rewriting the equations and solving for the currents. A current at time instance t_x is represented by I_x.

$$V_1 + V_2 = L\frac{I_1 - I_0}{t_1 - t_0} \tag{3.2}$$

$$V_1 - V_2 = L\frac{-I_0 - I_1}{t_h - t_1} \tag{3.3}$$

$$I_0 = A(V_2(2D-1) + V_1) \tag{3.4}$$

$$I_1 = -A(V_1(2D-1) + V_2) \tag{3.5}$$

Where:

$$t_0 = 0$$
$$t_1 = D t_h$$
$$V_1 = V_{in}$$
$$V_2 = n V_{out}$$
$$A = \frac{-1}{4 f_s L}$$

The output power can be obtained by calculating the average output current. The average output current can be calculated based on the inductor current and the state of the secondary bridge. The output current is shown in Figure 3.4.

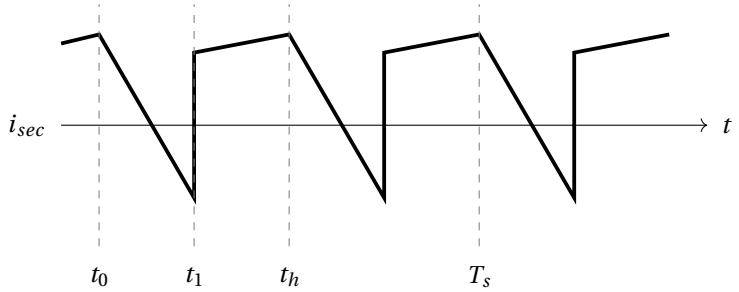


Figure 3.4: Output current with SPS, without filtering

The average output power can be calculated by integrating over t_h, leading to Equation 3.7.

$$I_{out} = \frac{1}{t_h} \int_0^{t_h} i_{sec}(t)\, dt \tag{3.6}$$

$$P_T = \frac{V_1 V_2}{2 f_s L} D(1 - D) \tag{3.7}$$

As can be seen from Equation 3.7, the maximum power will be transferred when $D = 0.5$. This results in a power limit as described in Equation 3.8.

$$P_{max} = \frac{V_1 V_2}{8 f_s L} \tag{3.8}$$

By rearranging Equation 3.7, the phase shift D can be determined for a given P_{out}.

$$D = \frac{1}{2} - \frac{1}{2}\sqrt{1 - p^*} \tag{3.9}$$

Where p^* is the normalized reference power $p^* = P_T / P_{max}$.

3.2. Component Design

In the next sections, a model of the DAB converter is formulated. To make this model it is useful to have some design requirements and parameters. In this section, a rough design is made and some preliminary component values are calculated. These values will be used to simulate a single DAB converter and to compare modulation strategies. In Chapter 6, the design of the submodule is optimized for the highest efficiency of the whole converter. The design in this chapter will not be perfect, but good enough for comparative analysis.

The converter will be supplied from a home storage system and the input voltage is assumed to be fixed at 750V. The output of the converter will be connected to a car battery. The output voltage of the converter will be 150V-1000V. Because the submodules can be placed in series, the output voltage of one submodule will be 150V-500V. In this section, the design will be optimized for an output voltage of 400V. The total output power of two converters is 25kW, so the power of one submodule is assumed to be 12.5kW.

The output current limit will be derived from the maximum power at nominal voltage. Resulting in a limit of 31.25A. The limit will be increased to 32A. The switching frequency f_s is given and fixed at 100kHz. The resulting converter design is summarized in Table 3.1.

Table 3.1: Design requirements of a single submodule without optimization.

Parameter	Symbol	Value
Frequency	f_s	100kHz
Input Voltage	V_{in}	750V
Output Voltage	V_{out}	150V — 500V
Output Power	P_{max}	12.5 kW
Output Current	I_{max}	32A

Inductor

The inductor can be designed with the parameters from Table 3.1. First the design of the inductor is discussed then the losses are modelled.

Design

The maximum inductor value can be calculated by rearranging Equation 3.8 to arrive at Equation 3.10. The maximum power transfer happens at $k = 1$ so V_1 and V_2 are equal. The inductor will be designed with the maximum inductor value. In Chapter 6, the design will be optimized.

$$L_{max} = \frac{V_1 V_2}{8 \cdot f_s \cdot P_{max}} = \frac{750^2}{8 \cdot 100kHz \cdot 12.5kW} = 56.25\mu H \tag{3.10}$$

For this first design, an E65 core will be used with N27 ferrite material. The properties of an E65 core and N27 ferrite material are listed in Table 3.2.

Table 3.2: Parameters of an E65 core with N27 material [27]

Parameter	Symbol	Value
Effective area	A_e	535 mm^2
Effective length	l_e	147mm
Effective volume	V_e	78650 mm^3
Rel. permeability	μ_r	1570
Saturation point	B_{sat}	350mT
	k_c	16.9
	α	1.25
	β	2.35

In Table 3.2, the saturation point of the N27 material is shown. Unfortunately, when the switching frequency is high, heat loss becomes a limiting factor. In this case, $B_{max} = 250mT$ is chosen from the datasheet as a maximum field strength at 100kHz.

From this field limit, it is possible to calculate the minimum amount of turns with equation 3.11 [28]. The maximum inductor current can be calculated by using Equation 3.4. The current is maximal at the maximum power and minimum output voltage. For 12.5kW the minimum output voltage is 400V, according to Equation 3.8. This results in a peak inductor current of $I_{max} = 33.3A$.

$$N_{min} = \frac{L \cdot I_{max}}{B_{max} \cdot A_e} = \frac{56.25\mu H \cdot 33.3A}{250mT \cdot 535mm^2} = 14.02 \text{ Turns} \tag{3.11}$$

N_{min} is rounded up and 15 turns are chosen for the inductor. The airgap length l_g can be calculated using Equation 3.12. In this equation, the fringing effect of the inductor is taken into account. The method is taken from [29]. The authors model the fringing effect by enlarging the effective area in the airgap. Half the length of the airgap is added to each side as shown in Figure 3.5. The resulting equation for the airgap is now calculated by Equation 3.12 [29].

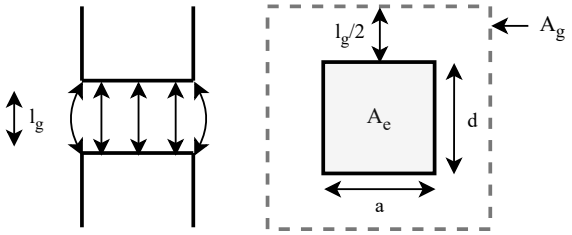


Figure 3.5: Area compensation for the fringing effect

$$l_g = \frac{A_e}{\frac{AeB_{max}}{\mu_0 N I_{max} - \frac{a+d}{Ng}}} \tag{3.12}$$

Where a and d are the width and depth of the core as defined in Figure 3.5 and N_g is the airgap distribution. In the used E-core, the airgap is distributed over three gaps so $N_g = 3$ resulting in an airgap length of 2.2mm. A standard gap of 2.5mm is chosen resulting in a maximum field strength of 226mT and an inductance of $50.8\mu H$.

Now that the core and amount of turns are defined, the Litz wire can be calculated. To design the optimal Litz wire, LitzOpt is used. The core and bobbin parameters are entered into LitzOpt to obtain a list of possible designs and associated losses for a current waveform. The designs are listed in Table 3.3.

Table 3.3: Output designs from LitzOpt

Gauge	Relative Costs	Loss (W)	No. Strands
36	0.0796	49.2	24.40
38	0.1330	33.2	60.30
40	0.2330	22.8	150
42	0.4490	16.1	373
44	1	12	890

The design with 42 AWG is chosen. A wire is selected from the catalog of the Pack Litz Wire website [30]. The final wire design has a wire diameter of 0.071mm (42AWG) and 405 strands. Resulting in a loss of 16.1W with an inductor current like in Figure 3.2 and a peak of 26A. To optimally use the wire copper area, the strand radius must be smaller than the skin depth at the operating frequency. Verification of the skin depth shows that this is indeed the case.

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi \mu_0 f_s}} = 0.21mm \tag{3.13}$$

The design is summarized in Table 3.4 and the losses are calculated in the next section.

Table 3.4: Inductor Design Parameters

Parameter	Value
Core	TDK E65/32/27
Material	N27 Ferrite
Turns	15
Airgap	2.5mm
Inductance	$50.8\mu H$
Wire	405x 42AWG

Losses

The losses of the inductor consist of two parts, winding losses and core losses. The winding losses are due to the resistance of the inductor wire. When the switching frequency is high, the wire resistance changes due

to the skin effect and proximity effect. A 1D method is chosen to calculate the proximity effect. This method will give a good approximation for comparative analysis [31]. With the 1D method, the DC wire resistance is scaled by an AC resistance factor F_r. Where F_r is defined in Equation (3.14) [31].

$$F_r = 1 + \frac{\pi^2 \omega^2 \mu_0^2 N^2 n^2 d_c^6 k}{768 \rho_c^2 b_c^2} \tag{3.14}$$

Where:

$\omega = 2\pi f_s$

N = Turns

n = Amount of Strands

d_c = Diameter of one strand

k = Winding Distribution Factor

ρ_c = Resistivity of copper

b_c = breath of the window area of the core

The wire losses can now be calculated with Equation (3.15). Where l_e was the effective wire length of one turn around the bobbin.

$$P_{wire} = I_{rms}^2 F_r \frac{l_e N \rho_c}{n\pi (d_c/2)^2} \tag{3.15}$$

The core losses are calculated by using the method described in [32]. The method can accurately predict core losses for non-sinusoidal waveforms using an improved "generalized Steinmetz Equation" (iGSE) method for Peacewise Linear (PWL) waveforms. The PLW waveforms can be split into one peace for each linear section. The time average volumetric power can be calculated for each section by Equation 3.16.

$$\overline{P_v} = \frac{k_i (\Delta B)^{\beta-\alpha}}{T} \int_0^T \left| \frac{dB}{dt} \right|^\alpha dt \tag{3.16}$$

Where ΔB is the peak-to-peak field variation, T is the total period of the waveform, α and β are the Steinmetz parameters that can be derived from the datasheet of the core material, and k_i is defined by Equation 3.17. Where k_c, α and β are the Steinmetz parameters of the material.

$$k_i = \frac{k_c}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^\beta d\theta} \tag{3.17}$$

When the slope of each segment is a linear function, as is the case with PWL waveforms, $\left|\frac{dB}{dt}\right|$ can be defined as

$$\left| \frac{dB}{dt} \right| = \frac{B_{m+1} - B_m}{t_{m+1} - t_m}$$

resulting in the power loss per unit volume per time segment in Equation 3.18.

$$\overline{P_v} = \frac{k_i (\Delta B)^{\beta-\alpha}}{T} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^\alpha (t_{m+1} - t_m) \tag{3.18}$$

The total loss is now calculated by using a weighted average of the losses in each period [32].

$$P_{core} = \sum_i P_i \frac{T_i}{T} \quad (W/m^3) \tag{3.19}$$

The Steinmetz parameters for N27 material are shown in Table 3.2. Venkatachalam, Sullivan, Abdallah, et al. have created a Matlab implementation of this method [32]. This Matlab function takes the Steinmetz parameters and a series of field strengths and times. The function then calculated the core loss per unit volume.

The field strength in the inductor is dependent on the inductor current. It can be defined by Equation 3.20.

$$B(t) = \frac{L \cdot i_L(t)}{NA_e} \tag{3.20}$$

By using the outcome from the modulation, the core losses can be calculated by filling in Equation 3.20 and using the resulting piecewise linear field in Equation 3.19.

The core losses and the winding losses are added to get the total losses in the inductor.

Transformer

the transformer is modeled and then a method for loss estimation is discussed.

Design

The DAB converter operates at the highest efficiency when $k = 1$. With this knowledge in mind, the turns ratio for the converter can be calculated to ensure the best efficiency for a 400V output. The turns ratio is optimized in Chapter 6.

$$n = 750/400 = 1.875 \tag{3.21}$$

The transformer will be modeled with the same core as the inductor. In comparison to the inductor design, the design of the transformer is based on the voltage across the windings.

$$B(t) = \frac{1}{NA_c} \int v(t)\,dt \tag{3.22}$$

Equation 3.22 describes the relation between the integral of the terminal voltage of the transformer and the field inside the core. This equation can be used to calculate the minimum amount of turns to prevent the core from saturating. The saturation point of the inductor is equal to that of the inductor, $B_{max} = 250mT$. In Figure 3.2, the voltage waveforms are shown. From this figure, it is easiest to retrieve the voltage at the secondary side. The voltage is equal to V_{out} for the period $(1 - D_3) \cdot t_h$. The integral is maximal when the voltage $V_{out} = V_{out,max} = 500V$ and the phase shift $D_3 = 0$.

$$N_s = \frac{V_{out,max}\, t_h}{\Delta B A_e} = \frac{500 \cdot 5\mu s}{500mT 535mm^2} = 9.3 \tag{3.23}$$

Where ΔB is the maximum field swing which is from -250mT up to 250mT resulting in a maximum allowable ΔB of 500mT. The turns count on the secondary side can be multiplied by the turns ratio to acquire the number of primary turns. The primary and secondary turns are chosen to be 19 and 10 respectively.

The transformer core will not be gapped to optimize the coupling factor of the two windings and increase efficiency. The primary wire will be chosen to be the same as the inductor wire as the current is identical. Since the secondary current will be almost twice as high, a litz wire with 775 strands is chosen for the secondary winding. The wire is again selected from the Pack Litz Wire catalog[30].

Losses

The losses are calculated in a similar way as the inductor. First, the primary and secondary winding losses are calculated using Equation 3.15 for each side. Then, the core losses can be calculated by using the same method as the inductor. The B field is now calculated using the secondary voltage instead of the current. The field will now be triangular and the peak can be calculated using Equation 3.22. The integral of the voltage can be easily calculated for the secondary side. The voltage is constant and equal to V_{out} and the time that the voltage is applied is $(1 - (D_3 - D_2))\,t_h$. This can be derived from Figure 3.2. When applying the aforementioned integral and when assuming the field is symmetric around the x-axis, Equation 3.22 will result in Equation 3.24.

$$B(t) = \frac{1}{NA_c} V_{out} * (1 - (D_3 - D_2))\,t_h \tag{3.24}$$

The field is again inserted into the coreloss function in Matlab to obtain the core losses per unit volume. The core losses and the winding losses are added to obtain the full loss of the transformer.

Switches

All the switches in the primary and secondary bridges are Silicon Carbide Mosfets. For this preliminary design, the C3M0016120K from CREE is selected. The switches are chosen because they fit the required current and voltage limits of 66A on the secondary side and 1000V on the primary side. The capabilities of the Mosfets are shown in Table 3.5.

Table 3.5: CREE C3M0016120K capabilities

Parameter	Symbol	Value
Drain Source Voltage	$V_{ds,max}$	1200V
Drain Current	$I_{d,max}$	115A
On resistance	$R_{ds,on}$	$16m\Omega$

The losses consist of two parts; conduction losses and switching losses. The conduction losses are caused by the resistance $R_{ds,on}$. These losses can be calculated by using the RMS current through the switch.

$$P_{cond} = I_{rms}^2 R_{ds,on} \tag{3.25}$$

The switching losses are calculated by interpolating data from the datasheet using Matlab. The interpolated data for the turn on losses are shown for three voltage levels in Figure 3.6.

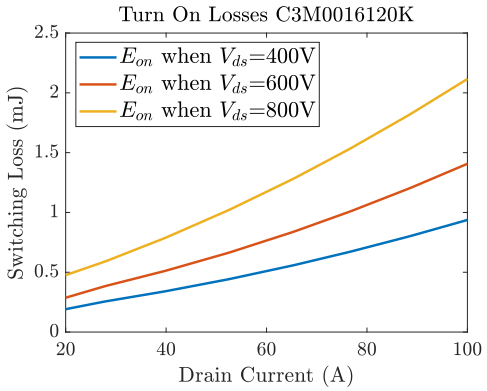


Figure 3.6: Turn On energy losses from the datasheet of the C3M0016120K. Shown for all drain currents and three drain-source voltages. Temperature 25°C

The data can be used to calculate the turn-on and turn-off losses for one second by multiplying the energy loss by the switching frequency.

$$P_{on} = E_{on}(V, I) \cdot f_s \tag{3.26}$$

The switching losses are calculated for every switching leg by correlating the corresponding peak current with the right switching leg. In the case of SPS, the first two bridges switch at the same instance and from Figure 3.2, it is visible that they switch at time instance t_1. Since $D_1 = 0$ with SPS, t_1 is the same instance as t_0. The secondary bridge switches on at time instance $t_2 = t_3$. Since the inductor current is reversely symmetric in the second half period, the switches turn off at the same current.

3.3. Diodes

The antiparallel diodes across the Mosfets carry the current when both switches are open. The diodes will have losses during this dead-time period. The losses are small because the dead-time is short. The losses can be approximated by using the forward diode voltage and the current flowing through the diode.

$$P_d = V_f \cdot I_d \, t_{dead} \, f_s \tag{3.27}$$

Where V_f is the diode forward voltage and I_d is the diode/switch current during the dead-time. The current I_d would actually be changing during the dead-time but, since the dead-time is small compared to the switching frequency, the current can be considered constant to approximate the losses. The current flowing through the diode can be approximated by the current through the switch at the switchover instance.

Capacitors

The input and output capacitors can be calculated based on the maximum input and output current ripple and the maximum allowed voltage ripple. The maximum allowed voltage ripple is set to 5% for both the input and the output. The current through the capacitor is the difference between the output current of the switching leg i_{sec} and the average output current I_{out}.

$$i_{cout} = i_{sec}(t) - I_{out} \tag{3.28}$$

The charge that needs to accumulate in the capacitor during a period. The charge can be calculated by integrating the current over the positive half of the period.

$$Q_{cap} = \int_0^T i_{sec}(t) - I_{out} dt \tag{3.29}$$

In Figure 3.4 the output current is shown. The peak current can be calculated by multiplying the peak current $I_{max} = 33A$ with the turn ratio n resulting in 62A.

$$Q_{c,out} = \frac{1}{2} I_{pk} \Delta t = \frac{1}{2} 62A \cdot 1.95\mu s \cdot = 60.05\mu C$$

$$Q_{c,in} = \frac{1}{2} I_{pk} \Delta t = \frac{1}{2} 33A \cdot 1.95\mu s \cdot = 32.2\mu C$$

The capacitor value can now be calculated by dividing the charge by the maximum allowed voltage ripple.

$$C_{out} = \frac{Q_{cap}}{\Delta V_{min}} = \frac{60.05\mu C}{0.05 \cdot 150V} = 8.1\mu F \tag{3.30}$$

$$C_{out} = \frac{Q_{cap}}{\Delta V_{min}} = \frac{32.2\mu C}{0.05 \cdot 700V} = 0.92\mu F \tag{3.31}$$

The output capacitor losses can be calculated with the Equivalent Series Resistance of the capacitor.

$$P_{cap} = i_{c,rms}^2 R_{esr} \tag{3.32}$$

For the output capacitor losses, an ESR is taken from the datasheet of an 800V $4\mu F$ film capacitor from TDK. The value was $3.2m\Omega$. Two in parallel would give an ESR of $1.6m\Omega$.

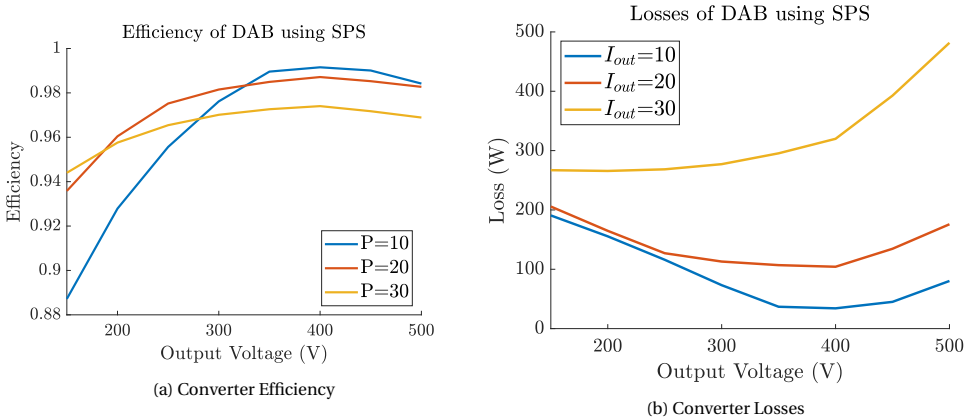
Battery Model

Eventually, this converter will be used for EV charging. The dynamics of the battery play a big role in the operation and design of the switchover circuit. The battery will be modeled in PLECS for use in dynamic simulations. The battery model is based on [33] and accounts for dynamic characteristics of the battery, from nonlinear open-circuit voltage, current-, temperature-, cycle number-, and storage time-dependent capacity to transient response [33].

The battery of choice is a battery from the Nissan Leaf. The battery characteristics are shown in Table 3.6 [34].

Table 3.6: Battery Characteristics of the Nissan Leaf [34]

Parameter	Value
Capacity	169 Ah
Cells Series	96
Cells Parallel	3
Chemistry	NCM 523
Cell Voltage	3.65V



(a) Converter Efficiency

(b) Converter Losses

Figure 3.7: Converter losses and efficiency calculated for different powers and output voltages.

Results

In the previous sections, the components are designed and the losses are calculated. The loss equations can now be used in Matlab to estimate the total losses of the converter in any operating condition. The losses and efficiency of a single converter with SPS modulation are shown in Figure 3.7.

From Figure 3.7 it is clear how the efficiency of the converter is affected by the output voltage and output current. When the output voltage is far from the optimal point (400V), the efficiency of the converter drops to 94% and even down to 88% at low power. This can be improved by using other modulation strategies. In the next sections, advanced range enlarging modulation methods will be explored.

3.4. Dual Phase Shift

Until now, only SPS was considered but this modulation is losing efficiency in operating points where the voltage ratio between the primary and secondary sides is large. SPS modulation suffers from high reactive power and a limited ZVS range [35], [36].

In 2008, Bai and Mi proposed a novel Dual Phase Shift modulation to eliminate reactive power and increase system efficiency[36]. This modulation reduced the reactive power flow of the DAB by adjusting the phase shift between the two bridges on the primary and secondary sides. This additional control variable gives freedom for further optimization. In 2012, Zhao, Yu, and Sun modeled the power transfer and dynamic performance of the DAB using DPS. In this report, the convention of Zhao, Yu, and Sun is used, where D_1 is the phase shift between Q_1 and Q_3 and between Q_a and Q_c. D_2 is the phase shift between Q_1 and Q_a. This modulation can be defined as the case where $D_3 = D_1 + D_2$ in Figure 3.8. The derivation of the inductor current is discussed in the next section, then the optimization strategies are discussed.

Inductor Current

To get a good understanding of the inductor and switching losses, the inductor currents at each time interval need to be calculated. The inductor current as shown in Figure 3.8 can be broken down into piecewise linear sections. By using KVL for each of the sections, a system of equations results[35]. The model of [35] is only valid for the cases where $D_1 + D_2 \leq 1$. The model is expanded by calculating the current equation for each of the four modes. In the next section, the current is calculated for Mode 1, where $D_1 \leq D_2$, $D_1 + D_2 \leq 1$. The same method can be applied to all four modes resulting in Table 3.7.

The inductor current consists of linear parts for each of the time intervals. During each interval, the slope of the current is depending on the inductor voltage. The inductor voltage is defined as $V_L = V_p - V_s$, where V_p and V_s are the resulting output voltages of the primary and secondary bridges. The voltage levels are presented in Figure 3.8.

$$V_p - V_s = L\frac{dI}{dt} \tag{3.33}$$

When Equation 3.1 is substituted for each time interval in Figure 3.8, a system of equations results. The time instances can be calculated from the phase shift values as shown below. The currents at t_0, t_1, t_2 and t_3 can be derived by rewriting the equations and solving for the currents.

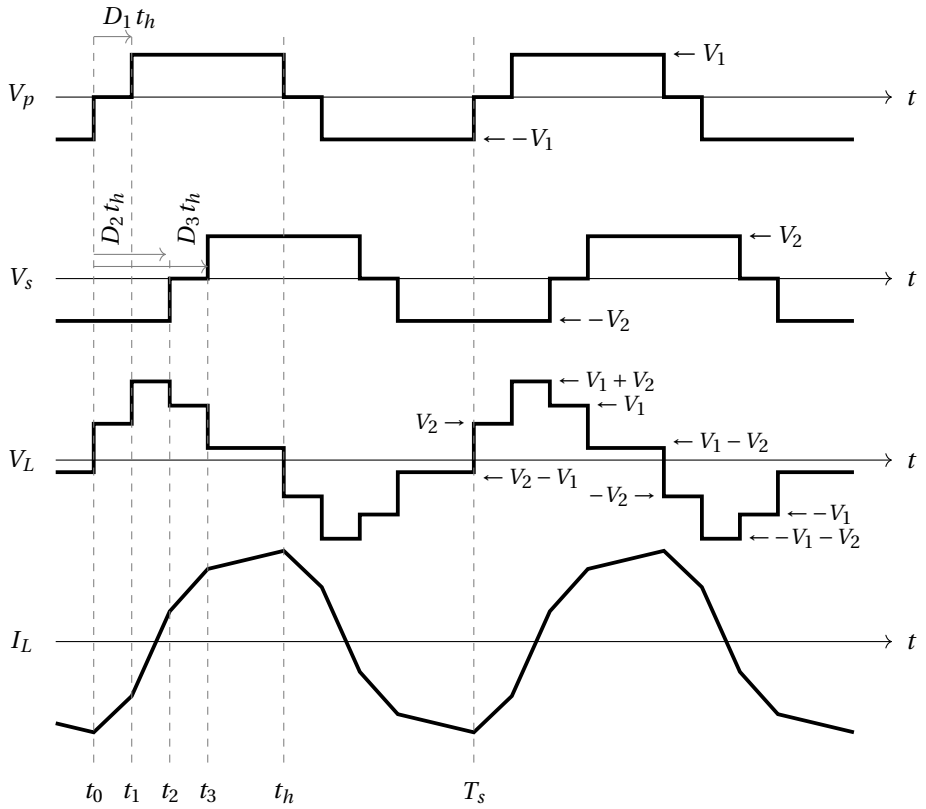


Figure 3.8: Switching patterns and inductor current for Triple Phase Shift Modulation. Where the following applies:$V_L = V_p - V_s$, $V_1 = V_{in}$, $V_2 = V_{out}/n$ and $t_h = 1/(2f_s)$

$$\begin{cases} V_2 & = L(I_1 - I_0)/(t_1 - t_0), \text{ where } t_0 \leq t < t_1 \\ V_1 + V_2 & = L(I_2 - I_1)/(t_2 - t_1), \text{ where } t_1 \leq t < t_2 \\ V_1 & = L(I_3 - I_2)/(t_3 - t_2), \text{ where } t_2 \leq t < t_3 \\ V_2 - V_1 & = L(I_0 + I_3)/(t_h - t_3), \text{ where } t_3 \leq t < t_h \end{cases} \tag{3.34}$$

Where:

$$\begin{aligned} t_0 &= 0 \\ t_1 &= D_1 t_h \\ t_2 &= D_2 t_h \\ t_3 &= (D_1 + D_2) t_h \\ V_1 &= V_{in} \\ V_2 &= V_{out}/n \\ A &= \frac{-V_2}{4Lf_s} \end{aligned}$$

Solving Equation 3.34 results in one equation for each of the current instances. The outcome for all the modes is presented in Table 3.7. Where I_x stands for the inductor current at time instance t_x.

The average output power can be derived by averaging the inductor current in Table 3.7 for the periods where the inductor is connected to the output terminals. The resulting power output for each D_1 and D_2 is shown in Figure 3.9 and is verified with the literature[35], [37]. The current output is verified for each mode using PLECS simulations. The error between the analytical equations and the simulation was on average 1.9%.

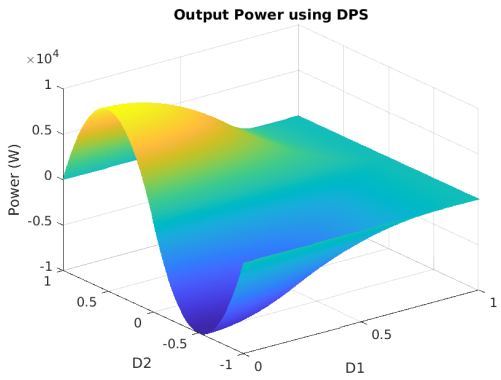


Figure 3.9: Power output for each D_1 and D_2 combination using DPS

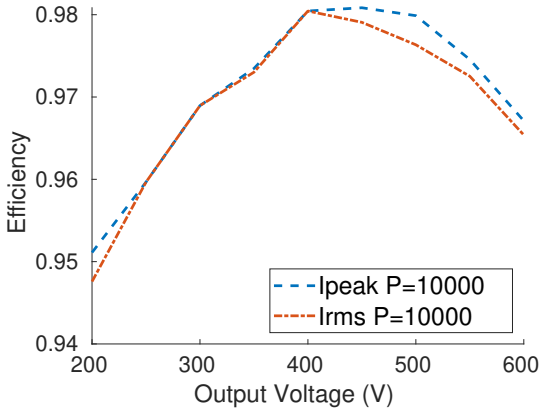


Figure 3.10: Efficiency comparison between I_{peak} optimization and I_{RMS} optimization using DPS modulation

Table 3.7: Inductor current and output power for all modes in Dual Phase Shift Modulation. Where $k = V_1/V_2$ and $A = -V_2/(4f_sL)$

	$D_1+D_2 \leq 1$		$D_1+D_2 > 1$	
	Mode 1 $D_1 \leq D_2$	Mode 2 $D_1 > D_2$	Mode 3 $D_1 \leq D_2$	Mode 4 $D_1 > D_2$
I_0	$A(k(1-D_1)+2D_2+D_1-1)$	$A(k(1-D_1)+2D_2+D_1-1)$	$A(k(1-D_1)-D_1+1)$	$A(k(1-D_1)-D_1+1)$
I_1	$A(k(1-D_1)+2D_2-D_1-1)$	$A(k(1-D_1)+D_1-1)$	$A(k(1-D_1)-D_1+1)$	$A(k(1-D_1)-D_1+1)$
I_2	$A(k(1+D_1-2D_2)+D_1-1)$	$A(k(1-D_1)+D_1-1)$	$A(k(1-D_1)+2D_2-D_1-1)$	$A(k(1-D_1)+D_1-1)$
I_3	$A(k(1-D_1-2D_2)+D_1-1)$	$A(k(1-D_1-2D_2)+D1-1)$	$A(k(1+D_1-2D_2)+D_1-1)$	$A(k(1-D_1)+D_1-1)$
P_{out}	$-AV_1(2D_2(1-D_2)-D_1^2)$	$-AV_1(D_2(2-D_2-2D_1))$	$-AV_1(1-D_2)(D_2-2D_1+1)$	$-AV_1(D_1-1)^2$

Optimization

Due to the introduction of the new control variable D_1, the operating point of the converter can be optimized to get the optimal combination of D_1 and D_2. In [37], the authors extend the DPS modulation by implementing various optimization strategies. The authors model the converter using three different optimization objectives; minimum reactive power, minimum peak current and minimum RMS current. The efficiency of the converter is compared over a wide voltage range for each of the optimization methods. Out of the three strategies, peak current optimization and RMS current optimization performed the best. In this project, both strategies are modeled using Matlab to confirm their performance over a wide output voltage range. The non-linear optimization problem for I_{peak} optimization is formulated in Equation 3.35.

$$\min\{I_{peak}(D_1,D_2)|D_1,D2 \in [0,1] \wedge P(D_1,D_2) = P*\} \tag{3.35}$$

The optimization problems can be solved numerically or analytically. For DPS modulation, the optimization is done numerically using the Matlab function fmincon. In Section 3.6, the analytical method is applied to TPS modulation. A similar method could be applied to DPS. Analytical optimization is preferred when it will be programmed into a microcontroller. For offline simulations, the numerical method will suffice.

The optimization problem is defined for mode 1. The procedure can be repeated for all modes. When considering the constraints applicable to mode 1, I_{peak} can be defined as I_0 for the whole region. Ultimately, the optimization problem in Matlab is shown in Equation 3.36.

$$\min_d \ I_{pk}(d) \ \text{such that} \begin{cases} P(d) & = P^* \\ A \cdot d & \leq b \\ d_{min} & \leq d \leq d_{max} \end{cases} \tag{3.36}$$

Where

$$d = [d_1, d_2]$$
$$C_{eq}(d) = A(2d_2(1-d_2) - d_1^2) - P^*$$
$$A = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}$$
$$b = [0, 1]$$
$$d_{min} = [0, 0]$$
$$d_{max} = [1, 1]$$

The optimization can now be solved in Matlab by running fmincon.

```
[d_o, i_o] = fmincon(@Ipk, d0, A, b, Aeq=[], beq=[], dmin, dmax, @C)
```

Where d_o and i_o are the optimal phase shift ratios and the achieved minimum peak current respectively. A similar optimization problem can be formulated for I_{rms}. The RMS current is defined by the piecewise RMS current as defined in Equation 3.37. Where N is defined as the number of linear sections in the inductor current.

$$I_{rms} = \sqrt{\sum_{n=1}^{N} \frac{1}{t_n - t_{n-1}} \int_{t_n}^{t_{n-1}} [I_L(t)]^2} \tag{3.37}$$

Both optimizations are tested in Matlab. In Figure 3.10, the efficiency is compared for both optimization strategies. The analysis shows a slight benefit of using peak current optimization over RMS current optimization, the optimization is most beneficial at low powers and high output voltages.

3.5. Extended Phase Shift

Extended Phase Shift (EPS), is a similar modulation as DPS. With EPS, the inner phase shift of only one bridge is changed. Different from DPS, where both the primary and secondary bridges will have an inner phase shift. This gives some extra flexibility in choosing which bridge will have the inner phase shift. EPS is introduced by Zhao, Yu, and Sun and can reduce a large amount of the reactive power that is present when using SPS modulation[38]. In [39], EPS is compared with other modulations. EPS modulation performed better than DPS modulation but not better than TPS modulation. For this reason, EPS will not be modeled. Instead, TPS is modeled in the next section.

3.6. Triple Phase Shift

By implementing Triple Phase Shift(TPS) modulation, all the bridges in the DAB converter have their unique phase shift. This method will enable another degree of freedom, by introducing a third phase shift D_3. D_3 is the phase shift between Q_1 and Q_c, which was previously bound to the sum of D_1 and D_2. The introduction of D_3 can further reduce peak and RMS currents compared to DPS[40]. The modulation is shown in Figure 3.8. TPS modulation can always provide the highest efficiency. The main reason for this is that SPS, DPS and EPS modulation are subsets of TPS. TPS can merge into SPS, DPS and EPS modulation in the following cases. For this reason, TPS is sometimes called Unified Phase Shift (UPS) modulation because it can unify all modulation strategies.

$$D_1 = 0, D_2 = D_3 \rightarrow SPS$$
$$D_3 = D_2 + D_1 \rightarrow DPS$$
$$D_1 = 0 | D_2 = D_3 \rightarrow EPS$$

Inductor Current

Like with DPS modulation, the inductor current is calculated to get a good insight into the total converter losses. The currents are derived using the same methods as in DPS modulation. TPS modulation consists of three modes[40]. In this report, the inner phase shifts between Q_1 and Q_3 and between Q_a and Q_c are considered to be strictly positive. This will limit the range of D_3 to only consider $D_2 \leq D_3$. The full list of inductor currents is shown in Table 3.8. The current waveforms are again verified using PLECS simulations.

Table 3.8: Inductor current and output power for all modes in Triple Phase Shift Modulation. Where $k = V_1 / V_2$ and $A = -V_2 / (4 f_s L)$

	Mode 1 $D_1 < D_2 \leq D_3$	Mode 2 $D_2 \leq D_1 \leq D_3$	Mode 3 $D_2 \leq D_3 \leq D_1$
I_0	$A(k(1-D_1)+D_2+D_3-1)$	$A(k(1-D_1)+D_2+D_3-1)$	$A(k(1-D_1)+D_2+D_3-1)$
I_1	$A(k(1-D_1)-2D_1+D_2+D_3-1)$	$A(k(1-D_1)-D_2+D_3-1)$	$A(k(1-D_1)-D_2+D_3-1)$
I_2	$A(k(1+D_1-2D_2)-D_2+D_3-1)$	$A(k(1-D_1)-D_2+D_3-1)$	$A(k(1-D_1)-D_2+D_3-1)$
I_3	$A(k(1+D_1-2D_3)-D_2+D_3-1)$	$A(k(1+D_1-2D_3)-D_2+D_3-1)$	$A(k(1-D_1)+2D_1-D_2-D_3-1)$
P_{out}	$-AV_1(-D_1+D_2+D_3-D_1^2-D_2^2-D_3^2+D_1D_2+D_1D_3)$	$-AV_1(-D_1+D_2+D_3+D_1D_3+D_3^2-D_1D_2)$	$-AV_1(-D_1+D_2+D_3+D_1^2-D_1D_2-D_1D_3)$

Optimization

In 2020, Hou and Li did an extensive review of many modulation and optimization strategies [39]. This review includes SPS, DPS, EPS and TPS modulation with different optimization strategies. The different control strategies are simulated for a wide operating voltage. From their comparison, TPS with Minimal Current Stress Optimization (MCSO) and Minimal RMS Current Optimization (MRMSCO) both performed the best.

An MCSO optimization has been proposed in multiple publications already. The authors in [41] propose an optimization using a 2-dimensional ergodicity method. This method shows a great reduction in peak power and an increase in efficiency over a wide voltage range. Hou, Song, and Wu present an optimization using the Lagrange Multiplier Method [40]. The MCSO proposed by [40] has an easy optimization method compared to the optimization of [41] and compared to the MRMSCO. Therefore this optimization will be the optimization of choice.

Hou, Song, and Wu use the Lagrange Multiplier Method (LMM) to optimize the peak power current and obtain equations for the optimal D_1, D_2 and D_3 based on the operating conditions[40]. This method is similar to the DPS optimization in Section 3.4 but the optimization is now done analytically instead of numerically.

The Lagrange Multiplier Method (LMM) is a commonly used method to find the local extremes of a function with constraints. In this case, the function to optimize is the peak current and the main constraint is the delivered output power. The LMM optimization expression for MCSO is shown in Equation 3.38. Where λ is the Lagrange Multiplier and p and p^* are the normalized output power and requested power respectively.

$$E = i_p + \lambda(p - p^*) \tag{3.38}$$

i_p is normalized by $I_N = \frac{V_2}{8 f_s L}$. The normalized current in Equation 3.39 is obtained by normalizing the peak current I_0 from Table 3.8. The output power can be normalized using the same method as shown in Equation 3.40.

$$i_p = 2(k(1-D_1)+D_2+D_3-1) \tag{3.39}$$

$$p = \frac{P_{out}}{P_N} \quad \text{where } P_N = \frac{V_1 V_2}{8 f_s L} \tag{3.40}$$

When filling in Equation 3.39 and 3.40 into Equation 3.35, the optimization problem can be solved using the LMM method. First, the gradient of Equation 3.38 is calculated. The gradient is set to 0 resulting in four equations. The equations can be solved for D_1, D_2, and D_3. Then, using the outcome of the system of equations, the constraints can be rewritten in terms of k and p. The full method is described in [40]. The resulting optimal solution is shown in Equation 3.42 and 3.43.

$$\nabla E = 0 \rightarrow \begin{cases} \frac{\delta E}{\delta D_1} &= 0 \\ \frac{\delta E}{\delta D_2} &= 0 \\ \frac{\delta E}{\delta D_3} &= 0 \\ \frac{\delta E}{\delta \lambda} &= 0 \end{cases} \rightarrow \begin{cases} -2k + 2\lambda(-1-2D_1+D_2+D_3) = 0 \\ 2 + 2\lambda(1-2D_2+D_1) = 0 \\ 2 + 2\lambda(1-2D_3+D_1) = 0 \\ 2(-D_1+D_2+D_3-D_1^2-D_2^2-D_3^2+D_1D_2+D_1D_3) - p^* = 0 \end{cases} \tag{3.41}$$

$$(k>1)\begin{cases}(0\le p^*<\frac{2(k-1)}{k^2}) & \begin{cases}D_1 &= 1-\sqrt{\frac{p^*}{2(k-1)}}\\ D_2 &= (k-1)(1-D_1)\\ D_3 &= D_1\end{cases}\\ (\frac{2(k-1)}{k^2}\ge p^*\le 1) & \begin{cases}D_1 &= (k-1)\sqrt{\frac{1-p^*}{(k^2-2k+2)}}\\ D_2 &= \frac{D_1(k-2)}{2(k-1)}+\frac{1}{2}\\ D_3 &= D_2\end{cases}\end{cases} \tag{3.42}$$

$$(k\le 1)\begin{cases}(0\le p^*<2(k-k^2) & \begin{cases}D_1 &= 1-\sqrt{\frac{p^*}{2k(1-k)}}\\ D_2 &= 0\\ D_3 &= kD_1-k+1\end{cases}\\ (2(k-k^2)\ge p^*\le 1) & \begin{cases}D_1 &= 0\\ D_2 &= \frac{1}{2}(1-\sqrt{\frac{1-p^*}{2k^2-2k+1}})\\ D_3 &= 2kD_2-D_2-k+1\end{cases}\end{cases} \tag{3.43}$$

The optimization method is programmed in Matlab and C to simulate it using Matlab and PLECS. In the next section, both DPS and TPS modulation will be compared to assess their performance.

3.7. Optimal Modulation

In Section 3.4 and 3.6, DPS and TPS modulation are introduced. In this section, a comparison is made between SPS, DPS and TPS. The modulations are compared by implementing them in the DAB model as defined at the beginning of this chapter. For both DPS and TPS, the optimization strategies are considered. Peak current optimization is used for DPS modulation and Minimum Current Stress Optimization (MCSO) is used for TPS modulation. In Figure 3.11, the output efficiencies for all the modulations are shown. The efficiency of the converter is calculated for three different output powers. At low output voltages, the converter is not capable of delivering high power. This is the reason why the voltage range is limited in the last two figures.

TPS modulation shows a clear advantage over SPS/DPS. TPS modulation has a high efficiency over the full output range. The advantage of TPS modulation is highest at high output voltage or low output power. Only when the voltage ratio between the primary and secondary sides are equal, the efficiency is equal to the SPS modulation. This is expected because both DPS and TPS modulation reduce to SPS when $k = 1$. TPS modulation can reduce power losses at high output voltages and with low output currents.

In Figure 3.12, the peak inductor currents are shown for each modulation. The peak currents are referred to the primary side of the transformer. TPS can achieve the lowest current stress in almost all situations.

In Figure 3.13, the ZVS region is shown for SPS, DPS using Peak current optimization, and TPS using MCSO. In the figures, the dark area represents the area where more bridges are in ZVS. In the light areas, the switching losses will be higher due to the lack of ZVS. The ZVS region is determined by the switch current. When the switch current is negative, the body diode of the switch will start conducting. This will limit the switch voltage to the forward voltage of the diode. When the switch current is positive, the voltage of the switching leg will always be equal to the input voltage or the output voltage for the primary and secondary side switches respectively.

When using SPS modulation, the converter can only achieve ZVS in all the switching legs when the voltage ratio is $k = 1$ or when the output power is high. DPS can achieve ZVS in a smaller region but at low output power, 3 of the 4 output bridges are still operating in ZVS. This will increase the overall efficiency of the converter.

TPS increases the ZVS region compared to SPS. Furthermore, at low output power, TPS with MCSO will reduce the inductor current to 0 in most switching instances. This improves efficiency because the switch will now operate with Zero Current Switching (ZCS). The ZCS region of the modulation is shown in Figure 3.15. When considering the ZVS and ZCS regions, TPS modulation is capable of switching with low losses, in almost all operating conditions.

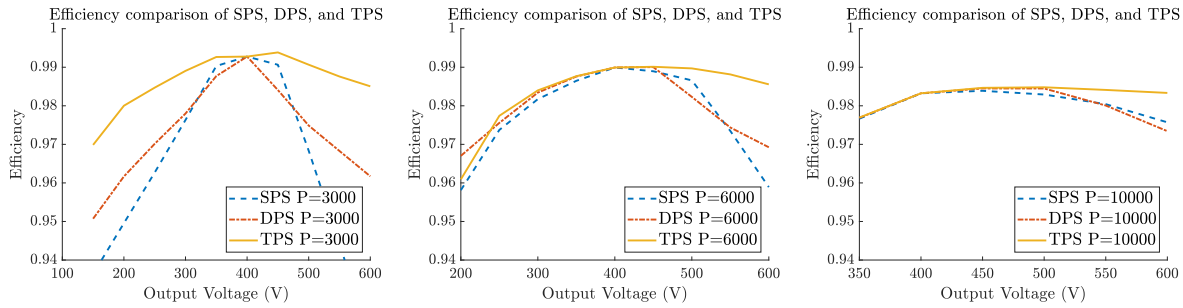
3.8. Bidirectional Control

The DAB converter is capable of bidirectional power-flow independent of the modulation type. SPS, DPS and TPS can all achieve bidirectional power. The power flow can be reversed by reversing the phase shift between

the primary and secondary bridge, as can be seen from Equation (3.7). In the case of TPS modulation, D_2 becomes negative and the inner phase shifts of the primary and secondary bridges swap. With a negative power flow, D_1 is the phase shift between Q_a and Q_c, D_2 is the phase shift between Q_a and Q_1, and D_3 is the phase shift between Q_a and Q_3. The reversal of the output current under TPS and MCSO is simulated using PLECS. In Figure 3.16 the output current is shown. The reference power is stepped down from 1000W to -1000W. The current can smoothly reverse direction.

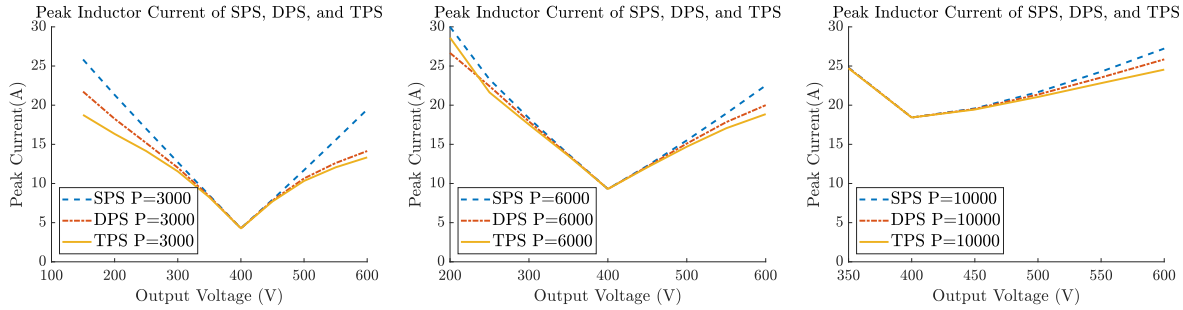
3.9. Conclusion

In this chapter, the Dual Active Bridge is introduced. The circuit components are designed and the losses are calculated analytically using Matlab. Then, the influence of modulation was evaluated. The efficiency of one single submodule can be improved greatly by implementing a more advanced modulation method. Triple Phase Shift (TPS) modulation with Minimum Current Stress Optimization (MCSO) is proven to be the most efficient modulation over a wide operating range. The modulation is tested using Matlab and PLECS, to show the benefits over DPS and SPS. TPS can improve efficiency in situations with low output power or high output voltage. The ZVS region is increased significantly and TPS reduces the switching current creating an additional ZCS region. TPS can operate with power flowing in both directions. The analytical equations for both TPS and MSCO are presented in this chapter.



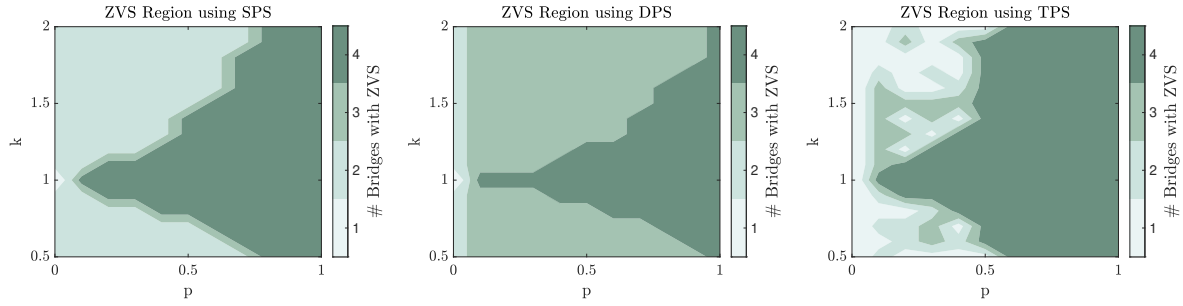
(a) $P_{out} = 3000W$ (b) $P_{out} = 6000W$ (c) $P_{out} = 10000W$

Figure 3.11: Output efficiencies of a DAB converter using SPS, DPS and TPS. Shown for the full output voltage range and three operating powers. Where $V_{in} = 750V$



(a) $I_{peak} = 3000W$ (b) $I_{peak} = 6000W$ (c) $I_{peak} = 10000W$

Figure 3.12: Peak inductor current when using SPS, DPS and TPS. Shown for the full output voltage range and three operating powers. Where $V_{in} = 750V$



(a) ZVS Region SPS (b) ZVS Region DPS (c) ZVS Region TPS

Figure 3.13: ZVS Regions when using SPS, DPS and TPS. Where $k = V_1 / V_2$ is the transfer ratio between the primary and the secondary side. And where p is the normalized output power.

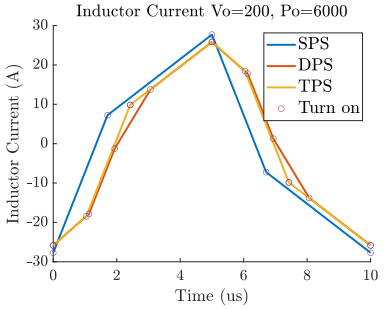


Figure 3.14: Inductor Current when $V_{in} = 750V, V_{out} = 200V, P_{out} = 6000W$

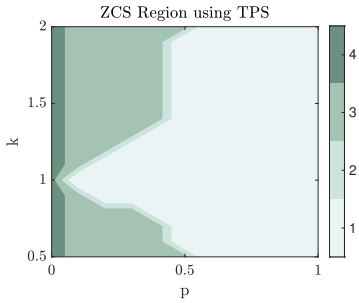


Figure 3.15: Range Where ZCS applies when using TPS and MCSO

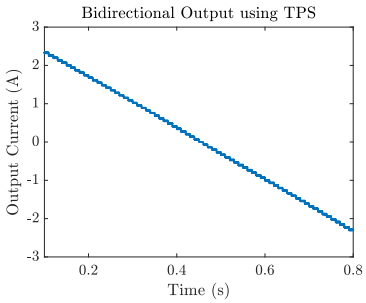


Figure 3.16: Reversing output current of a DAB using TPS and MCSO.

4

Smooth Transitioning

In this chapter, a new method of switchover is introduced and the following research question is answered.

> What topology and control methods can ensure smooth transitions, from series to parallel and vice versa, for two series-parallel-output DAB converters under live bidirectional power flow?

The goal of the switchover circuit is to ensure a smooth transition from series to parallel. This needs to be done without interruption of the output power and with minimal overshoot in the current or voltage. The switchover needs to be possible during live bidirectional power flow. The switchover circuit needs to have low losses to increase the efficiency of the complete circuit.

Firstly, the switchover circuit is discussed and the configuration of the output filter is determined. Then, a modulated switchover method is introduced to ensure a smooth transition. Finally, after modeling the new modulation scheme, the losses during a transition are analyzed.

4.1. Switchover Circuit

Converters with series-parallel output are not uncommon. Reconfiguration of the output can be done by using three switches, often relays. These relays can switch the outputs from series to parallel but they can not do so under live current. To overcome this, other types of switches can be used. In [11], Sun, Zhou, and Smedley introduced a converter with two outputs and a reconfigurable structure. A smooth switchover is done by making use of one Mosfet and two diodes to switch from series to parallel. The proposed circuit is shown in Figure 4.1. When the Q is open, the diodes conduct and the two converters are in parallel. When the Mosfet is closed, the current flows through the Mosfet and the diodes are reversed biased by the voltage from each output.

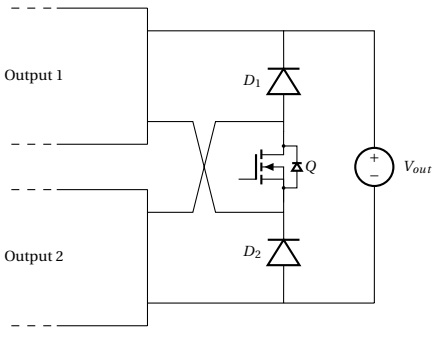


Figure 4.1: Switchover circuit used by Sun, Zhou, and Smedley [11]

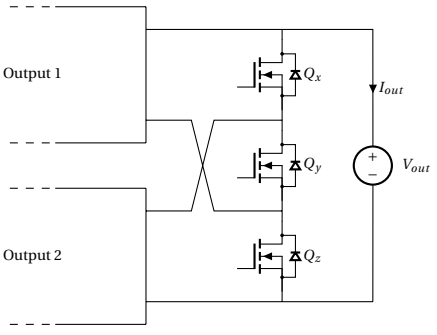
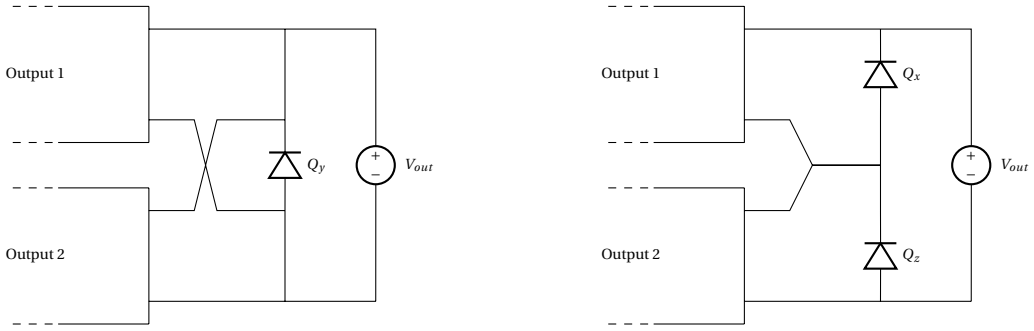


Figure 4.2: Proposed switchover circuit

This circuit allows transition under live current. The authors keep the output stable by adjusting the operating point of the converter at the same time the state of Q changes. It is possible to extend the method of [11] by replacing the two diodes with switches. This will make bidirectional power flow possible as the

Mosfets can conduct in both ways. The circuit is shown in Figure 4.2. When Q_x and Q_z are open and Q_y is closed, the two converters will be in series. Similarly, when Q_y is opened and Q_x and Q_z are closed, the converters will be in parallel as shown in Figure 4.3. When the gates of the switches are not driven and all switches are opened, the state of the switchover circuit depends on the current direction. When the current is positive, the converters will be in parallel, otherwise, they are in series. This effect is due to the bodydiodes. The bodydiodes — or other antiparallel diodes — are essential for the live transitioning of the converters. When the switches can block a current in both directions and no diode is present, the switches will either experience shoot-through or the output power will be cut off for a short amount of time. Since the output of the DAB converters is current-fed, this will result in high voltage spikes.



(a) Switchover circuit in parallel

(b) Switchover circuit in series

Figure 4.3: Switchover circuit in series and parallel

With the anti-parallel diodes present, a small dead time can be used to ensure a transition without shoot-through. In the next section, the output filter and its placement are discussed. In section 4.3, a 'hard' switchover is tested. This switchover method is similar to [11].

4.2. Output Filter

The placement of the output filter has a large influence on the operation and the performance of the switchover circuit. There are two possible positions for the output filter: before the switchover circuit, where each of the submodules will have its own filter capacitor. And behind the switchover circuit, where there will be a single filter on the output. In the next sections, the two possible positions are explained and compared. Then, the output filter is calculated.

Before The Switchover Circuit

When considering the control of the submodules, the easiest solution would be to give each submodule its own output capacitor. This way, the output voltage of each module is independent of the output circuit and the other module. The modules can be independently controlled and they can operate at any output power. Unfortunately, placing the output filter before the switchover circuit introduces new challenges for the switchover circuit. Firstly, when the output of the DAB is filtered by capacitors, the output becomes a voltage source. Because the characteristic of a battery is also a voltage source, large currents will flow during the transition of the output. This current flow can be limited by adding an inductor between the modules and the output capacitor but this will increase the losses significantly. Therefore, filtering on each of the submodules is not a good solution. A diagram of the solution is presented in Figure 4.4.

Behind the Switchover Circuit

Placing the output filter behind the switchover circuit — on the output of the converter — is an easy solution in terms of filter design. The filter can be made with only one single capacitor and there are no difficulties when switching from series to parallel. The circuit is shown in Figure 4.5. Although the filtering is simple, control of the two submodules will increase in complexity.

By having no capacitor connected to the output of the DAB submodules, the inductor current of both DAB converters will now be directly related to the state of the switchover circuit. In other words, when the converters are in series, the voltage V_2 — as defined in Chapter 3 — will now be $V_2/2$. Furthermore, the phase shifts of the two submodules need to be identical in series operation. Although the converters will be harder

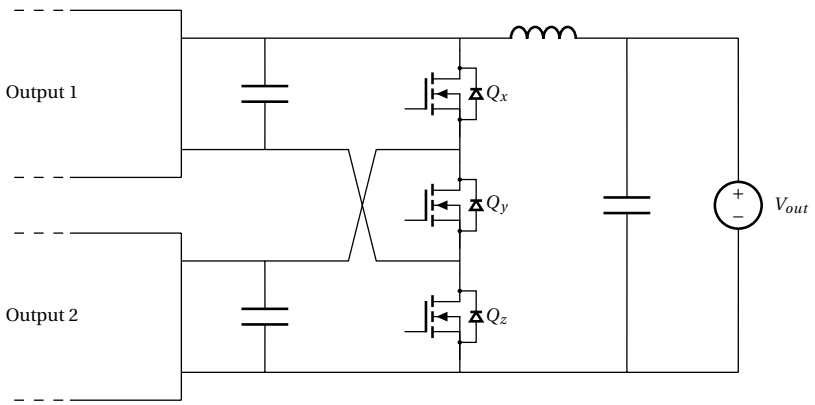


Figure 4.4: Output filter before the switchover circuit

to control, the benefit of low losses outweighs the drawbacks. The implications for the modulation will be discussed in section 4.4.

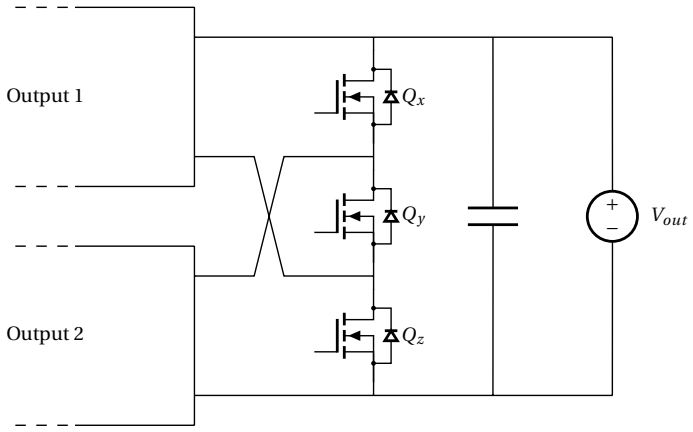


Figure 4.5: Output filter behind the switchover circuit

The output filter is calculated in a similar way as in Chapter 3 resulting in $C_{out} = 16\mu F$. Simulations are done with an output capacitance of $10\mu F$.

4.3. Hard Switchover

With a hard switchover, the switchover circuit is changed from parallel to series instantly. This kind of switchover is used in [11] and [26]. During this switchover, the output current will be returned to the reference current by adjusting the phase shift of the two converters.

When taking SPS as an example, the output power of the full converter can be written as

$$P_{out} = 2 \cdot \frac{V_{in} V_{mod} n}{2 f_s L} D(1-D) \tag{4.1}$$

Where V_{mod} is the output voltage of a single submodule.

$$V_{mod} = \begin{cases} V_{out} & \text{Parallel} \\ V_{out}/2 & \text{Series} \end{cases} \tag{4.2}$$

$$I_{mod} = \begin{cases} I_{out}/2 & \text{Parallel} \\ I_{out} & \text{Series} \end{cases} \tag{4.3}$$

The goal is to keep the output power and output voltage of the full converter at the same level after the transition. This can be done by changing D to a new operating point after the switchover. When transitioning

from parallel to series, the phase shift will be changed from D_{par} to D_{ser} at the same instance. Where D_{par} and D_{ser} are the phase shifts for parallel and series respectively.

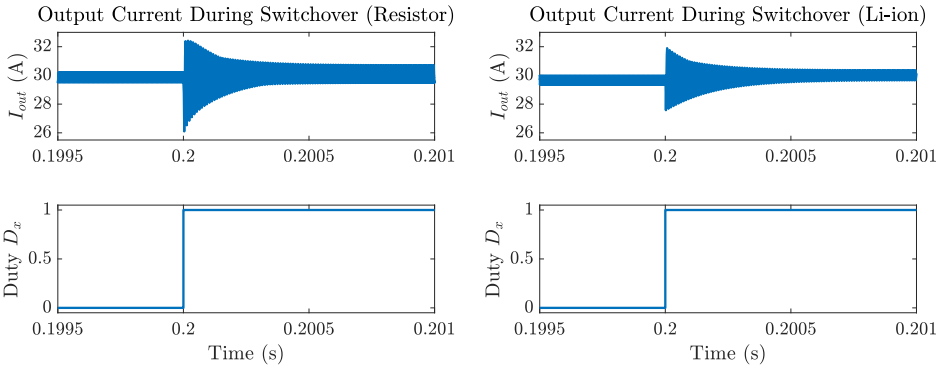
A switchover scenario is simulated using PLECS. The output of the converter will first be tested with a resistor. Then, the battery model is connected to the output. The output will be at 400V and the full converter will be delivering 30A. The operating points are calculated for series and parallel modes using MCSO. The operating points are shown in Table 4.1.

Shift	Parallel	Series
D_1	0	0.1815
D_2	0.0708	0.4613
D_3	0.1987	0.4613

Table 4.1: Operating points of the two submodules for series and parallel operation.

The output current oscillation is shown in Figure 4.6. When using a resistive load in combination with the calculated output filter of $20\mu F$, the current oscillation is 6A. The relative current deviation is 13%. When the switchover is tested with a battery model as defined in Section 3.3, the overshoot is reduced. The relative deviation of the current is now 7%.

An overshoot or undershoot of 7% is not desirable during a battery charging cycle. The output ripple could be improved by increasing the output capacitor or by replacing the output filter with a higher-order filter. Increasing the filter size will lead to higher losses and is therefore not desired too. Furthermore, the output ripple will still be highly dependent on the connected battery configuration. To overcome this ripple, the output state of the converter will need to transition more smoothly. In the next section, a modulated switchover method is introduced with this aim in mind.



(a) Resistive Load

(b) Li-ion battery load

Figure 4.6: Output current during switchover without control and with output filter and two different loads

4.4. Modulated Switchover

Although a live transition is already possible without any control, the large swing in the output current is not desirable. Rathore, Reddy, and Rajashekara introduce an isolated multilevel converter with hybrid resonant switching [25]. The authors use the same reconfigurable output circuit as [11] but they integrate the switch Q into the modulation. The authors use a PWM signal on the output switch to control the output state of the switchover circuit. The introduction of PWM on the output switches will add more flexibility in the control and allow for a smoother transition from parallel to series and vice versa. The PWM-modulated output circuit also gives rise to design constraints. In this section, the implications are discussed and, finally, the kind of modulation is chosen.

Impact on Inductor Current

Because the output filter is placed behind the switchover circuit, the state of the output circuit has a direct influence on the inductor current waveforms of the two submodules as the inductor voltage will change. When looking at the waveforms in Chapter 3.2, the voltage V_2 is now defined by Equation 4.4.

$$V_2 = V_{mod} \cdot n \tag{4.4}$$

Where V_{mod} is defined by Equation (4.2), and n is the turns ratio of the transformer.

This gives rise to restrictions on the modulation of the output circuit. Because the DC part of the inductor current will not contribute to power transfer through the transformer, the average DC current needs to equal 0. This can only be achieved if the inductor current is symmetric in the rising and falling part of the waveform. As the inductor current of each of the submodules needs to be symmetric, the output modulation needs to be symmetric within one period too.

$$I_{dc} = \frac{1}{T}\int_0^T I_L(t)dt = 0 \tag{4.5}$$

$$I_{dc} = \frac{1}{T_h}\int_0^{T_h} I_L(t)dt + \frac{1}{T_h}\int_{T_h}^{T} I_L(t)dt = 0 \tag{4.6}$$

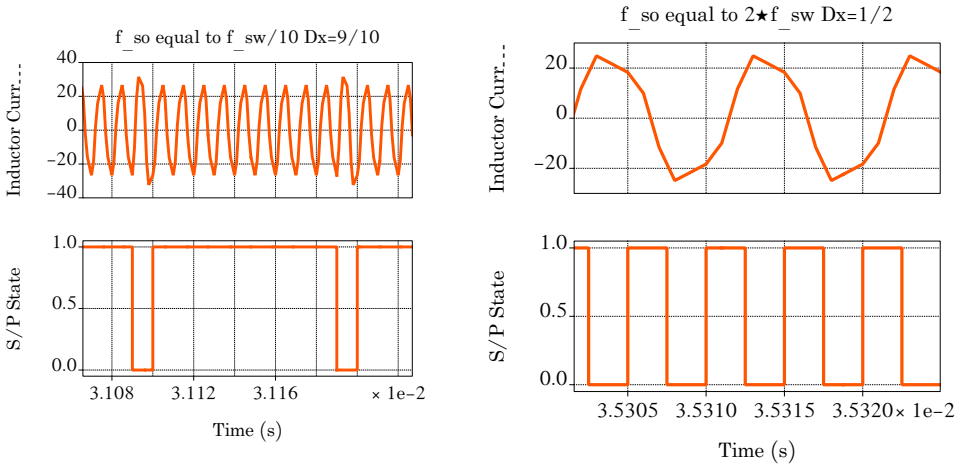
Equation (4.6) shows that the integral of the inductor current in the first half period needs to be equal to that of the second half period. Whenever a switchover is introduced by the output circuit, the inductor current changes shape because the effective inductor voltage is changed. To get a symmetric inductor voltage, either the full period needs to be in series/parallel or the switchover needs to happen identically in both half-periods. This can only be achieved in two ways, as discussed in the next two sections.

Lower Switchover Frequency

Firstly, f_{so} can be an integer divisor of f_{sw}. With this mode, the output circuit will be in series or parallel for a full period of the inductor current and a switch can only happen at the start of a new period. The on-time of the switchover circuit will then be limited to integer multiples of f_{so}. In other words, when $f_{so} = f_{sw}/n$ the dutycycle can be d_i/n. Where both n and d_i are integers, d_i is the integer dutycycle with $0 \leq d_i \leq n$. In Figure 4.7a, f_{so} is $f_{sw}/10$. The dutycycle is set at $d_i = 9$. It is shown in the figure that the inductor current has 9 periods of series operation and 1 period of parallel operation.

Higher Switchover Frequency

The second method is when $f_{so} = 2^n f_{sw}$. Where n is an integer higher than 0. With this modulation, the full period will be split into two or more equal parts. As the switchover happens similarly for both parts of the period, the inductor current stays symmetrical for the whole period. In Figure 4.7b, f_{so} is $2f_{sw}$ and the dutycycle is 50%. It can be seen that the inductor current stays symmetrical.



(a) Switchover frequency is lower than the switching frequency

(b) Switchover frequency is higher than the switching frequency

Figure 4.7: Inductor current of a single module and the switchover drive signal for two cases of switchover frequency

Comparison

Both methods have pros and cons. The first method is more efficient because it will lead to lower switching losses due to the lower switching frequency. Unfortunately, this benefit comes with the cost of losing flexibility in control. The resolution of the output will always be equal to n. n itself is limited too since a large n will introduce low-frequency components in the output current. For the case where n is 10, the output circuit will add 10kHz components to the output current when a switching frequency of 100kHz is used. This will require a larger filter design.

With the second method, the flexibility in control will offer a smoother transition but the losses during the transition will be higher due to the high switching frequency.

With all of the arguments considered, modulation with $f_{so} = 2f_{sw}$ is chosen. Although the losses are higher, the losses will only occur during the transition period. This period will be kept as short as possible. It might be worthwhile to still explore the case where $f_{so} = f_{sw}/n$ in the future.

4.5. Inductor Current

As mentioned before, the state of the output circuit now has a direct effect on the shape of the inductor current. The inductor current will get a new knee point at the instance where the output circuit switches from parallel to series and vice versa. The inductor current instances can be calculated with the same method as in Chapter 3. In this section, SPS with Switchover (SPSSO) modulation is introduced and the inductor current is calculated. The inductor current under SPSSO is shown in Figure 4.8. As can be seen in the figure, the inductor current changes shape due to the switching of the switchover circuit. The modulation uses two dutycycle values, D and D_x. As seen before D represents the phase shift between Q_1 and Q_a, relative to half the period t_h. D_x is a new variable that represents the relative duration of the series mode. SPSSO modulation will be defined as shown in Figure 4.8.

The switchover circuit will switch from parallel to series at time t_0. After the period $D_x t_h$ has passed, the output circuit will transition back to parallel. The voltage at the terminals of one submodule can now be defined as

$$V_{mod} = \begin{cases} V_{out}/2 & t_0 < t < D_x t_h \\ V_{out} & D_x t_h < t < t_h \end{cases}$$

Where SPS has only one possible operating mode, SPSSO now has two. The two modes are caused by the order of the two time instances. The modes are defined as mode 1 and mode 2 and the inductor current shown in Figure 4.8 is mode 1.

- Mode 1: $D_x \leq D$
- Mode 2: $D_x > D$

The inductor current can be determined by creating a system of equations for the different sections in the inductor current, which is a piecewise linear waveform. When analyzing the inductor voltage for mode 1 as shown in Figure 4.8, the inductor voltage can now be defined as

$$V_L = V_p - V_s = \begin{cases} V_1 + V_2/2 & t_0 \leq t < t_1 \\ V_1 + V_2 & t_1 \leq t < t_2 \\ V_1 - V_2 & t_2 \leq t < t_h \end{cases} \tag{4.7}$$

Where $V_1 = V_{in}$ and $V_2 = n \cdot V_{out}$. And where $t_0 = 0$, $t_1 = D_x t_h$, $t_2 = D t_h$, and t_h is half the period. The inductor currents can be calculated by relating the inductor voltage to the change in current.

$$V_1 + V_2/2 = L\frac{I_1 - I_0}{t_1 - t_0} \tag{4.8}$$

$$V_1 + V_2 = L\frac{I_2 - I_1}{t_2 - t_1} \tag{4.9}$$

$$V_1 - V_2 = L\frac{-I_0 - I_2}{t_h - t_2} \tag{4.10}$$

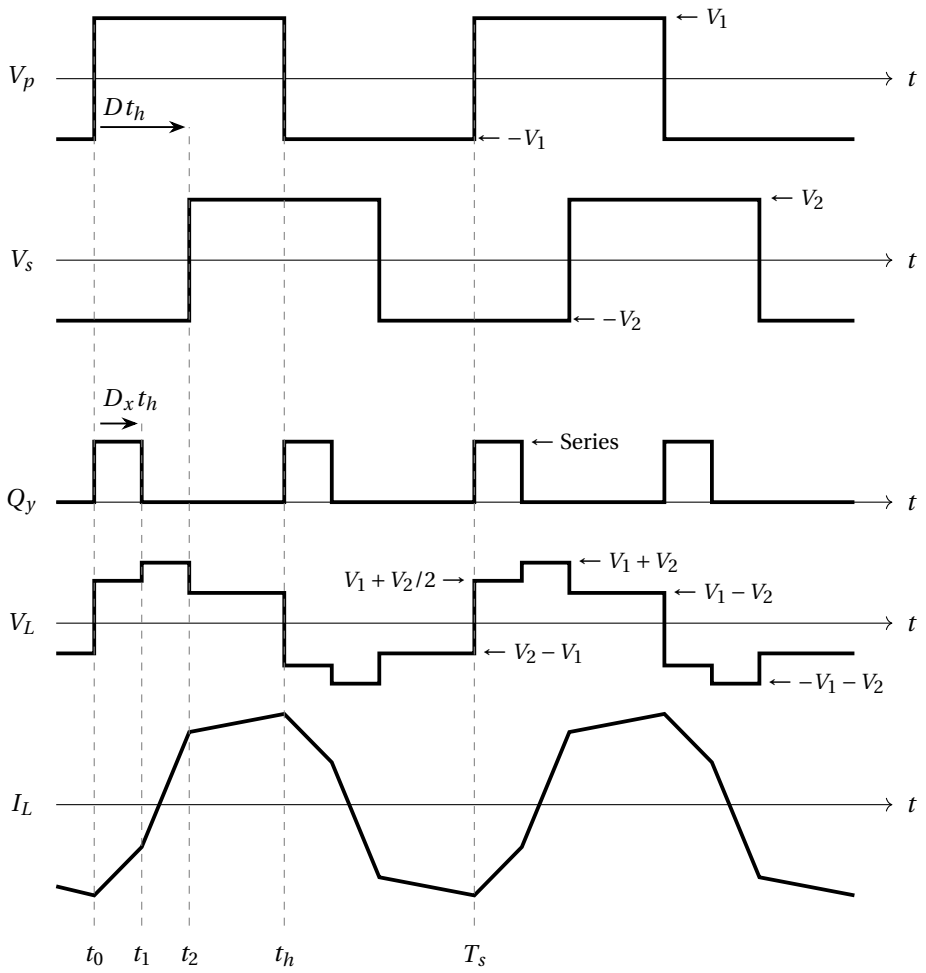


Figure 4.8: Switching and Inductor current with SPSSO

The system of equations can be solved as there are three equations and three unknowns. The resulting inductor currents are defined by Equations 4.11 - 4.16.

Mode 1 $(0 \le D_x \le D \le 1)$:

$$I_0 = A(2V_1 - 2V_2 + 4DV_2 - D_xV_2) \tag{4.11}$$
$$I_1 = A(2V_1 - 2V_2 + 4DV_2 - 4D_xV_1 - 3D_xV_2) \tag{4.12}$$
$$I_2 = A(2V_1 - 2V_2 - 4DV_1 + D_xV_2) \tag{4.13}$$

Mode 2 $(0 \le D < D_x \le 1)$:

$$I_0 = A(2V_1 - 2V_2 + 2DV_2 + D_xV_2) \tag{4.14}$$
$$I_1 = A(2V_1 - 2V_2 - 4DV_1 + D_xV_2) \tag{4.15}$$
$$I_2 = A(2V_1 - 2V_2 - 2DV_2 + 4D_xV_1 - 3D_xV_2) \tag{4.16}$$

Where $A = \frac{-1}{8f_sL}$.

It can be verified that the current equations will fold back into SPS modulation when the output circuit is purely parallel ($D_x = 0$). When the output is in series ($D_x = 1$), the inductor equations become equal to the SPS modulation where V_2 is now $V_2/2$.

These equations for the inductor current can now be used to determine the average output current and eventually, they can be used to determine the control signal needed to keep the output current stable during transition.

4.6. Output Current

The output current — and with that the output power — can be calculated by taking the average output current of the full converter. The output current of a single submodule (I_{mod}) is equal to I_L when Q_a and Q_d are on and equal to $-I_L$ when Q_b and Q_c are on. Furthermore, the output current is $2I_{mod}$ when the output is in parallel. When taking this into consideration, the output current for mode 1 can be defined as in Figure 4.9.

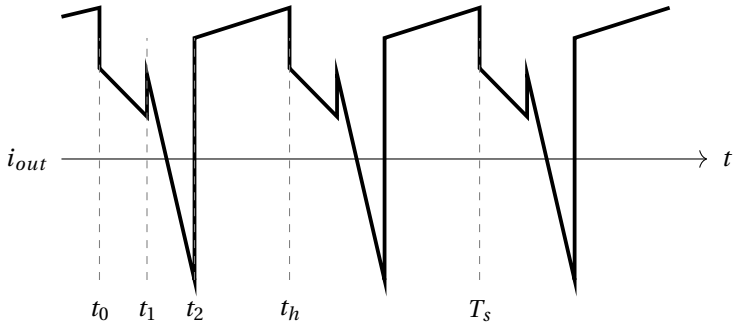


Figure 4.9: Output current with SPSSO

The average output current can now be calculated by averaging the linear parts during half the period.

$$I_{out} = \frac{1}{t_h}\int_0^{t_h} i_L(t)\,dt$$

The current integral can be split into three regions, U_1, U_2, and U_3.

$$I_{out} = \frac{1}{t_h}\left(\int_0^{t_1} i_L(t)\,dt + \int_{t_1}^{t_2} i_L(t)\,dt + \int_{t_2}^{t_h} i_L(t)\,dt\right) = \frac{1}{t_h}(U_1 + U_2 + U_3) \tag{4.17}$$

The integral of each region can be calculated as the integral of a trapezoid as defined in Equation 4.18.

$$U_n = \frac{1}{2}(i_L(t_n) + i_L(t_{n-1})) \cdot (t_n - t_{n-1}) \tag{4.18}$$

Resulting in the following integrals.

$$U_1 = \frac{1}{2}(-I_0 - I_1)D_x t_h \tag{4.19}$$

$$U_2 = \frac{1}{2}(-2I_1 - 2I_2)(D - D_x)t_h \tag{4.20}$$

$$U_3 = \frac{1}{2}(2I_2 - 2I_0)(1 - D)t_h \tag{4.21}$$

The integrals can be added together to obtain one equation for the output current. In Equation 4.22 the output current is presented for mode 1.

$$I_{out} = \frac{nV_1}{4f_sL}\left(-4D^2 + D_x^2 + 4D - D_x\right) \quad (0 \le D_x \le D \le 1) \tag{4.22}$$

The same can be done for mode 2, resulting in Equation 4.23.

$$I_{out} = \frac{nV_1}{4f_sL}\left(-2D^2 - D_x^2 + 2D + D_x\right) \quad (0 \le D < D_x \le 1) \tag{4.23}$$

As with a single DAB converter, the output current does not depend on the output voltage even with the switchover circuit in place. The resulting current equations are validated via PLECS simulations. The output currents can be normalized by defining a normal current I_N as two times the nominal current of a single submodule.

$$I_N = 2\frac{V_1 n}{8f_sL} = \frac{V_1 n}{4f_sL} \tag{4.24}$$

$$I_{out} = \begin{cases} I_N\left(-4D^2+4D+D_x^2-D_x\right) & (0 \le D_x \le D \le 1) \\ I_N\left(-2D^2+2D-D_x^2+D_x\right) & (0 \le D < D_x \le 1) \end{cases} \tag{4.25}$$

The maximum output current is reached when $D = 0.5$ and $D_x = 0$, the maximum output current is exactly twice the current from one single DAB converter.

$$I_{max} = \frac{V_1 n}{4 f_s L} \quad (D_x = 0, D = 0.5) \tag{4.26}$$

In the period that $D < D_x \le 1$ the maximum output current depends on the state of D_x. The peak will be reached when $D = 0.5$ and $D_x = 0.5$, then the output current is then 1.5 times higher than the output current of a single DAB. It can also be observed that when $D_x = 1$ the maximum output current is reduced to $0.5 I_{max}$.

4.7. Phase Shift Control

The resulting output current can be used to get an equation for the needed phase shift D for a given D_x and a required output current I^*_{out}. This will make sure that the output current can be stably controlled even during a transition. To make the equations more readable, the required output current is first normalized to $i^* = I^*_{out}/I_N$. Then the equation for the output current can be reversed for each mode. The following equation results for mode 1.

$$D^* = \frac{1}{2} - \frac{1}{2}\sqrt{1 + D_x^2 - D_x - i^*} \tag{4.27}$$

The required phase shift in mode 2 can be calculated similarly.

$$D^* = \frac{1}{2} - \frac{1}{2}\sqrt{1 - 2D_x^2 + 2D_x - 2i^*} \tag{4.28}$$

The reference D^* is now fully defined as

$$D^* = \begin{cases} \frac{1}{2} - \frac{1}{2}\sqrt{1 + D_x^2 - D_x - i^*} & (0 \le D_x \le D \le 1) \\ \frac{1}{2} - \frac{1}{2}\sqrt{1 - 2D_x^2 + 2D_x - 2i^*} & (0 \le D < D_x \le 1) \end{cases} \tag{4.29}$$

Where $i^* = I^*_{out}/I_N$.

4.8. Bidirectional Current

Until now, the current was assumed to be positive and more importantly the phase shift D was assumed to be positive. When the phase shift D is allowed to go negative, two more modes need to be considered in the modulation. D_x will always be positive. The third mode is defined as $D < 0$ and $D_x \le D + 1$. In other words, the dutycycle D_x is lower than the falling edge of V_s in Figure 4.8. In mode 4, the falling edge of V_s comes before D_x.

The inductor current can again be calculated for the two added modes.

Mode 3 $(D_x \le D + 1 < 1)$:

$$I_0 = A(2V_1 - 2V_2 - 4DV_2 + D_x V_2) \tag{4.30}$$
$$I_1 = A(2V_1 - 2V_2 - 4DV_2 - 4D_x V_1 + 3D_x V_2) \tag{4.31}$$
$$I_2 = A(2V_2 - 2V_1 - 4DV_1 - D_x V_2) \tag{4.32}$$

Mode 4 $(D + 1 < D_x \le 1)$:

$$I_0 = A(2V_1 - 2DV_2 - D_x V_2) \tag{4.33}$$
$$I_1 = A(2V_2 - 2V_1 - 4DV_1 - D_x V_2) \tag{4.34}$$
$$I_2 = A(2V_1 + 4V_2 + 2DV_2 - 4D_x V_1 - 3D_x V_2) \tag{4.35}$$
$$\tag{4.36}$$

Where $A = \frac{-1}{8 f_s L}$.

The inductor current is integrated to get the output current. Eventually, the output current is used to get the necessary phase shift D. This method is similar to the method used for modes 1 and 2.

$$I_{out} = \begin{cases} I_N\left(4D^2+4D-D_x^2+D_x\right) & (D_x \le D+1<1) \\ I_N\left(2D^2+2D+D_x^2-D_x\right) & (D+1 \le D_x \le 1) \end{cases} \tag{4.37}$$

$$D^* = \begin{cases} -\frac{1}{2}+\frac{1}{2}\sqrt{1+D_x^2-D_x+i^*} & (D_x \le D+1<1) \\ -\frac{1}{2}+\frac{1}{2}\sqrt{1-2D_x^2+2D_x+2i^*} & (D+1 \le D_x \le 1) \end{cases} \tag{4.38}$$

4.9. Mode Boundaries

The modes are now defined by the relation between D and D_x but these values are not known beforehand. It is therefore useful to calculate the boundaries of all the modes in terms of the known values D_x and i^*. The valid region for Mode 1 can be calculated by filling in Equation 4.27 into the boundary inequality $D_x \le D$.

$$D_x \le D^* \tag{4.39}$$

$$D_x \le \frac{1}{2}-\frac{1}{2}\sqrt{1+D_x^2-D_x-i^*} \tag{4.40}$$

$$i^* \ge \begin{cases} 3(D_x-D_x^2) & (D_x \le 0.5) \\ 2-5(D_x-D_x^2) & (D_x > 0.5) \end{cases} \tag{4.41}$$

The same can be done for all the modes resulting in a set of boundaries for all the modes in the modulation. In Table 4.2 all the calculated boundaries are presented. The boundaries only depend on i^* and D_x. With the boundaries the limits $0 \le D_x \le 1$ and $-1 \le i^* \le 1$ are considered.

Table 4.2: Boundaries of the modes in SPSSO

Mode	Lower Bound	Upper Bound
Mode 1	$i^* \ge 3(D_x-D_x^2)$ for $(D_x \le 0.5)$	$i^* < 1$
	$i^* \ge 2-5(D_x-D_x^2)$ for $(D_x > 0.5)$	
Mode 2	$i^* \ge D_x-D_x^2$	$i^* < 3(D_x-D_x^2)$ for $(D_x \le 0.5)$
		$i^* < 1-(D_x-D_x^2)$ for $(D_x > 0.5)$
Mode 3	$i^* \ge -2+5(D_x-D_x^2)$ for $(D_x \le 0.5)$	$i^* < D_x-D_x^2$
	$i^* \ge -3(D_x-D_x^2)$ for $(D_x > 0.5)$	
Mode 4	$i^* \ge -1$	$i^* \le -1+(D_x-D_x^2)$ for $(D_x \le 0.5)$
		$i^* \le -3(D_x-D_x^2)$

4.10. Final Definition of SPSSO

With the new mode boundaries calculated, it is possible to write a full definition of the SPSSO modulation control. This method can be programmed into simulation, Matlab and eventually a microcontroller.

$$\begin{aligned} D_x \le 0.5 & \begin{cases} D = \frac{1}{2}-\frac{1}{2}\sqrt{1+D_x^2-D_x-i^*} & 3(D_x-D_x^2) \le i^* \le 1 \\ D = \frac{1}{2}-\frac{1}{2}\sqrt{1-2D_x^2+2D_x-2i^*} & D_x-D_x^2 \le i^* < 3(D_x-D_x^2) \\ D = -\frac{1}{2}+\frac{1}{2}\sqrt{1+D_x^2-D_x+i^*} & D_x-D_x^2-1 \le i^* < D_x-D_x^2 \\ D = -\frac{1}{2}+\frac{1}{2}\sqrt{1-2D_x^2+2D_x+2i^*} & -1 \le i^* < D_x-D_x^2-1 \end{cases} \\ D_x > 0.5 & \begin{cases} D = \frac{1}{2}-\frac{1}{2}\sqrt{1-D_x^2-D_x-i^*} & 1-D_x+D_x^2 \le i^* \le 1 \\ D = \frac{1}{2}-\frac{1}{2}\sqrt{1-2D_x^2+2D_x-2i^*} & D_x-D_x^2 \le i^* < 1-D_x+D_x^2 \\ D = \frac{1}{2}+\frac{1}{2}\sqrt{1+D_x^2-D_x+i^*} & -3(D_x-D_x^2) \le i^* < D_x-D_x^2 \\ D = \frac{1}{2}+\frac{1}{2}\sqrt{1-2D_x^2+2D_x+2i^*} & -1 \le i^* < -3(D_x-D_x^2) \end{cases} \end{aligned} \tag{4.42}$$

4.11. Verification

In the last sections, a new SPSSO modulation is presented that can incorporate the switchover circuit into the modulation. All the equations in this section are validated using PLECS simulations to verify their correctness. The new modulation can be used to simulate the two submodules with the switchover circuit. The inductor current and output current waveforms are verified for both modes. The waveforms are shown in Figure 4.12. A full transition is also simulated in PLECS. The requested current was kept stable at 30A while the switchover dutycycle D_x was changed from 0 to 1. The resulting output current during the switchover is shown in Figure 4.10. The maximum deviation from the setpoint is 1.5%. In Figure 4.11, the maximum output current is shown during a transition. It is shown that the output reduces from I_N to $I_N/2$ when transitioning from parallel to series. This is exactly as expected as the output current is doubled in parallel operation.

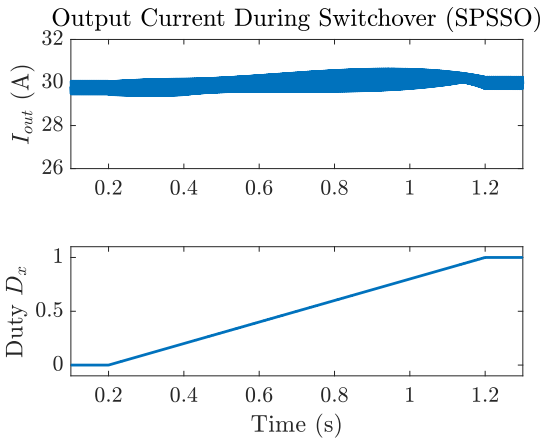


Figure 4.10: PLECS Simulation of the Output Current using SPSSO during Switchover $V_{out} = 400V$ and $I^*_{out} = 30A$

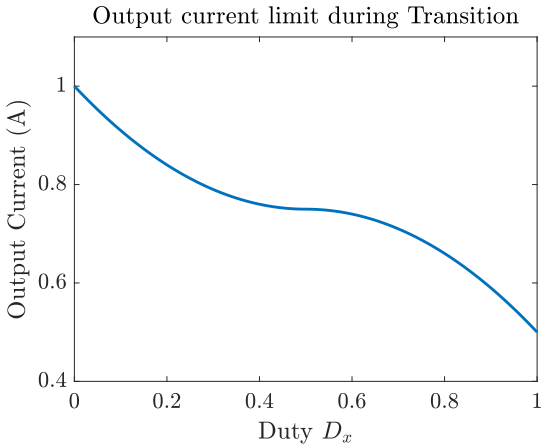


Figure 4.11: Current limit during transition

4.12. Dead Time

When using the switchover circuit from Figure 4.2 it is necessary to implement a small deadtime before the switches turn on. This dead time will prevent the current from shooting through and shorting the output bus. During the deadtime period, none of the output switches are conducting and the power will be temporarily conducted by the body diodes of the Mosfets. Due to the arrangement of the switches, the direction of the current will determine the output state of the converter during the deadtime period. Whenever the output current I_{out} is positive and all the switches are opened, the converter will be in parallel since the bodydiode of Q_y can not conduct the negative current. In contrast, whenever the output current is negative, the converters will be in series since the bodydiodes of Q_x and Q_z are blocking.

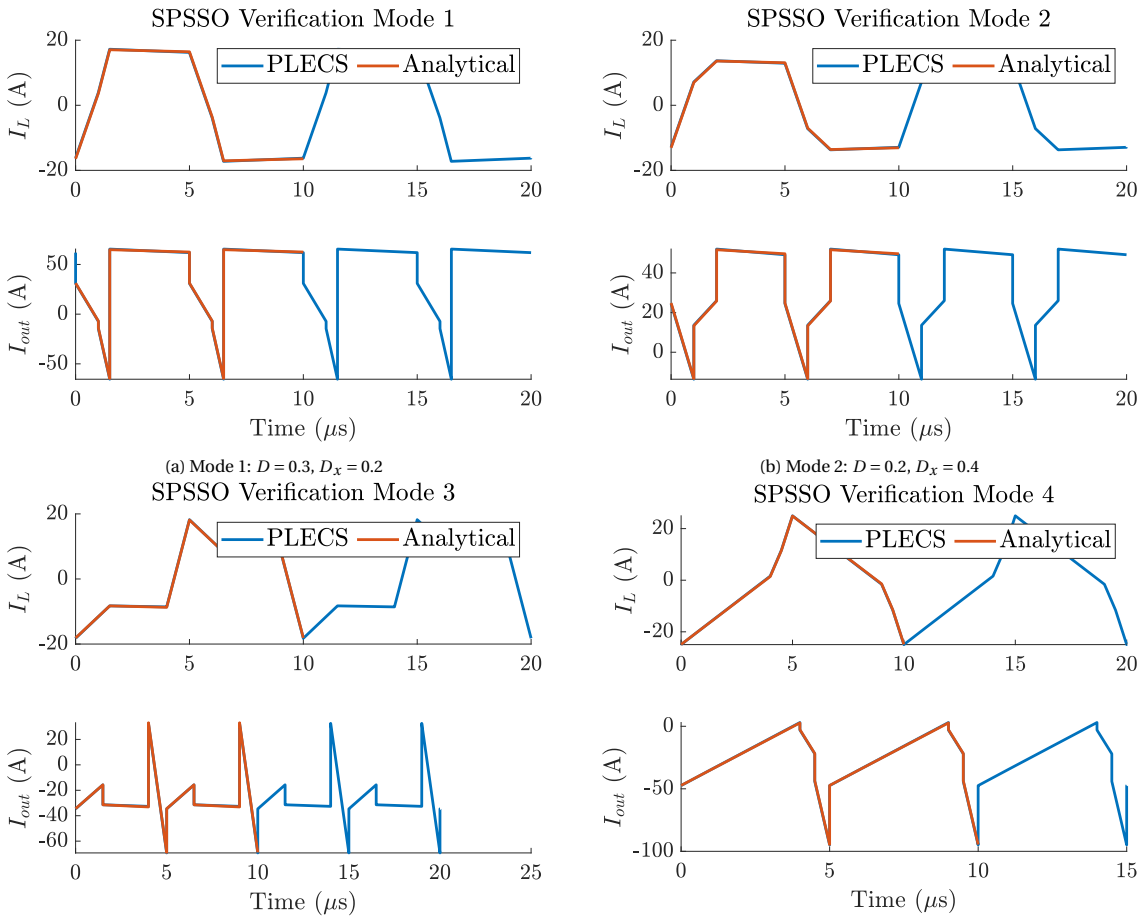
The effect of these small deadtimes introduces inaccuracy in the presented SPSSO model. Because the deadtime is relatively small, the effect will be neglected.

4.13. Output Circuit Losses

With the model presented above, it is now possible to calculate the losses in the output circuit accurately. The losses in the output circuit consist of two parts; conduction losses and switching losses. In this section, the output filter losses are not considered.

Conduction Losses

The switches in the switchover circuit add extra resistance to the conduction path. When the output circuit is stationary, the conduction losses can be calculated by simply using the $R_{ds,on}$ value from the datasheet in combination with the RMS output current. The RMS output current is calculated from Figure 4.9. In this case, D_x is either 0 or 1 and the output current collapses back into SPS modulation for which the output current is shown in Figure 3.4.



(a) Mode 1: $D = 0.3$, $D_x = 0.2$

(b) Mode 2: $D = 0.2$, $D_x = 0.4$

(c) Mode 3: $D = -0.2$, $D_x = 0.3$

(d) Mode 4: $D = -0.2$, $D_x = 0.9$

Figure 4.12: PLECS Verification of the analytical model for all possible modes. $V_{out} = 400V$, $V_{in} = 750V$

$$I_{RMS} = \sqrt{\frac{1}{t_h}\int_0^{t_h} (i_{out}(t))^2 dt} \tag{4.43}$$

The output losses are calculated for a few different operating points. The C3M0016120K switches are used for the loss calculations. The losses are shown in Table 4.3.

Table 4.3: Conduction losses in the switchover circuit for different operating points

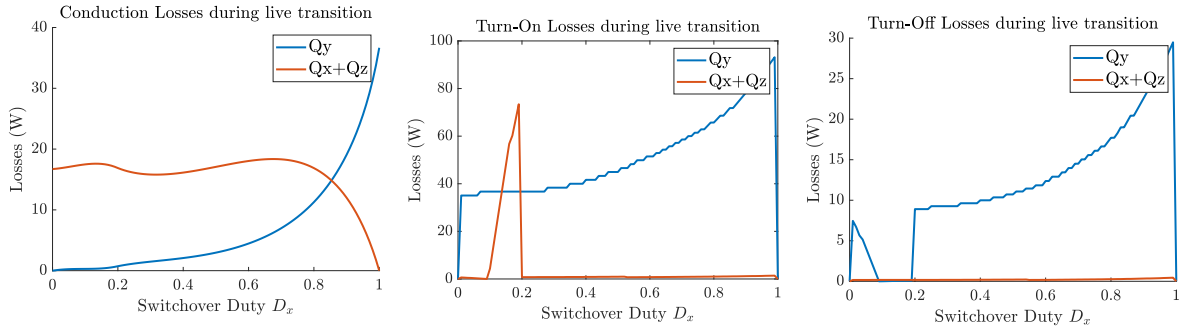
Mode	Output Power	Switch	Loss total
Parallel	25kW	$Q_x + Q_z$	134 W
Series	12.5kW	Q_y	43 W
Parallel	12.5kW	$Q_x + Qz$	18 W

As can be seen from the table, the losses in Q_y are approximately two times as high as the losses in the parallel switches Q_x and Q_z. The losses in the parallel switches are lower because the equivalent resistance of the two switches is half. When the converter is in transition, the output power will be divided by the three switches. Part of the output current will be fed by Q_y and another part by Q_x and Q_z. The RMS current through one of the switches can be calculated by integrating the current through that particular switch. The output current is fed by Q_y between time instances t_0 and $D_x t_h$. The rest of the current will flow through Q_x and Q_z. In Figure 4.13a, the losses are shown for a full transition. The x-axis represents the dutycycle D_x. As expected, the conduction losses in Q_y increase exponentially with a rising D_x. The conduction losses in $Q_x + Q_z$ start around 18W and stay stable. This is counterintuitive as the losses should also drop exponentially with an increasing D_x. The reason for the plateau in the conduction losses is due to the rise in instantaneous

current during the transition. When D_x rises, the peak inductor current rises too, causing the effective RMS current to stay stable.

Switching Losses

The switching losses are caused by switching the switchover circuit from series to parallel and vice versa. When D_x is 1 or 0 the output circuit is stationary and no switching losses are present. For dutycycles in between 0 and 1, the switching losses can be calculated using a similar method as described in Section 3.2. The turn-on and turn-off losses are calculated by taking the current at the moment of switchover. The switching voltage depends again on the direction of the current. If the current is flowing in a positive direction — against the direction of the bodydiode —, the switch voltage is equal to the output voltage. When the output current is flowing in a negative direction, the switch voltage is equal to the forward voltage of the bodydiode. In Figure 4.13, the switching losses for Q_y and $Q_x + Q_z$ are presented. The losses in Q_y are significantly higher since this switch carries higher currents and since the switches Q_x and Q_z are operating in ZVS most of the time. Q_x and Q_z are operating at ZVS because the output current of the submodules is positive when they turn on and off. Only in the region between $D_x = 0.1$ and $D_x = 0.2$ the output current is negative during turn-on causing the turn-on losses in Q_x and Q_z to rise. At the same time, the turn-off losses in Q_y drop since the current through this switch is negative in that period. The turn-on losses in Q_y can be reduced by shifting the dutycycle of the output circuit. This will be discussed in Section 4.14.



(a) Conduction losses during switchover with SPSSO with $V_{out} = 400V$ and $P_{out} = 12kW$

(b) Turn-on losses

(c) Turn-off losses

Figure 4.13: Losses during switchover with SPSSO with $V_{out} = 400V$ and $P_{out} = 12kW$

Reverse Recovery Losses

Reverse recovery is the phenomenon happening in the body diode when the diode switches from the conducting to the blocking state. During the reverse recovery time (T_{rr}), the charge is built up in the diode junction. In the case of the switchover circuit, the reverse recovery losses can be examined for both transitions. When the output circuit is switching from parallel to series with a positive output current, the bodydiodes in Q_x and Q_z are carrying current due to the inserted dead time. The reverse recovery charges $Q_{rr,x}$ and $Q_{rr,z}$ have to build up before the diodes will start blocking. To calculate those losses, the charge from the datasheet of the chosen switches can be used together with the switching frequency.

$$P_{rr} = Q_{rr} \cdot f_{so} \tag{4.44}$$

Loss Comparison with SPS

To verify the loss model and the model of SPSSO modulation, the modulation is compared against regular SPS. One converter is simulated with SPS and the output circuit for a stationary series and parallel operation. Then a converter using SPS is simulated for half the output current in parallel and half the output voltage in series. These simulations result in Figure **??**. It can be seen that the output losses are higher for the SPSSO circuit due to the conduction losses in the output switches. When the converters are in parallel, the losses are high at low output voltages because the output RMS current is higher at these operating points.

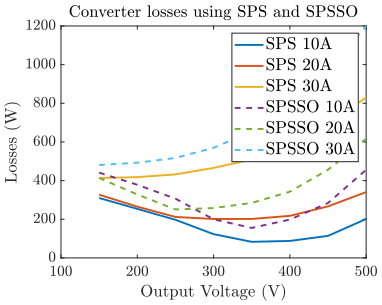


Figure 4.14: Output Losses for SPS and SPSSO modulation in series mode for different output currents and different output voltages.

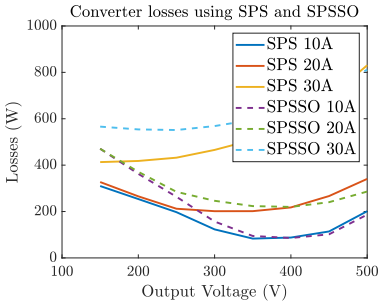


Figure 4.15: Output Losses for SPS and SPSSO modulation in parallel mode for different output currents and different output voltages.

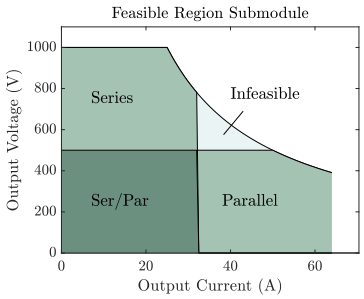


Figure 4.16: The feasible region where the converter can operate

4.14. ZVS Condition

In some cases, the bodydiodes create a ZVS condition during turn-on or turn-off. When the current I_{out} is positive and the circuit transitions from series to parallel, a ZVS turn-on transition is achieved in the switches Q_x and Q_z. Whenever the current is negative, ZVS is achieved at turn-on in Q_y while switching from parallel to series. It is possible to take advantage of this effect in the modulation of the output circuit. When looking at the output current of a single converter, as shown in Figure 4.9, the output current reaches a negative value before the secondary bridge switches over. Therefore, it could be beneficial to shift the output changeover to the time instance $D_2 t_h$. This way, the current will most likely be negative during the switchover resulting in a ZVS turn-on condition in Q_y. Unfortunately, the gain of ZVS at Q_y turn-on does come at the cost of losing ZVS at Q_x and Q_z turn-off. This would still be useful as the turn-on losses in Q_y are higher. Furthermore, it could help with a better distribution of the losses.

In the current representation of SPSSO, the phase shift is not implemented and Q_y does not turn on with ZVS. This could be a good topic for a future project and can reduce the losses during transition significantly.

4.15. Infeasible Region

The output capabilities of a power converter can be represented by considering the output voltage, current and power limits. The full converter with two submodules will have a power limit of 25kW, a current limit of 64A and a voltage limit of 1000V. This output region is shown in Figure 4.16 as all the colored regions combined. The light green region is the region where the converter can only be in series or parallel as the output voltage or current is higher than the respective limit of a single submodule. The dark green region is the region where the converter can be in both series and parallel. When the limits of the submodules are considered, a small region appears where the requested output is infeasible. This implies that the converter needs to be dimensioned bigger to ensure that the converter can output the advertised power in all operating conditions.

4.16. Conclusion

In this chapter, a switchover circuit with three Mosfets was introduced. The output filter will be placed on the output to reduce conduction losses as much as possible. The state of the output circuit now has a direct influence on the inductor current so a new modulation strategy with Single Phase Shift and Switchover (SPSSO) was introduced. The modulation strategy can ensure a stable transition without oscillations. The losses during a transition are modeled and analyzed and the infeasible region is introduced. In the next chapter, the efficiency of a single submodule is increased by applying a more advanced modulation strategy.

5

Triple Phase Shift with Switchover

In Chapter 4, a new modulation method was introduced to ensure a smooth transition between a parallel and series connection. With this modulation method, SPS was used for the purpose of explanation. In Chapter 3, TPS modulation with MCSO was proven to extend the efficiency of the submodules in a wide region. It is therefore necessary to integrate the switchover method with this modulation. In this chapter, the integration of TPS with Switchover (TPSSO) will be discussed in combination with MCSO. First, the model for the inductor current and output current will be derived. Then, the different approaches for control are discussed.

5.1. Inductor and Output Current

Like with SPSSO, the inductor current can be calculated for every switching point. The currents are calculated using the same method as in Chapter 4 but now with all the switchover points of TPSSO. Like with SPSSO, the output circuit switches between series and parallel two times per period. The resulting modulation has 12 modes since there are 3 possible modes in TPS and D_x can take any value between 0 and 1. The modes are shown in Equation 5.1. The equations for the inductor current can again be used to derive the output current. The inductor current and output current are used to calculate the losses in the full circuit.

$$\begin{aligned}
&\text{Mode 1: } D_1 \leq D_2 \leq D_3 \leq D_x \\
&\text{Mode 2: } D_1 \leq D_2 \leq D_x \leq D_3 \\
&\text{Mode 3: } D_1 \leq D_x \leq D_2 \leq D_3 \\
&\text{Mode 4: } D_x \leq D_1 \leq D_2 \leq D_3 \\
&\\
&\text{Mode 5: } D_2 \leq D_1 \leq D_3 \leq D_x \\
&\text{Mode 6: } D_2 \leq D_1 \leq D_x \leq D_3 \\
&\text{Mode 7: } D_1 \leq D_x \leq D_1 \leq D_3 \\
&\text{Mode 8: } D_x \leq D_2 \leq D_1 \leq D_3 \\
&\\
&\text{Mode 9: } D_2 \leq D_3 \leq D_1 \leq D_x \\
&\text{Mode 10: } D_2 \leq D_3 \leq D_x \leq D_1 \\
&\text{Mode 11: } D_2 \leq D_x \leq D_3 \leq D_1 \\
&\text{Mode 12: } D_x \leq D_2 \leq D_3 \leq D_1
\end{aligned} \tag{5.1}$$

Since the calculation is done already for SPSSO, the method is not shown in this section. The equations for the inductor current with TPSSO in all 12 modes are shown in Appendix A. All current equations are verified using PLECS simulations. The current is verified for all 12 modes at three different operating points. The average error is 1.4%.

5.2. Control Method

The control layout for a dual DAB configuration is shown in Figure 5.1. In the layout, a controller is added to steer the output current to the desired value. The reference current produced by the controller is fed into the optimization algorithm which finds the optimal combination of D_1, D_2, and D_3. These values are then translated to PWM signals for the two DAB converters. To adjust for the value of D_x there are four possible methods.

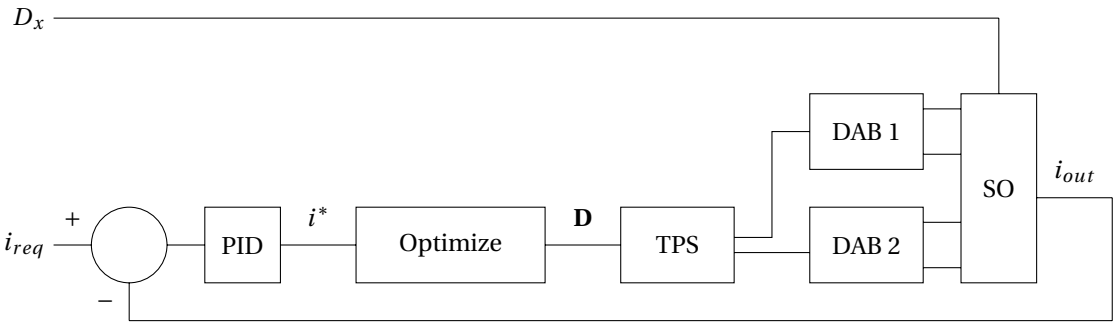


Figure 5.1: Overview of the control layout

Firstly, it is possible to integrate the value of D_x into the optimization block. This would give a similar result as given in Chapter 4 for SPSSO. With SPSSO it was possible to calculate the control signal D based on the required output current and the state of D_x. This can also be done for any optimization by redefining the optimization problem.

Secondly, it is possible to compensate reference signal i^* coming from the PID controller before feeding it to the optimization algorithm. This way, the compensation for D_x is done outside of the optimization, keeping the optimization flexible to change.

Another, option is to make use of the stabilizing ability of a controller. In a real-life environment, a controller is always necessary to have a stable output current. It is possible to use this controller to keep the output current stable even during a transition.

The final approach is to switch from TPS to SPS before the transition. This allows for a stable transition using SPSSO as described in Chapter 4. Then, after the transition is done, the converter will switch back to TPS modulation with the desired optimization.

All the mentioned control options are discussed in the next sections.

Integration with Optimization

The first option is to integrate the compensation into the optimization. With this method, the calculations for the MCSO are done again but now with the value D_x considered. This would result in a similar optimization outcome as MCSO as described in Section 3.6. by integrating D_x in the optimization, there are no added computations needed. Although this would be the cleanest option, it would limit the optimization method to the chosen one. It was chosen to keep the choice of optimization more flexible. Integrating D_x into the modulation could be a good subject for future research.

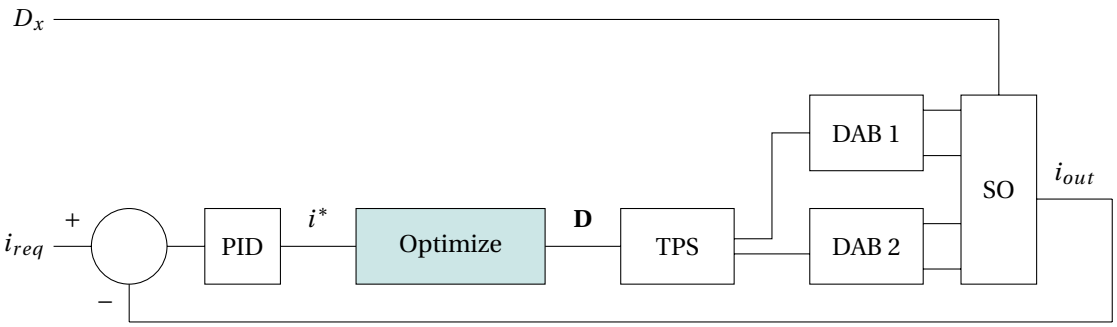


Figure 5.2: Overview of the control layout with compensation in the optimization

Compensated Control Signal

With a compensated control signal it is possible to use any optimization type. The idea is to compensate the reference signal i^* based on the value of D_x.

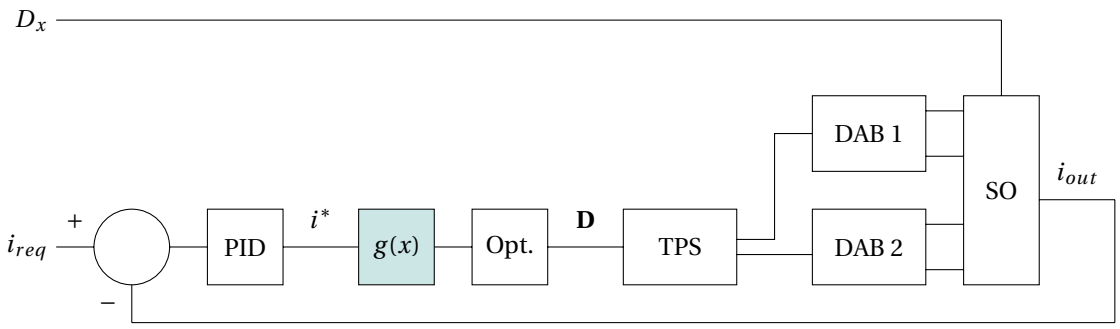


Figure 5.3: Overview of the control layout with compensation before the optimization

The compensation needs to be calculated for every mode and every modulation. SPSSO can serve as a good introduction. In Chapter 4, SPSSO was introduced. The SPSSO modulation takes a reference current which is used to calculate the required control signal D based on the value of D_x. The control signal for SPSSO can be compared to SPS. The required phase shift for SPS is calculated as

$$D^*_{SPS} = \frac{1}{2} - \frac{1}{2}\sqrt{1-i^*}. \tag{5.2}$$

When comparing this to the SPSSO, the required output current can be compensated for SPSSO.

$$D^*_{SPSSO} = \frac{1}{2} - \frac{1}{2}\sqrt{1-g(i^*)} = \begin{cases} \frac{1}{2} - \frac{1}{2}\sqrt{1+D_x^2-D_x-i^*} & (i^* \geq 3(D_x - D_x^2)) \\ \frac{1}{2} - \frac{1}{2}\sqrt{1-2D_x^2+2D_x-2i^*} & (i^* < 3(D_x - D_x^2)) \end{cases} \tag{5.3}$$

Where $g(i^*)$ is now defined as

$$g(i^*) = \begin{cases} i^* + D_x - D_x^2 & (i^* \geq 3(D_x - D_x^2)) \\ 2i^* + 2D_x^2 - 2D_x & (i^* < 3(D_x - D_x^2)) \end{cases} \tag{5.4}$$

Now, the compensated reference current $g(i^*)$ can be used as input to the controller or optimization method. When using this method with DPS or TPS modulation, the compensation can be computed from the output current equations. This has to be done for every mode in the modulation. With SPSSO only two modes are considered. With TPSSO, this would expand to 12 modes.

This method can be a very simple and robust solution that would allow flexibility in the choice of optimization but the compensation needs to be calculated for the used modulation. It was tried to use the approximated compensation for SPSSO for other modulations. Unfortunately, it will lead to inaccurate output currents. The inaccuracy is determined by the value of the inner phase shifts D_1 and $D_3 - D_2$. The bigger those inner phase shifts are, the bigger the output fluctuations are. In Figure 5.4, the output current is shown for TPS modulation with MCSO and with a compensated reference current based on Equation 5.4. It is noticeable that the current has a peak around 0.4s. This peak is caused by the inner phase shift $D_3 - D_2$. In Figure 5.5, the output current is shown again for an output voltage of 200V. Due to the low output voltage, the optimization algorithm outputs a high inner phase shift D_1. This causes the output current to fluctuate because the compensation does not take this phase shift into account. It is therefore not possible to use Equation 5.4 as compensation for every modulation.

Control with a compensated reference can be very useful because it does not affect the optimization strategy but it requires calculating the compensation for every modulation type.

PID Controller

The last solution is to use a controller for stabilizing the output current during the transition. This would add no extra complexity to the control because the output will most likely be already controlled by some form of feedback control.

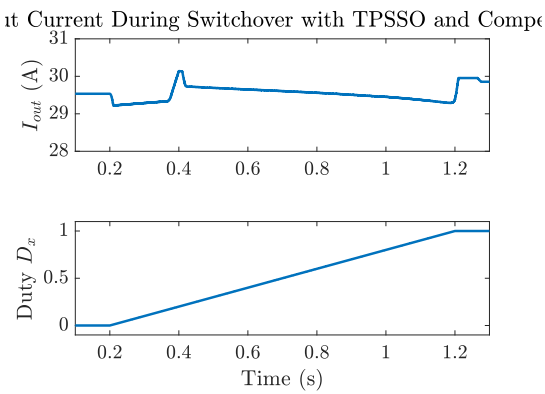


Figure 5.4: PLECS simulation of the output current and dutycycle D_x during switchover with TPS, MCSO and feedback compensation. $V_{out} = 400V$ and $i^* = 30A$

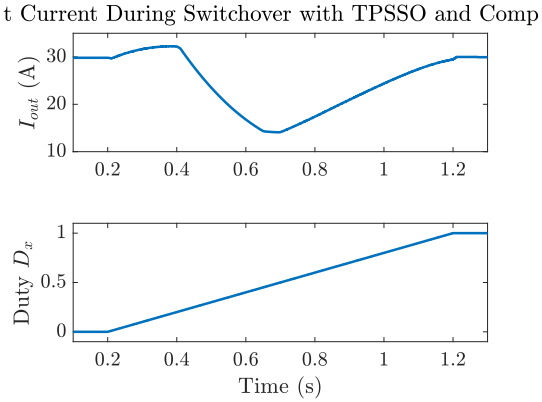


Figure 5.5: PLECS simulation of the output current and dutycycle D_x during switchover with TPS, MCSO and feedback compensation. $V_{out} = 200V$ and $i^* = 30A$

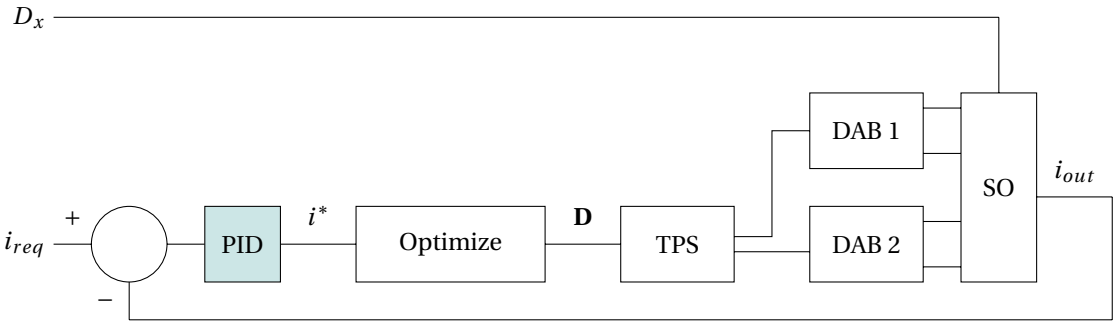


Figure 5.6: Overview of the control layout with compensation in controller

In this example, a PID controller is added to the input of the MCSO algorithm. This controller is tuned using a simple Ziegler-Nichols tuning method. With this method, the system is made critically stable using only a proportional controller. Then, depending on the value of k_p and the frequency of oscillation, the PID parameters can be determined.

The PID controller is finally tuned to the values in Table 5.1.

K_p	K_i	K_d
0.2	5	0.02178

Table 5.1: Tuned PID parameters for a fast responding controller

The full setup including the PID controller are simulated using PLECS to see the total deviation from the setpoint during the transition. The result is shown in Figure 5.7. When using a transition time of 1 second, the output current increases to 8.3% of the setpoint. This is a substantial increase and not desirable. The deviation can be reduced by increasing the transition time to 5 seconds. In Figure 5.8, the output current is shown during a transition of 5 seconds. The deviation is reduced to 2%.

Back to SPSSO

Since the transition period is very short, the converter doesn't need to be in the most efficient operating point during the transition. It could therefore be possible to first transition back into SPS modulation before the transition starts. Then, the transition can be done using SPSSO and finally, the modulation is switched back into TPS or any other modulation.

The main question that has to be answered is; can we switch back into SPS without large oscillations? PLECS simulations at different operating points show that there is no overshoot when changing between TPS and SPS instantly. There is however a small difference in output current between MCSO and SPS. In Figure 5.10 a transition is shown where the converter is first put back into SPSSO mode. At $t = 0.2s$ the converter

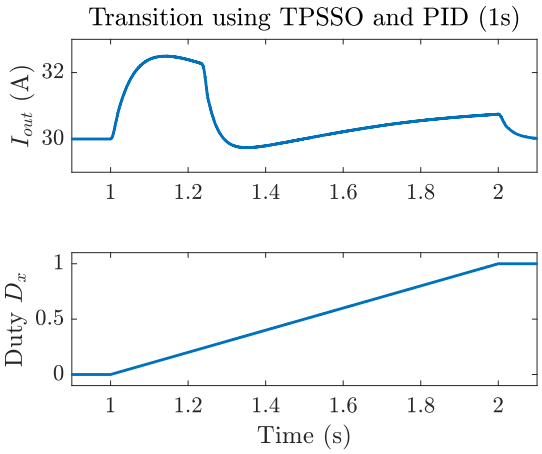


Figure 5.7: PLECS simulation of the output current and dutycycle D_x during switchover with TPS, MCSO and a PID controller. $V_{out} = 400V$ and $i^* = 30A$. Transition time is 1 second

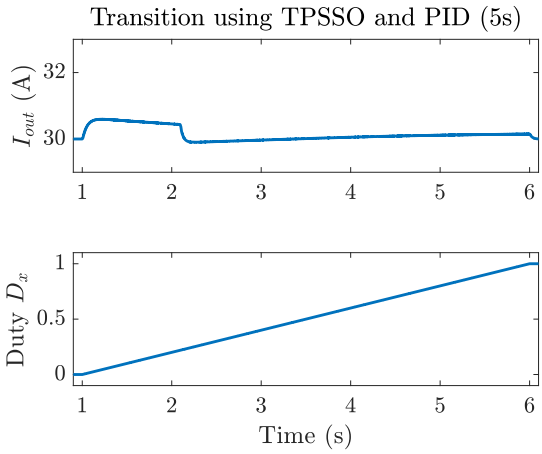


Figure 5.8: PLECS simulation of the output current and dutycycle D_x during switchover with TPS, MCSO and a PID controller. $V_{out} = 400V$ and $i^* = 30A$. Transition time is 5 seconds

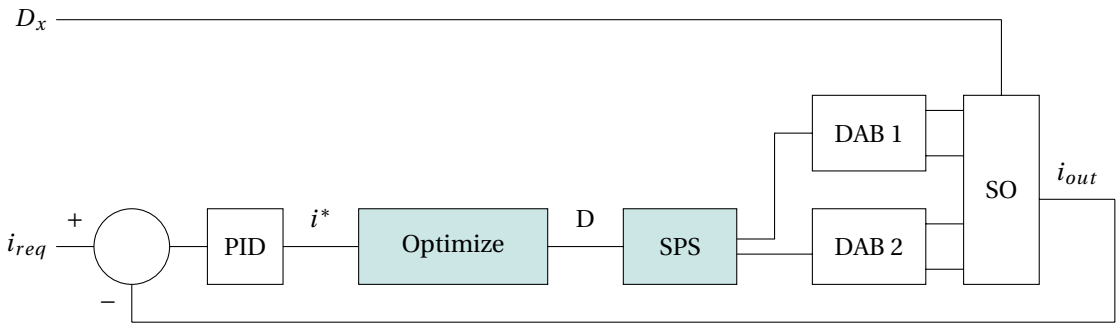


Figure 5.9: Overview of the control layout with compensation in modulation

is put in SPSSO mode. At $t = 0.5s$, the transition starts using SPSSO. At $t = 1.65$ the converter is put back to TPS modulation with MCSO. The output current has a maximum deviation of 1.6% from the setpoint. The largest jump in dutycycle is when the inner phase shifts of the bridges are high. This is the case when the output voltage and the output current are low. This situation is simulated and the switching instance from TPS to SPS is shown in Figure 5.11. The current is changing 0.38A which is a big change compared to the total output current. The change is however stable and not oscillating. The controller can compensate for this inaccuracy.

Comparison

The four methods shown above all have their pros and cons. Integration into the optimization would be the cleanest option but this would take a large effort and it would reduce the flexibility of changing the optimization later. The compensated control method can overcome this issue by taking the compensation for D_x outside of the optimization. This is done for SPSSO modulation but for TPSSO this would still be a mathematically intensive process. By integrating the compensation into the PID controller, the mathematical compensation can be omitted completely. With this method, the controller will be responsible to keep the output current stable during the transition. The last option is to switch over to SPSSO before the transition. The last two options are both easy and viable solutions that require little extra design steps. The switch to SPSSO seems to give the most stable transition and is not restricted in the transition speed in contrast to the PID controller. Therefore, a switch to SPSSO is recommended.

Integrating D_x in the optimization is still a good improvement for future research.

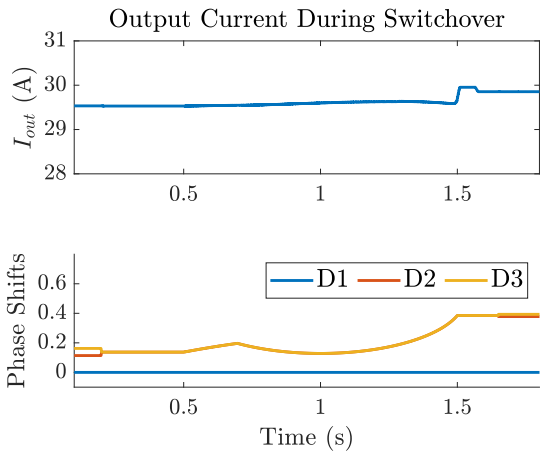


Figure 5.10: PLECS simulation of the output current and phase shifts for a transition in SPSSO. $V_{out} = 400V$ and $i^* = 30A$

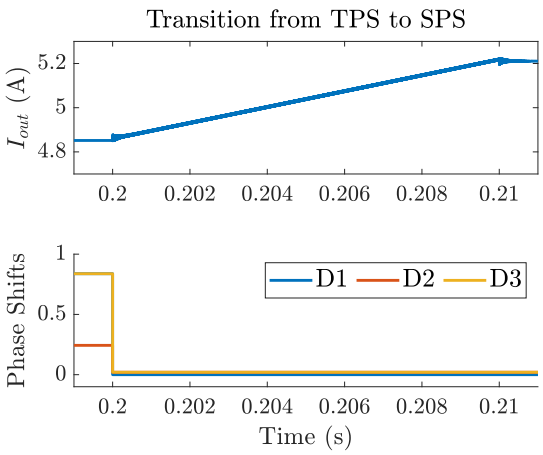


Figure 5.11: PLECS simulation of the output current and phase shifts for a transition from TPS to SPS. $V_{out} = 150V$ and $i^* = 5A$

5.3. Optimal Switchover Voltage

Now that it is possible to do a stable transition using TPSSO, it is useful to find the optimal switchover voltage. This voltage is the border where the converter will transition from parallel to series or back. There are two reasons to initiate a transition to series.

- The output voltage is above the maximum submodule voltage
- The efficiency in series mode is higher

The converter will transition back to parallel when the efficiency in parallel mode is higher or the requested output current is higher than the submodule current. The efficiency model from Chapter 3 is used to determine the efficiency of the converter in both series and parallel. In Figure 5.12, the efficiencies of two DAB converters are plotted for the full output voltage region. The efficiency in parallel operation is calculated for voltage from 150V up to 500V. The efficiency in series operation is calculated for voltages from 300V up to 1000V. From the figure, it is possible to derive when the series configuration is more efficient than the parallel configuration.

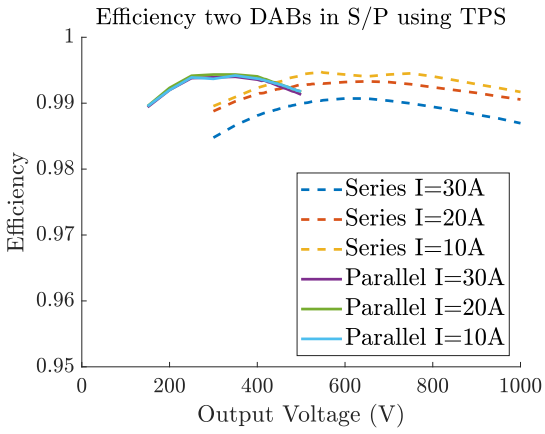


Figure 5.12: Efficiency of two DABs in Series and Parallel using TPS modulation. Calculated for a range of output voltages and output currents, $V_{in} = 750V$

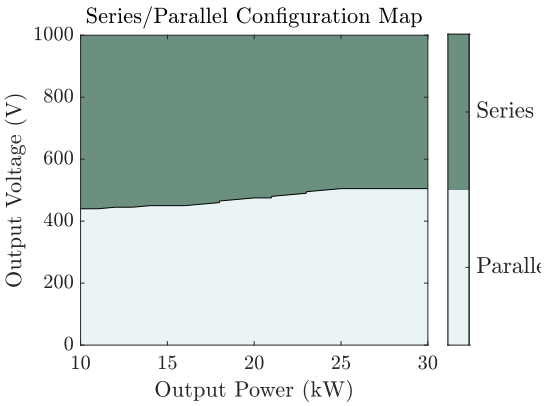


Figure 5.13: Region where Series or Parallel configuration is more efficient.

Eventually, the efficiency region will determine the switchover voltage. By calculating the efficiency for every voltage and every output power, a map can be drawn as shown in Figure 5.13. In this figure, the most

efficient output state is shown for all output voltages and output powers. It can be seen that the optimal changeover voltage with TPS is changing when the power increases.

Whenever the output voltage exceeds the transition line, the converter will initiate a transition. These values can be programmed into a microcontroller with a look-up table to get the best switchover voltage. Other solutions for estimating the best transition voltage can be good subjects for future research.

The transition voltage will incorporate hysteresis to prevent the converter from constantly transitioning when the output voltage experiences noise or small oscillations. A hysteresis between 10V and 20V will be enough depending on the voltage oscillations on the output.

5.4. Conclusion

In this section, TPS modulation was integrated with the switchover modulation strategy. To integrate the advanced modulation, four options were compared; Integration into the optimization, compensation before optimization, integration in the PID controller, and switching back to SPSSO. A transition in SPSSO is chosen to be the best solution. This method requires little extra effort for the designer and retains flexibility in the modulation and the control. A transition from TPS to SPS was tested and is stable enough to be controlled. Finally, the optimal switchover voltage using TPS was determined.

6

Design and Optimization

In this chapter, the design of both DAB submodules will be optimized to ensure the best efficiency over the full output voltage range. The following research question will be answered in this section.

> How can the operating point of the series-parallel-output DAB converter be optimized to ensure maximum efficiency in all operating conditions?

The optimization is done in Matlab and is done specifically for TPS modulation. First, the inductor and transformer ratio are optimized, then the inductor and transformer design will be optimized. Finally, the optimal components are selected for a 150V-1000V converter.

6.1. Optimization of L and n

In this section, the main components that determine the converter efficiency will be optimized. The size of L and the turn ratio n will be optimized together to get the optimal efficiency. First, an optimization is done for the full operation range. With this optimization, the circuit is optimized for full power and each voltage is treated equally. Then, the optimization is adapted for specific EV charging applications. The converter is optimized for common charging voltages and charging powers.

Full Power Optimization

In this section, the inductor and the turn ratio are optimized for the highest efficiency at the maximum output power for each output voltage in the output voltage range. The inductance and the turns ratio are optimized together as the converter efficiency is dependent on both. In [16], three optimization strategies are compared for a DAB converter. The optimizations are done based on I_{peak}, I_{rms}, and P_{loss}. From those three, P_{loss} optimization gave the optimal efficiency in a wide output voltage range. The optimization is done by calculating the converter losses for every combination of L and n and deriving the efficiency. The efficiency for every L and n combination is averaged for the full output voltage range. The optimization is defined as

$$\max\eta(L,n) = \frac{1}{1000V - 150V} \sum_{v_{out}=150V}^{1000V} \eta_{opt}(L,n,v_{out}) \tag{6.1}$$

Where v_{out} is the output voltage and η_{opt} is the efficiency in the optimal configuration (series or parallel). When the output voltage is above the maximum voltage of one submodule, the converter is automatically in series, so $\eta_{opt} = \eta_{series}$. Because the converter is optimized for the maximum output power, the converter is in parallel in all other cases.

$$\eta_{opt} = \begin{cases} \eta_{series} & v_{out} > v_{max} \\ \eta_{parallel} & \text{else} \end{cases} \tag{6.2}$$

The efficiencies are calculated by summing all the losses as shown in Chapter 3. In this optimization, an E65/32/27 ferrite core is used for the inductor and the transformer. The core selection will be optimized in a later section. For the inductor, the number of windings is calculated based on the core parameters, the required inductance and the peak inductor current.

$$N_{min} = \frac{L_{req} \cdot I_{max}}{B_{max} \cdot A_e} \tag{6.3}$$

Where L_{req} is the required inductance, I_{max} is the peak inductor current, B_{max} is the maximum allowable field in the core, and A_e is the effective area of the core.

For the transformer, the amount of turns on the secondary side is fixed at 10. This is valid because the volt seconds on the secondary side do not change.

$$N_s = \frac{V_{out,max} t_h}{\Delta B A_e} \tag{6.4}$$

Where N_s is the number of turns on the secondary side, $V_{out,max}$ is the maximum output voltage, t_h is half of the switching period which is the maximum time that the output voltage is applied to the secondary winding, ΔB is the maximum change of field inside the core, and A_e is the effective core area. The primary side is calculated by multiplying the N_s by the required turns ratio n_{req}.

$$N_p = N_s \cdot n_{req} = 10 \cdot n_{req} \tag{6.5}$$

The leakage inductance of the transformer core needs to be calculated to compensate for the inductance of the inductor. The leakage inductance is calculated with the method of Mohan, Undeland, and Robbins [29]. This method is valid for E-core transformers only.

$$L_{leak} = \frac{\mu_0 N_p^2 l_w b_w}{3 h_w} \tag{6.6}$$

Where N_p is the number of primary turns, l_w is the length of a single turn around the core, b_w is the window breath of the core and h_w is the window height.

The required inductance for the inductor is now calculated by

$$L_{ind} = L_{total} - L_{leak} \tag{6.7}$$

In the optimization only the inductance L_{ind} is optimized and shown.

The other components in the circuit like switches and output filters are kept the same as described in Chapter 3. The optimization is performed in Matlab and the efficiencies are shown in a contour diagram in Figure 6.1. The optimal design is marked with an asterisk.

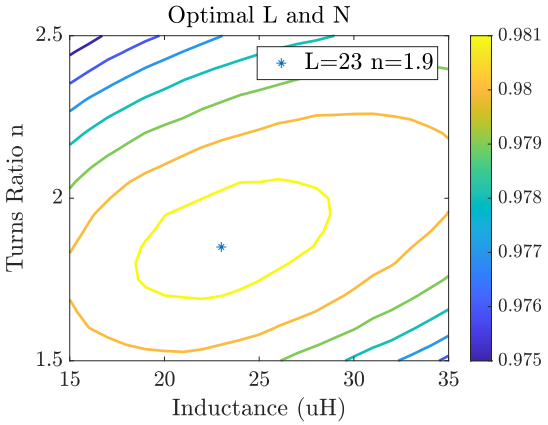


Figure 6.1: Efficiency of two converters for a range of inductances and turn ratios

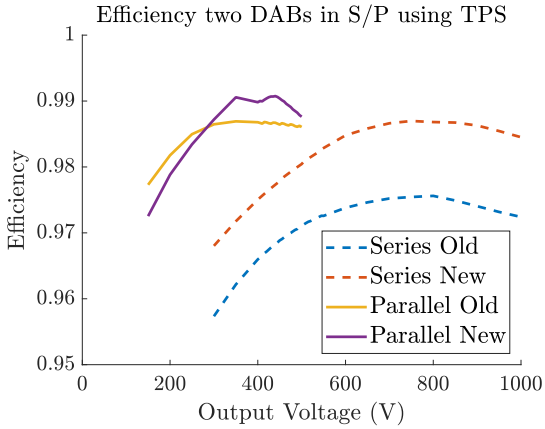


Figure 6.2: Comparison of the optimized converter vs the un-optimized converter

The optimal design for $L = 23\mu H$ and $n = 1.9$ is simulated and compared to the old design with $L = 56.25\mu H$ and $n = 1.87$. The results are shown in Figure 6.2 and summed in Table 6.1. With the optimized design the losses are reduced by 30%.

Table 6.1: Summary of the results after optimization

Parameter	Old Design	New Design
Inductance	$56.25\mu H$	$23\mu H$
Average Efficiency (30A)	97.97%	98.51%
Maximum Efficiency (30A)	98.32%	98.81%
Losses (30A)	424W	297W

Charging Cycle Optimization

In the end, this thesis aims at creating an efficient EV battery charger. It is useful to look at the optimization in this context. When looking at the charging power demand for residential chargers if Figure 6.3 [42], it is visible that in 2020 more than 65% of the charge requests are for powers below 10kW. More than 45% of the requests are for powers below 5kW. It makes therefore no sense to optimize the converter efficiency for maximum power output.

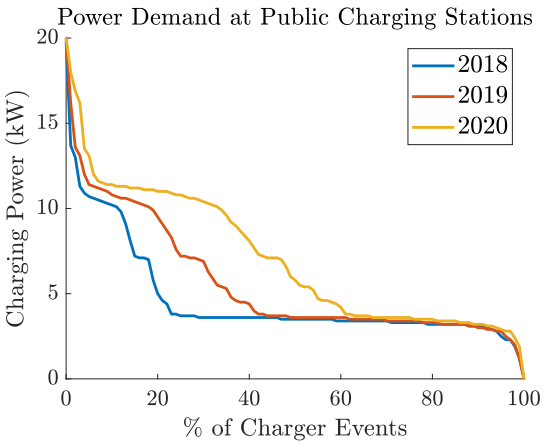


Figure 6.3: Power Demand at Public Chargers for 2018, 2019, and 2020 [42]

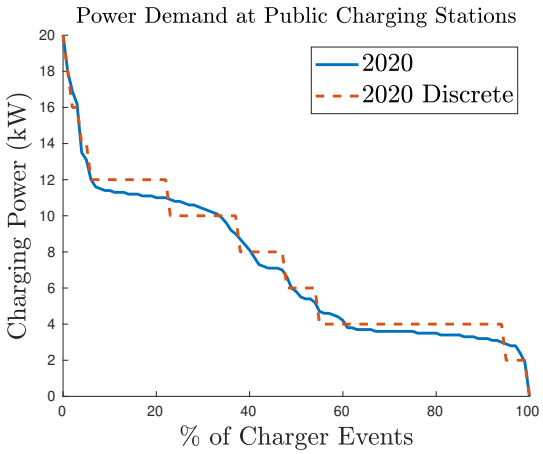


Figure 6.4: Power Demand at Public Chargers for 2020 [42] with discretization

Furthermore, not all voltages in the output range are equally likely to occur. Charging voltages like 400V, 600V and 800V are most common. The optimization can be adjusted to optimize certain commonly used operating points. For this optimization charging voltages 400V, 600V and 800V are considered. At each charging voltage, ten charging powers are considered. Each charging power is scaled based on the power demand from 2020 in Figure 6.3. The charging power demand is first discretized by rounding to the nearest step value as shown by the dotted line in Figure 6.4. Then the likelihood of each discrete charging power is computed in Figure 6.5. The efficiency for each charging voltage is calculated for all the discrete charging powers and the efficiencies are combined by weighing them by their likelihood. The optimization can be defined as

$$\max \eta(L,n) = \sum_{p} \eta_{opt}(L,n,V_{out},p) \cdot w_p \tag{6.8}$$

Where η is the weighted efficiency, p is the output power, w_p is the likelihood of the specific power as defined by Figure 6.5, L and n are the inductance and the turn ratio, and V_{out} is the output voltage.

The optimization is done for 400V, 600V and 800V resulting in the efficiency plots in Figure 6.7. Then the efficiencies of those three output voltages are averaged equally to obtain Figure 6.6. The optimization results in $L = 31\mu H$ and $n = 2.1$.

Comparison

In Figure 6.8 the resulting designs of the two optimizations are compared. It is clear that from the two optimizations, the Charging Cycle optimization performs better at low power and still performs well at higher power. In Table 6.2 the efficiencies of the two optimizations are compared. The high power optimization outperforms the other designs at maximum power but the efficiency of the EV optimization is close. The presented efficiencies are taken from the whole operating region. The EV optimization design is chosen be-

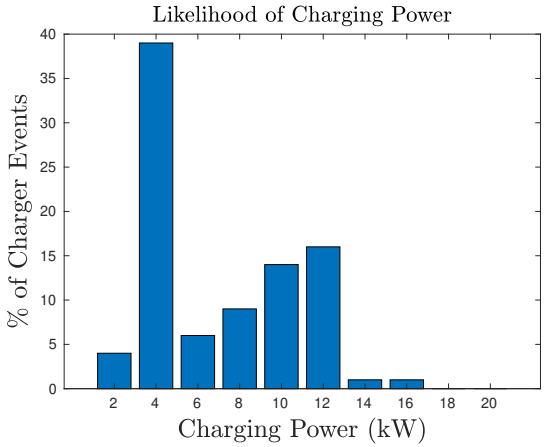


Figure 6.5: % of Charging requests done for each output power.

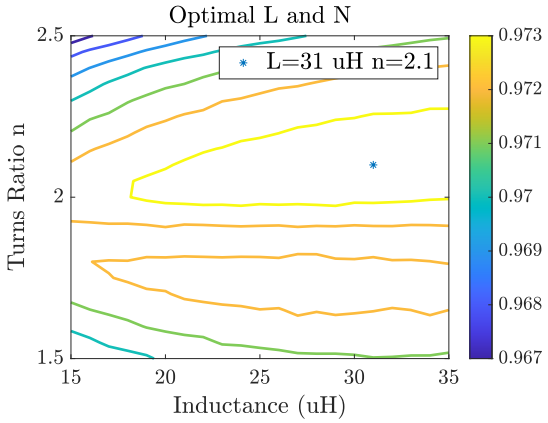
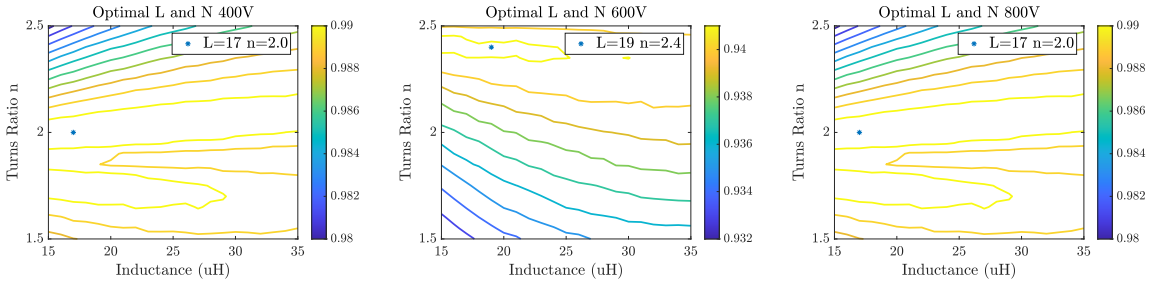


Figure 6.6: Optimization for a weighted output power and three voltages 400V, 600V and 800V combined



(a) 400V (b) 600V (c) 800V

Figure 6.7: Optimization for a weighted output power for 400V, 600V and 800V

cause the efficiency at lower power is the highest. Since the converter will often be working with lower output power, this optimization is the best choice. The inductor is optimized further in the next section.

Table 6.2: Summary of the results for both optimizations

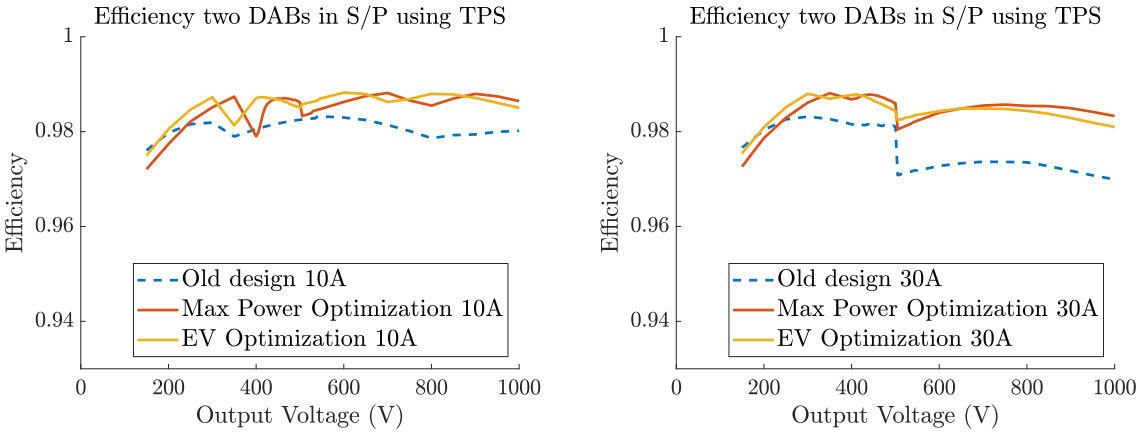
Parameter	Old Design	Max Power	Charging Cycle
Inductance	$56.25\mu H$	$23\mu H$	$31\mu H$
Turn Ratio	1.87	1.9	2.1
Avg Efficiency	97.97%	98.51%	98.56%
Max Efficiency	98.32%	98.81%	98.82%
Min Efficiency	96.90%	97.21%	97.50%

6.2. Submodule Limits

In Section 4.15, the infeasible region was introduced. This region is caused by the output voltage and current limits of the submodules. To remove the infeasible region, the limits of the power modules need to be increased. This can be done by increasing the submodule voltage or current limits. In this section, the optimal submodule limits are determined.

The optimization is done by selecting a range of viable voltage limits and calculating the efficiency for all operating voltages at the full output power. The full output power is chosen because, at this power, the influence of the submodule voltage limit is the largest. The efficiencies for all the output voltages are averaged and the resulting optimization is shown in Figure 6.9. In this optimization, the current limit in series mode is limited to

$$I_{lim} = \frac{P_{max}}{V_{lim}} \tag{6.9}$$



(a) 10A Output

(b) 30A Output

Figure 6.8: Comparison between the two optimized converter designs

Where P_{max} is the maximum output power and V_{lim} is the voltage limit of the submodule that will be optimized.

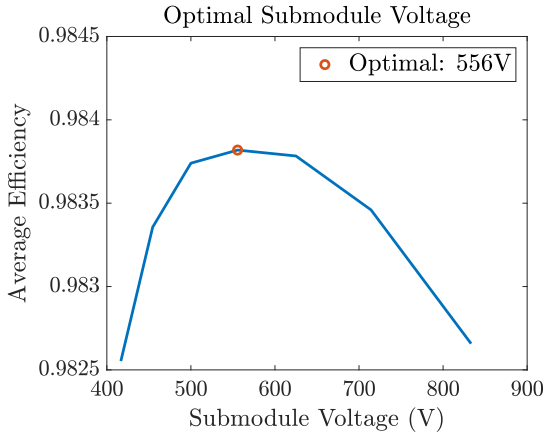


Figure 6.9: Optimization of the submodule voltage limit

From Figure 6.9 can be seen that the average efficiency of the converter increases up to around 550V. After this point, the efficiency decreases again because the converters are limited to parallel operation by the current limit. A voltage limit of 550V will be chosen for this design to reduce the infeasible region. With a voltage limit of 550V the submodule will need a current limit of at least 45.5A to achieve the full operating region as shown in Figure 4.16 (all colored regions). A limit of 46A is chosen and the voltage and current limits are shown in Table 6.3. These values can be used to select the switches and to do further optimization of the circuit.

Table 6.3: Final Optimized Submodule Limits

Submodule Voltage	550V
Submodule Current	46A

6.3. Transformer Design

Now that the required inductance and turn ratio are calculated, the inductor and transformer can be designed. First, the transformer design is optimized. Then the inductor is optimized. For the transformer, a selection of three E-shape cores is compared. These cores all fit the required area product of the transformer. The required area product is calculated by the stored energy in the inductor [43].

$$AP = \frac{V_p I_{rms,p}}{k_w J \Delta B} = \frac{800V \cdot 23.7A}{0.6 \cdot 3A/cm^2 \cdot 600mT} = 160000mm^4 \tag{6.10}$$

Where V_p is the primary voltage, k_w is the filling factor of the wiring space, $I_{rms,p}$ is the RMS primary current, J is the current density in the wire and is chosen to be $3A/cm^2$, and ΔB is the maximum allowed field fluctuation in the magnetic material. The maximum field is chosen to be 300mT, so ΔB is set to 600mT. The cores that fit the required area product are presented in Table 6.4.

Table 6.4: Selected inductor cores with all parameters

Core	Shape	P_{loss} (W)	Turns	B_{max} (mT)
E65/32/27	E	74.3	13	197
E70/33/32	E	68.3	12	167
E80/38/20	E	70.1	17	207

For the transformer, only the core size and amount of turns will be optimized. The core shape and material are kept constant. the chosen material in this optimization is N27 ferrite. The core losses and wire losses are very dependent on the number of turns. With more turns, the core losses will decrease because B_{max} is lower but the winding losses increase. In Figure6.11, the losses are shown for a selection of B_{max}. By choosing the number of turns on the primary side, the losses can be optimized. In Figure 6.10 the transformer losses are plotted against the turn count of the secondary winding. The number of primary turns is calculated by multiplying the secondary turns by the required turns ratio of $n = 2.1$. The wire losses are calculated by using the equations from Section 3.2. The wire size is adjusted to fill up the total wiring window of the core with compensation for a fill factor of $k_w = 0.6$. The winding area is divided equally between the primary and secondary winding.

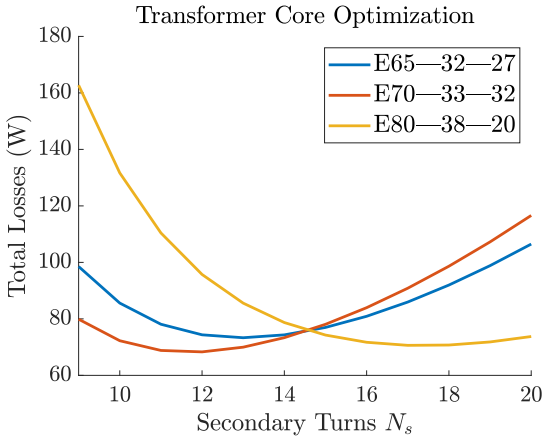


Figure 6.10: Comparison between the three selected transformer cores. The transformer losses are plotted for a selection of turns ratios

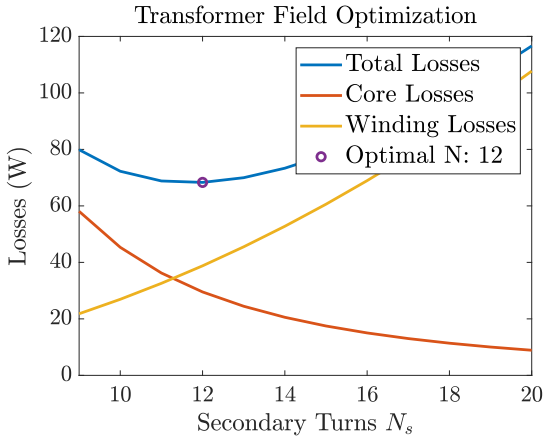


Figure 6.11: Optimization of the transformer turns for E70/33/32 core

It is visible that the E70/33/32 has the lowest losses at $N_s = 12$. The number of turns on the primary side is chosen to be 25 giving a turns ratio of $n = 2.08$.

With this information, the leakage inductance of the transformer can be derived. The method for calculating the leakage inductance is taken from [29].

$$L_{leak} = \frac{\mu_0 N_p^2 l_w b_w}{3 h_w} = \frac{\mu_0 \cdot 23^2 \cdot 163mm \cdot 16mm}{3 \cdot 43mm} = 13.4\mu H \tag{6.11}$$

Where l_w is the mean length of one turn, b_w is the window breath and h_w is the window height. The leakage inductance of the transformer needs to be compensated in the inductor value.

Table 6.5: Final Transformer Design

Parameter		Value
Core		E70/33/32
Primary Turns	N_p	25
Secondary Turns	N_s	12
Losses	P_{loss}	68.3W
Temperature Rise	ΔT	$101°C$
Power Density		$42.1 kW/L$
Max Flux	B_{max}	168mT
Leakage inductance	L_p	13.4 μH

6.4. Inductor Design

With the transformer parameters known, the inductor can be designed. The total required inductance is optimal at $31\mu H$. In this section, a comparison will be made between different inductor shapes and sizes. For this optimization, a selection of E cores and Potted cores are considered. The core material in this optimization is kept fixed at N27 to reduce the number of optimization parameters. The list of selected cores with their parameters is presented in Table 6.6. The cores are selected from a range of E, U and Toroidal cores that matched the requirement of the area product. The area product of the inductor can be calculated using Equation 6.12 [29].

$$AP = \frac{LI_{max}I_{rms}}{k_w J \Delta B} = \frac{17.6\mu H \cdot 44.7A \cdot 23.7A}{0.6 \cdot 3A/cm^2 \cdot 300mT} = 52000mm^4 \tag{6.12}$$

Table 6.6: Selected inductor cores with all parameters

Core	Shape	P_{loss} (W)	PD (kW/L)	ΔT ($°C$)	Turns	B_{max} (mT)	l_g (mm)
E55/28/21	E	63.0	100	153.4	14	252	5.8
E55/28/25	E	56.6	85	128.2	13	225	6
E65/32/27	E	58.4	55	103.8	12	186	6.6
E70/33/32	E	57.3	42	87.7	11	160	6.9
E80/38/20	E	66.2	51	110.3	15	214	7.3
PM74/59	Pot	47.3	47	79.3	10	147	6.7
PM87/70	Pot	54.4	30	70.0	10	134	7.3
PM114/93	Pot	48.4	15	42.4	8	86.5	8.8

For each core, the number of turns and the airgap are calculated using Equation 3.11, and Equation 3.12 respectively. In these equations the value B_{max} is used. Until now (in Chapter 3) the value of B_{max} was fixed at 250mT as was given in the datasheet. In practice, the value of B_{max} has a large influence on the inductor losses and the value can be optimized for every core. When B_{max} is large the core losses in the magnetic material will be higher but the required amount of turns is lower. This creates an optimal B_{max} where the total losses from the core and winding are minimal. The optimization is done by calculating the winding losses and the core losses for different flux density values. The losses are computed in the same way as in Section 3.2. In these equations, the improved General Steinmetz Equation (iGSE) is used and the skin effect and proximity effect are considered. When the optimal B_{max} is calculated, the required turns and the airgap can be calculated with the equations below [29].

$$N_{min} = \frac{LI_{max}}{B_{max}A_e} \tag{6.13}$$

$$l_g = \frac{A_e}{\frac{A_e B_{max}}{\mu_0 N I_{max} - \frac{a+d}{Ng}}} \tag{6.14}$$

Where, L is the required inductance, I_{max} is the peak inductor current, A_e is the effective area of the magnetic material, and A_g is the effective area of the air gap. In this optimization, the fringing effect is approximated by the length $l_g/2$ so $A_g = (a + l_g)(d + l_g)$ as explained in Section 3.2.

For each design, the required amount of turns is rounded up to an integer. The total losses in the inductor are calculated and the results are shown in Table 6.6.

The losses are calculated at the full converter power. The inductor current is calculated using Equation 3.4. First, the required phase shift is calculated for SPS modulation. Since the inductor value is reduced, the full output power is only a portion of the power capabilities and the phase shift D will be lower than 0.5.

$$P_{max} = \frac{V_1 V_2}{8 f_s L} = \frac{800 \cdot 550 \cdot 2.1}{8 \cdot 100kHz \cdot 31\mu H} = 37.3kW \tag{6.15}$$

$$D = 0.5 - 0.5\sqrt{1 - P_{req}/P_{max}} = 0.5 - 0.5\sqrt{1 - 25/37.3} = 0.2129 \tag{6.16}$$

At this phase shift, the inductor current can be calculated using Equation 3.4.

$$I_0 = A(V_2(2D-1) + V_1) \tag{6.17}$$

$$I_1 = -A(V_1(2D-1) + V_2) \tag{6.18}$$

Where $A = \frac{-1}{4 f_s L}$. The total losses can now be calculated with the method in Section 3.2. The power density of the core is also computed by dividing the total transferred power by the total volume of the core.

$$PD = \frac{P_t}{V_c} = \frac{12.5kW}{V_c} \tag{6.19}$$

With the obtained core losses, the total temperature rise in the core can be estimated too. The temperature rise is calculated by using the method from [44].

$$\Delta T = \left(\frac{P_{mag}}{2A_{mag}}\right)^{0.833} \tag{6.20}$$

Where P_{mag} are the total losses in the inductor (including winding losses), and A_{mag} is the total area of the inductor material. In this optimization, the area is approximated by a box enclosing the total inductor. The temperature rise is shown for every core in Table 6.6. When the temperature of the core is too high, this is an indication that the core is too small. A maximum temperature rise of $100°C$ is chosen as the limit. This results in a core temperature of $150°C$ with an ambient temperature of $50°C$.

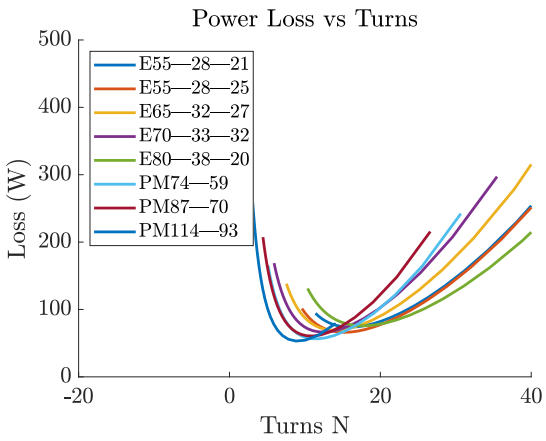


Figure 6.12: Optimization of the Inductor Turns

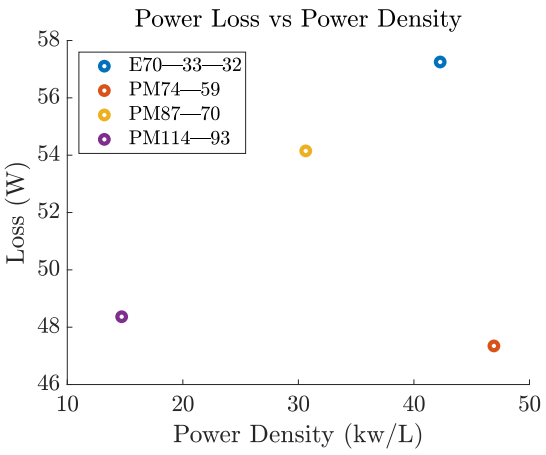


Figure 6.13: Power Density vs Losses of the viable designs. Only designs with a temperature spec within limits are selected.

From Figure 6.13 it is visible that the PM74-59 and PM114/93 have similar losses. Because the PM74-59 is more power-dense, this would be the preferred option. The final design is shown in Table 6.7. The Litz wire was optimized using Litzopt again but since the optimization gave similar results, the same Litz wire from Section 3.2 was used.

Table 6.7: Final Inductor Design

Parameter		Value
Core		PM74/59
Turns	N	10
Losses	P_{loss}	68.3W
Temperature Rise	ΔT	79.3°C
Power Density		47 kW/L
Max Flux	B_{max}	147mT
Wire		405x42AWG

6.5. Switch Selection

In this section, possible switches are compared and eventually, switches are selected for the final design. Switches are selected for the primary bridge, secondary bridge and switchover circuit. First, the voltage and current requirements for the switches are determined.

Switch Requirements

The voltage requirements for the switches are determined by the input and output voltages. The switches on the primary side are directly connected to the input supply and therefore need to withstand the maximum input voltage. The nominal input voltage is set to 750V maximum voltage will be set to 800V. The switch will be designed slightly higher to allow overshoots and allow derating of the switches. Normally 20% oversizing is recommended when the derating margin of the switches is taken into account [9]. This results in a voltage capability of at least 960V. For the secondary side, the switches only experience half of the maximum output voltage. The voltage rating of the secondary switches can thus be lower. The output voltage limit of a single module is 550V resulting in a minimum voltage capability of 660V for the secondary switches. The switches in the switchover circuit need to withstand the same voltage as the secondary side switches of the submodules. Whenever the voltage is above 550V (the submodule limit), the converter can only operate in series mode and Q_y is closed. In this case, the voltage over Q_x and Q_z is half of the output voltage. The switch Q_y can only be opened when the output voltage is below the submodule limit of 550V. Therefore, the switchover switches all need to withstand 660V. All the voltage limits are shown in Table 6.8.

The current requirements of the switches can be determined by the new output current and the new inductance. The output current of a single module is 46A. At this output current, the required phase shift can be calculated by Equation 3.9. The maximum output power P_{max} is calculated by Equation 3.8.

$$P_{max} = \frac{V_1 V_2}{8 f_s L} = \frac{800 \cdot 550 \cdot 2.1}{8 \cdot 100kHz \cdot 31\mu H} = 37.3kW \tag{6.21}$$

$$D = 0.5 - 0.5\sqrt{1 - P_{req}/P_{max}} = 0.5 - 0.5\sqrt{1 - 25/37.3} = 0.2129 \tag{6.22}$$

At this phase shift, the maximum current can be calculated by Equation 3.4 resulting in a current of 39A in the primary switches.

$$I_{max} = A(V_2(2D-1) + V_1) = 39A \tag{6.23}$$

This current is the maximal current at the primary side. The current is increased with 10% margin to 44A. The current on the secondary side needs to be multiplied with the turn ratio n = 2.1 resulting in 88A. The parallel switches of the switchover circuit Q_x and Q_z have to withstand the same current since the output filter is placed behind the switchover circuit. The series switch Q_y needs to withstand the same current since the output current of the converters is limited to the current limit of the submodules when the submodules are placed in series.

In Table 6.8 the switching frequencies of the specific switches are presented too. The switches Q_x, Q_y, and Q_z are switching with twice the switching frequency of the submodules.

Table 6.8: Voltage and Current limits for switches in the circuit

	Primary	Secondary	Q_{x+z}	Q_y
Voltage	960V	720V	720V	720V
Current	44A	88A	88A	88A
Frequency	100 kHz	100 kHz	200 kHz	200 kHz

Switch Type

In the previous section, the switch requirements were determined. In this section, a switch type will be chosen. Mosfets, Silicon Carbide (SiC) Fets, Gallium Nitride (GaN) Fets, and Insulated Gate Bipolar Transistors (IGBTs) were considered for this design.

In Table 6.9 a comparison between different switch technologies is shown. The switches are compared for their voltage capabilities, current capabilities, frequency capabilities, conduction losses, switching losses, and price. The switches are graded from high to low for each of the requirements.

Table 6.9: Comparison between different switch technologies

	Voltage	Current	Frequency	Conduction Losses	Switching Losses	Price
Mosfet	Low	Medium	High	High	Medium	Low
GaN Fet	Medium	Low	High	Medium	Low	Medium
SiC Fet	High	High	High	Medium	Low	High
IGBT	High	High	Low	Low	High	Low

When looking at the comparison in Table 6.9, the following can be noted. Mosfets are long used for high-power applications but their voltage capability is lacking behind compared to IGBTs, SiC and GaN. Some high voltage Mosfets are available but they often come at the cost of high $R_{ds,on}$. GaN fets are gaining more attention in the industry for their high frequency and high voltage capabilities. High voltage GaN switches are available for a good price but until now the current capabilities are not at the required level for this design. SiC fets are widely adopted by the industry especially, in high-power automotive applications. SiC fets provide high voltage and current capabilities with very low $R_{ds,on}$ and fast switching times. This makes them very suitable for high-power converters with high power density. The last technology to be considered is the IGBT. The IGBT can handle high voltages, high currents and offers low conduction losses. The downside of IGBT switches is the high-frequency limitation. Especially the turn-off time of the IGBT is high with values in the order of hundreds of nanoseconds. When the switching frequency increases the current capability of IGBT switches is decreased significantly. When considering the given comparison, the SiC Fet is chosen to be the optimal choice for all the switches.

Switch Comparison

A selection of commercially available devices is extracted from `https://www.digikey.com/`. To restrict the number of free variables, the switch selection is limited to the TO-247 package. This package is a common choice for high-power semiconductors and is often used within the research group. For SiC switches on the market, two common voltages above 720V are available: 750V and 1200V. In Figure 6.14 the selected switches are shown. The on-state resistance is one of the most important variables in this design since this influences the conduction loss in the switches. The switching loss is limited due to the ZVS during turn-on. A selection of candidates is shown in Table 6.10. The primary side switches need a withstand voltage of 1200V while the secondary side switches have to withstand 720V. Therefore, the switches on the secondary side can be different and different switches are selected for them.

The losses for the primary and secondary switches are modeled the same as in Chapter 3. A converter is modeled at an operating point from 800V to 550V with an output power of 12.5kW. In the calculation, the turn-on, turn-off, reverse recovery, and conduction losses are considered. The results are shown in Table 6.10, Figure 6.15, and Figure 6.16. The G3R30MT12K and UJ4SC075011K4S are chosen for the primary and secondary switches respectively.

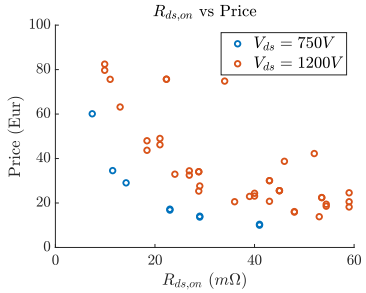


Figure 6.14: On resistance and price for a selection of 124 SiC switches from DigiKey

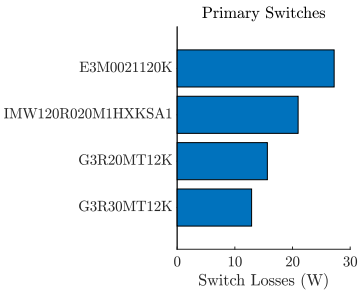


Figure 6.15: Best switch selection for the primary side

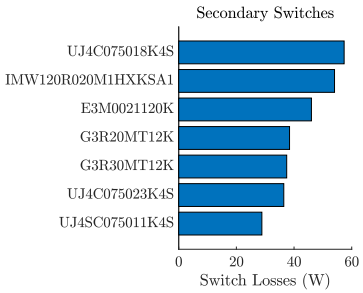


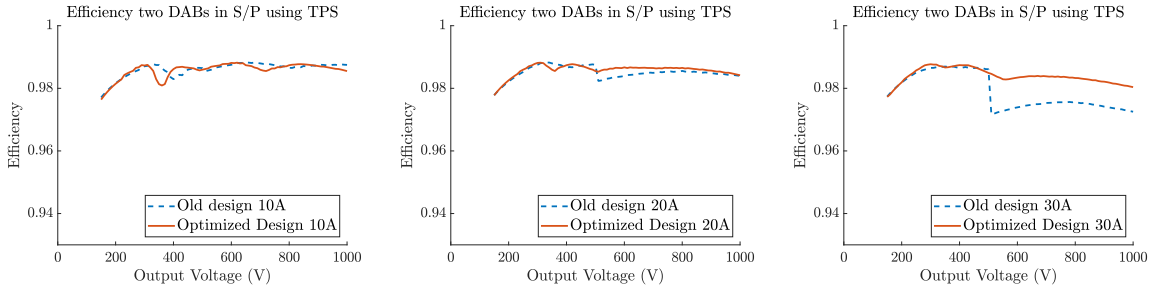
Figure 6.16: Best switch selection for the secondary side

Table 6.10: A selection of switch candidates taken from Figure 6.14. A selection of switches with the best prices and different $R_{ds,on}$ was chosen. For each switch, the conduction losses and switching losses are calculated for full power operation.

Switch	Mfr	Price	V_{ds}	I_d	$R_{ds,on}$	Q_{rr}	t_{rise}	t_{fall}	P_{cond}	P_{sw}	P_{tot}
Primary (1200V)											
G3R30MT12K	GeneSiC	€20.57	1200V	90A	$36m\Omega$	398nC	11ns	8ns	4.2W	8.7W	12.9W
E3M0021120K	Wolfspeed	€25.36	1200V	104A	$28.8m\Omega$	1264nC	39ns	13ns	3.4W	23.9	27.3W
IMW120R020M1HXKSA1	Infineon	€32.52	1200V	98A	$26.9m\Omega$	340nC	22ns	17ns	3.1W	17.8W	21W
G3R20MT12K	GeneSiC	€32.95	1200V	128A	$24m\Omega$	600nC	17ns	11ns	2.8W	12.8W	15.4W
Secondary (750V)											
UJ4C075023K4S	Qorvo	€14.06	750V	66A	$29m\Omega$	105nC	27ns	8ns	14.8W	21.5W	36.44W
UJ4C075018K4S	Qorvo	€17.22	750V	81A	$33m\Omega$	102nC	35ns	17ns	16.9W	40.4W	57.4W
UJ4SC075011K4S	Qorvo	€29.06	750V	104A	$14.2m\Omega$	288nC	26ns	9ns	7.3W	21.5W	28.8W

6.6. Efficiency

The converter is simulated with TPS modulation, the newly modeled switches, and the new inductor and transformer design. The losses are modeled in the same way as in Chapters 3. The resulting converter has an efficiency of >97.6% in the full operating range and a peak efficiency of 98.82%. Although the loss model was made carefully to simulate all the losses accurately, the results have to be interpreted with care. The model does not contain parasitic components or losses in the PCB and other wiring. The efficiency of a full scale model with most likely be slightly lower.



(a) 10A (b) 20AV (c) 30A

Figure 6.17: Final Efficiency of the full optimized circuit for different output currents and the full output voltage range

6.7. Conclusion

In this section, the circuit parameters of the DAB converters were optimized for maximum efficiency. First, the optimization was done for the full operating range at full power. Then, the optimization was adjusted to optimize a typical charging request at a home/public charger. Finally, the transformer and inductor designs were optimized and the best switches were selected. The final converter design is >97.6% efficient with a peak

efficiency of 98.82%.

7

Hardware Testing

Since the method of switchover is never done before, it is necessary to verify if the method is feasible on real hardware. A minified hardware setup is designed to verify if the designed switchover method is functional and to prove that it can ensure a smooth transition. In this section, the main design elements of the setup are discussed. Then, the hardware setup is tested and compared to the simulations.

7.1. Requirements

The goal of this setup is to test a full transition between series and parallel. The test setup needs to support the theory of SPSSO and prove the viability of a smooth transition using the switchover circuit. In this section, the requirements for the setup are discussed.

The Setup

A few possible methods were considered for testing. The easiest option for testing would be to use two lab-bench power supplies as submodules and then connect those to the input of the switchover circuit. Unfortunately, the behavior of the switchover circuit and especially the smoothness of the transition is very dependent on the DABs. This becomes clear in Chapter 4. To get a good feeling for the feasibility of the smooth transition method and the control, the DAB submodule is essential. For this reason, a test setup will be designed with two DAB converters as submodules.

Scaling

As mentioned before, the designed setup is a minified version of the real converter. The output voltage of a single submodule is chosen to be 24V nominal. With this voltage, two converters can safely be used in series without extra safety precautions in the lab. The output voltages are scaled to the values in Table 7.1 with a scaling factor of 12.5.

Parameter	Full Version	Prototype
Nominal voltage	400V	24V
Maximum voltage	500V	30V
Minimum voltage	150V	9V
Maximum current	30A	1.92A

Table 7.1: Converter output voltage scaling

The maximum current for each submodule is chosen to be 5A to keep some design margin. These limits will be used in the design when choosing components.

Easy Testing

The converter will mainly be tested in the ESP lab where plenty of equipment is available. It is however useful to allow testing with a simple test setup. This will ensure that testing can be done on lower-end equipment, which will be more abundantly available in the lab. The scaled-down voltages and currents are within the

limits of most lab-bench power supplies. For the load, a bidirectional power supply would be needed with a voltage capability of 60V. Although this device may be available, it would also be useful to test the converter with a simple resistor on the output. This requirement will be kept in mind during the design process.

Efficiency

The goal of this test setup is to verify the method of transition, including SPSSO. The efficiency of the converter is not a design requirement for this converter and thus no design optimization is done for this converter. The efficiency is however considered when selecting some of the components.

7.2. The Design

The design requirements in the previous section serve as a guide for the design process. In this section, a few important design decisions are considered. The circuit for the full setup is shown in Figure 7.1.

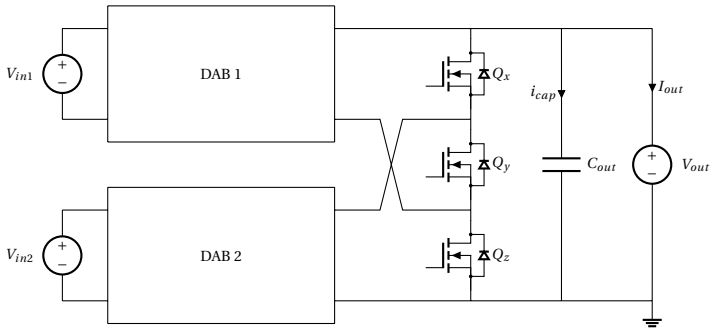


Figure 7.1: Layout of the test setup circuit

The setup consists of two DAB submodules with the switchover circuit and an output filter. The DABs are both supplied with separate power supplies to provide isolation of the converters. The reason for this is discussed in the next section.

Transformer and Inductor

To ease the design of the converter, it was chosen to omit the transformer in the DAB submodules. This would result in a 1:1 ratio between the input and output voltage. The circuit of a single submodule is shown in Figure 7.2. The converters do need to be isolated for the switchover to work. Therefore it is not possible to connect both submodules to the same power supply. Two isolated power supplies are used to provide the isolation needed.

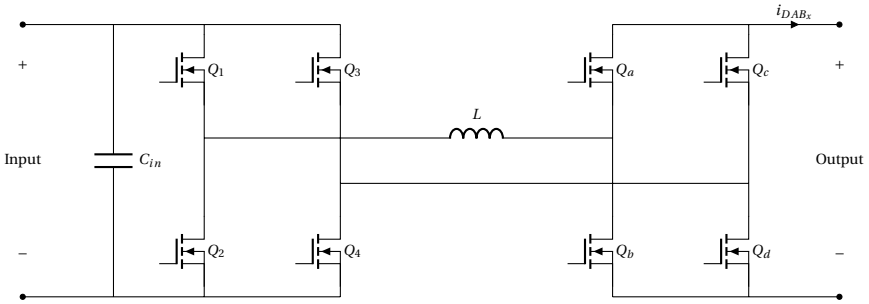


Figure 7.2: Circuit of a single submodule

The maximum inductor value can be calculated by considering the required output power and the switching frequency. The power equation from Equation 3.8 can be rewritten to get the maximum inductance as shown below.

$$L_{max} = \frac{V_1 V_2}{8 f_s P_{out}} \tag{7.1}$$

The frequency was lowered from 100 kHz to 50 kHz. This is done to ease the design since with higher frequencies parasitic effects become more prominent. First, 10 kHz was chosen but this would make the inductor size too big to find an off-the-shelf inductor. Finally, 50 kHz was chosen as a good compromise.

With a frequency of 50 kHz and a required output current of 5A, the maximum inductor current becomes

$$L_{max} = \frac{V_1 V_2}{8 f_s P_{out}} = \frac{24V}{8 \cdot 50kHz \cdot 5A} = 12\mu H \tag{7.2}$$

An inductor size of $10\mu H$ is chosen. The maximum inductor current can be calculated using Equation 3.2. When considering a maximum output voltage of 30V, the peak inductor current will be 15A.

$$I_{max} = \frac{1}{4 f_s L} V_{max} = \frac{30V}{4 \cdot 50kHz \cdot 12\mu H} = 15A$$

An off-the-shelf inductor is chosen with an inductance of $10\mu H$ and a maximum current of at least 15A. The SER2915H-103KL by Coilcraft is chosen. The specifications are shown in Table 7.2.

Parameter	Symbol	Value
Inductance	L	$10\mu H$
Maximum Current	I_{max}	30A
Saturation Current	I_{sat}	18A
DC Resistance	R_{dc}	1.86 $m\Omega$

Table 7.2: Specification of the Coilcraft SER2915H-103KL inductor

The inductor meets the requirements and will not saturate with the given current range. The DC resistance is good and according to the datasheet, the losses are low even at 100kHz switching frequency.

Capacitors

The input and output capacitors can be calculated based on the maximum input and output current ripple and the maximum allowed voltage ripple. The maximum allowed voltage ripple is set to 5%. The current through the capacitor is the difference between the output current of the switching leg and the average output current. The output current ripple will be the highest when the two submodules are connected in parallel and operating at maximum power. The capacitor current is calculated with Single Phase Shift modulation in mind.

$$I_{cap} = i_{sec}(t) - I_{out} \tag{7.3}$$

The charge that needs to accumulate in the capacitor during a period. The charge can be calculated by integrating the current over the positive half of the period.

$$Q_{cap} = \int_0^T i_{sec}(t) - I_{out} dt \tag{7.4}$$

In Figure 7.3 the capacitor current is shown for the maximum output power. The resulting charge becomes 70.07 μC.

$$Q_{cap} = \frac{1}{2} I_{pk} \Delta t = \frac{1}{2} 36.2A \cdot 3.9\mu s \cdot = 70.6\mu C$$

To keep the voltage ripple below 5%, the output capacitor needs to be at least $141\mu F$.

$$C_{out} = \frac{Q_{cap}}{\Delta V_{min}} = \frac{70.6}{0.05 \cdot 10V} = 141\mu F \tag{7.5}$$

A capacitor of 150 μF was installed.

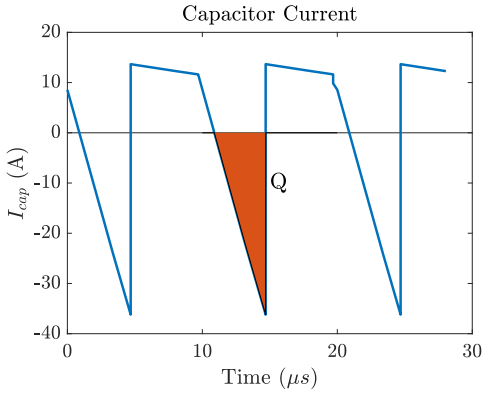


Figure 7.3: Capacitor current at max. output power with charge colored orange

Grounding and Isolation

The grounds of the two converters and their corresponding primary and secondary bridges can not be electrically coupled as this would create unwanted current flow. For this reason, four ground regions are created that each have their own power supply. The power supplies are covered in the next section. In this circuit, the negative terminal of the output circuit will be chosen as the reference ground as shown in Figure 7.1. This includes the negative output of the secondary bridge of DAB2. The microcontroller as well as the measurement IC will be connected to the reference ground. The ground plane of all other bridges will be isolated from the reference ground.

Supplies

Each bridge will have a small power supply. The power supplies are used to power the gate driver and to drive the gate pulses of the bridges. To keep as much freedom as possible to the range of the output voltage, the auxiliary electronics will all be powered from the primary input side since this voltage will remain stable during operation. The primary bridges will be powered by a linear voltage regulator from the respective input terminal. The secondary side will be powered by an isolated power supply. The isolated supplies are sourced from the primary input voltage. With this configuration, all the electronics are operational when an input voltage is supplied, and the gate drivers can operate independently of the voltage on the output of the submodule.

The primary supplies are simple 7815 linear regulators. They supply a stable 15V output with an output current of up to 1A. The secondary supplies are powered from the 15V primary supply with a TEA 1-1515 isolated supply. The supplies have a 1 to 1 output ratio and can supply up to 60mA.

Microcontroller

The chosen microcontroller should ideally be able to generate a high-frequency PWM to at least 9 output channels. This way, each DAB submodule can be controlled individually if needed. Two microcontrollers are considered; The TMS320F28379D and the STM32F334. The first microcontroller is from TI and offers 6 dual-channel PWM outputs. The advantage of this microcontroller is that it is often used in projects in the research group, the disadvantage is that I have no experience with this microcontroller family. Because the deadline for this hardware prototype was tight, the STM32F334 was chosen. The STM32F334 has five timers with two outputs per timer. All timers can be controlled by one master timer. Four timers are used to supply PWM signals to all the eight half bridges in the submodules and the last timer is used to supply the PWM to the switchover circuit. For each full bridge, the inner phase shift is controlled by the compare registers of timers A, B, C or D. The outer phase shifts are realized by the master timer compare registers. The master timer can reset the individual timers A-E using adjustable compare registers. The microcontroller is programmed using C and the LibOpenCM3 framework.

Switches and Drivers

The switches of the DAB converter and the switchover circuit are chosen to be N-channel Mosfets. The Mosfets are selected based on their low $R_{ds,on}$. The 'SIR680LDP-T1-RE3', with an $R_{ds,on}$ of $2.8m\Omega$, is chosen. The switches can handle a drain-source voltage of 80V and a drain current of up to 130A. The Mosfets are chosen

for the submodules and the switchover circuit.

For the DAB submodules, isolated half-bridge drivers are used to supply the gate signals. The driver takes in a single PWM signal at 3.3V signal level and features an adjustable dead time to prevent shoot-through. The gate of the high-side Mosfet is supplied by a bootstrap circuit.

The Mosfets for the switchover circuit (Q_x, Q_y, Q_z) are driven by three high-side drivers. Although the bottom Mosfet Q_z does not need a high-side driver, it was chosen to give all three Mosfets the same driver. This will keep the transmission delays from the input to the gate equal for all three Mosfets.

Q_y is supplied with a bootstrap circuit and Q_x is supplied with an isolated supply to ensure the voltage of the gate is driven to 5V above the source.

There are three relays connected in parallel with the switchover switches to reduce the conduction losses when no transition is needed.

Feedback and Measurments

In the end, the converter needs to perform a full transition with a stable output current. To accomplish this, the output current will be measured using a shunt resistor and a current amplifier. The amplified signal will be fed to the ADC of the microcontroller. The input voltages and the output voltage will also be measured as those are necessary for the calculation of the phase shift too.

The voltages are all measured using differential amplifiers. The input amplifiers have a gain of 13, giving a measurement range of up to 43V with a 3.3V ADC. The output amplifier has a gain of 22, giving a measurement range of up to 73V. The current will be measured using a 1mΩ shunt resistor and a TSC2012 current amplifier. The circuits for the current and voltage measurements are shown below.

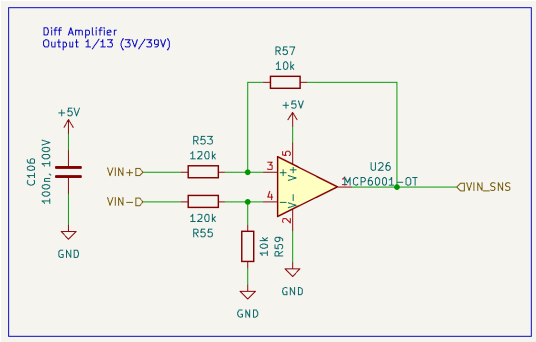


Figure 7.4: KiCAD schematics of the input voltage measurement circuit.

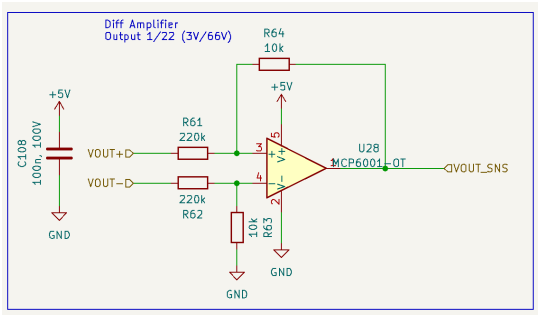


Figure 7.5: KiCAD schematics of the output voltage measurement circuit.

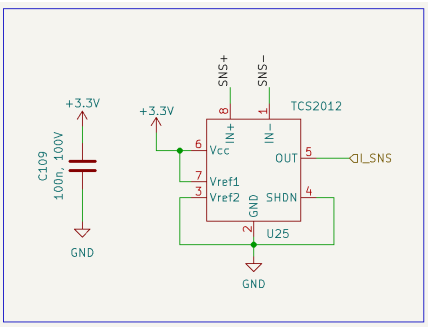


Figure 7.6: KiCAD schematics of the output current measurement circuit.

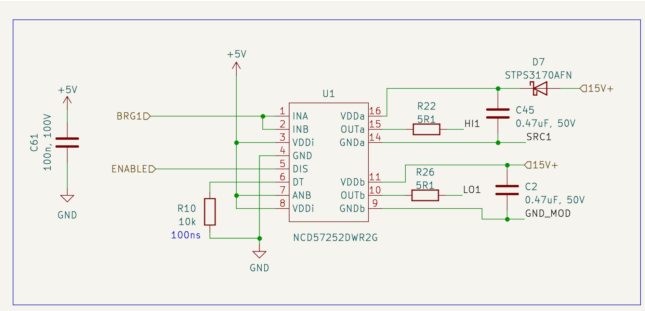


Figure 7.7: KiCAD schematics of the DAB gate drivers. One driver is used for each half bridge.

Circuit Board

The PCB is made in KiCAD and ordered at Eurocircuits. In Figure 7.8, the assembled PCB is shown. Components and traces are placed carefully to provide an optimal power path and low interference.

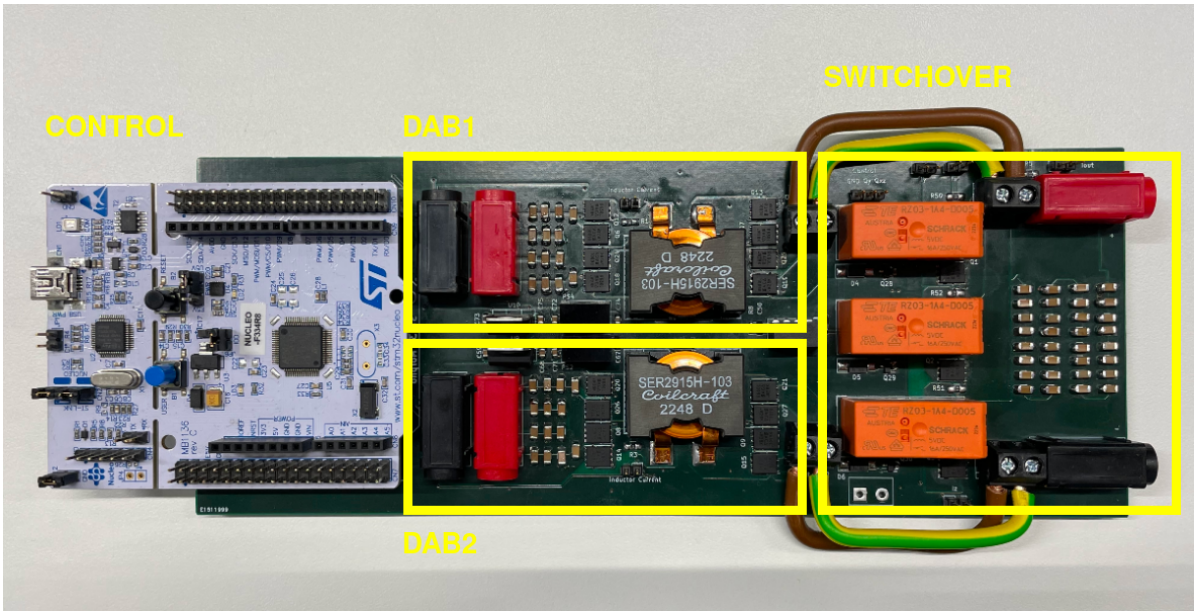


Figure 7.8: Fully assembled PCB with the indication of the submodules and the switchover circuit

7.3. Operation of the Submodules

Before the switchover is tested, the submodules are tested for functionality. The submodules are tested with an external output capacitor of $3300\mu F$ and a 5.5Ω load. The inductor current of a single submodule is compared with PLECS simulations of the same operating point. In Figure 7.9 both currents are shown. The converter is operating with SPS modulation and a phase shift of 5%. The current before the output capacitor is shown in Figure 7.10. This current is represented by i_{DAB_x} in Figure 7.2.

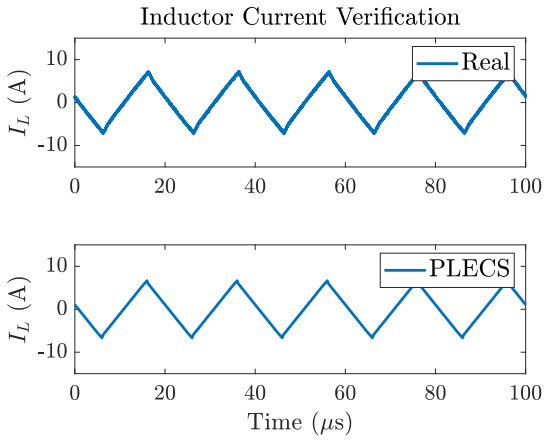


Figure 7.9: Inductor current from PLECS simulation and measurements from the setup. $V_{in} = 20V$, $D = 0.05$, $R_{load} = 5.5\Omega$

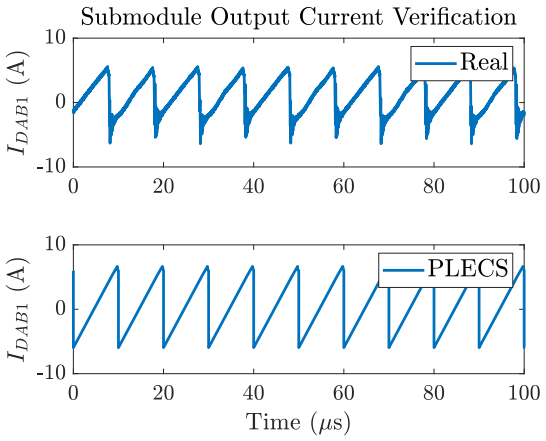


Figure 7.10: Output current from PLECS simulation and measurements from the setup. $V_{in} = 20V$, $D = 0.05$, $R_{load} = 5.5\Omega$

7.4. Transition

After the DAB submodules were tested, they were connected to the switchover circuit. First, the full converter was tested using a stationary D_x. The converters both had a phase shift of $D = 5\%$ and $D_x = 10\%$. The resulting waveforms for the inductor current I_L and output current I_{DAB_x} are shown in Figure 7.11 and Figure 7.12 respectively.

Now that the converters and the functionality of the switchover circuit are verified at a stable operating point, a full transition can be tested. The transition is done from parallel to series in Figure 7.13 and back

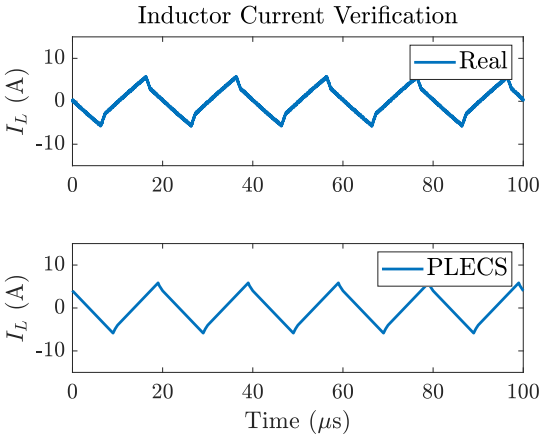


Figure 7.11: Inductor current from PLECS simulation and measurements from the setup. $V_{in} = 20V$, $D = 0.05$, $D_x = 0.1$, $R_{load} = 5.5\Omega$

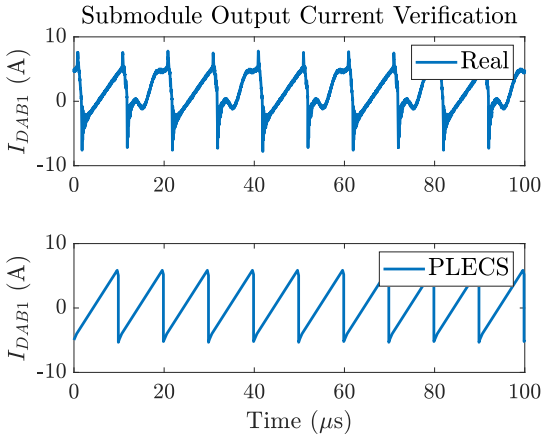


Figure 7.12: Output current from PLECS simulation and measurements from the setup. $V_{in} = 20V$, $D = 0.05$, $D_x = 0.1$, $R_{load} = 5.5\Omega$

from series to parallel in Figure 7.14.

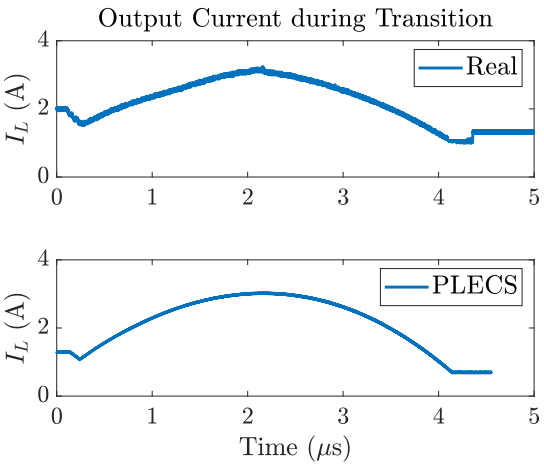


Figure 7.13: Output current from PLECS simulation and measurements from the setup during a full transition from Parallel to Series. $V_{in} = 20V$, $D = 0.05$, $R_{load} = 5.5\Omega$

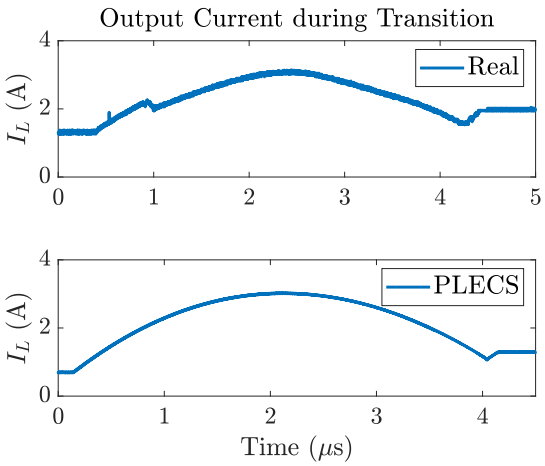


Figure 7.14: Output current from PLECS simulation and measurements from the setup during a full transition from Series to Parallel. $V_{in} = 20V$, $D = 0.05$, $R_{load} = 5.5\Omega$

The transition is done with a stable phase shift D so the output current is changing during the transition. The output current of the real setup is similar to the expected output current from simulations. In the next section, SPSSO is implemented to achieve a stable output current.

7.5. SPSSO

To get a stable output current during the transition, it is necessary to implement SPSSO in the microcontroller. Equation 4.42 is programmed into the microcontroller using C. The output current will be set to 3A while the output circuit transitions between parallel and series. To accommodate low currents using SPSSO, it is necessary to allow negative phase shifts D in the DAB converters. This is achieved by shifting the compare registers of the master timer to the center of the period. The resulting output current during transition is shown in Figure 7.15.

The current in Figure 7.15 shows a little ripple in the output current. The output current change is measured for some operating points to verify the deviation from the median current.

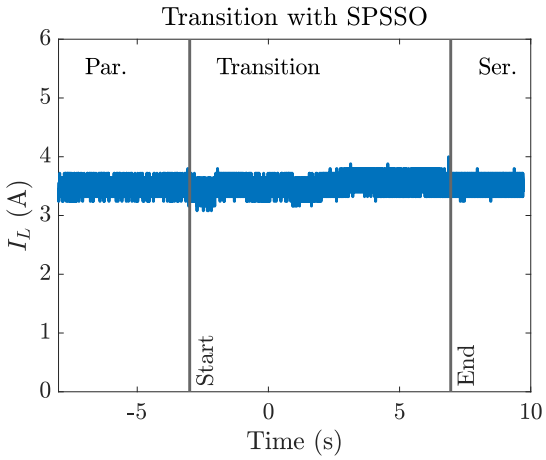


Figure 7.15: Output current during a full transition using SPSSO. $V_{in} = 20V$, $i^* = 0.3$, $R_{load} = 4\Omega$

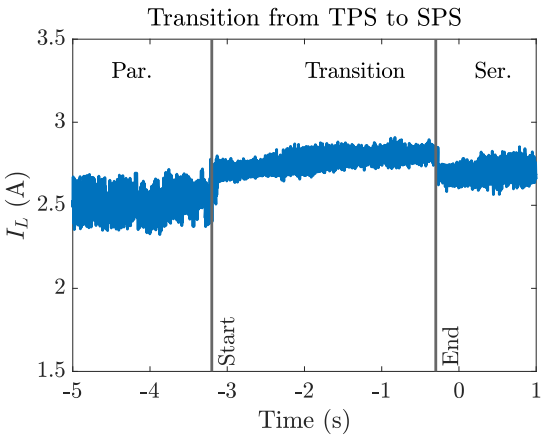


Figure 7.16: Output current during a full transition using TPS and SPSSO. $V_{in} = 20V$, $i^* = 0.2$, $R_{load} = 4\Omega$

7.6. TPSSO

Now that a transition in SPSSO is working, TPS can be implemented. First, TPS and MCSO are programmed into the microcontroller. Then, before a transition is about to happen, the phase shifts are adjusted to SPS. The outer phase shift D is changed to the calculated value from SPSSO and the inner phase shifts are switched to 0. In Figure 7.16, the switchover between TPS and SPS is shown. It can be observed that there are no oscillations but there is an observable difference between the amplitude of SPS and TPS.

7.7. Conclusion

In this Chapter, the method of SPSSO was verified on real hardware. A minified prototype was designed to test the switchover of two DAB converters and SPSSO modulation. The modulation was first verified with simulations for a transition where the phase shift D was not changed. This resulted in a similar value as obtained from simulations. Then, SPSSO was implemented to test a stable transition. Lastly, a transition between TPS and SPS was tested to verify that this is a viable solution to integrate TPS with the switchover method.

8

Results and Discussion

The goal of this thesis was to explore the design of a reconfigurable Dual Active Bridge (DAB) converter with series-parallel output and live transitioning. In Chapter 3, the design and model of a DAB converter were discussed. A preliminary design was made to model all the losses in the DAB. From these models, it became clear that the efficiency of the DAB converter suffers at low output voltage and low output power. To increase the efficiency even further, a comparison between different modulations was made. Triple Phase Shift was introduced and was able to increase efficiency to >96% in the full output range without losing efficiency in the optimal efficiency point.

In Chapter 4 a new method for reconfiguration, called SPSSO, was introduced. The method allows the DAB converter to reconfigure the output from series to parallel without the reduction of output power. The transition method is integrated with the modulation of the DAB to achieve a smooth output current during transitions. The method of reconfiguration and SPSSO was verified of hardware in Chapter 7. The method turned out to be viable and a smooth transition was achieved on real hardware.

Finally, the design of the full DAB converter was optimized to achieve the best efficiency in the full range. The optimization included; finding the optimal switchover voltage, optimizing the DAB inductor and transformer designs, and selecting the optimal switches for the primary and secondary sides.

8.1. Back to the Research Objective

In the introduction of this thesis, three research questions were posed. The three questions work together to answer the main research question. In this section, an answer is formulated to each of the research questions. In the last paragraph, the main question will be answered.

Live Transitioning

What topology and control methods can ensure smooth transitions, from series to parallel and vice versa, for two series-parallel-output DAB converters under live bidirectional power flow?

In Chapter 4, the switchover circuit and SPSSO were introduced to achieve a transition under live bidirectional power flow. The output circuit consists of three Mosfets Q_x, Q_y, and Q_z that can connect the two DAB submodules in parallel or series. By modulating the gate signals of the three switches together with the modulation of the DAB submodules, the converter can operate in a state between series and parallel. This method requires the output filter of the two DAB submodules to be behind the switchover switches and thus the output filter is integrated into one capacitor. The losses in the output circuit were modeled to assess the power distribution between the switches. The losses during a transition are high due to the lack of ZVS during a transition. Especially the middle switch Q_y will experience high switching losses. The total energy loss during a transition can be kept low by reducing the transition time. The transition time can be reduced to below 1s in simulations. One of the solutions to distribute the loss in output switches more evenly is the introduction of a phase shift in the signal D_x. By phase shifting the control signal to align with D_2 the switch Q_y will most likely benefit from ZVS due to a negative switch current. This relieves stress on the switch Q_y but the losses in Q_x and Q_x will increase. The transition method can be combined with range-enlarging modulation methods by transitioning back to SPSSO before transitioning.

Range Enlarging Modulation

Can advanced range-enlarging modulation schemes like DPS, EPS or TPS increase the efficiency over a wide output and power range?

To improve the efficiency of the DAB converter in a wide output range, other advanced modulations were compared in Chapter 3. A comparison between Single Phase Shift (SPS), Dual Phase Shift (DPS), and Triple Phase Shift (TPS) was made. For DPS modulation, two different optimization strategies were compared; peak current optimization, and RMS current optimization. Both optimizations were performed using constrained gradient based optimization in Matlab. TPS was modeled with Minimum Current Stress Optimization (MCSO), an optimization method proposed by [40]. From the comparison between DPS and TPS, TPS was the clear winner. TPS succeeded at reducing peak current and extending the soft switching region to the full operating range. The efficiency of the DAB using TPS was increased in all operating conditions but especially at low power the advantage was large.

Optimization

How can the operating point of the series-parallel-output DAB converter be optimized to ensure maximum efficiency in all operating conditions?

In Chapter 6, the design of the submodules was optimized to achieve the highest efficiency. The inductor and transformer were optimized to reduce losses and the best switches were selected for the primary and secondary side. First, the optimization was performed for maximum power. To make the optimization better suited for EV charging application of this thesis, the optimization was adapted to optimize the efficiency for common operating conditions. The design was optimized for common voltages (400V, 600V, 800V) and common charging powers taken from [42]. The final converter achieves an efficiency of >97.6% in all operating conditions according to simulations. Unfortunately, the efficiency of the converter could not be verified on real hardware since the design of a full-scale converter did not fit in the scope of this project.

Main Research Question

Can two DAB converters in series-parallel-output configuration extend the efficiency over a very wide voltage and power range?

In this thesis a design for two DAB converters with series-parallel output is proposed that can achieve very high efficiencies of >97% in the full voltage range (150V-1000V) and power range (4kW-25kW).

8.2. Limitations

The methods in this thesis are selected carefully to give the best balance between accuracy and speed. Unfortunately, everything in life comes with limitations. The limitations are discussed in the sections below.

Modelling of the DAB

The model presented in Chapter 3 comes with a few limitations. The winding capacitance in the inductor and transformer are neglected and the series inductance of the input and output filter are not modeled too. Parasitic capacitance, inductance and resistance in the switches are not taken into account. Due to these limitations, the loss model will not be 100% accurate but it will give a fair estimation of the losses.

Modulation

In Chapter 3 TPS and DPS modulation were compared to SPS. EPS modulation was kept out because other sources [39] already performed comparisons between the two. EPS modulation may perform better in a situation with series-parallel output but it is considered unlikely.

Dynamics and Parasitics

Unfortunately, it was not possible to do thorough dynamic modeling within the time of this thesis. The models used in this thesis do not include parasitic capacitances, inductances and resistances. Therefore, the stresses and stability during a transition can deviate from the simulated values.

Hardware
A transition is tested on real hardware. In contrast to the full power design, the hardware prototype did not include transformers. The hardware prototype was designed to test the transition and not the operation or efficiency of TPS. This is therefore yet to be discovered on a full-scale prototype.

Efficiency
The reported efficiencies are all a result of simulations in Matlab or PLECS. The parasitic components are not modeled and wire/trace resistances are neglected. Although the efficiency models are designed to be as accurate as possible, the efficiency of the full-scale model will most likely be lower.

Bi-directional Efficiency
In hindsight, the efficiency of the converter during V2G operation is underexplored. Although the possibilities for bidirectional current were explored during the modulation in Chapters 3 and 4, the efficiency is not yet verified during a reverse current.

Core Selection
The core selection in the optimization in Chapter 6 is limited. For the transformer model only E cores were considered and for the inductor E and Potted types were compared. It is therefore likely that another core shape can improve the efficiency even further.

PID Controller
In Chapter 5, a method with a PID controller was suggested to keep the output current stable. The controller was able to keep the current stable but only with slow transitions of 5s or more. The method of tuning can be questioned here. Now a Ziegler-Nichols method for fast response was used but another controller design may perform better with fast transitions. This is therefore a recommended subject for future work.

Frequency
In this thesis, the switching frequency of the converter was fixed at 100kHz. It is possible that the converter will be more efficient at another switching frequency.

Dead Time
In the derivation of SPSSO, dead time was not considered. Experimental simulations in PLECS showed that the deadtime has a small influence on the output current. The effects have to be explored more.

8.3. Future Work
The presented thesis gives opportunities for new research. In this section, a few topics are discussed.

Dynamic Modelling
The simulations of the presented converter do not simulate the dynamics of the converter. Testing the converter and especially the transition method with an accurate dynamic model would be useful to identify possible bottlenecks in the design of the converter.

Full Scale Prototype
The results in this thesis are promising and it is therefore worthwhile to test the presented converter on a full-scale prototype.

Live Transitioning
The live transitioning method SPSSO gives a sea of opportunities for future research. One particular subject is the balancing of the two converters. During hardware testing, the balance of the two converters changed during the transition. This is due to small component and control-signal mismatches. By adjusting the control signals of the DAB submodules these imbalances can be compensated. Apply advanced balancing techniques to the series, parallel, and transition modes could be a good subject for a research project.

Transition in TPS

In Chapter 5, the live transitioning modulation was integrated with TPS and MCSO. Multiple methods of integration were proposed and simulated and eventually, the best solution turned out to be a transition in SPSSO whereby the converter will first transition back from TPS to SPS and then does a transition in SPSSO. This method is however less efficient because the losses with SPS are higher. Integrating TPS and MCSO into the transition method to form TPSSO could be a good research project to increase the efficiency even further.

Other Topologies

In this thesis, the submodules were based around a DAB converter and the presented reconfiguration method is highly integrated with the modulation of the DAB. It could however be possible to integrate this method of 'switched transitioning' into other converter topologies. An exploration of the possibilities to perform live transitions on other topologies would be a great research topic that can open new doors to other topologies and designs.

9

Conclussion

In this thesis, the design of two Dual Active Bridge (DAB) converters with series-parallel output and live transitioning is presented. A novel method of reconfiguration is proposed to achieve a smooth transition between series and parallel under live bidirectional power flow. The new live transition method was verified on a hardware prototype of 200W. A 25kW version is modeled using Matlab and PLECS and the DAB converter is optimized for high efficiency in the full operating range (150V-1000V). A comparison between different modulations is performed and Triple Phase Shift (TPS) with Minimal Current Stress Optimization (MCSO) is implemented. The optimized 25kW converter achieves a peak efficiency of 98.8% with an efficiency of >97.6% over the full operating voltage (150V-1000V) and power (4kW-25kW).

A

Inductor Current TPSSO

In this Appendix, the inductor current calculations for TPS with Switchover are presented. The modulation consists of 12 operating modes as defined in Equation A.1. The current calculation is shown in the form of a matlab script. All the values used in the script can be found in Chapters 3, 4, and 5.

$$\begin{aligned}
&\text{Mode 1: } D_1 \le D_2 \le D_3 \le D_x \\
&\text{Mode 2: } D_1 \le D_2 \le D_x \le D_3 \\
&\text{Mode 3: } D_1 \le D_x \le D_2 \le D_3 \\
&\text{Mode 4: } D_x \le D_1 \le D_2 \le D_3 \\
&\\
&\text{Mode 5: } D_2 \le D_1 \le D_3 \le D_x \\
&\text{Mode 6: } D_2 \le D_1 \le D_x \le D_3 \\
&\text{Mode 7: } D_1 \le D_x \le D_1 \le D_3 \\
&\text{Mode 8: } D_x \le D_2 \le D_1 \le D_3 \\
&\\
&\text{Mode 9: } D_2 \le D_3 \le D_1 \le D_x \\
&\text{Mode 10: } D_2 \le D_3 \le D_x \le D_1 \\
&\text{Mode 11: } D_2 \le D_x \le D_3 \le D_1 \\
&\text{Mode 12: } D_x \le D_2 \le D_3 \le D_1
\end{aligned} \tag{A.1}$$

```
A = 1/(8*fs*L);

if D1 <= D2 && D2 <= D3 && D3 <= Dx
    % Checked
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 - Dx*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 4*D1*V2 - 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I2 = A*(V2 - 2*V1 - 2*D1*V1 + 4*D2*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 - 2*D1*V1 + 2*D2*V2 + 4*D3*V1 - 2*D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 + 4*Dx*V1 - 3*Dx*V2);
elseif D1 <= D2 && D2 <= Dx && Dx <= D3
    I0= -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + D3*V2);
    I1= -A*(2*V1 - V2 - 2*D1*V1 - 4*D1*V2 + 2*D2*V2 + D3*V2);
    I2= -A*(2*V1 - V2 + 2*D1*V1 - 4*D2*V1 - 2*D2*V2 + D3*V2);
    I3= -A*(2*V1 - V2 + 2*D1*V1 - 2*D2*V2 + D3*V2 - 4*Dx*V1);
    I4= -A*(2*V1 - V2 + 2*D1*V1 - 2*D2*V2 - 4*D3*V1 + D3*V2);
elseif D1 <= Dx && Dx <= D2 && D2 <= D3
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 + Dx*V2);
```

```
    I1 = -A*(2*V1 - V2 - 2*D1*V1 - 4*D1*V2 + D2*V2 + D3*V2 + Dx*V2);
    I2 = -A*(2*V1 - V2 + 2*D1*V1 + D2*V2 + D3*V2 - 4*Dx*V1 - 3*Dx*V2);
    I3 = A*(V2 - 2*V1 - 2*D1*V1 + 4*D2*V1 + D2*V2 - D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + D2*V2 + 4*D3*V1 - D3*V2 + Dx*V2);
elseif Dx <= D1 && D1 <= D2 && D2 <= D3
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 + Dx*V2);
    I1 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 - 3*Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D1*V2 - D2*V2 - D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 - 2*D1*V1 + 4*D2*V1 + D2*V2 - D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + D2*V2 + 4*D3*V1 - D3*V2 + Dx*V2);
elseif D2 <= D1 && D1 <= D3 && D3 <= Dx
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 - Dx*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 - 2*D1*V1 + 2*D2*V2 + 4*D3*V1 - 2*D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 + 4*Dx*V1 - 3*Dx*V2);
elseif D2 <= D1 && D1 <= Dx && Dx <= D3
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + D3*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I3 = -A*(2*V1 - V2 + 2*D1*V1 - 2*D2*V2 + D3*V2 - 4*Dx*V1);
    I4 = -A*(2*V1 - V2 + 2*D1*V1 - 2*D2*V2 - 4*D3*V1 + D3*V2);
elseif D2 <= Dx && Dx <= D1 && D1 <= D3
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + D3*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I3 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I4 = -A*(2*V1 - V2 + 2*D1*V1 - 2*D2*V2 - 4*D3*V1 + D3*V2);
elseif Dx <= D2 && D2 <= D1 && D1 <= D3
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 + Dx*V2);
    I1 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 - 3*Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + D2*V2 - D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 + 2*D1*V1 + D2*V2 - D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + D2*V2 + 4*D3*V1 - D3*V2 + Dx*V2);
elseif D2 <= D3 && D3 <= D1 && D1 <= Dx
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 - Dx*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 + 2*D1*V1 - 4*D1*V2 + 2*D2*V2 + 2*D3*V2 + Dx*V2);
    I4 = A*(V2 - 2*V1 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 + 4*Dx*V1 - 3*Dx*V2);
elseif D2 <= D3 && D3 <= Dx && Dx <= D1
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + 2*D3*V2 - Dx*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - 2*D3*V2 + Dx*V2);
    I3 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 + 2*D3*V2 - 3*Dx*V2);
    I4 = A*(V2 - 2*V1 + 2*D1*V1 - 2*D1*V2 + 2*D2*V2 + 2*D3*V2 - Dx*V2);
elseif D2 <= Dx && Dx <= D3 && D3 <= D1
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + 2*D2*V2 + D3*V2);
    I1 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I3 = A*(V2 - 2*V1 + 2*D1*V1 + 2*D2*V2 - D3*V2);
    I4 = A*(V2 - 2*V1 + 2*D1*V1 - 2*D1*V2 + 2*D2*V2 + D3*V2);
elseif Dx <= D2 && D2 <= D3 && D3 <= D1
    I0 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 + Dx*V2);
    I1 = -A*(2*V1 - V2 - 2*D1*V1 + D2*V2 + D3*V2 - 3*Dx*V2);
    I2 = A*(V2 - 2*V1 + 2*D1*V1 + D2*V2 - D3*V2 + Dx*V2);
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        I3 = A*(V2 - 2*V1 + 2*D1*V1 + D2*V2 - D3*V2 + Dx*V2);
        I4 = A*(V2 - 2*V1 + 2*D1*V1 - 2*D1*V2 + D2*V2 + D3*V2 + Dx*V2);
    else
        I0=0;
        I1=0;
        I2=0;
        I3=0;
        I4=0;
    end
```

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