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# Online Detection of Unique Faults in RRAMs

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***Abstract*—Due to the immature manufacturing process, Resistive Random Access Memories (RRAMs) are prone to exhibit new failure mechanisms and faults, which should be efficiently detected for high-volume production. Those unique faults are hard to detect but require specific Design-for-Test (DfT) circuit design. This paper proposes a DfT based on a parallel-reference write circuit that can detect all RRAM array faults during diagnosis, production testing, and its application in the field.**

***Index Terms*—RRAM, Defects, Faults, Test, DfT**

## I. Introduction

Resistive Random Access Memory (RRAM) is a promising technology for future non-volatile memory due to its benefits such as high scalability, low access latency, and energy efficiency for AI computing [1]. However, variations and defects in device characterization during production and their impact on product quality pose substantial challenges [2]. In addition, the production of RRAM requires extra procedures and the utilization of novel materials, potentially leading to the appearance of new failure mechanisms [3]. Moreover, the existence of parametric derivation of the device degrades the memory block reliability without logical faults, which may escape traditional logic tests [4]. Hence, it is crucial to have a thorough comprehension of manufacturing defects and the development of high-quality test solutions.

Several works have investigated test solutions for RRAMs. Those proposed solutions can be divided into March algorithms and specific Design-for-Test (DfT) solutions. These March algorithms can detect conventional RRAM faults, but are not designed to detect unique faults, such as undefined state faults. To detect those unique faults, DfT schemes are employed, such as weak write operations [5], On-Chip Sensor [6], DFT-HR-ET-NOR [7]. They can partially detect unique RRAM faults, but cannot guarantee the detection of the complete set of faults. In particular, they only detect the fault after manufacturing and strong faults that lead to logical errors. These limitations hinder the use of DfTs for reliability purposes as they cannot detect faults consistently. To address this, PMRR DfT [8] is proposed to compare the input against multiple references online in the field. However, it is still unable to detect weak faults that do not lead to logical errors. Clearly, there is no test solution for RRAMs that is capable of detecting all array faults.

This paper presents a new, easily trimmable DfT scheme based on monitoring the write current during the operation for testing RRAM memories. The circuit replaces standard write drivers. Instead, the proposed DfT scheme monitors the write current and compares it against multiple references simultaneously and thus can detect the faults. The scheme can do this during diagnosis and yield learning, during manufacturing tests, as well as in the field.

## II. Targeted RRAM defects and faults

The RRAM switches between a high resistance state (logic 0) and a low resistance state (logic 1) by applying a positive or negative voltage. Defects and faults may occur to affect the functionality and reliability of the device.

### A. RRAM Conventional Defects

Conventional defects consist of interconnects and contacts in RRAM arrays, which can cause bridges, shorts, and opens. They are typically modeled by *linear resistors* [9].

### B. RRAM Unique Defects

Unique defects are inside the RRAM itself. They are accurately modeled by the DAT approach, which accurately describes the physical and non-linear behavior of the defect.

### C. RRAM Faults

Manufacturing defects can lead to erroneous behavior or a derivation from the correct behavior. Those behaviors of defects are modeled as faults on the functional level. Faults describe the defect's behavior in terms of applied operations that sensitize the fault and the stored cell states after sensitization of the fault.

There are different types of faults. First, each fault can be either strong or weak [4]; a strong fault is always sensitized by operations with functional errors at time 0, while a weak fault does not cause any functional errors but parametric deviations out of the spec (e.g., a voltage drop in the BL during a writing operation). Depending on the ease of detection, partial strong faults are *guaranteed* to be detected by regular operations (i.e., March test) and called *Easy-to-Detect (EtD)* faults. Other strong faults that have no deterministic behavior (e.g., risky random read) are *strong Hard to Detect (sHtD)* faults. All weak faults are *weak Hard to Detect (wHtD)* faults. Moreover, there are permanent (always occur) and intermittent (not in every cycle) faults. The intermittent faults occur with probability due to the variation of the RRAM and are classified as sHtD faults.

Therefore, those different types of faults are all needed to be detected to reduce the test escape.

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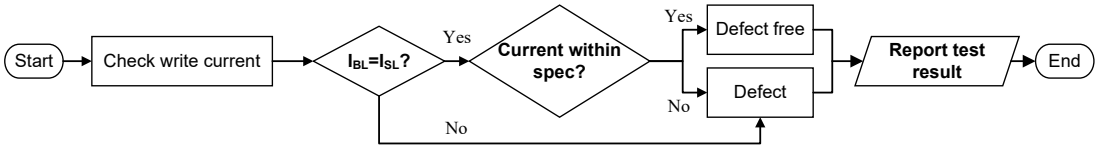
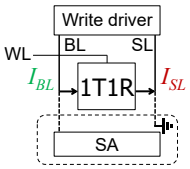



Fig. 1. The flow chart of the proposed DfT process.




| Condition | $I_{BL}$ | $I_{SL}$ |
|---|---|---|
| (1) | Correct | Correct |
| (2) | Correct | Incorrect |
| (3) | Incorrect | Correct |
| (4) | Incorrect | Incorrect |

Fig. 2. The concept of $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$ conditions during the write operation.

## III. Proposed DfT Methodology

Based on the discussion from previous sections, we can derive that a high-quality DfT scheme for RRAMs should be able to detect specific faulty states ('H', 'U', and 'L' states). For those parametric derivations without functional errors, weak faults should also be detected to enhance the chip's reliability. Furthermore, to detect aging degradation and intermittent behavior, the test should be performed during the runtime of the chip (e.g., in-field test).

To satisfy these requirements, we designed the DfT based on monitoring and comparing online write currents for fault and defect detection. By modifying write drivers, write currents can be online monitored during the write operation; thus achieving test without additional read operations. For instance, during the SET operation, currents from the write driver flow into the RRAM cell through BL ($I_{\mathrm{BL}}$) and out of the cell through SL ($I_{\mathrm{SL}}$). Totally, there are 4 conditions of $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$, as listed in Fig. 2. For a defect-free circuit, $I_{\mathrm{BL}}$ is expected to be the same as $I_{\mathrm{SL}}$, both of which are within the spec. However, there is an observation that some bridge and short defects can introduce extra current as a sneak path, which makes the current difference between $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$. Besides, some defects (e.g., opens) result in the same $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$, both of which are out of the spec.

Therefore, we notice that both $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$ can provide information to facilitate the defect/fault detection. To reduce the test escape, the large difference between $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$ can be measured and indicate the presence of defects. Furthermore, the same amplitude of $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$ cannot ensure the cell is defect-free since condition (4) exists; hence the magnitude of the write current should still be measured. We propose the DfT method based on write current comparison, as shown in Fig. 1. The process consists of two stages: 1) check the current difference of $I_{\mathrm{BL}}$ and $I_{\mathrm{SL}}$; 2) further check the magnitude of $I_{\mathrm{BL}}$ or $I_{\mathrm{SL}}$ in case they have the same magnitude. Note that it is a simultaneous detection with performing write operations.

## IV. Validation of DfT Methodology

To validate the proposed DfT, we implement the 1T1R RRAM array with read circuits and proposed write drivers. We use the TSMC $40\,\mathrm{nm}$ $2.5\,\mathrm{V}$ transistor model, and the JART VCM v1b [10] RRAM device model to implement the circuit. The circuit is simulated in Cadence's Spectre simulator.

First, the defect-free circuit is validated to perform both write and read operations. Then, we validate the DfT's defect-detecting capabilities by injecting defects into the netlist. We inject resistive defects in one memory cell, one defect at a time, and sweep their size (strengths) from $1\,\Omega$ up to $100\,\mathrm{M}\Omega$ in 81 logarithmically spaced steps. We apply all static sensitizing sequences, i.e., 0w0, 0w1, 1w0, 1w1, 0r0, 1r1. We observe that the fault coverage achieved by the proposed DfT is complete with both strong and weak faults. The detection range of defects is superior to those of existing test solutions.

## V. Conclusion

This paper proposed a novel write current monitor DfT that can guarantee the detection of all array faults that exist in RRAMs. It replaces the regular write drivers with a circuit that can drive the cell and measure the write currents at once. This allows for fast and efficient detection of faults not only during production testing but also in the field. Different from other memories such as STT-MRAMs, there are more faulty states and the intrinsic stochasticity of RRAMs, which lead to unique faults, and thus the test escapes. Therefore, the complete analysis of RRAM-related faults is essential to facilitate the design of testing and enhance the test coverage.

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