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***Abstract*—This brief presents an ultrasonically powered microsystem for deep tissue optogenetic stimulation. The developed system is composed of a Base for Powering and Controlling (BPC) and an implantable Dust for optogenetics and drug delivery. The Dust consists of a piezoelectric crystal, a rectifier chip, and a micro-scale custom-designed light-emitting-diode (μLED) integrated, miniaturized, and envisioned to be used for freely moving animal studies. The proposed Dust operates in frequencies up to 5 MHz, power levels in the 0–10 mW range, achieves start-up within 1.8 μs at 2.9 MHz operating frequency at 14.4 mW/mm^2 ultrasound power density, and 98.1% chip efficiency at 2 mW input power. With the BPC implemented and attached to (500 μm)^3 PZT4 crystals, set to 60 V at 2.8 MHz operating frequency at 3 mm distance in demineralized water, the dust delivered up to 6 mW to its load (μLED for optogenetics), which translates to 0.11% total system efficiency.**

***Index Terms*—Dust, optogenetic stimulation, rectifier, piezoelectric, ultrasonic power transfer.**

I. Introduction

As TECHNOLOGY and medicine come together, exciting new possibilities for treatment arise and theoretical concepts transform into tangible electronic devices that can be increasingly miniaturized. One particular concept of micro-sized electronic-based devices, known as neural Dust [1], [2], [3], has shown the potential to be used for deep brain recording and stimulation. This opens up the possibilities for *in vivo* optogenetics, electrophysiology, and triggered localized drug delivery. Although the development of such a device is highly challenging, it holds potential for treating neurological disorders like Parkinson's Disease (PD) and Alzheimer's Disease (AD).

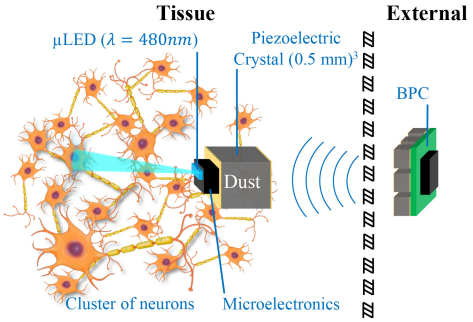

Fig. 1. Conceptual sketch of a neuron illuminated by a Dust, which is powered ultrasonically by a BPC.

Focusing only on optogenetic applications reduces the system to simply powering a Dust with an LED as the light source, and the BPC functioning only as a power-source for the Dust, as illustrated in Fig. 1. Designing a Dust for optogenetics, however, requires it to be millimeter-sized or even sub-millimeter-sized with the possibility of being powered at depths of several centimeters below the skin in the case of human subjects. The first requirement is the physically small size of the Dust due to the intention of testing it on mice, where the space at the targeted location in their brain is limited to approximately 500 μm^3. Regarding the second requirement, ultrasound, with its low tissue attenuation of about 0.5-1 dB/cm/MHz [2], allows for powering implants based on piezoelectric crystals at much greater depths [4], [5], [6], [7].

To enable the crystal to interface the load properly, a power management block is necessary in between. This block will consist of a rectifier which will convert the input AC signal into a DC signal, and a storage capacitor that will store the converted energy. The widely known passive diode-based bridge is the simplest form of a rectifier, but unfortunately suffers from a very high voltage drop resulting in both poor voltage and power conversion efficiency of the Dust. To resolve the aforementioned disadvantages, active rectifiers have been proposed [1], [2], [6], [8]. One of the challenges of these types is a safe and fast start-up of the system before the internal DC supply rail reaches a minimum level of normal operation.

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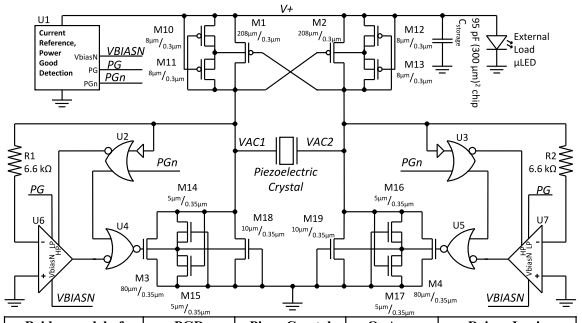

Bridge model of operation	PGD		Piezo Crystal		OpAmp		Driver Logic	
	PG	PGn	VAC1	VAC2	U6	U7	U4	U5
Passive, Start-up	Low	High	N/A	N/A	Off	Off	Disable	Disable
Active, running	High	Low	Low	High	HP	LP	Enable	Disable
Active, running	High	Low	High	Low	LP	HP	Disable	Enable
Active, intermittent	High	Low	High	High	LP	LP	Disable	Disable

Fig. 2. Top-level schematic of the dust active bridge rectifier. Modes of operation are shown in the table.

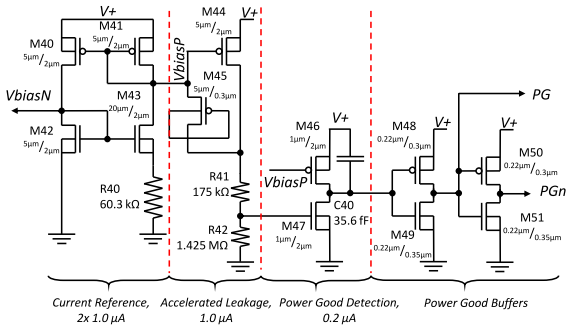

Fig. 3. Current reference and PGD sub-circuit of the Dust.

In our work, a new Dust with passive diode-connected transistors in parallel to active diodes with adaptable power modes is implemented, and a new circuit is proposed to speed up the start-up process of the Dust. Furthermore, we have developed a counterpart of the Dust, known as BPC, which drives a 2 by 2 PZT4 transducer in order to power up the Dust for optogenetics applications. In the next section, the system architecture and the circuit designs are explained. Section III is devoted to the system integration and the measurement results, and the last Section concludes this brief.

II. Proposed Fully Integrated Microsystem

A. Implantable Dust

The top-level schematic circuit of the proposed active-bridge rectifier in the Dust is shown in Fig. 2. The main current paths are four switches, two cross-coupled PMOS transistors (M1,2), and two controlled NMOS transistors (M3,4) used as active diodes, and their respective body biasing transistors to prevent latch-up (M10-17). Furthermore, the diode-coupled NMOSs (M18,19) are used during start-up when M3,4 are held OFF by the controlling logic of the Power Good Detection (PGD) circuit, U1. The PGD keeps the system in a passive rectification safe-mode until power levels have risen high enough for normal active rectification to begin. This design has no over-voltage protection since the normal operating voltage of the system is approximately 2.5 V, which is dictated by the blue μLED (480 nm wavelength) that will load the rectifier.

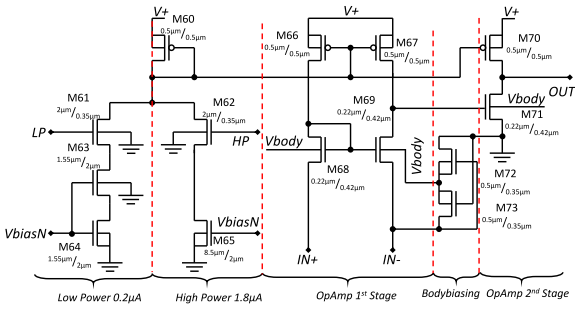

Fig. 4. Schematic of the adaptable OpAmp in the Dust rectifier with adjustable drive current.

The sub-circuit of the active rectifier seen in Fig. 3 contains two functions; 1) a current-reference for the OpAmps biasing voltage; 2) a PGD circuit that based on current supply levels controls whether the system is in a passive rectification safe-mode or running normally with active rectification. Shared between them sits a circuit based on the principle of accelerated leakage [9], which ensures the current reference starts up correctly and rises towards its nominal reference value of 1.0 μA. The PGD sets the logic circuits to keep the bridge in a passive rectifier safe-mode until the current reference reaches approximately 85% of the nominal value, at which point it triggers the logic for normal active rectification.

To control the two main switches, M3,4, two OpAmps are utilized, U6,7 (shown in Fig. 2), respectively, with a common-gate configuration of the first stage, and a single-ended amplifier for the second stage, as seen in Fig. 4. To manage the power, U6,7 include an adaptable current mirror circuit that selects between different current biasing modes. Three modes are used here by setting the two inputs LP (Low Power) and HP (High Power), and thereby disabling or enabling one or both current branches of the OpAmps: 1) Offline mode; both current branches are disabled, which is used in the bridge passive mode to save power during start-up. 2) LP mode; 0.2 μA bias current (0.8 μA total), only the low power branch is enabled, thereby biasing the individual OpAmp to an operational working point, but with a severely reduced unity gain bandwidth of 232MHz and an open loop gain of 63 dB. 3) HP mode; 2.0 μA bias current (8.0 μA total), both the low and high power branches are enabled and the individual OpAmp is biased and operating at the full bandwidth of 1.27 GHz and a gain of 62 dB. The OpAmps (U6,7) are kept in offline mode during start-up, however, they have both an LP and HP power mode for active bridge rectification mode. The reason for this lies in the fact that while one OpAmp is driving its respective main switch (M3,4) at a given time, the complementary OpAmp can enter an LP mode where it retains its operating point to keep its output stable, allowing for quick recovery back to HP mode. This works by taking advantage of the fact that the signals VAC1,2 from the piezoelectric crystal are essentially two opposing square-waves with respect to common ground under normal operation, with an intermittent short period where both are logically high when the piezoelectric crystal changes polarity. VAC1,2 are fed into

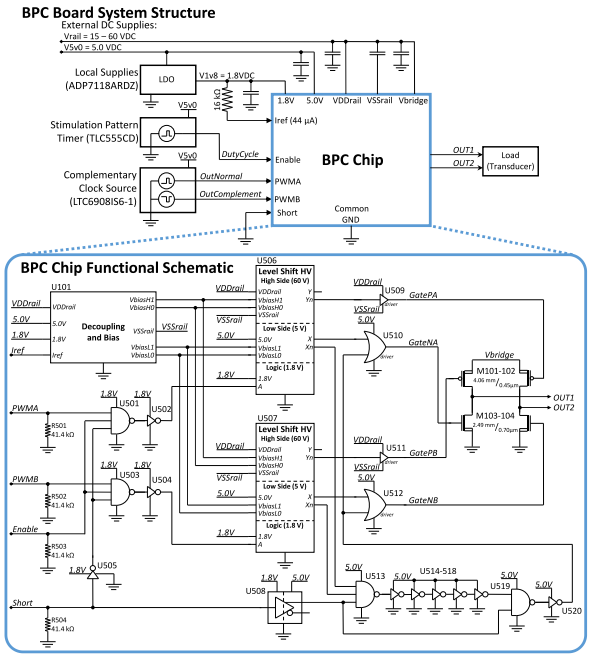

Fig. 5. System structure of the BPC test board, and the functional schematic of the BPC chip.

the logic gates of U2 and U3 in Fig. 2, respectively and they then control the mode of the adjacent OpAmp.

B. Base for Powering and Controlling

The counterpart to the Dust is the BPC, with its system structure and driver building blocks shown in Fig. 5. The BPC incorporates all required functionality into as few components as possible so it can be carried by mice. Using an H-bridge at the output of the BPC chip that employs Laterally Diffused Metal-Oxide-Semiconductor (LD-MOS), the BPC is capable of controlling and powering a piezoelectric load with high voltages of up to 60 V peak. The controlling input signals (PWM's, etc.) are all 1.8 V logic level and internal level-shifters bridges the gap between low-side and high-side LD-MOS transistors in the output driver stage (from 1.8 V to 5 V and then to 60 V). The Decoupling and Bias block, shown in Fig. 5, decouples the supplies and a series of bias voltages generated for the high voltage level-shifters.

III. Measurement Results

The Dust chip area is restricted to 300μm $\times$ 300μm, thereby making it directly size compatible with the piezoelectric crystal and the μLED. The Dust and BPC chip micrographs fabricated in standard 0.18μm and HV-BCD 0.18μm CMOS technologies respectively, are shown in Fig. 6. A miniaturized implantable Dust prototype is produced, with a PZT crystal attached onto a Ti/Au substrate, the Dust chip on top and wire bonded to the substrate and the crystal, and the μLED is attached on top of the chip (see Fig. 6).

For the BPC, there is an effective upper voltage limit depending on the load and stimulation pattern duty cycle. By observing the BPC board and chip under a thermal camera during experiments, the roughly upper thermal limit

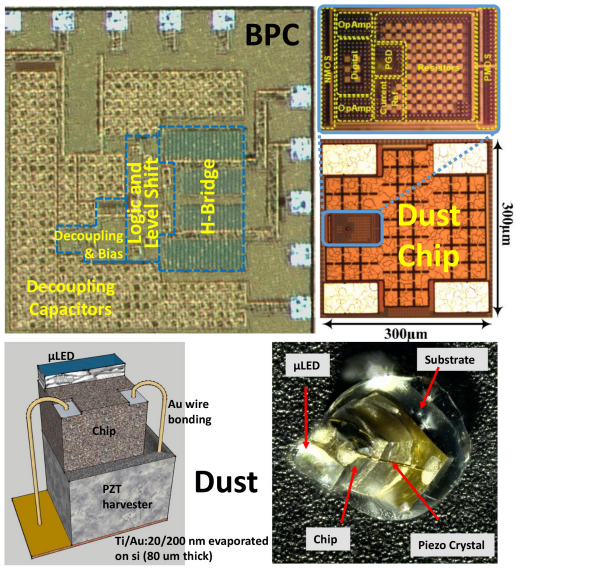

Fig. 6. Die micrograph of BPC and Dust cores, Dust integration strategy, and integrated Dust prototype.

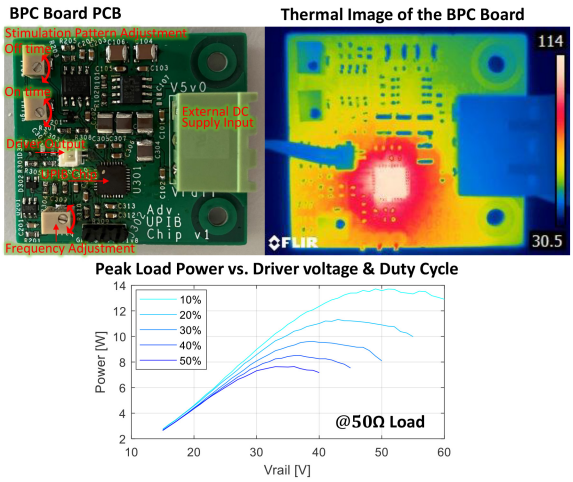

Fig. 7. BPC test board, a thermal image under maximum load, and peak load power vs. voltage and duty cycle.

was observed empirically to be around 100°C (see Fig. 7). However, that still allows for as much as 13.5W peak output power depending on the attached load, driver voltage, and overall PWM duty cycle (also see Fig. 7). Fig. 8 shows the BPC chip DC current consumption and high-side rail supply (40V limit). The internal power consumption of the BPC chip while driving its PWM inputs are measured while the frequency is swept from 0.5MHz to 5MHz in steps of 0.5MHz (Fig. 8).

The Dust chip DC characterization results are depicted in Fig. 9, where Config A is used for determining the LP current consumption, and Config B and C are for the two input states that force the respective active diode to enter the HP mode. The Dust chip stays in Offline mode until approximately 0.9V, then normal operation resumes in either LP or HP mode depending on the inputs. At 2.5V the chip consumes 3.0μA and 6.9μA

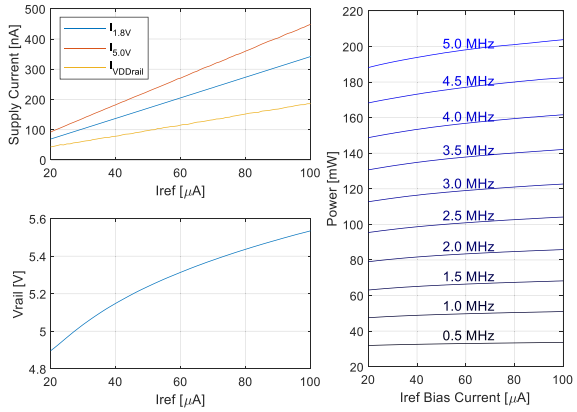

Fig. 8. Current draw of the *1.8V*, *5.0V*, *VDDrail* supplies, and *Vrail* voltage versus current reference *Iref*, and total chip biasing power consumption versus PWM driving frequency in the BPC chip. (*VDDrail* limited to 40 V by instruments.).

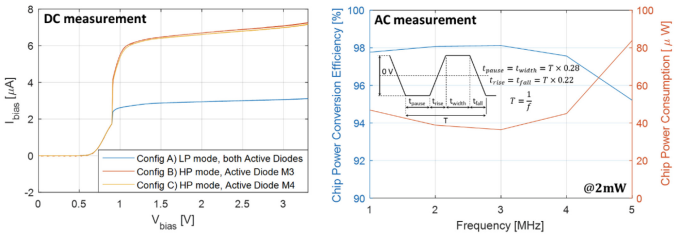

Fig. 9. DC characterization, and AC characterization of power consumption and conversion efficiency of the Dust chip.

in LP and HP mode, respectively, resulting in DC power consumption of 7.5μW and 17.3μW, respectively. In addition, Fig. 9 shows the AC characterization and how efficiently the chip operates when powered by high-frequency sources, corresponding to a sub-mm-sized piezoelectric crystal output. A μLED (480nm wavelength) is used as the loading of the chip, which results in the output voltage ending up around 2.5V. A signal generator is set to 6.0V_{pp}, and its frequency is swept from 1 – 5MHz in 1MHz steps. The input and output voltages and currents are recorded during the experiment for ten full periods at each frequency. Fig. 9 shows the resulting chip power conversion efficiencies and power consumption.

For measuring the Dust output power in a full system, a prototype Dust is produced (shown in Fig. 10) that consists of the same three base components, but with added buffer circuitry that allows for monitoring the power levels delivered to the μLED without interfering with the Dust system itself. A transducer prototype consisting of four (500μm)^3 PZT4 crystals arranged 2 × 2 and covered by ∼1 mm PDMS is used, powered by a BPC. Fig. 10 shows the Dust prototype used for full system measurements and its schematic, while Fig. 11 shows the water-tank setup used for ultrasonic experiments.

In the full system setup, the BPC drives the transducer, which in turn ultrasonically powers the Dust that drives a μLED. The output power of the Dust versus BPC voltage driving the Dust through 3mm of demineralized water is shown in Fig. 12. The rationale for using a 3mm distance is rooted in the practical limitations imposed by the small size of the mouse brain. Figure 12 also shows the start-up time measured

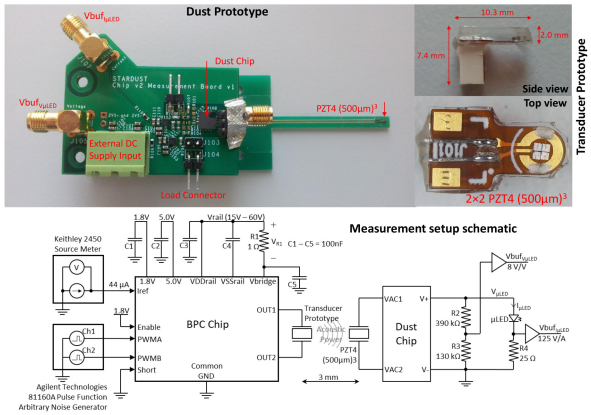

Fig. 10. Dust prototype with a (500 μm)^3 PZT4, 2 by 2 (500 μm)^3 PZT4 transducer, and full measurement setup schematic.

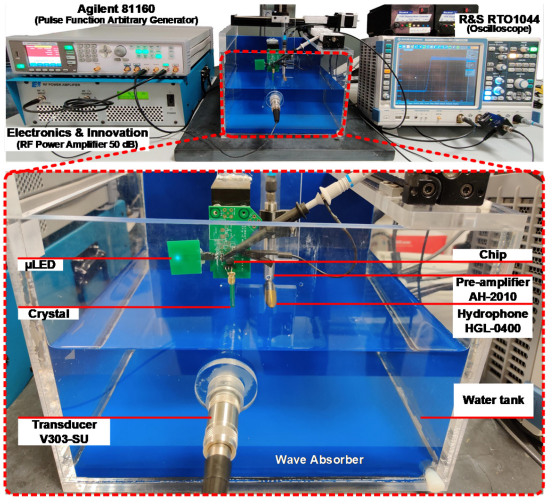

Fig. 11. Measurement setup for testing the entire system.

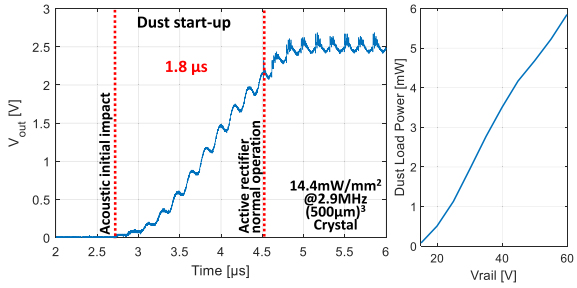

Fig. 12. Dust startup output voltage and Dust power versus BPC driver voltage through 3mm demineralized water.

at an acoustic intensity of 14.4mW/mm^2 @2.9MHz set by the crystal. It takes 1.8μs from the first impact of the acoustic waves until the active rectifier starts normal operation.

For the purpose of drug-delivery, a miniaturized Dust was assembled, including a (500μm)^3 PZT4, the Dust chip, and a μLED coated with a polymer (see Fig. 13). The prototype was subjected to bursts of acoustic energy powering the Dust and its μLED, which illuminates the polymer for the purpose of drug release.

TABLE I
SUMMARY OF SPECIFICATIONS AND COMPARISON

	This Work	ISSCC'19 [10]	TBioCAS'18 [7]	CICC 2018 [11]
Technology	0.18 μm	65 nm LP CMOS	0.18 μm HV BCD	65 nm LP CMOS
Dust chip area	0.09 mm^2	0.25 mm^2	3.58 mm^2	1 mm^2
Total implant volume	1.06 mm^2	0.8 mm^2	39 mm^2	6.5 mm^2
Powering method	Ultrasound	Ultrasound	Ultrasound	Ultrasound
Features	Optogenetic Drug Delivery	Reading Communication	Elec. Stim., Optogen., Communication	Elec. Stim., Communication
Dust input voltage range	3-6.6 V_{pp}	-	6-9 V_{pp}	6-10 V_{pp}
Dust output voltage	1.5-3.3 V	1.0 V	3 V & 15 V	2.5 V (nominal)
Dust output power	0-10 mW	-	-	3 mW
Dust capacitor	95 pF	130 pF	1.5 nF*	4 μF
Dust quiescent power	17.3 μW	28.8 μW	-	4 μW
Dust Start-up time	1.8 μs	11 μs	-	-
Dust max. power conv. effic.	98.1 % **@2m W	-	71.4%	82% @120 μW***

* Off-chip capacitor **@3MHz ***estimated

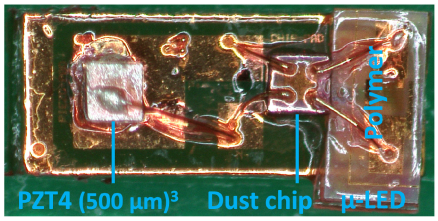

Fig. 13. Drug delivery Dust prototype with μLED coated in a polymer.

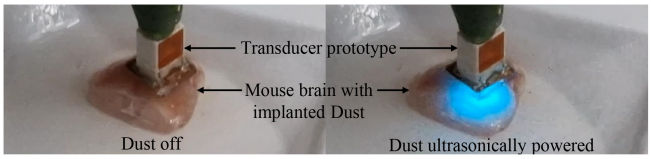

Fig. 14. *Ex vivo* experiment showing a transducer ultrasonically powering a Dust implanted in a mouse brain.

An ex vivo experiment was also conducted using the Dust, which was implanted inside a mouse brain, and then ultrasonically powered by a transducer prototype, as seen in Fig. 14. When the transducer is driven by the BPC (same as seen in Fig. 7) a part of the brain is illuminated by blue light emitted by the Dust μLED. Table I summarizes the performance and shows the comparison with the state-of-the-art.

IV. CONCLUSION

This brief describes a novel micro-system for ultrasonically-powered deep-tissue optogenetic, consisting of a base for powering and controlling and an implantable Dust with a piezoelectric crystal, a chip, and an μLED. The system has great potential for use in freely moving animal studies.

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