A 20-bit ±40-mV Range Read-Out IC With 50-nV Offset and 0.04% Gain Error for Bridge Transducers

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A 20bit ±40mV Range Read-Out IC with 50nV Offset and 0.04% Gain Error for Bridge Transducers

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***Abstract*—**This paper presents a 20-bit read-out IC with ±40mV full-scale that is intended for use with bridge transducers. It consists of a current-feedback instrumentation amplifier (CFIA) followed by a switched-capacitor incremental ΔΣ ADC. The CFIA's offset and 1/*f* noise are mitigated by chopping, while its gain accuracy and gain drift are improved by applying dynamic element matching to its input and feedback transconductors. Their mismatch is reduced by a digitally-assisted correction loop, which further reduces the CFIA's gain drift. Finally, bulk biasing and impedance balancing techniques are used to reduce the common-mode dependency of these transconductors, which would otherwise limit the achievable gain accuracy. The combination of these techniques enables the read-out IC to achieve 140dB CMRR, a worst-case gain error of 0.04% over a 0-2.5V common-mode range, a maximum gain drift of 0.7ppm/°C and an INL of 5ppm. After applying nested-chopping, the read-out IC achieves 50nV offset, 6nV/ºC offset drift, a thermal noise-floor of 16.2nV/√Hz and a 0.1mHz 1/*f* noise corner. Implemented in a 0.7µm CMOS technology, the prototype read-out IC consumes 270µA from a 5V supply.

Index Terms—Current-feedback instrumentation amplifier, incremental delta-sigma ADC, readout-IC, bridge transducer, gain accuracy, gain drift, linearity, dynamic element matching, chopping, 1/*f* noise, offset.

I. Introduction

Precision bridge transducers such as strain gauges and thermistors typically output low frequency signals with *mV*-levels. To process such signals, read-out integrated-circuits (ICs) with low noise, low offset and high accuracy are required. Since the sensor and read-out IC are usually calibrated as a single system, the read-out IC should also exhibit low offset and gain drift (a few ppm/°C) so as to maintain system accuracy over temperature. As shown in Fig. 1(a), a typical read-out IC consists of a precision instrumentation amplifier (IA) followed by a high-resolution analog-to-digital converter (ADC) [1], [2]. The IA provides high input impedance, and relaxes the offset and noise requirements of the ADC.

The IAs used in previous precision read-out ICs have generally employed either switched-capacitor (SC) [3], [4] or two-opamp topologies [5]. Although these topologies achieve high linearity and gain accuracy, they are inherently power inefficient: due to noise folding on the one hand, or the need for two high gain amplifiers on the other. Furthermore, in the case of a SC IA, an additional power-hungry input buffer is usually necessary to provide the high input impedance required for bridge read-out [3]. A read-out IC based on a SC IA consumed 80mW to achieve 18-bit resolution with 10mV full-scale [3], while a read-out IC based on a two-opamp IA dissipated 40mW to achieve 19-bit resolution with 28mV full-scale [5].

In contrast, indirect current-feedback IAs (CFIAs) can be more power efficient, since they avoid noise folding and only require a single output stage [6]-[9]. Although capacitively-coupled IAs (CCIAs) are even more power efficient than CFIAs [10] and have been applied to a read-out IC that achieves a low noise level of 6.7nV/√Hz [11], their input impedances are somewhat limited by the switching impedance of input capacitors. To achieve high input impedance for bridge read-out, a precision CFIA has been reported in [6] that achieves μV-level offset, a 15nV/√Hz noise density and a 1mHz 1/*f* noise corner, while only dissipating 1.2mW. However, it suffers from limited linearity and gain accuracy (0.5%). The main objective of this work is to explore ways in which this CFIA can be combined with an ADC without compromising the amplifier's offset and noise performance and simultaneously improving its linearity, gain accuracy and gain drift.

As shown in Fig. 1(b), the closed-loop gain of a CFIA is given by $(G_{m3}/G_{m4})\cdot((R_1+2R_2)/R_1)$. When precision gain-setting resistors (R_1 and R_2) are used, the CFIA's gain accuracy is mainly determined by the mismatch between the input and feedback transconductors (G_{m3} and G_{m4}). The gain accuracy can be improved by resistor-degeneration [13], [14], since resistors can be made to match better than transistors—either by careful layout or by trimming. However, for a given transconductance, this approach will result in significantly increased power consumption. Without sacrificing power efficiency, dynamic element

matching (DEM) can be applied to G_{m3} and G_{m4} to average out their G_m mismatch, thus permitting the use of simple and power-efficient G_m stages [12], [15]-[17]. However, the transconductance of a differential pair will exhibit a certain dependency on the CM input voltage. Thus, any difference in the input and output CM voltages of a CFIA will give rise to a CM-dependent mismatch that cannot be removed by DEM and which will limit the ultimate gain accuracy (0.12%) [12].

This paper presents a 20-bit read-out IC with improved gain accuracy and offset. It consists of a CFIA and a 21-bit switched-capacitor (SC) incremental ΔΣ ADC. DEM is applied to improve the CFIA's gain accuracy and gain drift, while the intrinsic G_m mismatch is reduced by a digitally-assisted gain error correction scheme, which further reduces the CFIA's gain drift. Finally, bulk biasing and impedance balancing techniques are used to reduce the CM-dependent error of the G_m stages [17]. In [12], [17], a multi-stage chopping technique has been applied to achieve mHz 1/f noise corner and μV-level offset. In this work, however, a simpler nested-chopping scheme is employed in which input stage chopping (in the CFIA) is combined with system-level chopping (of the entire read-out IC).

This paper is organized as follows. Section II describes the techniques used to improve the gain accuracy of the read-out IC. Section III discusses the offset and 1/f noise reduction techniques used in the read-out IC. Section IV summarizes all the error correction techniques. Section V and VI present the implementation of the CFIA and the ΔΣ ADC, respectively. The measurement results are presented in Section VII and the paper ends with conclusions.

II. Gain Accuracy Improvement Techniques

Fig. 2 shows the block diagram of the read-out IC. It consists of a CFIA and an incremental ΔΣ ADC. Since the ADC's gain is defined by switched-capacitor techniques, it is very well defined. However, the CFIA's gain accuracy is limited by the mismatch of the input and feedback transconductors (assuming the use of precision gain-setting resistors), and this, in turn, limits the gain accuracy of the entire read-out IC. This section explores the use of DEM to average out this mismatch. Furthermore, system-level collaboration between the CFIA and the ADC is used to further reduce the CFIA's gain drift.

A. Dynamic Element Matching

To average out the mismatch between the input and feedback transconductors, DEM is applied by periodically swapping the two transconductors shown in Fig. 3(a). This process causes their mismatch Δ to periodically appear in the input and feedback paths. The resulting gain error after applying DEM is then given by:

$$|Gain\ Error| = |1 - \frac{\frac{1+\Delta}{1} + \frac{1}{1+\Delta}}{2}| \approx \frac{\Delta^2}{2} \quad (for\ \Delta << 1) \tag{1}$$

The application of DEM reduces the mismatch from Δ to $\Delta^2/2$, e.g. for a typical G_m mismatch of 2%, the gain error can be reduced to 0.02%.

However, a CFIA typically operates with different input and feedback CM voltages. Due to their finite CMRR, the input and feedback transconductors will then exhibit a CM-dependent mismatch Δ_{cm}. Unlike the static mismatch Δ used in eq. (1), this CM-dependent mismatch Δ_{cm}, is always present and cannot be suppressed by DEM. The resulting gain error is given by:

$$|Gain\ Error| = |1 - \frac{\frac{1+\Delta+\Delta_{cm}}{1} + \frac{1+\Delta_{cm}}{1+\Delta}}{2}| \approx \frac{\Delta^2}{2} + \frac{\Delta \cdot \Delta_{cm}}{2} + \Delta_{cm} \quad (for\ \Delta << 1) \tag{2}$$

This mismatch, in the order of 0.12% [12], is the dominant source of gain inaccuracy. In Section V, a circuit-level technique will be proposed to address this problem. This issue will thus be neglected in the following analysis.

Another issue with the different CM levels of the CFIA's input and output is that swapping the inputs of G_{m3} and G_{m4} results in large voltage spikes at the CFIA's output. To avoid sampling these spikes, the DEM multiplexer's state is only altered during the reset period at the start of every AD conversion (Fig. 3(a)).

B. Digitally-Assisted Gain Error Correction Scheme

Although the use of DEM reduces the mismatch from Δ to $\Delta^2/2$, it will still vary over temperature, causing a gain drift of around 5ppm/ºC [12]. To reduce gain drift further, the intrinsic mismatch Δ should be minimized [12]. Therefore, a gain error correction scheme is used and is implemented in a digitally-assisted manner to minimize the complexity and area of the analog circuitry required.

Fig. 3(a) shows the gain error correction (GEC) scheme consisting of a $\Delta\Sigma$ ADC, a digital back-end and a 6-bit DAC. The GEC path trims the G_m mismatch by tuning the tail currents of G_{m3} and G_{m4} via transconductor G_{m6}. To achieve a targeted gain error of 0.02%, considering an initial gain error of the CFIA to be 1%, 6-bit resolution is required for the DAC. The DAC is implemented as an over-sampled $\Delta\Sigma$ DAC consisting of an interpolation filter, a digital $\Delta\Sigma$ modulator and an RC low-pass filter (LPF). For flexibility, the interpolation filter and the digital $\Delta\Sigma$ modulator were implemented in an external FPGA.

The GEC scheme uses linear interpolation to determine the appropriate calibration voltage during the start-up and Fig. 3(b) shows its concept. By applying a fixed DC signal to the CFIA, the appropriate value of V_{CAL} can be determined within two DEM periods. In the first DEM period, the maximum calibration voltage $V_{CAL,MAX}$ within the DAC's output range is applied to the inputs of G_{m6}. The decimated results of two conversions within one DEM period are given by

$$V_{conv1} = V_{out,ideal}\frac{1+\Delta+\Delta_{CAL,MAX}}{1} = V_{out,ideal}(1+\Delta+\Delta_{CAL,MAX}) \tag{3}$$

$$V_{conv2} = V_{out,ideal}\frac{1}{1+\Delta+\Delta_{CAL,MAX}} \approx V_{out,ideal}(1-\Delta-\Delta_{CAL,MAX}) \tag{4}$$

where Δ is the initial mismatch of G_{m3} and G_{m4}, $\Delta_{CAL,MAX}$ is the extra mismatch induced by $V_{CAL,MAX}$. In the digital backend, the output referred mismatch error due to $(\Delta+\Delta_{CAL,MAX})$ can then be determined from the difference of the two conversion results given by eq. (3) and (4):

$$V_{out,error,A} = 2V_{out,ideal}(\Delta+\Delta_{CAL,MAX}), \tag{5}$$

which is denoted by point *A* in Fig. 3(b). In the second DEM period, the minimum signal $-V_{cal,max}$ within the DAC's output range is applied to G_{m6}. Similarly, the output-referred mismatch error due to $(\Delta-\Delta_{CAL,MAX})$ can also be determined:

$$V_{out,error,B} = 2V_{out,ideal}(\Delta-\Delta_{CAL,MAX}), \tag{6}$$

which is denoted by point *B* in Fig. 3(b). Under the condition that the DAC's output range is a linear function of the induced mismatch and that it is larger than the worst-case static mismatch of G_{m3} and G_{m4}, the optimal calibration voltage $V_{CAL,SET}$ that minimizes the mismatch error (point *C*) can then be found by linear interpolation. To ensure the necessary linearity, a 6-bit $\Delta\Sigma$ DAC was used. Since the calibration voltage is found within two DEM periods, one decimated output is also chosen to be the average result of two DEM periods, i.e. one decimated output requires four conversions. The averaging function is implemented in the digital-backend.

Since G_{m3} and G_{m4} are biased in weak inversion for maximum power efficiency, their mismatch can be tuned by adjusting their tail currents via G_{m6}. To attenuate the noise contribution of the GEC path, the G_{m6} is implemented with resistor-degeneration stage (G_{m3}/G_{m6} = 480), and thus the voltage across the input of G_{m6} is indeed a linear function of the induced mismatch. Since the calibration voltage $V_{CAL,SET}$ is determined by the *ratio* of gain errors at points *A* and *B*, the value of the fixed DC input during calibration does not need to be known. After finding the calibration voltage $V_{CAL,SET}$, the digital word applied to the DAC is frozen and the read-out IC starts normal operation.

III. Offset and Flicker Noise Reduction Techniques

The CFIA is designed to have a gain of 100, thus relaxing the requirement on the ΔΣ ADC's noise and offset. Since most sensor applications operate near DC, a 5Hz signal bandwidth is targeted. The CFIA's 15nV/√Hz noise density then corresponds to a 20-bit resolution over a ±40mV full-scale range. To maintain this, the ΔΣ ADC is designed to have 21-bit resolution with the same bandwidth. At low frequencies, offset and 1/*f* noise are the dominant error sources. To mitigate these errors, nested-chopping techniques can be applied in at least two various ways. Two of these will be described in this Section.

A. Previous Approach (Multi-stage chopping and system-level chopping)

Fig. 4(a) shows a simplified block diagram of the implemented 3-stage CFIA. In previous work, the input and intermediate stages of the CFIA were both chopped, so as to suppress their own 1/*f* noise while providing enough gain to suppress the input-referred 1/*f* noise of the (un-chopped) output stage [6]. However, the resulting up-modulated offset and 1/*f* noise then gave rise to a few hundred mV of chopper ripple at the CFIA's output.

In [12], the input stages were chopped at 30 kHz, which was chosen to be slightly above their 1/*f* corner frequency and equal to the sampling frequency of ΔΣ ADC. The resulting ripple was removed by a continuous-time ripple-reduction loop (RRL) (Fig. 5), which synchronously demodulated the CFIA's output chopper ripple and used the information to null the offset, and hence the ripple [6]. The intermediate stage was chopped in a bitstream-controlled (BSC) manner [18], so as to eliminate the correlation between the chopper ripple and the quantization noise. The entire read-out IC was then chopped once every two conversions and the low-frequency ripple was averaged in the digital decimation filter, resulting in a worst-case offset of 200nV. However, this is still higher than expected, since the residual offset after system-level chopping should theoretically be limited by the system's resolution (50nV).

B. Proposed Approach (Input-stage chopping combined with system-level chopping)

In this work, a nested–chopping scheme that simply combines input stage chopping (in the CFIA) with system-level chopping (of the whole read-out IC) is shown to achieve much lower (tens of nV) offset and a sub-mHz 1/*f* noise corner. The key observation is that system-level chopping efficiently reduces the residual 1/*f* noise after input-stage-chopping. As a result, the intermediate stage no longer needs to be chopped, thus avoiding a potential source of residual offset and ripple. As in [12], a RRL is applied to reduce the ripple associated with the chopped input and feedback transconductors.

Applying DEM could give rise to some residual offset due to the difference between the input and feedback CM voltages. To average out such errors, the frequency of the system-level chopper is chosen to be the half of the DEM frequency, and thus one digital output is the average result of four ADC conversions. Instead of using a "0011" pattern for the system-level chopper in four conversions [12], a "0110" pattern [19] is chosen in this work as shown in Fig. 6. Assuming that X is the DC input signal, V_n is the read-out IC's low-frequency error due to offset, drift, and 1/f noise, and Y is the digital output of one system-level chopping period. When applying system-level chopping with "0011" pattern, the output Y can be expressed as

$$Y=\frac{(X+V_n)+(X+V_n)\cdot z^{-1}+(X-V_n)\cdot z^{-2}+(X-V_n)\cdot z^{-3}}{4}=X+\frac{V_n}{4}(1-z^{-1})(1+z^{-1})^2 \quad (7)$$

However, after applying "0110" pattern, Y can be expressed as

$$Y=\frac{(X+V_n)+(X-V_n)\cdot z^{-1}+(X-V_n)\cdot z^{-2}+(X+V_n)\cdot z^{-3}}{4}=X+\frac{V_n}{4}(1-z^{-1})^2(1+z^{-1}) \quad (8)$$

Fig. 7 shows the transfer functions of these two chopping patterns on the 1ow-frequency errors. It can be seen that the "0110" pattern achieves much better rejection of low frequency errors because of the second-order noise shaping, while "0011" pattern only exhibits a first-order noise shaping, as shown in Fig. 7. More intuitively, it can be seen that unlike the "0011" pattern, the "0110" pattern can exactly compensate for any offset drift that is a linear function of time.

In addition to reducing offset, system-level-chopping also effectively suppresses the CFIA's 1/f noise. Input-stage chopping reduces the 1/f noise corner from 10 kHz to about 0.3 Hz. Therefore, as long as the system-level chopping frequency is higher than this, it will effectively suppress the residual 1/f noise.

Simulations with periodic steady-state (PSS) and periodic noise analysis (PNOISE) tools of Spectre RF [20] were made to confirm the validity of above analysis. Fig. 8 shows the simulated input-referred noise spectrum of the read-out IC with various 1/f noise suppression techniques. The combination of the input-stage chopping and system-level chopping achieves the lowest 1/f noise corner frequency: 0.1 mHz.

IV. System Level Overview

Fig. 9 shows the proposed read-out IC and its associated timing diagram. Table I summaries the errors and the associated error correction techniques applied in this work. The 1/f noise and offset of the read-out IC is suppressed by a nested-chopping scheme that combines input stage chopping (in the CFIA) with system-level chopping (of the whole read-out IC). The chopper ripple of the input stage is suppressed by a ripple reduction loop, while further suppression is obtained by ensuring that the succeeding ADC only samples at

the zero-crossings of any residual ripple. The gain error associated with the mismatch of the CFIA's input stages is averaged out by the use of DEM. A digitally-assisted gain error correction scheme trims the G_m mismatch, thus improving gain error and gain drift further.

V. CFIA Realization

Fig. 5 shows a simplified top-level circuit diagram of the implemented CFIA. It consists of three gain stages: input and feedback stages G_{m3} and G_{m4}, the intermediate stage G_{m2} and the class-AB output stage G_{m1}. In contrast to [6], the input and feedback Gm stages have been modified to improve their CM immunity.

Input and Feedback G_m Stages

As indicated by eq. (2), the CM dependent transconductance of G_{m3} and G_{m4} leads to a CM dependant gain error, and hence limits the gain accuracy even with DEM applied. To improve gain accuracy, the transconductances of G_{m3} and G_{m4} should be constant over the input CM range. Fig. 10 shows the input and feedback G_m stages used in [6], [12]. Their CM dependency is mitigated by cascading the input transistors with low-threshold devices M_3-M_4. Transistors M_1-M_4 operate in weak inversion for the best power efficiency. The resulting drain-source voltage V_{DS} of M_1 equals the threshold difference of M_1 and M_3 is only about 0.18V in this process. This small V_{DS} limits the output impedance of the input G_m stages.

The threshold difference between M_1 and M_3 can be increased by using a bulk biasing technique. This can be done in two different manners: reducing the threshold of M_3 or increasing the threshold of M_1. The threshold of M_3 can be reduced by adding a resistor R_1 between the source of M_1 and the bulk of M_3, as shown in Fig. 11(a). The voltage drop across R_1 will reduce the threshold of M_3. However, this approach requires an extra bias current source I_1, leading to a power increase. To avoid this, the threshold of M_1 can be increased by adding a resistor R_3 between source and bulk of M_1 and M_2 as shown in Fig. 11(b). Due to the body effect, the voltage drop across R_3 increases the threshold of M_1 from about 0.9V to 1V. As a result, the output impedance of the input G_m stages is boosted from 200MΩ to 500MΩ.

In the circuit of Fig. 10, two opposing effects influence the G_m of the input (or feedback) stage. As shown in Fig. 12, when the CM voltage increases, the V_{DS} of M_1 also increases due to channel length modulation (Fig. 12(a)), leading to an increased G_m (Fig. 12(b)). On the other hand, the increased CM voltage reduces the head-room of the tail current source M_5 (Fig. 12(a)), hence reducing the tail current and thus the G_m of the input differential pair (Fig. 12(b)). These two opposing effects might compensate each other and provide an improved CMRR. However, the effect of channel-length modulation on M_1 is much larger than the effect

of the reduced bias-current provided by M_5. Fig. 13 shows the simulated G_m variations of the input stage for an input CM range of -0.1V to 2.8V. If the tail current source of the input differential pair is ideal, the G_m of the differential pair varies 0.6% over the CM range. If the cascode current source shown in Fig. 10 is used, the G_m variations affected by the differential pair and the tail current source partially compensate, because they are configured differently and the CM sensitivity of these two circuits differ. This results in a reduced G_m variation of 0.07%. To make the CM sensitivity between the input differential pair and the tail current source exactly compensate each, the same cascode configuration with the same current density are applied in both as shown in Fig. 14. This configuration ensures that the two opposing effects have nominally the same absolute CM sensitivity and so well compensated with each other. As shown in Fig. 13, the combination of bulk biasing and impedance balancing techniques reduces the G_m variation from 0.07% to 0.02% (typical corner) over the input CM range. The maximum G_m variation over all process corners is reduced from 0.089% (with Fig. 10) to 0.033% (with Fig. 14).

VI. ΔΣ ADC Realization

The output of the CFIA is digitized by a second-order incremental ΔΣ ADC, which consists of a ΔΣ modulator and a decimation filter. Here, the target resolution of the ΔΣ ADC is 21-bit within a 5Hz signal bandwidth in order to maintain the SNR of the CFIA. The reference voltage of the ΔΣ ADC is set to 5V at which it achieves 4V input full scale, which corresponds to a noise density of 600nV/√Hz in the signal band. Since the CFIA has a nominal gain of 100, the input referred noise density of the ΔΣ ADC is 6nV/√Hz, which is sufficiently low when compared to the CFIA's noise density of 15nV/√Hz.

Fig. 15(a) shows the block diagram of the second-order ΔΣ modulator, which employs feed-forward topology to relax the linearity and slewing requirements of the integrators [21]. To sufficiently filter out the quantization noise, a sinc^3 filter is used for the decimation filter. The second order ΔΣ ADC can obtain 21-bit resolution in 5200 clock cycles with four sub-conversions of 1300 cycles. To obtain a conversion time less than 0.2s, the required sampling frequency is only 30 kHz, which equals the chopping frequency of the CFIA. The system-level chopping frequency is then determined as 30 kHz / 5200 ≈ 6 Hz, which is enough to suppress the residual 1/*f* noise of the CFIA after input-stage chopping.

Fig. 15(b) shows the schematic diagram of the second order ΔΣ modulator. For maximum linearity, it employs a single-bit DAC. Furthermore, the *same* sampling capacitor C_{s1} is used to sample both the input

and feedback signals. As a result, the modulator's gain accuracy is not limited by capacitor mismatch. To meet the thermal noise requirement C_{s1} = 3pF. As shown in Fig. 2, the ADC's references, V_{ref+} and V_{ref-}, are connected to the reference of the bridge transducers in a ratio-metric manner, which means that the accuracy of the reference does not affect the system's gain accuracy. The first integrator essentially determines the accuracy of the modulator. The first integrator is therefore designed for complete settling. The first amplifier is implemented with a two-stage Miller-compensated OTA consisting of a gain-boosted telescopic first stage and a second stage with a 3V output swing, to minimize the effect of the nonlinear DC gain [22]. The gain variation is optimized to be less than 10dB over a 2.5V output swing at a 150dB nominal DC-gain. The first OTA has a UGB of 250 kHz with 8pF load capacitor and draws only 38μA. Due to the CFIA's gain of 100, the required offset level of the ADC is at the μV-level. To achieve this, the first integrator is auto-zeroed. After applying auto-zeroing, the residual offset is then mainly due to the charge injection mismatch of switches. This will then be removed by system-level chopping. Since the errors in the second integrator are attenuated by the loop gain of the first integrator, no offset cancellation or gain boosting techniques are necessary in the second stage. The second OTA has a 100-dB DC gain and a UGB of 60 kHz with 6pF load capacitor while consuming only 8μA. A passive adder is used for the feed-forward adder at the quantizer input. The feed-forward coefficients are determined by the ratio among feed-forward capacitors. Clocks with delayed falling edges (e.g. P_{1d}) are used to prevent signal-dependent charge injection. The quantizer makes decision at the end of the sampling frequency when the passive adder is fully settled.

VII. Measurement Results

The read-out IC is fabricated in a standard 0.7μm CMOS process. Fig. 16 shows chip microphotograph with an active area of 6mm^2. All the results are verified with 10 samples from one batch in a DIL package.

A. DC Measurements

The noise spectrum of the ROIC is shown in Fig. 17(a). In order to demonstrate the noise-shaping spectrum of the read-out IC, the system-level chopping and DEM have been turned off. The noise spectrum of the ROIC is measured with 2^{24} samples (Fig. 17(a)). The ADC's sampling frequency f_S and input stage chopping frequency f_{ch1} were lowered to 10 kHz to achieve more frequency resolution (10kHz / 2^{24} = 0.596mHz). It can be seen that the noise level is flat down to 1mHz with a noise density of 16.2nV/√Hz, corresponding to a resolution of 20-bit with respect to a full-scale range of ±40mV in 5Hz bandwidth. To eliminate the low-frequency lobe, the read-out IC's offset is removed before the FFT computation. As seen from the zero-input spectrum in Fig. 17(a), the noise level of the read-out IC is mainly limited by the thermal noise. Fig. 17(b) shows the output noise spectrum of the read-out IC with RRL turned "on" and

"off". The necessity of the RRL is clearly seen. The use of a RRL eliminates the sampling uncertainty. The result is a flat noise spectrum down to 1mHz.

To test the effectiveness of the proposed nested-chopping on suppressing the 1/*f* noise, the chopper in the intermediate stage is turned off, while input and system-level chopping are both on. Fig. 18 shows the measured noise spectrum with decimated output. The 1/*f* noise corner is suppressed below 0.1mHz.

Fig. 19 shows the measured gain error histogram with the same input and feedback CM voltage (2.5V). Applying DEM to the CFIA reduces the gain error from 6000 ppm to 35ppm. Applying the GEC path further reduces the gain error to 16.5ppm. However, the worst-case gain error drops to 0.12% when the input and output stages are at different CM voltages [12]. Fig. 20 shows the measured CMRR and the worst-case gain error. By using the proposed input G_m stages in the CFIA, the typical CMRR of the read-out IC is improved from 130dB to 140dB. It also achieves an improved worst-case gain error of 0.04% over a CM range of 0–2.5V, which is a 3× improvement compared to [12].

Fig. 21 shows the measured gain drift and integral nonlinearity (INL) of the read-out IC. The use of DEM improves the maximum gain drift from 6.1ppm/°C to 4.3ppm/°C and further applying GEC improves the gain drift to 1.2ppm/°C (with a typical value of 0.7ppm/°C). The CFIA determines the INL of the read-out IC, since the measured INL of the ADC is only around 1ppm. The use of DEM improves the INL from 35ppm to 5ppm (Fig. 21(b)). After turning on the GEC, the INL improvement is minor.

Fig. 22 shows the measured offset histograms with different chopping strategies. With only multi-stage chopping, the worst-case offset is 4.6μV. Turning on the system-level chopping reduces offset to less than 200nV [12]. As discussed in Section III.B, the combination of input stage chopping and system-level chopping results in 48nV offset, which is mainly limited by the resolution of the read-out IC. The offset drift is obtained by measuring the offset variation over a small temperature range (27°C to 50°C). The worst-case offset drift is also reduced from 7.6nV/°C [12] to 6nV/°C.

B. Performance Summary

The performance of the read-out IC is summarized in Table II and compared with that of other state-of-the-art [4], [5], [12], [23], [24]. The read-out IC achieves a typical gain drift of 0.7ppm/ºC and a 5ppm INL at a gain of 100. Furthermore, the simple nested-chopping scheme enables to achieve 0.1-mHz 1/*f* noise corner, a maximum offset of 48nV and an offset drift of 6nV/ºC. Compared to other designs, this work achieves the best gain error of 0.04%, 20× better offset and 1.5× better gain drift than [23]. Moreover, this work only consumes a 270μA supply current from a 5V supply.

VIII. Conclusions

To interface bridge transducers, a power-efficient low-drift 20-bit read-out IC has been presented that consists of a chopper CFIA and a SC incremental ΔΣ ADC. To improve gain accuracy, DEM is applied in CFIA to average out the mismatch between the input and feedback transconductors. To reduce gain error and gain drift further, a digitally-assisted gain error correction scheme is applied to compensate the mismatch. Since the CM dependency of the input and feedback transconductors limits the final gain accuracy, bulk biasing and impedance balancing techniques are applied to improve CM immunity. Finally, a nested-chopping scheme that combines input stage chopping (in the CFIA) and system-level chopping (of the entire read-out IC) is employed to achieve sub-mHz 1/*f* noise corner and nV-level offset. Measurement results show that the offset and drift performance of the proposed read-out IC exceeds the state-of-the-art. These qualities make the proposed read-out IC very suitable for demanding bridge transducer applications, which require low thermal and 1/*f* noise, high accuracy, low drift, and simultaneously low power consumption.

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Table I
Errors and the Associated Correction Techniques

Error	**Error Correction Techniques**
1/*f* noise and offset	Input stage chopping + System-level chopping
Chopper ripple from the input stage	Ripple reduction loop + Zero-crossing sampling
Gain error and gain drift	Dynamic element matching + Digitally-assisted gain error correction

Table II
Performance Summary and Comparison with the State-of-the-art

	This work	ISSCC11 [12]	ISSCC00 [5]	AD7193 [23]	CS5530 [4]	ADS1282 [24]
Year	2011	2011	2000	2011	2009	2007
Supply current	270µA	270µA	8.2mA*	4.3mA	7mA	4.5mA
Supply voltage	5V	5V	5V	5V	5V	5V
Die area	6mm^2	6mm^2	--	--	--	--
1/*f* noise corner	< 0.1mHz	< 1mHz	10mHz	-	25mHz	--
Input range	± 40mV	± 40mV	± 28mV	± 39mV	± 78mV	± 263mV
CMRR	140dB ††	130dB††	--	110dB††	120dB††	110dB††
Input referred noise density	16.2nV/√Hz	16.2nV /√Hz	6.2nV/√Hz	5nV/√Hz	12nV/√Hz	5nV/√Hz
Gain drift	0.7ppm/°C††	0.7ppm/°C††	15ppm/°C††	1ppm/°C††	2ppm/°C††	9ppm/°C††
Gain error CM: 0 -2.5V	0.037%†	0.12%†	--	0.39% ††	1%††	1%††
Offset drift	6nV/°C†	7.6nV/°C†	70nV/°C†	5nV/°C ††	10nV/°C††	20nV/°C††
Offset	48nV†	200nV†	--	1 µV†	9.5 µV†	200 µV†
Nonlinearity	5 ppm††	5 ppm††	--	--	30 ppm††	4ppm††
Conversion time	0.17s	0.17s	0.0083s	0.2s	0.13s	0.004s

†: worst case ††: typical case * Total supply current (analog + digital).