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Zhang, Jingping; Luo, Houcai; Wu, Huan; Wang, Zeping; Zheng, Bofeng; Zhang, Guoqi; Chen, Xianping

DOI
10.1088/1402-4896/ad049b

Publication date
2023

Document Version
Final published version

Published in
Physica Scripta

PAPER

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To cite this article: Jingping Zhang *et al* 2023 *Phys. Scr.* **98** 125955

Physica Scripta

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RECEIVED
20 April 2023

REVISED
16 August 2023

ACCEPTED FOR PUBLICATION
18 October 2023

PUBLISHED
21 November 2023

Jingping Zhang[1], **Houcai Luo**[1], **Huan Wu**[1], **Zeping Wang**[1], **Bofeng Zheng**[1], **Guoqi Zhang**[2] and **Xianping Chen**[1,3]

[1] Key Laboratory of Optoelectronic Technology & Systems, Chongqing University, Chongqing, People's Republic of China
[2] Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology, Delft 2628 CD, The Netherlands
[3] Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing, People's Republic of China

E-mail: xianpingchen@cqu.edu.cn

Keywords: 4H-SiC MOSFET, SG, Cgd, Qgd, HF-FOM, switching loss

Abstract

A novel 4H-SiC Multiple Stepped SGT MOSFET (MSGT-MOSFET) is presented and investigated utilizing TCAD simulations in this paper. We have quantitatively studied the characteristics of the device through simulation modeling and physical model calculations, and comparatively analyzed the performance and application prospects of this novel device. The gate-to-drain capacitance (C_{gd}) and gate-to-drain charge (Q_{gd}) of the MSGT-MOSFET are significantly reduced in comparison with the double trench MOSFET (DT-MOSFET) and the conventional SGT MOSFET (CSGT-MOSFET), due to the reduction of the overlapping area of the split gate (SG) structure and drift region. Therefore, the obtained high frequency figure of merit (HF-FOM) defined as [$R_{on} \times C_{gd}$] reduced by 23.9% compared with DT-MOSFET and CSGT-MOSFET. And the HF-FOM [$R_{on} \times Q_{gd}$] for the MSGT-MOSFET significantly decreased by 71% and 50%, respectively, compared to that of the DT-MOSFET and CSGT-MOSFET. Furthermore, the switching loss is also simulated and calculated. And the total switching loss of the proposed MSGT-MOSFET realizes 42.9% and 21.7% reduction in comparison with the DT-MOSFET and CSGT-MOSFET. The overall enhanced performances suggest that the MSGT-MOSFET is an excellent choice for high frequency power electronic applications.

1. Introduction

4H-SiC MOSFETs are an attractive power semiconductor device in electronic systems for its high power rating, fast switching speed, and low drive power consumption [1–5]. Compared to SiC planar MOSFETs, SiC trench MOSFETs are more popular in the industry for their better tradeoff between on-resistance and breakdown voltage [6–9]. The most advanced 4H-SiC trench MOSFETs in the industry today are Infineon's asymmetric trench MOSFETs and Rohm's double trench MOSFETs [10–12]. Double trench MOSFETs (DT-MOSFET) are more favored because of their greater design flexibility and lack of process limitations for high-energy ion implantation [13–16]. Therefore, 4H-SiC DT-MOSFETs are one of the best power switching devices due to their extremely low on-resistance (Ron), high breakdown voltage (BV) and fast switching speed, etc [17, 18].

In order to reduce the power dissipation in high frequency and high power applications, the Cgd of the MOSFET must be minimized because the power dissipation originates from their charging and discharging during each switching cycle [19–21]. Based on this, Split Gate Trench (SGT) MOSFETs are becoming key components for various high efficiency medium to high voltage power applications due to their relatively low switching losses [22–24]. The SG structure serves as a vertical field plate which optimizes the electric field distribution of the drift region under the instruction of RESURF theory [25]. The grounded SG electrode isolates the control gate from the drift region and the drain electrode, which results in a drastic decrease in the C_{gd} [26–28]. Hence, the Q_{gd} is reduced and better switching performance is assured. Conventional SGT MOSFETs (CSGT-MOSFET) can reduce C_{gd} and Q_{gd} to some extent [29, 30]. But in fact, it is far from bringing the

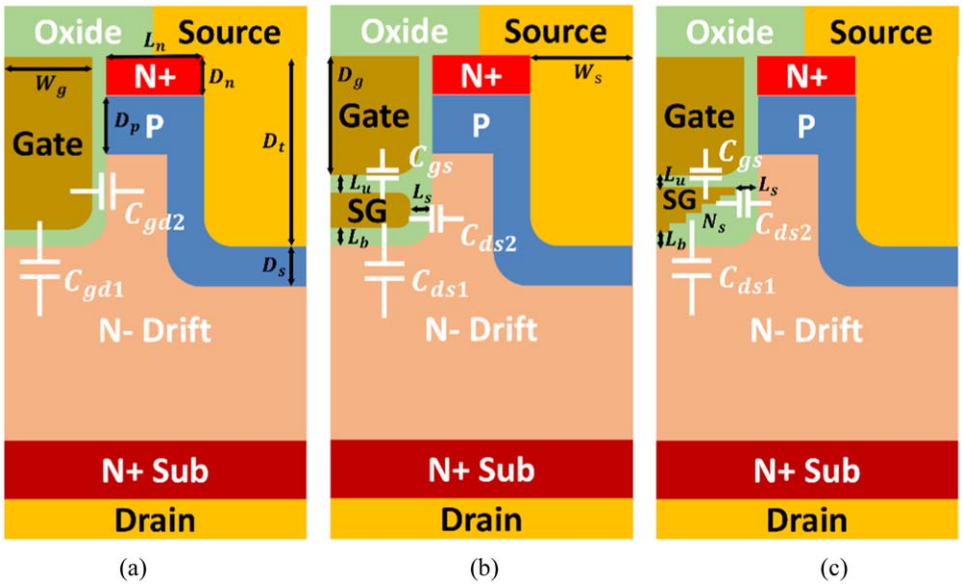

Figure 1. Cross-sectional view of the 4H-SiC (a) DT-MOSFET, (b) CSGT-MOSFET and (c) MSGT-MOSFET.

advantages of SG to full play. Besides, it makes an unsatisfactory compromise between static performance and switching losses.

This paper proposes a novel 4H-SiC Multiple Stepped SGT MOSFET (MSGT-MOSFET). In the MSGT -MOSFET, the SG structure is designed into a multi-step shape, which can achieve ultralow C_{gd} and Q_{gd}. And it achieves low values for the high frequency figure of merit, defined as [$R_{on} \times C_{gd}$] and [$R_{on} \times Q_{gd}$]. The SG structure was optimized by Sentaurus TCAD simulation, and the number of steps was also optimized. Moreover, the switching loss of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET is discussed in this paper.

2. Device structure and mechanism

Figure 1 shows the cross-sectional cell view of the 4H-SiC DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET. In the three SiC MOSFETs under study, a grounded P-shield region is employed to protect the gate oxide from the high electric field. The gate and source double trench technology could reduce the trench mesa without much reliance on special processes and enhance its performance. The three SiC MOSFETs under study are rated for 1.2 kV and have the same cell pitch for a fair comparison. The cell's detailed parameters are listed in table 1. For the CSGT-MOSFET, the L_u, L_s and L_b are the distance from the SG to the gate, the side wall of the oxide trench and the oxide bottom of the trench, respectively. And the initial value of all three is set to 0.05 μm. As for the MSGT-MOSFET, the Ns is the number of steps in the SG structure. The width and height of each step are consistent, which can be calculated by the L_u, L_s, L_b and N_s.

Figure 1 also illustrates the C_{gd} distribution of the three SiC MOSFETs. In figure 1(a), the C_{gd} of DT-MOSFET can be demonstrated as $C_{gd} = C_{gd1} + C_{gd2}$. For the CSGT-MOSFET in figure 1(b), the SG acts as a shielding region between the gate and drain, and the C_{gd} is $C_{gd} = (C_{gs}^{-1} + (C_{ds1} + C_{ds2})^{-1})^{-1}$ [3, 31]. As for the MSGT-MOSFET in figure 1(c), the composition of C_{gd} is the same as that of CSGT-MOSFET. But the only difference is that C_{ds1} and C_{ds2} change dynamically with the number of steps in the SG structure.

In this paper, Sentaurus TCAD tools are used to perform the device simulations and the compact model simulations. Standard SiC physical models are used in the simulation, including Fermi statistics, Shockley-Read-Hallre and Auger recombination, Okuto and GradQuasiFermi avalanche, incomplete dopant ionization, anisotropic material properties, and nonlocal tunneling [16, 32]. The bandgap models are OldSlotboom and NoFermi. Mobility models with doping dependence, high field saturation, and Enormal (IALMob) are also taken into consideration. The fixed charge concentration along the SiC/SiO_2 interface is 1×10^{11} cm^{-2} [33]. Other parameters of the material and models are adapted according to calibrated work in [16, 32, 34]. Besides, we also calibrated with the [4] as shown in figure 2. From this figure, the IV curves calibrated according to the structural simulation of [4] perfectly fit the data in the literature. It can also be found that the current of our proposed CSGT-MOSFET at Vg = 10 V is much higher than that of [4]. It should be noted that although the

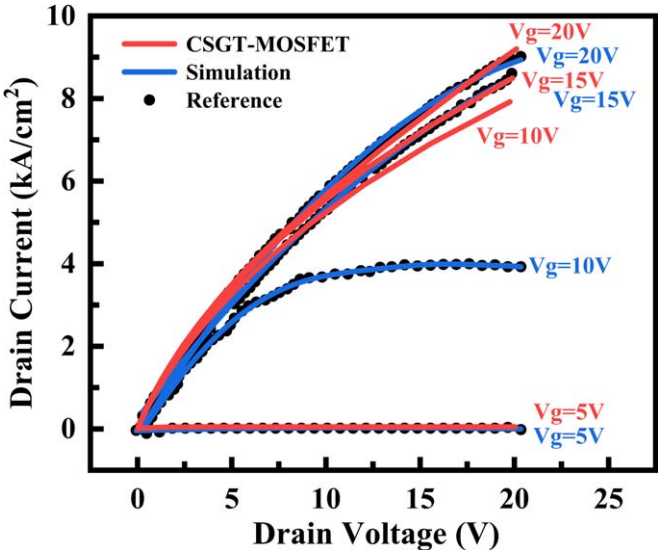

Figure 2. The IV output characteristics of the CSGT-MOSFET, the reference and the simulation based on the reference.

Table 1. Simulation parameters of 4H-SiC MOSFET structure.

Symbol	Structure parameter	Value	Unit
Ns	Substrate doping concentration	1.0×10^{19}	cm^{-3}
Td	Drift thickness	10.0	μm
Nd	Drift doping concentration	8.0×10^{15}	cm^{-3}
Wg	Gate trench half width	0.5	μm
Ws	Source trench half width	0.3	μm
Dt	Trench depth	1.5	μm
Dg	Gate depth	1.0	μm
Nn	N+ doping concentration	1.0×10^{19}	cm^{-3}
Ln	N+ length	0.6	μm
Dn	N+ depth	0.3	μm
Np	P-well doping concentration	1.0×10^{17}	cm^{-3}
Dp	P-well depth	0.5	μm
Ds	P-shield depth	0.3	μm
To	Gate oxide thickness	0.05	μm
Wc	Cell pitch half width	1.4	μm

calibration procedure was carried out, the simulation results are not fully representative of the actual results due to the influence of simulation accuracy and model bias. Therefore, it could be taken as a more general case study.

3. Simulation results and discussion

In order to optimize the HF-FOM [$R_{on} \times C_{gd}$] and [$R_{on} \times Q_{gd}$] of the proposed MSGT-MOSFET, it is necessary to first optimize L_u, L_s and L_b of the SG structure in the CSGT-MOSFET, and then bring the optimal values of the three into the SG of the MSGT-MOSFET. Finally, the step number N_s of SG is optimized to obtain the device with the best performance.

Figure 3 shows the influence of L_u on C_{gd} and Q_{gd}. And the C_{gd} is extracting at $V_{ds} = 800$ V, $V_{gs} = 0$ V and f = 1 Mhz. As L_u increases from 0.05 μm to 0.4 μm, C_{gd} and Q_{gd} remain basically unchanged, which indicates that L_u has little effect on the high frequency performance of the device. This is also verified in [3, 31, 35], since L_u mainly affects the gate-to-source capacitance and has little effect on the gate-to-drain capacitance, and thus has little effect on Q_{gd}. To increase the comparability of the CSGT-MOSFET and the DT-MOSFET, as well as improve the flexibility of the Lb optimization, L_u was set to 0.05 μm for subsequent optimization.

Figure 4(a) shows the dependences of C_{gd} on L_b and L_s for the CSGT-MOSFET. The C_{gd} slowly decreases with the increase in L_b and L_s, the reason is that the thickness of the oxide layer increases, and both the flat plate capacitance C_{ds1} and C_{ds2} decrease, resulting in a reduction of the total gate-to-drain capacitance. The decrease

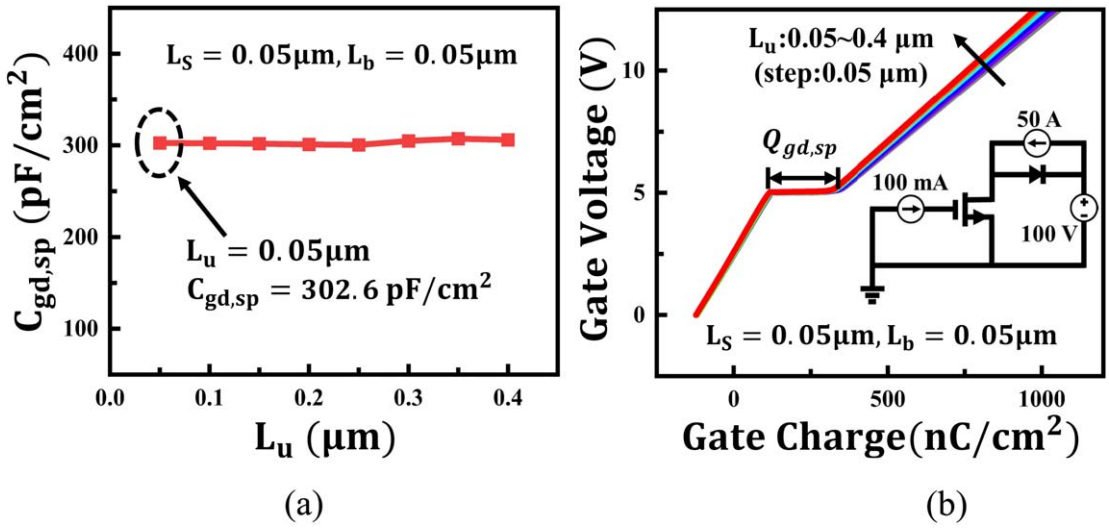

Figure 3. The effect of L_u on (a) Cgd,sp and (b) gate voltage for the CSGT-MOSFET.

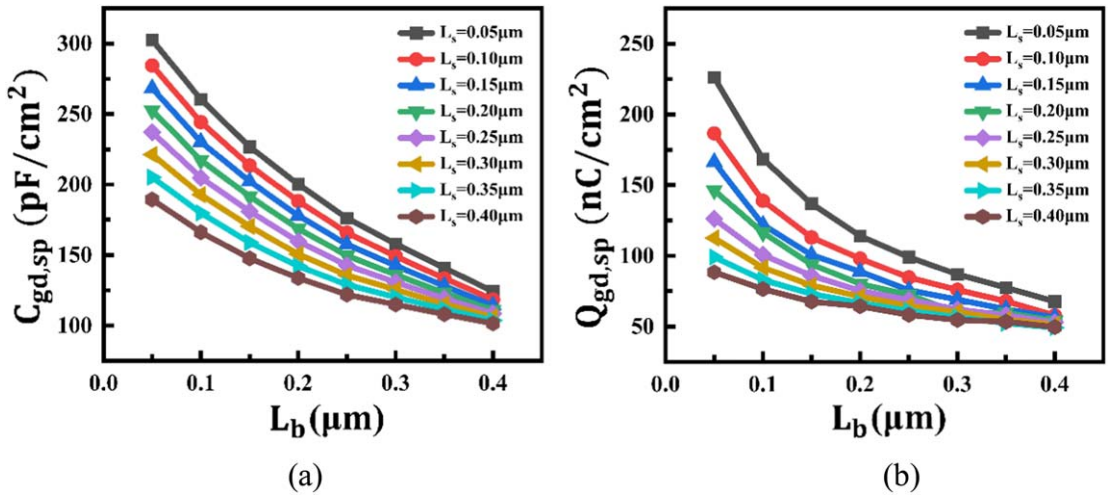

Figure 4. The dependence of (a) Cgd,sp and (b) Qgd,sp on Lb and Ls for the CSGT-MOSFET.

of Cgd in figure 4(a) is consistent with the literature [3, 23]. Due to the decrease in C_{gd}, the device's turn-on speed increases; thus, its Miller platform will become shorter, eventually leading to the reduction of Q_{gd}. And this is the reason why Q_{gd} also decreases with the increase of L_b and L_s in figure 4(b).

Figure 5 shows the relationship between HF-FOM [$R_{on} \times C_{gd}$], HF-FOM [$R_{on} \times Q_{gd}$] and Baliga's figure of merit (BFOM[BV^2/Ron,sp]) [36, 37] at different L_b and L_s, respectively. In figure 5(a), when L_s is set to 0.05 μm, both the HF-FOM and BFOM decrease as L_b increases. And when L_b is 0.15 μm, there is only a slight decrease in HF-FOM with the increase of L_s, and the overall change is not significant; however, BFOM will continue to decrease with increasing Ls, as shown in figure 5(b). Therefore, in order to determine the optimal parameters of the SG structure, the HF-FOM and BFOM of the device need a compromise. Because with the increase of L_b and L_s, the oxide layer at the bottom and side of the SG structure becomes thicker, which will strengthen the depletion region and narrow the current path, leading to an increase in R_{on}. This is confirmed by the current distribution of the device in the on-state in figure 6. When $L_b = 0.15$ μm and $L_s = 0.15$ μm in figure 6(b), the on-resistance of the CSGT-MOSFET is 16.3% (from 1.47 mΩ·cm^2 to 1.71 mΩ cm^2) larger than the initial value ($L_b = 0.05$ μm and $L_s = 0.05$ μm). By fully considering the high frequency characteristics and low frequency characteristics of the CSGT-MOSFET, the BFOM is still maintained at a high level while ensuring a low value of HF-FOM. Finally, the specific parameters of the SG structure were determined with $L_u = 0.05$ μm, $L_b = 0.15$ μm and $L_s = 0.15$ μm.

The thickness of the oxide layer on the top, bottom and side walls of the SG structure of the proposed MSGT-MOSFET is determined, and the remaining SG structure is constructed in a multiple stepped shape. For a

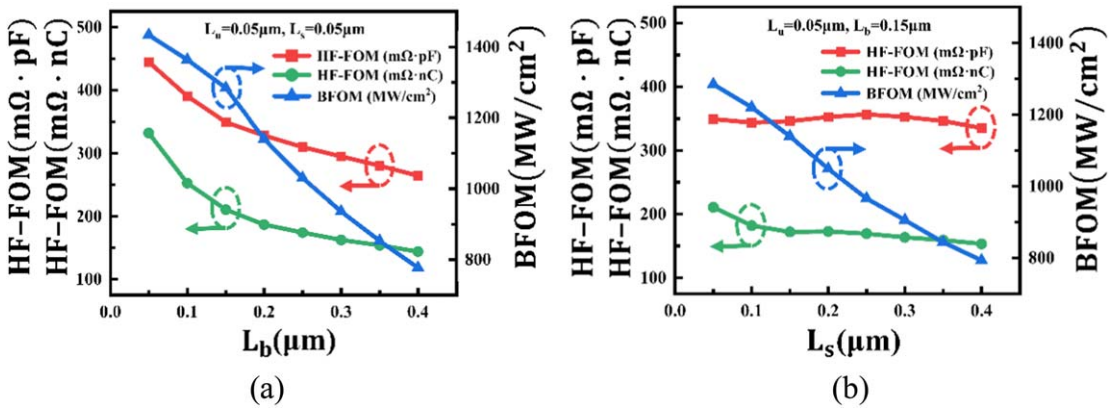

Figure 5. The HF-FOM [$R_{on} \times C_{gd}$], HF-FOM [$R_{on} \times Q_{gd}$] and BFOM as a function of (a) L_b and (b) L_s for the CSGT-MOSFET.

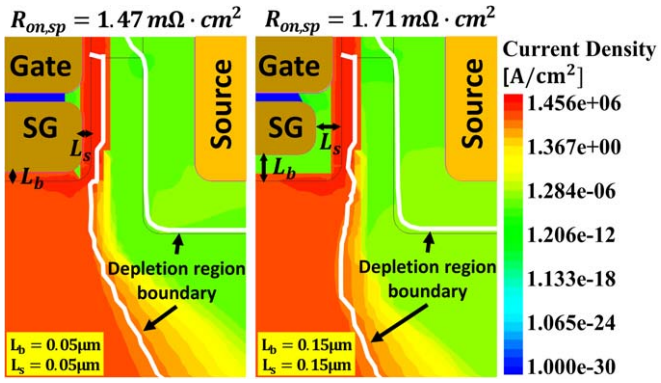

Figure 6. On-state depletion boundary and current density of the CSGT-MOSFET with (a) $L_b = 0.05\ \mu m$, $L_s = 0.05\ \mu m$, (b) $L_b = 0.15\ \mu m$, $L_s = 0.15\ \mu m$.

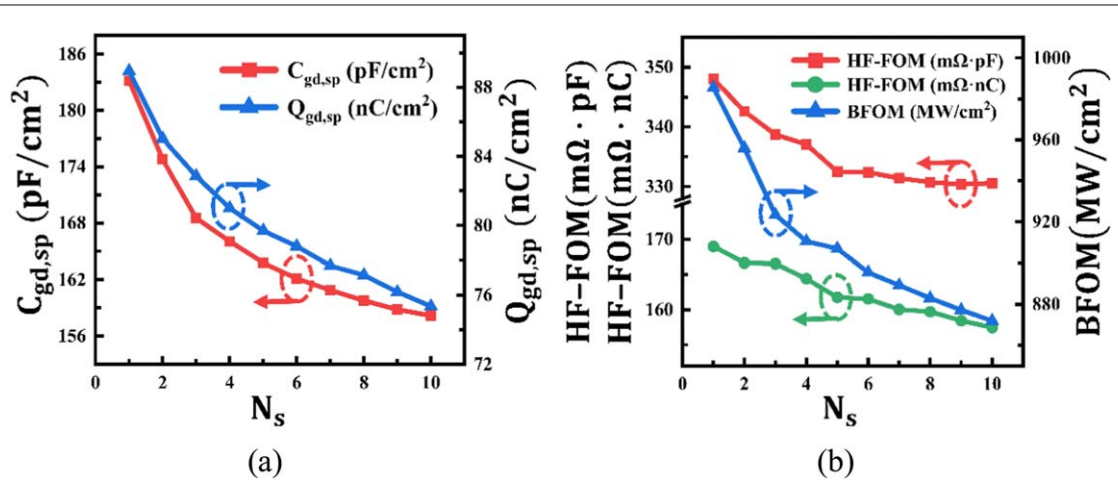

Figure 7. The effect of Ns on (a) $C_{gd,sp}$ and $Q_{gd,sp}$ and (b) HF-FOM [$R_{on} \times C_{gd}$], HF-FOM [$R_{on} \times Q_{gd}$] and BFOM for the MSGT-MOSFET.

determined number of steps N_s, the height and width of the steps are divided equally. Increase N_s from 1 to 10 and observe its effect on C_{gd} and Q_{gd}, as shown in figure 7. An increase in N_s will lead to a decrease in C_{ds1} and C_{ds2}, which in turn decreases C_{gd} and Q_{gd}. From the two slowly falling curves in figure 7(a), we can deduce that when N_s is infinite, the multiple stepped SG structure becomes triangular, and the capacitance and gate charge of the device could reach the minimum limit value at this time. However, etching a perfect triangle in a one-

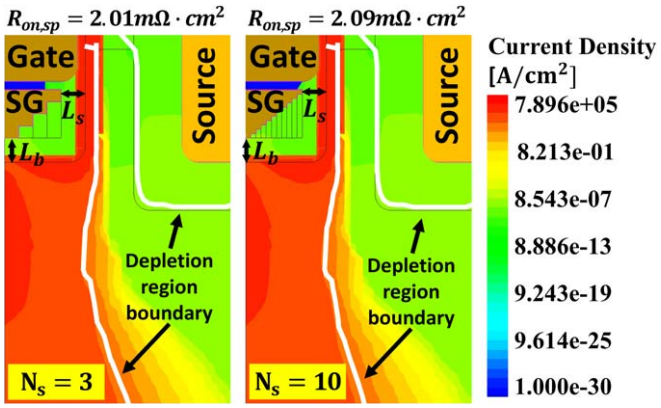

Figure 8. On-state depletion boundary and current density of the MSGT-MOSFET with (a) $N_s = 3$, (b) $N_s = 10$.

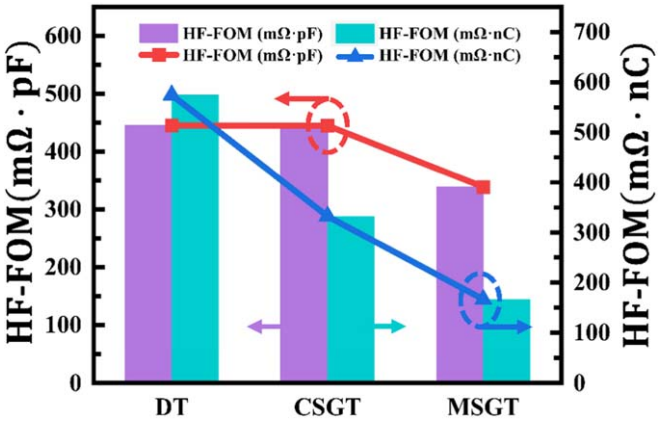

Figure 9. The HF-FOM [$R_{on} \times C_{gd}$] and HF-FOM [$R_{on} \times Q_{gd}$] of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET.

micron-wide trench is a great challenge for the current manufacturing process. By calculation, the curves of HF-FOM and BFOM of the MSGT-MOSFET with Ns are shown in figure 7(b). Unlike the slight decrease in figure 5(b), the magnitude of the HF-FOM decrease with N_s is larger because both the C_{gd} and Q_{gd} decrease significantly, while the increase in on-state resistance R_{on} is slight. It can also be found from this figure that the decline of both HF-FOM and BFOM becomes slower when N_s is greater than 3, from which it can also be inferred that $N_s = 3$ is a better result. From figure 8, it can be found that the current paths of $N_s = 3$ and $N_s = 10$ are basically the same, and the R_{on} of $N_s = 10$ is only increased by 4% (from 2.01 mΩ·cm^2 to 2.09 mΩ cm^2).

To obtain the optimal device performance, a compromise between the high and low frequency characteristics of the MSGT-MOSFET is needed again. On the other hand, as the number of steps of the device increases with N_s, the width and height of each step of the device become narrower, which requires higher precision in the fabrication process. Besides, the formation of each step requires at least one polysilicon etch-back and one oxide layer etch-back. Therefore, the more steps there are, the more complex the manufacturing process will be, and its cost will increase dramatically. After comprehensive consideration, $N_s = 3$ is the optimal result, where the HF-FOM of the MSGT-MOSFET is lower and the BFOM is higher, while the manufacturing process is less complicated and the cost is relatively low. Once N_s is determined, since the height and width of each step are equal, the specific structure of the multiple stepped split gate structure can be obtained by a simple calculation. And the MSGT-MOSFET studied in subsequent simulations are all 3-step SGT-MOSFET.

Figure 9 shows the comparison of the HF-FOM [$R_{on} \times C_{gd}$] and [$R_{on} \times Q_{gd}$] for the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET. The proposed MSGT-MOSFET has the best high frequency characteristics among the three devices. And the HF-FOM [$R_{on} \times C_{gd}$] for the MSGT-MOSFET is 23.9% (from 445.29 mΩ·pF and 444.82 mΩ·pF to 338.73 mΩ·pF) lower than that of both the DT-MOSFET and CSGT-MOSFET. The calculated HF-FOM [$R_{on} \times Q_{gd}$] of the MSGT-MOSFET is 71% (from 574.68 mΩ·nC to 166.55 mΩ·nC) and 50% (from 332.35 mΩ·nC to 166.55 mΩ·nC) lower than that of the DT-MOSFET and CSGT-MOSFET, respectively.

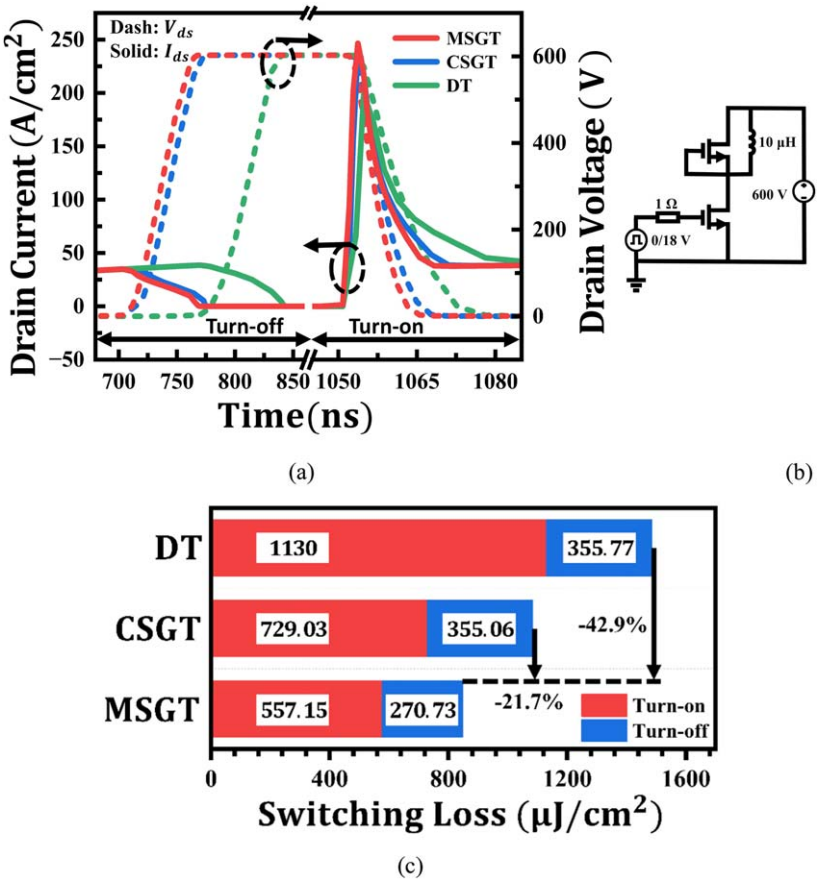

Figure 10. (a) Switching waveform, (b) double pulse test circuit configuration and (c) switching loss of the DT-MOSFET, CSG-MOSFET and MSGT-MOSFET.

The switching waveforms of the three 4H-SiC MOSFETs are further simulated, as shown in figure 10(a). There is a current spike when the device is turned on due to the reverse recovery current. Both the turn-on time and turn-off time of the MSGT-MOSFET are shorter than the DT-MOSFET and CSGT-MOSFET. And the switching loss of the proposed MSGT-MOSFET is greatly reduced due to the smaller C_{gd} and Q_{gd}. As shown in figure 10(c), the MSGT-MOSFET realizes a 42.9% (from 1485.77 μJ cm^{-2} to 847.88 μJ cm^{-2}) and 21.7% (from 1084.09 μJ cm^{-2} to 847.88 μJ cm^{-2}) reduction in the switching loss compared with the DT-MOSFET and CSGT-MOSFET, indicating the great superiority to enhance the system frequency in power conversion applications. Table 2 summarizes the key parameters of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET for a clear presentation.

Considering the feasibility of the proposed MSGT-MOSFET, one available fabrication process is given in figure 11. First, the P-well and N+ can be formed by implantation before trench etching, while the P-shield implantation under the source trench and the sidewall is carried out after source trench etching [see figure 11(a)]. Then, the fabrication of the split gate structure was started, which is the most challenging step of the manufacturing process. The oxide layer and polysilicon are deposited in the gate trench, and then the first etch-back of the polysilicon and the first etch-back of the oxide layer are carried out successively to form the first step [see figure 11(b)]. Repeat the previous step for the second etch-back of the polysilicon and the second etch-back of the oxide layer to form the second step [see figure 11(c)]. Repeat the previous step again for the third etch-back of the polysilicon and oxide layer, and then polysilicon deposition and etch-back to form a 3-step split gate structure [see figure 11(d)]. After the split gate structure is fabricated, the remaining step is compatible with that of the double trench MOSFET. Gate oxidation, polysilicon deposition, and polysilicon etch-back are performed [see figure 11(e)]. Finally, the substrate is thinned and metallized to form the gate, source and drain [see figure 11(f)].

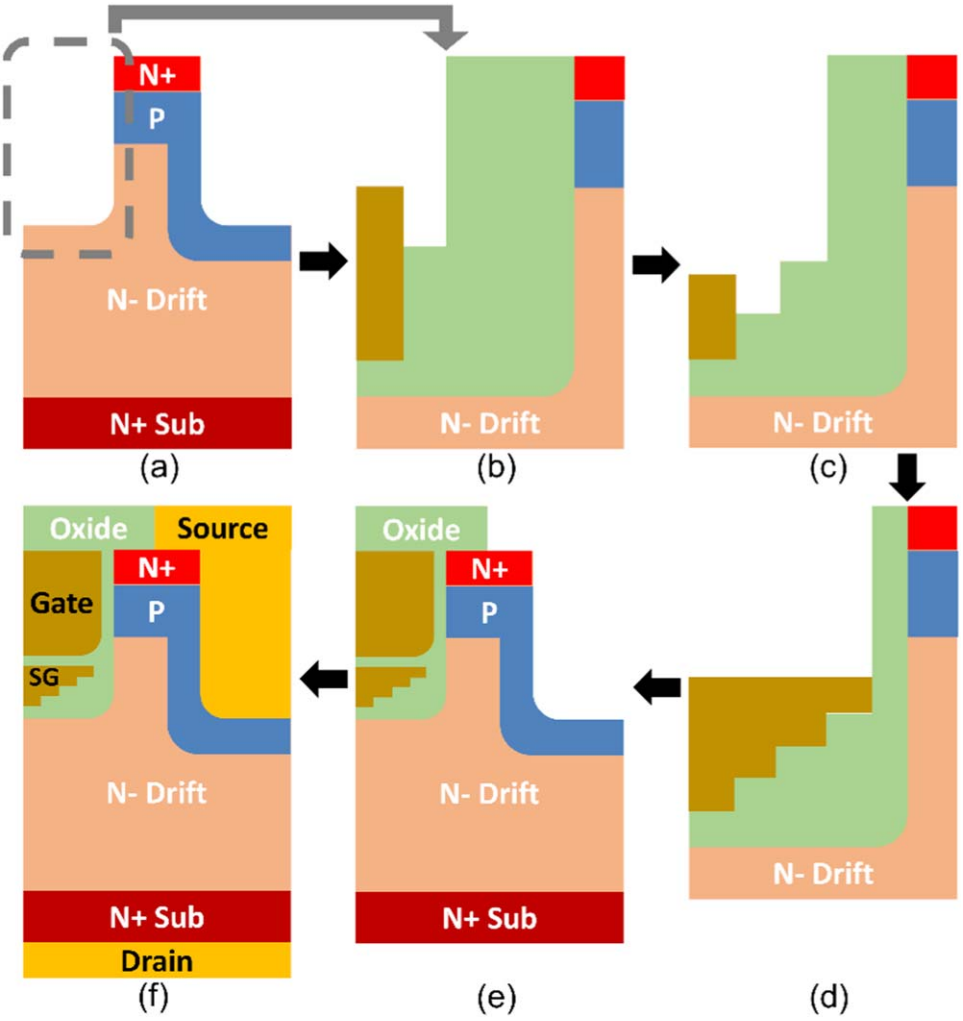

Figure 11. (a) P-well and N+ formation, gate and source trench etching, and p-shield region formation. (b) Gate trench oxidation, polysilicon deposition, and first etch-back of polysilicon and oxide. (c) Second etch-back of polysilicon and oxide. (d) Third etch-back of polysilicon and oxide, and polysilicon deposition and etching. (e) Gate trench oxidation, polysilicon deposition, and etch-back. (f) Metallization.

Table 2. Performance comparison.

Parameter	DT	CSGT	MSGT	Unit
Vth	4.86	4.86	4.88	V
$R_{on,sp}$	1.47	1.47	2.01	$m\Omega{\cdot}cm^2$
BV	1403.68	1401.38	1392.37	V
Cgd,sp	302.92	302.6	168.52	$pF\,cm^{-2}$
Qgd,sp	390.94	226.09	82.86	$nC\,cm^{-2}$
BFOM	1340.35	1335.96	964.52	$MW\,cm^{-2}$
HF-FOM[$R_{on} \times C_{gd}$]	445.29	444.82	338.73	$m\Omega{\cdot}pF$
HF-FOM[$R_{on} \times Q_{gd}$]	574.68	332.35	166.55	$m\Omega{\cdot}nC$
E_{on}	1130	729.03	557.15	$\mu J\,cm^{-2}$
E_{off}	355.77	355.06	270.73	$\mu J\,cm^{-2}$
E_{tot}	1485.77	1084.09	847.88	$\mu J\,cm^{-2}$

4. Conclusion

A novel 4H-SiC multiple stepped SGT MOSFET is proposed in this paper. The thickness of the oxide layer at the top, bottom and side of the SG structure and the number of steps were optimized using Sentaurus TCAD

simulation. And the optimal structural parameters were finally obtained: $L_u = 0.05\ \mu m$, $L_b = 0.15\ \mu m$, $L_s = 0.15\ \mu m$ and $N_s = 3$. The proposed MSGT-MOSFET has reduced HF-FOM [$R_{on} \times C_{gd}$] by 23.9%, and HF-FOM [$R_{on} \times Q_{gd}$] by 71% and 50% compared with that of the DT-MOSFET and CSGT-MOSFET, respectively due to the significantly decreased C_{gd} and Q_{gd}. Furthermore, the total switching losses including turn-on and turn-off processes are reduced by 42.9% and 21.7% compared with the DT-MOSFET and CSGT-MOSFET, which makes the dMSGT-MOSFET an excellent choice for high frequency and high power applications, such as on-board charger (OBC), power converters, inverters, etc.

Acknowledgments

This work was supported by the General Program of National Natural Science Foundation of China under Grant No. 62071073, the Frontier Innovation Program under Grant No. 19-163-00-KX-002-024-01 and the Key Laboratory Open Fund under Grant No. GD20201.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

ORCID iDs

Jingping Zhang https://orcid.org/0000-0003-3706-7084

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