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A 4-μW Bandwidth/Power Scalable Delta–Sigma Modulator Based on Swing-Enhanced Floating Inverter Amplifiers

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***Abstract*— This article presents a fully dynamic scalable switched-capacitor delta–sigma modulator that achieves a 94.1-dB dynamic range (DR). Power-and- bandwidth scalability by only changing the clock frequency is achieved using a capacitively biased and swing-enhanced floating inverter operational transconductance amplifier (OTA). Fabricated in a 180-nm CMOS process, the prototype achieves an signal-to-noise-and-distortion ratio (SNDR) of >87 dB across 4× scaling from 100 to 400 kHz of the sampling frequency f_S. At 200-kHz f_S, it achieves an SNDR/DR of 89.3/94.1 dB while consuming 4 μW, leading to a DR-based Schreier figure of merit (FoM) of 177.1 dB.**

***Index Terms*— Bandwidth (BW) scalable, high resolution, ultra-low power.**

I. Introduction

THE evolution of the Internet of Things (IoT) has fueled the demand for analog-to-digital converters (ADCs) with lower power dissipation and higher resolution in the past decade. Most of these converters for the IoT applications are powered by batteries or energy harvesters, so an ultra-low-power (ULP) design is essential to allow for a longer lifespan of up to 10–15 years. This type of converters also needs to measure small signals with different bandwidth (BW) requirements in the sub-kilohertz range for different applications. Moreover, IoT systems are often heavily duty-cycled to reduce power consumption, where on-demand conversions are executed when events of interest are detected. To allow for more flexible system-level partitioning and to cover a broader application space, higher resolution with low power consumption is desired while supporting scalable BW and power.

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However, it is challenging to achieve fully dynamic operation and high resolution simultaneously. Successive approximation register (SAR) ADCs feature fully dynamic operation and hence are BW and power scalable, and ULP designs have been reported [1]–[4]. They do not require operational transconductance amplifiers (OTAs), making them more power-efficient and suitable for conversion on-demand. However, to achieve high resolution, they need to implement complex calibration schemes to tackle mismatches in their capacitive DACs [5]–[7], which increases power and area. A low noise comparator is also required, which is often power-hungry.

A widely used architecture for high-resolution applications is the discrete-time delta–sigma modulator (DTDSM), which can achieve high power efficiency by oversampling and noise shaping [8]–[12]. However, their loop filters do not readily scale with the sampling frequency f_S on the fly because they are based on OTAs that draw static bias currents. Especially in ULP applications, the SNR of previous designs using active [13] or passive [14] loop filters was limited to about 50 dB. In these designs, the loop filter has been the bottleneck to achieve low power and high resolution simultaneously.

To improve the power efficiency of DTDSM, inverter-based integrators are a popular choice [8]. However, the CMOS inverter's quiescent current is strongly dependent on its input voltage and is prone to process, supply voltage, and temperature (PVT) variations. They usually require special biasing circuits addressing PVT sensitivity [9], [15], [16] and common-mode feedback (CMFB) circuitry [8], [9], [15], [16] that consumes extra power and takes a certain amount of time to settle after waking up in a ULP design before the output becomes valid.

The floating inverter amplifier (FIA) [17] presents an option for a fully dynamic OTA implementation. However, it suffers from a limited output swing and an ill-defined operating point, both of which are functions of the supply and threshold voltages. In [18], multiple supplies are required to ensure sufficient speed and output swing to address this issue, which increases system complexity.

In this article, a capacitive biasing technique is introduced to improve the FIA's performance over PVT and increase its

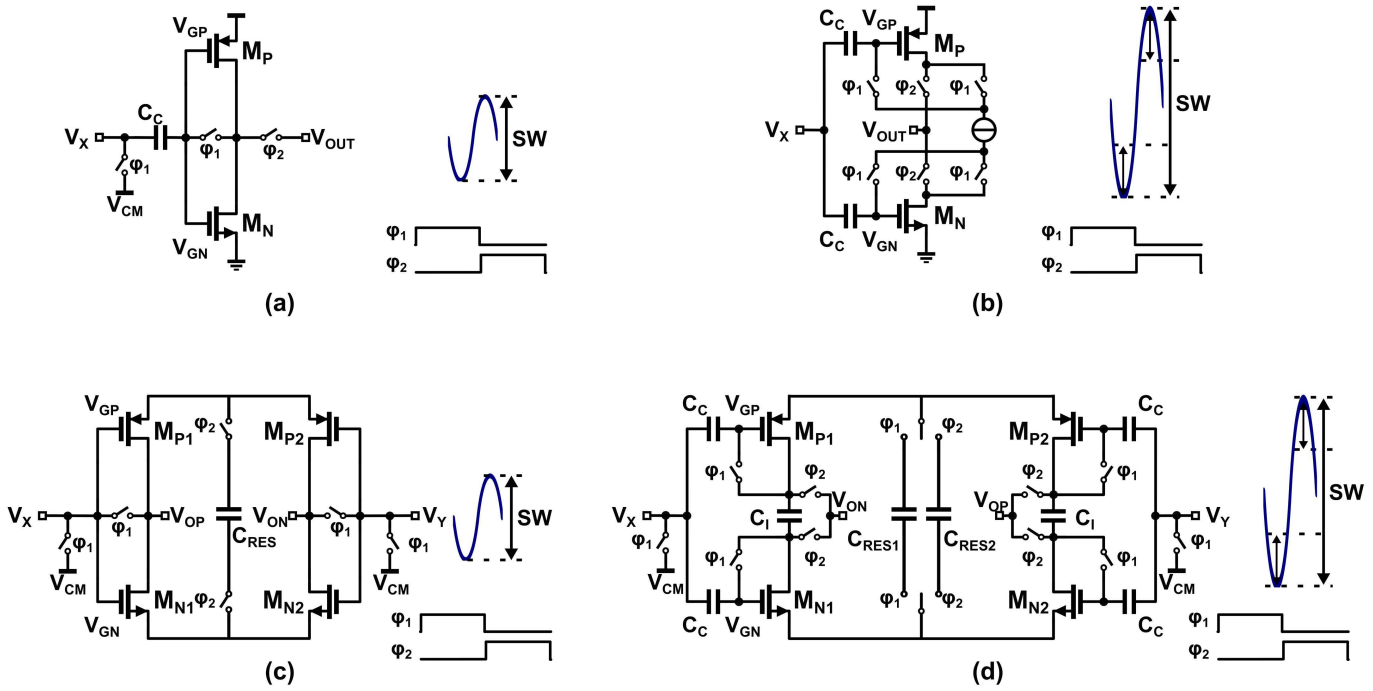


Fig. 1. (a) Conventional inverted-based OTA [8]. (b) Dynamic biasing scheme [9]. (c) Conventional floating inverted-based OTA [17], [18]. (d) Proposed capacitive biasing scheme.

output swing [19]. It also enables the proposed amplifier to adaptively change its BW when f_S is varied, enabling BW and power scaling of the DTDSM by simply varying the clock frequency. Measurement results of the prototype implemented in a 180-nm CMOS process indicate a consistent performance of >87-dB signal-to-noise-and-distortion ratio (SNDR) over 4× clock frequency scaling. The prototype only consumes 4 μW when operating with an oversampling ratio of 125- and 800-Hz signal BW.

This article is organized as follows. Section II reviews several existing inverter-based OTA designs. Section III presents the proposed capacitively biased swing-enhanced FIA (SEFIA) and analyzes the operation of the SEFIA in detail. The prototype SEFIA-based DTDSM implementation is detailed in Section IV, followed by measurement results in Section V. Section VI concludes this article.

II. Review of Existing Inverter-Based OTAs

Implementing OTAs has become increasingly challenging due to process scaling and the continuous quest to low power consumption. In [8], the use of logic inverters as OTAs is proposed, which achieves high power efficiency under low supply voltages because both NMOS and PMOS devices contribute transconductance (g_M). However, its bias current is sensitive to PVT variations. For example, across process variations from SS corner to FF corner, the supply current and g_M can vary by several orders of magnitude. To address this issue, a dedicated voltage regulator [20] or body biasing [21] can be applied at the cost of increased complexity and power. Furthermore, unlike conventional OTAs with differential input, the inverter does not offer a well-defined virtual ground. Therefore, they typically employ auto-zeroing (AZ) to store the tripping voltage (including offset and $1/f$ noise) onto a coupling capacitor C_C between the inverter's input and the actual input signal V_X, as shown in Fig. 1(a).

The inverter-based amplifier is also sensitive to input common-mode (CM) variations. To process a fully differential input robustly, extra CMFB circuitry is also required, which increases the loading and noise [8] and, thus, the amplifier's power consumption. Also, the amplifier's output swing is limited to $(V_{THN} + |V_{THP}| - 2V_{DSAT})$.

To achieve robust operation across PVT variations, a dynamic biasing scheme [9] can be applied, as shown in Fig. 1(b). During the AZ phase, a floating current source is employed to enforce a well-defined bias current by storing the bias voltages for the NMOS and PMOS devices separately on the 2 C_C values. This also improves the output swing to $(V_{DD} - 2V_{DSAT})$. However, like the inverter-based OTA in Fig. 1(a), the AZ procedure consumes as much additional power as the actual signal amplification.

Recently, the FIA is proposed [17], [18], shown in Fig. 1(c), which is insensitive to input CM variations and operates without CMFB. This is because the FIA is supplied by a reservoir capacitor C_{RES}, which forces the CM output current to zero [22]. However, similar to the conventional inverter-based amplifier, the FIA suffers from swing limitations, and its g_M varies considerably across PVT variations.

III. Analysis of the Proposed SEFIA

This section first presents the proposed capacitively biased swing enhancement technique. Afterward, the swing enhancement, BW scalability, and power efficiency of the proposed SEFIA are discussed.

A. Proposed SEFIA Using Capacitive Biasing

The proposed SEFIA using capacitive biasing is shown in Fig. 1(d). It is supplied by reservoir capacitors similar to the FIA in Fig. 1(c) and employs separate input coupling capacitors (C_C's) as the dynamically biased inverter in Fig. 1(b). The capacitor C_I functions as a dynamic floating current source. During the AZ operation, $M_{N1,2}$ and $M_{P1,2}$ are diode-connected, charge redistribution occurs between C_{RES1}, C_I, and the C_C values, and the bias voltages for $M_{N1,2}$ and $M_{P1,2}$ are stored on the C_C's. During the amplification phase, C_I is discharged, and the C_C values couple the input to $M_{N1,2}$ and $M_{P1,2}$. Two reservoir capacitors, C_{RES1} and C_{RES2}, supply the amplifier in a ping-pong manner during the two phases.

Compared to the conventional FIA, the SEFIA achieves a wider output swing by the voltage across C_I at the end of AZ. Meanwhile, the fully dynamic and CMFB-free operation of the FIA is also preserved.

Compared to the dynamically biased inverter-based OTA in Fig. 1(b), which consumes as much power in AZ as in the amplification phase, C_{RES1} can be set smaller than C_{RES2} in the SEFIA to save power, while the extra degree of freedom offered by C_C can be used to ensure sufficient driving capability for amplification.

B. Swing Enhancement

Since the SEFIA is supplied dynamically by reservoir capacitors, its bias current changes with time. This section discusses its operation in detail and analyzes the output swing and BW characteristics of the SEFIA, which are essential parameters for switched-capacitor (SC) circuits.

Fig. 2(a) shows the operation of SEFIA during $\Phi 1$. At the beginning of AZ, charge redistribution between $C_{C1\text{-}4}$ and the $C_{I1,2}$ occurs. This takes little time, assuming the switches' $R_{on} \ll 1/g_M$. Then, the reservoir capacitor C_{RES1} discharges into the $C_{I1,2}$ through $M_{N1,2}$ and $M_{P1,2}$. During this stage, the instantaneous current is a function of the voltages on C_{RES1} and $C_{I1,2}$ and changes with time. As shown in Fig. 2(b), the current flowing into $C_{I1,2}$ reduces over time, as the overdrive of $M_{N1,2}$ and $M_{P1,2}$ reduces. At the end of $\Phi 1$, the gate voltages of $M_{N1,2}$ and $M_{P1,2}$ are sampled onto $C_{C1\text{-}4}$.

Compared to the conventional FIA, the output swing of the SEFIA is increased by the voltage across $C_{I1,2}$ at the end of AZ, which changes as the clock frequency, and thus, the duration of AZ is varied, as shown in Fig. 2(b). Assuming that $M_{N1,2}$ and $M_{P1,2}$ operate in weak inversion, it can be shown that the voltage across $C_{I1,2}$ increases logarithmically with time[1]

$$V_{CI}(t) = V_{GP}(t) - V_{GN}(t) = \frac{2C_{RES1}}{2C_I + C_{RES1}} nU_T \ln(\zeta t) + c \tag{1}$$

[1]To simply the derivation, we assume that the NMOS and PMOS have the same $I_{D0}W/L$, implying the same g_M. In reality, the PMOS and NMOS devices have different mobility and threshold voltages, and in the implementation, the W/L of the PMOS is two times that of the NMOS, which gives acceptable, but not exact matching of g_M's, so the waveform for V_{GP} and V_{GN} has different shapes.

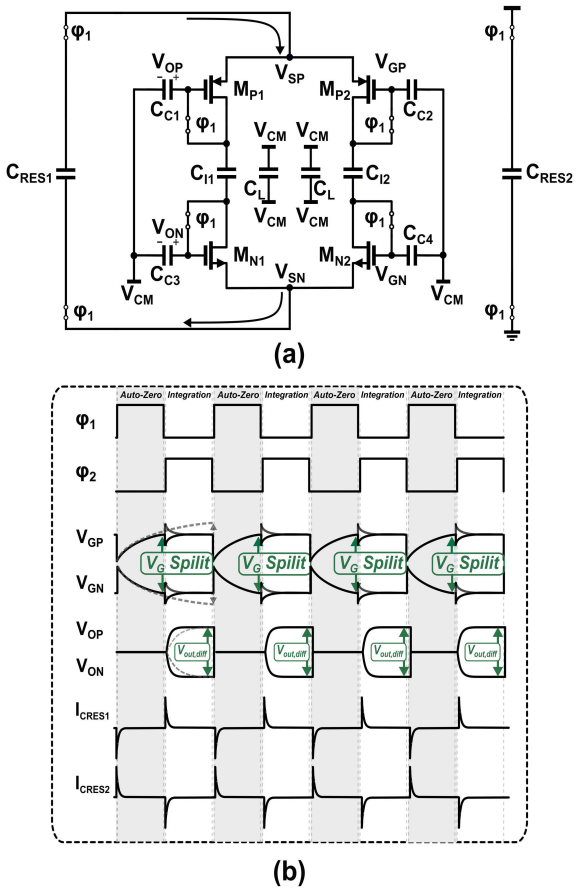


Fig. 2. (a) Operation and (b) time-domain behavior of the SEFIA during AZ.

where

$$c = \frac{C_{RES1}}{2C_I + C_{RES1}} V_{DD} \tag{2}$$

where n is the slope factor in weak inversion and U_T is the thermal voltage kT/q. ζ is also a constant (see the Appendix), and V_{GP} and V_{GN} are the gate voltages for the PMOS and NMOS devices, respectively. Fig. 3 shows that the amount of swing enhancement is a function of the clock period, in which AZ takes half of the time. As shown, the swing increases less when the clock period is reduced. However, due to the logarithmic relation in (1), the variation across the clock period is relatively small.

Fig. 4(a) shows the simulated dc gain of an example of the proposed SEFIA and the conventional FIA, sized for the same dc gain and settling speed, versus output swing when operating with a 200-kHz clock. Compared to the conventional FIA, the swing is expanded by 1.8 times, from 0.62 to 1.12 V at 6-dB gain compression. According to (1), the swing also widens with a higher supply voltage. As shown in Fig. 4(b), when V_{DD} increases from 1.2 to 1.8 V, the output swing expands accordingly from 0.82 to 1.37 V.

C. Scalable BW

The conventional FIA is turned off automatically after the reservoir capacitor is discharged, and the output voltage

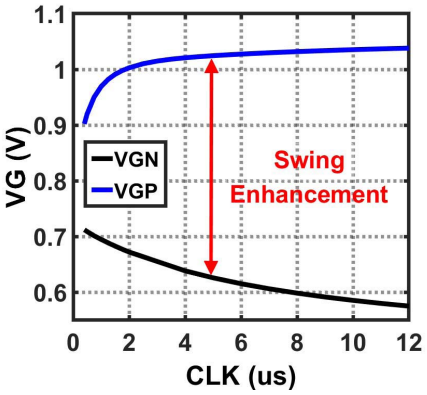


Fig. 3. V_{GN} and V_{GP} versus CLK period at the end of AZ.

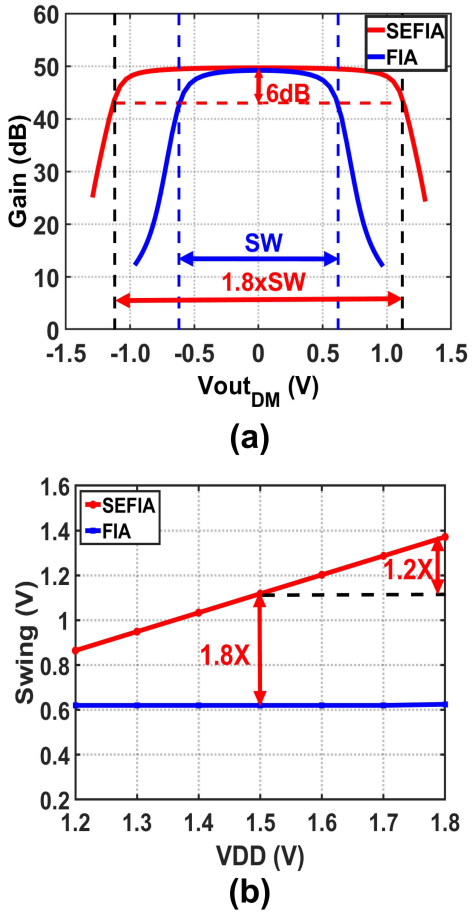


Fig. 4. (a) Output swing comparison of the proposed SEFIA and conventional FIA. (b) Output swing as a function of the supply voltage.

remains constant afterward until the next clock cycle, leading to fully dynamic power consumption.

Similarly, the proposed SEFIA is also fully dynamic, as shown in Fig. 5. Furthermore, the amplifier's speed tracks the clock frequency f_S. For a lower f_S, C_{RES1} has more time to discharge during $\Phi 1$, and it can be shown that assuming weak inversion operation, the V_{GS}'s of $M_{N1,2}$ and $M_{P1,2}$ reduces logarithmically with time t due to the exponential I_D–V_{GS}

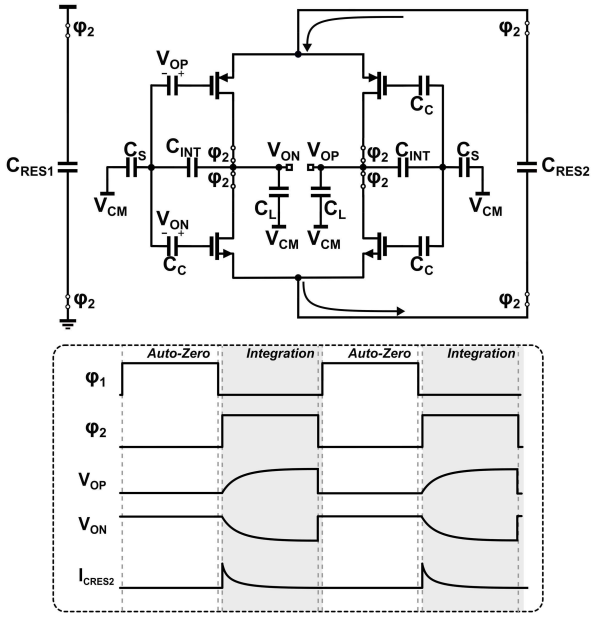


Fig. 5. Time-domain behavior of the proposed SEFIA during the amplification phase.

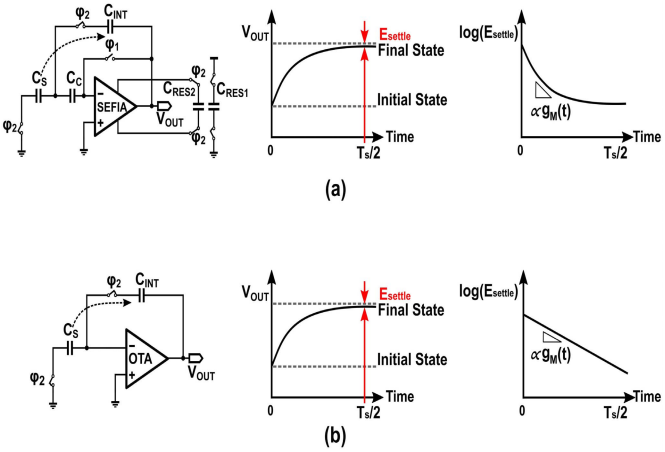


Fig. 6. Equivalent circuit for evaluating the settling errors of the SC integrator based on (a) SEFIA and (b) conventional amplifier with constant g_M.

relation [22], i.e.,

$$V_{GS} \sim -\ln(at+b) \tag{3}$$

where a and b are constants related to device parameters and capacitance values (see the Appendix). Since the g_M–V_{GS} relation is also exponential, we have

$$g_M \sim \exp(V_{GS}) \sim \frac{1}{at+b}. \tag{4}$$

For the low-BW applications of this work, the clock period is large, and g_M becomes approximately proportional to f_S.

Since g_M changes with time, we consider the effective g_M by evaluating the settling error of the SEFIA and compare it with that of a conventional amplifier with a constant g_M using the equivalent circuits shown in Fig. 6 and assuming

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISSCC'18 Gagnon-Turcotte	ISSCC'18 Yeknami	ISSCC'19 Konijnenburg	ISSCC'20 Jang	ISSCC'18 Chandrakumar
Process (nm)	180	130	65	55	110	65
Architecture	SCSD	SCSD	SCSD	SAR	CTSD	CTSD
BW/Power Scalable	Yes	No	No	Yes	No	No
Area (mm^2)	0.75	-	-	-	0.078	0.053
V_{DD} (V)	1.5	1.2	0.3	0.9	1	1.2
Power (μW)	4	4.4	0.18	0.9	6.5	4.5
f_S (Hz)	200k	500k	256k	32k	1280k	400k
OSR	125	25	42.7	107	64	40
BW (Hz)	800	7k	3k	150	10k	5k
DR (dB)	94.1	-	-	-	81	96.5
SNDR (dB)	89.3	60.8	60	78.8	80.4	93.5
FoM_{DR}	177.1	-	-	-	172.9	187.0
FoM_{SNDR}	172.3	154.4	162.2	161	172.3	184.0

infinite dc gain. For the SEFIA, we then define the effective transconductance $g_{M,eff}$ to be equal to the g_M of a conventional amplifier with the same settling error E_{settle} at the end of the $\Phi 2$. From the conventional amplifier, we have

$$g_{M,eff} = -\frac{2f_S C_O}{\beta} \ln E_{settle} \tag{5}$$

where C_O is the total load capacitance and β is the feedback factor around the amplifier. For the SEFIA, the following can be derived (see the Appendix)

$$E_{settle} = \left(\frac{t}{\alpha} + 1\right)^{-\frac{C_{RES2}}{C_O}} \tag{6}$$

where $\alpha = (nU_T/I_{D0})(L/W)C_{RES2}\exp(((V_{GP}(T_S/2) - V_{DD})/nU_T))$.

Combining (5) and (6), we have

$$g_{M,eff} = \frac{2f_S C_{RES2}}{\beta} \ln\left(\frac{1}{2\alpha f_S} + 1\right). \tag{7}$$

Fig. 7 plots the simulated $g_{M,eff}$, as a function of f_S, which is almost linear.

D. Power Efficiency

As shown in Fig. 6, the reduction in $\log(E_{settle})$ equals the integral of $g_M(t)$ over time. In other words, to achieve the same settling accuracy, the time-averaged g_M of the SEFIA and the conventional amplifier is the same. Therefore, assuming similar g_M/I_D ratio and the same settling accuracy, the two amplifiers will consume a similar amount of power in the amplification phase.

IV. DTDSM WITH SEFIA

Fig. 8 shows the third-order DTDSM employing the proposed SEFIA. It employs a feedforward topology for low

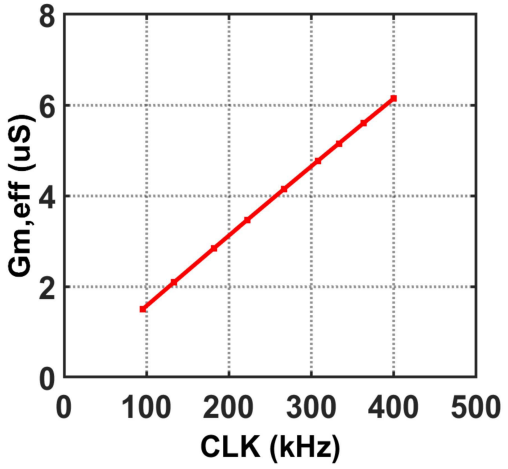


Fig. 7. $G_{m,eff}$ versus CLK frequency of the proposed SEFIA.

distortion and optimally spread NTF zeros for high signal-to-quantization-noise ratio (SQNR), and passive feedforward summation is implemented using $C_{F1\text{-}3}$. The input sampling capacitors are sized to 1 pF to meet the kT/C noise requirement. The 1-bit quantizer is composed of an FIA-based preamplifier and a StrongArm latch. The optimized NTF zeros are implemented with another SC sampling branch (shown as x for simplicity in Fig. 8). Each of the integrators has its own set of C_{RES1} and C_{RES2} and is optimized according to its noise and swing requirements. The SEFIAs are designed for 50 dB of dc gain. The resulting finite dc gain impact on SQNR is negligible according to MATLAB simulations.

Fig. 9 shows the complete schematic of the SEFIA-based SC integrator and its timing diagram. A short reset pulse is used at the beginning of $\Phi 1$ to remove any differential voltage

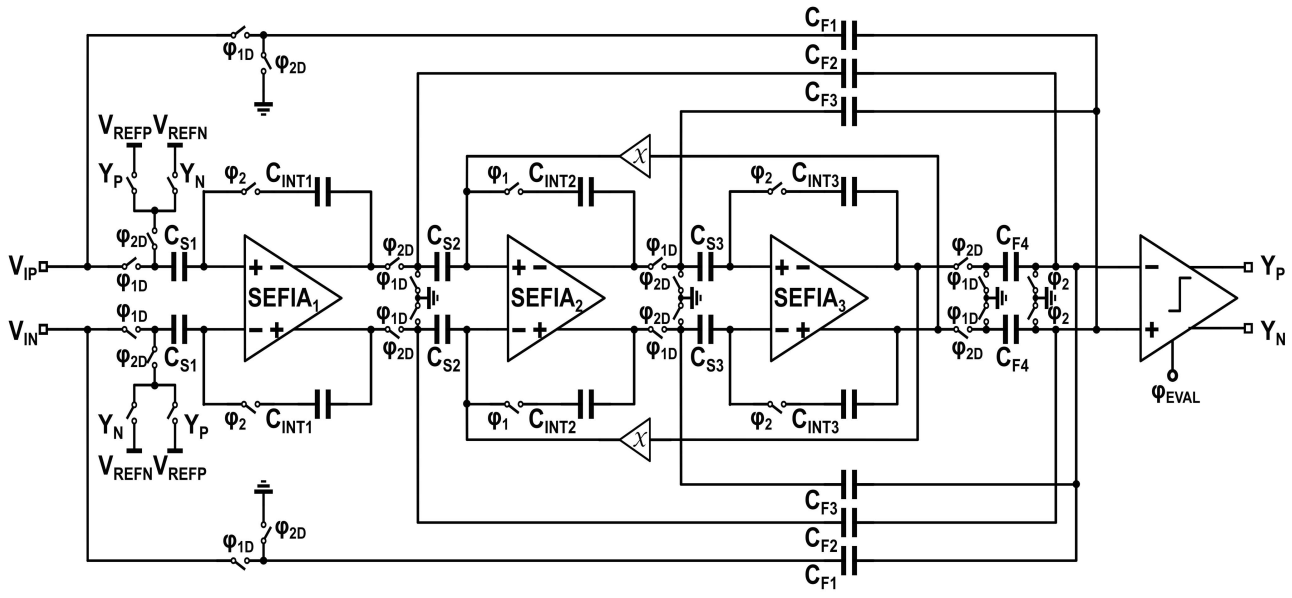
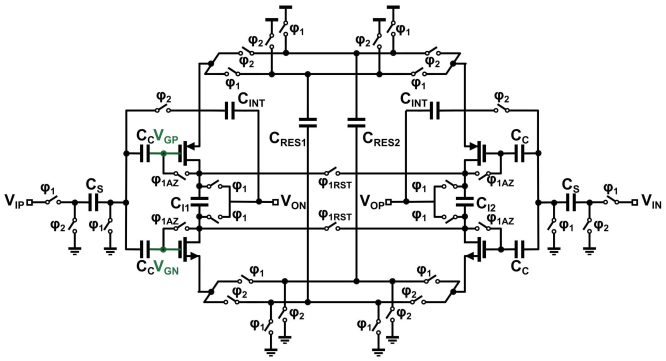


Fig. 8. Circuit schematic of the $\Delta\Sigma$ modulator.



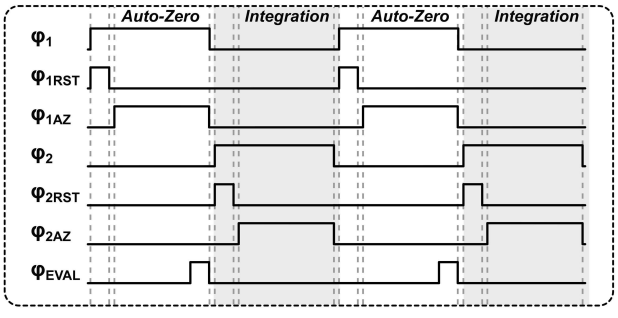


Fig. 9. Circuit schematic of the SEFIA-based SC integrator and the corresponding timing diagram.

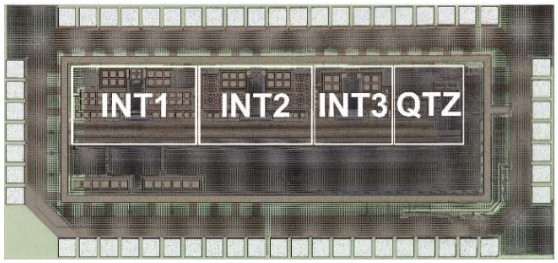


Fig. 10. Chip micrograph of the $\Delta\Sigma$ modulator.

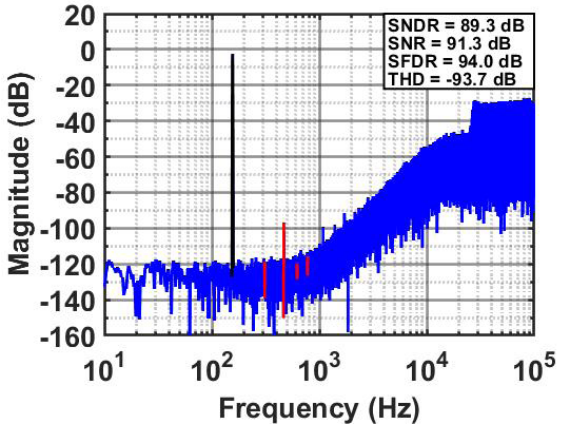


Fig. 11. Measured output spectrum at 200-kHz f_S(500k points). Harmonic distortion bins are plotted in red.

at the top and bottom plates of $C_{I1\text{-}2}$ and ensure that the AZ operation is signal-independent.

V. Measurement Result

The modulator is fabricated in a 180-nm standard CMOS technology and occupies 0.75 mm^2. Fig. 10 shows the chip microphotograph. At 200-kHz f_S, the DTDSM consumes 4 μW from a 1.5-V supply.

Fig. 11 shows the output spectrum at 200 kHz f_S. The DTDSM achieves a peak SNDR of 89.3 dB. Fig. 12 shows the measured SN(D)R performance over input amplitude at a 1.5-V supply. The prototype achieves a dynamic range (DR) of 94.1 dB. To verify the performance over supply voltage variations, Fig. 13 shows the measured SN(D)R of the DTDSM

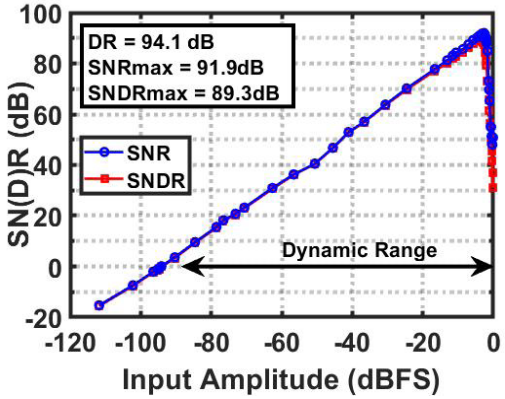


Fig. 12. Measured SN(D)R versus input amplitude at $f_S = 200$ kHz.

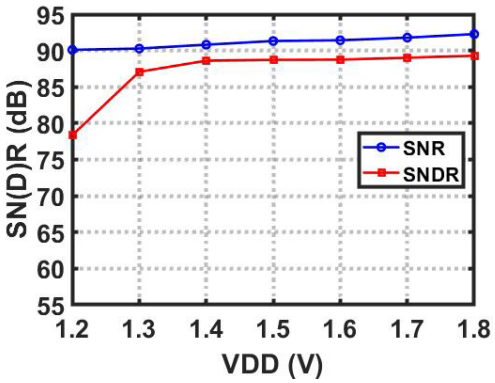


Fig. 13. Measured SN(D)R versus V_{DD}.

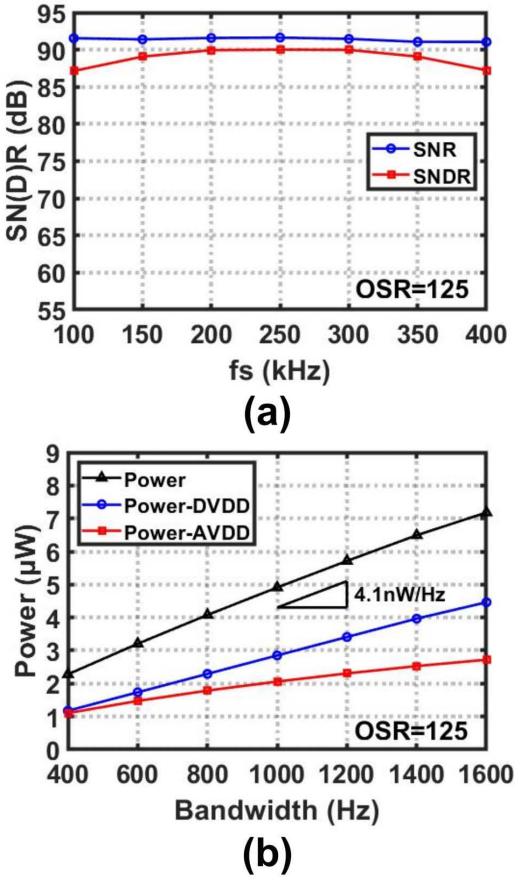


Fig. 14. (a) Measured SN(D)R versus f_S when OSR = 125. (b) Power consumption versus signal BW at $V_{DD} = 1.5$ V.

when the supply and reference are varied together from 1.3 to 1.8 V. The SNDR remains above 87 dB, demonstrating the robustness of the proposed SEFIA to supply voltage variations. At low supply, the SNR is lower since the full-scale input amplitude reduces when the supply voltage and reference are reduced. Toward 1.2 V, the SNDR drops because the amplifier swing becomes too small.

Fig. 14(a) presents the performance for various clock frequencies at 1.5-V supply. Due to the BW scalability of the SEFIA, the SNDR remains above 87 dB for f_S between 100 and 400 kHz. At high f_S, the SNDR slightly drops due to the reduced output swing. At low f_S, the SEFIA's driving ability reduces, as mentioned in Section III. Although the small-signal effective g_M scales linearly with f_S, the large-signal performance degrades because the transistors operate in deeper subthreshold, causing the drop in the SNDR. The power consumption also scales with f_S, from 2.2 to 7 μW, as shown in Fig. 14(b).

Table I shows the performance summary and comparison with other state-of-the-art microwatt-level ADCs with similar BW. This is the first power/BW scalable DTDSM, due to the capacitive biased SEFIA. Moreover, it achieves the highest SNDR among the power/BW ADCs while maintaining high energy efficiency. The single-bit DTDSM achieves a Schreier figure of merit (FoM) of FOM_{DR} of 177.1 dB and FOM_{SNDR} of 172.3 dB, which are among the best reported for single-bit DTDSM designs.

VI. Conclusion

In this article, a capacitively biased FIA is presented, which features a wide voltage swing that increases with the supply voltage and a scalable BW that adapts to the clock frequency. A DTDSM employing the proposed SEFIA-based integrators is implemented, demonstrating comparable power efficiency to state-of-the-art DTDSM and features scalable BW and power over two octaves of the sampling frequency range. The proposed SEFIA is thus a promising candidate for implementing power-efficient, fully dynamic SC circuits.

Appendix

Detailed Analysis of the SEFIA

Since the SEFIA is used for a low-power application in this work, the transistors mainly operate in weak inversion to take advantage of the high g_M/I_D ratio. When the transistor's V_{DS} exceeds $3U_T$ to $5U_T$ ($\sim$130 mV), the drain current can be expressed as

$$I_{DS} = I_{D0}\frac{W}{L}\exp\left(\frac{V_{GS}}{nU_T}\right) \tag{8}$$

where I_{D0} is a process-dependent parameter of the transistor, n is the slope factor in weak inversion, and U_T is the thermal voltage kT/q. The transconductance is then given by

$$g_M = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_{D0}}{nU_T}\frac{W}{L}\exp\left(\frac{V_{GS}}{nU_T}\right). \tag{9}$$

During the AZ operation, C_{RES1} discharges into C_I through the diode-connected transistors (Fig. 3). According to charge conservation,

$$\begin{aligned} C_{\mathrm{RES1}}(V_{\mathrm{DD}} - (V_{\mathrm{SP1}}(t) - V_{\mathrm{SN1}}(t))) \\ = (C_C + 2C_I)(V_{\mathrm{GP}}(t) - V_{\mathrm{GN}}(t)) \\ + C_C(V_{\mathrm{GP}}(T_S/2) - V_{\mathrm{GN}}(T_S/2)). \end{aligned} \quad (10)$$

Since the current flowing through the two terminals of each capacitor C_I, C_{RES1}, and C_{RES2} must be equal, we have

$$V_{\mathrm{GP}}(t) + V_{\mathrm{GN}}(t) = V_{\mathrm{GP}}(T_S/2) + V_{\mathrm{GN}}(T_S/2) \quad (11)$$

$$V_{\mathrm{SP1}}(t) + V_{\mathrm{SN1}}(t) = V_{\mathrm{SP1}}(T_S/2) + V_{\mathrm{SN1}}(T_S/2) \quad (12)$$

$$V_{\mathrm{SP2}}(t) + V_{\mathrm{SN2}}(t) = V_{\mathrm{SP2}}(T_S/2) + V_{\mathrm{SN2}}(T_S/2). \quad (13)$$

Here, $V_{\mathrm{GP}}(T_S/2)$ and $V_{\mathrm{GN}}(T_S/2)$ are the final values of the PMOS and NMOS gate voltages, respectively. $V_{\mathrm{SP1}}(T_S/2)$ and $V_{\mathrm{SN1}}(T_S/2)$ are the final voltages at the two terminals of C_{RES1}. Similarly, $V_{\mathrm{SP2}}(T_S/2)$ and $V_{\mathrm{SN2}}(T_S/2)$ are the final voltages at the two terminals of C_{RES2}. The sum of $V_{\mathrm{SP1}}(T_S/2)$ and $V_{\mathrm{SN1}}(T_S/2)$ is equal to the supply voltage if the PMOS and NMOS transistors have the same $I_{\mathrm{D0}}W/L$ (implying the same g_{M}), so is the sum of $V_{\mathrm{SP2}}(T_S/2)$ and $V_{\mathrm{SN2}}(T_S/2)$.

When C_{RES1} discharges into C_I, we have

$$-C_{\mathrm{RES1}}\frac{dV_{\mathrm{SP1}}(t)}{dt} = I_{\mathrm{D0}}\frac{W}{L}\exp\left(\frac{V_{\mathrm{SP1}}(t) - V_{\mathrm{GP}}(\mathrm{t})}{nU_T}\right). \quad (14)$$

Combining (8), (10)–(12), and (14), and assuming g_{M} of the NMOS and PMOS transistor are the same, V_{GP} at the end of $\Phi 1$ (as a function of the clock frequency) can be derived as

$$\begin{aligned} V_{\mathrm{GP}}(f_S)|_{t=T_s/2} = \frac{C_{\mathrm{RES1}}}{2C_I + C_{\mathrm{RES1}}} nU_T \ln\left(\zeta\frac{1}{2f_S}\right) \\ + \frac{C_{\mathrm{RES1}} + C_I}{2C_I + C_{\mathrm{RES1}}} V_{\mathrm{DD}} \end{aligned} \quad (15)$$

where

$$\zeta = \frac{1+\gamma}{nU_T}\frac{I_{\mathrm{D0}}}{C_{\mathrm{RES1}}}\frac{W}{L} \quad (16)$$

and

$$\gamma = \frac{C_{\mathrm{RES1}}}{2C_I + C_C}. \quad (17)$$

Similarly, during the amplification phase, we have

$$-C_{\mathrm{RES2}}\frac{dV_{\mathrm{SP2}}(t)}{dt} = I_{\mathrm{D0}}\frac{W}{L}\exp\left(\frac{V_{\mathrm{SP2}}(t) - V_{\mathrm{GP}}(T_S/2)}{nU_T}\right). \quad (18)$$

Combining (9), (13), and (18), and according to the small-signal model [Fig. 6(a)], the normalized error E_{settle} of the charge-transfer process can be calculated as follows:

$$E_{\mathrm{settle}} = \left(\frac{t}{\alpha} + 1\right)^{-\frac{C_{\mathrm{RES2}}}{C_O}} \quad (19)$$

where

$$\alpha = \frac{nU_T}{I_{\mathrm{D0}}}\frac{L}{W}C_{\mathrm{RES2}}\exp\left(\frac{V_{\mathrm{GP}}(T_S/2) - V_{\mathrm{DD}}}{nU_T}\right). \quad (20)$$

Therefore, the effective transconductance $g_{\mathrm{M,eff}}$ can be expressed as

$$g_{\mathrm{M,eff}} = \frac{2f_S C_{\mathrm{RES2}}}{\beta}\ln\left(\frac{1}{2\alpha f_S} + 1\right). \quad (21)$$

Combining (15)–(17), (20), and (21), $g_{\mathrm{M,eff}}$ can be written as

$$g_{\mathrm{M,eff}} = \frac{2f_S C_{\mathrm{RES2}}}{\beta}\ln\left(\lambda\left(\frac{1}{f_S}\right)^{\frac{C_I}{2C_I + C_{\mathrm{RES1}}}} + 1\right) \quad (22)$$

where

$$\begin{aligned} \lambda = \frac{I_{\mathrm{D0}}}{2nU_T}\frac{W}{L}\frac{1}{C_{\mathrm{RES2}}}\exp\left(\frac{C_I}{2C_I + C_{\mathrm{RES1}}}\frac{V_{\mathrm{DD}}}{nU_T}\right) \\ \cdot\left(\frac{1+\gamma}{2nU_T}\frac{I_{\mathrm{D0}}}{C_{\mathrm{RES1}}}\frac{W}{L}\right)^{-\frac{C_{\mathrm{RES1}}}{2C_I + C_{\mathrm{RES1}}}}. \end{aligned} \quad (23)$$

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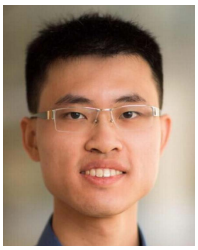

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