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The optical performance of random and periodic textured mono crystalline silicon surfaces for photovoltaic applications

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Abstract. Surface textures that result in high optical yields are crucial for high efficiency photovoltaic (PV) devices. In this work three different texturing approaches are presented that result in smooth concave structures devoid of sharp features. Such features can sustain the crack-free growth of device quality nano- to poly-crystalline materials such as nano-crystalline silicon, perovskites or C(I)GS, facilitating routes towards hybrid multijunction PV devices. A sacrificial implanted poly-c-Si layer is used to develop a random surface texture for the first texturing approach (T_{sac}). The influence of the processing conditions, such as layer thickness, implantation energy, dose and ion type, annealing time and temperature, of the sacrificial layer on the developed surface features is investigated. Additionally, a photolithographically developed honeycomb texture (T_{honey}) is presented. The influence of mask design on the honeycomb features is discussed and a relation is established between the honeycomb period and crack formation in nano-crystalline silicon layers. The reflective properties (spectral reflection, haze in reflection and angular intensity distribution) of these approaches are characterized and compared to a third texturing approach, T_{sp}, the result of chemically smoothened pyramidal <111> features. It was demonstrated that high optical scattering yields can be achieved for both T_{honey} and T_{sp}. Additionally, the performance of a-Si/nc-Si tandem devices processed onto the different textures is compared using both optical device simulations and real device measurements. Simulations demonstrate strong improvements in J_{sc}-sum (≈45%), in reference to a flat surface, and high $V_{oc}*FF$ of over 1 V are demonstrated for T_{sp}.

Keywords: Crystalline silicon texturing / random smooth texture / periodic honeycomb texture / thin film silicon / optical scattering yield

1 Introduction

Surface textures that result in high optical yields are crucial for high efficiency photovoltaic (PV) devices. The technology that dominates the PV market, the mono crystalline-silicon (c-Si) solar cell [1], predominantly of PERC design [2], uses the pyramidal <111> silicon crystal orientation as a front surface texture. This texture is very easy to process through a single chemical etching step, and very efficient at light in-coupling.

A next route for photovoltaics, potentially offering higher yields at low production costs, are multijunction PV devices. In these devices, a crystalline silicon junction is combined with additional junction(s) based on different PV technologies. However, many of these technologies, including nano-crystalline silicon [3–5], perovskites and C(I)GS materials [6–8], contain a crystalline phase which is incompatible with the relatively steep slopes of the conventional <111> crystal orientation. The formation of defective regions, or cracks, in the crystalline phase has been reported to occur in the focal point of perpendicular growth on steep features [9–11]. These defective regions are detrimental to solar cell performance.

Consequently, in this work, three alternative texturing approaches are presented. The aim of these approaches is to produce smooth concave structures devoid of sharp features, that result in high optical scattering yields. These approaches involve the use of a temporary layer, or sacrificial layer, to achieve the desired anisotropic etching of a mono-crystalline silicon surface. For the first texturing approach, presented in Section 3.1 and referred to as T_{sac}, a sacrificial poly-c-Si layer is used to develop a random surface texture. This approach is similar to the one presented in our earlier work [12], for which no optimization was performed on the poly-Si layer processing conditions. In Section 3.2, using a photolithographically developed SiO_2 mask, a periodic texturing approach is presented, resulting in a honeycomb structure (T_{honey}). In Section 3.3, the optical scattering yields of these two

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approaches are compared to a third texturing approach, referred to as T_{sp}, which is the result of consecutive alkaline and acidic etching steps, producing random, smooth and concave structures [12]. Additionally, the performance of multijunction devices processed on the different textured substrates is optically simulated. Finally, in Section 3.4, the performance of the three textures integrated in thin film multijunction PV devices are compared.

2 Experimental details

Three different texturing approaches are presented in this work. 300 µm n-type crystalline silicon wafers from Topsil are used for all three approaches.

T_{sp} is the result of consecutive alkaline and acidic etching steps. A 10 min TMAH etch and rinse was followed by an acidic poly-etch, consisting of 1 part HF (40.5% wt. in H_2O), 6 parts HNO_3 (69.5% wt. in H_2O) and 3 parts H_2O. The influence of these etchings steps on the surface features, as well as the exact solutions and etching conditions, can be found in [12].

T_{sac} is developed using a dedicated sacrificial layer. A flowchart of the processing method is presented in Figure 1. The figure additionally includes SEM images to visualize the state of the substrate along the process. Starting with a c-Si wafer that is stripped of the native oxide layer, an amorphous silicon (a-Si) layer is grown in step 1 using a tempress low pressure chemical vapour deposition tube furnace. In step 2, ion implantation of the a-Si layer is performed with a Varian Implanter. At this point the sacrificial layer is amorphous and the surface is relatively flat. The substrate is then subjected to a high temperature thermal anneal in an N_2 atmosphere in step 3. At this point, the surface and cross-section appear largely unchanged, but the Raman plots demonstrate that the sacrificial layer is now poly-crystalline. Finally, in step 4, the sacrificial layer is etched in a poly-etch solution. After etching for 4.5 min, just over half of the poly-Si sacrificial layer is etched and the crater-like surface features are present. When the sacrificial layer is fully etched, the silicon surface is exposed with craters up to 600 nm in diameter.

T_{honey}, the honeycomb textures, are obtained using an approach similar to [13]. A flowchart of this approach is presented in Figure 2. In step 1, a 300 nm SiO_2 layer is grown on the silicon wafer using a 1100 °C wet oxidation process. After SiO_2 growth the wafer is consecutively coated with an adhesive, hexamethyl disilizane, using nitrogen as a carrier gas. In step 2, spin coating is used to apply a 1.4 µm Shipley SPR3012 positive photoresist. An annealing step is then performed, at 95 °C for 90 s, followed by lithographic exposure during step 3, at a 140 $mJ \cdot cm^{-2}$, and another anneal for 90 s at 115 °C. An optical microscope image of the mask used for exposure is indicated by A. In this image, the red honeycomb structure is added to indicate the eventual formation in reference to the position of the holes. Step 4 is the development phase, during which the areas of the photoresist that were irradiated are removed. This involves coating the wafer with the developer, followed by an anneal at 100 °C for 90 s. During step 5 the pattern is transferred from the mask to the SiO_2 layer through a 4 min dip in a bath of commercially available buffered oxide etch (7:1). Afterwards, the acid is removed by rinsing with DI water and the remaining photoresist is removed in a bath of acetone at 40 °C. In step 6 the wafer is exposed to a poly-etch to etch the silicon wafer. The etching time should be optimized such that the etched hexagonal areas underneath the holes come into contact with one another. The evolution of the surface as a function of etching time is presented through visuals C–E. If the SiO_2 is not fully etched during this step 5, the poly-etch will first have to etch through the remaining SiO_2, resulting in longer required etching times for honeycomb completion and the SiO_2 triangles that are observed in visual B. Finally, in step 7, the remaining SiO_2 mask is removed using another HF etching step.

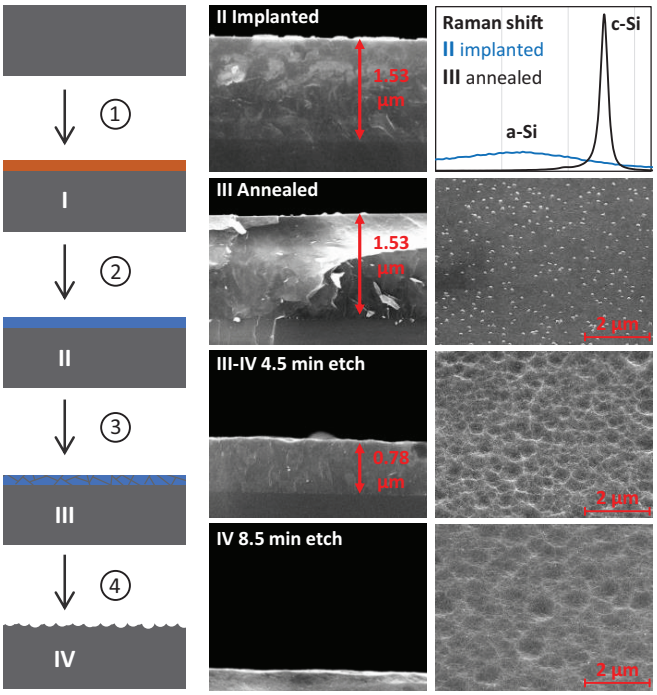

Fig. 1. Flowchart of the sacrificial-layer texturing approach (T_{sac}). A schematic representation of the sacrificial layer and silicon surface at each phase (phase I–IV) is presented on the left. Processing steps 1–4 are referenced in the text. A cross-sectional SEM image of the silicon surface and sacrificial layer at phase II is presented in the centre, following implantation in an approximately 1.5 µm a-Si layer. Raman spectroscopy measurements of the sacrificial layer at phase II and phase III are presented in the top right plot, where the peak referred to as c-Si is positioned at 520 cm^{-1} and the peak referred to a-Si at around 480 cm^{-1}. SEM images of the cross-section and surface of the substrates at a 40° tilt, at phase III and IV and at some point between these phases are presented as well.

A schematic representation of the solar cell device architecture is shown in Figure 3. For this research, the Si wafer is not part of the photoactive stack but exclusively acts as a textured substrate. For the solar cell depositions, a 300 nm SiO_2 layer was processed first, using a 1100 °C wet oxidation process, to electrically isolate the textured wafer from the photo-active stack. Next, a 500 nm silver layer was

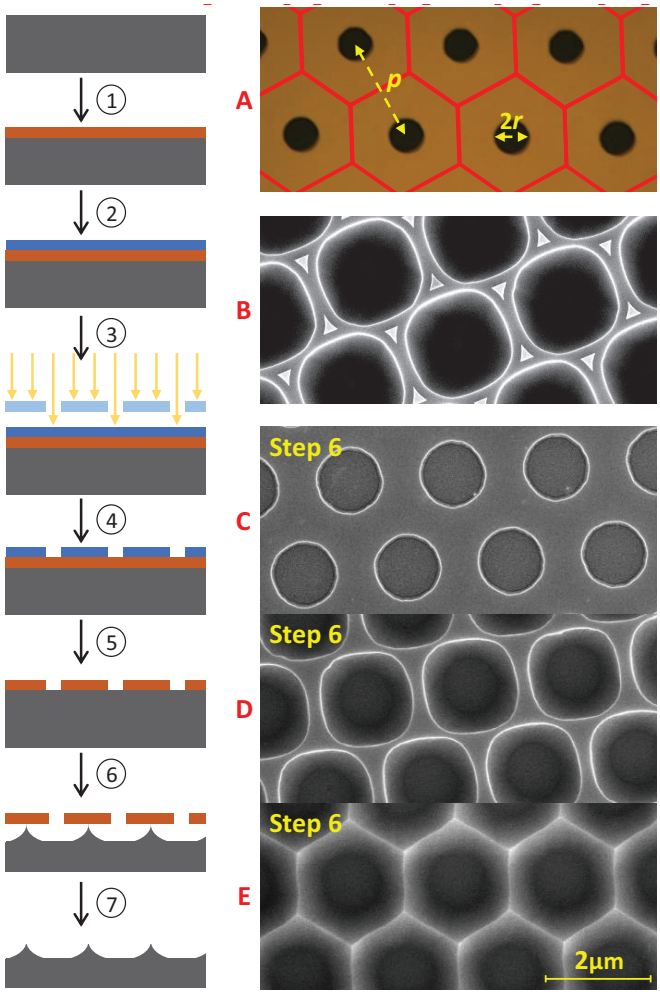

Fig. 2. Flowchart of the honeycomb texturing approach. A schematic representation of the silicon surface and additional layers phase is presented on the left. Processing steps 1–7 are referenced in the text. Visual A. is optical microscope image of the mask used for exposure. Red lines are added to indicate the honeycomb structure resulting from the used mask. Visual B–E are SEM images at 0 degrees tilt, Visual B indicates the effect of under-etching at step 4. Visuals C–E indicate the effect of etching time during step 6.

evaporated on the SiO_2 layer, followed by a 90 nm sputtered aluminum doped zinc-oxide (AZO) layer. The photoactive stack is processed in n-i-p substrate configuration, using plasma enhanced chemical vapour deposition (PECVD). The deposition conditions of the intrinsic and n-type (n-) PECVD processed layers can be found in [14]. For the p-type (p-)layer a p- nano-crystalline (nc-) hydrogenated (:H) siliconoxide (SiO_X) layer layer is used, with a graded dopant profile. For the initial 12 nm of SiO_X growth, the diborane gas flow rate is set at 10 sccm 0.02% B_2H_6 in H_2, which is increased to 50 sccm for the final 4 nm. The other p-layer deposition conditions are similar to those reported in [15]. Following deposition of the photoactive stack, a 70 nm indium-doped tin-oxide (ITO) is sputtered and a 500 nm Al metal front grid is evaporated.

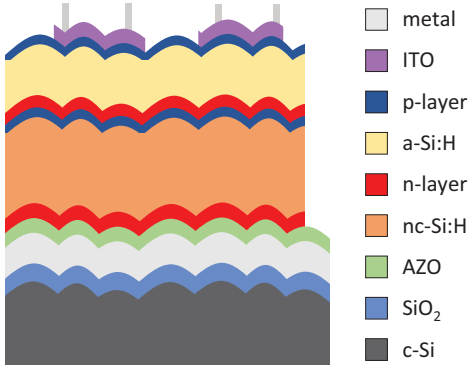

Fig. 3. Schematic structure of the solar cells. Note that Ag is used as a metal back contact, while Al is used for the metal front contact.

Details regarding the used scanning electron microscope (SEM) and atomic force microscope (AFM) are reported in [12]. The mean pore diameter D_{pore} and other metrics for the surface features were extracted using the NanoScope Analysis software from Bruker. A Lambda 950 Spectrophotometer was used to determine the angular intensity distribution (AID) of the reflectance. A Lambda 1050 Spectrophotometer was used for spectral reflectance and Haze measurements. The haze in reflection (H_R) is defined as the ratio of diffuse to the total reflection:

$$H_R(\lambda) = \frac{R_{dif}(\lambda)}{R_{tot}(\lambda)}. \quad (1)$$

More information about the haze and AID measurements can be found in [16–18].

Raman spectroscopy, using an inVia confocal Raman microscope with a laser operating at a wavelength of 514 nm, was performed to determine the crystallinity of a few selected layers. The method for obtaining the crystallinity is reported elsewhere [19]. The external quantum efficiency (EQE) was obtained using an in-house EQE setup. The EQE of an individual junction in a multijunction device was obtained by saturating the other junction(s) with bias light. By weighing the EQE spectra with the $AM1.5_G$ solar spectrum, the short-circuit current density (J_{sc}) of the individual junctions was obtained. EQE measurements are performed without bias voltage, unless mentioned otherwise. The J–V curves of the devices are measured at 25 °C using an $AM1.5_G$ solar simulator. The open circuit voltage (V_{oc}), fill factor (FF), series resistance (R_s) and shunt resistance (R_{sh}) are obtained from these J–V curves. On each sample, 24 individual 16 mm^2 cells are processed. All 24 cells are measured and the results presented in this work are the average of the five best cells. More detailed descriptions of these measurements can be found in [14].

3 Results and discussion

3.1 Random texturing using a sacrificial layer

A random surface texture can be developed using a heterogeneous sacrificial layer. The purpose of the heterogeneity is to achieve anisotropic etching of

the sacrificial layer. As a result of this anisotropic etching, the etchant will reach the silicon surface, having locally etched through the sacrificial layer, at different points in time, spatially. Consequently, when the sacrificial layer is fully etched over the entire sample, the silicon surface will have been exposed to the etchant for a non-uniform period of time, resulting in a random surface texture. The heterogeneity of the sacrificial layer can be the result of factors like material stoichiometry, different material phases or pinholes. In this section a sacrificial poly-crystalline silicon film is used, where the porous grain boundaries in reference to the dense c-Si grains result in the desired anisotropic etching behaviour. The T_{sac} texturing approach has been presented before in our earlier work [12], where it was concluded that the surface features were too small to yield the desired optical behaviour. In this section an optimisation of the sacrificial layer is performed to achieve larger surface features, which would result in lower reflectance and better wide-angle scattering.

All four steps presented in Figure 1 can influence the features formed on the c-Si surface. In earlier work it was observed that the etching time of step 4 should be chosen such that sacrificial layer has just been fully etched [12]. Prolonged exposure to the etchant results in smoothening of the craters and a decrease of surface roughness. In this section, the conditions used for steps 1–3 are characterized. These include the a-Si sacrificial layer thickness (d_{asi}) developed in step 1, the implantation conditions used in step 2, which include the implantation dose (δ_{imp}), implantation energy (E_{imp}) and ion type used for implantation, and finally the annealing time and temperature in step 3. Of these conditions, only the annealing time and temperature did not significantly affect the size of the craters. For the crater size, the mean pore diameter (D_{pore}) is used as a metric, as obtained from AFM measurements. For a series of samples annealed at both 950 °C and 1050 °C, for 15–30–60–90 min, the D_{pore} was observed to increase slightly from 370–380 nm to 385–395 nm when the annealing time was increased from 15 min to 30 min. A further increase of annealing time, for either temperature, did not result in a significant change of D_{pore}. The discussion will therefore focus on the influence of d_{asi} and conditions used for ion implantation. All following samples are annealed for 20 min at 1050°.

SEM images and D_{pore} of the silicon surfaces as a function of E_{imp} and d_{asi} are shown in Figure 4. Additionally, in the top left of the figure, a sample is included for which step 2 of Figure 1 was omitted, so where no implantation occurred. The SEM image shows that implantation is essential for the formation of large surface features. In Figure 5, the influence of δ_{imp} is shown in some more detail. For the P-implanted samples shown in the inset, D_{pore} is observed to increase continuously with increasing δ_{imp}. Raman measurements performed on an additional set of Ar-implanted samples with varying δ_{imp} indicate a direct relation between δ_{imp} and the Raman signature of the sacrificial layer. The peak positioned at a Raman shift of ≈500 cm^{-1} is observed to increase in reference to the peak positioned at a shift of 520 cm^{-1}. The latter peak corresponds the vibration of bulk mono-c-Si material. The peak at 500 cm^{-1} is associated to a

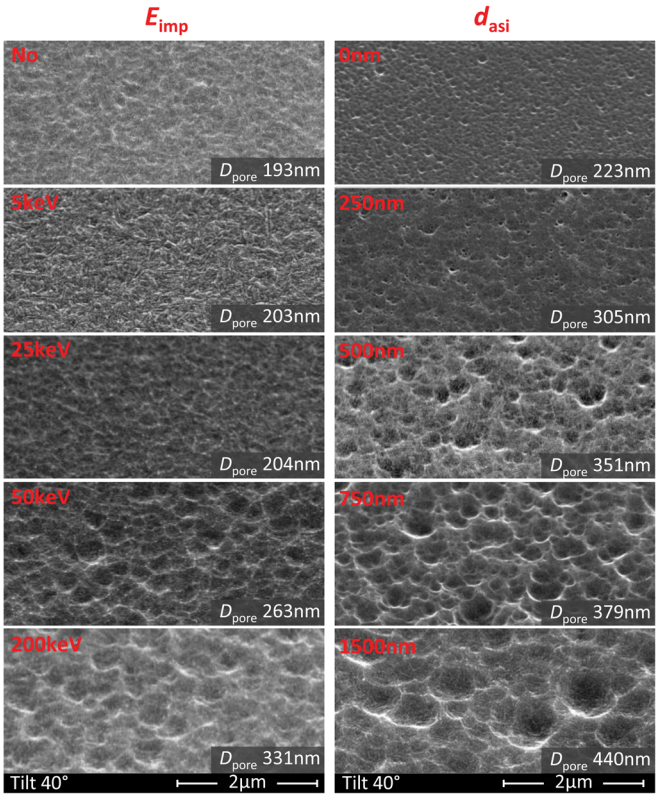

Fig. 4. SEM images and D_{pore} values of two argon implanted series of samples. Samples on the left are processed with increasing E_{imp} and $d_{asi} = 1\,\mu$m. Samples on the right are processed with increasing d_{asi} and $E_{imp} = 250$ keV. All samples implanted with $\delta_{imp} = 1\mathrm{e}16$ cm^{-2}. No implantation occurred for the top-left sample, while the implantation was performed without amorphous silicon layer for the top-right sample.

poly-crystalline phase [20,21], with the Raman shift in reference to mono-c-Si resulting from strain from the crystalline grains. Similar Raman shifts are observed in nano-c-Si and micro-c-Si, where crystalline grains are embedded in an amorphous Si phase [22]. In these materials the exact shift was demonstrated to be a function of the crystalline grain size [20]. The increase of the 500 cm^{-1} peak in reference to the 520 cm^{-1} peak, with increasing δ_{imp}, indicates an increase of the fraction of strained c-Si in reference to the mono-c-Si phase. The relation between the observed change in the Raman signature, the size of the crystalline grains and D_{pore} is not fully clear, as no grain size measurements are performed in this work. The increase of the 500 cm^{-1} peak with increasing δ_{imp} could suggest either (i) a decrease of the crystalline grain size, as the fraction of strained Si, near the ground boundaries, is increased with respect to the bulk Si fraction. In this scenario, the larger D_{pore} for higher dose would be a result of the presence of more ground boundaries in reference to a more mono-c-Si sacrificial layer, increasing anisoptropic etching behaviour. Or, (ii) an increase of the crystalline grain size as the overall strain increases when larger grains develop and their expansion becomes constrained by neighbouring grains. In this scenario, the presence of fewer grain boundaries would result in the observed increase of D_{pore}.

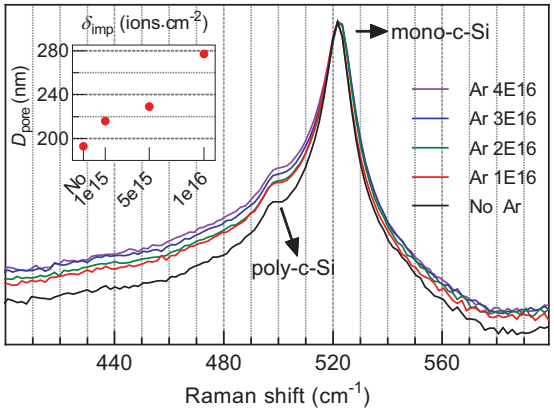

Fig. 5. Raman measurements of Ar implanted poly-Si sacrificial layers at phase 3 (post-anneal) at different δ_{imp}. Samples are processed with $d_{asi} = 1.5$ µm and $E_{imp} = 250$ keV. Raman measurements are normalized using the highest count and plotted on a semi-logarithmic scale. The inset show D_{pore} as a function of δ_{imp} for P implanted sacrificial layers, with $E_{imp} = 5$ keV and $d_{asi} = 1$ µm.

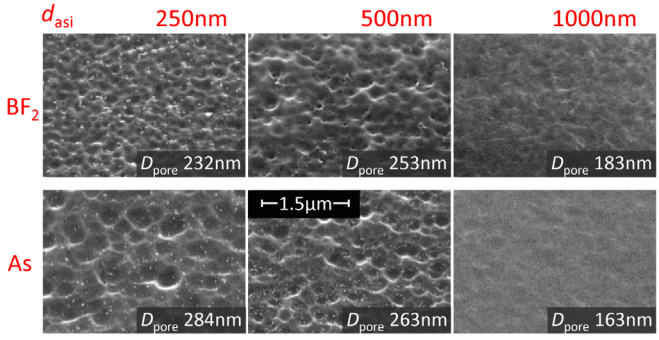

Fig. 6. SEM images and D_{pore} values of sacrificial layers implanted with BF_2 and As, with d_{asi} varied between 250–500–1000 nm. Implantation occurred at $\delta_{imp} = 1e16$ cm^{-2} and $E_{imp} = 250$ keV.

The latter mechanism would be more in line with earlier reports, where an increase of the average grain size in poly-Si layers with increased δ_{imp} was observed [23–25]. Reportedly, the Si self-diffusion coefficient during anneal can be improved through impurity doping, which facilitates the merger of small grains during anneal and consequently results in an increase of the average grain size [24,25]. Regardless of the mechanisms, it is clear that D_{pore} scales with the crystalline phase characteristics of the sacrificial layer and that the development of the grain size is influenced by the presence and dose of implanted ions.

Grain formation is not exclusively affected by δ_{imp}. Figure 4 shows that the crater size increases with both E_{imp} and d_{asi}, for the selected conditions. For $d_{asi} = 1$ µm, increasing E_{imp} of the Ar implanted samples from 5 keV to 200 keV results in an increase of D_{pore} from about 200 nm to over 330 nm. Similarly, increasing d_{asi} from 250 nm to 1500 nm, for an Ar implantation energy of 250 keV, results in an increase of D_{pore} from about 300 nm to 440 nm. Figure 4 shows that: (i) if no implantation takes place, no craters are formed. (ii) The surface of a no-implantation sample strongly resembles the surface of a low energetic implantation sample and (iii) if no a-Si layer is used for the implantation, craters are still formed, but with a very small D_{pore}. This is not unexpected, since the Raman measurements in Figure 1 show that the energetic ion bombardment during implantation amorphizes a thin top region of the silicon wafer, which will recrystallize to form a poly-Si layer upon annealing.

These combined observations lead to suspect that the development of the grain size, for a given δ_{imp}, is the result of an interplay between d_{asi} and E_{imp}. The profile of implanted ions can be approximated by a gaussian distribution [26,27]. Note that the ions will no longer have a ionic nature following implantation. With increasing E_{imp}, the width of the gaussian widens and the peak is positioned further away from the surface. This means that with a low E_{imp}, the ions will be predominantly implanted near the surface of the a-Si layer and will not affect grain formation, upon thermal anneal, close to the silicon wafer surface. With higher E_{imp}, more energetic implantation occurs and the ions are implanted deeper into the amorphous silicon layer. Consequently, for the 1000 nm Ar implanted a-Si layer of Figure 4, a larger fraction of ions will be positioned close to the silicon surface, facilitating grain formation near the silicon wafer surface. Similarly, for the 250 keV Ar implanted a-Si layers, D_{pore} can be observed to increase with d_{asi}. Experiments with much thicker d_{asi} of 3 µm and 4 µm again showed a strong decrease of D_{pore} and RMS roughness.

The implantation profile is not exclusively a function of E_{imp} however. For similar E_{imp}, larger, heavier ions are implanted closer to the surface. This effect is shown in Figure 6, Where it can be observed that for As, which has a larger ion size than BF_2, the largest D_{pore} are achieved in thinner layers in reference to BF_2, for a given δ_{imp} and E_{imp}. This interplay between d_{asi}, E_{imp} and the used ion type is schematically shown in Figure 7. This schematic visualizes how the grain size near the silicon surface will vary as a function of these parameters. This means that for a given ion type, E_{imp} and d_{asi} should be optimized in tandem for the development of large crystal grains. Note that for the purpose of this visual (Fig. 7) it is assumed that ion implantation leads to the formation of larger crystals. As mentioned earlier, from the results presented in this work it cannot be concluded whether the increased anisotropic etching behaviour with ion implantation is the result of the formation of much smaller or much larger grains in reference un-implanted a-Si sacrificial layer that was subject to an anneal-induced crystallisation.

In addition to the interplay between these three parameters, Figures 6 and 7 indicate that, if E_{imp} and ion type are chosen such that ions are implant close to the c-Si surface, the largest D_{pore} are achieved for relatively thick a-Si layers. For similar δ_{imp}, the largest D_{pore} of the Ar implanted sacrificial layers is 440 nm, while that of the BF_2 and As implanted sacrificial layers is 253 nm and 284 nm, respectively. This observation seems to suggest that the

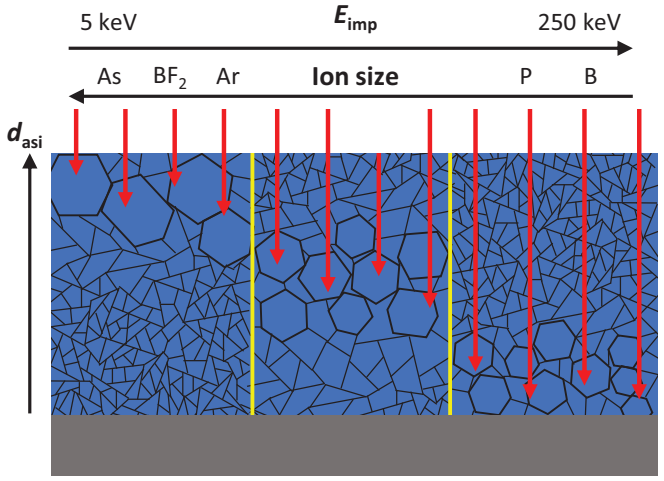

Fig. 7. Simplified schematic representation of the grain size development as a function of the ion distribution (red arrows) in reference to the silicon surface (grey rectangle), as a function of d_{asi}, the ion type and E_{imp}.

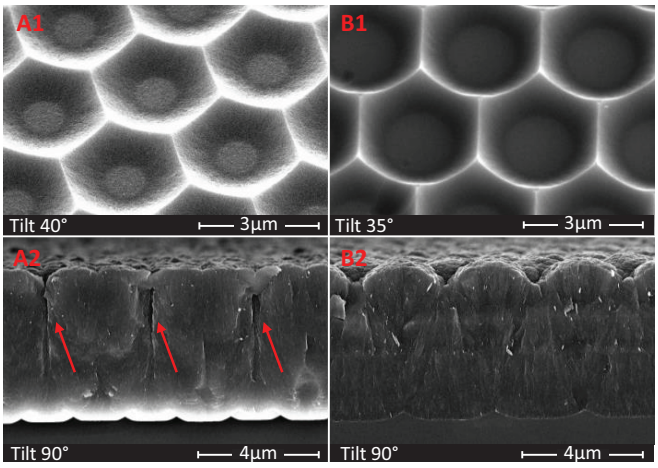

Fig. 8. SEM images of honeycomb structures. **A1-2** have a honeycomb periodicity of 2 µm, while **B1-2** have a periodicity of 3 µm. **A1** and **B1** are surface images at 35–40° tilt. **A2-B2** are cross-sectional images of a c-Si honeycomb surface structure on top of which a 5 µm nc-Si layer is grown. Red arrows in image **A2** indicate cracks formed in the nc-Si phase as a result of the honeycomb surface texture.

formation of larger grains is impeded in thin films, or conversely that thicker films facilitate the formation of larger grains.

3.2 Periodic honeycomb texturing

A flowchart of all steps involved in developing the periodic honeycomb features is presented in Section 2. When all steps are optimized, the developed honeycomb texture is determined by the mask used during step 3. The formed honeycomb structure is a function of two parameters, which are the period (p), defined as the distance between the centre of two hexagons, and the height difference (h) between the corner of the hexagon and the centre. As an isotropic etchant is used, the texture depth is equal to the distance between edge of a hole in the mask and nearest corner of the hexagon. Consequently, h will be equal to the distance from the centre of the hexagon to the corner, which is equal to $\frac{p}{\sqrt{3}}$, minus the radius (r) of the hole, or:

$$r = \frac{p}{\sqrt{3}} - h. \tag{2}$$

The ratio of h over p is referred to as the aspect ratio. For use in thin film silicon solar cells, the aspect ratio of the honeycomb texture should be around 0.25 [28]. Moreover, it was concluded in earlier work that maximum photocurrents are realized in nano-crystalline silicon (nc-Si) solar cells when p is about 0.5 µm larger than the film thickness [29]. Taking into account this desired aspect ratio of 0.25 and $p = 3$ µm, a mask is used in this work with $r \approx 1$ µm, in accordance with equation (2). If the texture is used in combination with a different PV absorber material, with a different bandgap energy and absorption coefficient, different reflective behaviour might be preferred. In order to characterise the change in optical behaviour as a function of p, a second mask is used with $r = 1$ µm and $p = 2$ µm. The resulting surface textures are presented in Figure 8.

Finally, in addition to improving the optical behaviour of the silicon surface, the honeycomb texture should facilitate the growth of crack-free nano- to poly-crystalline. The growth of a crystalline phase on sharp surface features can result in the formation of cracks [10,11], which is detrimental to solar cell performance [3,9]. It has been observed that cracks tend to form in the focal point of perpendicular growth on steep features. For the honeycombs features, this focal point is a function of both p and r. SEMS **A2** and **B2** in Figure 8 demonstrate the crack formation as a function of p at different positions along the nc-Si growth. The texture with $p = 3$ µm can facilitate the growth of a 5 µm crack free nc-Si film, while the texture with $p = 2$ µm can only facilitate very thin nc-Si films before significant crack formation occurs. For that reason, the devices presented in Section 3.4 are exclusively processed on the larger honeycomb textures with $p = 3$ µm.

3.3 Optical performance of surface textures

To determine the optical behaviour of the different surface textures, the spectral reflectance (R) and haze in reflection (H_R), as well as the angular intensity distribution (AID) are measured. This comparison is performed between the texture using a sacrificial layer (T_{sac}) developed in Section 3.1, the honeycomb textured (T_{honey}) developed in Section 3.2 and the texture with chemically smoothened pyramidal features (T_{sp}) developed in [12]. SEM images for each texture are shown in Figure 9.

The reflective behaviour of the different bare silicon surfaces is shown in Figure 10. R provides information on the light in-coupling effectiveness of the textured surface.

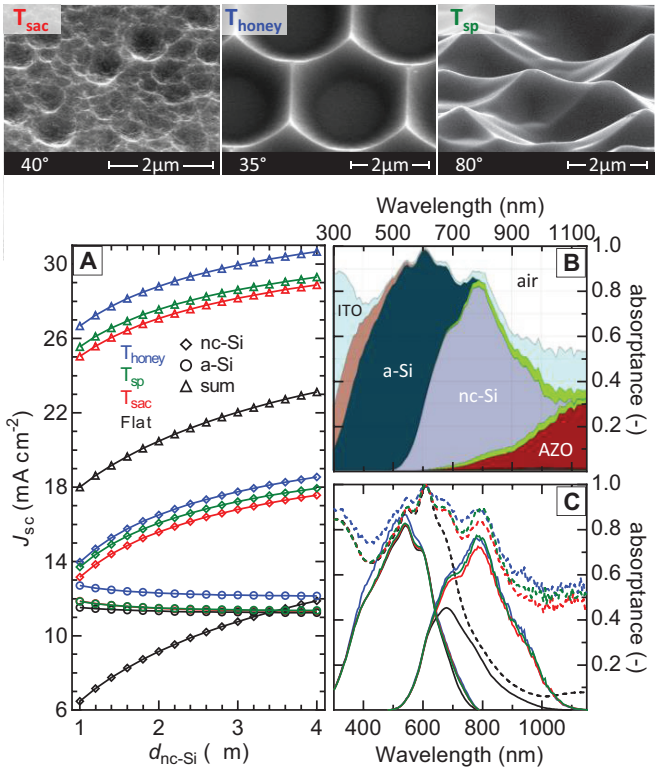

Fig. 9. Simulated performance of a-Si/nc-Si tandem devices on flat substrates and substrates with T_{sac} (red), T_{sp} (green) and T_{honey} (blue) textures. SEM images (top) show surface morphology T_{sac}, T_{sp} and T_{honey}. A) shows the J_{sc} of the a-Si junction, nc-Si junction and the sum of both junctions for the different substrate types, as a function of nc-Si absorber thickness (d_{nc-Si}). B) shows the spectral absorptance in each of the layers of the tandem device on T_{honey}. In addition to the layers indicated in the plot (air, ITO, a-Si, nc-Si, AZO) absorptance in the p-nc-SiO$_X$:H layer (brown), n-nc-SiO$_X$:H layers (green) and Ag layer (dark grey, close to bottom horizontal axis) are indicated. C) shows the a-Si and nc-Si absorptance curves and 1-R curves for the different substrate types, for tandem device with $d_{a-Si} = 300$ nm and $d_{nc-Si} = 1.2$ µm.

Light in-coupling is predominantly related to the probability of multiple reflection events. The probability of such an event taking place decreases when the mean slope of surface features decreases. A decrease of the mean slope with increasing etching time is the cause of the decrease in R over the entire spectral range observed for T_{sp}, which is in line with [12]. The low probability of multiple reflection events for T_{sp}, especially for 9.5–11 min etching time, result in R-values that are not much different from that of a flat surface, as can be observed in the T_{sac} R spectra. It should be noted that the change in reflectance can also arise from a change of the angle of incidence, as the mean slope of the surface features changes. However, this angle of incidence related change in reflection, following from the Fresnel equations, is minimal in the $\leq 45°$ mean slope range, and would be opposite in trend.

The use of the T_{sac} approach results in only a marginal R decrease, by about 0–5%. While the influence on light in-coupling is minimal, application of T_{sp} or T_{sac} changes the scattering behaviour significantly in reference to a flat surface. The H_R of T_{sac} is observed to increase from a few percent to 5–60% with increasing d_{asi}, depending on the spectral range. Nevertheless, the small R-decrease and $H_R \leq 30\%$ for wavelengths (λ) > 500 nm indicate that the T_{sac} approach might have limited effectiveness for light in coupling and/or scattering applications, presumably as a result of the limited depth of the formed craters. The relatively poor scattering nature is confirmed by the *AID* measurements of the $d_{asi} = 1500$nm sample. Note that the slope distribution, height profile and additional surface parameters of T_{sac}, T_{sp} and T_{honey} are available in the supplementary information.

On the other hand, the H_R of T_{sp} is close to 100% over the entire spectral range for all etching times, indicating that no specular component remains to the reflection. While the R and H_R measurements show a minimal etching time dependence, the *AID* shows a subtle yet significant change in reflective behaviour. At 6.5mins the reflected intensity in the $\theta_{det} = 10$–$65°$ range is roughly equally distributed. However, when the etching time is increased to 11 min, the mean slope is decreased to approximately 30° and light in the visible range ($\lambda = 400$–700 nm) is predominantly scattered into wide 60°.

The application of T_{honey} appears more effective at light in-coupling than T_{sp} and T_{sac}, especially at smaller p where width-to-depth ratios are larger and slopes are steeper. As with T_{sp}, the reflectance of T_{honey} increases with etching time. For $p = 3$ µm, at an etch time of 8 min, the different holes have barely reached one another (Fig. 2 between D and E) and the slopes are relatively steep, resulting in effective light in-coupling. With increasing etching time, steep features are smoothened and reflection increases. H_R of the T_{honey} is in the 88–100% range, owing to the full surface coverage of concave features. The periodic nature of the T_{honey} is also apparent in the reflective behaviour. Constructive and destructive interference effects can be observed over the H_R and R spectral range. The interference behaviour, can clearly be observed in the *AID* spectra. On the bottom right the *AID* spectrum normalized in the $\theta_{det} = 30$–$100°$ range of the $p = 3$ µm (12 min) sample is presented. The maximum reflection, so the peak of constructive interference, is observed to shift to larger θ_{det} with increasing λ. Additionally, an increase of $\Delta\theta_{det}$ between peaks of constructive interference can be observed with increasing λ, so that at larger wavelengths fewer interference peaks are present. The left figure of T_{honey} *AID* shows however that the largest fraction of the reflected light still occurs in the normal direction. This is likely a result of the relatively flat areas at the bottom of the honeycomb structure positioned underneath the hole in the SiO_2 mask.

Next we compare the light management effectiveness of the various textured substrates when integrated in a PV device, using the GenPro4 optical model [30]. GenPro4 gives the spectral reflectance and absorptance of each layer in a PV device and allows for the use of AFM scans to simulate the texture. Using the multijunction a-Si/nc-Si tandem device schematically shown in Figure 3 as a model, and various AFM scans, current generation in the different absorbers as a function of surface texture was simulated. Figure 9 shows the J_{sc} generated in a 250 nm a-Si absorber and nc-Si absorber,

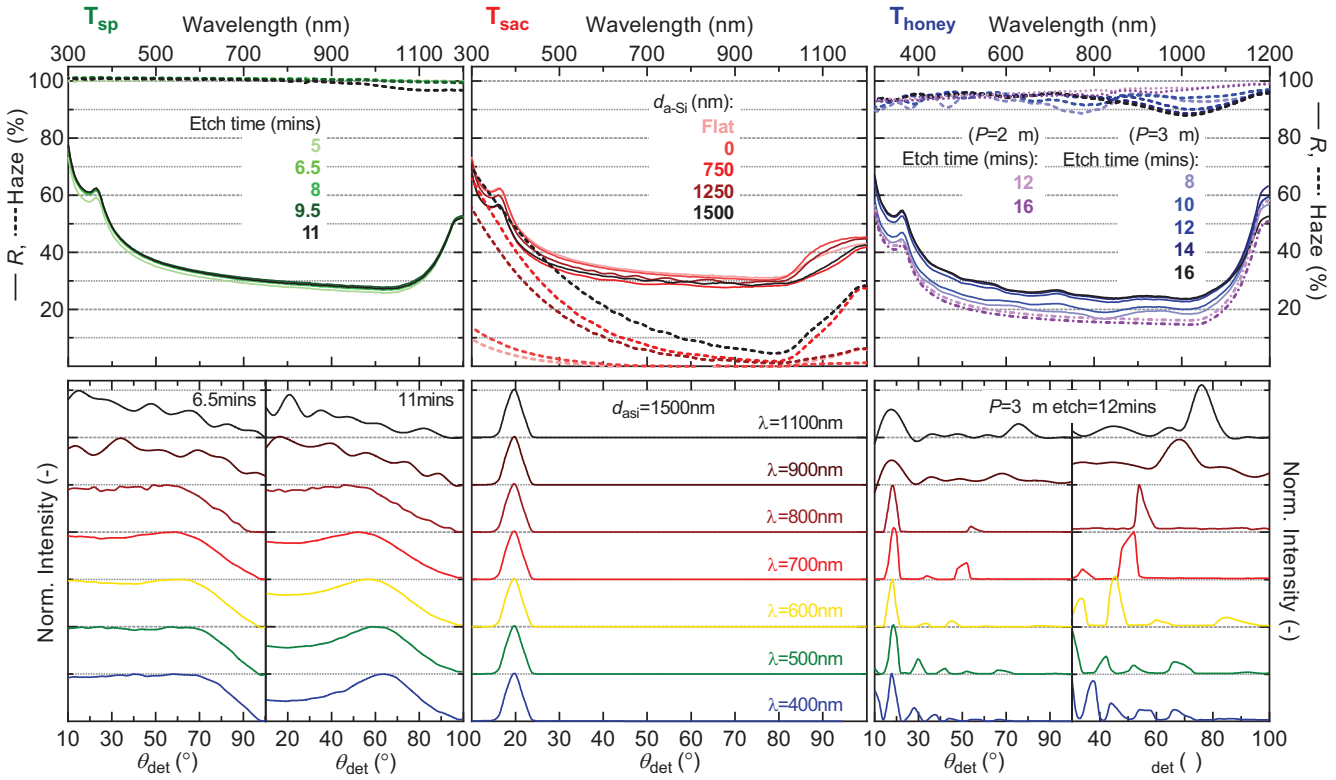

Fig. 10. Reflective behaviour of T_{sp} (green, left), T_{sac} (red, centre) and T_{honey} (blue, right). Presented are R (top, solid lines) and H_R (top, dashed lines) and AID (bottom). AID measurements show normalized intensity (normalized to maximum value) as a function of detector angle (θ_{det}) in reference to the incident light, with the sample positioned at a 10 degree angle, for different wavelengths (λ). For T_{sp}, R and H_R are shown as a function of etching time and AID measurements are shown for samples etched at 6.5 mins (left) and 11 mins (right). For T_{sac}, R and H_R are shown as a function of d_{asi}. R and H_R of a flat, polished wafer is included as reference. AID measurements are shown for the sample with $d_{asi} = 1500$ nm. For T_{honey}, R and H_R are shown as a function of etching time (step 4) for honeycombs with p = 2 μm (R = dashed/dotted, H_R = dotted) and p = 3 μm (R = solid, H_R = dashed). AID measurements are shown for samples with p = 3 μm etched for 12 mins, with right image showing AID normalized to max value in $\theta_{det} = 30°$–$90°$ range.

with a thickness varied from 1 to 4 μm, for a device with flat interfaces as well as T_{sp} (6.5 and 11 min), T_{sac} (d_{asi} = 1500 nm), and T_{honey} (12 min) textured interfaces.

Since the J_{sc}-mismatch between subcells various for the different surface textures, the optical effectiveness of the surface features on the device performance can be evaluated through the sum of the J_{sc} of the two subcells. The figure demonstrates that the J_{sc}-sum is strongly increased for all three textured surfaces in reference to a flat surface. The J_{sc} difference mainly originates from the nc-Si bottom junction, as the a-Si-J_{sc} values are not much different. This is not unexpected since (i) a relatively thick a-Si absorber thickness (d_{aSi}) of 250 nm is used, (ii) the absorption probability of light with $\lambda = 300$–600 nm in the direct-bandgap a-Si junction is relatively high and (iii) the light in-coupling effectiveness between the different textures does not differ much, as shown in Figure 10. T_{honey} achieves better light in-coupling than the other textures, as indicated by the lower R-values in Figure 10, which is reflected in the higher J_{sc} values of the a-Si junction.

The main difference is achieved in the nc-Si junction, which has a lower absorption probability and therefore benefits more from the increased optical pathlengths, and the potential for total internal reflection events, achieved with textures that scatter light effectively. This is demonstrated in Figure 9C, where a strong increases in the $\lambda = 700$–1100 nm region can be observed for the different textures in reference to the flat surface, for which the optical path length is just two times d_{ncSi} before light is lost in air (1-R). The effect of the increased scattering efficiency, as represented by H_R, of T_{honey} and T_{sp} in reference to T_{sac} is mainly observed in the $\lambda = 700$–950 nm region.

According to the simulations, J_{sc}-sum of T_{sp} and T_{sac}, in reference to a flat surface, is increased by about 7–7.5 mA cm^{-2} and that of T_{honey} by about 8.5 mA $\cdot$ cm^{-2}, which represents an increase of over 45%. No current matched situations are presented in Figure 9A. Additional simulations show that current matching can be achieved at $d_{aSi} = 310$ nm and $d_{ncSi} = 1$ μm for both T_{sac} (J_{sc}-match = 12.61 mA $\cdot$ cm^{-2}) and T_{honey} (J_{sc}-match = 13.41 mA $\cdot$ cm^{-2}). For T_{sp}, achieving current matching with $d_{ncSi} = 1$ μm requires an a-Si absorber with $d_{aSi} = 350$ nm (J_{sc}-match = 12.98 mA $\cdot$ cm^{-2}).

Additionally, Figure 9B shows that the difference between 1-R and the summed absorptance in the a-Si and nc-Si absorbers is mainly due to parasitic absorption in the TCOs positioned at the front (ITO) and back (AZO) of the device and some minor absorption in the p- and n-doped SiO_X:H layers.

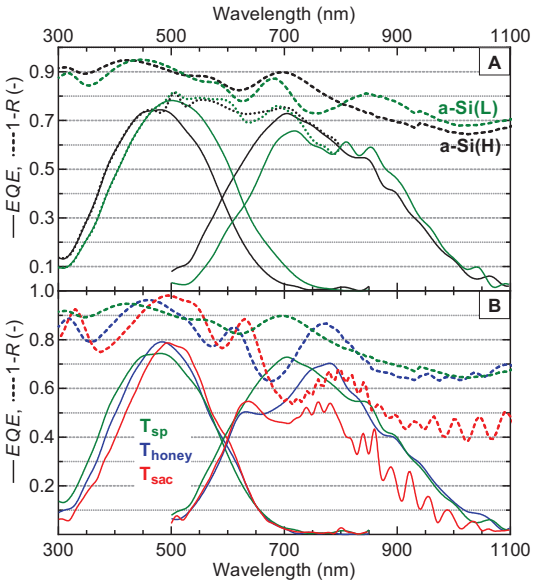

Fig. 11. *EQE* and 1-R spectra as a function of wavelength. **A** shows the spectra of tandem devices with a-Si(H) and a-Si(L) absorber on T_{sp} (6.5 mins) textured substrate, with dotted line indicating *EQE*-sum. **B** shows the spectra of tandem devices with a-Si(H) absorbers on T_{sac} (6.5 mins), T_{sac} (12 mins) and T_{sac} (d_{asi}=1500 nm) textured substrates.

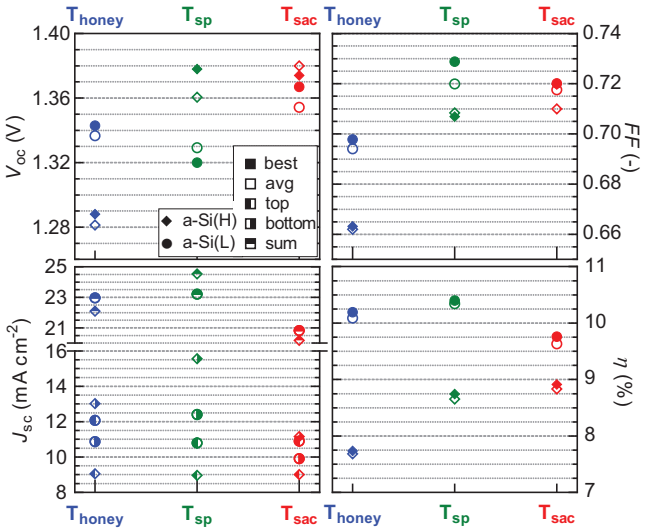

Fig. 12. Solar cell characteristics of a-Si/nc-Si tandem devices as a function of substrate texture. Symbols indicate the characteristics of the best (closed) and average of best 5 (open) cells on a substrate, based on conversion efficiency. Symbol type indicates results of devices with high-E_G a-Si (diamond) and low-E_G a-Si (circle). J_{sc} is obtained from *EQE*-measurements and is presented separately for the bottom nc-Si junction, top a-Si junction and sum of both junctions.

3.4 Influence of textures on solar cell performance

Finally, the performance of n-i-p a-Si/nc-Si tandem devices processed on silicon wafers that are textured using T_{sac} (6.5 min), T_{sac} (12 min) and T_{sac} (d_{asi} = 1500 nm) is compared. The device structure is schematically shown in Figure 3. Two sets of devices are processed; one with a high bandgap energy (E_G) a-Si absorber (a-Si(H)) with $E_{Ga-Si(H)}$≈1.7 eV, developed in [31], and the other with a low-E_G a-Si absorber (a-Si(L)), with $E_{Ga-Si(L)}$≈1.6 eV. Deposition conditions for both can be found in [32]. The difference between the a-Si(L) and a-Si(H) absorber can be observed in Figure 11A, where the absorption onset is observably shifted from about λ = 730 to λ = 780 nm. As a consequence, use of the a-Si(H) absorber results in increased absorption in the nc-Si absorber.

From the *J*–*V* characteristics of the tandem devices presented in Figure 12, a number of observations can be made.

– The highest J_{sc}-sum is achieved with T_{sp}, which is unlike in the optical simulations presented in the preceding section. The J_{sc}-sum is especially high for the a-Si(H) samples, while for the a-Si(L) samples it is not much different from the T_{honey}. The high J_{sc}-sum of T_{sp} is mainly a result of generation in the bottom junction, which is considerably higher in reference to T_{sac} and T_{honey}. The *EQE*-curve in Figure 11B shows that is mostly due to a large interference fringe with high reflectance for T_{honey} in the λ = 600–800 nm range. The presence of the interference peak likely results from the bottom of the honeycomb, which appears optically flat, as indicated by the relatively large specular component in the *AID* measurements of T_{honey}. A spectral shift of the interference fringes has been demonstrated, for instance, as a function of the thickness of a *n*-nc-SiO$_X$:H layers positioned between two junctions [5]. The difference between simulated and experimental results is therefore likely due to a difference in layer thicknesses.
– The J_{sc}-sum of T_{sac} is 2–4 mA · cm^{-2} lower than T_{sp} and T_{honey} due to the relatively low roughness of the surface. The interference fringes that can be expected from an optically flat surface with a large specular component to the reflection (no anti-reflection coating, refractive index grading and/or nanoscale-roughness at the front of the devices), and with thin layers in the 10–250 nm wavelength range, can be observed in Figure 11B for λ > 700 nm. T_{sac} also has the highest V_{oc}s. The relation between substrate roughness and V_{oc} is well documented [9,10,17,33,34] and is especially relevant for the growth of nano- to poly-crystalline materials. This J_{sc}–V_{oc} trade-off as a function of substrate roughness demonstrates well the challenges in developing the right texture of optimal device performance.
– The highest efficiencies are achieved on the T_{sp}, with T_{honey} (a-Si(L)) a close second. The V_{oc}**FF* of T_{honey} suffers, presumably due stress induced in the nc-Si layer due to the relative steepness and periodic nature of the honeycomb slopes. More detailed research is being performed on the relation between (1) the honeycomb design (*r* and *p* of the mask and etching time), (2) the nc-Si properties (d_{ncsi} and processing conditions) and (3) the external PV device characteristics.

– The *EQE* of T_{honey} in Figure 11B also demonstrates the attractiveness of this periodic texture, as the highest response in the infrared ($\lambda > 1000\,\text{nm}$) is achieved using this periodic texture, which is in line with the constructive interference peaks observed in the *AID* measurements in this spectral range. This feature makes it of potential interest in multijunction silicon devices such as the one in [35–38], where high (infra)red response is essential for achieving high conversion efficiencies.

4 Conclusion

In this work, the optimization of two texturing approaches are presented that results in smooth, concave surface features on monocrystalline silicon. For T_{sac}, a sacrificial implanted poly-c-Si layer is used to develop a random surface texture. The influence of the processing conditions (layer thickness, implantation energy, dose and ion type, annealing time and temperature) of the sacrificial layer on the developed surface features is investigated. A relation is established between the implantation energy and ion type and the a-Si layer thickness. Additionally it was found that the largest features are formed at high implantation dose and relatively thick a-Si layers.

Additionally, a photolithographically developed honeycomb texture (T_{honey}) is presented. The influence of mask design on the honeycomb features is discussed and a relation is established between the honeycomb period and crack formation in nano-crystalline silicon layers.

The reflective properties of a number of T_{honey} and T_{sac} surfaces are characterized and compared to a third texturing approach, consisting of chemically smoothened pyramidal <111> feature (T_{sp}). It was demonstrated that high optical scattering yields can be achieved for both T_{honey} and T_{sp}. The angular intensity distribution of the period honeycomb texture shows a strong wavelength dependence, that should be tunable through photolithographic mask design.

Finally, the performance of the different textures integrated in a-Si/nc-Si tandem devices is compared using both optical device simulations and real device measurements. Simulations demonstrate strong improvements in J_{sc}-sum (≈45%), in reference to a flat surface, for T_{honey} and T_{sp} and high $V_{oc}{*}FF$ of over 1V are demonstrated for T_{sp}.

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Author contribution statement

Conceptualization: T. de Vrijer, Investigation: M. Wiering, D. van Nijen, G. Padmakumar, S. Sambamurthy, G. Limodio, Supervision: G. Limodio, T. de Vrijer, Writing – Original Draft: T. de Vrijer, Writing – Review & Editing: A.H.M Smets, T. de Vrijer, Funding acquisition: A.H.M Smets.

Supplementary material

Figure S1: Additional surface parameters and height profiles of the different textures, as obtained by atomic force microscopy.

Figure S2: SEM images of the textured surfaces (bottom) and cross-sectional SEM images of the texured surfaces + films.

The Supplementary Material is available at https://www.epjpv.org/10.1051/epjpv/2022021/olm.

References

1. Fraunhofer ISE, Photovoltaics Report, Tech. Rep. (2021). https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf
2. Joint Research Centre, Photovoltaics Technology Development Report 2020 (2020). https://doi.org/10.2760/827685
3. P. Perez-Rodriguez, W. Vijselaar, J. Huskens, M. Stam, M. Falkenberg, M. Zeman, W. Smith, A.H. Smets, Designing a hybrid thin-film/wafer silicon triple photovoltaic junction for solar water splitting, Prog. Photovolt.: Res. Appl. **27**, 245 (2019)
4. S. Kirner, H. Sarajan, A. Azarpira, T. Schedel-Niedrig, B. Stannowski, B. Rech, R. Schlatmann, Wafer surface tuning for a-Si:H/mc-Si:H/c-Si triple junction solar cells for application in water splitting, Energy Procedia **102**, 126 (2016)
5. T. de Vrijer, S. Miedema, T. Blackstone, D. van Nijen, C. Han, A.H.M. Smets, Application of metal, metal-oxide and silicon-oxide based intermediate reflective layers for current matching in autonomous high voltage multijunction photovoltaic devices, Progr. Photovolt.: Res. Appl. (2022). https://doi.org/10.1002/pip.3600
6. A. Blanker, P. Berendsen, N. Phung, Z. Vroon, M. Zeman, A. Smets, Advanced light management techniques for two-terminal hybrid tandem solar cells, Solar Energy Mater. Solar Cells **181**, 77 (2018)
7. M. Jošt, E. Köhnen, A.B. Morales-Vilches, B. Lipovšek, K. Jäger, B. Macco, A. Al-Ashouri, J. Krč, L. Korte, B. Rech, R. Schlatmann, M. Topič, B. Stannowski, S. Albrecht, Textured interfaces in monolithic perovskite/silicon tandem solar cells: advanced light management for improved efficiency and energy yield, Energy Environ. Sci. **11**, 3511 (2018)
8. M. Lozac'h, S. Nunomura, K. Matsubara, Double-sided TOPCon solar cells on textured wafer with ALD SiO_X layer, Solar Energy Mater. Solar Cells **207**, 110357 (2020)
9. M. Python, E. Vallat-Sauvain, J. Bailat, D. Dominé, L. Fesquet, A. Shah, C. Ballif, Relation between substrate surface morphology and microcrystalline silicon solar cell performance, J. Non-Cryst. Solids **354**, 2258 (2008)
10. H. Sai, K. Saito, N. Hozuki, M. Kondo, Relationship between the cell thickness and the optimum period of textured back reflectors in thin-film microcrystalline silicon solar cells, Appl. Phys. Lett. **102**, 053509 (2013)
11. H. Sai, T. Koida, T. Matsui, I. Yoshida, K. Saito, M. Kondo, Microcrystalline silicon solar cells with 10.5% efficiency realized by improved photon absorption via periodic textures and highly transparent conductive oxide, Appl. Phys. Express **6**, 104101 (2013)
12. T. de Vrijer, A.H.M. Smets, Advanced textured monocrystalline silicon substrates with high optical scattering yields and low electrical recombination losses for supporting

crack-free nano- to poly-crystalline film growth, Energy Sci. Eng. **9**, 1080 (2021)
13. H. Sai, K. Saito, M. Kondo, Enhanced photocurrent and conversion efficiency in thin-film microcrystalline silicon solar cells using periodically textured back reflectors with hexagonal dimple arrays, Appl. Phys. Lett. **101**, 173901 (2012)
14. T. de Vrijer, D. van Nijen, H. Parasramka, P.A. Procel Moya, Y. Zhao, O. Isabella, A.H. M Smets, The fundamental operation mechanisms of nc-$SiO_{X<0}$:H based tunnel recombination junctions revealed, Solar Energy Mater. Solar Cells **236**, 111501 (2022)
15. T. de Vrijer, H. Parasramka, S.J. Roerink, A.H. Smets, An expedient semi-empirical modelling approach for optimal bandgap profiling of stoichiometric absorbers: a case study of thin film amorphous silicon germanium for use in multi-junction photovoltaic devices, Solar Energy Mater. Solar Cells **225**, 111051 (2021)
16. K. Jäger, O. Isabella, L. Zhao, M. Zeman, Light scattering properties of surface-textured substrates, Phys. Stat. Solidi **7**, 945 (2010)
17. G. Yang, R.A. van Swaaij, H. Tan, O. Isabella, M. Zeman, Modulated surface textured glass as substrate for high efficiency microcrystalline silicon solar cells, Solar Energy Mater. Solar Cells **133**, 156
18. K. Jäger, O. Isabella, R.A.C.M.M. van Swaaij, M. Zeman, Angular resolved scattering measurements of nano-textured substrates in a broad wavelength range, Measur. Sci. Technol. **22**, 105601 (2011)
19. T. de Vrijer, A. Ravichandran, B. Bouazzata, A.H.M. Smets, The impact of processing conditions and post-deposition oxidation on the opto-electrical properties of hydrogenated amorphous and nano-crystalline Germanium films, J. Non-Cryst. Solids **553**, 120507 (2021)
20. S. Periasamy, S. Venkidusamy, R. Venkatesan, J. Mayandi, J. Pearce, J.H. Selj, R. Veerabahu, Micro-Raman scattering of nanoscale silicon in amorphous and porous silicon, Zeitsch. Phys. Chem. **231**, 1585 (2017)
21. W.S. Yoo, T. Ishigaki, T. Ueda, K. Kang, N.Y. Kwak, D.S. Sheen, S.S. Kim, M.S. Ko, W.S. Shin, B.S. Lee, S.J. Yeom, S.K. Park, Grain size monitoring of 3D flash memory channel poly-Si using multiwavelength Raman spectroscopy, in *2014 14th Annual Non-Volatile Memory Technology Symposium (NVMTS)*, IEEE (2014), pp. 1–4
22. T. de Vrijer, B. Bouazzata, A.H. M Smets, Spectroscopic review of hydrogenated, carbonated and oxygenated group IV alloys, Vibrat. Spectr. **121**, 103387 (2022)
23. R.B. Iverson, R. Reif, Stochastic model for grain size versus dose in implanted and annealed polycrystalline silicon films on SiO_2, J. Appl. Phys. **57**, 5169 (1985)
24. Y. Wada, S. Nishimatsu, Grain growth mechanism of heavily phosphorus-implanted polycrystalline silicon, J. Electrochem. Soc. **125**, 1499 (1978)
25. L. Mei, M. Rivier, Y. Kwark, R.W. Dutton, Grain-growth mechanisms in polysilicon, J. Electrochem. Soc. **129**, 1791 (1982)
26. W.K. Hofker, D.P. Oosthoek, N.J. Koeman, H.A.M. de grefte, Concentration profiles of boron implantations in amorphous and polycrystalline silicon, Radiat. Effects **24**, 223 (1975)
27. K. Suzuki, Y. Tada, Y. Kataoka, T. Nagayama, Monte Carlo simulation of ion implantation profiles calibrated for various ions over wide energy range, J. Semicond. Technol. Sci. **9**, 67 (2009)
28. E. Manea, E. Budianu, M. Purica, D. Cristea, I. Cernica, R. Muller, V. Moagar Poladian, Optimization of front surface texturing processes for high-efficiency silicon solar cells, Solar Energy Mater. Solar Cells **87**, 423 (2005)
29. H. Sai, K. Maejima, T. Matsui, T. Koida, M. Kondo, S. Nakao, Y. Takeuchi, H. Katayama, I. Yoshida, High-efficiency microcrystalline silicon solar cells on honeycomb textured substrates grown with high-rate VHF plasma-enhanced chemical vapor deposition, Jpn. J. Appl. Phys. **54**, 08KB05 (2015)
30. R. Santbergen, T. Meguro, T. Suezaki, G. Koizumi, K. Yamamoto, M. Zeman, GenPro4 optical model for solar cell simulation and its application to multijunction solar cells, IEEE J. Photovolt. **7**, 919 (2017)
31. M. Fischer, H. Tan, J. Melskens, R. Vasudevan, M. Zeman, A.H.M. Smets, High pressure processing of hydrogenated amorphous silicon solar cells: relation between nanostructure and high open-circuit voltage, Appl. Phys. Lett. **106**, 043905 (2015)
32. T. de Vrijer, B. Bouazzata, A. Ravichandran, J. van Dingen, P. Roelandschap, K. Roodenburg, S. Roerink, F. Saitta, T. Blackstone, A.H.M. Smets, Opto-electrical properties of group IV alloys: the inherent challenges of processing hydrogenated germanium, Adv. Sci. **9**, 2200814 (2022)
33. H.B. Li, R.H. Franken, J.K. Rath, R.E. Schropp, Structural defects caused by a rough substrate and their influence on the performance of hydrogenated nano-crystalline silicon n–i–p solar cells, Solar Energy Mater. Solar Cells **93**, 338 (2009)
34. H. Sai, K. Maejima, T. Matsui, T. Koida, K. Matsubara, M. Kondo, Y. Takeuchi, S. Sugiyama, H. Katayama, I. Yoshida, Impact of front TCO layer in substrate-type thin-film microcrystalline silicon solar cells, in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)* (IEEE, 2015), pp. 1–6
35. H. Tan, E. Moulin, F.T. Si, J.-W. Schüttauf, M. Stuckelberger, O. Isabella, F.-J. Haug, C. Ballif, M. Zeman, A.H.M. Smets, Highly transparent modulated surface textured front electrodes for high-efficiency multijunction thin-film silicon solar cells, Progr. Photovolt.: Res. Appl. **23**, 949 (2015)
36. H. Sai, T. Matsui, K. Matsubara, Stabilized 14.0%-efficient triple-junction thin-film silicon solar cell, Appl. Phys. Lett. **109**, 183506 (2016)
37. D.Y. Kim, E. Guijt, F.T. Si, R. Santbergen, J. Holovský, O. Isabella, R.A. van Swaaij, M. Zeman, Fabrication of double- and triple-junction solar cells with hydrogenated amorphous silicon oxide (a-SiO_X:H) top cell, Solar Energy Mater. Solar Cells **141**, 148 (2015)
38. J.-W. Schüttauf, B. Niesen, L. Löfgren, M. Bonnet-Eymard, M. Stuckelberger, S. Hänni, M. Boccard, G. Bugnon, M. Despeisse, F.-J. Haug, F. Meillaud, C. Ballif, Amorphous silicon–germanium for triple and quadruple junction thin-film silicon based solar cells, Solar Energy Mater. Solar Cells **133**, 163 (2015)

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