A Capacitively Degenerated 100-dB Linear 20-150 MS/s Dynamic Amplifier

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A Capacitively Degenerated 100-dB Linear 20–150 MS/s Dynamic Amplifier

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***Abstract*— This paper presents a new dynamic residue amplifier topology for pipelined analog-to-digital converters. With an input signal of 100 $mV_{pp,diff}$ and 4× gain, it achieves −100-dB total harmonic distortion, the lowest ever reported for a dynamic amplifier. Compared to the state of the art, it exhibits 25 dB better linearity with twice the output swing and similar noise performance. The key to this performance is a new linearization technique based on capacitive degeneration, which exploits the exponential voltage-to-current relationship of MOSFET in weak inversion. The prototype amplifier is fabricated in a 28-nm CMOS process and dissipates only 87 μW at a clock speed of 43 MS/s, thereby improving the energy per cycle by 26× compared with that of state-of-the-art high-linearity amplifiers.**

***Index Terms*— Amplifier, analog linearization technique, analog-to-digital converter (ADC), capacitive degeneration, cross-coupled capacitors, digital nonlinearity calibration, dynamic residue amplifier, integrator, split-capacitor technique.**

I. Introduction

THE evolution of software-defined radio (SDR) [1] over the past few decades has fueled the demand for analog-to-digital converters (ADC) with wider bandwidth and lower power dissipation. The attractions of the SDR-based approach are its flexibility and easy scalability to include new standards. However, for wireless communication systems such as GSM or LTE, a weak desired signal often needs to be processed in the presence of a strong interferer (or blocker) from an adjacent channel. This imposes tough requirements on the wideband ADC because the channel selection is performed in the digital domain rather than in the analog front-end. In particular, the presence of such interferers imposes a stringent linearity requirement (>80 dB) on the ADC [2], since the intermodulation products caused by ADC nonlinearity cannot be improved by subsequent digital filtering. Simultaneously, it needs to be power efficient [3], in order to compete with traditional mixer-based solutions.

Pipelined ADCs are often chosen for such wide-bandwidth and moderate-to-high resolution (>10 b) applications. In a pipelined ADC, residue amplifiers are used to improve the noise performance. However, they need to have sufficiently low noise and nonlinearity to avoid degrading ADC performance. Since noise is fundamental, achieving the desired noise level is going to require a certain amount of power dissipation. Nonlinearity, on the other hand, results in deterministic errors and thus can be improved by analog [4] or digital [5] techniques. It is our goal to spend as little power as possible on improving linearity.

Residue amplification with high linearity (>60 dB) traditionally relies on closed-loop amplifiers with high loop gain [6], [7]. However, these require large bandwidth to settle accurately, degrading power efficiency. Alternative amplifier topologies [8]–[16] have been introduced to improve the amplification efficiency. Dynamic amplifiers (or integrators) [3], [14]–[16] inherently allow for the lowest possible small-signal bandwidth and hence the lowest possible power dissipation for a given noise performance [3]. However, they exhibit more nonlinearity. Digital nonlinearity calibration [5], [16]–[20] can be used to detect and correct these errors. Although detection can be done at a much lower rate compared to the sampling speed F_S, digital error correction requires logic operating at F_S, often consuming considerable power.

In this paper, a linearization technique is introduced that employs capacitive degeneration to significantly improve the linearity of a dynamic amplifier. A power-efficient amplifier topology is then proposed that uses this "capacitively degenerated" linearization (CDL) technique. It employs a cross-coupled capacitor configuration that results in reduced capacitor size and improved common-mode (CM) rejection capability. To compensate for the effects of process spread, the amplifier can be placed in a slow control loop which digitally detects any residual nonlinearity and minimizes it via an analog control-voltage with negligible power overhead. The proof-of-concept amplifier demonstrates 100-dB linearity up to 150 MS/s clock speed for 100-$mV_{pp,diff}$ input signal. Compared to published high-linearity amplifier designs [4]–[7], the proposed amplifier requires at least 26 times less energy per cycle.

This paper is organized as follows. Section II explains the capacitively degenerated linearization technique and its implications on noise. Section III describes the proposed dynamic amplifier design and its operation. Section IV discusses the implementation details. Finally, Sections V and VI present the measurement results and the conclusion.

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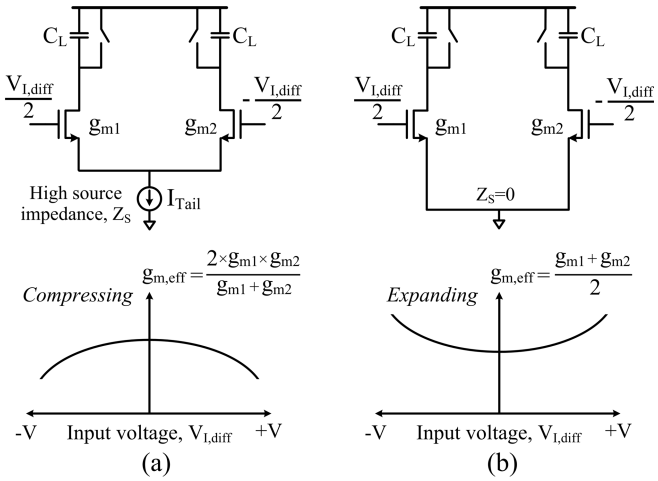

Fig. 1. Differential pair with (a) tail-current source and (b) grounded source nodes, and their nonlinear effective transconductances ($g_{m,\text{eff}}$).

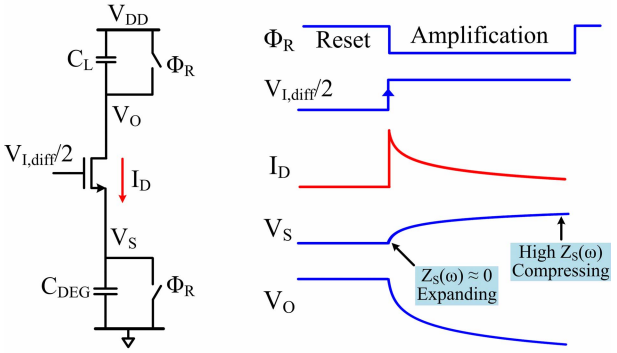

Fig. 2. Time-domain analysis of a dynamic amplifier half circuit having capacitive degeneration.

II. Capacitively Degenerated Linearization Technique

The proposed linearization technique assumes that the MOSFETs are biased in the weak inversion saturation region, where their voltage-to-current (V–I) relationship is exponential. The same concept can therefore be applied to bipolar junction transistors as well, since their V–I characteristic is also exponential. In this section, the CDL technique is first explained intuitively, and then analytically. Finally, the effect of this technique on the amplifier's overall noise performance is discussed.

A. Intuitive Explanation

1) Expanding and Compressing Nonlinearity: To get an intuitive understanding of the CDL technique, it is useful to distinguish between two types of nonlinearity: expanding and compressing. Fig. 1 illustrates two amplifiers that are biased in the weak inversion saturation region. Consider first the differential pair with a tail-current source having high source impedance Z_S [Fig. 1(a)]. The two transistors of the amplifier have transconductances g_{m1} and g_{m2}. The effective transconductance can be expressed as $g_{m,\text{eff}} = (2 \times g_{m1} \times g_{m2}/(g_{m1} + g_{m2}))$, which is dominated by the smaller of g_{m1} and g_{m2}. With larger input signals $V_{I,\text{diff}}$, the fixed tail-current forces one transistor to carry less current, decreasing its transconductance. Thus, the effective transconductance $g_{m,\text{eff}}$ of the amplifier decreases as well, exhibiting a compressing nonlinearity. However, if the source nodes of the differential pair are tied to ground ($Z_S = 0$), instead of to a current source, the two half circuits can operate independently without limiting each other [Fig. 1(b)]. The $g_{m,\text{eff}}$ becomes the average of two individual tansconductances g_{m1} and g_{m2}, which is dominated by the stronger one. As a result, the effective transconductance increases with input, leading to an expanding nonlinearity.

2) Capacitive Degeneration: Resistive degeneration [21] is a commonly used technique to linearize an amplifier's effective transconductance. In a discrete-time environment, capacitors can also be used as a degeneration element. Fig. 2 shows a half circuit of a dynamic amplifier which is degenerated by a source capacitor C_{DEG}. A load capacitor C_L is added at the drain, which together with the C_{DEG} capacitor defines the amplifier's small-signal gain (C_{DEG}/C_L). Since the amount of degeneration due to the capacitor C_{DEG} changes over time, it is more useful to analyze this circuit in the time domain rather than in the frequency domain.

The circuit operates in two phases: reset and amplification. During reset, C_{DEG} and C_L capacitors are pre-charged to the ground and supply, respectively. At the start of the amplification phase, an input step ($V_{I,\text{diff}}/2$) is applied to the amplifier. As a result, drain current I_D flows through the amplifier charging the capacitors. Since $C_L < C_{\text{DEG}}$, the drain voltage V_{O} changes faster than the source voltage V_S, providing gain. For the high-frequency components associated with the step input, the degeneration capacitor C_{DEG} acts like a low impedance ($Z_S(\omega) \approx 0$), and thus only slightly degenerates the MOS transistor. The circuit then behaves like a differential pair with grounded sources [Fig. 1(b)] and exhibits an expanding nonlinearity. However, as the amplification progresses, the impedance $Z_S(\omega)$ of the C_{DEG} capacitor gradually becomes higher. The high impedance then degenerates the amplifier more, eventually causing it to exhibit a compressing nonlinearity similar to the differential pair with a tail-current source [Fig. 1(a)].

The amplifier experiences a large gate–source voltage V_{GS} due to the initial input step at the beginning of integration. If V_{GS} is too large and pushes the device into the strong-inversion regime, then the V–I characteristic is no longer exponential, gradually degrading the proposed CDL technique. Note that V_{GS} goes down during the integration as the source voltage V_S goes up, bringing the amplifier toward weak inversion. However, the moment when the V–I characteristic becomes exponential will now be signal dependent, since the integration starts in strong-inversion for large signals and in weak inversion for small signals. Therefore, the amplifier has to be designed to operate in the weak-inversion region with the maximum input signal. If for example, the input signal range is 100 $\text{mV}_{\text{pp,diff}}$, then each MOSFET sees a maximum of 25-mV peak signal, which it needs to handle while still operating in the weak-inversion region.

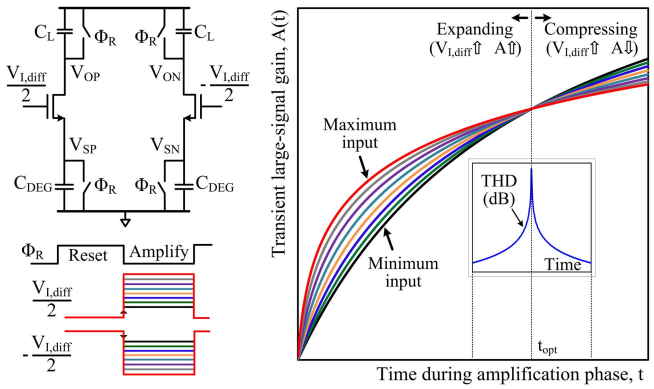

Fig. 3. Illustration of the CDL technique using a dynamic amplifier.

Fig. 3 illustrates the transition from expanding to compressing nonlinearity by plotting the amplifier's large-signal gain against time for several values of the input step $V_{I,\text{diff}}$. The transient gain $A(t)$ can be expressed by taking a ratio of the differential output signal to the differential input step as follows:

$$A(t) = (V_{\text{OP}}(t) - V_{\text{ON}}(t))/V_{I,\text{diff}}. \tag{1}$$

The gain $A(t)$ increases with time, but in an input-amplitude dependent manner, indicating nonlinearity. However, there is a crossover moment t_{opt}, where the nonlinearity changes from an expanding to a compressing characteristic. At this moment, the amplifier's gain $A(t)$ is independent of the input signal $V_{I,\text{diff}}$, indicating perfect linearity. This can also be proven mathematically, as will be described next.

B. Analytical Approach

The drain–source current I_{DS} of NMOS transistor in the weak-inversion region (assuming that its body is tied to ground) can be expressed [22] as follows:

$$I_{\text{DS}} = I_{\text{D0}} \exp\left(\frac{V_G}{nU_T}\right) \exp\left(-\frac{V_S}{U_T}\right)\left(1 - \exp\left(-\frac{V_{\text{DS}}}{U_T}\right)\right) \tag{2}$$

where I_{D0} is a process-dependent parameter, n is the weak-inversion slope factor $\approx$1.4, and U_T is the thermal voltage $= kT/q$. When $V_{\text{DS}} > 4U_T$, the term $\exp(-V_{\text{DS}}/U_T) \ll 1$ and the transistor is saturated. Moreover, the V_{DS} voltage required to keep the transistor in weak-inversion saturation is independent of the V_{GS} voltage unlike in strong-inversion saturation. The drain current I_{DS} in the weak-inversion saturation region thus can be simplified as follows:

$$I_{\text{DS}} \cong I_{\text{D0}} \exp\left(\frac{V_G}{nU_T}\right) \exp\left(-\frac{V_S}{U_T}\right). \tag{3}$$

It can be mathematically shown (Appendix A) that after a specific time t_{opt} during amplification, the amplifier's gain $A(t)$ is independent of the input signal and hence a purely linear amplification is achieved. This optimum time t_{opt} and gain $A(t_{\text{opt}})$ are given by

$$t_{\text{opt}} = C_{\text{DEG}}U_T/I_{Q0} \tag{4}$$

$$A(t_{\text{opt}}) = C_{\text{DEG}}/2nC_L. \tag{5}$$

The optimum gain $A(t_{\text{opt}})$ is approximately one-third ($1/2n \approx 1/3$) of the amplifier's steady-state gain (C_{DEG}/C_L). The amplifier therefore only needs to settle to less than half a time constant (τ) to achieve $A(t_{\text{opt}})$. Hence, it effectively behaves like an integrator, which is good for noise performance [3]. Note that any parasitic source resistance in series with C_{DEG} capacitors slightly affects this $A(t_{\text{opt}})$ value (Appendix B).

Degeneration usually improves linearity at the expense of the amplifier's effective transconductance $g_{m,\text{eff}}$. With traditional resistive (R_S) degeneration, the degeneration factor ($1 + g_m R_S$) needs to be significant ($\sim$10) to get a reasonable linearity improvement, sacrificing both $g_{m,\text{eff}}$ and power efficiency. A key benefit of the proposed CDL technique is that it degenerates the amplifier by only $\sim$33% to achieve the optimum linearity performance. Hence, $g_{m,\text{eff}}$ is only reduced by a factor of $\sim$1.5, resulting in significantly better power efficiency than resistive degeneration.

C. Calibration "Knob"

The final goal is to use this amplifier as a residue amplifier in a pipelined ADC. As discussed above, the amplifier's output needs to be sampled at a time t_{opt} to ensure optimal linearity, which is a function of bias current and C_{DEG} according to (4). However, in a pipelined ADC, the allocated time for amplification ($t_{\text{amp}} \approx T_{\text{clk}}/2$) is governed by the system clock and cannot be changed easily. Therefore, the bias current of the amplifier is used as a calibration "knob" to adjust t_{opt} and ensure that $t_{\text{opt}} = t_{\text{amp}}$, without any capacitor tuning. In this paper, the nonlinearity that occurs when $t_{\text{opt}} \neq t_{\text{amp}}$ is detected off-chip. In an ADC, this could be detected by processing its digital output with the help of various background techniques [5], [16]–[20]. Having nonlinearity indicates that $t_{\text{opt}} \neq t_{\text{amp}}$ assuming it is primarily caused by the residue amplifier. Subsequently, the bias current is adjusted to ensure $t_{\text{opt}} = t_{\text{amp}}$ and optimize linearity over process voltage temperature (PVT).

D. Impact on Noise Performance

To analyze the impact of the proposed linearization technique on the amplifier's overall noise performance, the half circuit shown in Fig. 2 can be considered. At the end of the reset phase, the noise sampled across the degeneration capacitor C_{DEG} due to the switching action is kT/C_{DEG}. During the amplification phase, the noise on the C_{DEG} capacitor is transferred to the amplifier's output. Note that since the body of the transistor is connected to the ground, the amplifier's gain from the source to the output is n(=weak-inversion slope factor) times larger than that from the gate to the output. Assuming that the amplification period t_{amp} is equal to the optimum linearity time t_{opt}, the output noise power due to switched-capacitor (SC) C_{DEG} can be expressed as

$$P_{n,\text{cdeg}} = (kT/C_{\text{DEG}})(n \times A(t_{\text{opt}}))^2. \tag{6}$$

Of course, the amplifier's transistors also contribute noise. Since the amplifier behaves like an integrator as discussed in

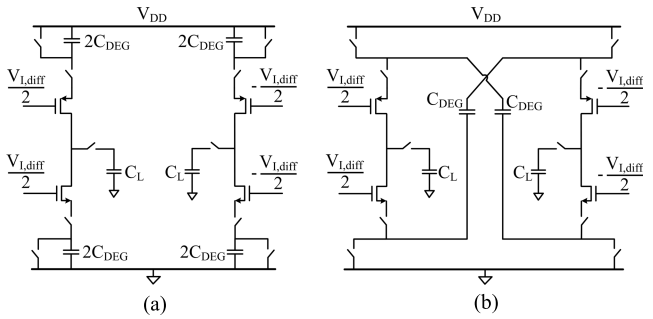

Fig. 4. Push–pull (a) pseudo-differential and (b) proposed differential dynamic amplifiers.

Section II-B, its integrated output noise power $P_{n,\mathrm{gm}}$ at the end of the amplification period can be approximated [3] as

$$P_{n,\mathrm{gm}} = \gamma\,(2kT/C_L)A(t_{\mathrm{opt}}) \tag{7}$$

where γ is the noise factor of the MOS transistor ($\approx$2/3). Dividing (6) by (7) gives

$$P_{n,c\mathrm{deg}}/P_{n,\mathrm{gm}} = (n^2 C_L/2\gamma\, C_{\mathrm{DEG}})A(t_{\mathrm{opt}}). \tag{8}$$

Substituting $A(t_{\mathrm{opt}})$ from (5) results in

$$P_{n,c\mathrm{deg}} = (n/4\gamma)\,P_{n,\mathrm{gm}} \approx P_{n,\mathrm{gm}}/2. \tag{9}$$

Therefore, the noise power associated with the degeneration capacitor C_{DEG} is approximately two times smaller than the amplifier's own noise. In reality, this contribution will be even smaller considering the fact that there are other noise sources in the circuit, e.g., input sampling noise and reset noise on C_L.

In the case of residue amplifiers with sufficient settling, jitter on the output sampling clock contributes negligible noise since their outputs do not change much at the end of the amplification period. However, due to the integrating nature of the proposed amplifier, its output will still be changing significantly at the sampling moment, resulting in jitter-induced noise $P_{J,\mathrm{amp}}$ [23]. In addition, any amplifier is affected by jitter-induced noise $P_{J,\mathrm{in}}$ at its input due to high-frequency signal acquisition by a noisy clock. Unlike $P_{J,\mathrm{amp}}$ which is not affected by the input frequency F_{IN}, $P_{J,\mathrm{in}}$ increases with F_{IN}. So, the system needs to be designed to accommodate jitter noise at close to Nyquist frequencies (worst case). It can be shown that the integrated jitter noise power at the input $P_{J,\mathrm{in-Nyq}}$ for near-Nyquist signals is similar to the output jitter power $P_{J,\mathrm{amp}}$. If an amplifier gain of 4 is assumed, $P_{J,\mathrm{amp}}$ will be reduced by a factor of 16 when referred to the input. Hence, its contribution is negligible compared to $P_{J,\mathrm{in-Nyq}}$.

III. Dynamic Amplifier Design

A. Proposed Amplifier

As discussed above, Fig. 3 illustrates the principle of capacitive degeneration, using a dynamic amplifier with an NMOS differential pair only. Fig. 4(a) shows an improved dynamic amplifier, which also employs a PMOS differential pair to obtain push–pull capability. Hence, its effective transconductance is doubled by current reuse, improving the amplifier's power efficiency. However, this topology has some disadvantages. First, it is pseudo-differential, and thus exhibits equal CM and differential-mode gain (i.e., it has no CM rejection). When used in a pipelined ADC, any CM signals will be amplified while propagating through the pipelined stages and may end up overloading the ADC. Secondly, the degeneration capacitors C_{DEG} require a significant amount of area.

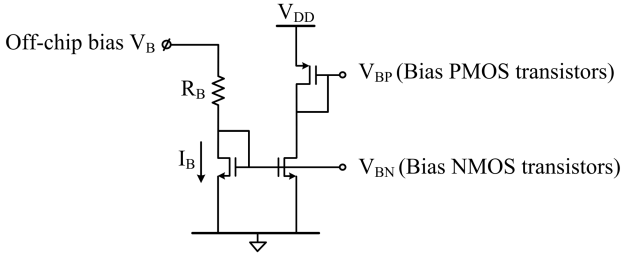

Fig. 5. Biasing circuit of the proposed dynamic amplifier.

The topology shown in Fig. 4(b) alleviates these disadvantages. It employs degeneration capacitors C_{DEG} in a differentially cross-coupled configuration. Therefore, the amplifier reacts differently to CM and differential-mode signals, resulting in excellent CM suppression as will be discussed later in this section. Moreover, due to the differential capacitor configuration, the overall value of C_{DEG} capacitors is reduced by 4$\times$ for the same amplifier gain. The amplifier's biasing circuit is shown in Fig. 5. The bias current I_B acts as the amplifier's calibration "knob" and can be programmed via an off-chip bias voltage V_B.

B. Circuit Operation

The proposed amplifier has two different operating phases, i.e., reset and amplification, as shown in Fig. 6. During reset, the C_{DEG} capacitors are connected between the supply and ground for pre-charging it. At the same time, the load capacitors C_L are reset to their CM voltage. Furthermore, the amplifier is switched off by opening the series switches at the NMOS and PMOS sources, reducing its power consumption by nearly half. After reset, the amplifier enters the amplification phase and gets disconnected from the supplies. During this period, the C_{DEG} capacitors act as the degeneration capacitor as well as a local supply for the amplifier.

Symmetry in differential amplifiers is essential to avoid offset and even-order distortion. However, mismatch between the transistors and capacitors in the two half circuits will limit this symmetry. The proposed linearization technique only addresses odd-order distortion and so cannot correct for these effects. To overcome this problem, a tunable offset voltage V_{OS} is stored on the load capacitors C_L during the reset phase. Note that in an ADC, background calibration techniques [24] can be used to detect second-order distortion in the digital domain over PVT in order to adjust the V_{OS} voltage. This V_{OS} tunes the MOSFETs' initial drain-to-source voltages and mitigates even-order distortion caused by mismatch.

C. Common-Mode Behavior

A key benefit of the proposed amplifier is its excellent CM rejection capability. This becomes obvious by observing that

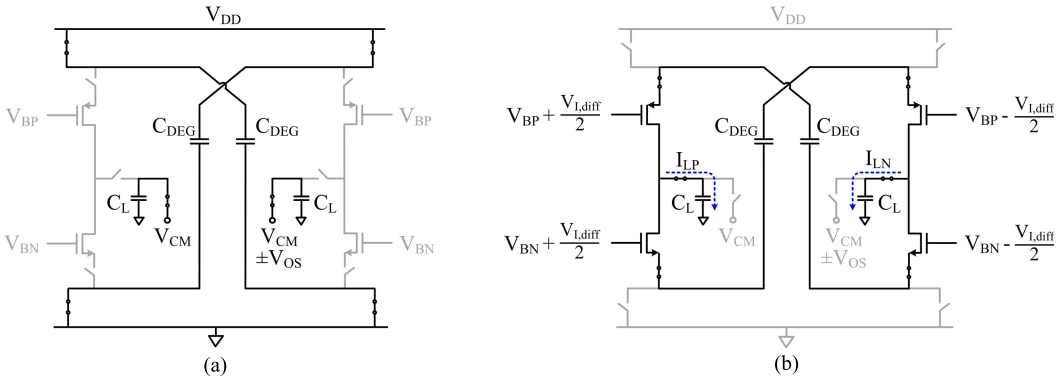

Fig. 6. Operation of the proposed dynamic amplifier during the (a) reset and (b) amplification phases.

in the amplification phase [Fig. 6(b)], there is no connection to the supply voltages, i.e., the circuit is completely floating. Only parasitic capacitances between the source nodes and supply or ground can cause a finite CM transfer function. As a result, the CM gain as well as the CM to differential-mode conversion is reduced significantly.

The proposed amplifier does not require any dedicated CM feedback (CMFB) circuit to stabilize its output CM voltage, which saves power and area. This can be understood by realizing that during amplification, ignoring parasitic capacitances, the entire circuit is only connected to ground through both load capacitors C_L [Fig. 6(b)]. So, the output load currents $I_{\rm LP}$ and $I_{\rm LN}$ have to be the equal but opposite in sign ($I_{\rm LP} = -I_{\rm LN}$), allowing only differential current to flow through C_L. The CM current (($I_{\rm LP} + I_{\rm LN}$)/2) has to be zero, and hence no CMFB circuit is required.

IV. Implementation Details

The proposed amplifier with CDL technique can achieve excellent linearity (<−100-dB total harmonic distortion (THD)) at high input frequencies. However, measuring this is quite challenging because any measurement circuitry added to the signal path must itself be extremely linear. Using a spectrum analyzer suitable for high-frequency signal measurement introduces two issues. First, most cannot support measurements over a 100-dB dynamic range. Second, most use 50-Ω input termination, which in our case would require an additional buffer, and hence introduce extra nonlinearity.

The use of an audio analyzer (APx555) eliminates both of these issues since it facilitates high-linearity measurements (<−120-dB THD) and employs 100-kΩ input termination, making it relatively easy to drive. However, it can only measure audio-frequency signals. Therefore, to measure the amplifier's performance with high-frequency inputs, an output chopper is implemented to down-convert higher frequency signals to the audio band, as will be described later in this section. Moreover, a low-pass filter (LPF) is used to remove high-frequency spurs before taking the output off-chip to measure with the audio analyzer.

A. Low-Pass Filter Design

At the end of the amplification phase $\Phi_{\rm A}$, the amplifier's output voltage is sampled on the load capacitors C_L.

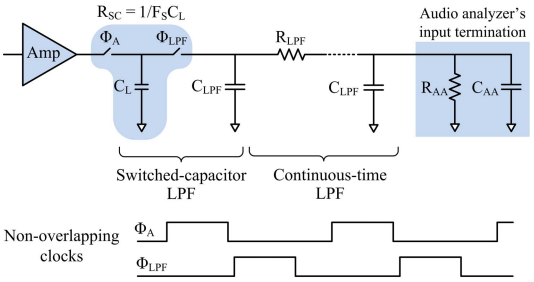

Fig. 7. LPF design.

Subsequently, the output signal needs to be taken off-chip for measurement. To do this, the voltages on C_L are re-sampled onto larger capacitors $C_{\rm LPF}$ during an additional clock phase $\Phi_{\rm LPF}$, as shown in Fig. 7. The circuit effectively behaves like a SC LPF with a cut-off frequency given by

$$f_{\rm SC,-3\,dB} = (1/2\pi) F_S (C_L/C_{\rm LPF}) \tag{10}$$

where F_S is the operating speed of the clock. For example, if $C_{\rm LPF} = 125\ C_L$ and $F_S = 50$ MS/s, then the cut-off frequency of the filter becomes $f_{SC,-3\,\rm dB} \approx 64$ kHz.

The audio analyzer has a 100-kΩ input termination resistor ($R_{\rm AA}$) in parallel with a 100-pF capacitor ($C_{\rm AA}$). Due to the resistive part $R_{\rm AA}$ of the termination, there could be considerable signal attenuation if the design under test is not sized appropriately to drive the audio analyzer. This becomes evident by recognizing that the SC C_L is equivalent to a resistor $R_{\rm SC} = 1/F_S C_L$. This SC-resistor $R_{\rm SC}$ together with the audio analyzer's termination resistor $R_{\rm AA}$ gives a signal attenuation β as follows:

$$\beta = R_{\rm SC}/(R_{\rm AA} + R_{\rm SC}). \tag{11}$$

If we assume that $C_L = 500$ fF and $F_S = 50$ MS/s, the equivalent SC resistor $R_{\rm SC}$ is 40 kΩ. Given $R_{\rm AA} = 100$ kΩ, this leads to a signal loss of approximately 30%. Therefore, the whole design is sized ($C_L = 7.6$ pF and $C_{\rm DEG} = 30$ pF) to keep signal attenuation below 5% while maintaining the same amplifier gain and filter bandwidth.

Due to sampling action, the SC LPF generates images around multiples of the clock frequencies. Any spurs around those frequencies will not be filtered out before going to the

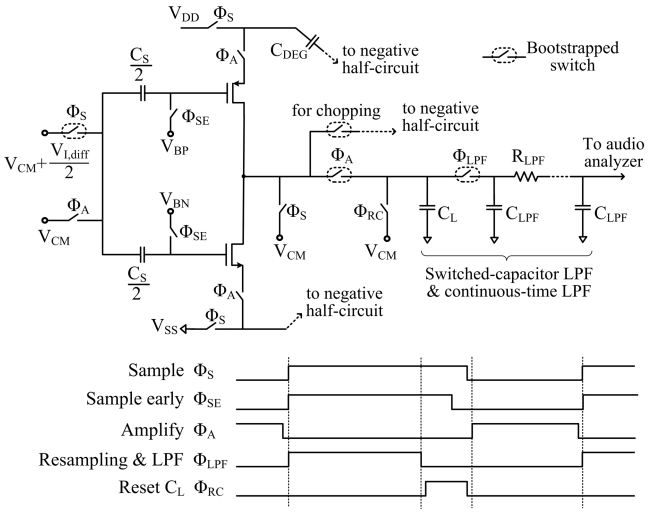

Fig. 8. Half circuit of the implemented topology to test the amplifier.

audio analyzer. So, a continuous-time LPF is used after the SC LPF (Fig. 7), resulting in an overall cut-off frequency $f_{-3\,\mathrm{dB}}$ of 45 kHz. Since the input signals are assumed to be at 2.5 kHz, this allows measurements of up to the 17th harmonics of the input signal. Any unwanted signals, including noise beyond $f_{-3\,\mathrm{dB}}$ frequency, will be suppressed by the LPF. Although it limits the amplifier's noise measurement, it plays a crucial role in measuring −120-dB distortion tones relative to the main signal.

B. Implemented Circuit Topology

Fig. 8 shows the half circuit of the implemented topology along with its timing diagram. All the switches in the signal path are bootstrapped to ensure sufficient linearity. During the sampling phase Φ_S, the input signal is sampled on the sampling capacitor C_S. An early sampling clock Φ_{SE} is used for bottom plate sampling. Sampling capacitor C_S is split into two parts in order to bias the amplifier's NMOS and PMOS transistors independently [11]. As a result, no capacitor level shifters are required [18], which improves power efficiency and saves area. Since the amplifier is not used during Φ_S, it is switched off to save power, while the degeneration capacitors C_{DEG} are pre-charged to the supply voltage.

During the amplification phase Φ_A, the amplifier is connected to the cross-coupled capacitors C_{DEG}. Simultaneously, the top plates of the input sampling capacitors are tied to the CM voltage to pass the signal to the bottom-plate side, thus giving an input step to the amplifier. At the end of the amplification, the output signal is captured on the load capacitor C_L. While the input network captures the next data sample, two events happen at the output. First, during Φ_{LPF} the output signal is resampled onto the filter capacitors C_{LPF} and also low-pass filtered. After that, the load capacitors C_L are reset (Φ_{RC}) to their CM voltages to remove any inter-symbol interference. During this time, a tunable offset voltage is also added on the C_L capacitors to mitigate circuit imbalance, as described in Section III-B.

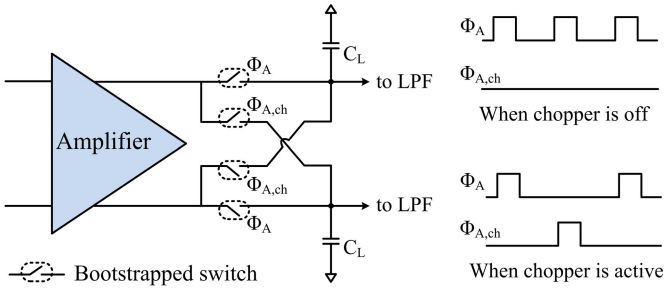

Fig. 9. Output chopper to measure with near-Nyquist frequency input.

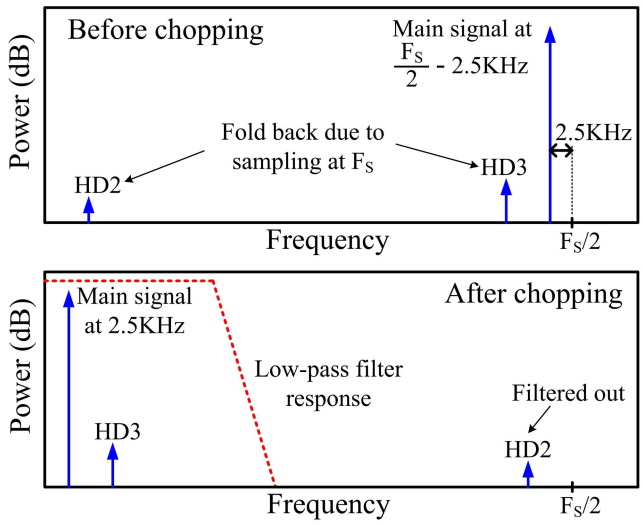

Fig. 10. Conceptual spectra before and after output chopping.

C. Output Chopper Design

A chopper is implemented at the amplifier output to facilitate its high-frequency signal measurement, as shown in Fig. 9. It can be programmed to be either ON or OFF. When the chopper is off, the Φ_A clock runs at the full sampling speed and the other clock $\Phi_{A,\mathrm{ch}}$ becomes inactive to disable the chopping switches. However, when the chopper turns on, both the clocks Φ_A and $\Phi_{A,\mathrm{ch}}$ operate at half the sampling speed. The input signal is applied close to the Nyquist frequency ($F_S/2$ − 2.5 kHz). Since there is no chopping at the input, the amplifier's high-frequency signal performance is truly captured. The signal is only down sampled to the audio band (2.5 kHz) after the output chopping. As a result, it can pass through the filter and be measured by the audio analyzer. The drawback, however, is that the even-order harmonic distortion tones will be near the Nyquist frequency after the chopping, as shown in Fig. 10. Hence, they are filtered out by the LPF and cannot be measured.

V. Measurement Results

Fig. 11 shows the setup used for low-frequency and near-Nyquist frequency signal measurements. The audio analyzer's high-precision signal generator is used for measurements with audio-frequency input signals. To measure with near-Nyquist input frequencies, a high-frequency signal generator is used. It is followed by an off-chip bandpass filter to

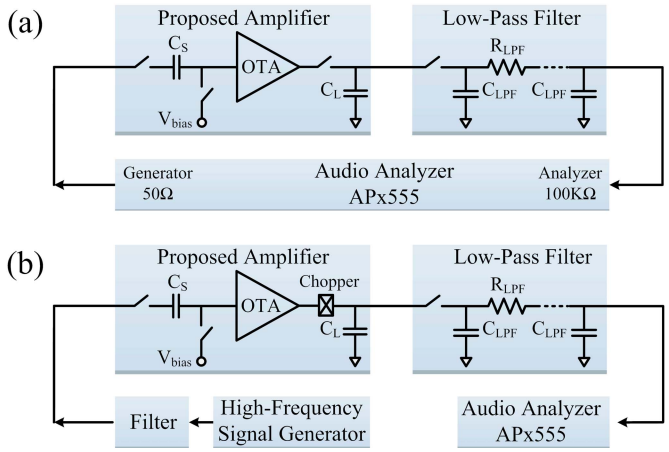

Fig. 11. Measurement setups for (a) low-frequency and (b) near-Nyquist frequency inputs.

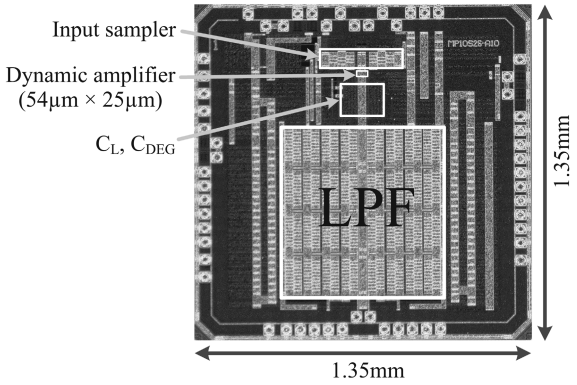

Fig. 12. Chip photograph.

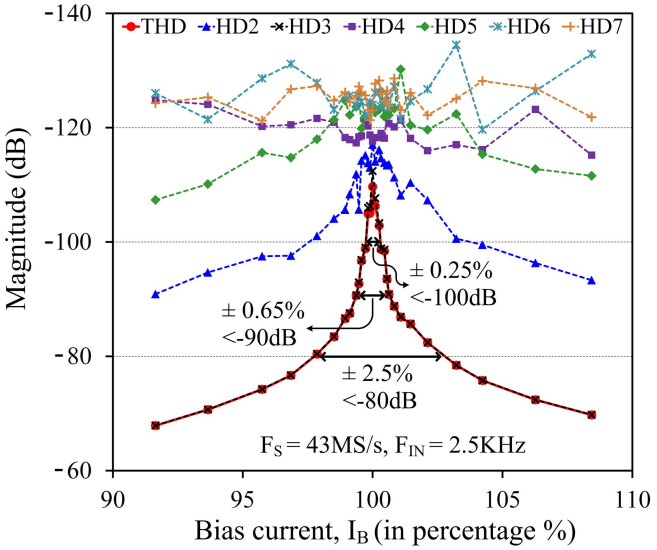

Fig. 13. Measured THD and harmonics as a function of bias current (in percentage).

remove harmonic tones. For this measurement, the chopper is enabled to bring the signal in the audio band, as explained in Section IV-C. The prototype design is fabricated in a 28-nm digital CMOS process. The area occupied by the proposed amplifier is approximately 0.0014 mm^2. A die photograph of the chip is shown in Fig. 12.

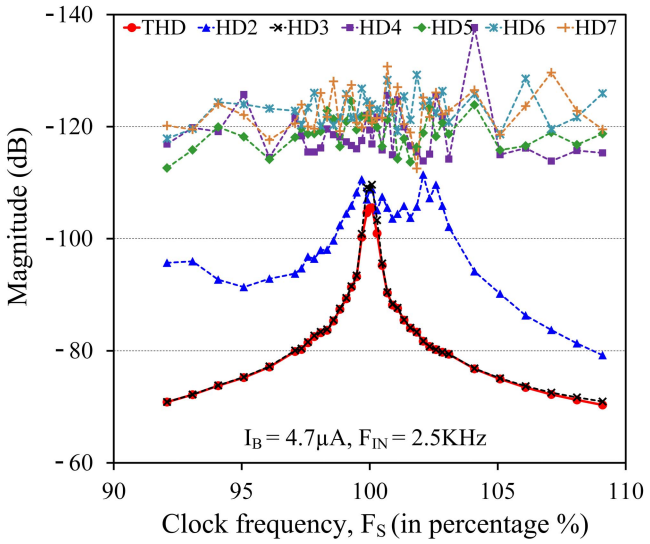

Fig. 14. Measured THD and harmonics as a function of clock frequency (in percentage).

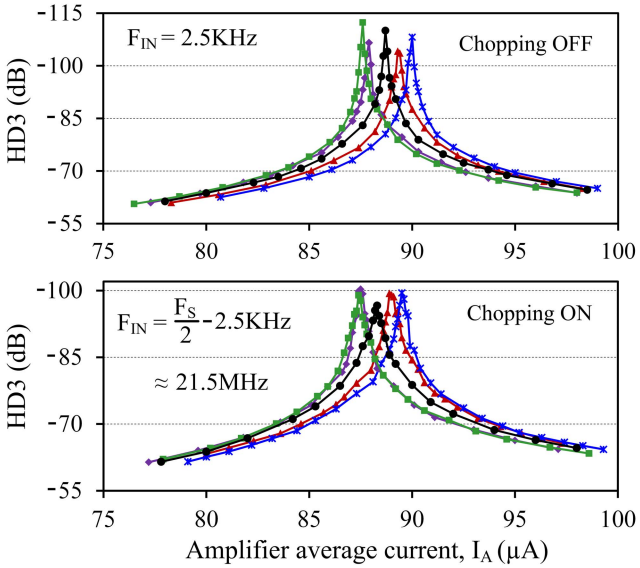

Fig. 15. Measured HD3 for five chips with low and near-Nyquist inputs.

Unless otherwise stated, all the measurements are performed at 43 MS/s clock speed with a 100-$mV_{pp,diff}$ input signal and ~4× gain. Fig. 13 shows the amplifier's linearity when its bias current I_B (i.e., the calibration knob) is varied. The THD is limited by HD3 (as expected) with an optimum of −108 dB. Note that the shape as well as the measured THD is very close to the simulated curve (Appendix C). Even with ±2.5% bias current I_B variation, the THD remains better than −80 dB, showing the wide linear range of the proposed amplifier. Although the bias current is used as the calibration knob in this design, the clock frequency F_S can also be adjusted to calibrate the amplifier's nonlinearity (if allowed by the system), as shown in Fig. 14. Fig. 15 shows the linearity measurement over five chips. Even with a near-Nyquist frequency input, the amplifier achieves around −100-dB HD3. The measured output spectra corresponding to the optimum

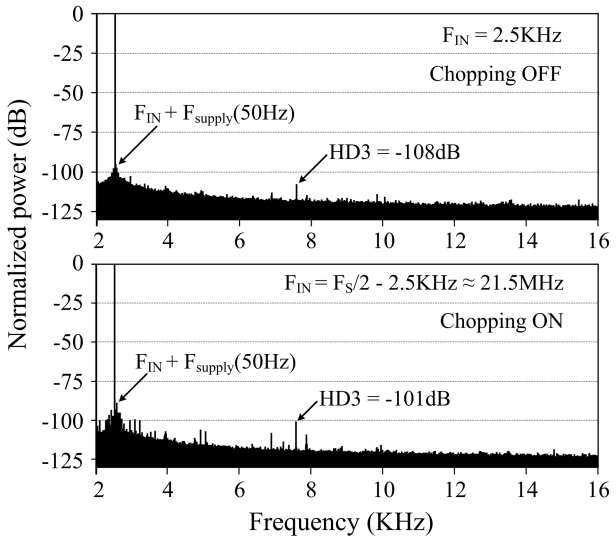

Fig. 16. Measured output spectra at 43 MS/s for a 100-$mV_{pp,diff}$ input signal.

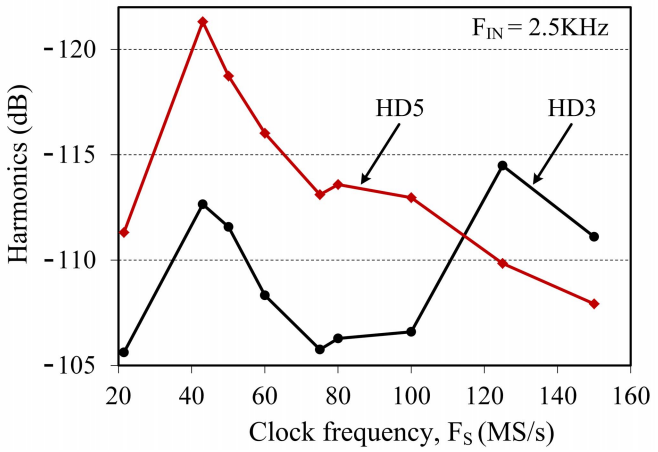

Fig. 17. Measured linearity performance from 20 MS/s to 150 MS/s clock frequencies.

linearity settings are shown in Fig. 16. Intermodulation tones between the desired signal and the supply (50 Hz) appear around the main tone at multiples of the supply frequency. The proof-of-concept amplifier consumes 87 μA from a 1-V supply. The clock circuitry consumes 230 μW while the rest dissipates 39 μW. The measured noise spectral density after the LPF is 57 nV/$\sqrt{\text{Hz}}$, which corresponds well with simulations (Appendix C).

The sampling speed F_S of the amplifier is varied from 20 to 150 MS/s with an input amplitude of 100 $mV_{pp,diff}$. For each of these F_S, the bias current is adjusted to calibrate the linearity, as shown in Fig. 17. Over the entire clock frequency range, the amplifier achieves an HD3 better than −100 dB. Fig. 18 shows the measurement over −40 °C to 125 °C temperature with a near-Nyquist input signal. With only a single calibration at room temperature (25 °C), the amplifier maintains an HD3 better than −77 dB over the entire temperature range. Recalibrating the amplifier at different temperatures improves the HD3 to about −100 dB.

The amplifier's input amplitude is swept from 50–200 $mV_{pp,diff}$ with ∼4× gain at both low and

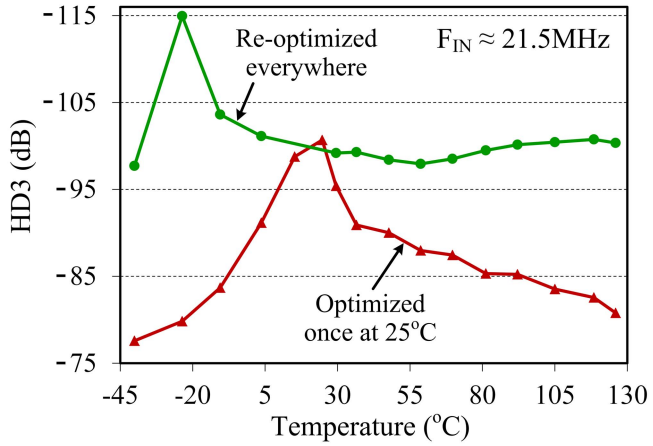

Fig. 18. Measured amplifier linearity over −40 °C to 125 °C temperature.

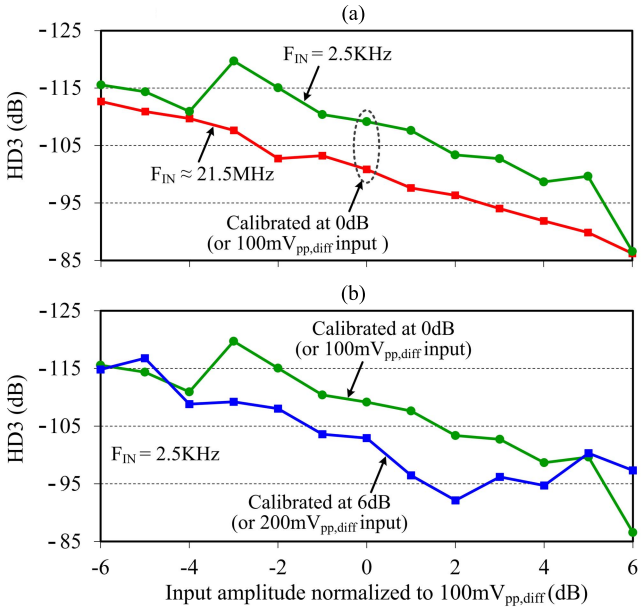

Fig. 19. Measured amplitude sweeps (a) at two input frequencies and (b) while calibrating at two different signal amplitudes.

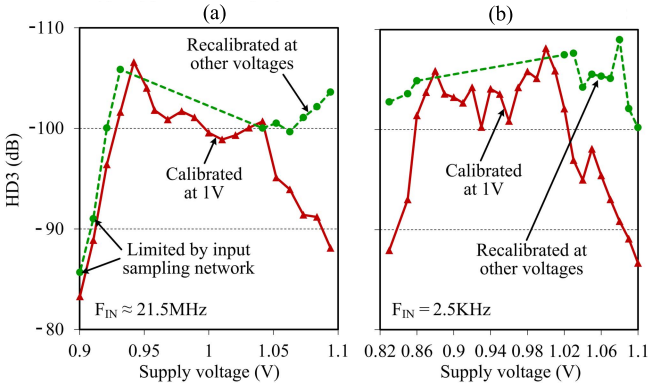

Fig. 20. Supply sweep measurements at (a) near-Nyquist and (b) low-frequency input signals.

near-Nyquist input frequencies, as shown in Fig. 19(a). With a one-time calibration at 100-$mV_{pp,diff}$ input, the amplifier exhibits better than −86-dB HD3 over the entire amplitude range. The degradation in linearity at higher signal amplitudes

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[4]	[5]	[6]	[7]	This work	
Technology	0.18µm	90nm	65nm	0.25µm	28nm	
Clock frequency F_S (MS/s)	60	100	90	100	43	
Load capacitor C_L (pF)	6**	2	7.5	4	7.6	
Amplifier power P_{Amp} (µW)	27400	5760†	14700	12500	87	96
Supply voltage V_{DD} (V)	1.6	1.2	-	2.5	1	
Output signal V_{out} ($V_{pp,diff}$)	1	0.6	1.6	1.8	0.4	0.8
Relative signal swing V_{out}/V_{DD}	0.63	0.5	-	0.72	0.4	0.8
SFDR at Nyquist (dB)	84*	85*	63	80	99	86
Energy-per-cycle P_{Amp}/F_S (pJ)	456	57.6	163	125	2	2.2

*ADC SFDR **ADC input capacitance †Estimated from simulation
Note that P_{Amp} is the power of a single amplifier.

is due to the amplifier's nonlinear output impedance, which cannot be entirely corrected by the proposed linearization technique. Although calibrating the amplifier at 200-$mV_{pp,diff}$ input improves the HD3 to −97 dB (by overcompensating the output impedance nonlinearity), it degrades to −92 dB at 125-$mV_{pp,diff}$ input [Fig. 19(b)]. As a result, the overall performance of the amplifier remains almost the same over the entire amplitude range irrespective of the signal amplitude chosen for calibration.

The supply voltage of the amplifier is varied from 0.9 to 1.1 V with near-Nyquist input, as shown in Fig. 20(a). With a single calibration at 1-V supply, the amplifier exhibits better than −83-dB HD3 over the entire supply range. Calibrating the amplifier at different supply voltages improves the HD3 to −100 dB except when the supply voltage drops below 0.93 V. The degradation is due to the nonlinearity of the input sampling network since the signal acquisition is happening at near-Nyquist frequencies. However, when the supply sweep (0.83 to 1.1 V) is performed at a low-frequency input signal, as shown in Fig. 20(b), the sampling network does not limit the linearity anymore. Therefore, the amplifier exhibits better than −100-dB HD3 even with 0.83-V supply after recalibration.

Table I shows a comparison of this design with other high-linearity amplifiers. Compared to [4]–[7], the proposed amplifier requires 26× less energy per cycle and achieves similar spurious-free dynamic range (SFDR) in spite of supporting the largest load capacitor C_L and relative output swing (V_{out}/V_{DD}). Moreover, even without continuous calibration, the amplifier is quite robust to supply voltage and temperature variations (THD < −77 dB). Compared to the state-of-the-art dynamic amplifiers [3], [14], [15], the proposed amplifier with CDL technique demonstrates 25 dB better linearity while allowing two times larger output swing.

VI. CONCLUSION

A linearization technique based on capacitive degeneration is introduced that can be used with dynamic amplifiers to ensure excellent linearity. Furthermore, a new dynamic amplifier topology is proposed, which uses differential cross-coupled capacitors to reduce their area and enhance the amplifier's CM rejection capability. Nonlinearity is minimized by adjusting the amplifier's bias current to the appropriate level, with negligible power overhead. Fabricated in a 28-nm CMOS process, the proof-of-concept amplifier demonstrates 100-dB linearity up to 150 MS/s sampling speed. Compared to published dynamic amplifier designs, it achieves 25 dB better linearity with twice the output swing. In spite of exhibiting linearity similar to state-of-the-art high-linearity amplifiers, the proposed dynamic amplifier improves the energy per cycle by a factor of 26.

APPENDIX A
MATHEMATICAL ANALYSIS OF CDL TECHNIQUE

During amplification, the drain-to-source current I_{DS} flows through the degeneration capacitor C_{DEG} according to (3) in order to charge it. Therefore, the following equality holds for the positive half circuit of the Fig. 3 amplifier:

$$\begin{aligned} C_{\mathrm{DEG}}\frac{dV_{\mathrm{SP}}}{dt} &= I_{D0}\exp\left(\frac{V_{\mathrm{BN}}+(V_{I,\mathrm{diff}}/2)}{nU_T}\right)\exp\left(\frac{-V_{\mathrm{SP}}}{U_T}\right) \\ \Rightarrow \exp\left(\frac{V_{\mathrm{SP}}}{U_T}\right)\frac{dV_{\mathrm{SP}}}{dt} &= \frac{I_{D0}}{C_{\mathrm{DEG}}}\exp\left(\frac{V_{\mathrm{BN}}+(V_{I,\mathrm{diff}}/2)}{nU_T}\right) \end{aligned} \tag{12}$$

where V_{BN} is the biasing voltage of the NMOS differential pair. Integrating both sides of (12) and re-arranging the

equation results in the following:

$$V_{\mathrm{SP}}(t) = U_T \ln\left(\frac{I_{Q0}t}{C_{\mathrm{DEG}}U_T}\exp\left(\frac{V_{I,\mathrm{diff}}}{2nU_T}\right) + c_1\frac{1}{U_T}\right) \quad (13)$$

where c_1 is an integration constant and $I_{Q0} = I_{D0}\exp(V_{\mathrm{BN}}/nU_T)$ = amplifier's quiescent current at the beginning of the amplification phase ($t = 0$). By using the initial condition of $V_{\mathrm{SP}} = 0$ at $t = 0$, c_1 can be found as U_T. Putting $c_1 = U_T$ in (13) results in

$$V_{\mathrm{SP}}(t) = U_T \ln(1 + \alpha(t)\exp(V_{I,\mathrm{diff}}/2nU_T)) \quad (14)$$

where the factor $\alpha(t)$ is given by

$$\alpha(t) = I_{Q0}t/C_{\mathrm{DEG}}U_T. \quad (15)$$

Similarly for the negative half circuit, the source voltage V_{SN} can be expressed as

$$V_{\mathrm{SN}}(t) = U_T \ln(1 + \alpha(t)\exp(-V_{I,\mathrm{diff}}/2nU_T)). \quad (16)$$

During the amplification period, the amplifier's output signal increases with time as a response to its input step. From (1), the amplifier's transient gain can be written as

$$A(t) = \frac{V_{\mathrm{OP}}(t) - V_{\mathrm{ON}}(t)}{V_{I,\mathrm{diff}}} = \frac{C_{\mathrm{DEG}}}{C_L}\frac{V_{\mathrm{SP}}(t) - V_{\mathrm{SN}}(t)}{V_{I,\mathrm{diff}}}. \quad (17)$$

By substituting (14) and (16) into (17), the gain $A(t)$ can be expressed as

$$A(t) = \frac{C_{\mathrm{DEG}}}{2nC_L} + \frac{C_{\mathrm{DEG}}}{C_L}\frac{U_T}{V_{I,\mathrm{diff}}} \times \ln\left(\frac{\alpha(t) + \exp(-V_{I,\mathrm{diff}}/2nU_T)}{1 + \alpha(t)\exp(-V_{I,\mathrm{diff}}/2nU_T)}\right). \quad (18)$$

From (18), it is clear that if $\alpha(t) = 1$, the second term (i.e., signal dependent) equals to zero and the gain $A(t)$ is independent of the input signal $V_{I,diff}$. This condition is met at time t_{opt} given by (4), which is rewritten as follows:

$$t_{\mathrm{opt}} = C_{\mathrm{DEG}}U_T/I_{Q0}.$$

Using the condition $\alpha(t) = 1$ in (18) results in a linear gain of

$$A(t_{\mathrm{opt}}) = C_{\mathrm{DEG}}/2nC_L$$

where $A(t_{\mathrm{opt}})$ is the transient gain at the optimal time t_{opt}.

APPENDIX B
EFFECT OF SOURCE RESISTANCE ON CDL TECHNIQUE

In this Appendix, the effect of parasitic source resistance $R_{S,\mathrm{par}}$ on the proposed linearization technique is discussed. $R_{S,\mathrm{par}}$ can come from transistor parasitic or from finite ON-resistance of switch that is in series with C_{DEG} capacitor (Fig. 4). It tends to linearize the exponential V–I characteristic of weak-inversion MOSFET, making its transconductance $g_{m,\mathrm{eff}}$ less expanding. As a result, the optimum linear gain $A(t_{\mathrm{opt}})$ slightly reduces, as shown in Fig. 21. However, parasitic source resistance of MOSFET is not that high in practice and also the series switches operate close to the supply or ground. Hence, they can be designed with low ON-resistance ($R_{S,\mathrm{par}} \ll 1/g_{m,\mathrm{eff}}$), making their effect negligible.

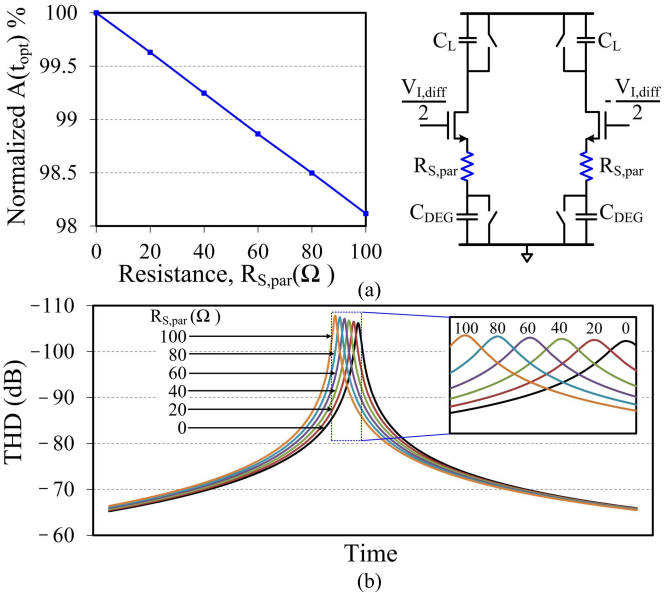

Fig. 21. Simulation results to show the effect of source resistance $R_{S,\mathrm{par}}$ on the amplifier's (a) optimum gain $A(t_{\mathrm{opt}})$ normalized to that when $R_{S,\mathrm{par}} = 0$ and (b) linearity.

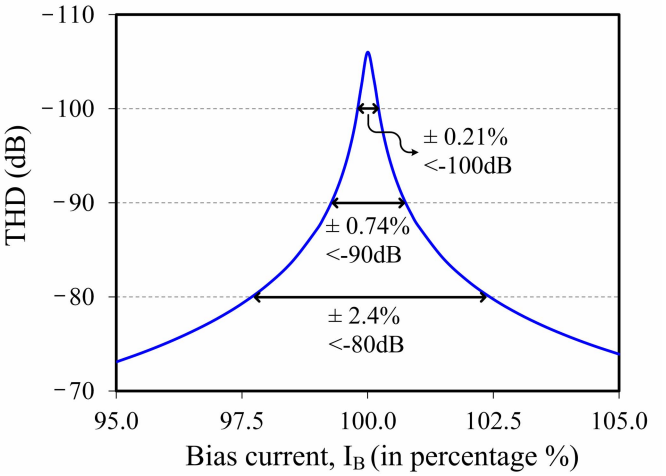

Fig. 22. Simulated THD as a function of bias current (in percentage).

APPENDIX C
SIMULATION RESULTS

Fig. 22 shows the results of a simulation in which the bias current is swept and THD is plotted as a function of bias current. The shape of the curve as well as the absolute THD corresponds well with measurement results (Fig. 13). The required tuning range of the biasing circuit depends on its implementation and the desired amplifier accuracy. For the current bias design, a THD < -77 dB is measured with a single calibration over $\pm 10\%$ supply voltage and -40 °C to 125 °C temperature variation. A 3-bit coarse and 5-bit fine current DAC should be sufficient to achieve a THD around -100 dB over PVT. A smaller tuning range and less THD variation can be achieved by implementing a constant-g_m biasing circuit, which automatically adjusts the bias current over PVT to keep the g_m constant.

Fig. 23 shows the simulated noise spectrum at the output of the LPF. At 20-kHz frequency, simulated output noise density

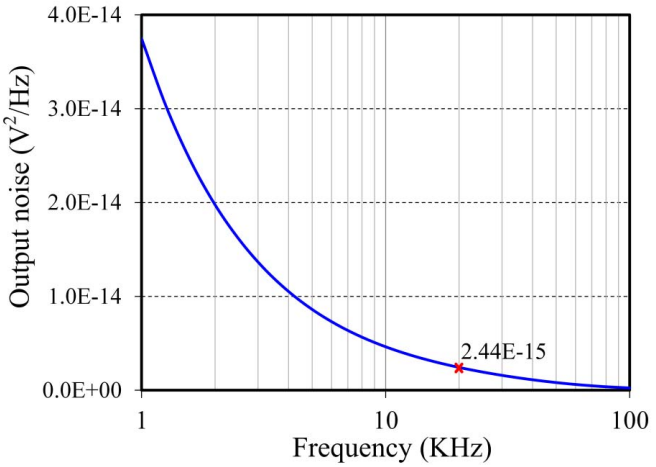

Fig. 23. Simulated noise spectrum at the output of the LPF.

is 2.44E−15 V^2/Hz or 49.4 nV/$\sqrt{\text{Hz}}$, which corresponds well with the measured noise density of 57 nV/$\sqrt{\text{Hz}}$ at the same frequency.

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