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Interdigitated-back-contacted silicon heterojunction solar cells featuring novel MoO_x-based contact stacks

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Abstract

The fabrication process of interdigitated-back-contacted silicon heterojunction (IBC-SHJ) solar cells has been significantly simplified with the development of the so-called tunnel-IBC architecture. This architecture utilizes a highly conductive (*p*)-type nanocrystalline silicon (nc-Si:H) layer deposited over the full substrate area comprising pre-patterned (*n*)-type nc-Si:H fingers. In this context, the (*p*)-type nc-Si:H layer is referred to as *blanket* layer. As both electrodes are connected to the same blanket layer, the high lateral conductivity of (*p*)nc-Si:H layer can potentially lead to relatively low shunt resistance in the device, thus limiting the performance of such solar cells. To overcome such limitation, we introduce a thin (<2 nm) full-area molybdenum oxide (MoO_x) layer as an alternative to the (*p*)nc-Si:H blanket layer. We demonstrate that the use of such a thin MoO_x minimizes the shunting losses thanks to its low lateral conductivity while preserving the simplified fabrication process. In this process, a novel (*n*)-type nc-Si:H/MoO_x electron collection contact stack is implemented within the proposed solar cell architecture. We assess its transport mechanisms via electrical simulations showing that electron transport, unlike in the case of tunnel-IBC, occurs in the conduction band fully. Moreover, the proposed contact stack is evaluated in terms of contact resistivity and integrated into a proof-of-concept front/back-contacted (FBC) SHJ solar cells. Contact resistivity as low as 100 $m\Omega cm^2$ is achieved, and fabricated FBC-SHJ solar cells obtain a fill factor above 81.5% and open-circuit voltage above 705 mV. Lastly, the IBC-SHJ solar cells featuring the MoO_x blanket layer are fabricated, exhibiting efficiencies up to 21.14% with high shunt resistances above 150 $k\Omega cm^2$. Further optimizations in terms of layer properties and fabrication process are proposed to improve device performance and realize the efficiency potential of our novel IBC-SHJ solar cell architecture.

KEYWORDS
interdigitated-back-contacted solar cells, MoOx blanket layer, silicon heterojunction solar cells, simple processing

1 | INTRODUCTION

Crystalline silicon (c-Si) silicon heterojunction (SHJ) solar cells have achieved the highest single junction photoconversion efficiency, reaching 26.81%.[1] The excellent performance of SHJ devices results from the use of carrier selective passivating contacts based on (i) thin intrinsic hydrogenated amorphous silicon (a-Si:H), which ensures good passivation quality,[2] and (ii) doped hydrogenated nanocrystalline silicon (nc-Si:H)-based layers, which enable efficient selective transport of charge carriers.[1,3–7] Such solar cells demonstrated high open-circuit voltages (V_{OC}) above 750 mV.[1,8–10] While the record efficiency has been achieved in front/back-contacted (FBC) architecture, the short-circuit current density (J_{SC}) could be higher. In fact, the shading from the metal grid and the parasitic absorption induced by the silicon-based layers and the transparent conductive oxide (TCO) layer[11] at the front side are unvoidable limiting factors. Alternatively, in interdigitated-back-contacted (IBC) configuration, as both charge carriers are collected on the rear side of the device, the front contact stack can be developed to minimize optical losses, thus obtaining a higher J_{SC}.[10,12,13] With such architecture, efficiencies up to 26.7%[13] were achieved with a J_{SC} of 42.65 mA/cm^2,[13,14] which is significantly higher as compared to the 41.45 mA/cm^2 demonstrated in the record FBC-SHJ solar cell.[1] However, the fabrication of IBC-SHJ solar cells comes with increased complexity compared to FBC-SHJ solar cells due to the need to pattern the contact stacks on the rear side. Aiming to simplify the fabrication process and develop IBC-SHJ solar cells that are more industry-appealing, Tomasi et al.[15] introduced the so-called tunnel-IBC architecture. This process reduces the fabrication steps by introducing the formation of self-aligned contacts. Specifically, following the deposition of pre-patterned (*n*)nc-Si:H, (*p*)nc-Si:H is deposited on the full rear area as a blanket layer. Hole collection takes place through the (*p*)nc-Si:H layer, while electron collection occurs through the tunneling recombination junction formed by (*n*)nc-Si:H and (*p*)nc-Si:H stack.[15] The implementation of this device architecture facilitates lower fabrication costs while still enabling efficiencies of up to 25%.[16] In such devices, a highly conductive (*p*)nc-Si:H layer contacts both electrodes, which can potentially lead to lower shunt resistance in the solar cell, resulting in deteriorated FF.[15]

To overcome this limitation while maintaining a simple fabrication process, we present a novel IBC-SHJ solar cell architecture that features molybdenum oxide (MoO_x)-based contact stacks for the collection of both types of charge carriers. MoO_x is selected because it is characterized by lower lateral conductivity compared to (*p*)nc-Si:H.[17–19] In the proposed architecture shown in Figure 1A, a thin (<2 nm) MoO_x layer is deposited as a blanket layer on the full rear side of the device on a pre-patterned (*n*)nc-Si:H layer. In this novel architecture, holes are collected through the (*i*)a-Si:H/MoO_x/TCO stack, and electron collection occurs through the (*i*)a-Si:H/(*n*)nc-Si:H/MoO_x/TCO stack.

While MoO_x is a hole transport layer that is increasingly implemented in combination with SHJ technology,[18,20–25] this study introduces and focuses on the implementation of the proposed novel MoO_x-based electron collection layer stack in proof-of-concept FBC- and IBC-SHJ solar cells. Firstly, the proposed electron collection stack is analyzed through TCAD Sentaurus simulations[26] to gain a comprehensive understanding of the transport mechanism of electrons through this layer stack. Then, the contact resistivity of the proposed electron collection stack is evaluated, and the performance of FBC-SHJ solar cells endowed with this electron collection stack is assessed and optimized. Lastly, the IBC-SHJ solar cells featuring the MoO_x blanket layer are fabricated and characterized.

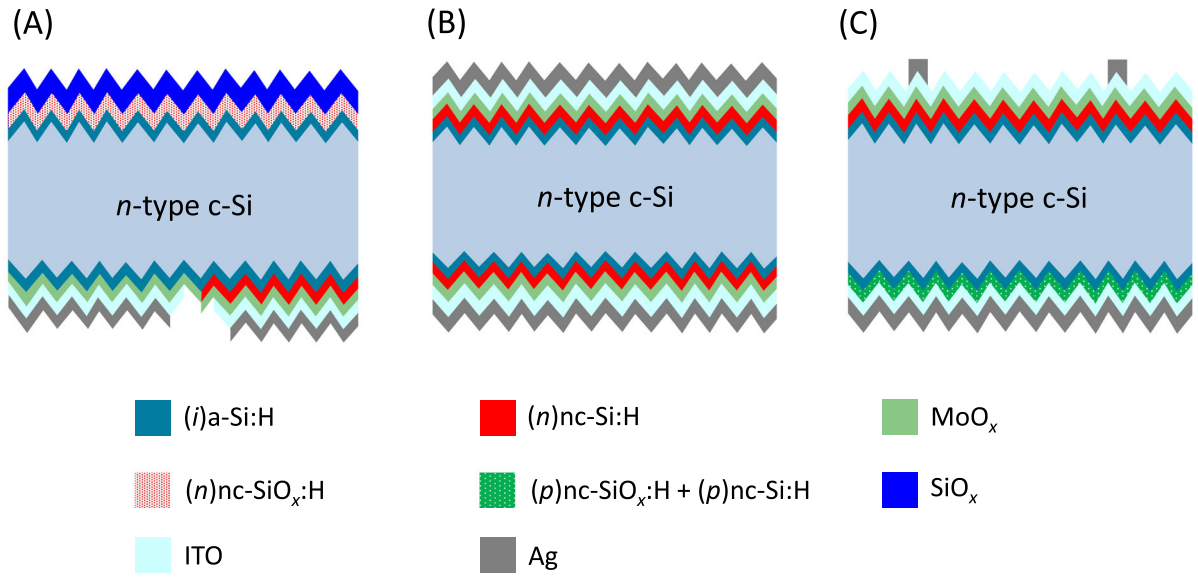


FIGURE 1 Schematic representation of (A) IBC-SHJ solar cell with full area MoO_x on the rear side, (B) symmetric contact resistivity sample, and (C) FBC-SHJ solar cell with MoO_x as a part of electron collection contact stack on the front side.

2 | METHODOLOGY

To evaluate charge transfer in the novel (*i*)a-Si:H/(*n*)nc-Si:H/MoO_x/TCO contact stack and to gain a comprehensive understanding of its working principle, we carried out numerical simulations using TCAD Sentaurus software by Synopsys Inc.[26] More details about the simulation methods can be found in our previous publications.[27,28]

Passing to experiments, we fabricated contact resistivity test samples, as well as FBC and IBC solar cells as presented in Figure 1. Contact resistivity samples (Figure 1B) and FBC solar cells (Figure 1C) were fabricated to evaluate the performance of the novel electron collection contact stack independently before the integration into IBC solar cells (Figure 1A). For the fabrication of all samples, we used (*n*)-type Topsil float-zone (FZ) <100> c-Si wafers with thicknesses of 280 ± 20 μm and resistivities of 3 ± 2 Ωcm. Firstly, the wafers underwent texturing to achieve a random distribution of pyramids. The texturing process was carried out using a diluted tetramethylammonium hydroxide (TMAH) solution with ALKA-TEX additive.[29] Subsequently, the wafers were cleaned using room-temperature 99% nitric acid (HNO_3), 110°C 69.5% HNO_3, and, finally, 0.55% hydrofluoric acid (HF).[30]

After the cleaning, wafers were loaded into a multi-chamber plasma-enhanced chemical vapor deposition (PECVD) tool (Elettrorava S.p.A.) to deposit thin-film silicon layers. In the case of FBC solar cells, we first deposited (*i*)a-Si:H/(*n*)nc-Si:H layer stack. Then, with a brief vacuum break, the wafers were flipped and reloaded into the tool for the deposition of (*p*)-contact layer stack. In the case of contact resistivity samples, the symmetric structure was deposited on both sides of the wafer. The deposition conditions for (*i*)a-Si:H layer and (*p*)-type layer stack are described in previous studies,[17,31] respectively, while Table S1 shows the deposition conditions and electrical properties (measured in-house prior to contact resistivity sample and solar cell fabrication) of (*n*)nc-Si:H layers with different thicknesses. During the PECVD process, additional plasma treatments were optionally introduced to the layer stack before the deposition of MoO_x as described in.[24,25] Two treatment conditions are here discussed: *plasma treatment without doping* (PT), which involves a precursor gas mixture consisting of SiH_4, H_2, and CO_2, and *plasma treatment with boron* (PTB), which additionally includes B_2H_6.[24,25] The presence of SiH_4 in the gas mixture leads to the growth of a thin interfacial oxidic Si-rich layer. The controlled growth of this oxidic layer through plasma treatments ensures the contained reaction of MoO_x with the substrate and enables preserving stoichiometry of MoO_x. These plasma treatments were initially developed for the MoO_x hole collection contact stack. The treatments are directly introduced into the electron collection stack without adjustments and the possible effect of the treatments on electron collection is briefly discussed in Sections 3.1 and 3.2. Following the PECVD steps, MoO_x layers were thermally evaporated at a base pressure of 5.0×10^{-6} mbar from a stoichiometric MoO_3 powder source (Sigma-Aldrich) at a deposition rate of about 0.1 nm/s. Then, room-temperature tin-doped indium oxide (ITO) was deposited in a radio-frequency (RF) magnetron sputtering tool (Polyteknik AS) through a metal mask defining five solar cells or six samples per wafer for FBC solar cells or contact resistivity samples, respectively. The thicknesses of ITO layers in FBC solar cells were 75 and 150 nm for the front and the rear side, respectively, and 75 nm for contact resistivity samples. The samples with as-deposited ITO were annealed in air at 180°C for 5 min. Lastly, FBC-SHJ cells were screen-printed with Ag paste and cured in an air environment at 170°C for 40 min. The solar cells have a designated area of 3.86 cm^2. Contact resistivity samples were metalized with evaporated Ag and have the same area as the FBC solar cells.

As for the IBC solar cells, the order of deposition and patterning steps is shown in Figure 2. Firstly, (*i*)a-Si:H passivation layers were deposited symmetrically on both sides of the wafer and (*n*)nc-SiO_x:H was deposited on the front side of the cell precursors as a front surface field (FSF) (see Figure 2A). This was followed by the deposition of 800-nm- and 1600-nm-thick SiO_x layers on the front and rear side, respectively, in the Plasmalab 80 Plus PECVD tool (Oxford

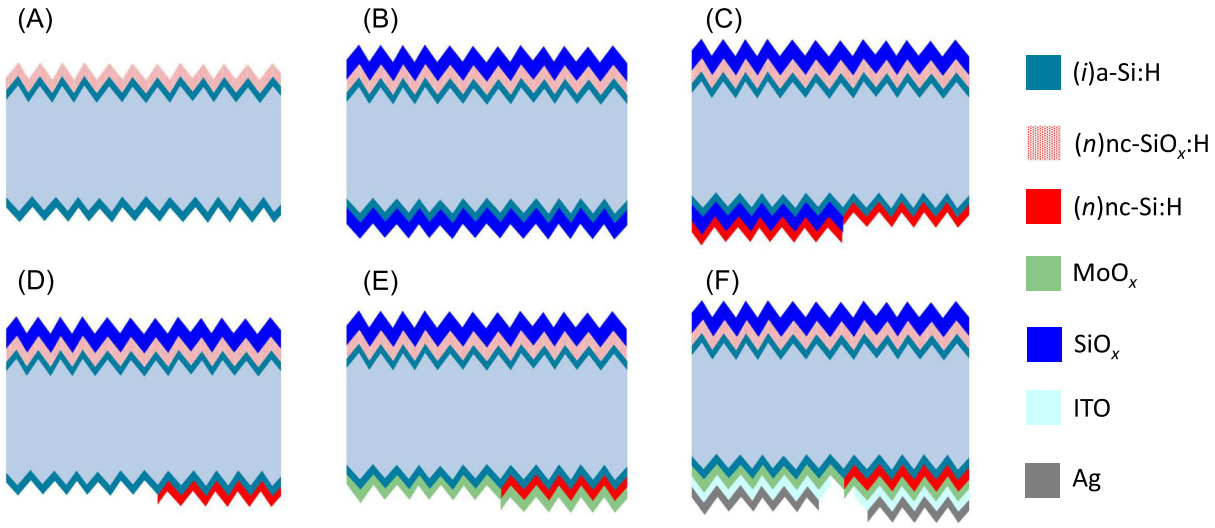


FIGURE 2 Schematic representation of fabrication process of IBC-SHJ solar cell with MoO_x.

Instruments plc) shown in Figure 2B. SiO_x layer in IBC solar cells serves as a sacrificial layer for etching steps on the rear side and, on the front side, as a protective layer for passivation layers and an anti-reflection coating (ARC). It should be noted that before each following PECVD (Elettrorava S.p.A.) step, the wafers are dipped in 0.55% HF solution for the removal of the native oxide layer from the rear side. Only during these native oxide removal steps, the front side of the wafer is not protected, and part of the front side SiO_x is removed. Hence, the final thickness of the front SiO_x in the finished solar cell is expected to be about 100 nm. After the SiO_x deposition, the rear side of the device was patterned using photolithography and 7:1 buffered hydrofluoric (BHF) acid solution to remove SiO_x layer from the electron collection region. During the patterning of the rear SiO_x, the front SiO_x is protected with photoresist to ensure this layer is preserved. The patterning is followed by full-area (*n*)nc-Si:H layer deposition shown in Figure 2C. Then, the second photolithography step and 1% room-temperature potassium hydroxide (KOH) etching solution were utilized to remove (*n*)nc-Si:H layer from the hole collection region. This was followed by the removal of SiO_x from the hole collection region using BHF solution (see Figure 2D) during which the front SiO_x layer is again protected by photoresist. Next, the samples were again loaded into the PECVD chamber for plasma treatments, as discussed in our previous publications.[24,25] Full-area MoO_x layer was evaporated as shown in Figure 2E, and, afterward, a 150-nm-thick room-temperature ITO layer was also deposited on the full area. Cell precursors were then annealed at 180°C for 5 minutes, and the ITO layer was patterned using photolithography and etched in 37% hydrochloric (HCl) acid solution. Eventually, another photolithography step was introduced prior to the evaporation of 2-µm-thick Ag, followed by Ag lift-off in acetone solution (see Figure 2F). Seven IBC solar cells were fabricated per wafer—three with a designated area of 4.05 cm^2 and 300 µm pitch size and two with areas and pitch sizes of 4.09 cm^2 and 650 µm and 4.19 cm^2 and 1200 µm. Solar cell area is defined by a measurement mask placed on the front side of the wafer and corresponds to the solar cell area on the back side, excluding the busbars.

During the fabrication process of solar cells, we conducted measurements of the effective carrier lifetime (τ_{eff}) of the cell precursors after every deposition, patterning, or annealing step. These measurements were performed using the Sinton WCT-120 instrument with either transient photoconductance decay mode or quasi-steady-state photoconductance mode.[32,33] The current–voltage (I–V) characteristics of the completed solar cells were evaluated using a AAA class Wacom WSX-90S-L2 solar simulator under standard test conditions and calibrated with reference solar cells validated at Fraunhofer ISE CalLab. To determine the series resistance of the solar cells, we obtained the pseudo-fill factor (pFF) using the Sinton Instruments Suns-V_{OC}-150 Illumination-Voltage Tester.[34] The same Suns-V_{OC} setup was used to measure solar cells' shunt resistance. Lastly, we calculate contact resistivity (ρ_c) from a dark I–V curve that is used to extract the total resistance of the sample, as discussed in our previous work.[17] From the total resistance of the sample, bulk components of all involved layers can be subtracted, leaving the ρ_c as the final contribution. As the TCO/Ag interface ρ_c is negligible compared to total ρ_c, we assume that the ρ_c values represent the contacts from c-Si to TCO.[35]

3 | RESULTS AND DISCUSSION

3.1 | Transport mechanism in electron collection contact stack

In the proposed solar cell structure, MoO_x is part of the novel electron collection contact stack together with (*n*)nc-Si:H (see Figure 1A). Figure 3A shows the band diagram in equilibrium of this contact stack

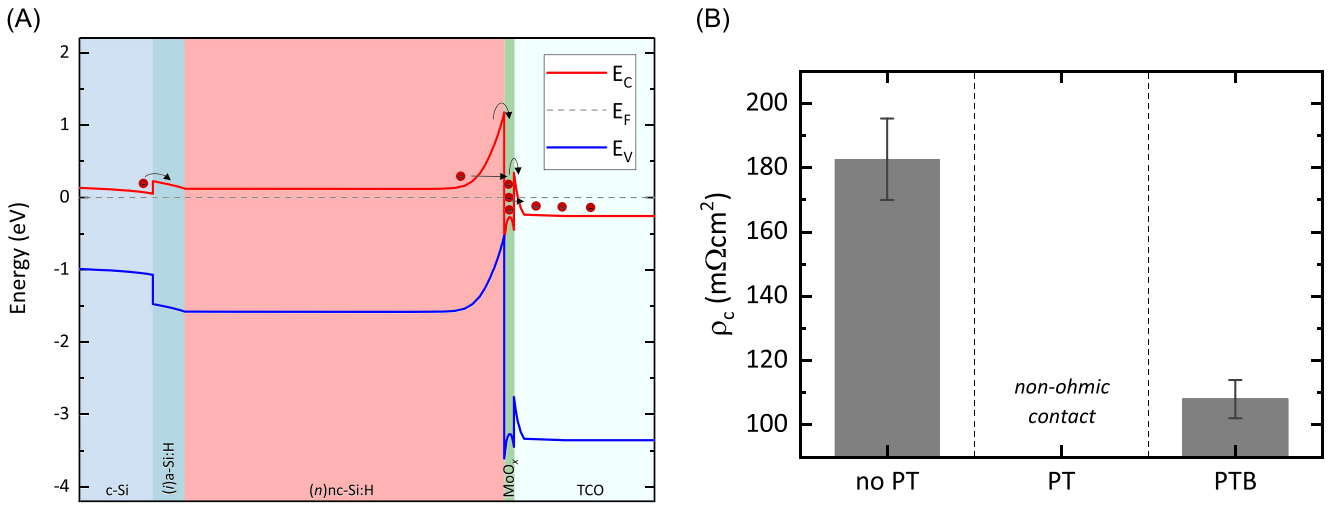


FIGURE 3 (A) Band diagram of electron transport layer stack featuring (*n*)nc-Si:H/MoO_x contact. Conduction and valence bands are shown in solid red and blue lines, respectively. The transport of electrons (red circles) is exemplified by the black arrows. (B) Contact resistivity (ρ_c) of 20-nm-thick (*n*)nc-Si:H/1.7-nm-thick MoO_x stack without plasma treatment (no PT), with plasma treatment (PT), and with plasma treatment with boron (PTB). The average values and error bars are based on six samples from one wafer. Samples with PT are characterized by non-ohmic contact behavior.

derived from the TCAD Sentaurus simulation. The band diagram shows a conduction band bending at c-Si towards (*i*)a-Si:H, inducing the electron accumulation at the c-Si/(*i*)a-Si:H interface. Electrons can cross through the energy barrier at c-Si/(*i*)a-Si:H heterointerface into (*n*)nc-Si:H toward MoO_x. Due to the arrangement of the charge at MoO_x influenced by (*n*)nc-Si:H and TCO, the Fermi energy is above the conduction band energy, indicating a large population of electrons accumulated in MoO_x. Such charge accumulation facilitates the transport of electrons from (*n*)nc-Si:H to MoO_x. Then, electrons cross toward TCO and finally to the metal electrode. Note that the electron transport occurs solely in the conduction band as MoO_x behaves like (*n*)-type material.[36] Therefore, the charge transfer processes occurring at heterointerfaces are thermionic emission and direct tunneling.[27]

It should be noted that due to the high work function (WF) of MoO_x[37] together with the relatively low WF of (*n*)nc-Si:H layer, an energy barrier is formed at (*n*)nc-Si:H/MoO_x interface that charge carriers (electrons) must cross over or tunnel through. To mitigate the effect of such an energy barrier, we focus on the properties of (*n*)nc-Si:H, particularly its activation energy (E_a). We choose (*n*)nc-Si:H because it exhibits lower E_a compared to (*n*)a-Si:H.[4,7,38] The relatively low E_a in silicon nanocrystalline materials is achieved thanks to the higher doping efficiency coming from the crystalline phase embedded in the amorphous matrix.[39] Moreover, thicker (*n*)nc-Si:H layers exhibit lower E_a due to the higher crystalline fraction.[38,40] Thus, we aim to use 20-nm- and 50-nm-thick (*n*)nc-Si:H layers to achieve efficient electron collection in the fabricated solar cell. Additionally, we optionally apply plasma treatments to the election collection contact stack after (*n*)nc-Si:H. As these plasma treatments are developed in nanocrystalline plasma regime,[17,24,25] the crystallinity (*n*)nc-Si:H may influence subsequent growth of such treatments,[15,40] which may have an impact on the transport of electrons. As the plasma treatments originate from the previous work on MoO_x-based hole collection contact stack,[24,25] a detailed study on understanding the role and character of plasma treatments in electron collection contact stack is still ongoing.

3.2 | Experimental results

3.2.1 | Contact resistivity study of electron collection contact stack

Figure 1B shows the sketch of symmetrical samples fabricated to evaluate ρ_c of the MoO_x-based electron collection contact stack and to investigate the effect of plasma treatments on ρ_c. The layer stack implemented in the symmetric structure is the same as applied in solar cells (see Figure 1).

We fixed the thickness of (*n*)nc-Si:H to 20 nm and MoO_x to 1.7 nm while fabricating symmetric samples without PT, with PT, and with PTB. The results of the contact resistivity study are displayed in Figure 3B. In the case of PT samples, we observe non-ohmic contact behavior measured in dark I–V measurement. This can be related to the intrinsic character of the treatment, which potentially leads to the growth of a thin intrinsic layer, which then can hinder charge transfer between (*n*)nc-Si:H and MoO_x. Looking at ρ_c values of the samples without PT and with PTB, we observe an average drop of 75 $m\Omega cm^2$ when introducing PTB with average ρ_c decreasing from 183 to 108 $m\Omega cm^2$. These values are comparable to other reported contact resistivities in (*n*)-type contacts for SHJ solar cells,[41] while reduced ρ_c with the introduction of PTB was also observed in the MoO_x-based hole collection stack reported by Cao et al.[24] This beneficial effect can be related to the preserved WF of MoO_x by the introduction of PTB, as discussed in literature.[24] Further investigation is necessary to obtain a comprehensive understanding of the effect of PTB and preserved WF of MoO_x on electron transport. Still, the results of contact resistivity study showed the overall low contact resistivity of the studied contact stack and the positive effect of the introduction of PTB.

3.2.2 | Proof-of-concept FBC-SHJ solar cells

To evaluate the performance of the proposed electron collection contact stack in solar cells, we fabricated rear junction FBC-SHJ solar cells (see Figure 1C), which feature (*n*)nc-Si:H/MoO_x stack and varied plasma treatments on the front side. Additionally, we compared the performance of solar cells with 20-nm- and 50-nm-thick (*n*)nc-Si:H layers. On the rear side of the devices, our laboratory standard (*p*)-type contact stack[17] was deposited to assess the performance of the front contact stack independently. For the evaluation of solar cell performance and comparison of different stacks, we present in Figure 4 the V_{OC}, FF, pFF, and $R_{s,SunsVoc}$ of solar cells.

As presented in Figure 4, by introducing PT to solar cells with 20-nm-thick (*n*)nc-Si:H, both V_{OC} and FF exhibit significant drops compared to cells without PT. The degradation in FF originates from a significant increase of an average $R_{s,SunsVoc}$ from 1780 to 2968 $m\Omega cm^2$, and it is in good agreement with previous contact resistivity study where samples with PT exhibit non-ohmic contact behavior (see Figure 3B). By introducing PTB, an average gain in FF of $4.5\%_{abs}$ compared to the device without treatment is observed. The improved FF is a result of a decrease in $R_{s,SunsVoc}$ from an average of 1780 $m\Omega cm^2$ to an average of 867 $m\Omega cm^2$, and it is in agreement with contact resistivity results where samples with PTB observed decreased ρ_c (see Figure 3B). The reason behind FF gain and the effect of PTB on the transport of electrons is still under investigation. Simultaneously, V_{OC} exhibits a moderate drop of 5 mV on average, possibly due to the additional processing steps for the plasma treatment. Overall, the results of solar cells align with the previous contact resistivity study and show an overall positive influence, especially enabling a significant gain of FF, by implementing the PTB in the proposed electron collection contact stack.

As for solar cells with a 50-nm-thick (*n*)nc-Si:H layer (see Figure 4), we observe simultaneous gains in V_{OC} and FF when introducing PT and further improvements with PTB. The average FF of solar cells with PTB increases up to 80.7%, with the highest achieved FF of 81.56%, representing a gain of $2.5\%_{abs}$ compared to solar cells without PT. This is a result of lower series resistance of 1057 $m\Omega cm^2$, as well as slightly higher pFF for cells with PTB as compared to

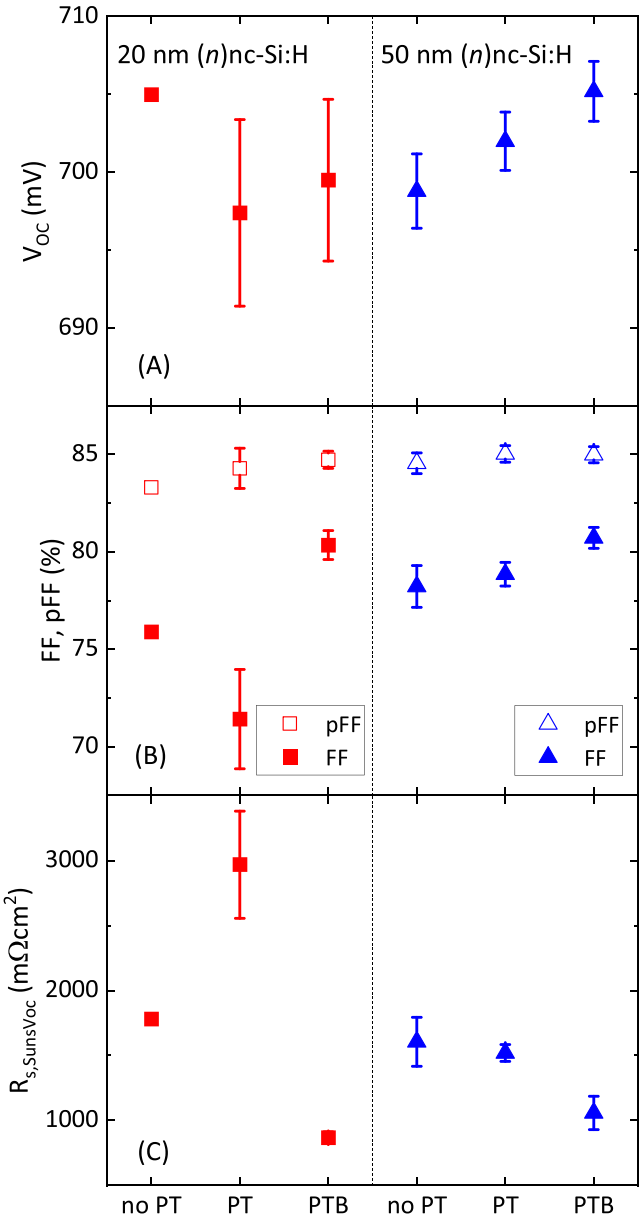


FIGURE 4 (A) V_{OC}, (B) FF and pFF, and (C) $R_{s,SunsVoc}$ of FBC-SHJ solar cells with (*n*)nc-Si:H/MoO_x contact stack with 20-nm- and 50-nm-thick (*n*)nc-Si:H layer and varied plasma treatment conditions. The average values and error bars are based on five solar cells from one wafer for all points apart from the samples with 20-nm-thick (*n*)nc-Si:H without PT and with PTB. 20-nm-thick (*n*)nc-Si:H without PT represents results from a single solar cell, whereas 20-nm-thick (*n*)nc-Si:H with PTB represents 10 solar cells from two wafers.

devices without PT. The highest average V_{OC} of 705.2 mV is also observed when introducing 50-nm-thick (*n*)nc-Si:H and PTB. Unlike the case of 20-nm-thick (*n*)nc-Si:H, the V_{OC} increases when introducing both plasma treatments in the stack with 50-nm-thick (*n*)nc-Si:H. This can be related to the potentially lower impact of plasma treatment on passivation quality if introduced on top of a thicker (*n*)nc-Si:H layer. Similarly, the introduction of PT to the contact stack with 50-nm-thick (*n*)nc-Si:H does not harm the $R_{s,SunsVoc}$ and FF. Simultaneously, devices with a thicker (*n*)nc-Si:H and the same treatment conditions show overall better performance over their thinner counterparts. This can be supported by the improved charge transport through the contact stack due to the lower activation energy of thicker (*n*)nc-Si:H layers, as discussed in Section 3.1. Lastly, it appears that PTB relaxes the requirements for the thickness of (*n*)nc-Si:H, as we can obtain comparable FF with 20-nm-thick and 50-nm-thick (*n*)nc-Si:H when introducing PTB.

3.2.3 | IBC-SHJ solar cells

As FBC-SHJ solar cells with 50-nm-thick (*n*)nc-Si:H demonstrated higher V_{OC} compared to the case of 20 nm while also obtaining high FF, we selected a 50-nm-thick layer to fabricate IBC-SHJ solar cells as sketched in Figure 1A. External parameters are shown in Figure 5, representing results from two processing runs before and after the fine-tuning of the fabrication process for variable pitch size. When discussing process optimization, we mainly refer to the optimization of patterning steps, which are addressed in more detail in Section 2 of the Supporting Information. Solar cells from the unoptimized run were fabricated with PT, while the ones completed with the optimized processing conditions contain PTB instead. This was a pivotal variation, as suggested by the results of the contact resistivity study and FBC-SHJ solar cells, as well as our previous results on the MoO_x hole collection contact stack.[24] Moreover, to further justify the advantage of using PTB, in Section 3 of the Supporting Information, we compare the results of IBC solar cells without PT and with PT and PTB in the intermediate optimization step.

The results from the unoptimized run show improvements in V_{OC}, FF, and, ultimately, the efficiency as the pitch size increases. The V_{OC} and FF increase from an average of 493.5 mV and 63.83% for cells with 300 µm pitch size, respectively, up to 535 mV and 67.88% for cells with 1200 µm pitch size. As a result, we observe an overall efficiency improvement of $1.85\%_{abs}$ on average from 10.75% to 12.60% for an increasing pitch size. Theoretically, a smaller pitch size works in favor of device performance as resistive losses can be reduced.[28] However, experimental results show opposite trends, which can be related to the unprecise patterning and additional defects forming at the gap between electron and hole collecting regions. Specifically, with decreased pitch size, the gap-to-area ratio across a single solar cell increases; thus, the defects at the gap have a stronger influence on final device performance.[42] Additionally, we suspect that (*i*)a-Si:H layer is damaged due to unprecise patterning and larger gap opening during wet chemical etching steps, leading to passivation loss. Detailed evidence on patterning problems and optimization is included in Section 2 of the Supporting Information.

After the optimization of the fabrication process and related patterning steps, there are no visible trends with changing pitch size, indicating that charge collection regions and a gap between them are sufficiently well structured for all pitch sizes (see Figure 5). In addition to the process optimizations, the implementation of PTB enabled the fabricated IBC-SHJ solar cells to feature overall improved J–V parameters. Specifically, these optimized solar cells show an average

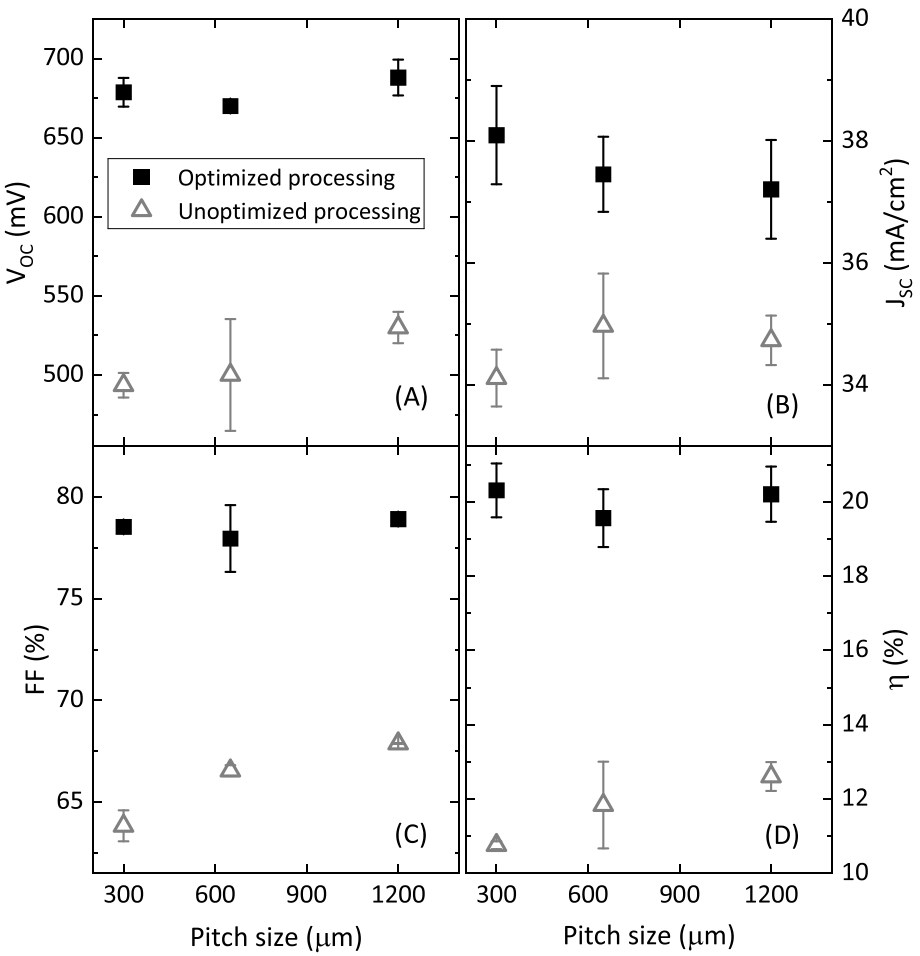
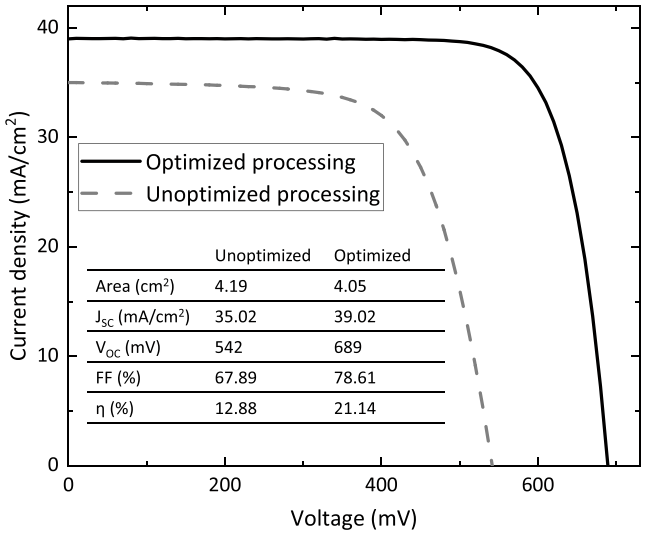


FIGURE 5 External J–V parameters of fabricated IBC-SHJ solar cells with MoO_x blanket layer fabricated during unoptimized (gray triangles) and optimized (black squares) processing conditions. The average values and error bars are based on two cells for 650 and 1200 μm pitch sizes and 3 cells for 300 μm pitch size. All seven cells from the unoptimized processing run are fabricated on the same wafer, whereas the results of the seven cells from the optimized processing run are from two wafers.



	Unoptimized	Optimized
Area (cm^2)	4.19	4.05
J_{SC} (mA/cm^2)	35.02	39.02
V_{OC} (mV)	542	689
FF (%)	67.89	78.61
η (%)	12.88	21.14

FIGURE 6 J–V curves and solar cell parameters of best unoptimized and optimized IBC-SHJ solar cells with MoO_x blanket layer.

efficiency of 20.06%, an FF exceeding 78%, a V_{OC} above 650 mV, and a J_{SC} exceeding 37 mA/cm^2 across various pitch sizes (see Figure 5). The champion solar cell reaches a J_{SC} of 39.02 mA/cm^2, a V_{OC} of 689 mV, an FF of 78.61%, and a conversion efficiency of 21.14% (see Figure 6). The champion solar cell has an area of 4.05 cm^2 and features a pitch size of 300 μm. Aside from the conversion efficiency, we measured pFF above 82%, signifying good junction quality in the device,[43] shunt resistance above 150 kΩcm^2, and calculated $R_{s,SunsVoc}$ of 789 mΩcm^2. Obtained shunt resistance values are comparable to our lab standard 23.71% efficient FBC-SHJ solar cells,[31,44] indicating a shunt-free IBC solar cell.

Compared to the best solar cell from the unoptimized run, the champion device gained 8.26%$_{abs}$ in efficiency mainly due to significant improvements of 147 mV in V_{OC} and 10.72%$_{abs}$ in FF. Moreover, enhancements in both series and shunt resistance can be observed by comparing two J–V curves in Figure 6. As previously discussed, these improvements can be attributed to the optimization of photolithography steps, which enabled precise rear-side patterning and, therefore, preserved passivation quality throughout device fabrication, as well as the introduction of PTB. Further fine-tuning of patterning steps is expected to additionally improve the device performance in terms of V_{OC} and FF. Besides, exploring alternative plasma treatments suited to achieve an optimized collection of both electrons and holes and evaluating the influence of MoO_x thickness in the proposed IBC-SHJ architecture could further benefit device performance. In addition, although we managed to decrease E_a by increasing the thickness of (n)

nc-Si:H layer (see Table S1), we measured relatively high E_a values for these (*n*)nc-Si:H layers compared to our previous publications.[38] This could be related to the variability of processing conditions of our PECVD. Hence, fine-tuning the electrical properties of (*n*)nc-Si:H layer, especially the E_a, is expected to improve charge transfer in the device, as discussed in Section 3.1, and lead to a boost in the FF of solar cells. We also expect additional improvement in FF by introducing copper electroplated electrodes, as this method enables thicker deposition of metal fingers, thus ensuring lower series resistance.[45] Moreover, in comparison to the initial (unoptimized processing) run, we note a 4 mA/cm^2 improvement in J_{SC} when processing was improved. This enhancement in Jsc can be attributed to an improved collection of charge carriers, primarily stemming from preserved passivation, as evidenced by the improved V_{OC}. However, J_{SC} is still limited mainly due to the unoptimized ARC on the illuminated side (approximately 100 nm of SiO_x on top of 8-nm-thick (*n*)nc-SiO_x:H FSF in current devices). This is expected to be improved through careful selection of the FSF layer in combination with SiN_x ARC[15,46,47] or additionally implementing double-layer ARC.[42,48] With the proposed improvements, we expect J_{SC} to increase up to 41 mA/cm^2,[42,46] V_{OC} to reach our laboratory standard FBC-SHJ solar cell V_{OC} (above 725 mV),[44] and FF to get closer to pFF with values around 82% (or even higher pFF due to improved passivation quality and enhanced collection of charge carriers), therefore leading to efficiencies well above 24% in future experiments.

4 | CONCLUSION

In this work, we present the development of IBC-SHJ solar cells with a MoO_x blanket layer aiming to simultaneously enable simplified device processing and high shunt resistance in the solar cell. In the proposed device architecture, hole collection takes place through (*i*)a-Si:H/MoO_x/TCO stack, while electrons are collected through a novel layer stack consisting of (*i*)a-Si:H/(*n*)nc-Si:H/MoO_x/TCO. Results of numerical simulations indicate that electron transfer in the novel contact stack occurs in the conduction band via thermionic emission and direct tunneling unlike in the case of previously reported tunnel-IBC solar cells. We evaluated and optimized the proposed electron collection contact stack in terms of contact resistivity and solar cell performance, along with optionally applied plasma treatments (PT or PTB). We obtained contact resistivities as low as 100 mΩcm^2 when introducing PTB before the deposition of MoO_x on top of the 20-nm-thick (*n*)nc-Si:H layer. Further, we fabricated proof-of-concept FBC-SHJ solar cells to assess the effects of plasma treatments and (*n*)nc-Si:H thickness on the solar cell performance. Overall, solar cells with a thicker (*n*)nc-Si:H layer (50 nm) and additional PTB featured better V_{OC} and FF, which agrees well with the results of the contact resistivity study. The FBC-SHJ solar cell that features 50-nm-thick (*n*)nc-Si:H, PTB, and 1.7-nm-thick MoO_x showcased the best performance with an FF of 81.56% and a V_{OC} above 705 mV. These results indicate efficient electron collection through the proposed contact stack.

Following the optimization of this electron-collecting contact stack, we demonstrated for the first time IBC-SHJ solar cells with a MoO_x blanket layer. The champion solar cell achieved an efficiency of 21.14%, accompanied by an FF of 78.61% and a high shunt resistance above 150 kΩcm^2. Aside from refining the electron-collecting contact stack, the optimization of the fabrication flowchart and precise photolithographic patterning, ensuring well-defined and well-passivated gaps between electron and hole collecting regions, were the key factors that facilitated the achievement of the champion solar cell. Guided by optoelectrical simulations, further optimization of the fabrication process, fine-tuning of plasma treatments, MoO_x and (*n*)nc-Si:H layer, and introduction of improved ARC(s) are expected to facilitate efficiencies well above 24% in the short run with the proposed architecture.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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