

## Analysis and Design of Power Supply Circuits for RF Oscillators

Urso, Alessandro; Chen, Yue; Dijkhuis, Johan F.; Liu, Yao-Hong; Babaie, Masoud; Serdijn, Wouter A.

**DOI**

[10.1109/TCSI.2020.3020001](https://doi.org/10.1109/TCSI.2020.3020001)

**Publication date**

2020

**Document Version**

Final published version

**Published in**

IEEE Transactions on Circuits and Systems I: Regular Papers

**Citation (APA)**

Urso, A., Chen, Y., Dijkhuis, J. F., Liu, Y.-H., Babaie, M., & Serdijn, W. A. (2020). Analysis and Design of Power Supply Circuits for RF Oscillators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(12), 4233 - 4246. Article 9186814. <https://doi.org/10.1109/TCSI.2020.3020001>

**Important note**

To cite this publication, please use the final published version (if applicable).  
Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights.  
We will remove access to the work immediately and investigate your claim.

# Analysis and Design of Power Supply Circuits for RF Oscillators

Alessandro Urso<sup>1</sup>, *Student Member, IEEE*, Yue Chen<sup>2</sup>, *Student Member, IEEE*,  
 Johan F. Dijkhuis, *Member, IEEE*, Yao-Hong Liu<sup>3</sup>, *Senior Member, IEEE*,  
 Masoud Babaie<sup>4</sup>, *Member, IEEE*, and Wouter A. Serdijn<sup>5</sup>, *Fellow, IEEE*

**Abstract**—This article presents guidelines for designing the power supply blocks of RF oscillators. To preserve their spectral purity, the requirements on the noise and ripple of the supply voltage are firstly evaluated based on the oscillator supply pushing factor and the oscillator Figure-of-Merit (FOM). Those specifications are then employed to design and estimate the power efficiency of an analog low-dropout regulator (LDO) and a switched-capacitor DC-DC converter. As a proof of concept, a 2:1 or 3:2 switched-capacitor DC-DC converter is implemented and directly connected to our previously published 4.9 – 5.5 GHz LC oscillator. The converter provides a 1 V supply voltage with a noise  $\leq 0.9 \text{ nV}/\sqrt{\text{Hz}}$  at 1 MHz and does not affect the inherent phase noise of the oscillator. The ripple amplitude of the converter is 30 mV while its effect is suppressed by the spur reduction block embedded in the oscillator.

**Index Terms**—Power supply requirements, switched-capacitor DC-DC converter, noise analysis, LDO, reverse isolation of power supply circuits, LC oscillator, spur reduction block.

## I. INTRODUCTION

OSCILLATORS are widely used in modern integrated circuits. Due to the stringent regulation's requirements on the spectrum of the oscillator, a lot of effort has been put to reduce its phase noise (PN) and improve its Figure-of-Merit (FOM) [1]–[5]. Every oscillator exhibits inherent PN caused by device noise (e.g., flicker and thermal noise) and the quality factor of its tank. However, the noise on the power supply affects the output through the supply pushing factor ( $K_V$ ) of the oscillator, potentially degrading the PN performance. To preserve the oscillator spectral purity, it is required that the PN induced by the supply noise is much lower than the inherent PN of the oscillator. To this end, usually, a low-noise low-dropout regulator (LDO) is used to generate a 'clean' supply for the oscillator. However, the input-referred noise

of the LDO's voltage reference, error amplifier and feedback resistors directly appears at its output, potentially degrading the oscillator PN. Low noise LDOs can be implemented at the cost of an additional quiescent current [6]–[9], which, however, impacts the system power efficiency significantly.

For example, in [6], an inductor-based buck-boost DC-DC converter is used to regulate the voltage coming from the storage element. Several LDOs are then employed to provide a clean voltage for various supply-sensitive blocks of a transceiver architecture. Each LDO has a minimum dropout voltage of 200 mV, which, together with its quiescent current, makes the whole system power inefficient. On the other hand, a co-design of a class-D oscillator and an LDO is presented in [7]. The co-design relies on the fact that the error amplifier (EA) of the LDO regulates the gate voltage of the tail transistor directly. To avoid limiting the oscillator PN performance, the EA operates from a separate supply of 1.2 V and consumes 0.5 mA of quiescent current, meaning that more than 40% of the power consumption is wasted in the LDO itself.

The primary focus of this article is on the requirements, analysis and design of the supply blocks of LC oscillators (e.g., LDOs, and switched-capacitor DC-DC converters). Section II derives the voltage ripple and the noise level required by the power supply of an LC oscillator not to affect its inherent spectral purity. In Section III, a design guideline for an analog LDO to meet these supply requirements is presented. As a result, the derived closed-form equations relate the system requirements to the LDO's maximum power efficiency and its components parameters. Given the poor LDO efficiency performance, in Section IV, a power efficiency and noise analysis of a reconfigurable 2:1 and 3:2 switched-capacitor (SC) DC-DC converter is carried out. A closed-form equation to estimate the output noise of the SC DC-DC converter is derived merely based on its equivalent resistance and capacitance. The insights of this analysis are then used to design a SC DC-DC converter that meets the requirements discussed in Section II. Based on the analysis above, a new scheme in which a DC-DC converter directly powers up our previously published LC oscillator [10] is presented in Section V. To mitigate the effects of the ripple generated by the DC-DC converter, a spur reduction block is embedded in the oscillator, which reduces the spurs level by 27 dB. Section VI presents the measurement results as well as a comparison with the state of the art. Section VII discusses a possible system-level power management solution to supply several

Manuscript received January 25, 2020; revised April 28, 2020 and July 5, 2020; accepted August 16, 2020. Date of publication September 4, 2020; date of current version December 1, 2020. This work was supported in part by The Netherlands Organization for Scientific Research (NWO) under Project 13598 and Project 17303. This article was recommended by Associate Editor L. Ye. (Alessandro Urso and Yue Chen contributed equally to this work.) (Corresponding author: Alessandro Urso.)

Alessandro Urso, Yue Chen, Masoud Babaie, and Wouter A. Serdijn are with the Microelectronics Department, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: alessandro01.urso@gmail.com).

Johan F. Dijkhuis and Yao-Hong Liu are with the Holst Centre, imec-NL, 5656 AE Eindhoven, The Netherlands.

Color versions of one or more of the figures in this article are available online at <https://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TCSI.2020.3020001

supply-sensitive blocks. Finally, Section VIII wraps up the paper with conclusions.

## II. SUPPLY NOISE REQUIREMENTS OF AN LC OSCILLATOR

The voltage ripple and noise on the power supply can significantly degrade the oscillator's spectral purity. In this section, the requirements on the power supply noise and ripple are calculated such that the oscillator phase noise and spurious tones are not limited by the supply.

### A. Power Supply Rejection Requirement

It is well-known that the level of the spurious tones around the carrier, induced by a sinusoidal supply ripple with an amplitude of  $V_m$  and a frequency of  $f_m$  can be calculated by

$$S_{spur} = 10 \log_{10} \left( \frac{K_V V_m}{2 f_m} \right)^2 \text{ dBc}, \quad (1)$$

where  $K_V$  is the supply pushing factor of the oscillator expressed in Hz/V [11]. Given the desired spur level, the maximum supply ripple tolerated by the oscillator can be calculated by

$$V_m < \frac{2 * f_m}{K_V} 10^{(S_{spur})/20}. \quad (2)$$

For powering up the oscillator, a cascade connection of a switched-capacitor DC-DC converter and an LDO is usually used to simultaneously achieve a higher power efficiency and larger power supply rejection. The switched-capacitor DC-DC converter generates a sawtooth-shaped supply voltage with a peak-to-peak ripple amplitude

$$V_{ripple} = \frac{I_L}{C_{fly} f_{CLK}}, \quad (3)$$

where  $I_L$  is the current drawn by the oscillator.  $f_{CLK}$  and  $C_{fly}$  are the converter switching frequency and flying capacitance, respectively. Considering the sawtooth shape of the DC-DC converter output voltage, the magnitude of the fundamental component of the ripple is  $V_{ripple}/\pi$ . As a result, The required power supply rejection (PSR) of the LDO can be estimated by

$$PSR = \frac{\pi \cdot V_m}{V_{ripple}} = \frac{2\pi C_{fly} f_{CLK}^2 10^{(S_{spur}/20)}}{I_L K_V}. \quad (4)$$

Note that there is a quadratic relation between the PSR and  $f_{CLK}$ , since both the ripple of the DC-DC converter and the filtering capability of the oscillator simultaneously improve by increasing  $f_{CLK}$ . It, however, comes at a price of a higher dynamic power consumption to drive the switches of the DC-DC converter, potentially degrading the system efficiency.

### B. Noise Requirement

The phase noise (PN) performance of an oscillator is determined by device excess noise factor, and its tank quality factor and can be calculated by

$$\mathcal{L}(\Delta f) = 10 \log_{10} \left( \frac{10^{-\frac{FOM}{10}}}{10^3 P_{DC}} \left( \frac{f_0}{\Delta f} \right)^2 \right), \quad (5)$$

where  $P_{DC}$  is the oscillator power consumption, and FOM is its Figure-of-Merit<sup>1</sup> with a typical value of 190-195 dBc/Hz [12], [13].  $f_0$  and  $\Delta f$  are the carrier frequency and the offset frequency with respect to the main tone, respectively. Note that Eq. (5) is only valid in the thermal noise (20 dB/dec) region of the oscillator PN. Since the FOM is a general performance metric for LC oscillators and the variation of its typical value is not large, its use in Eq. (5) allows to reach more general conclusions in the following sections, which are independent of the oscillator topology and parameters.

On the other hand, the PN induced by the noise on the oscillator supply can be estimated to be

$$\mathcal{L}_{sup}(\Delta f) = 10 \log_{10} \left( \frac{K_V^2}{\Delta f^2} V_{n,supply}^2(\Delta f) \right) \quad (6)$$

where  $V_{n,supply}^2(\Delta f)$  is the PSD of the supply noise. To preserve the inherent phase noise of the oscillator,

$$\mathcal{L}_{sup}(\Delta f) \ll \mathcal{L}(\Delta f), \quad (7)$$

leading to

$$V_{n,supply}^2 < \frac{10^{-\frac{FOM}{10}}}{10^3 P_{DC}} \left( \frac{f_0}{K_V} \right)^2. \quad (8)$$

Superficially, Eq. (8) indicates that a larger supply noise can be tolerated at higher oscillation frequencies. However, the total tank capacitance ( $C_{tot}$ ) is composed of a variable capacitor used to tune  $f_0$  and a voltage-dependent parasitic capacitance of the oscillator core transistors ( $C_{par}$ ). Hence, the effective value of  $C_{par}$  is modulated by the supply voltage. As  $f_0$  increases, the variable capacitance is reduced, and  $C_{par}$  becomes a bigger portion of  $C_{tot}$ , thereby increasing  $K_V$ . Consequently,  $f_0/K_V$  and the noise requirement remain almost constant over the operating frequency range. The variation of the equivalent value of  $C_{par}$  comes from the fact that the time interval during which the transistors stay in various operating regions is altered when the oscillation amplitude varies due to supply ripple. When the ripple frequency increases, the time that the transistor stays in each region becomes shorter. However, its ratio to the period of the supply ripple remains relatively constant, leading to a similar equivalent value of  $C_{par}$ . Therefore,  $K_V$  is weakly related to the ripple frequency.

## III. LDO DESIGN GUIDELINES AS A VOLTAGE SUPPLY OF LC OSCILLATORS

Several LDOs are reported in the literature with a power efficiency higher than 95% [14]–[16], which, however, do not meet the requirements discussed in the previous section. The goal of this section is to quantify the efficiency degradation of an analog LDO while meeting the requirements discussed in the previous section.

The LDO shown in Fig. 1 consists of an Error Amplifier (EA), a feedback network ( $R_{F1}$  and  $R_{F2}$ ), an accurate voltage reference ( $V_{ref}$ ), and a pass transistor ( $M_p$ ). The feedback network provides a scaled version of the output voltage,  $V_{FB}$ . The EA compares  $V_{ref}$  with  $V_{FB}$  and generates an error signal

$${}^1\text{FOM} = |PN| + 20 \log_{10} \left( \frac{f_0}{\Delta f} \right) - 10 \log_{10} \left( \frac{P_{DC}}{1mW} \right).$$

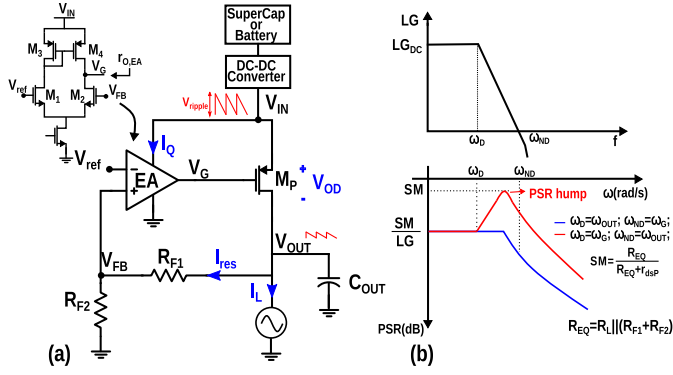


Fig. 1. (a) Block diagram of a typical LDO topology; (b) its PSR with (blue line) and without (red line) the use of an external capacitor.

$V_G$  that modulates the gate terminal of the pass transistor such that the output voltage  $V_{OUT}$  is kept constant. In steady state, the output voltage can be expressed as

$$V_{out} = \left(1 + \frac{R_{F1}}{R_{F2}}\right) V_{ref} = \frac{V_{ref}}{\beta}, \quad (9)$$

where  $\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$  is the closed-loop gain of the LDO. The power efficiency can be written as

$$\eta = \left(\frac{V_{IN} - V_{OD}}{V_{IN}}\right) \left(\frac{I_L}{I_L + I_{res} + I_Q}\right) \quad (10)$$

$$\eta = \left(\frac{V_{IN} - V_{OD}}{V_{IN}}\right) \left(\frac{I_L}{I_L + \frac{V_{OUT}}{R_{F1} + R_{F2}} + I_Q}\right)$$

where  $V_{OD}$  is the overdrive voltage of transistor  $M_p$ ,  $I_L$  is the current drawn by the oscillator,  $I_{res}$  and  $I_Q$  is the current that flows through the resistors and the quiescent current, respectively.  $V_{OD}$ ,  $I_{res}$  and  $I_Q$  affect the power efficiency. Hence, in this section, their minimum value is calculated such that the oscillator's requirements are met.

#### A. Calculation of $I_{res}$ Based on Noise Requirements

A bandgap voltage reference is usually used to generate  $V_{ref}$ . Its noise is filtered out either by placing a big external capacitor, or by implementing an  $RC$  filter with a big on-chip resistor and a capacitor [17]. Consequently, it is neglected in the following analysis.

Resistors  $R_{F1}$  and  $R_{F2}$  generate an input-referred voltage noise with a power spectral density (PSD), in  $V^2/Hz$ , of  $4kT(R_{F1}||R_{F2})$ , where  $k$  is Boltzmann's constant and  $T$  is the absolute temperature expressed in kelvin. Their noise contribution directly appears at the output and it is filtered only at frequencies above the non-dominant pole of the LDO. For this reason, one would choose  $R_{F1}$  and  $R_{F2}$  as small as possible while keeping the ratio constant. However, the lower the value of the resistors, the higher the current ( $I_{res}$ ) flowing through them, thus degrading the power efficiency of the LDO (Eq.(10)). The PSD of the feedback resistors noise is multiplied by  $\frac{1}{\beta^2}$  and appears at the output of the LDO, resulting in  $S_{V,OUT,R} = \left(\frac{R_{F1}}{R_{F2}}\right)4kT(R_{F1} + R_{F2})$ .

To not affect the inherent PN of the oscillator, the PN induced by the feedback resistors must be significantly smaller

(e.g.,  $\sim 10$  times smaller) than the inherent PN of the oscillator. By using Eq.(7) and Eq.(8), we have

$$\left(\frac{R_{F1}}{R_{F2}}\right)4kT(R_{F1} + R_{F2}) < \frac{1}{10} \frac{10^{-\frac{(FOM+30)}{10}}}{P_{DC}} \left(\frac{f_0}{KV}\right)^2. \quad (11)$$

Given that  $P_{DC} = \frac{V_{OUT}^2}{R_L}$  and  $V_{OUT} = V_{ref} \left(1 + \frac{R_{F1}}{R_{F2}}\right)$ , Eq.(11) can be rewritten as

$$\left(\frac{I_{res}}{I_L}\right) > 10 \frac{4kT\left(\frac{1}{\beta} - 1\right)(V_{OUT})^2}{10^{-\frac{(FOM+30)}{10}} \left(\frac{f_0}{KV}\right)^2}. \quad (12)$$

Eq.(12) allows to quantify the efficiency degradation due to the current,  $I_{res}$ , flowing through the feedback resistors.

Assuming  $P_{DC} = 1$  mW,  $V_{OUT} = 1$  V,  $KV = 40$  MHz/V and  $FOM = 190$  dBc/Hz, the maximum supply noise is  $V_{n,supply} = 38$  nV/ $\sqrt{Hz}$ . Furthermore, by using Eq.(12), the two feedback resistors are found to be  $R_{F1} = 5.3$  k $\Omega$  and  $R_{F2} = 7$  k $\Omega$ . As a result,  $I_{res} \sim 80$   $\mu$ A, which results in a current efficiency of 92%. Note that high-performance oscillators have a higher FOM, posing even more stringent requirements on the supply noise, and the size of the feedback resistors (e.g., an FOM of 196 dBc/Hz leads to  $V_{n,supply} < 19$  nV/ $\sqrt{Hz}$ ,  $R_{F1} = 1.8$  k $\Omega$ ,  $R_{F2} = 7$  k $\Omega$  and  $I_{res} \sim 130$   $\mu$ A).

It is worth to point out that the efficiency degradation due to  $I_{res}$  does not change with  $P_{DC}$  or  $I_L$  for a constant  $V_{OUT}$ . When  $I_L$  increases, the noise power tolerated by the oscillator decreases with the same ratio. Hence,  $I_{res}$  should proportionally increase to reduce the noise contribution from the feedback resistors, leading to a constant  $\frac{I_{res}}{I_L}$ . Therefore, the efficiency degradation due to  $I_{res}$  also remains constant.

#### B. Calculation of $I_Q$ Based on Noise Requirements

The input-referred noise of the EA can be written as [18]

$$S_{V,EA} = 2S_{V,M1} + 2\left(\frac{g_{m3}}{g_{m1}}\right)^2 S_{V,M3}, \quad (13)$$

where  $S_{V,M1}$  and  $S_{V,M3}$ , are the power spectral density of the noise (voltage) generated by  $M_1$  and  $M_3$ , respectively. Each of the PSD is made of thermal and flicker noise components. Given that at higher frequencies, the thermal component is dominant, in this analysis, the flicker noise is neglected. Hence,

$$S_{V,M_i} = \frac{4kT\gamma}{g_{mi}} \quad (14)$$

where  $\gamma$  is the excess noise factor and it is equal to  $\frac{2}{3}$  in strong inversion saturation. By substituting Eq.(14) into Eq.(13), and assuming  $M_{1-4}$  of the same size, the total noise at the input of the EA can now be expressed as

$$S_{V,IN,EA} = \frac{16\gamma kT}{g_m}. \quad (15)$$

The total output-referred noise of the EA can be written as

$$S_{V,OUT} = \frac{S_{V,IN,EA}}{\beta^2}. \quad (16)$$

It is worth mentioning that due to the gain of the error amplifier, the noise of the pass transistor  $M_P$  has a negligible contribution compared to the error amplifier noise when referred to the LDO input.

Similarly to the noise of the feedback resistors, it can be assumed that the PN induced by the EA is  $\sim 10$  times smaller than the inherent PN of the oscillator (Eq. (7, 8)). Hence,

$$g_m > 10 * \frac{16\gamma kT P_{DC}}{10^{\frac{-(FOM+30)}{10}} \beta^2 \left(\frac{f_0}{K_V}\right)^2}. \quad (17)$$

By multiplying both sides of (17) by  $I_Q$ , the quiescent current can be expressed as

$$I_Q > 10 * \frac{\frac{32}{3} kT P_{DC}}{10^{\frac{-(FOM+30)}{10}} \left(\frac{f_0}{K_V}\right)^2 \beta^2 \left(\frac{g_m}{2I_D}\right)^2}, \quad (18)$$

where  $I_D = \frac{I_Q}{2}$  is the drain current of  $M_{1:4}$ . Assuming  $g_m/I_D = 12 \text{ S/A}$  and  $\gamma = \frac{2}{3}$ ,  $I_Q$  must be  $> 145 \mu\text{A}$ , further degrading the power efficiency by a factor of 0.87.

To avoid degrading the oscillator phase noise, Eq.(18) suggests that  $I_Q$  should be increased proportionally to  $P_{DC}$  for the same  $V_{OUT}$  and  $g_m/I_D$ . As a result,  $\frac{I_Q}{I_L}$ , and therefore, the power efficiency degradation due to the error amplifier is constant with respect to  $P_{DC}$ .

### C. Calculation of $V_{OD}$ Based on PSR Requirement

The two poles of the LDO topology shown in Fig. 1 are located at the gate of  $M_P$  ( $\omega = \omega_G$ ) and at the output node  $V_{OUT}$  ( $\omega = \omega_{OUT}$ ) [19]–[21], and can be calculated by

$$\omega_G = \frac{1}{r_{O,EA}(C_{gsP} + (1 + g_{mP} R_{OUT})C_{gdP})}$$

$$\omega_{OUT} = \frac{1}{R_{OUT}C_{OUT}} \quad (19)$$

where  $r_{O,EA}$  is the output impedance of the error amplifier,  $R_{OUT} = R_L || (R_{F1} + R_{F2}) || r_{DSP}$ ,  $r_{DSP}$  is the output impedance of  $M_P$ ,  $C_{gdP}$  and  $C_{gsP}$  is the gate-to-drain and gate-to-source capacitance of  $M_P$ , respectively. Based on the location of the dominant pole ( $\omega_D$ ), the LDO topologies can be divided into two categories [22] whose PSR profile is sketched in Fig. 1(b). To have the dominant pole located at  $V_{OUT}$  [23]–[28], one can increase  $C_{OUT}$ . In this scenario, the LDO can easily achieve high PSR at high frequencies, as the output capacitor provides a low-impedance path to ground for the supply ripple (blue curve in Fig. 1(b)). To guarantee stability, the output capacitor is increased in the  $\mu\text{F}$  range. For LDOs with the dominant pole located at the gate of  $M_P$  ( $\omega_D = \omega_G$ ) [14]–[16], [28]–[30], the value of  $C_{OUT}$  is reduced significantly. The corresponding PSR is sketched with a red curve in Fig. 1(b). For  $\omega_G < \omega < \omega_{OUT}$ , due to reduced loop gain, the PSR degrades and a hump in the PSR curve is observed. However, at  $\omega > \omega_{OUT}$ , the output capacitor provides a low-impedance path to ground, thereby improving the PSR. In order to favor full-system integration, the cap-less LDO solution is chosen, whose dominant pole needs to be located at the switching frequency of the DC-DC converter (e.g.  $f_D = f_{CLK} = 10 \text{ MHz}$ ).

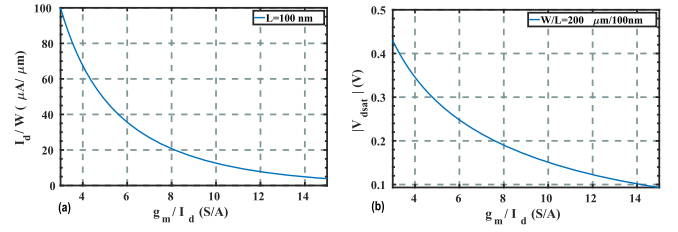


Fig. 2. (a) Current density and (b) overdrive voltage of the pass transistor for different  $g_m/I_D$  values.

The peak of the PSR hump is located at the unity-gain frequency and it is equal to  $\frac{R_{EQ}}{R_{EQ} + r_{DSP}}$ , where  $R_{EQ} = R_L || (R_{F1} + R_{F2})$ . To guarantee a PSR of 0.5 around the hump,  $r_{DSP} = R_{EQ} \approx R_L$  is required. Hence, the length of  $M_P$  can be calculated as

$$r_{dsP} = \frac{1}{\lambda I_L} = \frac{V_a L_P}{I_L} \Rightarrow L_P = \frac{R_{EQ} I_L}{V_a} = 0.1 \mu\text{m} \quad (20)$$

where  $V_a = 10 \text{ V}/\mu\text{m}$ .

To guarantee a phase margin of  $60^\circ$  with a PSR of  $-40 \text{ dB}$ , the frequency of the non-dominant pole should be located a frequency  $\sim 400$  times higher than the dominant one, i.e.,  $f_{ND} > 400 f_{CLK}$ . Consequently, by employing Eq.(19), the total output capacitance should be  $< 100 \text{ fF}$ . As will be shown shortly, the width of  $M_P$  should be maximized to reduce its overdrive voltage and improve the LDO's efficiency. Therefore, it is desired that the parasitic capacitance of  $M_P$  absorbs all available  $C_{out}$ . Also, any extra decoupling capacitance would push the non-dominant pole closer to the dominant one, potentially affecting the stability of the LDO.  $C_{out}$  is dominated by the drain-to-bulk,  $C_{db}$ , and drain-to-gate,  $C_{dg}$ , capacitances of  $M_P$ :

$$C_{out} = C_{db} + C_{dg} = C_{ov}W + 0.5C_{jbd}WE + C_{jbdsg}W$$

$$\approx 500 \text{ pF/m} \cdot W \quad (21)$$

where  $C_{ov} = 50 \text{ pF/m}$  is the overlapped capacitance per unit width,  $C_{jbd} = 1.4 \text{ mF/mm}^2$  is the bulk-to-drain junction capacitance per unit area,  $E = 140 \text{ nm}$  and  $C_{jbdsg} = 300 \text{ pF/m}^2$ . Hence, the maximum width of  $M_P$  to guarantee enough PSR at  $f_{CLK}$  is  $W_P = 200 \mu\text{m}$ .

Fig. 2(a) shows the current density for different  $g_m/I_D$  values for the pass transistor. Given,  $I_L = 1 \text{ mA}$  and  $W_P = 200 \mu\text{m}$ , a  $g_m/I_D$  of 12 can be achieved. Consequently,  $M_P$  can operate in the weak-inversion region with only  $V_{OD}$  of  $125 \text{ mV}$ , as can be gathered from Fig. 2(b). This further degrades the power efficiency of the LDO by a factor of 0.89.

If  $P_{DC}$  increases,  $R_L$  proportionally decreases for a constant  $V_{OUT}$ . Hence, to keep  $\omega_{OUT}$  the same,  $C_{OUT}$  should be increased by the same ratio. This, in turn, leads to an increase in the width of  $M_P$ , which makes the current density of the pass transistor relatively constant, resulting in a similar overdrive voltage. Consequently, the power efficiency degradation due to  $V_{OD}$  is not a function of  $P_{DC}$ .

<sup>2</sup>Note that  $C_{ov}$ ,  $C_{jbd}$ , and  $C_{jbdsg}$  are technology-dependent parameters and the values used here are from a 40-nm CMOS technology.

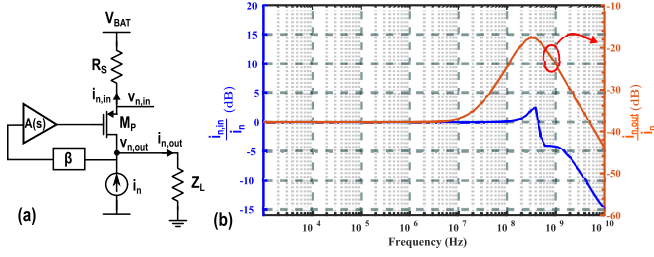


Fig. 3. (a) Equivalent small-signal circuit of the LDO with (b) its simulated transfer functions from  $i_n$  to  $i_{n,in}$  and  $i_{n,out}$  when  $R_S = 2\Omega$ .

#### D. Satisfying the PSR Requirement

The PSR at frequencies below the dominant pole of the LDO can be expressed as

$$PSR = \frac{SM}{1 + LG_{DC}} \approx \frac{SM}{A_{EA}A_{MP}\beta} \quad (22)$$

where  $SM = \frac{R_{eq}}{R_{eq} + r_{DSP}}$ ,  $LG_{DC} = A_{EA}A_{MP}\beta$  is the loop gain of the LDO at DC,  $A_{EA}$  is the voltage gain of the EA, while  $A_{MP}$  is the voltage gain of the pass transistor and can be written as

$$A_{MP} = g_{m_P}R_{OUT} = g_{m_P} \cdot R_L || (R_{F1} + R_{F2}) || r_{DSP}. \quad (23)$$

$A_{EA}$  can be written as

$$A_{EA} = g_m r_{O,EA} = 0.5 \frac{g_m}{I_Q} V_a L_1. \quad (24)$$

Consequently, the length of the error amplifier devices to satisfy the PSR requirement can be calculated by

$$L_1 > \frac{2SM}{\frac{g_m}{I_Q} \cdot V_a \cdot \beta \cdot A_{MP} \cdot PSR} \quad (25)$$

By considering  $PSR = -40$  dB, and the relevant parameters calculated in the previous sub-sections, the minimum length of the transistors in the error amplifier should be 280 nm.

#### E. Reverse Isolation of Analog LDOs

In a complex System-on-Chip (SoC), there might be some noise coupled to the output of the LDO due to the activity of other aggressor modules. In this subsection, its side effects on the LDO's input and output voltages are investigated. Fig. 3 (a) shows the equivalent small-signal representation of the LDO. It is assumed that the LDO is powered by a battery, whose output resistance is  $R_S$ . It can be shown that the resulting current noise at the LDO's input ( $i_{n,in}$ ) from the injected noise ( $i_n$ ) can be expressed by

$$\frac{i_{n,in}}{i_n}(s) = \frac{g_{m_P} Z_L A(s) \beta}{1 + g_{m_P} R_S + g_{m_P} Z_L A(s) \beta}. \quad (26)$$

Note that  $LG = g_{m_P} Z_L A(s) \beta$  is the open-loop gain of LDO, which is much larger than 1 for frequencies below the dominant pole. Hence, Eq.(26) can be approximated as

$$\frac{i_{n,in}}{i_n}(s) \sim 1. \quad (27)$$

This equation indicates that the injected current noise directly appears at the input, and is then converted into voltage

TABLE I

SUMMARY OF LDO PERFORMANCE AND COMPONENT VALUES

Component	Value	Parameter	Value	Eff. degrad.
$M_{1:4}$	$\frac{30\ \mu\text{m}}{500\ \text{nm}}$	$V_{OD}$	125 mV	0.89
$M_P$	$\frac{200\ \mu\text{m}}{100\ \text{nm}}$	$I_Q$	145 $\mu\text{A}$	0.87
$R_{F1}, R_{F2}$	5.3 k $\Omega$ , 7 k $\Omega$	$I_{res}$	80 $\mu\text{A}$	0.92
$I_L$	1 mA	-	-	-

noise through the resistor  $R_S$ . Consequently, it is critical to minimize  $R_S$  to avoid the propagation of the injected noise to other blocks. Similarly, due to  $i_n$ , the current noise flowing to the LDO's load ( $i_{n,out}$ ) can be expressed as

$$\frac{i_{n,out}}{i_n}(s) = \frac{1 + g_{m_P} R_S}{1 + g_{m_P} R_S + LG}. \quad (28)$$

At frequencies lower than the dominant pole,  $LG \gg 1 \gg g_{m_P} R_S$ . Hence, Eq.(28) can be simplified to

$$\frac{i_{n,out}}{i_n}(s) = \frac{1}{LG_{DC}}. \quad (29)$$

Interestingly, the LDO attenuates any noise injected at its output by the loop gain.

#### F. Verification

To verify the guidelines developed in the previous sub-sections, an LDO is designed accordingly, and its simulation results are compared with the requirements and calculations. Table I reports the component values used in the simulation.

Fig. 4 (a) shows the magnitude and the phase of the open-loop transfer function. The location of the dominant pole,  $f_D \sim 10$  MHz, and non-dominant pole,  $f_{ND} \sim 4$  GHz, are in close accordance with the calculated values, leading to a phase margin of  $\sim 60^\circ$ . Fig. 4 (b) shows the closed-loop transfer function from  $V_{ref}$  to  $V_{OUT}$  normalized to  $1/\beta$ . This shows that, for frequencies below  $f_{ND}$ , any noise at the input of the error amplifier directly appears at its output, proving that the noise generated by the feedback resistors and the error amplifier plays an important role and should therefore be minimized.

Fig. 5 (a) shows the simulated output noise of the LDO versus frequency. The noise floor is  $< 38\ \text{nV}/\sqrt{\text{Hz}}$ , which is in line with the calculations, thereby satisfying the requirements. Otherwise, the phase noise of the oscillator would be degraded, as shown in Fig. 6, where external white noise is added to its supply. Fig. 5 (b) shows the simulated PSR of the LDO. The PSR hump  $\sim -6$  dB, which is in accordance with the predicted value. At frequencies below the dominant pole (i.e.,  $f_D \approx 10$  MHz), the PSR is  $\sim -40$  dB, as predicted by Eq.(22). In the simulation, the efficiency degradation due to  $I_{res}$ ,  $I_Q$ , and  $V_{OD}$  is 0.92, 0.87 and 0.89, respectively, leading to a total power efficiency of 71%. Those values are in agreement with our analysis.

Finally, Fig. 3 (b) illustrates the simulation results related to the injected current noise at the LDO's output. As expected from our analysis in Section III.E, the LDO does not offer

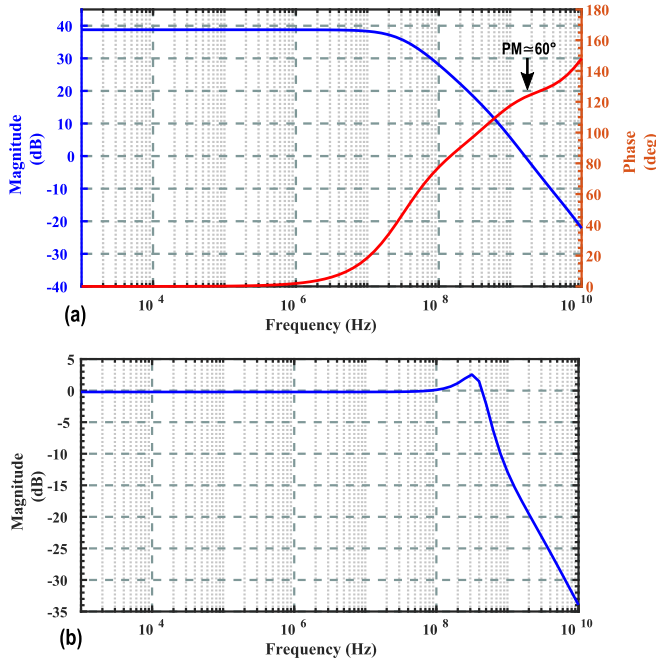


Fig. 4. (a) Open-loop transfer function of the LDO and (b) its transfer function from  $V_{ref}$  to  $V_{OUT}$  normalized to  $1/\beta$ .

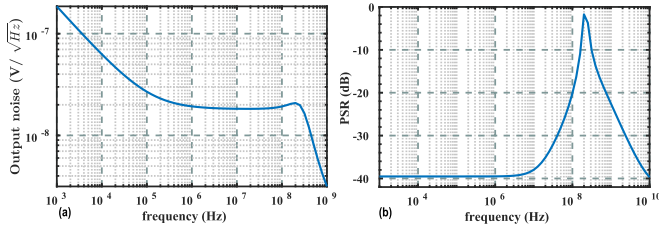


Fig. 5. (a) Simulated output noise and (b) PSR of the LDO using the component values reported in Table I.

any filtering at  $f \leq f_D$ , and all the injected noise directly appears at the input. On the other hand, only a small fraction of the injected noise flows through the load. However, for frequencies  $f > f_D$ , this amount significantly increases due to the reduction of the EA gain until the output non-dominant pole provides a low impedance path to ground for the noise.

#### IV. POWER EFFICIENCY AND NOISE ANALYSIS OF A 2:1-3:2 DC-DC CONVERTER

In this section, a switched-capacitor cell capable of providing a conversion ratio (CR) of 2:1 or 3:2 is first introduced. Then, based on its working principle, the output noise is derived, and the converter is designed to minimize the output noise while maximizing the power efficiency.

##### A. DC-DC Converter Working Principles

The left side of Fig. 7 shows the circuit representation of a 2:1 switched-capacitor (SC) DC-DC converter. It is made of a charge transfer capacitor,  $C_{fly}$ , and four (two PMOS and two NMOS) switches driven by two non-overlapping clock phases,  $\phi_1$  and  $\phi_2$ . Using an energy-conservation analysis, one can express the output voltage,  $V_{OUT} = \frac{V_{IN}}{2}$  [31].

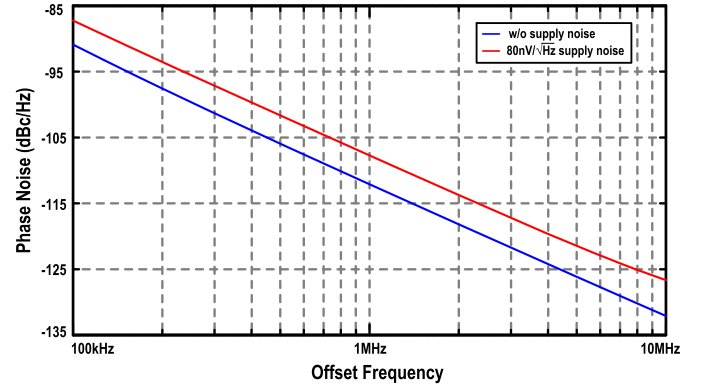


Fig. 6. Simulated phase noise degradation of the LC oscillator when its supply noise exceeds the value estimated by Eq. (8).

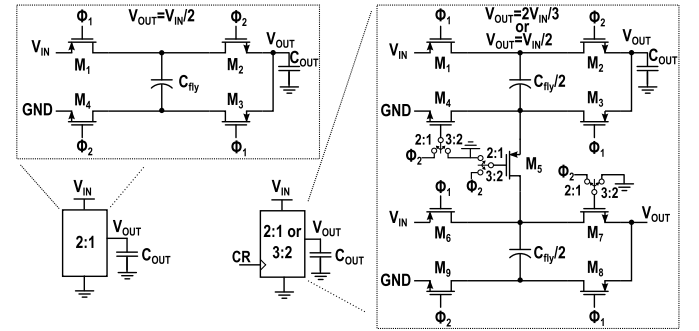


Fig. 7. Circuit representation of a 2:1 topology (left); and a reconfigurable 2:1, 3:2 switched-capacitor DC-DC converter (right).

Two 2:1 stacked topologies are connected by an additional switch,  $M_5$ , allowing the implementation of a 3:2 topology ( $V_{OUT} = \frac{2}{3}V_{IN}$ ), as shown in the right side of Fig. 7. When used in the 2:1 configuration,  $M_5$  is always turned off and the two 2:1 topologies are connected in parallel. When used in the 3:2 configuration, switches  $M_4$  and  $M_7$  are always off and the two flying capacitors are charged in parallel and discharged in series.

##### B. Power Efficiency

Fig. 8(a) shows the equivalent model of a SC DC-DC converter, in which  $CR = \{\frac{1}{2}, \frac{2}{3}\}$  is the conversion ratio. The key power-loss contributions in a switched-capacitor DC-DC converter are the switching losses (due to the dynamic operation of the switches) and the conduction losses (due to the output impedance of the converter). Consequently,

$$P_{LOSS} = nC_g V_{sw}^2 f_{sw} + R_{OUT} I_L^2, \quad (30)$$

where  $n$  is the number of switches operating at  $f_{sw}$  with a clock voltage swing of  $V_{sw}$ , and  $C_g$  is the equivalent gate capacitance of each switch.  $R_{OUT}$  is the converter's output impedance, and can be estimated by [32], [33]

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\frac{\rho}{C_{fly} f_{sw}}\right)^2 + (\alpha R_{on})^2}, \quad (31)$$

where  $\rho = \{\frac{1}{4}, \frac{2}{9}\}$  and  $\alpha = \{2, \frac{14}{9}\}$  are topology dependent parameters in the 2:1 and 3:2 topology, respectively.  $R_{SSL}$  and

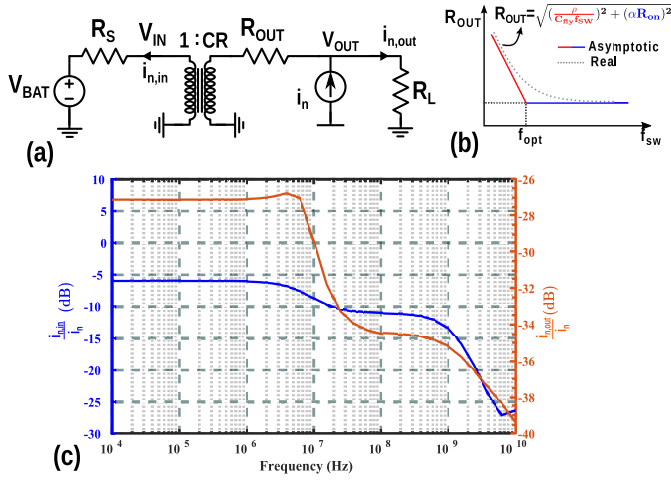


Fig. 8. (a) Equivalent model of a SC DC-DC converter with the noise current  $i_n$  used for the calculation of the transfer function; (b) its output resistance versus the switching frequency and (c) the simulated transfer functions from  $i_n$  to  $i_{n,in}$  and  $i_{n,out}$ .

$R_{FSL}$  are the resistances in the slow (red curve) and fast (blue curve) switching region, respectively (see Fig. 8 (b)). To simultaneously reduce the output voltage ripple and maximize the power efficiency, it is required that the converter operates at the boundary of the slow and the fast switching regions. Hence,  $R_{OUT} = \alpha R_{on}$ , and the contribution of the resistances in the two different regions should be the same, leading to

$$R_{SSL} = R_{FSL} \Rightarrow f_{sw} = f_{opt} = \frac{\rho}{\alpha C_{fly} R_{on}}. \quad (32)$$

By substituting the optimum frequency to Eq. (30), the power loss can be expressed as

$$P_{LOSS} = \frac{n \cdot \rho \cdot C_g V_{sw}^2}{\alpha C_{fly} R_{on}} + \alpha R_{on} I_L^2. \quad (33)$$

As can be gathered from this equation, the power loss is a function of  $C_g$ , and  $R_{on}$ , which both are related to the switch width ( $W$ ). Hence,  $P_{LOSS}$  can be rewritten as

$$P_{LOSS} = \frac{n \cdot \rho \cdot \overline{C}_g V_{sw}^2 W^2}{\alpha C_{fly} \overline{r}_{on}} + \alpha \frac{\overline{r}_{on}}{W} I_L^2, \quad (34)$$

where  $\overline{C}_g$  and  $\overline{r}_{on}$  are the capacitance and on-resistance of a unit-width transistor, respectively. To maximize the power efficiency, Eq.(34) should be minimized with respect to  $W$ , leading to

$$W_{opt} = \left( \frac{C_{fly}}{2 \cdot n \cdot \rho \cdot \overline{C}_g} \right)^{\frac{1}{3}} \left( \frac{\alpha \overline{r}_{on} I_L}{V_{sw}} \right)^{\frac{2}{3}}. \quad (35)$$

Assuming  $\overline{r}_{on} = 5 \cdot 10^3 \Omega \cdot \mu m$ ,  $\overline{C}_g = 6 \cdot 10^{-15} \frac{F}{\mu m}$ ,  $C_{fly} = 1 \text{ nF}$ ,  $V_{sw} = 2 \text{ V}$  and  $P_{OUT} = 1 \text{ mW}$  ( $V_{OUT} = 1 \text{ V}$ , and  $I_L = 1 \text{ mA}$ ), the optimal width is  $W_{opt} = 130 \mu m$ , resulting in  $f_{sw} \sim 10 \text{ MHz}$ . Table II reports the optimal switch width, the minimum power loss and the estimated efficiency for the DC-DC converter in the 2:1 and 3:2 configurations.

It is worth to mention that the power efficiency does not depend upon the delivered output current. As  $I_L$  increases,  $C_{fly}$  should also increase accordingly to keep the ripple

TABLE II  
SUMMARY OF THE DC-DC CONVERTER KEY PARAMETERS

Parameter	2:1 mode	3:2 mode
$W_{opt}$	130 $\mu m$	93 $\mu m$
$P_{loss}$	117 $\mu W$	126 $\mu W$
$\eta$	89%	87%

amplitude constant (see Eq.(3)). Consequently, as can be gathered from Eq.(34) and (35),  $W_{opt}$  and  $P_{LOSS}$  increase linearly with  $I_L$ . As a result, both the the power efficiency and  $f_{opt}$  remain constant with respect to  $I_L$ .

### C. Noise Analysis

From noise point of view, a switched-capacitor DC-DC converter can be modeled by the equivalent circuit shown in Fig 9(a).  $R_{eq}$  is the equivalent resistance of the switches that are involved in each phase of the conversion. Assuming all the switches have the same  $R_{on}$ ,

$$R_{eq} = \begin{cases} 2R_{on}, & \text{in } \phi_1 \text{ and } \phi_2 \text{ of the 2:1 mode} \\ 2R_{on}, & \text{in } \phi_1 \text{ of the 3:2 mode} \\ 3R_{on}, & \text{in } \phi_2 \text{ of the 3:2 mode} \end{cases} \quad (36)$$

On the other hand, the equivalent capacitance can be calculated by

$$C_{eq} = \begin{cases} \frac{C_{fly} C_{OUT}}{C_{fly} + C_{OUT}}, & \text{in } \phi_1 \text{ and } \phi_2 \text{ of the 2:1 mode} \\ \frac{C_{fly} C_{OUT}}{C_{fly} + 2C_{OUT}}, & \text{in } \phi_1 \text{ of the 3:2 mode} \\ \frac{C_{fly} C_{OUT}}{4 C_{OUT} + C_{fly}}, & \text{in } \phi_2 \text{ of the 3:2 mode.} \end{cases} \quad (37)$$

During the tracking phase (blue phase in Fig. 9(b)) the switches due to their  $R_{on}$ , produce a noise voltage with a PSD equal to  $m4kTR_{eq}$ , where  $m = 0.5$  is the duty cycle. As can be gathered from Fig. 9(c), the thermal noise generated by the resistors is shaped by  $C_{eq}$  with a time constant of  $\tau = R_{eq} C_{eq}$ . As a result, the PSD of the noise voltage across the equivalent capacitor during the tracking phase can be written as

$$S_d(f) = \frac{m4kTR_{eq}}{1 + (2\pi f\tau)^2}. \quad (38)$$

At the end of tracking phase, the switches are open and the noise previously sampled is now held on  $C_{eq}$  (red phase in Fig. 9(b)). As a consequence, aliasing due to the sampling of the noise occurs [34]. In particular, the noise at frequencies higher than  $\frac{f_{sw}}{2}$  is folded back into the 0-to- $\frac{f_{sw}}{2}$  range and adds up to the thermal noise. The PSD due to the aliasing of the sampled noise during the holding phase is sketched in Fig. 9 (d). It has a sinc<sup>2</sup> shape, and can be written as

$$S_{fol}(f) = (1 - m)^2 \frac{\sin^2[(1 - m)\pi f / f_{sw}]}{[(1 - m)\pi f / f_{sw}]^2} \frac{2kT}{C_{eq} f_{sw}}. \quad (39)$$

If the bandwidth of the equivalent circuit ( $BW = \frac{1}{2\pi R_{eq} C_{eq}}$ ) is larger than  $f_{sw}/2$ , the summation of all the folded noise leads to a flat PSD over 0-to- $\frac{f_{sw}}{2}$  with an amplitude that is



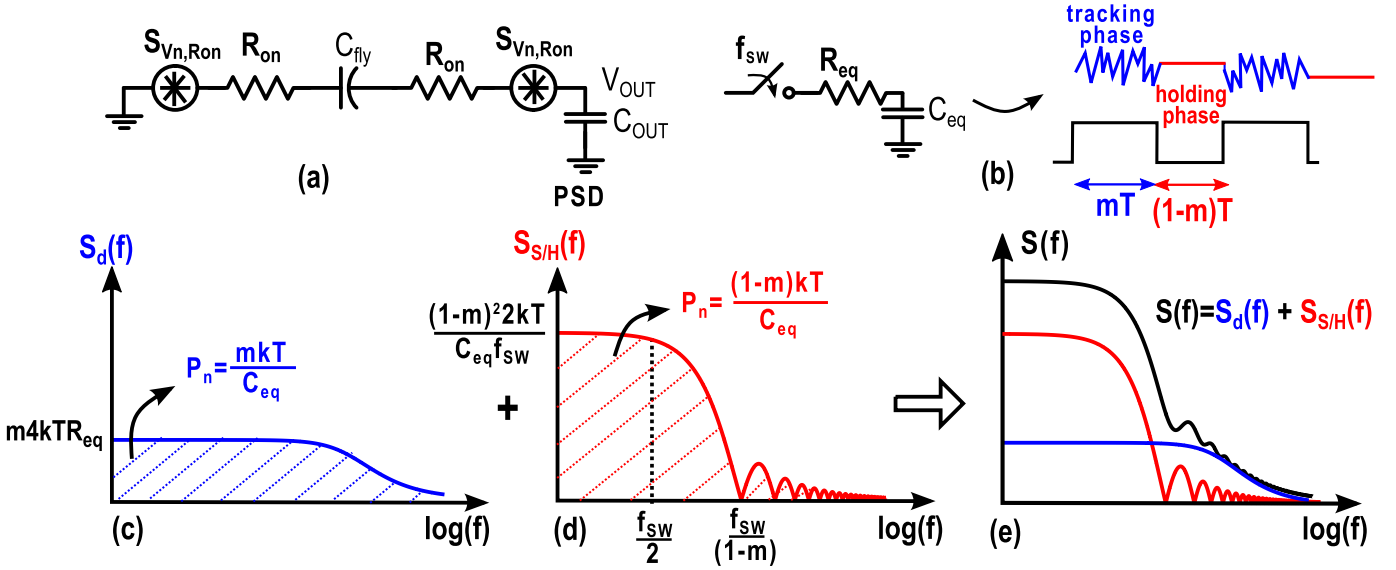


Fig. 9. (a) Equivalent circuit model for the DC-DC converter in the 2:1 mode (b) output noise waveform during the tracking and the holding phases (c) PSD of the resistor ( $R_{eq}$ ) shaped by the capacitor ( $C_{eq}$ ) during the tracking phase (d) PSD during the holding phase and (e) a sketch of the total PSD (black line) due to the aliasing of the sampled noise.

$\left(\frac{(1-m)^2 \pi BW}{m f_{sw}}\right)$  times higher than the PSD of the switches' resistance itself [34], [35], as illustrated in Fig. 9(c). In this region, the PSD of the converter is dominated by  $\frac{2kT(1-m)^2}{C_{eq} f_{sw}}$ , thus further reducing  $R_{on}$  would degrade the power efficiency without improving the noise performance. However, at frequencies between  $\frac{f_{sw}}{2}$  and  $BW$ , the noise due to aliasing starts to fade out and the total PSD is dominated by the thermal noise of the equivalent resistance. At frequencies higher than  $BW$ , the noise due to  $R_{eq}$  is filtered by the equivalent capacitor.

Since the noise across  $C_{eq}$  is uncorrelated during phases  $\phi_1$  and  $\phi_2$  of the converter, their PSDs should be added together. Hence, the total output-referred, single-sided PSD can be written as

$$S(f) = A_V^2 \left( S_{d\phi_1}(f) + S_{d\phi_2}(f) + S_{fol\phi_1}(f) + S_{fol\phi_2}(f) \right), \quad (40)$$

where  $S_{d\phi_1}(f)$ ,  $S_{d\phi_2}(f)$ ,  $S_{fol\phi_1}(f)$  and  $S_{fol\phi_2}(f)$  are the PSD due to the direct and the folded noise during  $\phi_1$  and  $\phi_2$ .  $A_V$  is a scaling factor for referring the noise to the output and can be calculated by

$$A_V = \frac{C_{eq}}{C_{OUT}}. \quad (41)$$

#### D. Reverse Isolation of SC DC-DC Converters

Similarly to the approach used for the LDO, this subsection investigates the side effects of a noise coupled into the output of the DC-DC converter. When a current noise,  $i_n$ , is injected at the output node of the converter shown in Fig. 8(a), the current noise that reaches the input can be expressed as

$$\frac{i_{n,in}}{i_n} = CR \cdot \frac{R_L}{R_L + R_{OUT} + R_S \cdot CR^2}. \quad (42)$$

Since  $R_L \gg (R_{OUT} + R_S \cdot CR^2)$ , Eq. (42) can be simplified to  $CR$ . In contrast to the LDO structure, the injected current noise is *firstly* attenuated by  $CR$  (e.g.,  $CR=0.5$  or  $0.66$ ) when it is

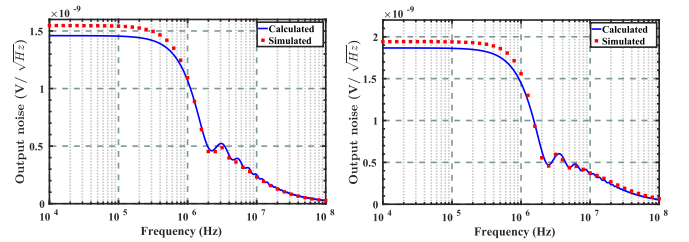


Fig. 10. Calculated (solid line) and simulated (dotted line) output noise of the DC-DC converter for the (a) 2:1 and (b) 3:2 configurations with  $C_{fly} = 1$  nF,  $C_{OUT} = 1$  nF,  $R_{on} = 30 \Omega$  and  $f_{sw} = 1.25$  MHz.

referred to the input and then be converted into voltage noise through resistor  $R_S$ . Similarly, due to  $i_n$ , the current noise that flows through the load can be written as

$$\frac{i_{n,out}}{i_n} = \frac{R_{OUT} + R_S \cdot CR^2}{R_L + R_{OUT} + R_S \cdot CR^2} \approx \frac{R_{OUT}}{R_L}. \quad (43)$$

This equation reveals that the output current noise is also reduced by the converter. However, the attenuation is smaller compared to that of the LDO, where the noise is attenuated by the open-loop gain.

#### E. Verification

The noise of a DC-DC converter with  $C_{fly} = 1$  nF,  $C_{OUT} = 1$  nF,  $f_{sw} = 1.25$  MHz and  $R_{on} = 30 \Omega$  is simulated in Cadence by means of a Pnoise simulation. As shown in Fig. 10, the simulation results are in close accordance with the predicted values of Eq. (40) for the 2:1 and 3:2 configurations. At any frequency, the noise of the DC-DC converter is well below the noise voltage tolerated by the oscillator (i.e.  $< 38$  nV/√Hz @ 10 MHz).

Fig. 8(c) shows the simulation results related to the injected current noise at the converter's output. At DC, the simulation results are in close accordance with Eqs. (42) and (43). For

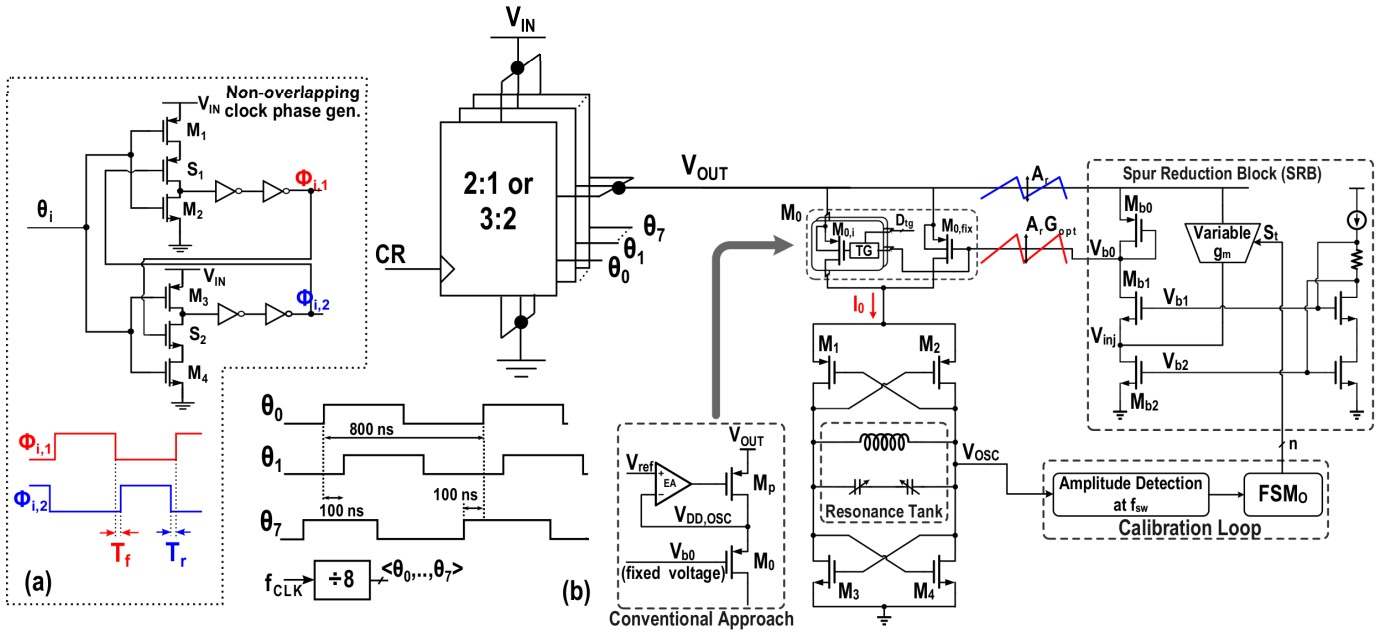


Fig. 11. (a) Schematic of the non-overlapping phase generator; (b) System level representation showing the 2:1 or 3:2 reconfigurable SC stage directly connected to the oscillator.

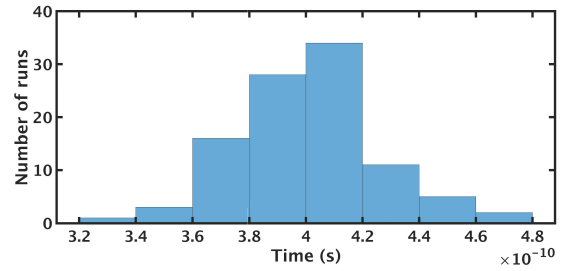
frequencies above 10 MHz, the input-referred noise is gradually being filtered by the on-chip flying capacitance of the converter. Whereas, the output referred noise is hardly filtered, as can be gathered from the red curve. This is mainly due to the lack of the output filtering capacitance of SC DC-DC converters.

## V. SYSTEM DESIGN

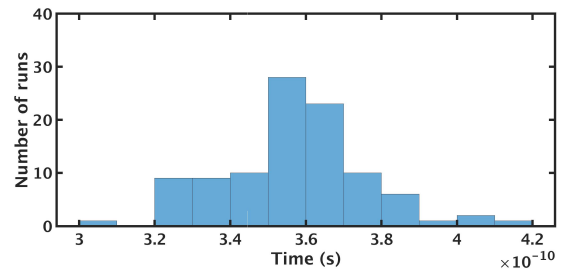
Given the clear advantages in terms of output noise and power efficiency of the SC DC-DC converter compared to an LDO-based approach, in this section an alternative solution is proposed, in which the DC-DC converter directly powers up the oscillator.

The DC-DC converter consists of a 2:1 or 3:2 stage, as discussed in the previous section. The stage is divided into 8 smaller units driven by 8 interleaved phases ( $\Phi_0, \dots, \Phi_7$ ), as shown in Fig. 11. The total on-chip capacitance  $C_{fly} = 1$  nF is equally divided into the 8 units, while each switch has a width of  $\sim \frac{W_{opt}}{8}$  and is operated at  $f_{SW} = \frac{f_{CLK}}{8} = 1.25$  MHz, as discussed in the previous section. The practical implementation of this technique comes at the expense of circuit overhead due to the generation and routing of all the different phases. From circuit simulations, 8 interleaving units are found to be the best trade-off between circuit overhead and benefits coming from the interleaving technique. By implementing an interleaved converter, the output capacitance  $C_{OUT}$  can be omitted, as each unit sees a load capacitance equal to the flying capacitance of the other units operated in the opposite phase. In [36], the benefits of adopting such an interleaving technique are further discussed.

Each unit generates two non-overlapped clock phases,  $\phi_1$  and  $\phi_2$  directly from  $\phi_i$ . To ensure non-overlapped condition between  $\phi_1$  and  $\phi_2$ , each of the 8 units embeds a non-overlapping circuit, whose schematic is shown in Fig. 11 (a).



(a)



(b)

Fig. 12. Monte Carlo simulations (100 runs) of the non-overlapping time between  $\Phi_1$  and  $\Phi_2$  (a) for the rising ( $T_r$ ), and (b) for the falling event ( $T_f$ ).

To quantify the non-overlapping time,  $T_r$  ( $T_f$ ) is defined as the time difference between the falling (rising) edge of  $\phi_1$  ( $\phi_2$ ) and the rising (falling) edge of  $\phi_2$  ( $\phi_1$ ). By adding switches  $S_1$  and  $S_2$ , which are directly driven by,  $\phi_1$  and  $\phi_2$ , each phase of the clock can change state only when the other phase has already switched, thus guaranteeing the non-overlapping condition. To guarantee that the non-overlapping condition is satisfied over process variation and device mismatch, a Monte-Carlo simulation with 100 points has been performed, and the results are shown in Fig. 12. Both  $T_r$  and  $T_f$  are always greater than zero, proving that the non-overlapping condition is met.

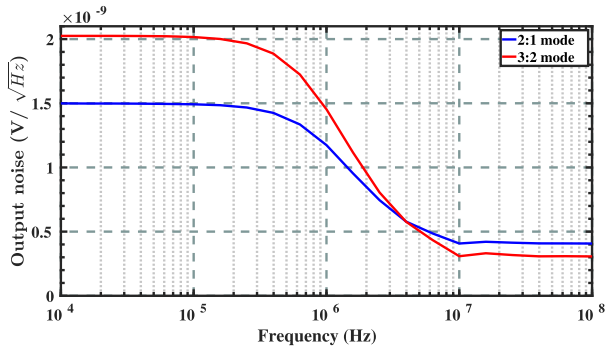


Fig. 13. Simulated output noise of the 8-unit interleaving converter for the two different configurations.

Fig. 13 shows the simulated output noise of the interleaved DC-DC converter in the 2:1 and 3:2 mode. The output noise of the converter is always below the noise requirement derived in Section II (i.e.,  $< 38 \text{ nV}/\sqrt{\text{Hz}}$ ), thereby preserving the oscillator inherent PN.

Fig. 11 (b) shows the block diagram of the oscillator with its spur-reduction block (SRB), which is based on our previous work in [10]. In the conventional LDO-based approach, the tail transistor,  $M_0$ , which is used to adjust the DC level of the oscillator current  $I_0$ , is placed in cascade with the pass transistor of the LDO, whose function is to stabilize the internal supply voltage of the oscillator. By removing the LDO,  $M_0$  is now directly connected to the converter output. In this design,  $M_0$  also contains a bank of unit transistors  $M_{0,i}$  that can be switched on separately through the corresponding transmission gate (TG) to set the DC level of  $I_0$  for optimum oscillator performance. Meanwhile, to tolerate the ripple on the converter output, a conventional oscillator biasing network is modified into the SRB with only  $20 \mu\text{A}$  extra power consumption. The SRB replicates the supply ripple to the gate terminal of  $M_0$  with a proper gain  $G$ , in order to stabilize  $I_0$  under supply variation, which in turn suppresses the spur level at the oscillator output. The optimum gain  $G_{\text{opt}}$  is found by sweeping the control code of the variable  $g_m$  stage with a finite-state machine (FSM<sub>O</sub>). Once the monitored oscillation amplitude variation at  $f_{\text{SW}}$  reaches its minimum, FSM<sub>O</sub> fixes the corresponding gain as  $G_{\text{opt}}$ . Such a calibration process is only performed at the system start-up, and the same calibrated  $G_{\text{opt}}$  is used for the rest of the operation. Note that for the extra noise of the SRB, only those around the DC and even harmonics of the oscillation frequency ( $f_0$ ) would be converted to phase noise [37]. The PN degradation due to the flicker noise of the SRB around DC is suppressed by tuning the common-mode resonance frequency of the oscillator to around  $2f_0$  [13], [38]. For thermal noise at even harmonics of  $f_0$ , their effect is suppressed due to the limited bandwidth of the SRB. For good enough spur suppression, the bandwidth of the single-pole SRB is  $\sim 200 \text{ MHz}$  in this design to guarantee replicating the ripples with low enough phase shift. In contrast,  $f_0$  is in gigahertz range (i.e., 4.9–5.5 GHz in this design). Hence, the thermal noise of the SRB is suppressed by at least 33.8 dB, and becomes negligible. A more detailed description of the SRB can be found in [10].

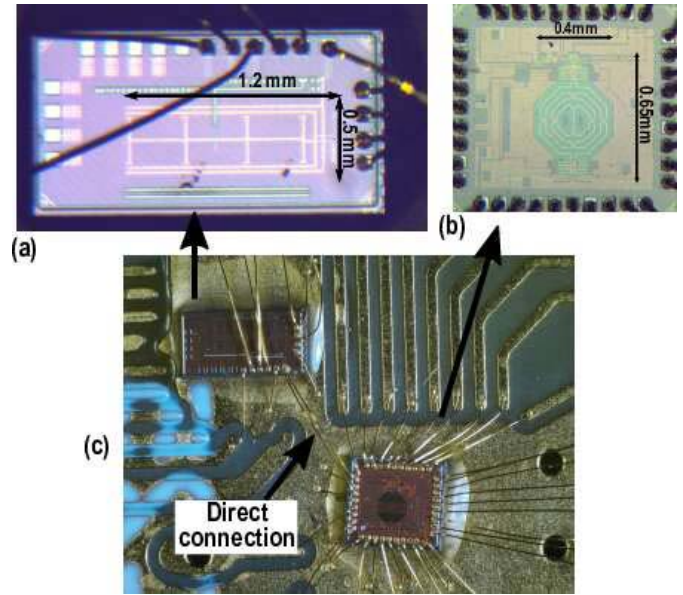


Fig. 14. Chip micrographs of (a) the DC-DC converter, and (b) the oscillator; (c) A photo highlighting their direct connection.

## VI. EXPERIMENTAL RESULTS AND COMPARISON

The DC-DC converter and the oscillator have been fabricated in the same standard 40-nm CMOS process. Their chip micrographs, as well as a photo highlighting their direct connection, are shown in Fig. 14. The two circuits occupy an active area of  $0.6 \text{ mm}^2$  and  $0.23 \text{ mm}^2$ , respectively. The  $f_{\text{CLK}} = 10 \text{ MHz}$  clock signal of the DC-DC converter is provided externally, while the 8 phases at  $f_{\text{SW}} = 1.25 \text{ MHz}$  are generated on-chip.

### A. Measurement Results

In Fig. 15(a), the simulated and the measured power efficiency of the DC-DC converter in the two configurations and for different  $V_{\text{IN}}$  values are shown. The average currents needed to compute the power efficiency are measured with a Keithley 6430 source-meter. The peak power efficiency is 83% and 80% for the 2:1 and the 3:2 mode, respectively. In the 3:2 mode, the output impedance of the converter increases, degrading the power efficiency, as predicted by Eq. (34). The overdrive voltage of the switches is proportional to  $V_{\text{IN}}$ . As a consequence, at lower values of  $V_{\text{IN}}$ , the  $R_{\text{on}}$  of the switches increases and therefore the power efficiency tends to degrade. Fig. 15(b) shows the DC-DC converter output voltage waveform in the 2:1 mode, while powering up the oscillator. The ripple frequency equals the converter's switching frequency (i.e., 10 MHz), while the ripple amplitude is  $\sim 30 \text{ mV}$ .

The spectrum of the output voltage of the DC-DC converter is shown in Fig. 15(c) and (d) (black line) for the 2:1 and 3:2 configurations, respectively. The main tones are located at multiple integers of  $f_{\text{CLK}}$ , whereas the frequency components due to the interleaving technique are located at multiple integers of  $f_{\text{CLK}}/8 = 1.25 \text{ MHz}$ . Those components are much smaller than the main tones, hence they do not

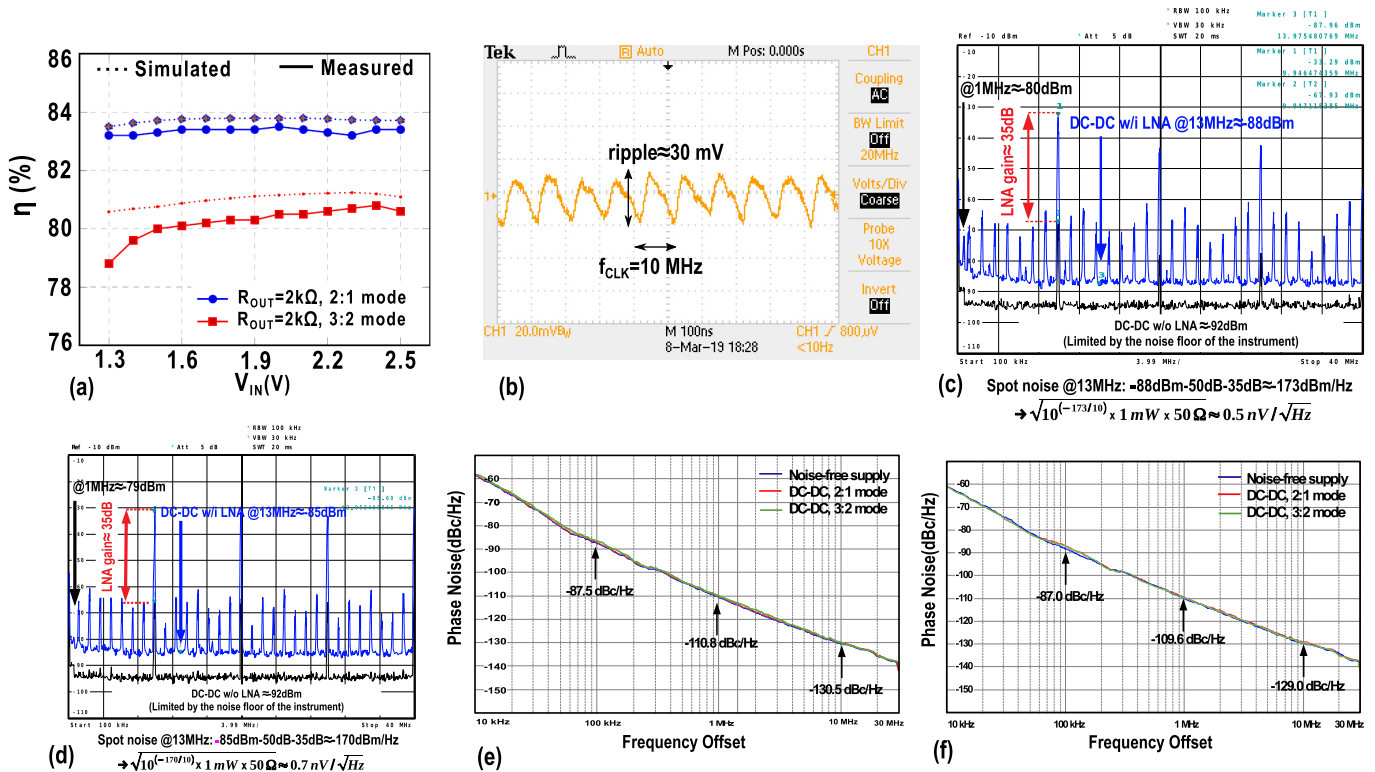


Fig. 15. (a) Measured power efficiency versus  $V_{IN}$ ; (b) output voltage of the DC-DC converter when directly connected to the oscillator; (c) spectrum of the output voltage of the DC-DC converter without (black line) and with (blue line) the use of an LNA in the 2:1 mode and (d) the 3:2 configuration, respectively; (e) phase noise of the oscillator when powered by an ideal supply and the DC-DC converter in the 2:1 mode and 3:2 mode for  $f_0 = 5.5\text{ GHz}$  and (f)  $f_0 = 4.9\text{ GHz}$ .

appear in the spectrum of the oscillator, as the SRB will greatly suppress them. The measurement of the output noise of the DC-DC converter is limited by the noise floor of the spectrum analyzer. Hence, an LNA with a gain of 35 dB is placed after the DC-DC converter. The resulting spectrum is shown in Fig. 15(c) and (d) (blue curve) for the 2:1 and the 3:2 configuration, respectively. When the LNA is used, the amplitude of the peaks is amplified by 35 dB, whereas the noise is amplified by only 7 dB (in the 3:2 mode), proving that the measure is not longer limited by the noise floor of the spectrum analyzer. At around 13 MHz, the measured noise in the 2:1 configuration integrated over the resolution bandwidth of the spectrum analyzer (100 kHz) is  $\approx -88\text{ dBm}$ . As a result, the spot noise at around 13 MHz is  $-88\text{ dBm} - 35\text{ dB} - 10\log_{10}(100\text{ kHz}) = -173\text{ dBm/Hz} \approx 0.5\text{ nV}/\sqrt{\text{Hz}}$ . It is in close accordance with the simulated value (Fig. 13), and much lower than the supply noise tolerated by the oscillator ( $38\text{ nV}/\sqrt{\text{Hz}} @ 10\text{ MHz}$ ).

Fig. 15(e) and (f) show the phase noise of the oscillator when powered from a noise-free supply and from the DC-DC converter in the two different configurations for the oscillator frequency of 5.56 GHz and 4.9 GHz, respectively. The inherent PN of the oscillator is not degraded, proving that the condition imposed by (7) is met and the supply does not limit the oscillator performance. The spectrum of the oscillator powered by the converter is also shown in Fig. 16. The spur level at the initial gain setting of the SRB, which corresponds to  $G \approx 1$ , is as high as  $-40\text{ dBc}$ . After performing an automatic calibration to find the optimum gain setting, the spur level

is reduced by about 27 dB and reaches  $-67\text{ dBc}$ . It is worth mentioning that 27 dB represents the difference of the spur levels between the initial and optimal gain setting of the SRB, which does not represent the PSR of the SRB.

### B. Comparison With the State of the Art

Table III summarizes the performance of the system and compares it with a conventional LDO-based approach. Since the SRB is always functioning, the equivalent PSR of our approach in this table is calculated by the difference between the spur level measured at optimum setting and the calculated one based on the simulated  $K_V$  of the oscillator without SRB. Compared to [6] and [7], our approach exhibits the lowest output noise and a high PSR without the use of an LDO or any external component, thereby avoiding the LDO voltage headroom while achieving the highest power efficiency. Therefore, our work is more suitable for full system integration. Two independent LDO designs ([26], [39]) with relatively high PSR are also added to the table of comparison to highlight the advantages of our structure. [26] requires an external output capacitor, making the voltage regulator bulky. [39] employs a cap-less solution with a drop-out voltage of 200 mV, bringing its power efficiency below 80%.

## VII. DISCUSSION

In a real system-on-chip (SoC), beside the oscillator, there are other modules, that need to be powered with an appropriate voltage. Conventionally, one LDO is used for each module

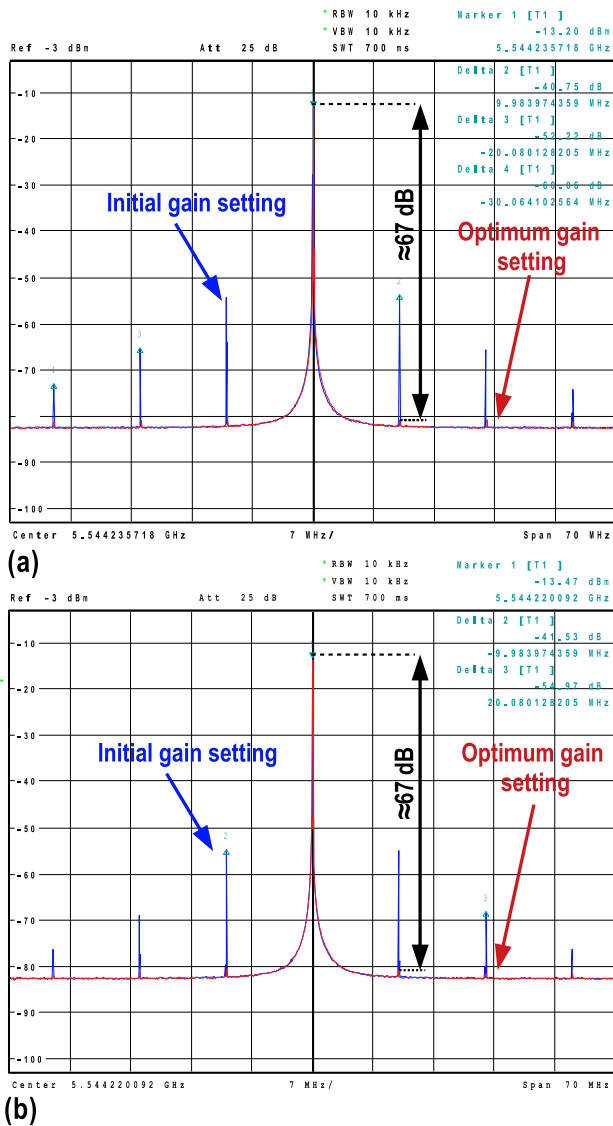


Fig. 16. Oscillator spectrum before and after calibration when directly powered by the DC-DC converter in 2:1 (a) and 3:2 mode (b).

to isolate its supply from others. As shown in Section III.E, below the LDO's dominant frequency, the current noise generated by the aggressor module would not be filtered and would directly appear at the LDO input. Due to the typically small impedance of the power source, the resulting voltage noise is also small. This voltage noise would be further suppressed by the PSR of the oscillator's LDO. Similarly, in our proposed scheme, a *separate* DC-DC converter should be designed for each module. As shown in Section IV.D, the injected current noise at the output of the converter of the aggressor block is first reduced by the CR when referring to the input and then converted to voltage noise with the small impedance of the power source,  $R_S$ . Another converter would then suppress the generated voltage noise by CR when supplies the oscillator. The rest of the rejection is guaranteed by the SRB that provides an equivalent PSR as the LDO. Consequently, the proposed approach enjoys the additional attenuation of  $CR^2$  compared to the LDO scheme.

TABLE III

PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

	This work	JSSC15 [2]	ESSCIRC14 [6]	JSSC17 [24]	CICC17 [36]	
System Architecture	DC-DC+ OSC	LDO+ OSC**	LDO+ OSC	LDO	LDO	
CMOS tech	40 nm	55 nm	65 nm	130 nm	65nm	
$V_{IN}$ (V)	2.2@2:1 1.65@3:2	1.4	0.6	1.05-2.0	1.2	
$V_{OUT}$ (V)	1.0	1.2	0.4	1.0	1.0	
$C_{OUT}$ (F)	-	>6p	390p	1 $\mu$	<240p	
Noise (nV/ $\sqrt{Hz}$ )	<0.7@ 13MHz 0.9@1MHz	-	22.4#@ 10MHz	100@ 1MHz	-	
#ext. components	0	0	0	1	0	
$\eta$ (%)	83@2:1 81@3:2	<80	<60	<95	<80	
LDO voltage headroom (mV)	0	200	200	50	200	
PSR (dB)	@5MHz	-48.9 <sup>†</sup>	-20	-31 <sup>†</sup>	-27 <sup>†</sup>	-48
	@10MHz	-45 <sup>†</sup>	-20	-26 <sup>†</sup>	-33 <sup>†</sup>	-50

\*PSR of the SRB (simulated value) \*\*Oscillator is part of the whole transceiver

#Calculated from phase noise with  $K_{SUP}=50$  MHz/V <sup>†</sup>Simulated value

## VIII. CONCLUSION

In this article, we have developed guidelines for designing the supply voltage block of LC oscillators to preserve their spectral purity. First, the requirements on the ripple and noise of the supply have been quantified. An analog LDO and a switched-capacitor DC-DC converter were designed to meet those requirements. Given the poor LDO efficiency, a 2:1 or 3:2 switched-capacitor DC-DC converter is implemented and, as a proof of concept, it is directly connected to the oscillator. The converter's peak power efficiency is 83%, while its output noise is  $< 0.9$  nV/ $\sqrt{Hz}$  at 1 MHz and does not degrade the inherent oscillator phase noise. The spur reduction block embedded in the oscillator suppresses the spurs induced by the DC-DC converter ripple down to  $-67$  dBc.

## REFERENCES

- [1] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
- [2] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- [3] M. Babaie and R. B. Staszewski, "A Class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
- [4] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.
- [5] F. Wang and H. Wang, "A noise circulating oscillator," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 696–708, Mar. 2019.
- [6] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.
- [7] L. Fanori, T. Mattsson, and P. Andreani, "A Class-D CMOS DCO with an on-chip LDO," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 335–338.

- [8] W. Hou, S. Li, G. D. Geronimo, and M. Stanacevic, "An ultra-low-noise LDO regulator in 65 nm for analog front-end ASICs in cryogenic environment," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Proc. (NSS/MIC)*, Nov. 2018, pp. 1–4.
- [9] J. Torres *et al.*, "Low drop-out voltage regulators: Capacitor-less architecture comparison," *IEEE Circuits Syst. Mag.*, vol. 14, no. 2, pp. 6–26, 2nd Quart., 2014.
- [10] Y. Chen *et al.*, "A supply pushing reduction technique for LC oscillators based on ripple replication and cancellation," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 240–252, Jan. 2019.
- [11] I. Galton and C. Weltin-Wu, "Understanding phase error and jitter: Definitions, implications, simulations, and measurement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 1–19, Jan. 2019.
- [12] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F<sub>2</sub> CMOS oscillator with 191 dBc/Hz FoM and long-term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.
- [13] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.
- [14] R. Magod, N. Suda, V. Ivanov, R. Balasingam, and B. Bakkaloglu, "A low-noise output capacitorless low-dropout regulator with a switched-RC bandgap reference," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2856–2864, Apr. 2017.
- [15] X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A LDO regulator with weighted current feedback technique for 0.47 nF–10 nF capacitive load," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2658–2672, Nov. 2014.
- [16] Y. Lim *et al.*, "An external capacitor-less ultralow-dropout regulator using a loop-gain stabilizing technique for high power-supply rejection over a wide range of load current," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 11, pp. 3006–3018, Nov. 2017.
- [17] J. C. Tell, "Understanding noise in linear regulators," *Analog Appl. J.*, pp. 5–8, Apr. 2005. [Online]. Available: <http://www.ti.com/lit/an/slyt201/slyt201.pdf>
- [18] T. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design* (Analog Integrated Circuit Design). Hoboken, NJ, USA: Wiley, 2011.
- [19] B. Yang, B. Drost, S. Rao, and P. K. Hanumolu, "A high-PSR LDO using a feedforward supply-noise cancellation technique," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2011, pp. 1–4.
- [20] G. A. Rincon-mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.
- [21] E. Rogers, "Stability analysis of low-dropout linear regulators with a PMOS pass element," *Analog Appl.*, Texas Instrum. Incorporated, Dallas, TX, USA, Tech. Rep., Aug. 2005, pp. 10–13. [Online]. Available: <http://pdfs.icssupply.com/server131/dsa/3/381873.pdf>
- [22] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, "An external capacitorless low-dropout regulator with high PSR at all frequencies from 10 kHz to 1 GHz using an adaptive supply-ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2675–2685, Sep. 2018.
- [23] K. Wong and D. Evans, "A 150mA low noise, high PSRR low-dropout linear regulator in 0.13  $\mu\text{m}$  technology for RF SoC applications," in *Proc. 32nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2006, pp. 532–535.
- [24] D.-K. Kim and H.-S. Kim, "A 300 mA BGR-recursive low-dropout regulator achieving 102-to-80dB PSR at frequencies from 100 Hz to 0.1 MHz with current efficiency of 99.98%," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C132–C133.
- [25] H. Abbasizadeh *et al.*, "A design of ultra-low noise LDO using noise reduction network techniques," in *Proc. Int. SoC Design Conf. (ISOC)*, Nov. 2017, pp. 198–199.
- [26] Q.-H. Duong *et al.*, "Multiple-loop design technique for high-performance low-dropout regulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2533–2549, Oct. 2017.
- [27] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.
- [28] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 356–360, Jun. 2012.
- [29] K. Nang Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.
- [30] F. Lavalle-Aviles, J. Torres, and E. Sanchez-Sinencio, "A high power supply rejection and fast settling time capacitor-less LDO," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 474–484, Jan. 2019.
- [31] T. V. Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY, USA: Springer, 2013.
- [32] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Dept. EECS, Univ. California, Berkeley, Berkeley, CA, USA, May 2009. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html>
- [33] T. M. Andersen, "On-chip switched capacitor voltage regulators for granular microprocessor power delivery," Ph.D. dissertation, Dept. D-ITET, ETH Zürich, Zürich, Switzerland, 2015.
- [34] R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*. Hoboken, NJ, USA: Wiley, 1986.
- [35] B. Murmann, "Thermal noise in track-and-hold circuits: Analysis and simulation techniques," *IEEE Solid State Circuits Mag.*, vol. 4, no. 2, pp. 46–54, Spring 2012.
- [36] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.
- [37] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.
- [38] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A 1/f noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.
- [39] Y. Lim, J. Lee, S. Park, and J. Choi, "An external-capacitor-less low-dropout regulator with less than -36dB PSRR at all frequencies from 10kHz to 1GHz using an adaptive supply-ripple cancellation technique to the body-gate," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr./May 2017, pp. 1–4.



**Alessandro Urso** (Student Member, IEEE) was born in Lecce, Italy, in 1991. He received the bachelor's and M.Sc. degrees (*cum laude*) in electronic and telecommunications engineering from the University of Ferrara, Italy, in 2013 and 2015, respectively. He is currently pursuing the Ph.D. degree with the Section Bioelectronics, Delft University of Technology, Delft, The Netherlands. His research interests include the design of power efficient neural stimulator and the design of switched capacitor dc–dc converter for energy harvesting application.



**Yue Chen** (Student Member, IEEE) received the B.Eng. degree in microelectronics and the M.Eng. degree in electronic science and technology from Xian Jiaotong University, Xi'an, China, in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree in electronic engineering with the Microelectronics Department, Delft University of Technology, Delft, The Netherlands. His current research interests include frequency synthesizer techniques and integrated circuits for wireless communications.



**Johan F. Dijkhuis** (Member, IEEE) received the M.S. degree in electrical engineering from the University of Twente in 1998. From 1998, he has worked as a RF and an Analog Design Engineer for Philips Semiconductor, NXP, ST-Ericsson, and NVIDIA. Since 2014, he has been with the Holst Centre/imec-NL. His research interests include ultra-low power RF circuit design and power management circuits for ultra-low power radios.



and healthcare applications. He currently serves as a Technical Program Committee of the IEEE ISSCC and the RFIC Symposium.

**Yao-Hong Liu** (Senior Member, IEEE) received the Ph.D. degree from National Taiwan University, Taiwan, in 2009. He was with Terax, Via Telecom (now Intel), and Mobile Devices, Taiwan, from 2002 to 2010, working on Bluetooth, WiFi, and cellular wireless SoC products. Since 2010, he joined imec, The Netherlands. He is currently a Principal Membership of Technical Staff. He is leading the development of the ultra-low power wireless IC design. His research interests include energy-efficient RF transceivers and radar for the IoT



Delft University of Technology, where he is currently a tenured Assistant Professor. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie has been a Committee Member of the Student Research Preview (SRP) of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017. He is currently serving on the Technical Program Committee of the IEEE European Solid-State Circuits Conference (ESSCIRC). He was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award and the 2019 IEEE ISSCC Best Demo Award. In 2019, he received the Veni Award from the Netherlands Organization for Scientific Research (NWO).

**Masoud Babaie** (Member, IEEE) received the Ph.D. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016.

In 2006, he joined the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From 2009 to 2011, he was a CTO of that company. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the



**Wouter A. Serdijn** (Fellow, IEEE) was born in Zoetermeer (Sweet Lake City), The Netherlands, in 1966. He received the M.Sc. (*cum laude*) and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively.

He is currently a Full Professor of bioelectronics with the Delft University of Technology, where he heads the Section Bioelectronics, and a Medical-Delta Honorary Professor with the Delft University of Technology and the Erasmus Medical Center, Rotterdam. His research interests include integrated biomedical circuits and systems for biosignal conditioning and detection, neuroprosthetics, transcutaneous wireless communication, power management, and energy harvesting as applied in, e.g., cardiac pacemakers, cochlear implants, neurostimulators, bioelectronic medicine, and electroceuticals. He is the Co-Editor and a co-author of ten books, eight book chapters, four patents, and more than 300 scientific publications and presentations. He teaches Analog Integrated Circuit Design, Active Implantable Biomedical Microsystems, and Bioelectronics.

Dr. Serdijn is an IEEE Distinguished Lecturer and a mentor of the IEEE. In 2016, he received the IEEE Circuits and Systems Meritorious Service Award and the Electrical Engineering Best Teacher Award in 2001, 2004, and 2015. He has served, a.o., a General Co-Chair for the IEEE ISCAS 2015 and the IEEE BioCAS 2013, a Technical Program Chair for the IEEE BioCAS 2010 and the IEEE ISCAS 2010, 2012, and 2014, a member for the Board of Governors (BoG) for the IEEE Circuits and Systems Society from 2006 to 2011, a Chair of the Analog Signal Processing Technical Committee for the IEEE Circuits and Systems Society, and the Editor-in-Chief for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2010 to 2011. He is a Chair of the Steering Committee and an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (T-BioCAS). More information on Prof. Serdijn can be found at: <http://bioelectronics.tudelft.nl/~wout>.