DELFT UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering, Mathematics and Computer Science
MSc Sustainable Energy Technology

DC-DC Bidirectional Converter with USB Type-C for Power Delivery

Master Thesis

Nikitas G. Karatzaferis

Supervisor

Dr.ir. Laura Ramirez Elizondo

Advisor

L.J. (Laurens) Mackay

Committee Members

Prof.dr. P. Bauer

Dr.ir. Laura Ramirez Elizondo

Dr.ir. Milos Cvetkovic

Dedicated to

To my family who has supported me in every aspect of my life, has provided me the opportunity to make dreams but also taught me to work hard with devotion and passion to succeed my life goals.

To my partner and future wife Freda who has supported me in the most difficult times, has inspired me to become a better man and has given me the strength to continue and succeed my goals.

To my dear friends who have been always there for me, in good and bad situations, have advised me when I needed and helped me to make my free time fun and unforgettable.

Abstract

Focusing on real life commercial applications, this thesis presents the theoretical and practical control requirements of an application board, which exploits flexible bidirectional DC-DC converters, to power up a unit of multi USB type-C ports. Emphasis is given in the power management between the connected devices since the power flow is bidirectional.

The USB type-C interface allows power management between the devices and offers the possibility of using the Li-ion batteries of the end-devices as a backup power source in case of a blackout or source failure. At the beginning of this research, the appropriate topology of the converter is defined based on the requirements of the application. The power stage and the system control is fully simulated to prove the application concept. The final stage is the design and implementation of the real application board to extract useful results regarding the viability and feasibility of producing such an integrated solution.

The results arising from the application board prove the real application use. This research topic is setting the foundations for a further research on future applications of the USB type-C interface, in commercial or domestic buildings which are powered by a DC network.

Keywords: *USB type-C, USB-C Power delivery, DC-DC converter, bidirectional converter, synchronous converter, buck-boost converter, non-isolated DC converter, DC converter control, PID control, PCB design, C2000 microcontroller, STM32 microcontroller.*

Contents

TABLE OF FIGURES

INTRODUCTION

Since the beginning of the 19th century, when the first electrical grids were set and the importance of electrical energy became vital for society, continuous research was implemented to improve and evolve the electrical energy transmission and distribution. The initial dilemma between AC and DC networks, introduced by Nicola Tesla and Thomas Edison, was at the time resolved due to the premature semiconductor technology thus, AC conquered as the best solution for power generation and distribution [1].

A chain sequence of events during the last decades as the increasing negative environmental impacts due to the excess use of fossil fuels and the continuous technological improvement of semiconductor materials, opened the way to the introduction of renewable energy sources in the energy field. From an environmental point of view, it is a fact that the penetration of renewable energy sources in the energy market has a proven positive impact in the reduction of the levels of greenhouse gases as well as the protection of the natural landscape of the planet. From a technical point of view, the introduction of sustainable energy sources, imposed the need for further research on the DC distribution grids. Fortunately, the last years have shown that the support of the electrical grid by renewable sources is feasible both technically and economically [2].

The increased participation of renewables in the centralized and decentralized grids, in combination with the growing demand for power delivery that modern society dictates, accommodates the need for an innovative approach in the management of the electrical grids. In the quest of a grid with high efficiency, capacity and reliability, the management of the electrical power sources has to be done in the most efficient way. The introduction of “smart grids” was one way to address this need for an efficient solution. Smart grids represents the use of individual smart technologies such as smart meters, sensors, energy storage and power management systems in order to ensure an optimal use of the available resources [3]. By exploiting the modern technology infrastructures, “smart grids” can provide energy in the most effective way, even in difficult ranging conditions and failing events. More specifically, a “smart grid” is capable of reacting immediately in a failing event at any point of the grid such as power generation, transmission and distribution. An example can be the unlikely event of a voltage transformer failure, when the power flow can directly change to an alternative path and information regarding the failure can be provided to the central management system. In this way, the reliability of the system is improved and the downtime is decreased significantly [4].

Focusing more on the future of smart grids, the incorporation and participation of multiple energy providers such as smart buildings and smart houses, is of great importance due to their high potential of energy generation. Nowadays, a rising number of commercial buildings and smart houses, are producing their own energy through installed renewable sources. As in smart grid technology, the technological infrastructure is also being used by smart buildings in order to realize a more local power management. The term “Nano-grid” is important to address which presents the management of power generation and distribution inside a smart building.

The application of a DC smart building has increasing popularity in recent years. The idea of a DC building is based on a power distribution network which is using DC power since, as of today, most of the electrical and electronic devices operate on DC. Currently, in a smart building that uses renewable sources, there is a need for the power to be converted to AC first for distribution and back to DC to provide power to the devices. This is a rather inefficient way of power distribution, due to the losses occurring in each power conversion, which could be minimized by using a DC electrical network.

There are multiple possible configurations for a DC network in a building. A reasonable solution is comprising of two DC voltage buses. A high voltage bus of 380VDC for high-power appliances, and a low voltage bus of 24VDC for small appliances and lighting [5]. The supply of

these buses could come from renewable sources, such as PV panels, connected directly to the main high voltage bus. Through a step-down conversion the 24VDC bus could be supplied from the high voltage bus.

In the line of creating a smart building operating on DC power produced mainly by renewable sources, the existence of an energy storage system which could serve as a back–up supply in case of source failures or inefficient power delivery, is essential. When considering the idea of creating a back-up grid, Li-ion batteries provide an optimal solution. Today, most of the end-devices such as laptops, smartphones and tablets existing in a commercial building or a house, are equipped with high capacity Li-ion batteries. The Li-ion batteries serve as power supplies for the standalone use of the devices. The electrical network of a building, through power conversion (AC/DC converters), supports the charging of those devices. This leads us to the question of *how could the high capacity Li-ion batteries of end devices support the energy storage system as a back-up power supply?* As already stated in the case of a building using DC power, two DC buses are present to support powering of the interconnected devices. If the interconnected devices were able to supply DC power from their Li-ion batteries back to the DC buses, then they could actively participate in the local energy storage system as power cells. The success of this bidirectional power flow is dictating the need for a DC-DC conversion with no fixed source and sink capabilities. A solution to this challenge is the use of a DC-DC buck boost bidirectional converter introduced by Vinciarelli [6].

The next challenging topic is whether there is an interface that can support bidirectional power flow. Currently, most of the end-devices are equipped with a USB type A or type B connector which serves the purpose of data communication and charging of the Li-ion batteries. *But what if there was a USB interface that could support bidirectional power flow from and to the devices?* In the search of new innovative methods of power delivery, a new USB type-C port has been released on the market offering multiple possibilities for various applications. Some of the most important features that the type C port can offer is high power delivery standards up to 100W and bidirectional power flow which means no fixed host or client. Furthermore, optimization of power management across multiple peripherals is possible by allowing each device to take only the power it requires, and to get more power when required for a given application [7].

In conclusion, in order to address the need for an integrated solution which would support bidirectional power flow between end-devices using the USB-type C interface, the main objective of this research is;

"The building of a DC-DC buck boost bidirectional converter with a USB type-C interface for power delivery"

Research Target

The aim of this research is to propose a new solution for power management and distribution between the interconnected end-devices of a smart building with the use of the type–C interface. Additional aims of this research are to understand:

- How could power management between the connected devices be accomplished, through the use of the USB type-C Power Delivery Protocol (PD protocol)?
- How could the host devices be used to power up the DC "Nano-grid" as a backup?
- How can the bidirectional power flow be accomplished from controlling point of view of the bidirectional converter?

Thesis Outline

This master thesis will focus on the building of a DC-DC bidirectional converter that will be able to deliver or acquire power from a USB type-C port. The thesis is organized in seven chapters and an overview of each chapter is described below.

The introductory chapter one is explaining briefly the reasons that the DC electrical networks are becoming more attractive solutions, since they are presenting high potential in the energy transmission and distribution. The terms of a “smart-grid” and a “Nano grid” are addressed, in order to emphasize the need for a high and low level power management. A further focus is made on addressing the important role of smart buildings in the implementation of a smart-grid. An effort is made to demonstrate the way the end-devices could contribute in the energy storage system of a building. An introduction to the new USB type-C interface, in collaboration with a bidirectional DC-DC converter, aims to provide a solution of supporting a smart building electrical “Nano grid”.

The second chapter is focusing on the new USB type-C interface, providing information on the benefits and possibilities that this interface could offer. The use of the type-C interface for power delivery applications dictates the need for a power management protocol. The purpose of this protocol would be the optimization of power management across multiple peripherals by allowing each device to negotiate the required power, voltage and current levels. The implementation of the protocol in discrete power profiles is being described. Finally, the way the port role is being resolved (as DFP, UFP or DRP) is presented along with some examples for deeper understanding of the challenge.

In the third chapter, the choice of the DC-DC converter topology is explained based on the requirements of the application that this thesis is focusing on. Some more detail is provided regarding the technical background of the chosen topology, the theoretical analysis of the topology as well as the calculations of the most important components of the system.

In the fourth chapter the analysis of the proposed controlling theory is detailed. A functional block diagram of the control is presented, focusing on the interaction between the different operational modes and the power flow swap. Furthermore, the simulation of the system in Simulink is presented. The simulation includes both the power stage and the control as well as the results occurring during the simulations. The control is done based on the different discrete power profiles that the application dictates. The simulation step is necessary to understand and overcome the difficulties of creating a stable control. A model based design helps in defining critical values and parameters of the system, without jeopardizing the safety of the application board.

In the fifth chapter there is a detailed explanation of the hardware choices, component selection and placement. Critical choices made during PCB designing are discussed. A functional specification of the application board will be provided.

Furthermore, chapter six contains all the results arising from the qualification of the application board. All the challenges and difficulties faced during the building of the application, will be discussed along with issues that were not able to be resolved within the scope of this thesis. Those points will provide stimulating questions for further research in the future.

Finally, chapter seven will be the closing chapter where all the conclusions of this research will be addressed. A discussion will be made upon the concluding answers given on the research questions that were stated at the beginning of the thesis. In this final chapter, there will be discussions upon challenging topics, which arise during the implementation of this thesis and present plausible interest for further research.

USB TYPE-C

The most common and successful serial interface that is being used by almost every electronic device is the Universal Serial Bus (USB). Initially, the USB interface was developed to provide serial connectivity between computer peripherals such as keyboards, printers, pointing devices and similar applications. Through gradual upgrades, the USB interface was able to provide both data communication and power supply to the end device. The emerging new computing platforms and electronic devices dictated the need for thinner and lighter USB connectors that the existing USB-A and USB-B standards could not cover. Moreover, the idea of developing a single cable that could satisfy the needs of high data speed, multimedia support and high power delivery for different applications furthered the research for a new USB interface. Thus, the new USB-type C interface appeared on the market in August 2014 [8].

The USB Type-C cable is considered as a "universal" cable solution since it can support fast data transfer with speeds up to 10 GB/s, provides continuous and bidirectional power flow of up to 100Watts and supports ultra-high band video capabilities. The USB Type–C cable is reversible which means that there is no fixed plugging method and can be pluggable in any direction left to right, or upside down. Furthermore, in the USB-type C interface the data and power flow are not fixed, as in previous USB standards. This flexibility offers the opportunity for new applications, since the connected devices can act as hosts, sinks or dual role devices. It is important that the data and power flow remain independent and can be at any moment dynamically altered through the USB Power Delivery protocol [8].

In order to define and better understand the roles of data and power flow through the connected devices, there is a need to address some terms. Regarding the data flow in a USB connection, the term of a downstream facing port (DFP) refers to a port on a USB hub that allows peripheral devices to connect and therefore send data. The term upstream facing port (UFP), refers to a port existing on an end-device and provides connectivity to a USB hub therefore, receiving data. The term dual role data port (DRD), refers to a port that can act both as DFP or a UFP depending on the occurring event. The decision for a DRD to act as a DFP or UFP is being taken by the USB power delivery protocol after an attach event.

On the power flow side, the terms that need to be addressed are those of a source, sink and a dual role power (DRP) port. The term source is referred to a port which can provide power on the V_{BUS} node when attached. A sink is a port that once it is connected, it can consume power from the V_{BUS} node. A DRP is a port that can act both as a source or a sink, with the advantage that this role can always be swapped dynamically. When a DRP is behaving as a source, from data point of view, initially the port acts as a DFP (sending data). In the case that a DRP is operating as a sink, initially the port takes a UFP data role (receiving data). The role of power flow can always change without affecting the data role of the port thus making the two different roles independent [9].

The ability of the USB type-C interface to be fully configurable is given by the introduction of the pair of configuration channels (CC1 and CC2 lines). These two logic channels are used to determine the port attach or detach, the cable orientation as well as the data and power role of every connected device since they are providing all the necessary information to the USB power delivery protocol [10].

USB Type-C pinout

Before introducing the operation of the USB-type C, it is beneficial to present the functional model and pinout of the type-C interface. Figure 1 shows the pinout of the receptacle of a USB type-C [11]. Several new pins are introduced in comparison to the type-A and type B connectors. These pins offer the possibility of high speed data transfer, cable reversibility and bidirectional power flow. All the pins of a receptacle come in almost symmetrical pairs in order to allow the reversible connection of the cable.

The pins appearing on the USB type-C interface have the following functionality:

- TX/RX: SuperSpeed differential pair that can support data transfer speeds up to 10GB/s.
- V_{BUS} node: Power bus supporting up to 100Watts.
- GND: Return signal path.
- CC1/CC2: Configuration channels used for cable attach event, cable orientation, maximum current advertisement and port role swap when a PD is available.
- SBU1/SBU2: Sideband lines for low speed data transmission. These lines can be used only during “alternate mode” with USB PD.
- D+/D- : High Speed differential pair used for USB 2.0 data, supporting speeds up to 480Mbps.

Figure 2 shows the cable side of the USB type-C interface. In the cable side there is only one pair of D+/D- pins since according to the specifications of the Type-C, it is permitted to short the D+ with D+ and D- with D- signal since the data transfer speeds are relatively low thus, the noise levels introduced are quite small. The CC1 and CC2 lines are reversed in order to allow the detection of cable orientation. The TX/RX pairs are also flipped. Since the data speed on these lines is very high, shorting the common lines is not acceptable because high noise is introduced. This problem is resolved in one of two ways. Either, two physical layers (PHYs) are needed and depending on the cable orientation only one would be active, or a SuperSpeed MUX which switches to the correct line depending on the orientation [9].

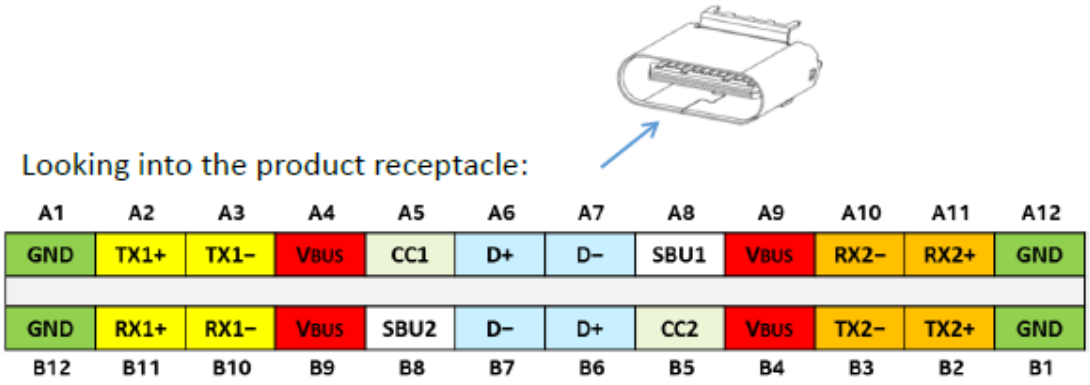


Figure 1. USB type-C receptacle pinout [12]

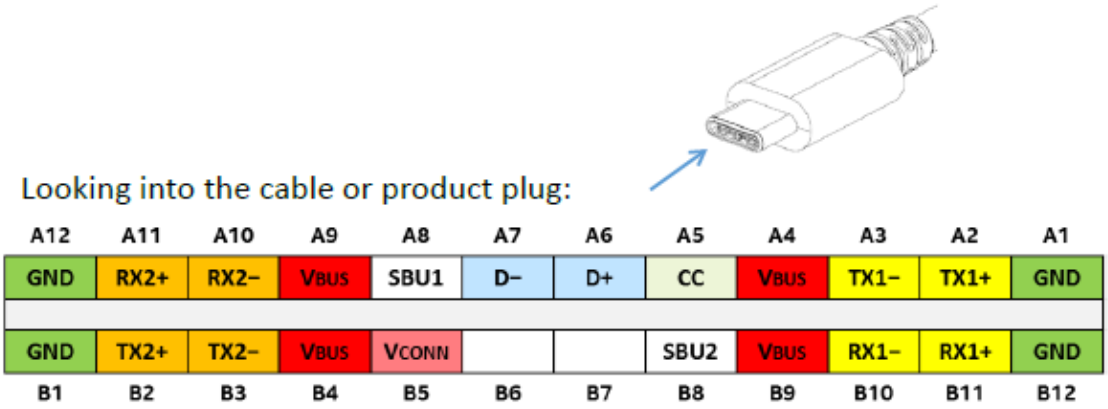


Figure 2. USB type-C cable pinout [12]

Type-C without PD

In the simple case of a connected device operating as a UFP, which would not require high speed data exchange, the USB 2.0 PHY would be responsible to transfer the data of D+ and D- lines between the type-C port and the processor. According to the specifications of USB type-C the shorting of the D line pairs, by connecting D+ to D+ and D- to D- is allowed. However, it is recommended to include a USB 2.0 MUX in order to realize high signal integrity [7].

The configuration channel (CC) is always dedicated to provide information regarding the cable orientation and current-carrying capability. Figure 3, shows the block diagram of an application without the use of the PD manager [9].

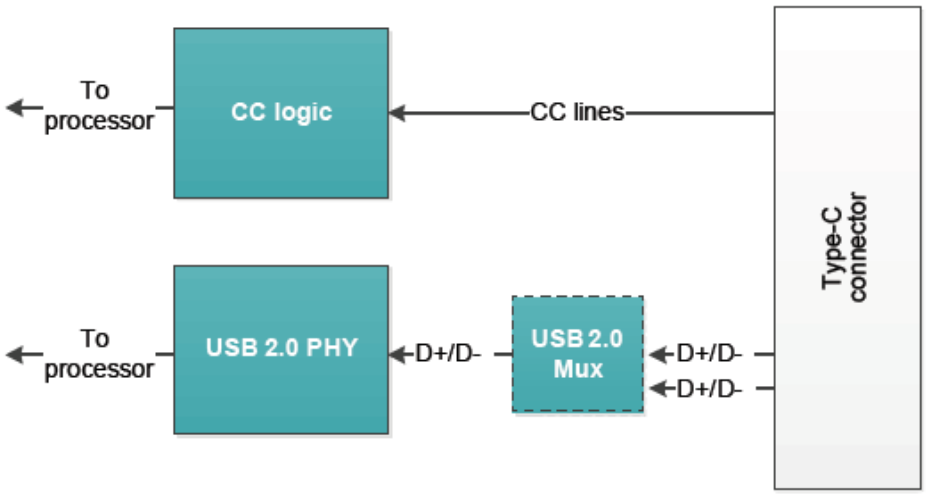


Figure 3. Type-C without PD manager [13]

In Figure 4 the pull-up/pull-down CC model is being presented which is responsible to recognize if a device has been connected, as well as the orientation of the cable. When a device is connecting, one of the CC lines (CC1 or CC2) is pulled down. A DFP by default, has the CC lines pulled-up through resistors R_p, and a UFP has the CC lines pulled down through resistors R_d. Once a connection is established, the DFP is “sensing” the pull-down of the CC line. Depending on which CC line is pulled down, the orientation of the cable is becoming known to the controller.

The values of R_p determine the desired current capability. A UFP device would have a fix R_d value thus, when connecting to the CC line a voltage divider will be formed which will provide information to the controller about the desired current capability.

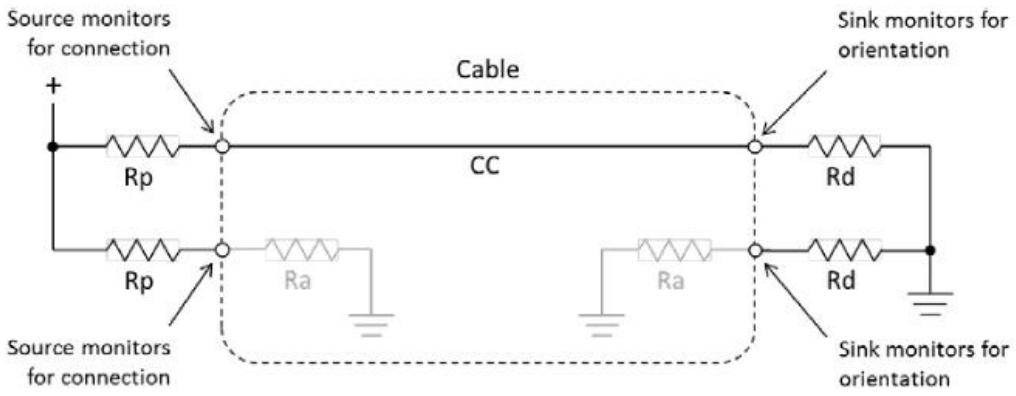


Figure 4. Pull-Up/Pull-down CC model [7]

USB Type-C Power Delivery

Electronic devices use the USB interface not only to transfer data, but also to charge. The flexibility of bidirectional power flow of the type-C interface provides the ability to create a network where the interconnected devices can power each other depending on the power policy. The idea of the USB type-C interface becoming a “universal” solution which can support fully the power needs of all the connected devices, imposed the need for a power delivery manager (PD) [9].

According to the USB PD specification there are specific power rules that need to be followed when designing the PD manager [13]. Following Figure 5, which presents an example of PD profiles, the source must be able to cover all the previous profiles in the power pyramid. More specifically, if a power profile of 45Watts has been negotiated, the source should be able to supply all the previous profiles of 15V at 3A, 9V at 3A, 5V at 3A. This power rule was introduced to guarantee that high powered supplies could support lower-powered devices, for example, a USB type-C hub which would be able to deliver power to a phone, a laptop and a TV monitor that need different power profiles [11].

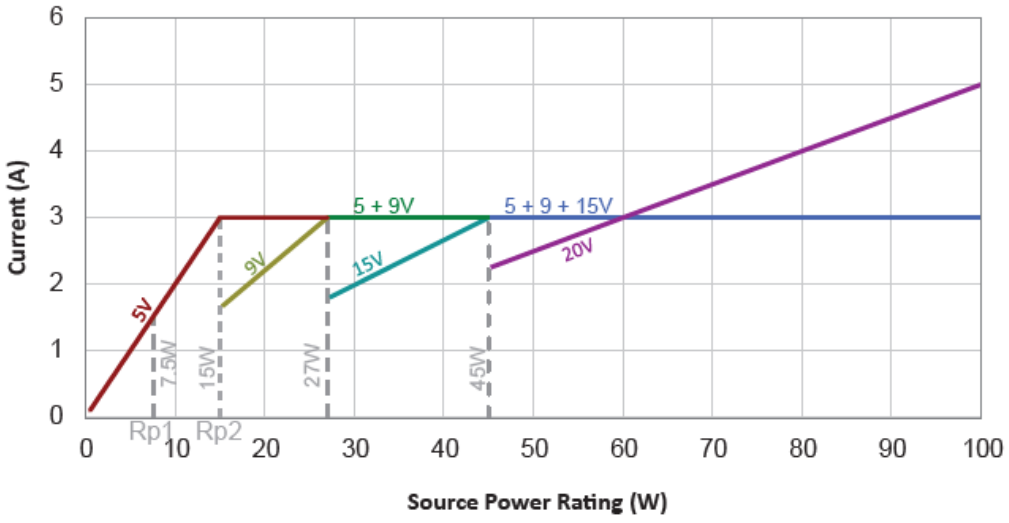


Figure 5.PD-profile graph [13]

Depending on the application form, the PD manager can be bypassed and thus the type -C interface can operate as a normal USB 2.0, with a type-A or type B connector. Applications can be grouped into two different cases where a PD manager is or is not necessary.

Power Profiles

Applications with increased complexity and high power demands, dictate the need for a power delivery manager (PD). As stated in the specifications of the USB type–C with PD manager, power levels up to 100Watts can be supported. The USB PD is organizing the power delivery in discrete power profiles as shown in Figure 6 (STMicroelectronics, 2017). The power profiles can be modified in voltage and current levels as long as they are not exceeding the physical power limitations of the type-C interface.

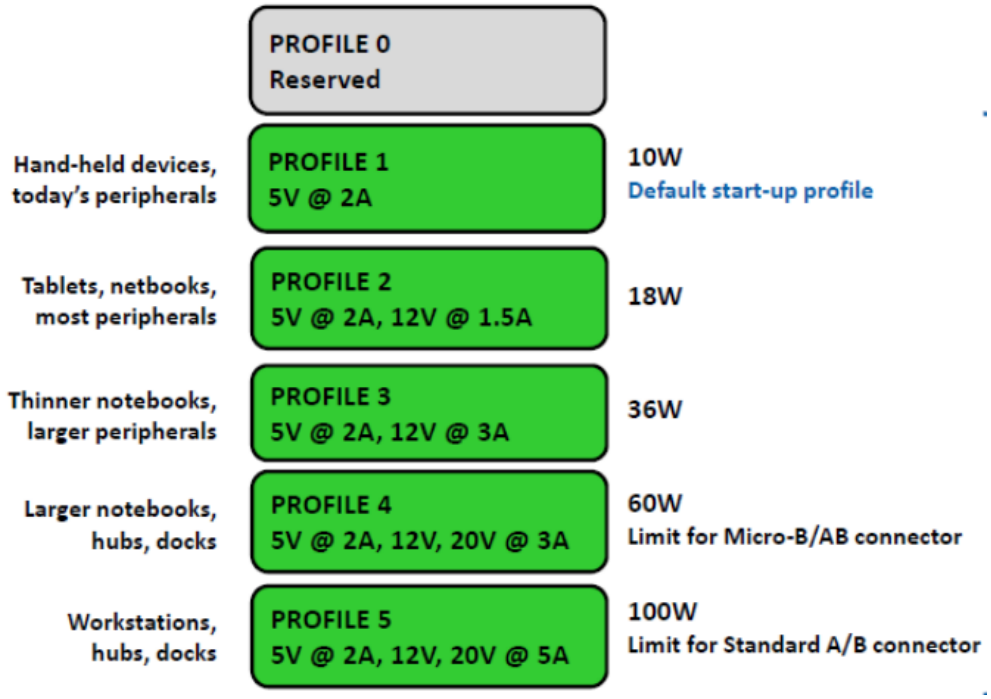


Figure 6. USB type-C power profiles [13]

Every application would need different power profiles depending on the specifications of the connected devices therefore, modifications in the USB PD manager are granted to the developer to offer flexibility. Though, it is always necessary to keep discrete voltage levels between the profiles. The current limitations are adjusting based on the power profile though, the current can be fluctuating but never exceeding the upper limit of the profile [9].

In Figure 7, an example of a USB type-C application with a PD manager is presented. In this example the use of the V_{BUS} node is realized. An optional V_{BUS} FET can be used in order to disconnect physically the V_{BUS} line from the port. In this case, a V_{BUS} discharge circuit is needed to discharge the node within 650ms according to the type-C specification when the sink is disconnected from the port [7]. The discharge circuit can also be implemented in the end-device. Due to the fact that the V_{BUS} node can have voltages up to 20V and the pin density is significantly high comparing to the previous USB connectors, a protection circuit is recommended to avoid shorting the 20V with the 5V pins of the connector (CC lines, SBU pins) [9].

The current protection block is optional and the purpose is to protect the end-devices from drawing excessive current. It is possible that the current protection block is implemented in the power conversion side. Moreover, the V_{CONN} switch is used only in the case of an active cable.

The active or e-marked cable is being introduced in the USB type-C interface and it is required to support USB 3.1 Super Speeds as well as current levels over 3A up to 5A. In addition, an active cable is supporting longer distances since re-driving and re-timing functions are being implemented in the IC circuit included in the cable [9].

In applications where a port should be acting as a DRP meaning that it could behave both as a source (DFP) or a sink (UFP) an R_P/R_D switch is necessary to swap the behavior of the port. When the switch is driving the R_P high then the port behaves as a DFP and when the switch is driving the R_D low then the port behaves as UFP.

For complex applications, which need a power management protocol, the two new blocks of PD manager and PD PHY are introduced. These two blocks use the CC lines to communicate between the host and the end-devices and offer information to the processor. The source is addressing the power levels that can support and the sink is addressing the needed power. When a power contract is accomplished, the voltage levels and current limitations are being adjusted by the processor. It is important to note that the two blocks are acting independently and under certain circumstances a system can operate only with one of the two blocks. The PD PHY is responsible to drive the CC lines but when it comes to power negotiation the PD manager is necessary. More specifically, the PD manager is responsible for addressing the different power profiles, negotiating power between the interconnected devices and controlling the PD PHY.

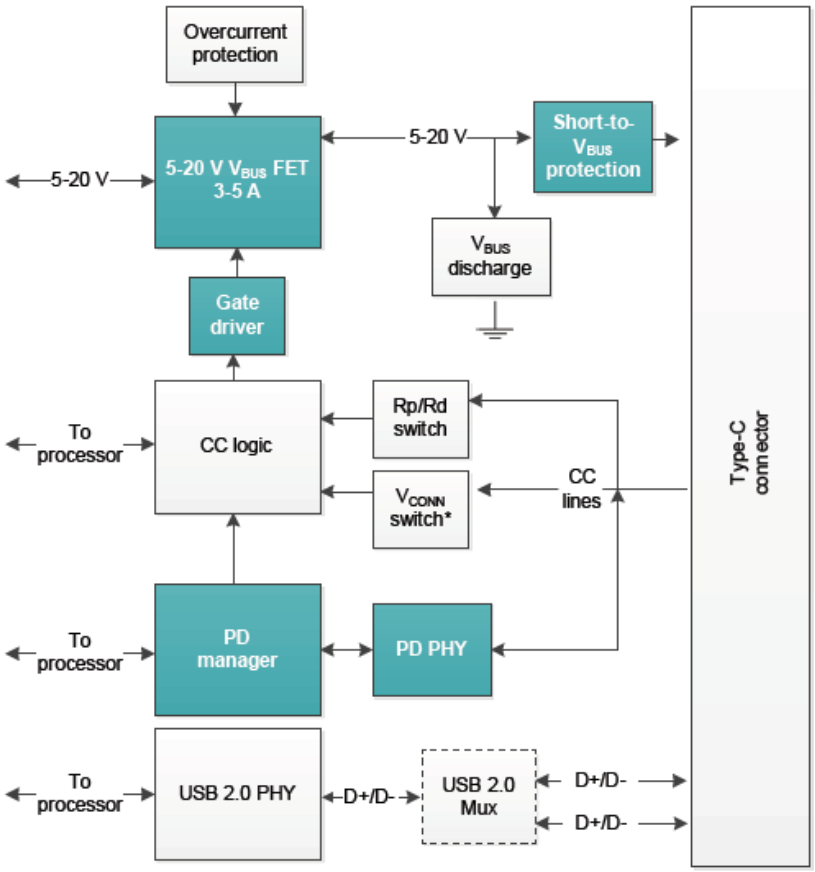


Figure 7. Type C with PD manager [13]

USB type-C System Architecture

Incorporating the USB type-C interface in complex systems and applications that require power negotiation between them, addresses the need for a standard power delivery policy. The policy manager is responsible to monitor the power needs of the interconnected devices and

based on a power plan, to optimize the power distribution. The architecture of such a system is being presented in Figure 8.

For clarification of the system architecture, the functional blocks are explained below in detail:

1. ***System Policy manager***: This functional block is not presented in Figure 8 since it is necessary only in complex power systems, where monitoring of various consumers and providers would be essential to manage the power distribution between them (power hubs operating as DRP).
2. ***Device Policy manager***: Every consumer or provider, when using USB type-C PD should have a device policy manager which enforces local policies by handling the power delivery across multiple ports, making decisions on how to obtain power and detecting the cable orientation. The device policy manager communicates directly, if one exists, with the system policy manager.
3. ***Policy Engine***: Every source or sink port should have a policy engine which directly communicates with the device policy manager and the protocol layer, and is responsible to handle the individual message sequence.
4. ***Protocol Layer***: The protocol layer is in charge of forming the messages that are sent between a pair of ports. It receives feedback from the policy engine, stating which messages need to be send and which are the responses to those messages.
5. ***Physical Layer***: The physical layer is responsible for sending and receiving messages from and to the V_{BUS} and the CC lines. It is also responsible for the data integrity, collision avoidance of the messages and error detection on all of the messages [11], [13].

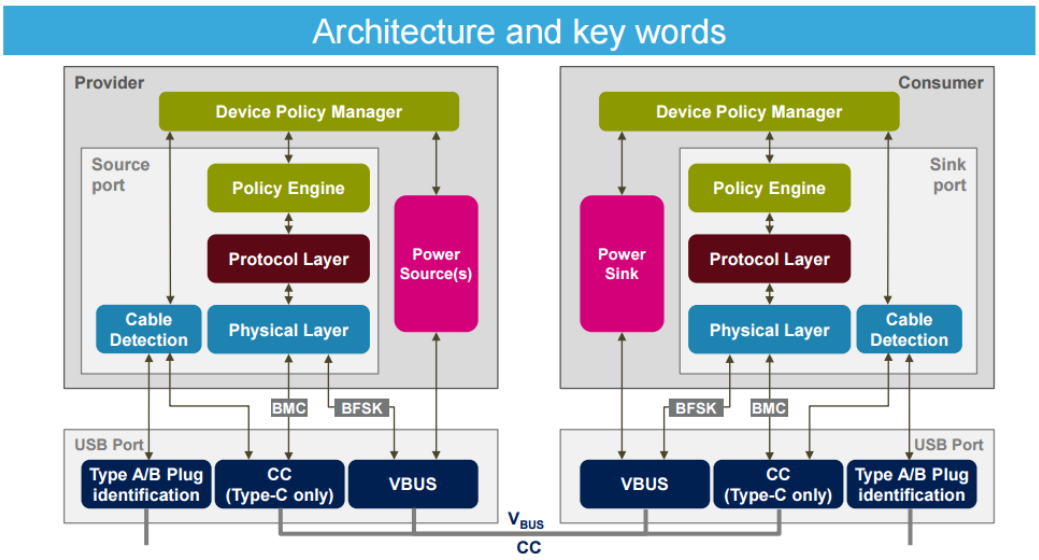


Figure 8. USB type-C system architecture [13]

Port Power roles

After presenting the architecture of the type-C system and the power roles that the devices can obtain when participating in a power delivery negotiation, it is beneficial to explain more in detail how it is decided by the PD manager to define the power role of every port. As already stated in the introduction of the chapter a device can get the role of a source, a sink or a dual role power. For every one of these states, the PD manager has predefined mandatory states and driving paths through which the PD algorithm is running. In order for the PD manager to determine the roles, monitoring the V_{BUS} node is critical. The detection of the V_{BUS} is used to define if a UFP or DFP port has been attached or detached [10]. In Figure 9 the block diagram of

a port acting as source (DFP) is being presented. Three possible states are available which are the Unattached.SRC, the AttachWait.SRC and the Attached.SRC. The arrows show exactly the paths that the algorithm is following in every state [11].

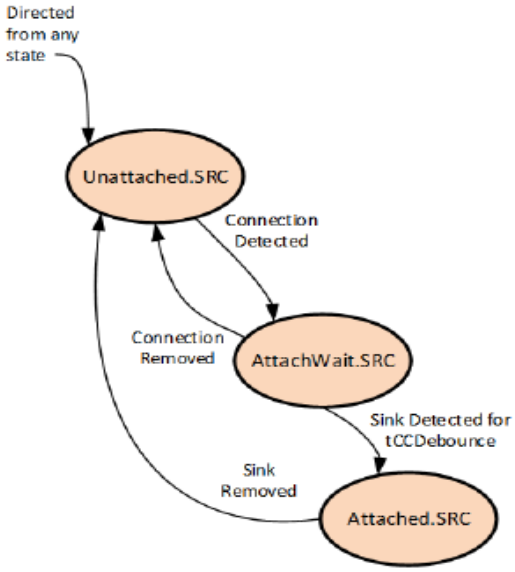


Figure 9.Source port role [11]

When a port is acting as a sink (UFP) the block diagram with all the states and the execution paths is being presented in Figure 10. Three possible states are available which are the Unattached.SNK, the AttachWait.SNK and the Attached.SNK [11].

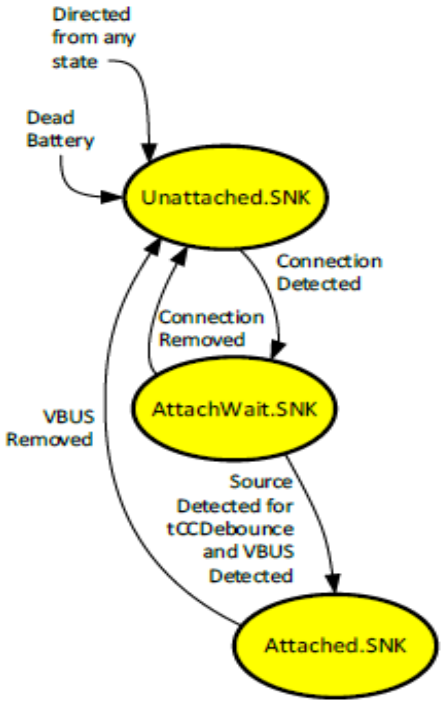


Figure 10.Sink port role [11]

The combination of these two cases are forming the execution tree of the dual role power port (DRP). The transition between the two phases, UFP and DFP, is guaranteed by the new execution paths that are introduced in the block diagram in Figure 11 [11]. As shown in the diagram, the PD manager is toggling the ports between the two states until the role of the port is resolved based on the role of the other attached port.

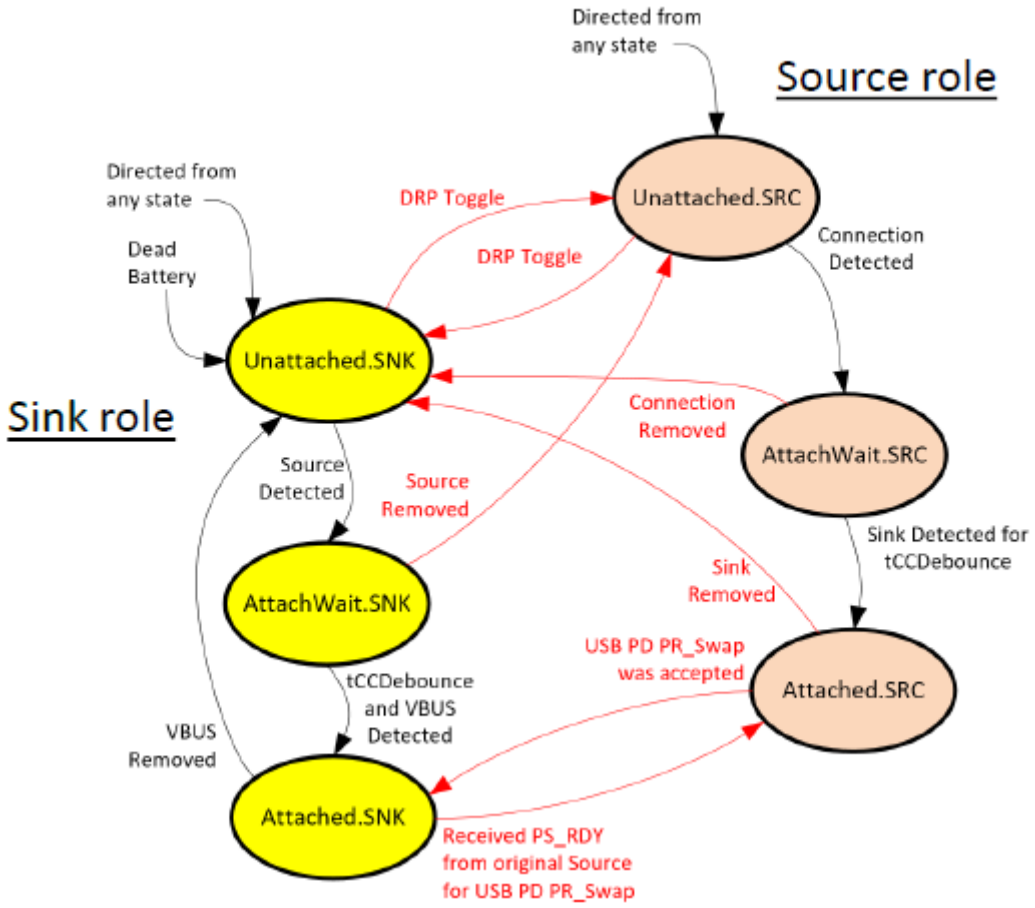


Figure 11.DRP port role [11]

DFP-UFP connections

Depending on the role of the port (DFP, UFP, DRP), specific steps are followed until a valid connection is established between the two ports. Following the USB type-C specification, all three cases are presented below [7].

DFP Functional Model

Initially the V_{BUS} FET is disabled thus the V_{BUS} node is not powered. Every DFP port is supplied with R_P pull-up resistors on the CC lines which are constantly monitored for the existence of a R_D pull-down resistor from a UFP. The monitoring of the pull-down resistor also provides information in case of a detach event of the cable. When a pull-down resistor is detected, which indicates a UFP connection, the V_{BUS} FET is enabled and the UFP can be powered. The DFP should be able to adjust the value of the R_P by enabling or disabling resistors in order to address different current carrying capabilities to the UFP. In Figure 12, the functional model of the DFP is being presented [7].

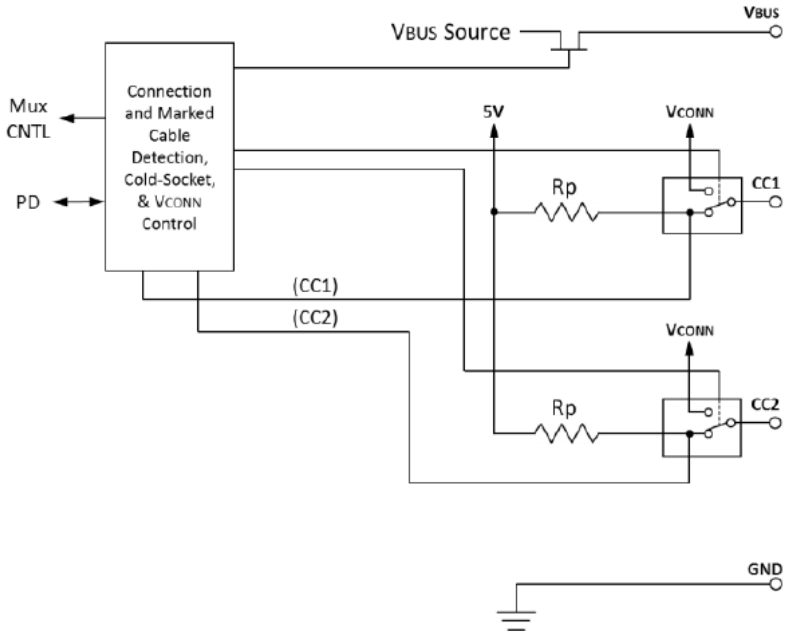


Figure 12. DFP functional model [7]

UFP Functional Model

A UFP port has both of the CC lines terminated to ground through pull-down resistors. A UFP is monitoring the VBUS net in order to locate the existence of a DFP attach. Furthermore, the CC lines are used by a UFP to track the changes of the pull-up resistor of the DFP, which would indicate different current capability. In Figure 12Figure 13 the functional model of the UFP is presented [7].

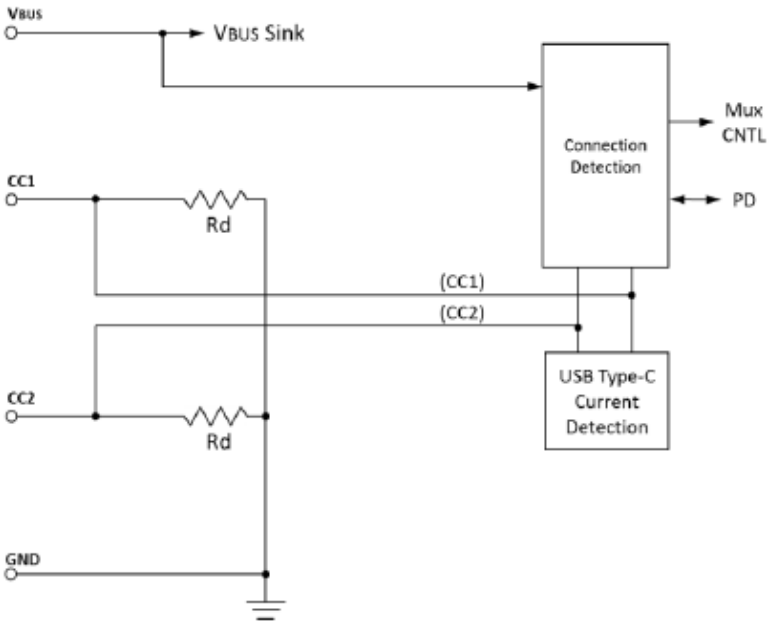


Figure 13. UFP functional model [7]

DRP Functional Model

The DRP port combines fundamentals from both the UFP and DFP operations as shown in Figure 14. The V_{BUS} FET is used to enable or disable the V_{BUS} net. When the port is acting as a DFP initially the $V_{BUS\ Source}$ FET is disabled. As soon as a UFP is detected, the $V_{BUS\ Source}$ FET is enabled and the swapping shown in Figure 15 is ceasing.

If the port is acting as a UFP, the $V_{BUS\ SINK}$ FET is initially disabled. The external connection from V_{BUS} to the controller as shown in Figure 14, is used to determine the attachment of a DFP. As soon as a DFP is detected by the pull-up of the CC line, the $V_{BUS\ SINK}$ FET is enabled and allows power to be transferred. When the port role has been resolved, the swapping shown in Figure 15 is ceasing. The DRP needs an R_P/R_D switch to swap the port behavior.

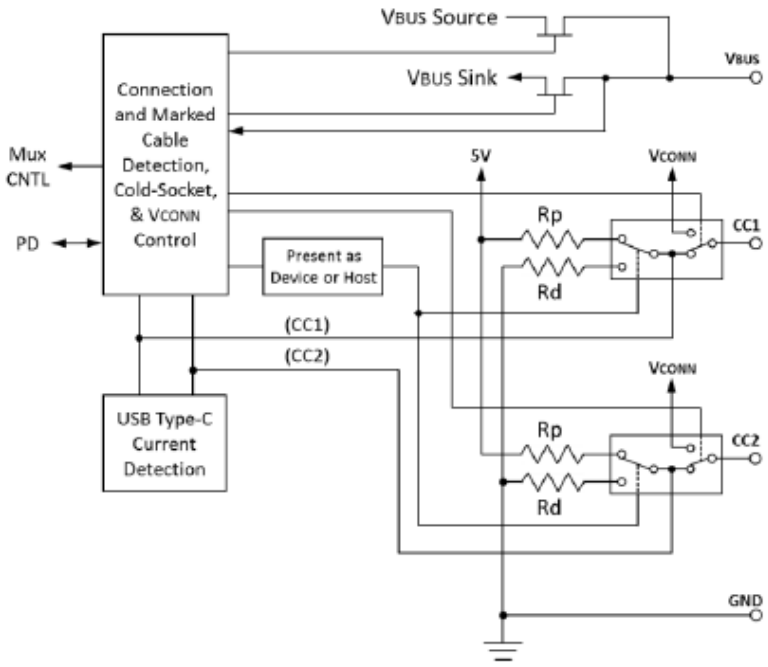


Figure 14. DRP functional model [7]

Until the role of the port has been established the DRP is toggling between a DFP and a UFP. Figure 15 shows the transition timing of a DRP. The time, tDRP, represents the period of the event. Within this period the port acts as either a DFP or a UFP. It is critical that the clock, which is used to control the swap, is not reoccurring the event with exact timing but within a range of time, in order to minimize the possibility of failing to resolve a DFP-UFP connection.

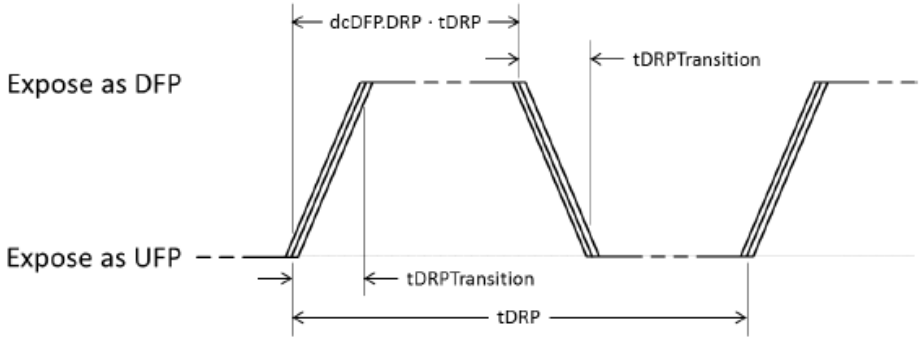


Figure 15. DRP transition timing [7]

DC-DC CONVERTER

The objective of power electronic systems is the processing and control of electrical energy. This can be accomplished by proper formation of the voltage and current levels that can be used by a load [14]. Since the establishment of the electrical power grids in the beginning of the 19th century, the necessity for power conversion was essential to cover the needs of different loads. The research undertaken on power electronic systems in combination with the evolution of semiconductor materials, formatted the power conversion systems in four classes; AC/DC rectifiers, DC /AC inverters, DC/DC converters and AC/AC transformer. Every power electronic converter performs different functions thus, they are supporting various applications such as switching mode power supplies, electrical machine motors, energy storage systems, power generation and distribution or renewable energy conversion.

In recent years, the participation of renewable sources in the electrical energy production is noticeable. A tension of incorporating DC grids in the main electrical grids has increasing popularity, since studies show that the DC grids present several benefits. As a result, DC/DC converters have started playing a very important role in the realization of DC grids. A DC/DC converter is an electronic device which is necessary when there is a need for changing the voltage level. Unlike the AC power, DC power cannot be stepped up or down through the use of a transformer. Thus, the comparable device to a transformer for DC power is the DC-DC converter [15].

When it comes to grids that are supported by renewable energy sources, an energy storage system is crucial. Some of the most important reasons for a battery energy storage system (BES) are discussed. Firstly, with the existence of a BES the grid can react appropriately during the low and high demand periods. That means that the system is able to store the available excess energy for later use, depending on the power demands of the consumers. Moreover, a BES can provide protection against disastrous overload situations by managing the grid assets [16]. Thus, it is plausible that the reliability of a DC grid can be increased significantly by a back-up battery system.

The implementation of a DC grid which can collaborate with a BES, in order to optimize the management of the produced and consumed energy, dictates the need for a DC-DC bidirectional converter. In this way, the power flow in both directions (source-sink swap) becomes feasible, therefore the BES system can charge or discharge to support the DC grid [17]. As a result, the DC-DC converters become the key element of an energy efficient management.

As stated in the introduction of this thesis, the main focus remains in the power management of a DC Nano-grid of a smart building. Within the scope of this research is the building of a buck-boost DC-DC bidirectional converter which could exploit the high potential of Li-ion batteries of end-devices such as smartphones, tablets or laptops in case of a grid failure. An example of such an application is given in Figure 16.

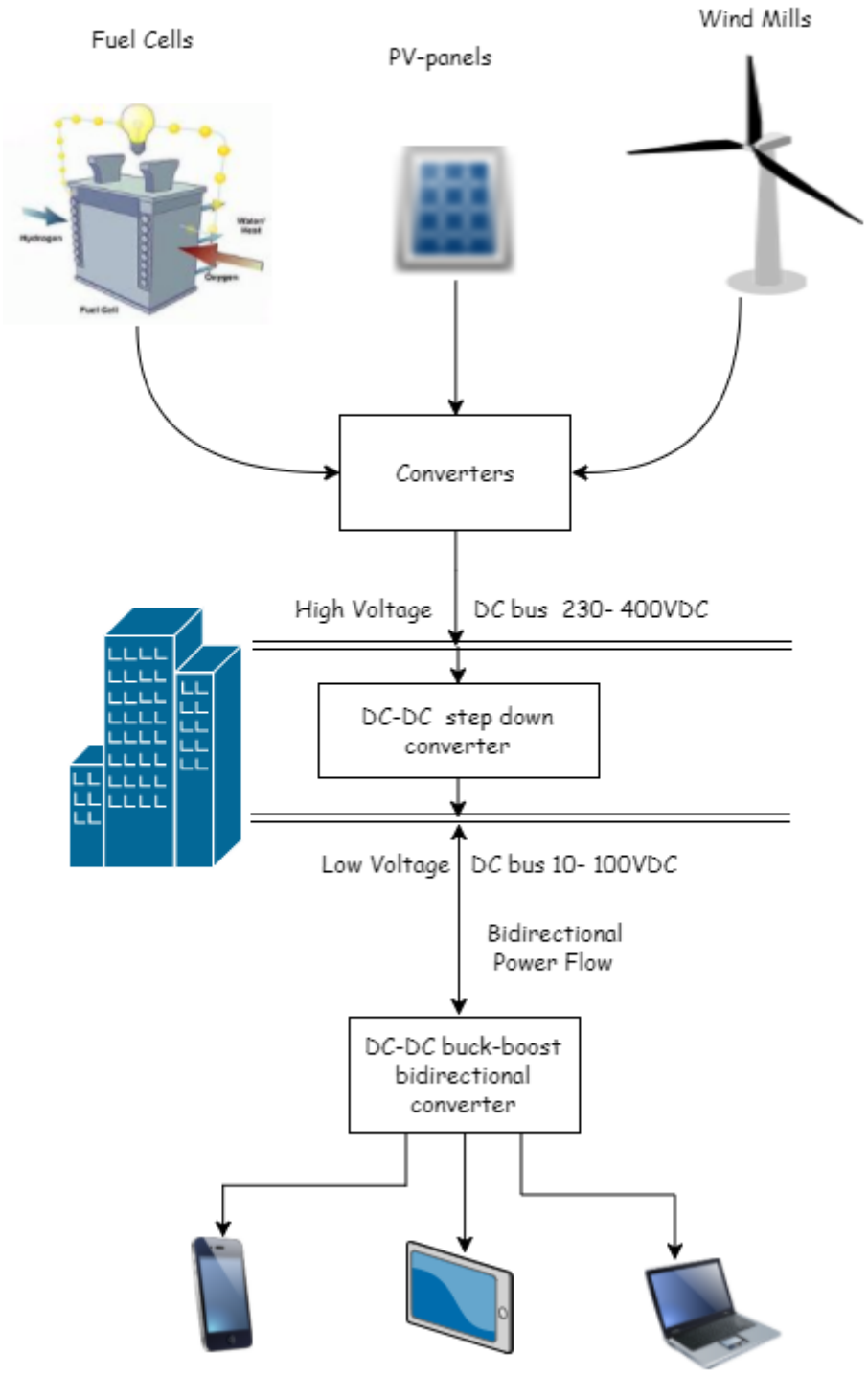


Figure 16. Application of a DC-DC bidirectional converter with USB type-C for commercial smart buildings

The purpose of this DC-DC bidirectional converter is to be able to provide power to the connected end-devices under specific voltage and current levels. In the unlikely event of grid failure, the DC-DC converter should be able to discharge the end-devices and provide energy back to the main DC bus at a specific voltage level. Those were the initial requirements that defined the need for buck-boost DC-DC converter that can step-up, generate an output voltage higher that the input source voltage or step-down, generating an output voltage lower that the input source voltage. The necessity for role swapping of the source which, in principle, is the main DC bus (grid), and the sink which, in principle, are the end-devices, dictated the need for the bidirectional character of the buck-boost converter.

Converter Topology

Seeking for the most suitable topology of the DC-DC converter that could cover the needs of the application under research, the topology which is proposed by Albert Andreas Maria Esser [18] ,was chosen as a fitting solution. The topology is shown in the next Figure 17

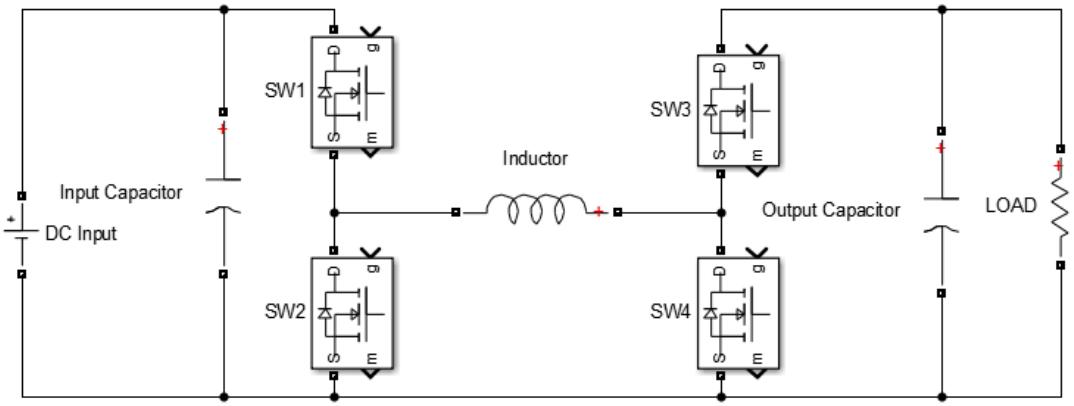


Figure 17. Buck-Boost Bi-directional Converter [18]

This topology is known as a synchronous buck-boost converter since the four MOSFETs are switching in pairs complementary to each other. This non-inverting buck–boost topology guarantees a higher or lower voltage level on the output (load side) than that of the DC input, while maintaining the voltage polarity of the output same as that of the input. Fours high speed MOSFETs (SW1-SW4) are used to control the power flow direction, as well as the mode operation (buck or boost).

This topology is considered a non-isolated DC-DC converter. The reason that a non-isolated converter is used mainly because the isolation of the system from the grid is guaranteed from a previous stage of the system. Furthermore, the low power nature of the research application is limiting the safety liabilities. The lack of an isolation transformer is decreasing the conduction and transformer losses thus, providing a high efficiency solution. Moreover, the need for less components minimizes the implementation cost.

The analysis of the power flow will follow in the next chapter where the controlling of the system will be explained in detail. In this chapter the analysis of the operation modes (buck/boost) will be made.

Buck Mode Operation

When the output voltage on the load needs to be lower than the input voltage of the DC input then the DC-DC converter needs to operate as a step-down or buck converter. The simplified figure of a DC-DC buck converter is given in Figure 18. The analysis of the dc-dc buck converter will be performed assuming CCM (continuous conduction mode operation) during steady state.

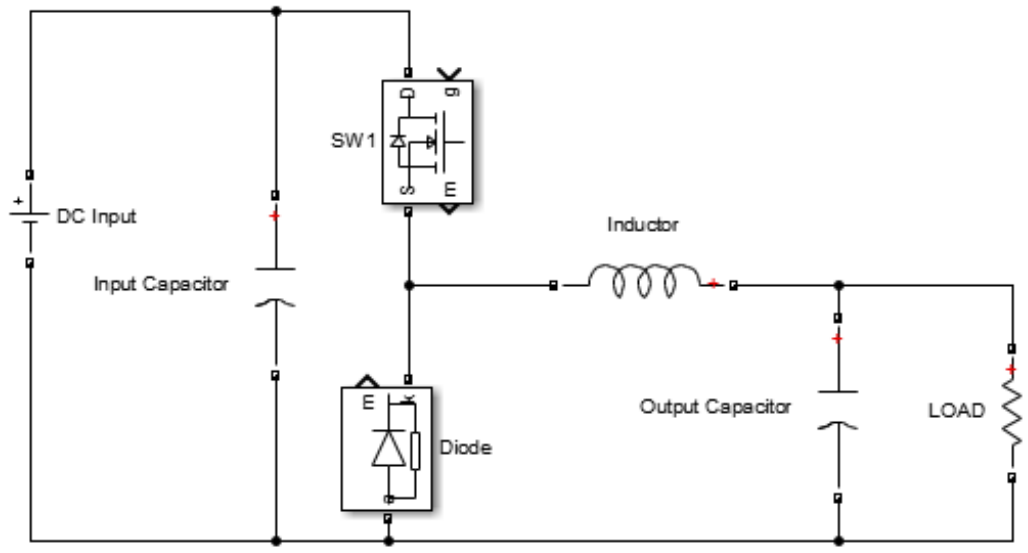


Figure 18. DC-DC Buck Converter topology Simulink

The controlling of the output voltage of the buck converter is done by controlling the duty cycle of the MOSFET SW1. The switching operation of SW1 is generating a rectangular waveform $V_s(t)$ of the DC input that is applied on the circuit. When the switch is conducting then $V_s(\mathrm{t}) = V_{\mathrm{in}}$. When the switch is not conducting then $V_s(t) = 0$. The average value of $V_s(t)$ defines the output voltage of the buck converter. The frequency at which the switch is changing state is defined as switching frequency f_s. The reverse of the frequency is the period $T_s = \frac{1}{f_s}$. In every period, there is a time that the switch is conducting and is defined as T_{ON} and a time that the switch is not conducting T_{OFF}. The sum of those two times is equal to $T_{s=} T_{\mathrm{ON}} + T_{\mathrm{OFF}}$. The ratio of the time that the switch is conducting to the total period time is defined as the duty cycle and is given as $D = \frac{T_{\mathrm{ON}}}{T_s}$. The time that the switch is not conducting is complementary to the duty cycle thus, is given as $1 - D = \frac{T_{\mathrm{OFF}}}{T_{\mathrm{s}}} = D'$. From Fourier analysis, Equation 1 shows how the average value of $< V_s(t) >$ can be calculated [19].

$$(1) \quad < V_{\mathrm{s}}(t) >= \frac{1}{T_{\mathrm{s}}} \int_0^{T_s} V_{\mathrm{s}}(t)dt = \frac{1}{T_{\mathrm{s}}} (DT_{\mathrm{s}}V_{\mathrm{in}}) = DV_{\mathrm{in}}$$

$$< V_{\mathrm{s}}(t) >= V_{\mathrm{out}} = DV_{\mathrm{in}}$$

$$D_{\mathrm{Buck}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}$$

Due to the fact that in the real world there are no ideal components, and since ohm as well as switching and conducting losses are introduced in the system, a more realistic calculation of the duty cycle for a buck converter is given in Equation 2 .

$$(2)\ D_{\mathrm{Buck}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \cdot \frac{1}{n}$$

where n is the efficiency of the buck converter.

The introduction of the low pass filter on the output of the buck converter, which is composed of the inductor and the filter capacitor, allows the pass of the DC component and

rejects the harmonics produced during switching of the MOSFET. Thus, the filter is responsible to maintain a significantly constant dc voltage on the output of the buck converter [19].

Analyzing further the role of the inductor, when the switch SW1 is conducting, the left side of the inductor is connected to the DC input supply (V_{in}) and current starts flowing through the inductor slowly at the beginning and gradually building up, since the inductor nature is to oppose sudden changes of the current levels. Equation 3 gives the inductor voltage when SW1 is conducting [19].

$$V_L = V_{\text{in}} - V_{\text{out}} \quad (3)$$

In reality V_{out} is never a perfect DC voltage since there is always a voltage ripple (V_{ripple}) but in a well-designed converter the ripple is negligible thus, it can be excluded in the calculations. When SW1 is not conducting, the diode is becoming forward-biased and the current is flowing through the diode. The voltage of the inductor during this period is derived by Equation 4 (4) V_L(3since the DC input is not connected anymore and the term $V_{\text{in}} = 0$ [19].

$$(4)\ V_L = -V_{\text{out}}$$

The change of the voltage on the inductor is shown in Figure 19 where $V_{\text{g}} = V_{\text{in}}$ and $V = V_{\text{out}}$.

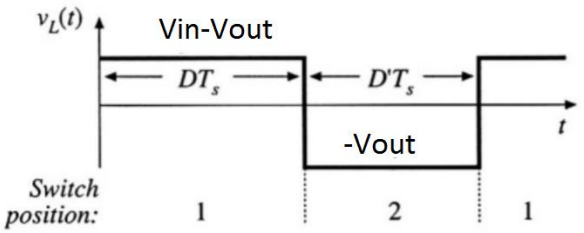


Figure 19. Inductor voltage of buck converter over period Ts [19]

Knowing the inductor voltage in each subinterval, gives us the possibility to investigate what is happening with the inductor current in each case. When the switch SW1 is conducting, the slope of the inductor current can be calculated using Equation 5.

$$V_L(t) = L\frac{di_L(t)}{dt},$$

$$\frac{di_L(t)}{dt} = \frac{V_L(t)}{L} \cong \frac{V_{\text{in}} - V_{\text{out}}}{L} \quad (5)$$

When the switch SW1 is not conducting, the slope of the inductor current can be calculated using Equation 6.

$$\frac{di_L(t)}{dt} \cong -\frac{V_{\text{out}}}{L} \quad (6)$$

In Figure 20, the voltage and current slopes of the inductor are visible during both subintervals.

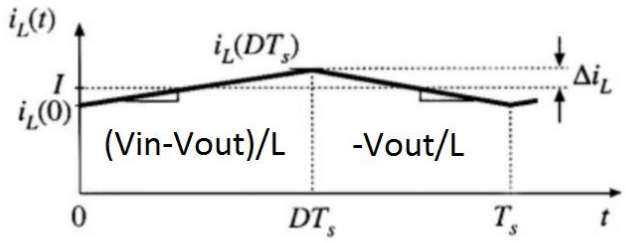


Figure 20. Inductor current of buck converter over period Ts [19]

During a steady state operation, the net energy change of the output capacitor over a period T_S should be zero. The change of the capacitor current over time is given by Equation 7

$$(7) \quad i_c(t) = C\frac{dV_c(t)}{dt}$$

The change during a hole period T_S is given by Equation 8.

$$(8) \; V_c(T_s) - V_c(0) = \frac{1}{C}\int_0^{T_s} I_c(t)dt = 0$$

Boost Mode Operation

When the output voltage on the load needs to be higher than the input voltage of the DC input then the DC-DC converter needs to operate as a step-up or boost converter. The simplified figure of a DC-DC boost converter is given in Figure 21. The analysis of the dc-dc boost converter will be performed assuming CCM (continuous conduction mode operation) during steady state.

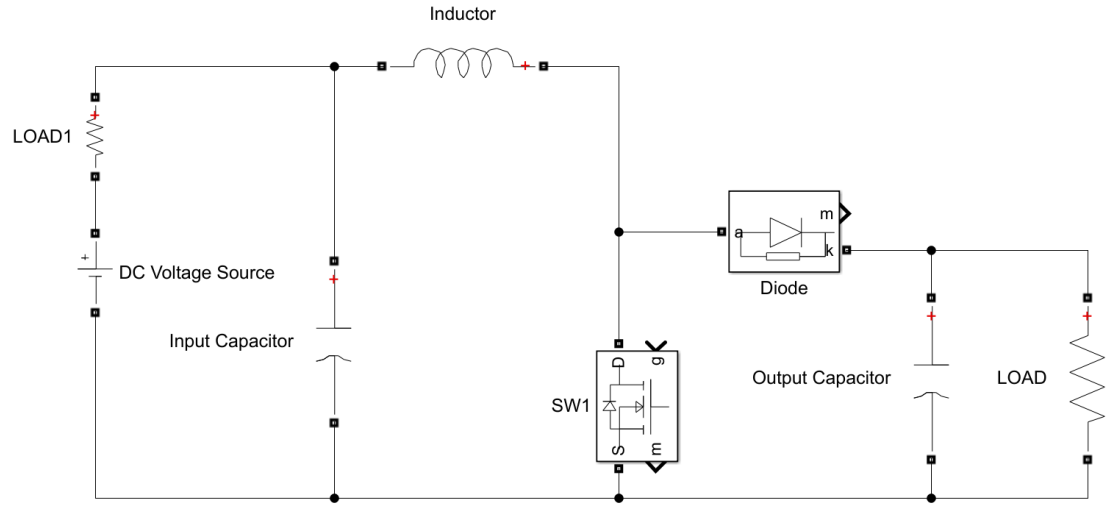


Figure 21. DC-DC Boost Converter topology Simulink

In the boost converter, the controlled switch SW1 is placed after the inductor. This allows to exploit the inductor properties to generate a voltage at the output that has a greater magnitude than that of the input. The inductor and capacitor current and voltage analysis in every subinterval is completed [19].

When switch SW1 is conducting, the voltage on the inductor is defined by Equation 9.

$$(9)\ V_L = V_{\text{in}}\ ,$$

and the current on the filter capacitor is defined by Equation 10.$(10)\quad i_C = -\frac{V_{\text{out}}}{R_{\text{LOAD}}}\ ,$

$$(10)\quad i_C = -\frac{V_{\text{out}}}{R_{\text{LOAD}}}\ ,$$

When the switch SW1 is not conducting, the diode is forward biased and the voltage on the inductor is defined by Equation 11.

$$(11)\ V_L = V_{\text{in}} - V_{\text{out}} \quad \text{considering}\, V_{\text{out}} \cong \text{const},$$

and the current on the filter capacitor is defined by Equation 12.

$$i_C = i_L - \frac{V_{\text{out}}}{R_{\text{LOAD}}}\ , \text{considering}\ that\ i_L = I_{\text{in}}$$

$$(12)\ i_C = I_{\text{in}} - \frac{V_{\text{out}}}{R_{\text{LOAD}}},$$

The voltage change on the inductor in each subinterval is shown in Figure 22 where $V_{\text{g}} = V_{\text{in}}$ and $V = V_{\text{out}}$. The graph of the current change on the capacitor is shown in Figure 23 where $R = R_{\text{LOAD}}$, $V = V_{\text{out}}$ and $I = i_L = I_{\text{in}}$.

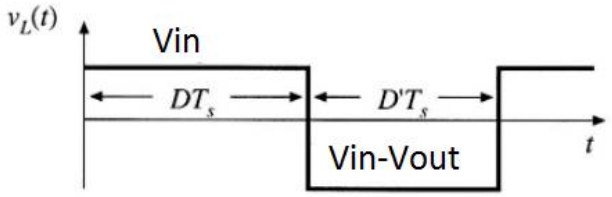


Figure 22. Inductor voltage of boost converter [19]

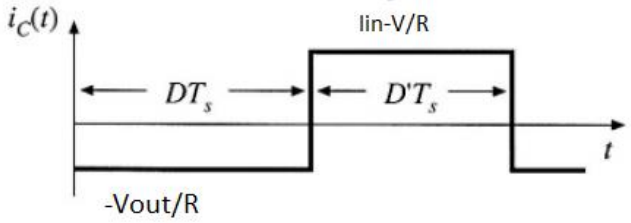


Figure 23.Capacitor current boost converter [19]

Since the voltage change over the inductor is known, the inductor current change over a period can be investigated next. During the time that the switch SW1 is conducting, the slope of the inductor current can be calculated from Equation 13

$$(13)\quad \frac{di_L(t)}{dt} = \frac{V_{L\,(t)}}{L} = \frac{V_{\text{in}}}{L}$$

When the switch SW1 is not conducting, the slope of the inductor current can be calculated from Equation 14

$$(14)\quad \frac{di_L(t)}{dt} = \frac{V_{L\,(t)}}{L} = \frac{V_{\text{in}} - V_{\text{out}}}{L}$$

The waveform of the change of the inductor current over a period is presented in Figure 24.

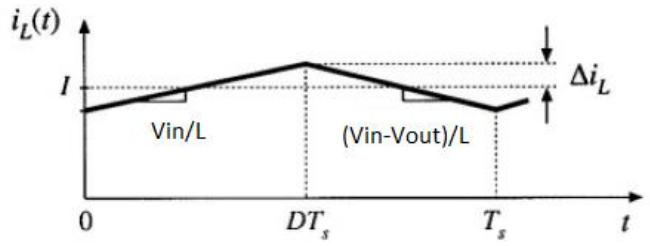


Figure 24. Inductor current boost converter [19]

Equation 15 analyses the voltage on the inductor over a period T_s.

$$(15)\int_0^{T_s} V_L(t)dt = V_{\text{in}}DT_s + (V_{\text{in}} - V_{\text{out}})D'^{T_s} \quad ,$$

Since $D + D' = 1$ and the net voltage change of the inductor over a period is zero

$$V_{\text{in}}(D+D')T_s - V_{\text{out}}D'T_s = 0 \rightarrow$$
$$V_{\text{in}}(D+D')T_s = V_{\text{out}}D'T_s \rightarrow$$
$$V_{\text{in}} = V_{\text{out}}D' \rightarrow$$
$$D_{\text{Boost}} = 1 - \frac{V_{\text{in}}}{V_{\text{out}}}$$

Same as for the buck converter, a more realistic approach of the duty cycle of the boost converter is presented in Equation 16.

$$(16)\quad D_{\text{Boost}} \rightarrow (1 - \frac{V_{\text{in}}}{V_{\text{out}}}) \cdot \frac{1}{n}$$

where n is the efficiency of the boost converter.

Equation 16 shows that for duty cycles that approach 100%, V_{out} tends to become infinite. While the duty cycle approaches values close to 100%, the inductor current becomes very large, and the non-ideal components present very high power losses. Thus, a significant reduction in the efficiency of the converter is noticed [19].

Buck-Boost Operation

A problem caused by physical limitations of the hardware is the situation when the input and the output voltage should be almost similar. In an ideal converter, that could operate with duty cycles close to 0% or 100%, this case would not be an issue. As previously mentioned, the boost converter has an upper duty cycle limitation, dictated by the physical limitations of the components. Moreover, limitations are introduced by the minimum T_{ON} times that can be controlled on the MOSFET switches. Another limitation on the duty cycle values is introduced by the necessity of a dead-time period, which is needed to charge the high side of the switching MOSFET.

All the above restrains make the regulation challenging when the input voltage approaches the output voltage. In this case, a buck-boost operation is implemented. The figure of a DC-DC buck-boost converter is given in Figure 25. The analysis of the DC-DC buck-boost converter will be performed assuming CCM (continuous conduction mode operation) during steady state.

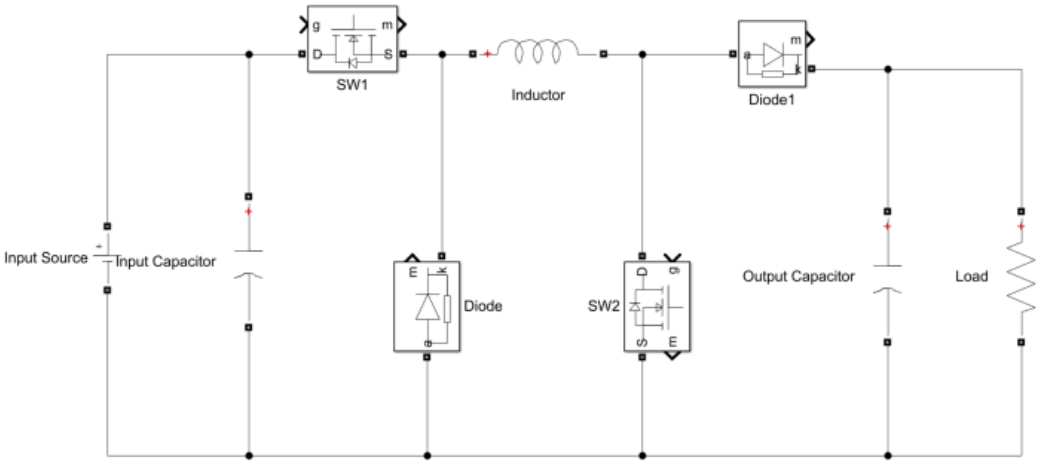


Figure 25. DC-DC Buck-Boost Converter topology Simulink

In the buck-boost converter, the controlled switches SW1 and SW2 are acting as a pair. When SW1 and SW2 are conducting, the voltage on the inductor is defined by Equation 17.

$$(17)\ V_L = V_{\text{in}}$$

When the switches SW1 and SW2 are not conducting, the voltage on the inductor is defined by Equation 18.

$$(18)\quad V_L = -V_{\text{out}}$$

The graph of the inductor voltage over a period T_s is presented in Figure 26.

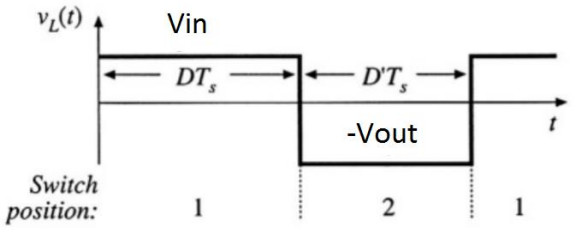


Figure 26. Inductor voltage buck-boost converter [19]

Since the voltage change over the inductor is known, the inductor current change over a period can be calculated. During the time that the switches SW1 and SW2 are conducting the slope of the inductor, current can is defined by Equation 19.

$$(19)\quad \frac{di_L(t)}{dt} = \frac{V_{L\,(t)}}{L} = \frac{V_{\text{in}}}{L}$$

When the switches SW1 and SW2 are not conducting, the slope of the inductor current can be calculated from Equation 20.

$$(20)\quad \frac{di_L(t)}{dt} = \frac{V_{L\,(t)}}{L} = \frac{-V_{\text{out}}}{L}$$

The waveform of the change of the inductor current over a period is presented in Figure 27.

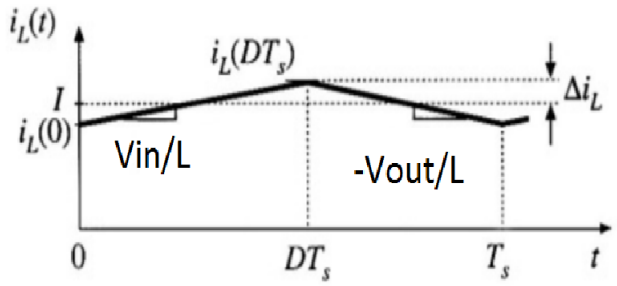


Figure 27. Inductor current buck-boost converter [19]

Equation 21 analyses the voltage on the inductor over a period T_s.

$$(21)\int_0^{T_s} V_L(t)dt = V_{\text{in}}DT_s - V_{\text{out}}D'^{T_s} \quad ,$$

Since $D + D' = 1$ and the net voltage change of the inductor over a period is zero

$$V_{\text{in}}DT_s - V_{\text{out}}D'T_s = 0 \rightarrow$$
$$V_{\text{in}}DT_s = V_{\text{out}}D'T_s \rightarrow$$
$$V_{\text{in}}D - V\text{out} + V\text{out}D = 0 \rightarrow$$
$$D_{\text{Buck-Boost}} = \frac{V_{\text{out}}}{V_{\text{in}} + V_{\text{out}}} \cdot \frac{1}{n}$$

where n is the efficiency of the boost converter.

Converter Calculations

As presented in the introduction, within the scope of this thesis is the design and build of a DC-DC bidirectional converter which is intended to be used as an interface between the DC link of a building and the end devices equipped with a battery. The DC link is assumed to have an input voltage range of 10-100V. The end devices are assumed to be using a USB type C port as a power and communication interface. The voltages that the devices can accept are ranging between 5-20V. Based on the idea of building a flexible hardware which can be used for different applications or higher power profiles which USB type-C might be supporting soon, the design of the converter is for a maximum output power of 300W with an output voltage between 5-100V and an output current between 0-8A.

After defining the topology of the converter, it is essential to calculate the main components such as the inductor of the system, the filter capacitors and the switching MOSFET's. Selecting appropriate components will ensure the build of a stable converter for the research application. A wide input voltage range is selected between $10V \leq V_{\text{in}} \leq 100V$. The input current is selected to be between $0A \leq I_{\text{in}} \leq 8A$. The output voltage is ranging between $5V \leq V_{\text{out}} \leq 100V$ and the output current $0A \leq I_{\text{out}} \leq 8A$.

The values of the components should cover all the operation modes (buck, boost and buck-boost). The switching frequency is selected to be f_s=250Khz. The benefits of a high frequency are multiple. High frequency allows the use of smaller components thus, the total size of the application can be decreased significantly. Furthermore, the transient response of the system is

improving when the switching frequency is higher. The main disadvantage occurring with high switching frequency, is the increased switching losses which could be minimized with zero voltage or zero current switching control [20].

Inductor Selection

In order to calculate the inductor value first, the ripple of the inductor current Δ_{iL} has to be defined. The typical values for the current ripple lie between 10% to 30% of the maximum DC current of the highest load. The ripple current must be maintained low in order to avoid high peak currents, which would dictate the use of bigger and more expensive components. For the research application, a current ripple of $\Delta_{iL} = 20\%$ is selected. Every operation mode needs to be analyzed separately [19]. For buck operation, the inductor value is calculated using Equation 22

$$(22)\ L_{\text{buck}} = \frac{V_{\text{inmax}} - V_{\text{out}}}{2\Delta_{iL}}\ DT_s,$$

Where V_{inmax} is the maximum input voltage of the system, V_{out} is the output voltage of the system, D is the duty cycle, T_s is the witching period and Δ_{iL} is the current ripple of the inductor. For the given maximum input voltage V_{inmax}=100V and considering all the other variables are constant apart from V_{out}, Equation 22 can be reformed.

$$L_{(\text{VOUT})} = V_{\text{inmax}} - V_{\text{out}} \cdot \frac{V_{\text{out}}}{V_{\text{in}}} \rightarrow$$

Which is an equation of the form

$$f_{(x)} = x - \frac{x^2}{a}$$

and presents maximum at

$$f_{(\text{xmax})} = \frac{a}{2} = \frac{100}{2} = 50V$$

Thus the maximum inductor value needed would occur when $V_{\text{out}} = 50$ and the duty cycle is $D = 0.5$. Solving Equation 22 with those values gives a result of $L_{\text{buck}} \approx 31.25\mu H$.

For boost operation, the inductor value is calculated using Equation 23

$$(23)\ L_{\text{boost}} = \frac{V_{\text{inmin}}}{2\Delta_{iL}}\ DT_s,$$

In the case of the boost converter, the calculation of the maximum inductor is dictated by the maximum V_{out} which in the research application is limited at 100V. Thus, the maximum inductance is occurring when $D = 0.5$. The maximum input voltage that this duty cycle can be achieved is $V_{\text{in}} = 50\text{V}$. Solving Equation $(23$, based on those values, gives a result of $L_{\text{boost}} \approx 31.25\mu H$. Based on those results and the available market solutions, an inductor of $\boldsymbol{L = 38.8\mu H}$ was chosen.

Capacitor Selection

The output filer capacitor selection is critical in order to ensure a stable output voltage. The normally required voltage ripple which would comply also with the USB type C specifications should be around 1% [21] of the desired output voltage V_{out}. In a buck converter, the formula which provides the minimum capacitance required is given by Equation 24.

$$(24)\ C\text{out}_{\text{buck}-\text{min}} = \frac{\Delta_{iL}}{8\, f_s V_{\text{ripple(pp)}}}$$

Where $V_{\text{ripple}}$is the desirable output ripple, f_s is the switching frequency of the MOSFETs and Δ_{iL} is the ripple current on the inductor. Solving Equation 24 for $V_{\text{ripplemax(pp)}} = 1V$, $f_s = 250Khz$ and $\Delta_{iL} = 1.6A$ gives a result of $C\text{out}_{\text{min}} = 0.8\mu F$

As a boost converter, the formula that provides the minimum capacitance is given in Equation 25.

$$(25) \qquad C\text{out}_{\text{boost-min}} = \frac{I_{\text{outmax}}\, D}{f_s V\text{out}_{\text{ripple}}}$$

Since the application converter presents some limitations on maximum power rating $P_{\text{max}} = 300W$ and maximum output voltage $V\text{out}_{\text{max}} = 100V$, the solution of the Equation 25 must be achieved based on specific assumptions. In the calculations, the USB type-C specifications [21] need to be considered for the maximum voltage ripple and maximum output current. Thus, for $V_{\text{ripple(pp)}} \approx 1V$, $f_s = 250Khz$ and $I_{\text{outmax}} \approx 5A$ which can be achieved for a maximum duty cycle of $D \approx 0.5$ due to minimum $V\text{in}_{\text{min}} = 10V$, the solution of Equation 25 gives an approximate result of $\boldsymbol{C\text{out}_{\text{min}} \approx 10\mu F}$**.** In order to guarantee a substantially low output ripple even for higher output voltages up to $V\text{out}_{\text{max}} = 100V$, the capacitor value is chosen to be $\boldsymbol{C = 15.6\mu F}$. Since the converter is bidirectional and the output can swap to an input and vice versa, the same filter capacitor will be used in the input. Moreover, the input voltage which is delivered by the DC link is a dc voltage with small ripple thus, there is no need for additional input filtering.

MOSFET selection

The selection of the MOSFET's for a converter are of critical importance since, the efficiency, stability and reliability of the system depends highly on the switching elements. There are five key essentials to determine the characteristics of the MOSFET's that are used in a converter. The maximum input voltage of the converter dictates the maximum value of V_{ds} needed. The maximum output current of the application is also a key factor to determine the $R_{DS\,(on)}$needed. Moreover, the efficiency of the converter is affected by the switching and conducting losses of the MOSFET ($Q_{ds}\ and\ R_{DS\,(on)}$). When it comes to designing a compact product solution which can be produced and sold in a competitive price, the size and cost of every component matters [22].

Since the input voltage of the application is known, the factor of the V_{ds} can be determined. The next step is to calculate the operational current levels of the low and high side MOSFET. The current levels affect the selection of the maximum $R_{DS\,(on)}$) needed at a required V_{gs}. In order to calculate the current requirements, the duty cycles that are used in the application need to be determined. The nature of the research application dictates variable duty cycles in the range of 5-95% for the buck operation and 5-85% for the boost operation. Taking into consideration the worst scenarios, the duty cycle values will be $D_{\text{max}} = 95\%$ and $D_{\text{min}} = 5\%$.For both the high side and low side MOSFET's, the highest RMS current is calculated by Equation 26 and the lowest RMS current value is calculated by Equation 27.

$$(26)\ I_{\text{RMS-highside}} = I_{\text{in}} \cdot \sqrt{D_{\text{max}}} = 8A \cdot \sqrt{0.95} = 7.79A$$

$$(27)\ I_{\text{RMS-lowhside}} = I_{\text{in}} \cdot \sqrt{D_{\text{min}}} = 8A \cdot \sqrt{0.05} = 1.78A$$

The value of the $R_{DS\,(on)}$ is affecting the efficiency of the converter thus, the lower the value is the higher the efficiency can get. In principle, bigger MOSFET packages can host smaller $R_{DS\,(on)}$ resistances. The maximum value of $R_{DS\,(on)}$ that can result in an efficient converter solution can be roughly estimated by Equation 28 [22]

$$(28) R_{\mathrm{DS(on)max}} = \frac{t_j - t_a}{I^2_{\mathrm{max}} \cdot 1.7 \cdot R_{\mathrm{th(j-a)}}} = \frac{150 - 25}{8^2 \cdot 1.7 \cdot 50} = 22.97m\Omega$$

Where t_j is the junction temperature ≈ 150℃, t_a is the ambient temperature ≈ 25℃, I^2_{max} is the maximum input current and $R_{\mathrm{th(j-a)}}$ typically around 50℃/W.

Based on those calculations the MOSFETS that will be used have the characteristics that are presented on Table 1.

Table 1. MOSFET characteristics

MOSFET CHARACTERISTICS	
$\boldsymbol{V_{DS}}$ Drain to Source Voltage	100V
$\boldsymbol{I_D}$ continuous drain current	10.3A
$\boldsymbol{R_{DS(on)}}$ Static drain to source on resistance	10.3mΩ

Theoretical Efficiency

In every power application, the total efficiency of the system is playing an important role. When it comes to power conversion, a high efficiency design is desired. The main causes that affect the efficiency of a DC-DC converter are the inductor conduction losses, the MOSFET conduction losses and the MOSFET switching losses [23]. Based on those parameters the total efficiency of a DC-DC converter can be estimated by Equation 29

$$(29) \quad n = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_D}$$

where, $$P_D = P_L + P_{\mathrm{FET}} + P_{\mathrm{switch}} + P_{\mathrm{other-losses}}$$

The inductor conduction losses can be calculated using Equation 30.

$$(30) \quad P_L = (I^2_{\mathrm{out}} + \frac{\Delta I_L^2}{12}) \cdot R_{\mathrm{DCR}}$$

Solving Equation 30 for $I_{\mathrm{outmax}} \approx 8A$, ΔI_Lconstant $\approx 1.6A$ and $R_{\mathrm{DCR}} \approx 6m\Omega$ dc resistance of inductor, gives a result of $P_L \approx 0.385W$.

The conduction losses of the high and low side MOSFETs can be calculated using the Equations 31, 32.

$$(31)\ P_{Q1} = I^2_{\mathrm{RMS_{Q1}}} \cdot R_{\mathrm{DS(on)1}} = (I_{\mathrm{in}} \cdot \sqrt{D})^2 \cdot R_{\mathrm{DS(on1)}}$$

$$(32)\ P_{Q2} = I^2_{\mathrm{RMS_{Q2}}} \cdot R_{\mathrm{DS(on)2}} = (I_{\mathrm{in}} \cdot \sqrt{1-D})^2 \cdot R_{\mathrm{DS(on2)}}$$

Solving Equations 31 and 32 for the worst case when $I_{\mathrm{in}} \approx 8A$, $D = 0.5, 1 - D = 0.5$ and $R_{\mathrm{DS(on1)}} = R_{\mathrm{DS(on2)}} = 10.3m\Omega$ results in $P_{Q1} = 0.3296$W and $P_{Q2} = 0.3296$W.

The switching losses of the MOSFETs are a function of the load current and the switching frequency. More specifically the switching losses can be calculated using Equation (33) $P_{SW} = V_{\mathrm{in}} \cdot I_{\mathrm{out}} \cdot f_s$ ·33.

$$(33)\ P_{SW} = V_{\text{in}} \cdot I_{\text{out}} \cdot f_s \cdot \frac{Q_{GS} + Q_{GD}}{I_G}$$

Based on the values given in the datasheet of the MOSFETs and considering the worst case parameters $V_{\text{inmax}} = 100V$, $I_{\text{outmax}} = 8A$, $f_s = 250Khz$, $Q_{GS} = 1.6nC$, $Q_{GD} = 17.3nC$, $I_{\text{Gmax}} = 0.7A$. Solving Equation 33 gives a result of maximum switching losses P_{SW} ≈5.4W. Thus, the total losses resulting only from the known parameters of the system are

$$P_D = 0.3296 + 0.3296 + 0.385 + 5.4 + P_{\text{other-losses}} \approx 6.442W + P_{\text{other-losses}}$$

The other power losses are resulting from quiescent current losses, power supply losses, and PCB losses that cannot be calculated.

SYSTEM CONTROL & SIMULATION

In this chapter, the controlling of the converter will be presented as well as the model that was built in Simulink to simulate the power stage at different operational modes (buck, boost and buck-boost). The controlling of the DC-DC converter is essential to ensure a stable and reliable system which can react rapidly in sudden changes of the input voltage of the DC link, or requested power from the end-devices. The support of the DC grid by the end devices (batteries of the hosts) as a backup plan in the unlikely event of a DC source failure, creates an extra focus on the bidirectional power flow control.

The design of the control is implemented in separate steps [24]. The first step is to define the main components of the system such as the filter capacitors, the magnitude of the inductor and the controlling MOSFET's which are ensuring a stable operation during the steady state operation of the system. The choices that were taken for the research application have already been analyzed in the second chapter. The next step is to define the different operational modes that the converter needs to support, in order to provide the power needed at the output of the system under the requested voltage levels. At this step, it is critical to analyze how the different operational modes are interacting and under which circumstances there is a transition from one mode to the other. When a dynamical model of the controller has been implemented, the tuning is the last step to achieve a set of transient specifications such as minimum overshoot and fast response time.

Controlling Methods

Before focusing more on the controlling of the system, it is essential to make an overview of the controlling methods that are used to control the power flow in DC-DC conversion systems. Depending on the topology of the system, such as Buck, Boost, Buck-Boost, Cuk, Flyback, Push-Pull or other topologies, and the converter specifications, different techniques are used to provide a stabilized and controlled output [25]. Some of the most well-known methods are presented below :

1. **Voltage Control**: It is a single closed loop control, where the output voltage is measured and compared with the reference value that has been specified. The produced error is used to drive a compensation loop, usually a PID controller in order to generate a correction action on the PWM signal which drives the switching MOSFET. This method is considered as a simple control method but presents some disadvantages. The reliability is poor when multiple converters are used in parallel and the controlling response is rather slow in comparison to other methods.
2. **Current Control**: It is a double closed loop control, which consists of a voltage control loop followed by a current control loop. Initially, as in the case of the voltage control method, the output voltage is measured and compared to a reference value. The output of the this comparison is fed to a compensation loop which provides the reference for the current control loop. This reference is compared to the measured current, at the output of the converter (or the current of the inductor) and the result is fed to a second compensation loop. This compensation loop is generating a correction action on the PWM signal which drives the switching MOSFET. The current control method presents several advantages. It has better transient response as the order of the system is reduced to first order [25]. The overload is avoided since it is protected by the control loop. Thus, the switching MOSFETS have better protection. The main disadvantage of the current control method is the increased instability for duty cycles over 50%.

3. **Sliding Mode Control**: A sliding mode control is used when the system is non-linear. This control method is implemented in two steps. Initially a sliding layer needs to be defined and consequently a control rule to drive the system from a random primary state to approach the sliding layer in a specific amount of time. At some point the system meets an equilibrium state, that is the origin point of the phase plane [25]. The advantage of the sliding mode control, is that it can be used in nonlinear systems, has high robustness and fast response. On the contrary, the controlling parameters depends strictly on the system specifications thus, there are no available standard IC components in the market to implement this type of control.
4. **Fuzzy Logic Control**: Another method of controlling non-linear systems is the fuzzy logic. A fuzzy logic controller is composed by four stages, which are the fuzzifier, rules, inference engine and defuzzifier. The first step is the collection of Crisp data which are translated into linguistic terms or membership functions through the fuzzifier. Consequently an inference is made based on a set of rules that is predefined. Finally the outcome is deffusified into Crisp data and can used to control a system. The fuzzy logic presents the advantage to upgrade the logic by improving or adding new rules and also provide a stable converter performance under load discrepancy [26].

Based on the research done on the controlling methods it was selected to follow the current control loop method since it is a simple method which can easily be tuned and provide high power conversion efficiency. In the second chapter, the converter topology that will be used and needs to be controlled was introduced. The four-quadrant converter shown in Figure 28 uses four MOSFET's that can operate in all modes (buck, boost, buck boost) and can transport energy in both directions. When controlling the switches in a certain way, the topology can transform in any mode following the dynamics as analyzed in chapter two. The analysis of the modes is being done based on the assumption that the converter operates under continuous conduction mode (CCM). The following Table 2 shows which switches are conducting in every mode and direction [27].

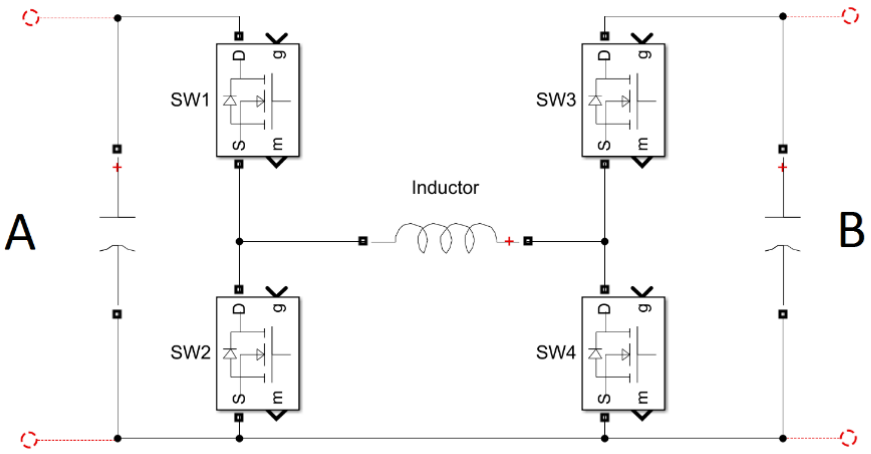


Figure 28. Bidirectional four quadrant topology

Table 2 Operational Mode vs Conducting Switches

Power Flow Direction	Operational Mode	SW1	SW2	SW3	SW4
A→ B	Buck	Active (D)	Active $(1-D)$	1	0
A→ B	Boost	1	0	Active $(1-D)$	Active (D)
A→ B	Buck-Boost	Active (D)	Active $(1-D)$	Active $(1-D)$	Active (D)
B→ A	Buck	1	0	Active (D)	Active $(1-D)$
B→ A	Boost	Active $(1-D)$	Active (D)	1	0
B→ A	Buck-Boost	Active $(1-D)$	Active (D)	Active (D)	Active $(1-D)$

In every operational mode, the purpose is to regulate the average DC output voltage appropriately to match the specifications of the application. For a known input voltage, the output voltage is regulated based on the switching time of the MOSFET's. When a constant frequency f_s is used, the control of the MOSFET can be implemented by regulating the ON time of the switch. This method is called pulsed width modulation (PWM) and the width is defined by the duty cycle D which is the ratio of the time that the switch is conducting to the total period time T_s.

Switching Schemes

In this sector, the switching scheme of the MOSFETS for every operational mode, is explained in detail. When the input voltage is higher than the desired load voltage and power needs to be transferred from A to B, the converter is operating as a buck converter. As shown in Table 2, SW1 is active and being driven by the duty cycle D that is produced by the PWM signal. The complementary switch SW2 is driven by the complementary duty cycle $D-1$. A dead time is necessary between conduction of the switches to avoid short-circuiting the supply. During the period T_s the third switch SW3 is always conducting and the fourth switch SW4 is always not conducting with the antiparallel diode being always reverse biased. The inductor current flow sequence is presented in Figure 29.

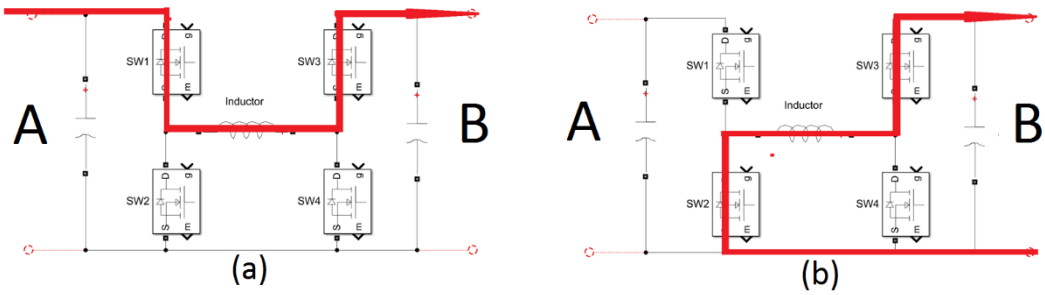


Figure 29. Inductor current sequence of Buck converter from A to B (a) $0 \leq t \leq T_{\text{on}}$, (b)$T_{\text{on}} \leq t \leq T_s$

In Figure 30, the switching scheme of the switches SW1-SW4 is presented during buck operation mode and power direction from A to B. The change on the inductor current is visible.

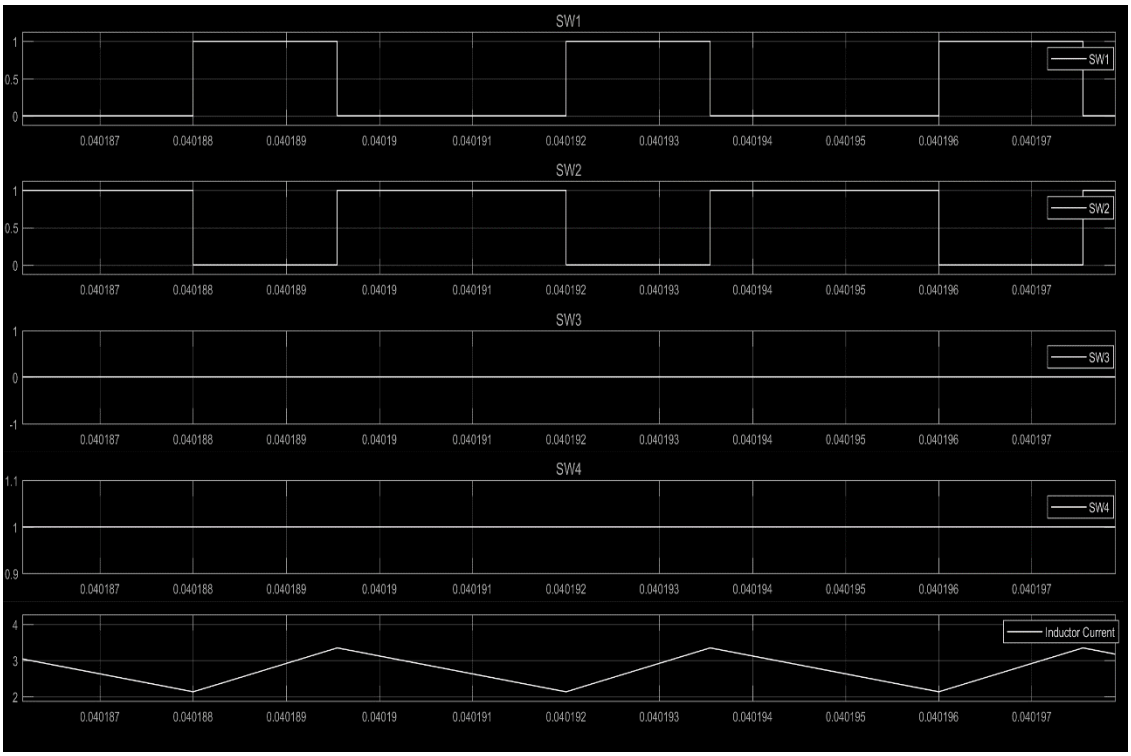


Figure 30. Switching scheme of switches SW1-SW4 of Buck converter from A to B

When the input voltage is lower than the desired load voltage and power needs to be transferred from A to B, the converter is operating as a boost converter. As shown in Table 2, SW4 is active and being driven by the duty cycle D that is produced by the PWM signal. The complementary switch SW3 is driven by the complementary duty cycle $D-1$. During the period T_S the first switch SW1 is always conducting and the second switch SW2 is always not conducting with the antiparallel diode being always reverse biased. The inductor current flow sequence is presented in Figure 31.

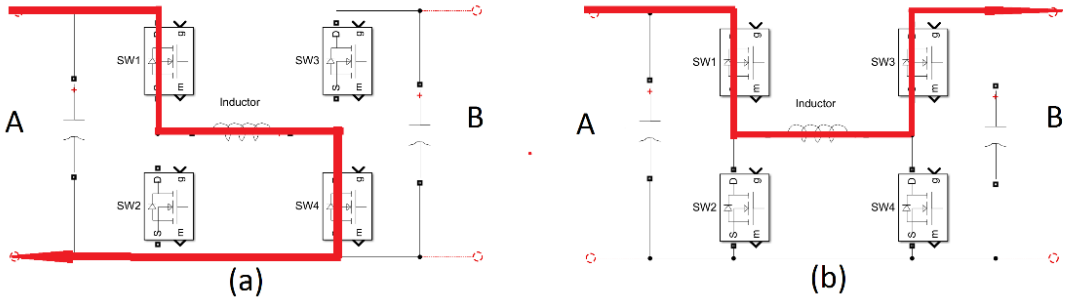


Figure 31. Inductor current sequence of Boost converter from A to B (a) $0 \leq t \leq T_{on}$, (b)$T_{on} \leq t \leq T_s$

In Figure 32, the switching scheme of switches SW1-SW4 is presented during boost operation mode and power direction from A to B. The change on the inductor current is visible

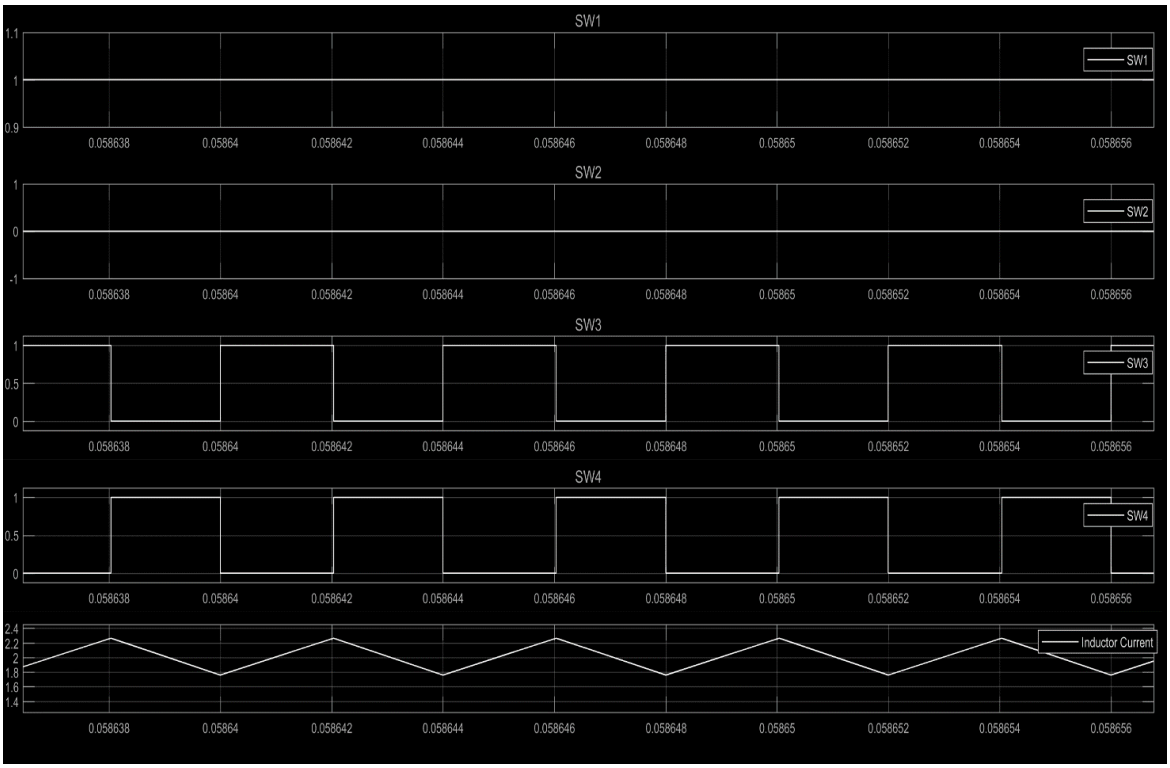


Figure 32. Switching scheme of switches SW1-SW4 of Boost converter from A to B

When the input voltage is very close to the desired load voltage $V_{in} = V_{out} \pm 0.3V$ and power needs to be transferred from A to B, the converter is operating as a buck-boost converter. This operation mode is necessary since there is physical limitations on the minimum and maximum duty cycles. The details of the limitations have been explained in the second chapter in the buck-boost operation. As shown in Table 2 in this case, switch SW1 is operating as a pair with SW4 and the pair of switches SW2, SW3 are operating complementary to the first pair. Thus, SW1 and SW4 are driven by the duty cycle D that is produced by the PWM signal. The complementary duty cycle $D - 1$ is driving SW2 and SW3. The inductor current flow sequence is presented in Figure 33.

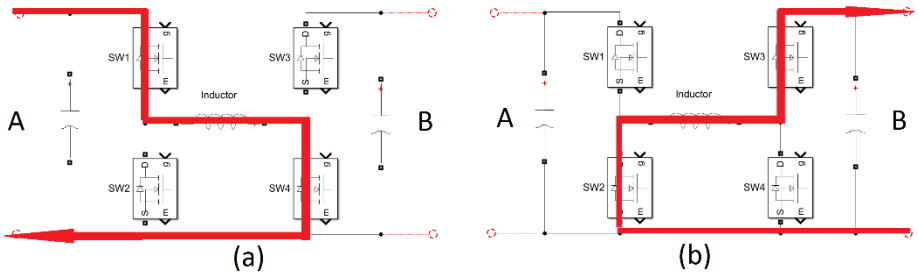


Figure 33. Inductor current sequence of Buck-Boost converter from A to B(a) $0 \leq t \leq T_{on}$,(b)$T_{on} \leq t \leq T_s$

In Figure 34, the switching scheme of switches SW1-SW4 is presented during buck-boost operation mode and power direction from A to B. The change on the inductor current is visible.

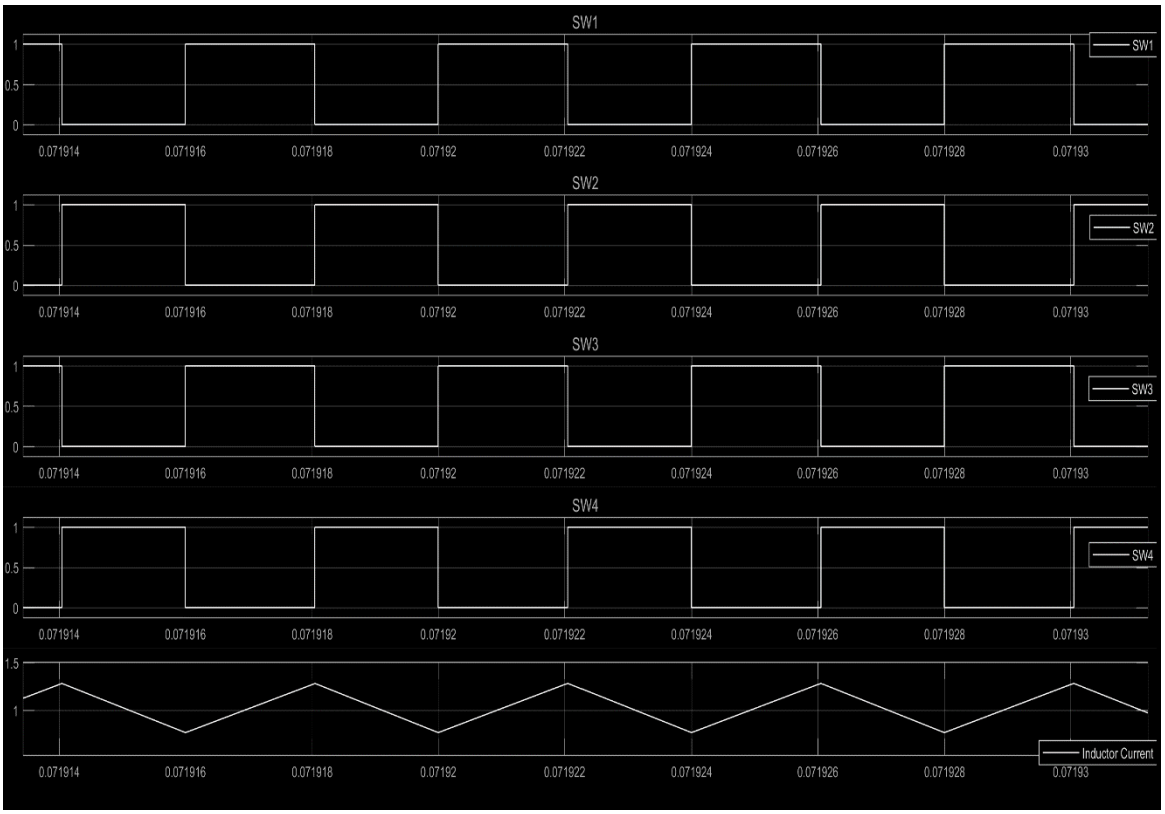


Figure 34. Switching scheme of switches SW1&SW4 and SW2&SW3 of Buck-Boost converter from A to B

When the output voltage is higher than the desired load voltage in the input and power needs to be transferred from B to A, the converter is operating as a buck converter with reverse power flow. As shown in Table 2 in this case, SW3 is active and being driven by the duty cycle D. The complementary switch SW4 is driven by the complementary duty cycle $D-1$. During the period T_s the first switch SW1 is always conducting and the second switch SW2 is not conducting. The inductor current flow sequence is presented in Figure 35.

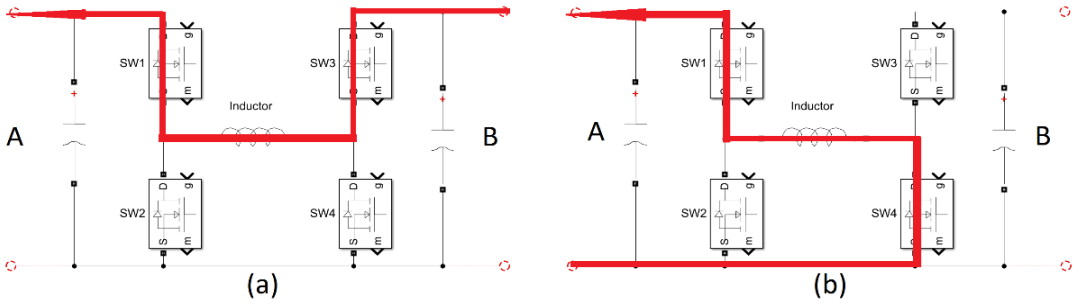


Figure 35. Inductor current sequence of Buck converter from B to A (a) $0 \leq t \leq T_{on}$, (b) $T_{on} \leq t \leq T_s$

In Figure 36, the switching scheme of switches SW1-SW4 is presented during buck operation mode and power direction from B to A. The change on the inductor current and the inverted polarity due to change in the power direction is shown.

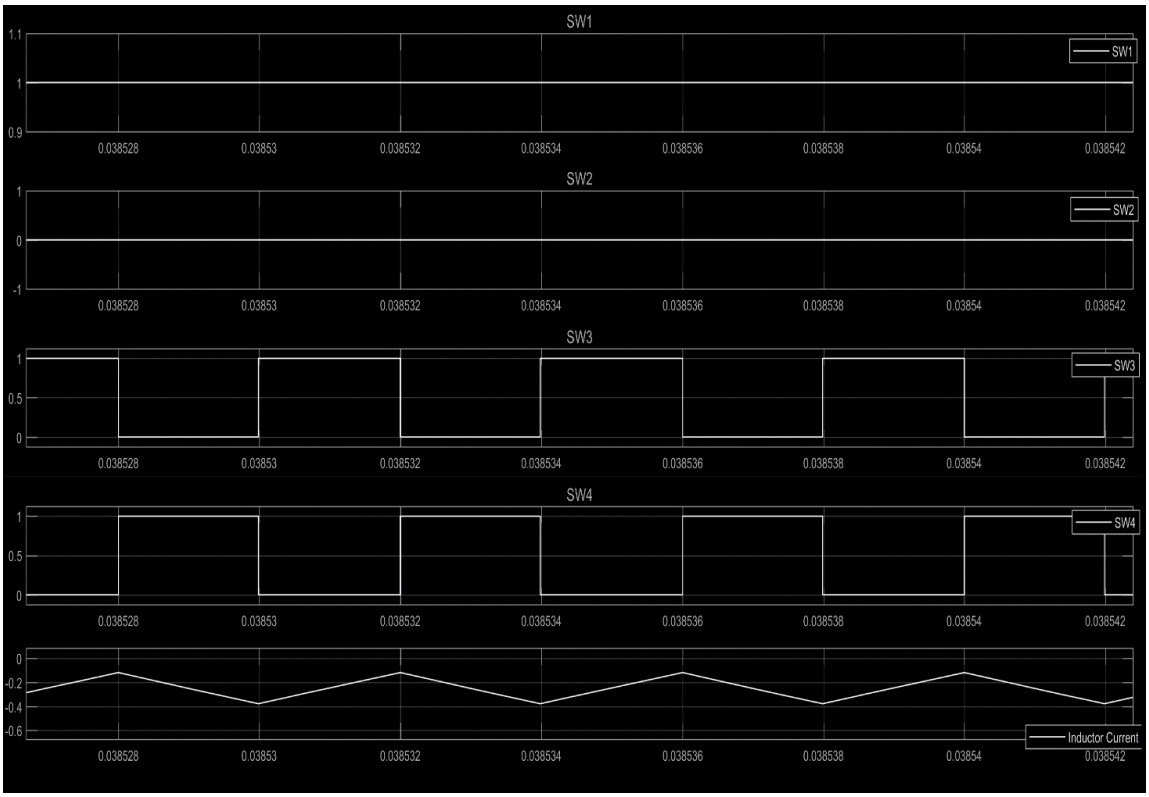


Figure 36. Switching scheme of switches SW1-SW4 of Buck converter from B to A

When the output voltage is lower than the desired load voltage in the input and power needs to be transferred from B to A, the converter is operating as a boost converter. As shown in Table 2 in this case, SW2 is active thus driven by the duty cycle D. The complementary switch SW1 is driven by the complementary duty cycle $D-1$. During the period T_s the third switch SW3 is always conducting and the fourth switch SW4 is not conducting. The inductor current flow sequence is presented in Figure 37.

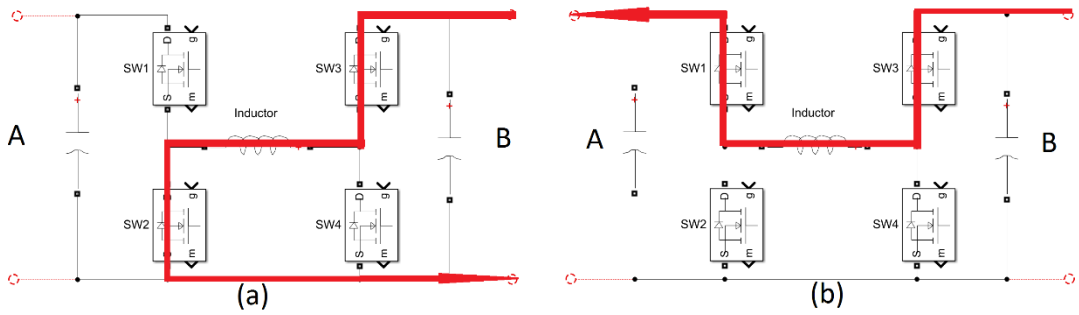


Figure 37. Inductor current sequence of Boost converter from B to A (a) $0 \leq t \leq T_{on}$, (b) $T_{on} \leq t \leq T_s$

In Figure 38, the switching scheme of switches SW1-SW4 is presented during boost operation mode and power direction from B to A. The change on the inductor current and the inverted polarity due to change in the power direction is presented.

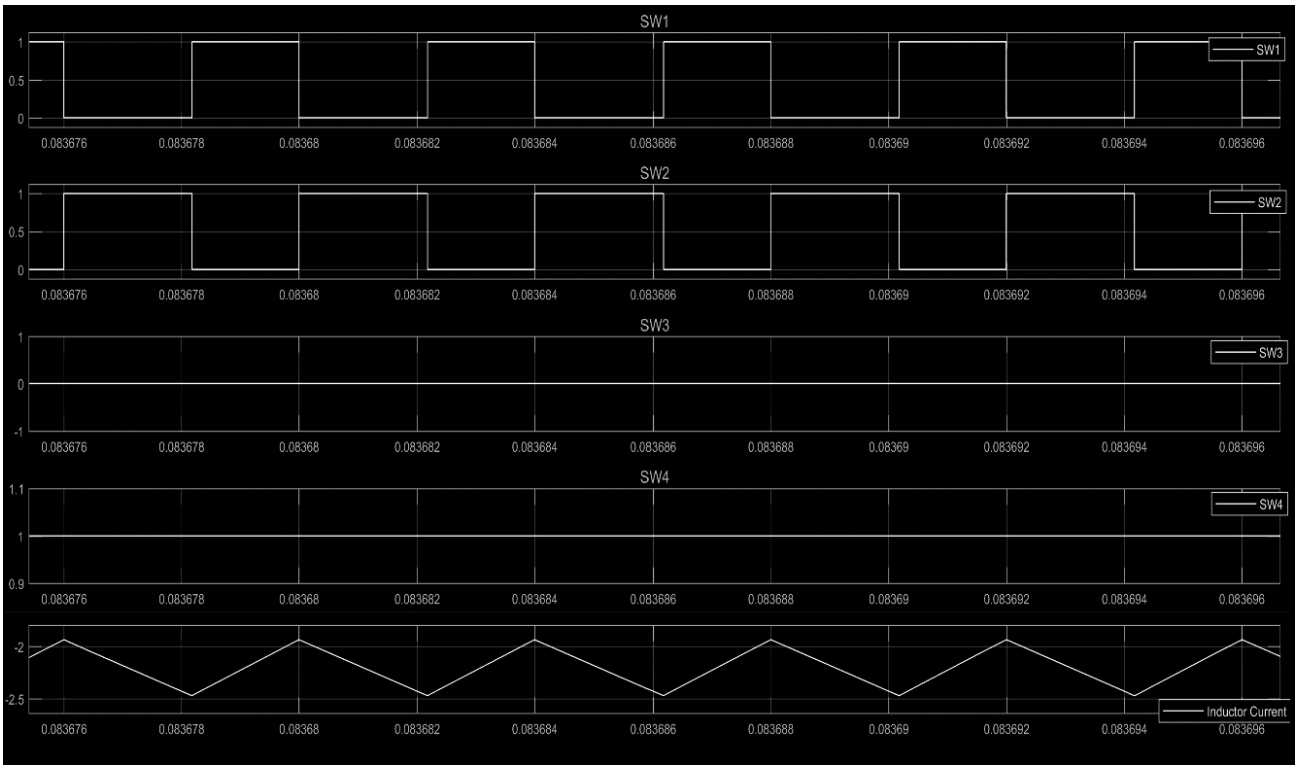


Figure 38. Switching scheme of switches SW1-SW4 of Boost converter from B to A

When the output voltage is very close to the desired load voltage $V_{out} = V_{in} \pm 0.3V$ at the input and power needs to be transferred from B to A, the converter is operating as a buck-boost converter. As shown in Table 2 in this case, switch SW3 is operating as a pair with SW2 and the pair of switches SW4, SW1 are operating complementary to the first pair. Thus, SW3 and SW2 are driven by the duty cycle D that is produced by the PWM signal. The complementary duty cycle $D - 1$ is driving SW4 and SW1. The inductor current flow sequence is presented in Figure 39.

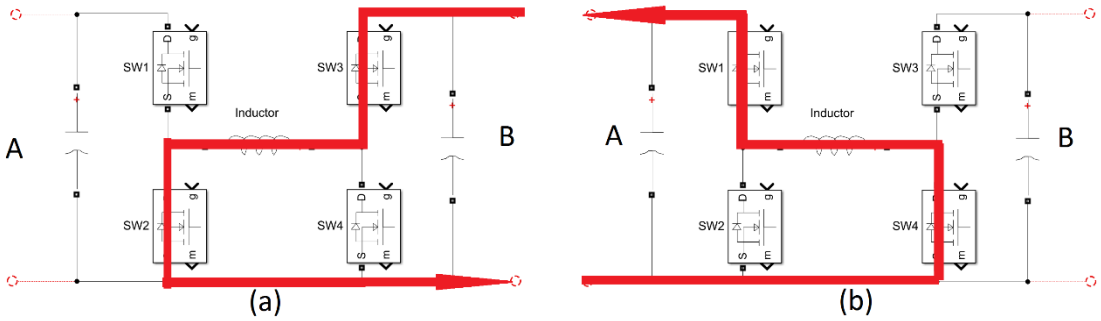


Figure 39. Inductor current sequence of Buck-Boost converter from B to A (a)$0 \leq t \leq T_{on}$,(b)$T_{on} \leq t \leq T_s$

In the switching scheme of switches SW1-SW4 is presented during buck-boost operation mode and power direction from B to A. The change on the inductor current and the inverted polarity due to change in the power direction is presented in Figure 40.

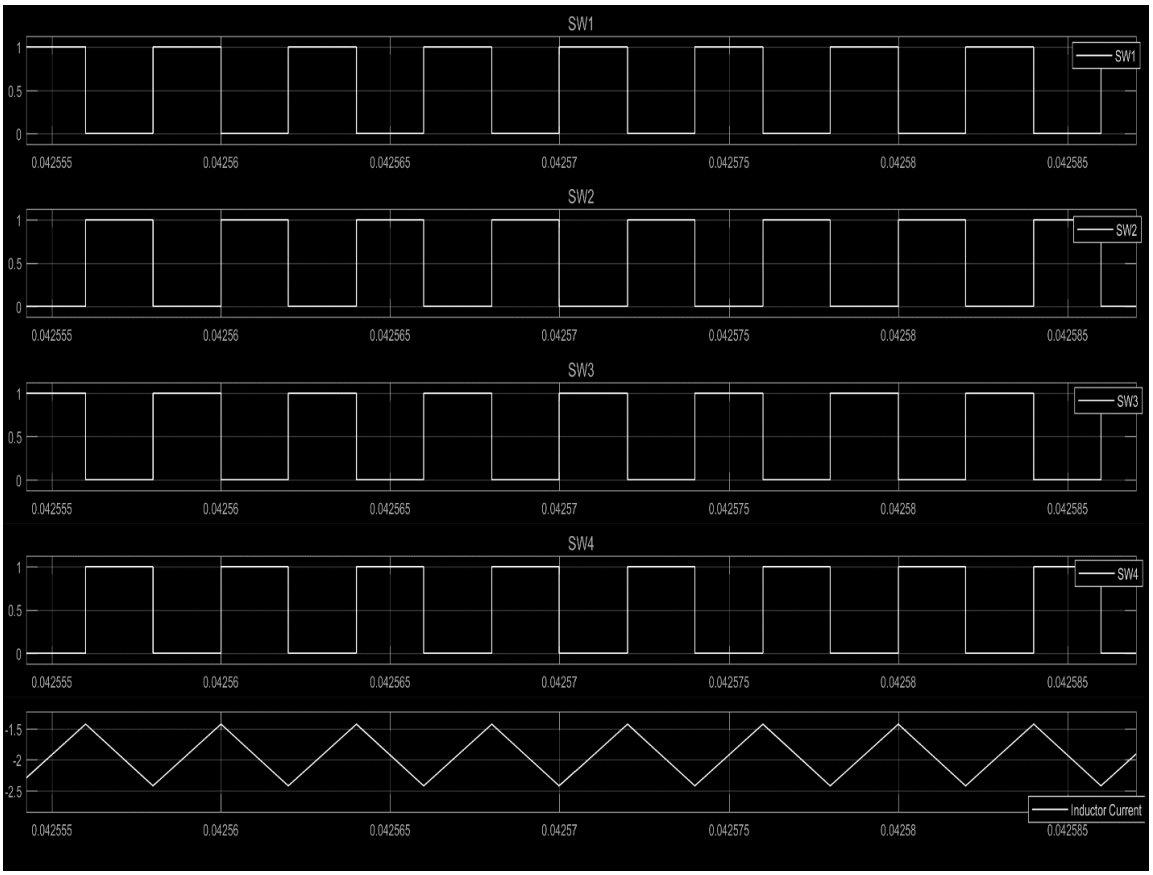


Figure 40. Switching scheme of switches SW1&SW4 and SW2&SW3 of Buck-Boost converter from B to A

Controller Design

After defining all the operational modes, it is important to explain how the different modes are interacting and under which circumstances there is a change of operation mode. Figure 41 presents the functional block diagram of the controller. At the beginning of the control loop, the controller checks which side of the converter presents the highest input voltage. The control theory is based on the fact that the input of the converter is always attached to the DC link and the output is attached to the end-devices through the USB-type C cable. For the design of the controller, an assumption has been taken into consideration that the DC link is acting as the default source and the end-devices are acting as the default sinks.

The DC link is presenting a voltage which can range between 10-100V. Assuming that the DC link is providing constant voltage of 20V at the input of the DC-DC converter once a device is connected at the output, the controller will measure both voltages at the input and the output. The output voltage is measured for the first time before the end-device applies any voltage on the V_{BUS} node. Thus, if the DC link provides voltage over the boundary value the controller is checking the FB_{pin} status. The FB_{pin} provides information regarding the desired output voltage. If the desired output voltage is $FB_{pin} \leq D_{BUCK-MAX} \cdot V_{in}$ that means that the converter can support the output voltage by operating as a buck converter. If the desired output voltage is $FB_{pin} \geq \frac{V_{IN}}{1-D_{BOOST-MIN}}$, that means that the converter can support this output voltage by operating as a boost converter. If the FB_{pin} is between those two values, it means that the output voltage can only be supported by a buck-boost operation.

While the converter is operating in any operational mode, the controller is checking whether the DC input can keep supporting properly the output voltage. If at any moment, the DC link voltage falls lower than the boundary conditions, the controller will check again the initial

conditions. If the voltage of the connected device is higher than the DC link voltage, then the converter will swap the power flow and it will provide power to the DC link. As shown in Figure 41, the controller follows exactly the same principles to decide which operational mode should be selected to support properly the powering of the DC link.

In addition, while an operational mode has been selected, the controller provides the flexibility to swap between the buck, boost and buck-boost modes. If, for example, the input voltage of the DC link changes from 20V, while providing 15V supply on the output, to 10V then the mode will be swapped from buck to boost. If the DC link voltage change from 20V, while supplying 15V on the output, to 15V then the operational mode will change from buck to buck-boost mode.

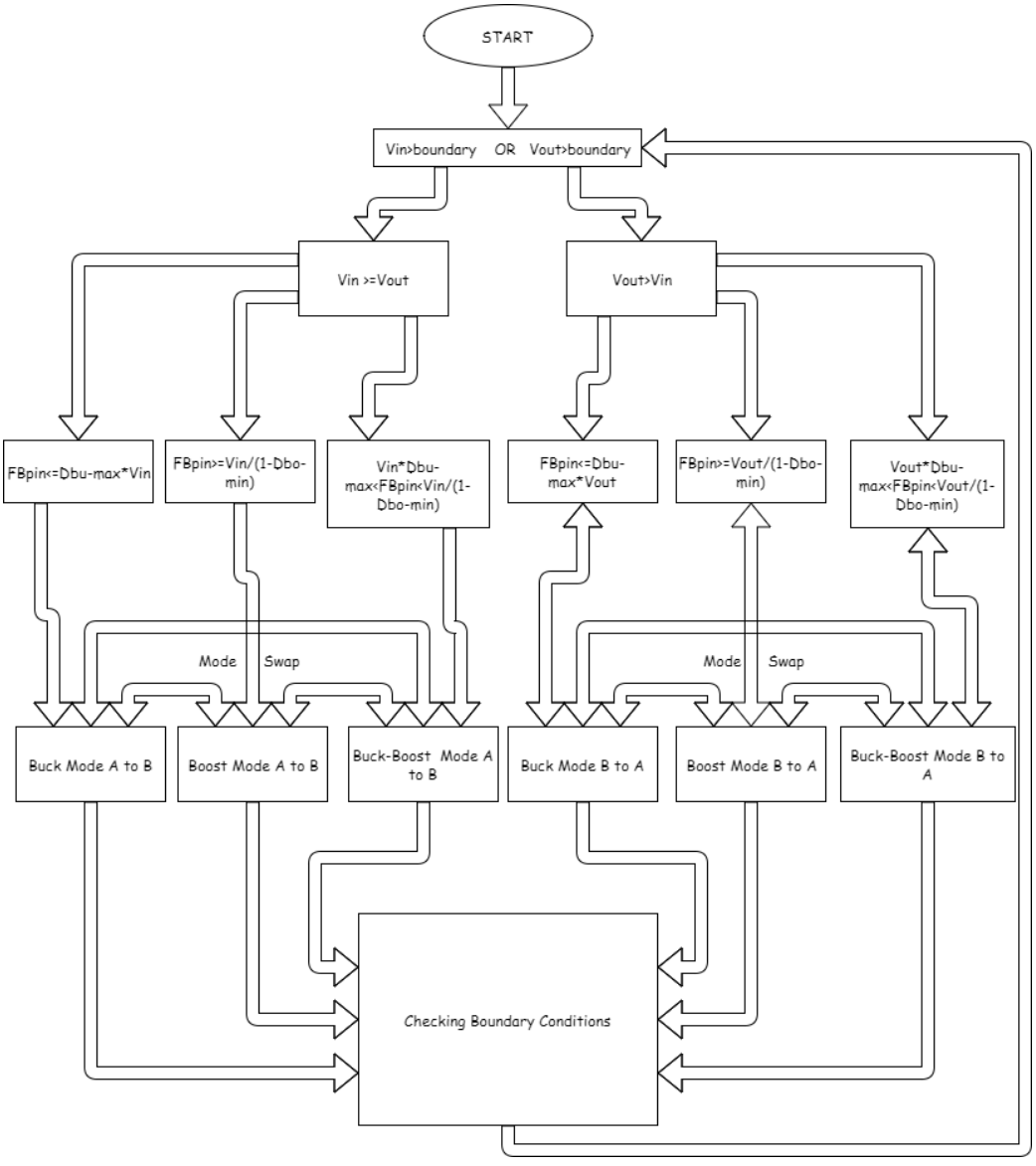


Figure 41. Controller Functional Diagram

Digital Control

In this section an analysis is made to understand how the duty cycles, which drive the different MOSFET's SW1-SW4, are generated and regulated. Any changes in the desired output voltage or current, or in the supply voltage or current have to be appropriately manipulated by the controller of the DC-DC converter. In this way, a stable output voltage and current, within the specification limits, to the end-devices or to the DC-link is ensured. As already mentioned in the introduction of this chapter, the pulse width modulation (PWM) method is used to drive the controlling signals of the switching MOSFET's. Usually, the control of the width of the pulse is being done by an IC which is dedicated to this task. Since the application that is being implemented within the scope of this thesis is custom, a microcontroller which can support up to four PWM signals is used and a digital control is realized.

The use of a digital control instead of an analog, provides benefits such as lower power consumption and reduction of application cost. The fact that many microcontrollers in the market offer the functionality of multiple PWM channels, encourages the development of digital controlling methods.

In the PWM, the duty cycle is defining the width of the pulse. The value of the duty cycle can be calculated using several methods. Depending on the characteristics of the system, the input and desired output voltage as well as the current limitations of the input and the output, the duty cycle needs to be adjusted appropriately. The method that was chosen to regulate the duty cycles is the use of a PI controller (Proportional-Integral).

The PI controller [28] is one of the most common forms of feedback control in a closed-loop system. The principle of a PI controller is to attempt to eliminate the error between the measured feedback value and the reference point which has been set. In every loop, depending on the magnitude of the error the controller is enforcing an action that can adjust the process accordingly. By using feedback measurements of the input voltage, input current, output voltage and output current as well as the desired reference values the PI controller is able to regulate the output voltage and current accordingly.

PID Controller

The PID controller uses three different parameters to enforce a correcting action on the controlled parameter. The P parameter (proportional value), affects the correcting action based on the current error between the measured value and the reference point, the I parameter (integral value) influences the correcting action based on the sum of the previous errors and the D parameter (Derivative value) based on the changing rate of the error. By tuning the three quantities, the PID algorithm can provide a control action based on the system specifications. By optimizing the value of the parameters, the response time can be minimized and the stability of the control can be improved.

The function that describes the PID controller is outlined in Equation $(34$ where K_p, K_i, K_d are all non-negative factors representing the terms P, I, D. The $u(t)$ is the control signal and the $e(t)$ is the control error [29].

$$(34)\ u(t) = K_p e(t) + K_i \int_0^t e(r)dr + K_d \frac{de(t)}{dt}$$

Proportional Parameter

The P (proportional parameter) is affecting the control signal based on the present error value. The proportional reaction can be manipulated by multiplying the present error $e(t)$ with the gain factor K_p. The proportional factor is defined by the term:

$$P_{out} = K_p e(t)$$

Where t is the present time, K_p is the proportional gain, e is the error (set point- present value), and P_{out} is the proportional output. When the proportional gain is too big, the P_{out} change is also large for a given error. When the proportional gain is small, then for a specific error, the change of P_{out} is respectively small thus, making the control less responsive. In the case that the proportional gain is very small, the controller would not be able to react in small system instabilities [29].

Integral Parameter

The integral parameter I is defined by both the size of the error as well as the duration of the error. Summarizing the errors occurred at each sampling time, results in the compensation that should have been adjusted previously. The summarized error is multiplied by the integral gain and added to the controlling signal $u(t)$. The integral parameter is defined by the term:

$$I_{out} = K_i \int_0^t e(r)dr$$

The integral factor tends to reduce the steady state error that is occurring due to the proportional term. Due to the fact that the integral parameter is accruing the errors that have happened in the past, a big integral gain will result in a big overshoot of the offset value. A large integral gain might cause an unstable control that can never stabilize at the reference set point value.

Derivative Parameter

The derivative term is contributing in the error elimination by taking into account the rate of change of the error over time. The change of the error over time is being multiplied by the derivative gain. The derivative parameter is defined by the term:

$$D_{out} = K_d \frac{de(t)}{dt}$$

The derivative parameter offers the advantage of a slower controlling signal change, when the feedback value approaches the set point value. This is contributing to the elimination of the overshoot which is produced by the integral term. Though, the derivative term makes the system very sensitive to noise and thus, often it is being excluded by the controlling algorithm in order to prevent control instability.

In Figure 42 the block diagram of the PID controller is being presented.

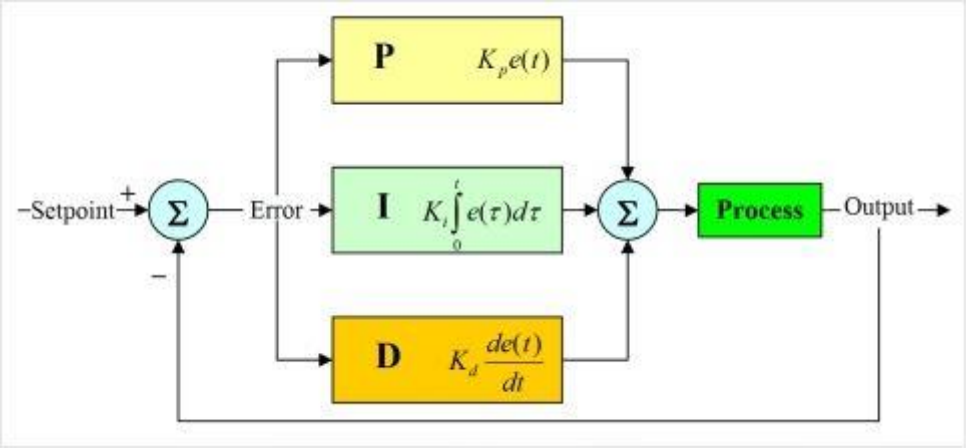


Figure 42. Block diagram of PID controller [30]

For the thesis application, the derivative term has been excluded from the control in order to avoid high complexity which can lead to system instability. Thus a PI controller has been realized in order to define the appropriate value of the duty cycle needed to achieve the reference point value of the voltage and current. Every operational mode presents different dynamics, thus for every operational mode the optimized values of the proportional and integral gain are different. Therefore, for every operational mode there is a dedicated PI controller. Depending on the operational mode, the controller selects to use the different PI controller in order to obtain the appropriate value for the duty cycle needed. In Figure 43, the different PI controllers are presented.

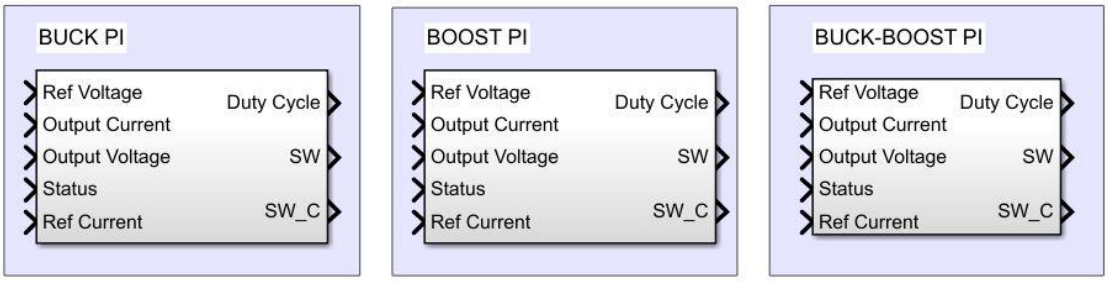


Figure 43.Buck, Boost, Buck-Boost PID

PID Tuning

In order to tune the gain parameters for the PID controllers there are several methods known as tuning methods. Some of the most important factors that need to be taken into consideration when tuning a PID controller are the load disturbances, load changes, noise on the system or process uncertainty. One of the most well-known methods that has been used widely in the automation industry for the tuning of PID controllers is the Ziegler Nichols method [28].

In order to tune the PID controller using the Ziegler Nichols method, the first step is to zero all the gain parameters. Then, the P parameter needs to be increased up to the point that the control loop gives constant and stable fluctuations. When the value of the optimal P gain has been found P_{opt} then the fluctuation period T_{fl} is assisting to tune the optimal value for the I and D gain. In Table 3, the factors to calculate the P, I and D gains are shown [31].

Table 3. Ziegler-Nichols Tuning Method [31]

Ziegler-Nichols method			
Controller	K_p	K_i	K_d
P	$0.5P_{opt}$	–	–
PI	$0.45P_{opt}$	$T_{fl}/1.2$	–
PD	$0.8P_{opt}$	–	$T_{fl}/8$
PID	$0.6P_{opt}$	$T_{fl}/2$	$T_{fl}/8$

Using the Ziegler-Nichols method and adjusting the values based on the experimental data that emerged from the MATLAB model, the values shown in Table 4 were used for the PI controllers.

Table 4. Gain values

Gain Values				
MODE	***Voltage PI***		***Current PI***	
Gain	K_p	K_i	K_p	K_i
Buck	0.71	32	0.63	310
Boost	0.007	8.1	0.0072	80
Buck – Boost	0.13	1.1	0.13	10

Voltage & Current Control

The purpose of the control is to be able to achieve the requested voltage by meeting the current limitations dictated by the end-device. In order to achieve that through the digital control, some limitations need to be set for every PI controller. Every PI controller is fed with the reference voltage and current, dictated by the end- device or the DC link depending on the operational mode. Each PI controller is composed by two PI controllers in series. Initially, the reference voltage is compared with the present voltage level at the output of the DC-DC converter and the error value is fed at the first PI controller.

The first PI has a low and a high saturation limit. The low limit is set to zero and the upper limit is set to the current reference thus, the output of the first PI cannot exceed the maximum allowed current. The output of the first PI is compared to the present output current and the error value is fed to a second PI controller. The second PI controller has also a low and high saturation limit which is dictated by the minimum and maximum allowed duty cycle which can drive the MOSFET's. In Figure 44, the expanded block of the PI is presented. The absolute values for the output voltage and current have been used in order to implement the bidirectional form of the control. The output of the PI controller is the produced duty cycle signal which is provided to the PWM generator. A complementary signal is produced for the complementary switches. The status box is used to trigger the respective PI controller box (BUCK, BOOST or BUCK-BOOST).

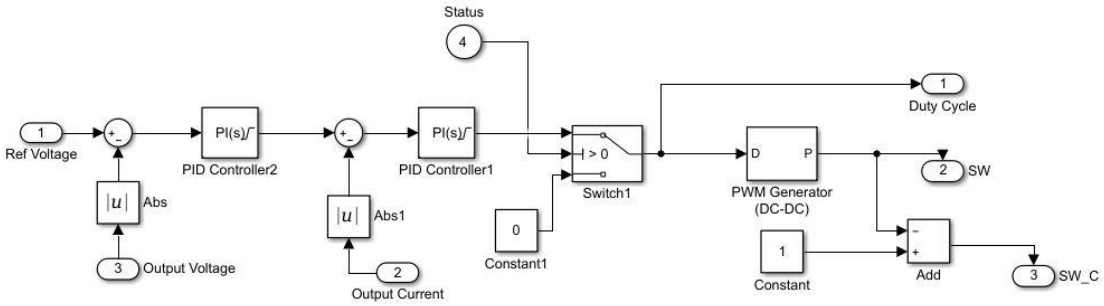


Figure 44. Function block of PI controller

Power Stage Simulation

In order to be able to study the behavior of the DC-DC bidirectional converter, the power stage was built in MATLAB. As shown in Figure 45, the four quadrant topology is simulated using the MOSFET's SW1-SW4. Voltage and current measurements are used at the input and output in order to be able to control the desired voltage and current outputs as well as the power flow direction. An identical design with two resistors at the input and output has been realized. The MOSFET's being in series with the resistors are used to enable the participation of the resistors in the circuit. The two pairs of resistors are composed of a small resistor $R_{int} = 10m\Omega$, which is considered as an internal resistance of the source and a bigger resistor $R_{LOAD} = 25\Omega$,which is used as a load resistance. These two resistors are able to simulate the change of the source and the load at any given moment in order to investigate the transition phase when the power direction is alternating.

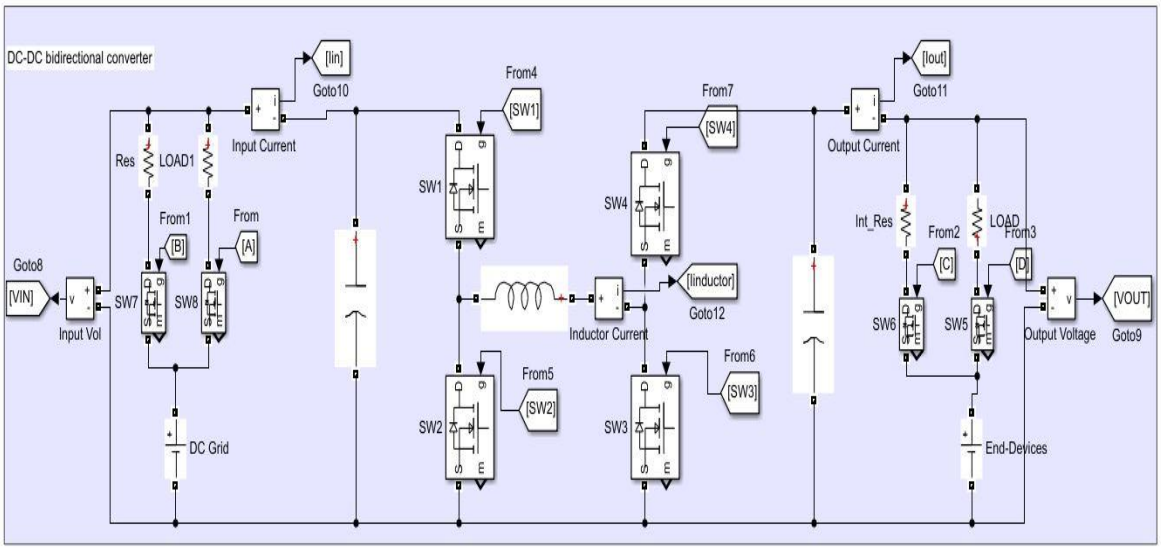


Figure 45.Power Stage Simulation

The control signals SW1-SW4 are being produced by the PI controllers depending on the operational mode and the direction of the power flow. The logic of the controller has been explained previously in section 0 and the source code is provided in Appendix . The simulation of this part has been implemented through a MALTBAL function as shown is Figure 46. The controller is fed by the input and output voltage and current, the requested voltage and the current limitation of the sink. The present and previous state of the operational mode is provided to the controller to allow the transition to a different mode only when specific

parameters have changed. After the controller has defined which operational mode should be applied, the corresponding mode signal is enabled which in turn drives the relevant PI controller.

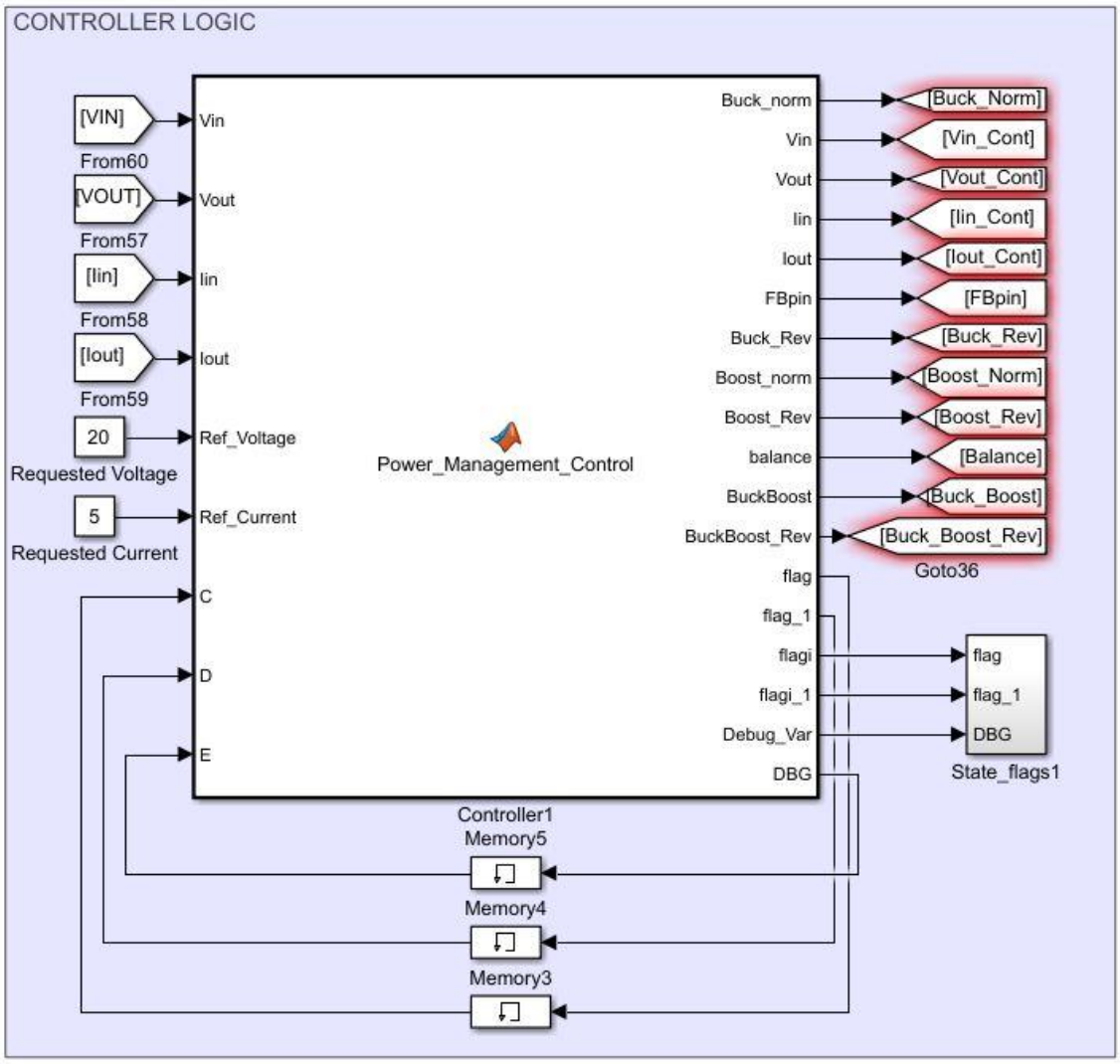


Figure 46. Main Controller Block

Since every switch can obtain four different states (active-pulsed, active-complementary, passive-on and passive-off) a switching logic has been implemented to drive the correct signal to the each MOSFET SW1-SW4.

Simulation Results

In order to verify the advisability of the controlling algorithm in combination with the power stage of the system, some scenarios were created to test the results. As explained in the introduction of chapter 0, it is assumed that the source of the DC-DC bidirectional converter is a low voltage DC link ranging between 10-100V. The purpose of the DC-DC bidirectional converter is to provide power to end-devices such as laptops, smart-phones or tablets and acquire power from them to support the DC link when the DC grid presents a failure. Therefore, some case scenarios were developed which are presented in Table 5.

Table 5. Simulation Scenarios

Scenario	Mode	DC Link (Voltage)	End-Device (Operating Voltage)	End Device (Max Current)
1St Case			***Smartphone***	
	Buck	10 V	5 V	1 A
	Buck	20 V	5 V	1 A
	Buck	30 V	5 V	1 A
2nd Case			***Tablet***	
	Boost	10 V	12 V	1 A
	Buck − Boost	12 V	12 V	1 A
	Buck	50 V	12 V	3 A
3rd Case			***Laptop***	
	Boost	15 V	20 V	3 A
	Buck − Boost	20.2 V	20 V	5 A
	Buck − Boost	19.7 V	20 V	5 A
	Buck	50 V	20 V	3 A
4th Case			***Smartphone***	
	Buck	24 V	5 V	1 A
	Source Failure	0	5 V	1 A
	Boost Reverse	24 V	5 V	1 A

1st Scenario

In the first case it is assumed that a smartphone is connected to the output of the DC-DC converter. The BMS of the smartphone dictates that the required charging voltage is 5V and the maximum allowed current is 1A. Assuming that the DC link presents some fluctuations, the simulation starts with a DC link voltage of 10V. In Figure 47, the response of the controller is shown and the output voltage is regulated at 5 V approximately after 10ms.

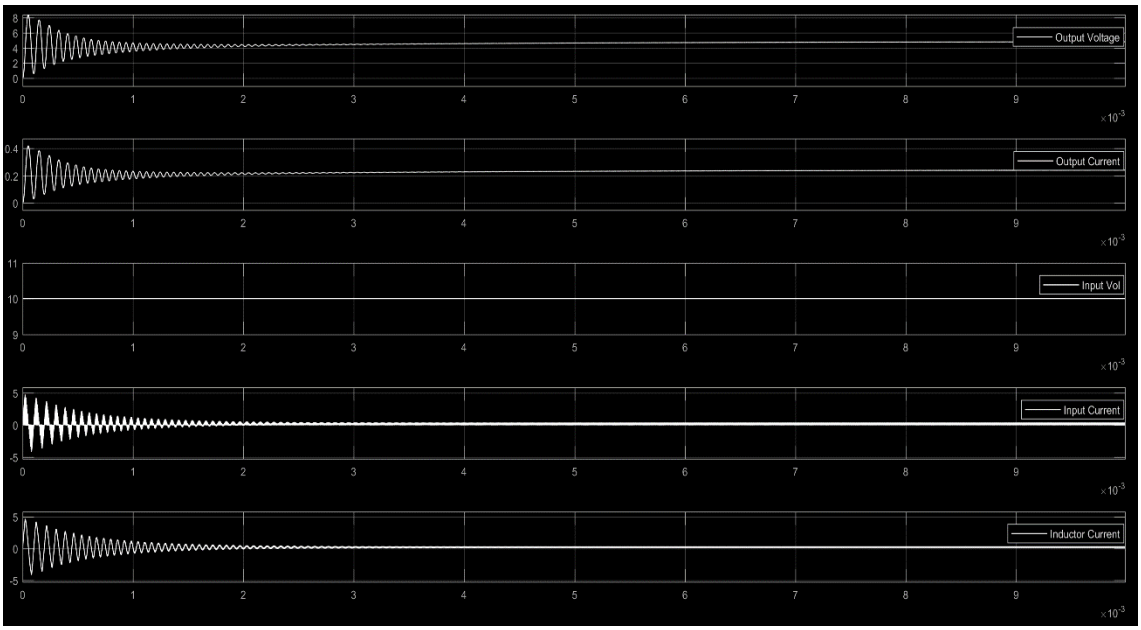


Figure 47. 1st Case Scenario- DC link (10V) - Smartphone (5V)

When the output voltage has been regulated to 5V, it is assumed that there is a fluctuation in the DC link thus, the input voltage is changing from 10V to 20V. The response of the controller is immediate and after approximately 2ms the output voltage is stabilized at 5V. The results during the input voltage change are presented in Figure 48. As soon as the voltage has been stabilized, a second change in the input voltage of the DC link is assumed to test the response of the controller. The input voltage is changing from 20V to 30V and the response of the controller is presented in Figure 49.

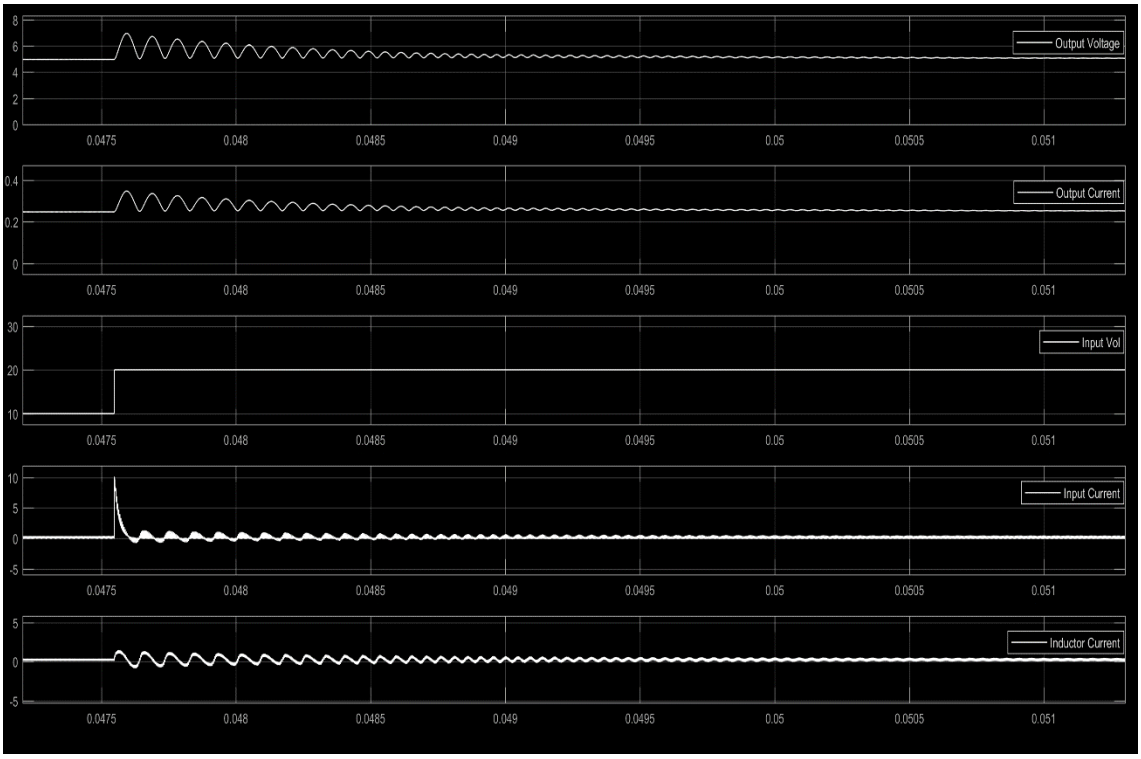


Figure 48. 1st Case Scenario- DC link (20V) - Smartphone (5V)

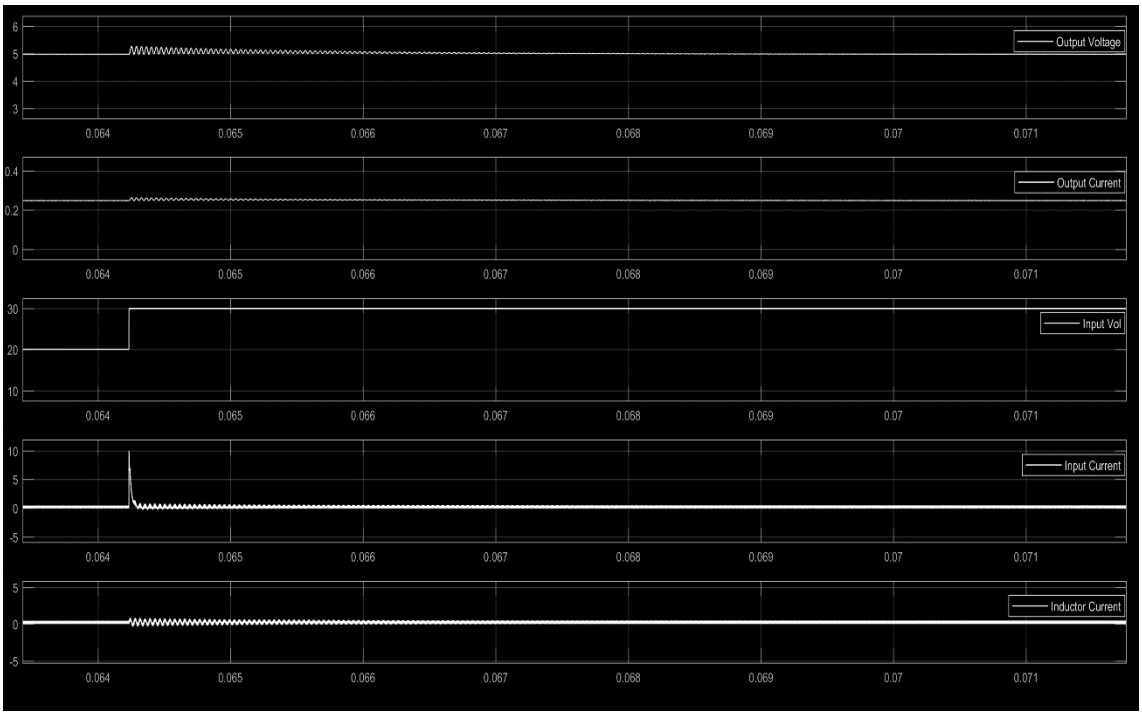


Figure 49. 1st Case Scenario- DC link (30V) - Smartphone (5V)

2nd Scenario

The second scenario of the simulation is the case that a tablet is connected to the bidirectional DC-DC converter output and according to the specifications of the tablet, it needs 12V and maximum boost mode in order to achieve the specified output. The response of the system is presented in the following Figure 50. In the case of the boost mode, the response time is slightly slower in the range of 50ms.

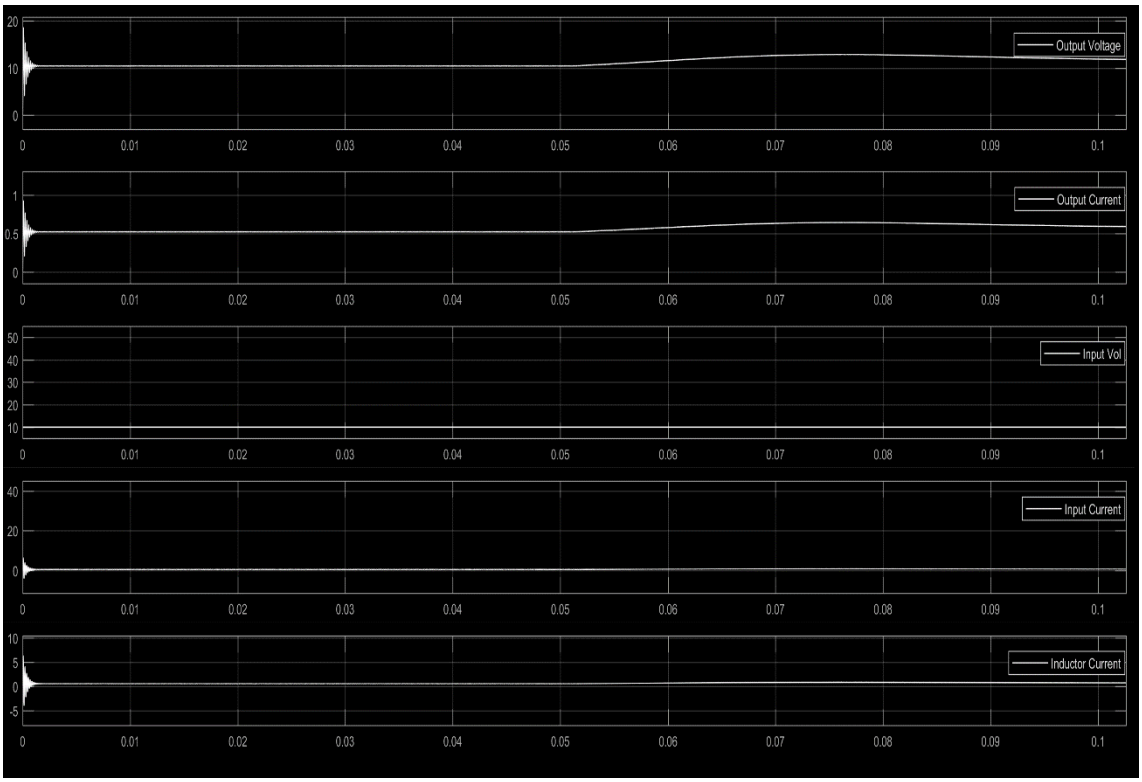


Figure 50. 2nd Case Scenario- DC link (10V) - Tablet (12V)

When the output voltage has been stabilized around 12V then, it is assumed that the input voltage provided by the DC link is changing from 10V to 12V. The converter needs to swap operational mode and change from boost to buck-boost mode. The response of the system is shown in Figure 51. The reaction time is measured around 130ms. A second change is applied and the DC link voltage increases up to 50 V. The controller is swapping to buck mode and the results are presented in Figure 52. The response time is measured around 1ms.

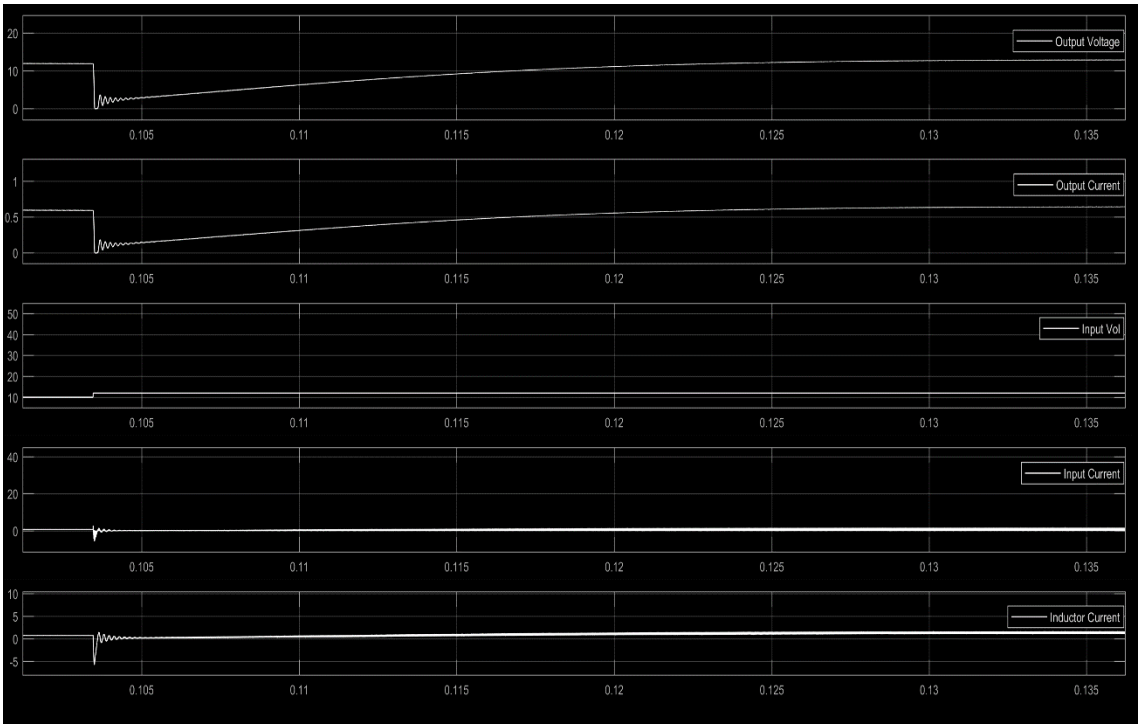


Figure 51. 2nd Case Scenario- DC link (12V) - Tablet (12V)

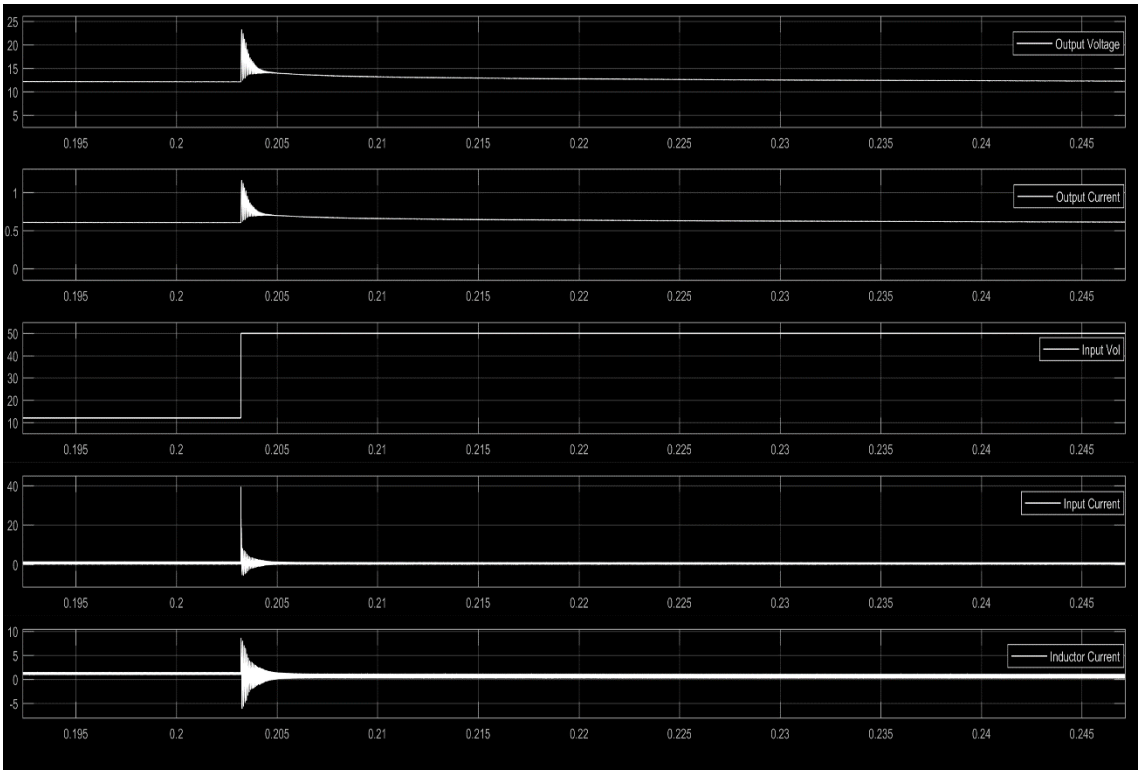


Figure 52. 2nd Case Scenario- DC link (50V) - Tablet (12V)

3rd Scenario

During this case, it is assumed that a laptop is connected to the output of the DC-DC converter and needs 20V and maximum 3A to charge. The DC link initially provides 15V at the input of the converter. Thus the converter starts operating in boost mode. The response time to reach the requested output voltage level is approximately 50ms as shown in Figure 53. As soon as the output voltage has been stabilized, the DC link voltage increases to 20.2V and the controller swaps the operational mode from boost to buck-boost mode. The response of the controller is visible in Figure 54.

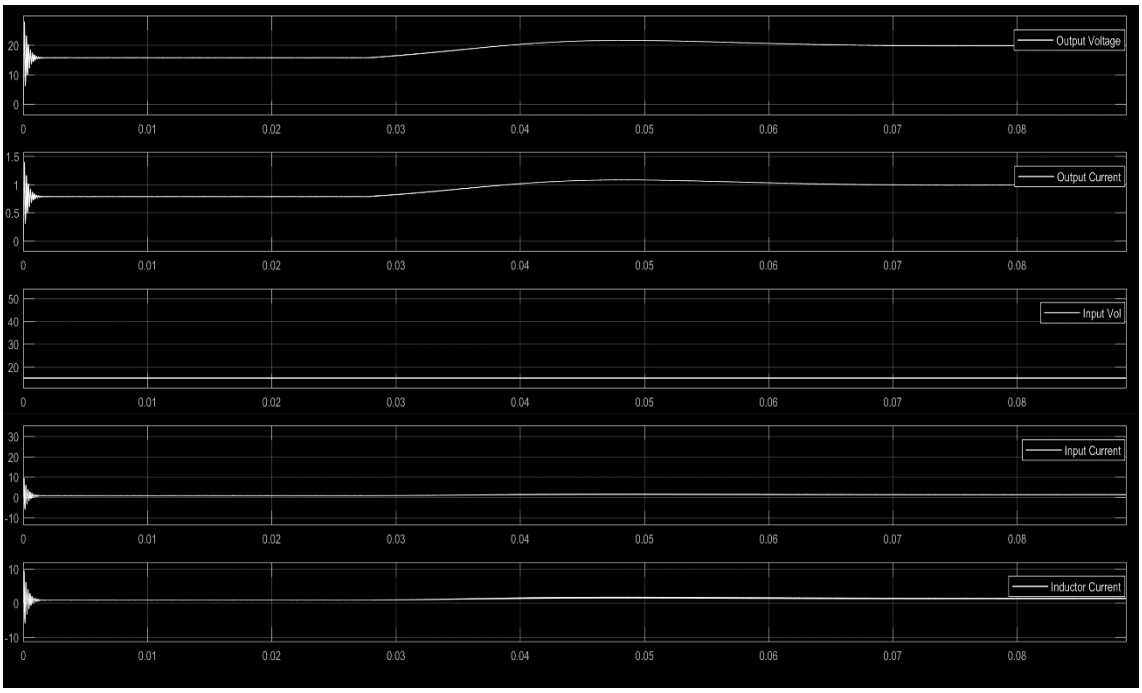


Figure 53. 3rd Case Scenario- DC link (15V) - Tablet (20V)

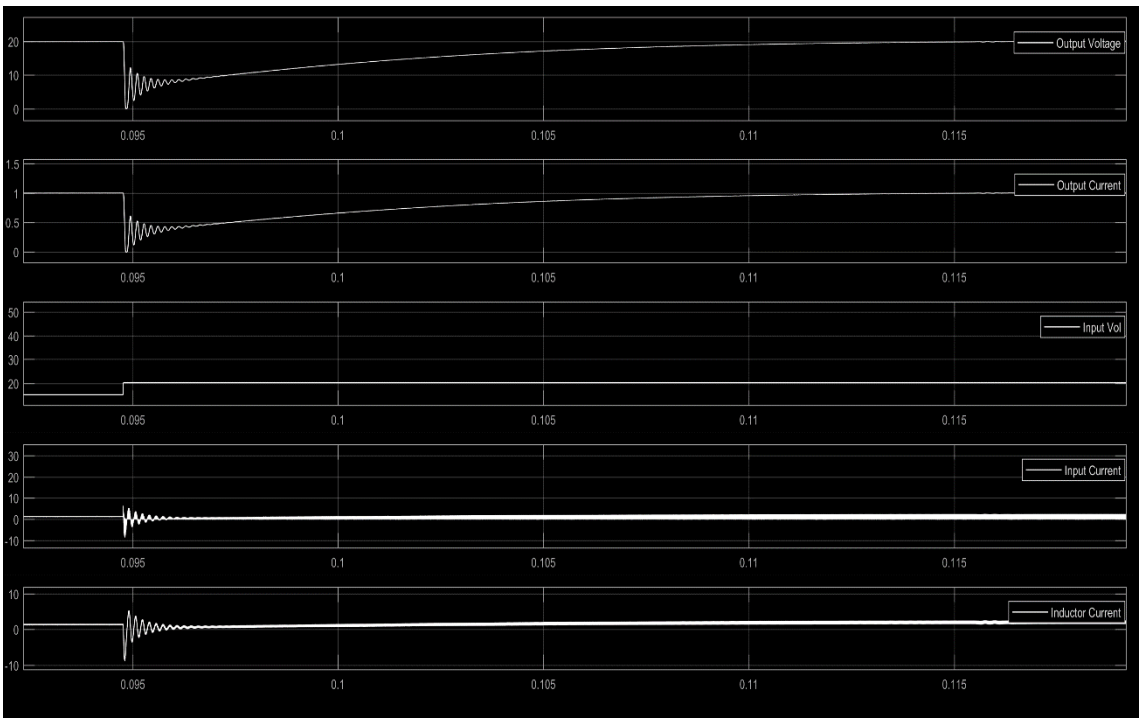


Figure 54. 3rd Case Scenario- DC link (20.2V) - Tablet (20V)

A change in the voltage of the DC link is realized again and therefore changes from 20.2V to 19.7V. The operational mode stays as buck-boost and after a small oscillation, the control soothes the output voltage at 20V. In Figure 55, the response of the controller is presented. As a final step, the DC input voltage increases suddenly at 50V. The controller alters the operational mode to buck conversion and the results are shown in Figure 56.

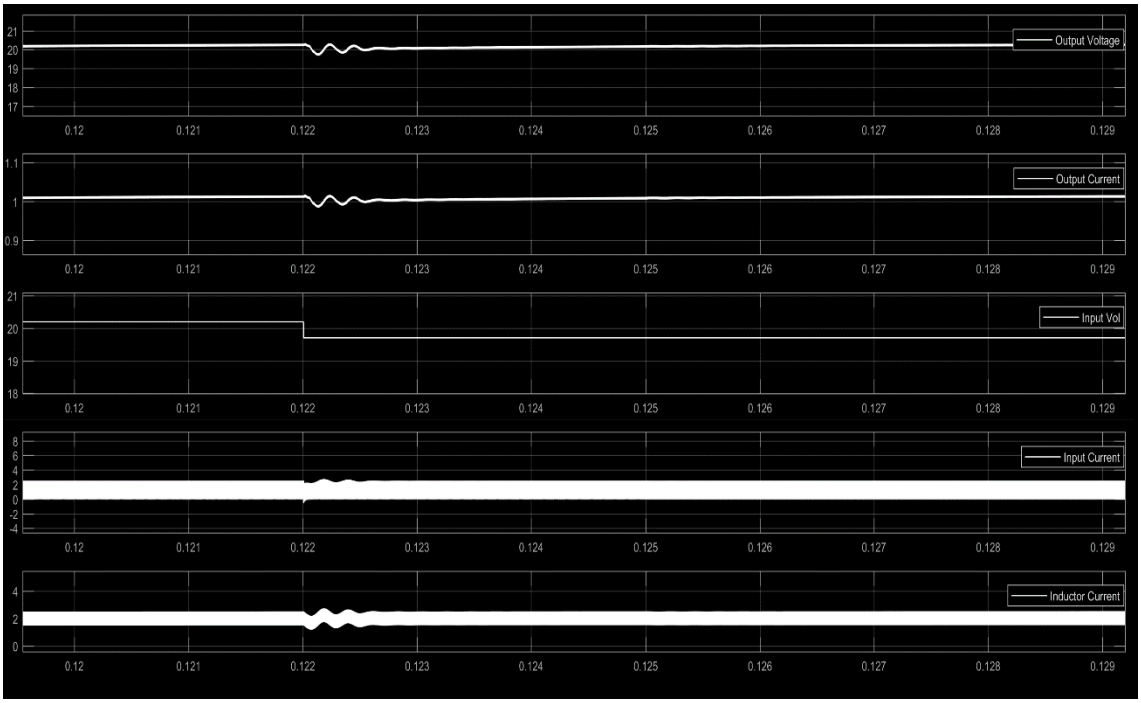


Figure 55. 3rd Case Scenario- DC link (19.7V) - Tablet (20V)

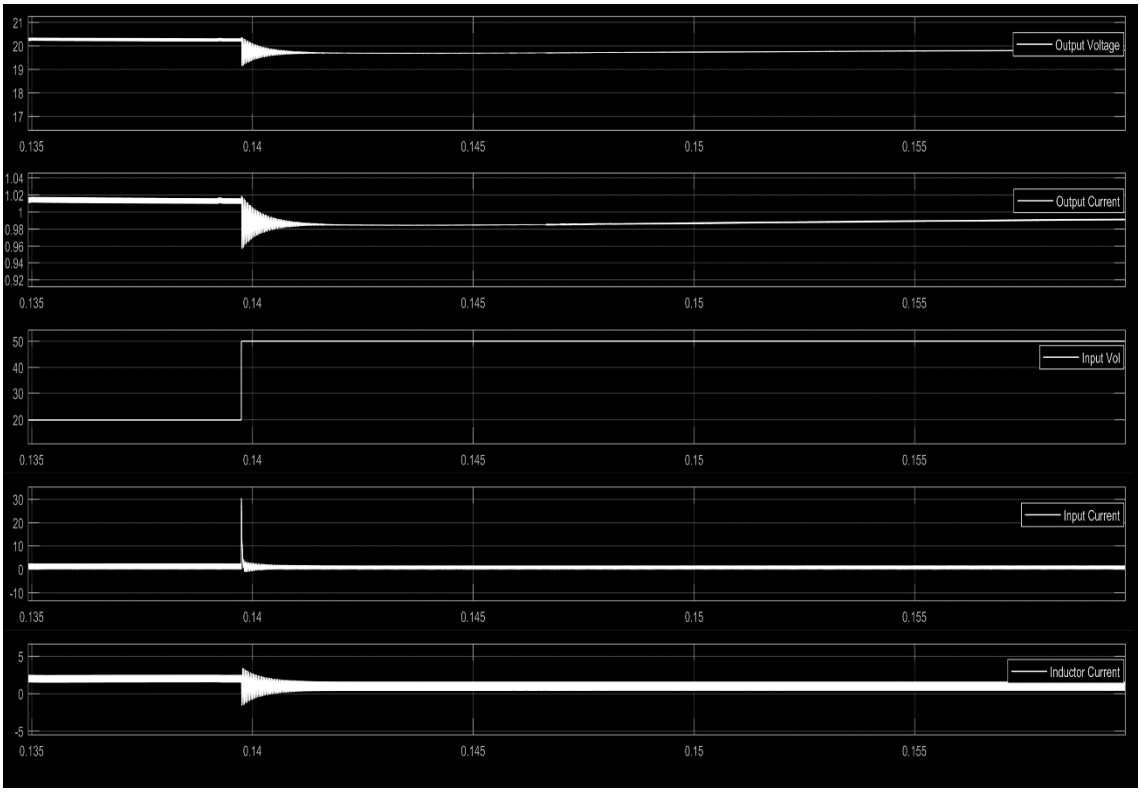


Figure 56. 3rd Case Scenario- DC link (50V) - Tablet (20V)

4th Scenario

The last case was developed to prove the swap of the power flow in the case that there is a source failure from the DC link of the building. As stated in the Introduction chapter, the goal of the bidirectional DC-DC converter is to be able to support the DC grid of a smart building, by using the Li-ion batteries of the interconnected smart devices such as laptops, smartphone or tablets. In this scenario the case where a smartphone is connected at the output of the DC-DC converter is realized.

Initially the DC link provides 24V at the input of the converter and the phone starts charging. The converter is regulated to produce a voltage of 5V at the output of the converter with a maximum current of 1A. At some point a source failure is presented in the system and the input of the converter drops to 0V. The controller senses this drop, isolates the input and the output from the DC link and measures again the input and output voltage. Since the output voltage, where the smartphone is connected is this time higher than the DC link voltage the mode swaps from buck_normal to boost_reverse. The voltage at the DC link starts increasing and is regulated at 24V as shown in Figure 57.

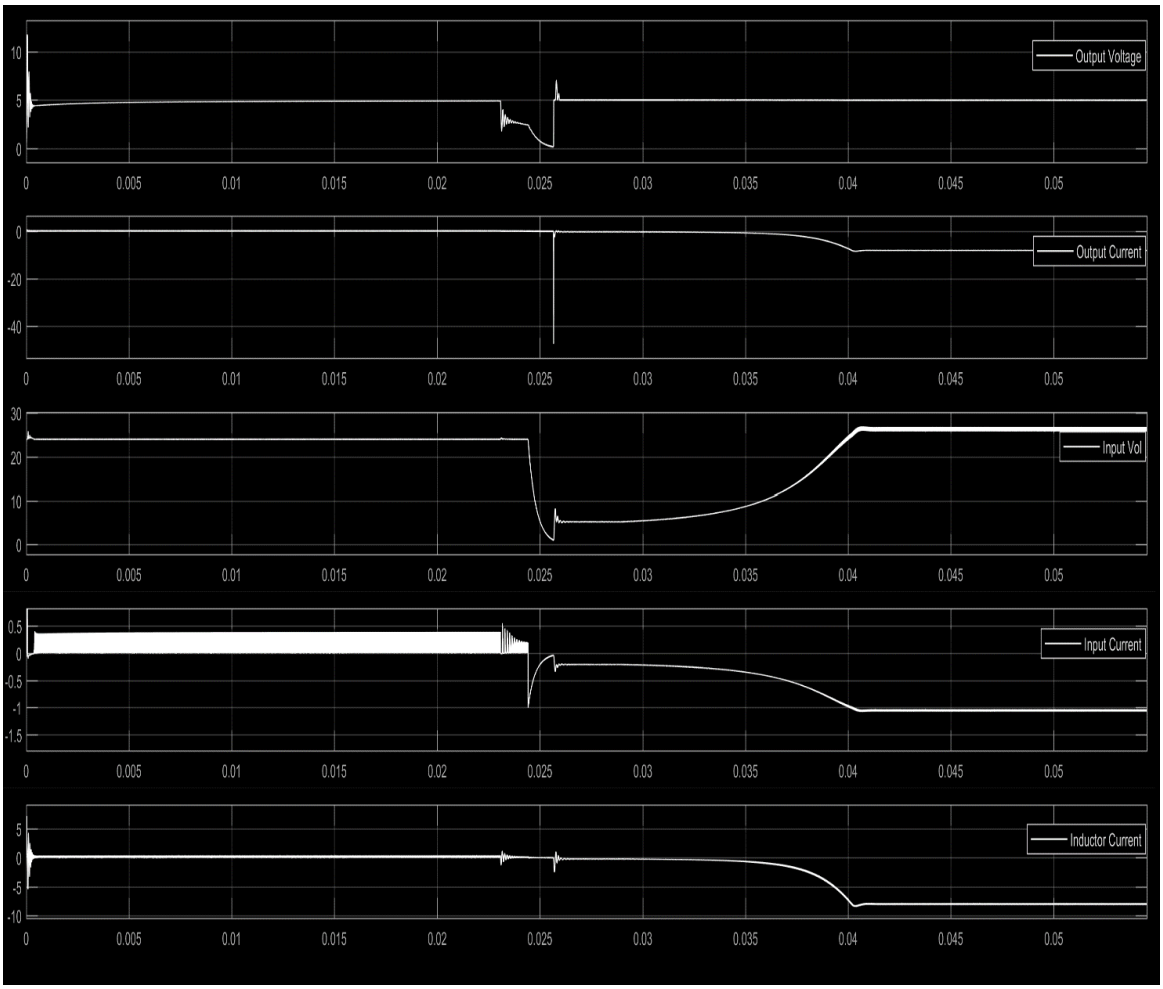


Figure 57. 4th Case Scenario- Power Swap

HARDWARE IMPLEMENTATION-PCB DESIGN

After completing the theoretical analysis regarding the development and control of the bidirectional DC-DC converter, as well as proving the concept idea using a model based design in Simulink-MATLAB, the hardware implementation was realized. For the better understanding of the system, a functional block diagram is provided in Figure 58 showing exactly how the different component groups are collaborating to create a hardware solution, which corresponds to the requirements of the thesis application.

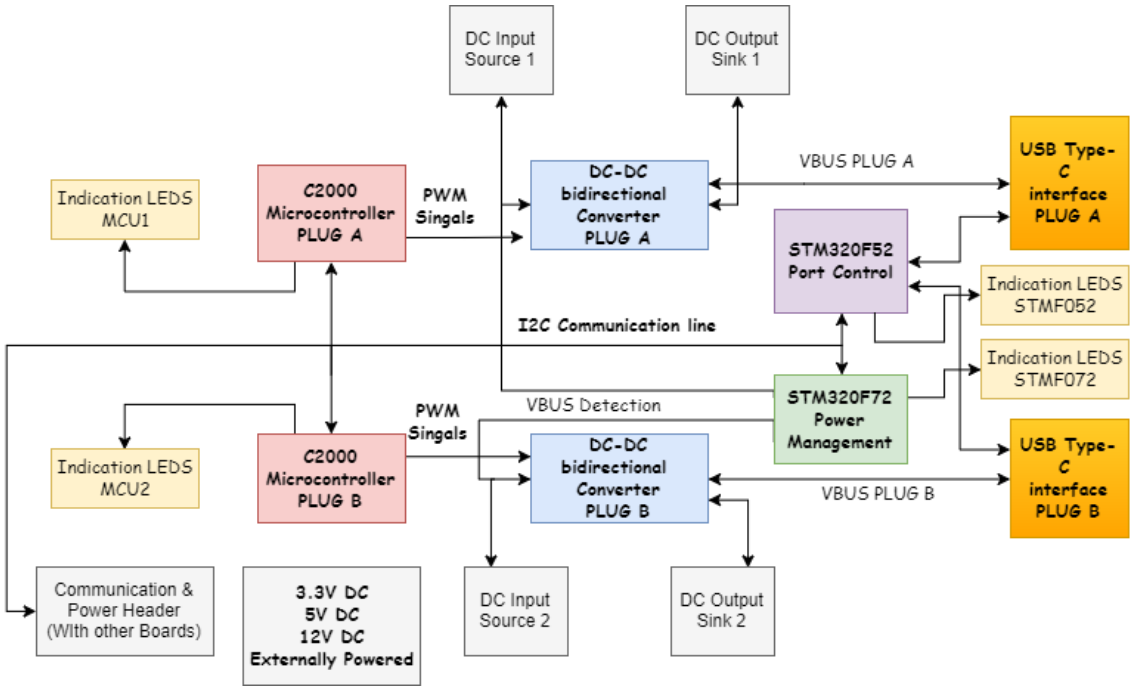


Figure 58. Hardware Functional Block Diagram

For clarification of the system architecture, the functional blocks are explained below in detail:

1. **C2000 TI Microcontrollers**: The controlling algorithm for the bidirectional DC-DC converters is implemented on the C2000 microcontrollers. The controllers are responsible to adjust and provide the PWM signals to the drivers of the MOSFETS. The voltage and current sensors, implemented in the system, provide feedback to the controller through the available ADC channels. Based on the information delivered by the power management controller STM32F072, on the I2C line, the C2000 controller becomes “aware” of the reference voltage and current limitations of the sink device. Indication LEDS are used and driven by the C2000 GPIOs, to demonstrate the status of the system.
2. **DC-DC bidirectional converter**: A four quadrant bidirectional converter as stated in section 0 has been implemented to allow bidirectional power flow. Fours MOSFET’s are used to switch different parts of the circuit. The controlling signals are produced by the C2000 microcontrollers. Voltage and current measurement sensors have been implemented in the converter circuitry to allow regulation of the voltage and current levels of the input and the output.
3. **STM32F052 Microcontroller**: The port control is implemented by the STM32F052 microcontroller. This controller is responsible to resolve the port role (UFP, DFP, and DRP) as well as provide information regarding the voltage and current limitations of the end-device. In case of an active cable, the STM32F052 is enabling the 5V supply and supports the VCONN operation. The STM32F052 is responsible for the device policy management, policy engine, protocol and physical layer as stated in section 0

4. **STM32F072 Microcontroller**: The power management of the system is implemented by the STM32F072 microcontroller. The STM32F072 has a VBUS detection pin which provides power information of the source and sink connected to the system. In collaboration with the information given by the STM32F052 the power delivery contract can be accomplished and the power exchange can be initialized between the source and the sink. The STM32F072 acts as the System Policy manager as stated in section 0.
5. **USB-Type C interface:** The USB-Type C interface is used as a connection port between the source and the sink. The hardware board is equipped with two type-C ports, which can support different power levels at the same time. The advantage of the Type-C port is that it offers the flexibility to a device to swap from being a sink to become a source and vice versa, at any moment. The Type-C interface supports high power transfer up to 100W.
6. **20 Pin Header:** A twenty pin header is used to provide serial communication of the application board with other boards using I2C communication. The pin header provides external power of 5VDC and 12VDC.
7. **I2C communication line:** Every microcontroller has a specified address. Thus, a common I2C line is used where all the data are transferred and the microcontrollers can exchange information.
8. **External Power Supplies:** An external 12VDC supply, provided by the pin header is powering the auxiliary power converters used to deliver 3.3VDC, 5VDC and 12VDC to the hardware circuitry.
9. **Power Connectors:** The board is equipped with power connectors. For every DC-DC converter there is an input and an output connector.

Hardware Design & Component Selection

The functional block diagram of Figure 58 shows the first step of the hardware design. After specifying the requirements of the application, the initial focus turned on the designing of the DC-DC bidirectional converter. In the search for an optimal solution which would provide high efficiency and system quality, a reference design of Texas Instruments was found which was covering fully the specifications of the application [32]. The calculations made in section 0 matched the characteristics of the reference design. The topology comprises of a four switch synchronous buck-boost converter with a maximum power rating of 300W. The converter parameters are shown in Table 6.

Table 6. DC-DC bidirectional converter parameters

Characteristics	Rating
Input Voltage	10-100V DC max
Input Current	0-8A max
Input Power	<300W
Output Voltage	5-100V DC max
Output Current	0-8A max
Power Rating MAX	300 W
Switching Frequency (Fsw)	250KHz

The basic component selection is presented in the following Table 7.

Table 7. DC-DC bidirectional converter basic components [32]

Component	Name	Characteristics	Manufacturer
MOSFETS	IRF6644 DirectFET	100V , 60A, 10.3mΩ	INFINEON
MOSFET Drivers	UCC27211DDA High Side, Low Side Driver	8V-17V Supply, 4A Out, 18ns Delay, SOIC-8	TEXAS INSTRUMENTS
POWER Inductor	HA55L-3623400LF	40uH, 26A , 5.7mΩ	TT Electronics
Filter In/Out Capacitors	SMD Multilayer Ceramic Capacitor	2.2 µF, 100 V, ± 10%, X7R	AVX
Voltage Measurement Sensor	TLV2371IDBVT	3 MHz, 2 V/µs, 2.7V to 16V	TEXAS INSTRUMENTS
Current Measurement Sensor	OPA340NA/250	5.5 MHz, 6 V/µs, 2.7V to 5V	TEXAS INSTRUMENTS
Voltage Reference	REF3318AIDBZT	1.8V	TEXAS INSTRUMENTS
MCU	TMS320F28035PNT	32bit, 60 MHz, 128 KB, 20 KB, 80 Pins	TEXAS INSTRUMENTS

For the controlling of the converter, the microcontroller Piccolo C2000 TMS320F28035PNT from Texas Instruments was selected, since its functions covered fully the application needs. The microcontroller can support up to four pairs of complementary high resolution PWM signals and multiple ADC and GPIO channels. Furthermore, the toolbox provided by Simulink-MATLAB for the programming of the C2000 series, made the selection of this microcontroller more attractive since the embedded programming fluency was not required.

The USB Type-C interface was designed based on the reference design of Google on the Chromium Projects [33]. Several adjustments were made on the design to meet the requirements of the thesis application. Two microcontrollers, the STM32F052 and the STM32F072, were used to run the system device policy and device policy manager. Each microcontroller runs a firmware which is provided by the repository of Google Git [34]. The provided software included only a single power profile, thus extra profiles were created based on the unpublished report by “Shruthi Kashyap” [35]. In Table 8, the characteristics of the two microcontrollers which implement the USB-Type-C interface are given.

Table 8. USB-TYPE C MCU interface

Component	Name	Characteristics	Manufacturer
ARM Microcontroller	STM32F051C8T6	STM32 F0 ARM Cortex-M0 Microcontrollers, 32bit, 48 MHz, 64 KB	STMICROELECTRONICS
ARM Microcontroller	STM32F072RBT6	STM32 F0 ARM Cortex-M0 Microcontrollers, 32bit, 48 MHz, 128 KB	STMICROELECTRONICS

On the application board, two USB Type-C ports were placed in order to provide or acquire power from two different end-devices. Each of the DC-DC converters, is dedicated to only one port thus, the flexibility of different power profiles in each port is ensured. The USB-C connector that was used is listed in Table 9.

Table 9. USB Type-C connector

Component	Name	Characteristics	Manufacturer
USB Connector	DX07S024JJ2R1300	USB 3.1 Gen 2, Current Rating 5 A, Voltage Rating 20 V	JAE Electronics

For the powering of all the power components, external power supply of 12V DC is used. Three different voltage levels 3.3V DC, 5V DC and 12V DC are required for the operation of the ICs used in the application board. For this purpose, two integrated DC-DC isolated converters were used and a 3.3V LDO regulator. The isolated converters were used to protect the application board from possible faults occurring in the power supply side. In Table 10, the auxiliary power supplies are presented.

Table 10 Auxiliary Power Supplies

Component	Name	Characteristics	Manufacturer
Fixed LDO Voltage Regulator	TLV1117-33CDCYR	4.7V to 15V, 1.2V Dropout, 3.3Vout, 800mAout	TEXAS INSTRUMENTS
Isolated Board Mount DC/DC Converter	MEV3S1212SC	3kV Isolation 12 V, 250 mA, 3W	MURATA POWER SOLUTIONS
Isolated Board Mount DC/DC Converter	MEV3S1205SC	3kV Isolation 3 W, 5 V, 600 mA	MURATA POWER SOLUTIONS

In order to be able to program all the microcontrollers, four mini JTAG connectors have been used. Each connector is dedicated to a single microcontroller. Every mini JTAG connector has a 3.3V DC supply, a ground pin, a reset pin and two serial connection pins TMS and TCK. In Figure 59, the schematic design of the mini JTAG connector is presented. In Table 11, the characteristics of the connector are given.

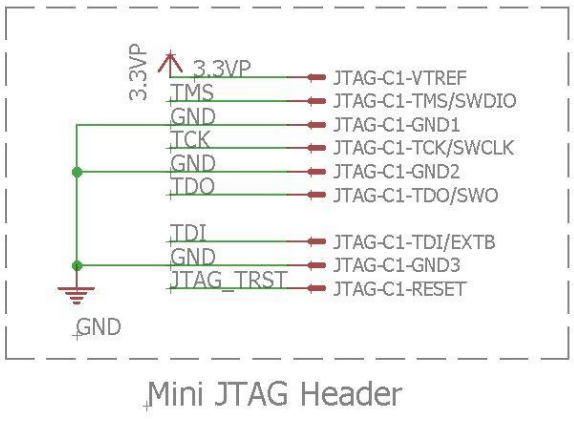


Figure 59. Mini JTAG connector

Table 11. Mini JTAG header

Component	Name	Characteristics	Manufacturer
Mini JTAG header	FTSH-105-01-L-DV	1.27 mm, 10 Contacts	SAMTEC

Design Options

Since the application board was developed for educational purposes, the design has some enhancements in order to make the board more flexible and provide the chance to other students to be able to use it for their research. For instance, the use of two separate C2000 microcontrollers for the controlling of the DC-DC converters, could be accomplished by the use of just one microcontroller, since it provides enough PWM signals to control two four-quadrant bidirectional converters. Though, the idea during developing was to have two completely separate systems as a backup option in case there was some error or failure in one of the two systems.

The USB Type-C interface could be combined in one microcontroller which implements both the system policy management and the device policy manager. Though, the existence of two separate microcontrollers provides more flexibility for further research on the communication protocols.

The schematics and PCB designing were conducted using the EAGLE 7.6.0 software and can be found in Appendix . For the PCB design, four layers were used. One layer was a dedicated ground layer which provides the following advantages:

- A low ohm connection for all ground points with low noise and small potential differences between the ground and the connected components
- Minimize the current loops
- Assists in the development of an electromagnetic compatible design which has low radiated emission and high immunity to external noise.
- A uniform impedance, which minimizes the noise and reflections of high frequency signals.

A second layer was dedicated to 3.3V DC, making the connection of supply to the components easier, minimizing the routing traces and avoiding current loops. Two more layers were necessary for the routing of the components.

One isolation zone was used to correctly place the DC-DC isolated converters, as well as the serial communication lines (with other boards) coming from the twenty pin header. Multiple polygons were designed on the PCB especially on the converters location in order to provide a uniform trace plate for high power transfer. Following PCB design guidelines [36], the width and thickness of the traces and vias was calculated. All the traces were calculated for a maximum temperature increase of 50°C when the maximum power (300W) is transferred. No heat sinks were necessary for this design. The programming of the controllers is done through a mini JTAG interface. A USB to JTAG interface designed by previous students was used.

In Figure 60, the final layout of the PCB design is presented. In Figure 61 the main blocks are shown on the PCB layout.

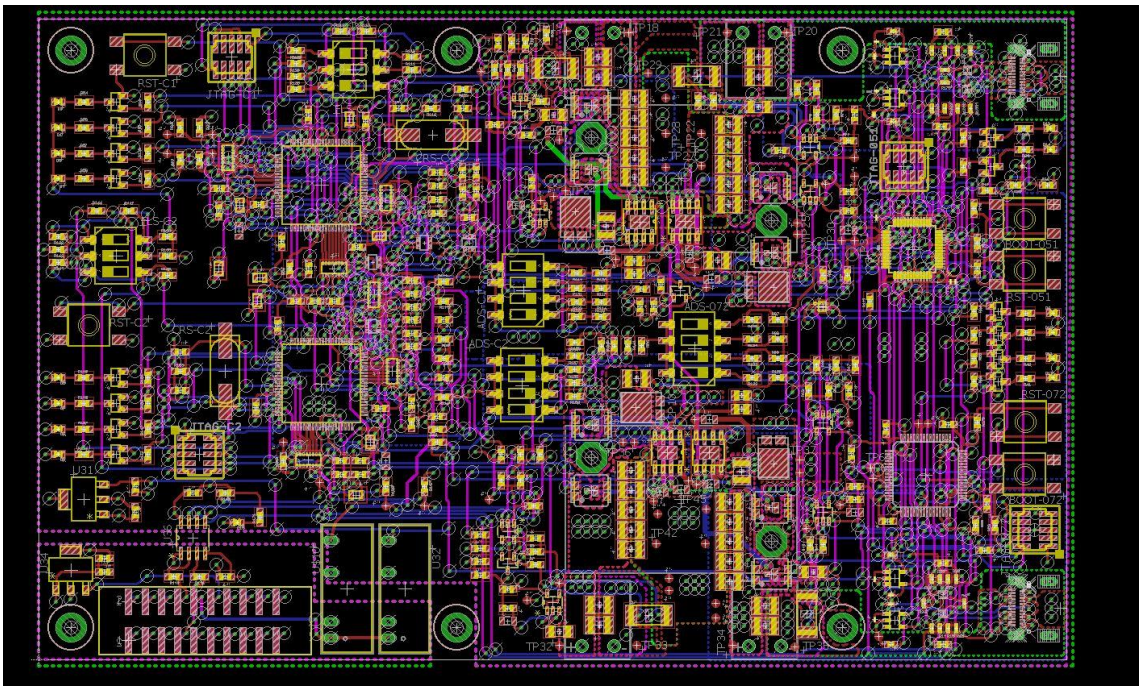


Figure 60. PCB design

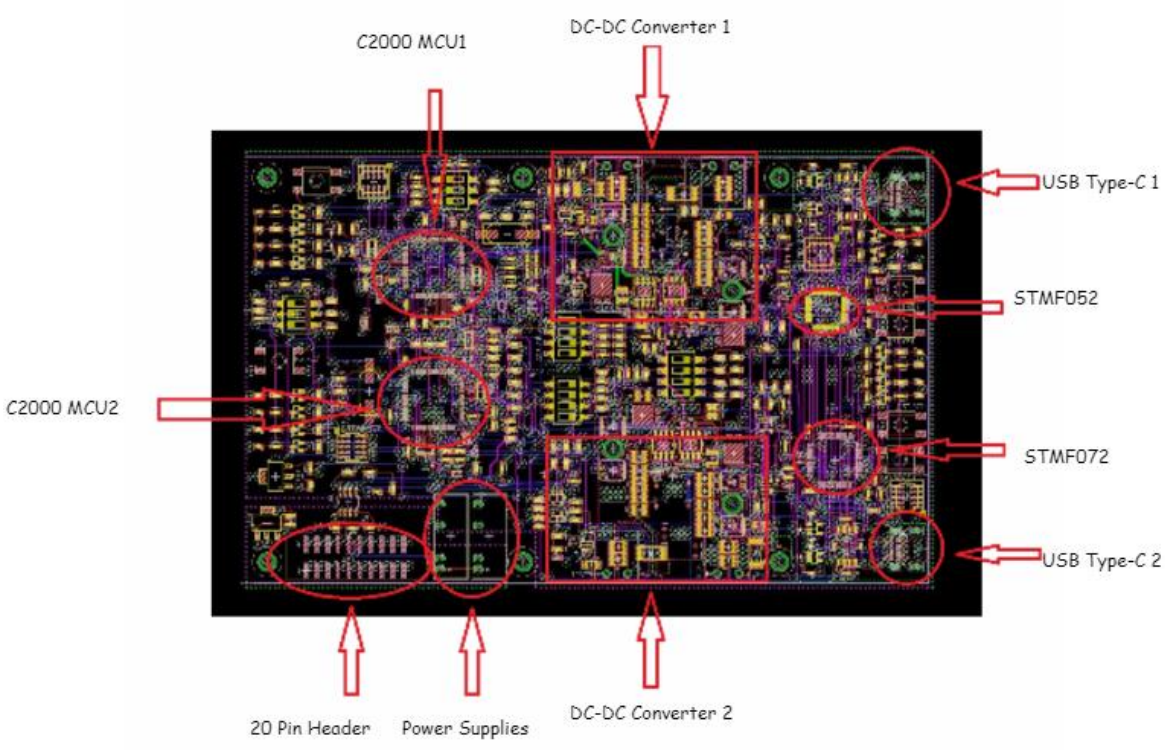


Figure 61. PCB Layout Main Blocks

Application Description

As previously explained in the introduction chapter, the goal of this thesis is the development of an integrated solution which would support bidirectional power flow between smart devices and the DC link of a smart building, using the USB-type C interface. A description is detailed below, in order to clearly understand how the integrated hardware solution is operating:

1. It is assumed that the inputs of the DC-DC converters are always connected to the low voltage DC link of the building. Based on the system requirements, the input of the DC link can vary between 10-100V DC.
2. The user attaches the smart-device (laptop, smartphone, tablet) using a USB-C cable to the USB-Type-C interface of the application. The type-C female ports of the application board are configured as DRP ports. Assuming that all smart-devices have also DRP ports, meaning that they can act both as host or sinks, the port role configuration is beginning.
3. Since the main role of the end-device is to act as sink (UFP ports) which needs to be charged by the grid, the configuration starts by setting the DRP port of the end-device as a UFP port. Once the USB-C interface "decides" that the source is providing enough power to charge the end-device, a power contract negotiation starts. As soon as the power contract has been negotiated, a communication starts through the I2C line with the controller of the DC-DC converter.
4. The USB-C interface transmits information through the I2C line regarding the reference voltage and current limitation of the end-device.
5. The controller of the DC-DC converter resolves the power flow direction and sets the limits for the output voltage and maximum output current. Thus, power starts flowing from the grid to the end-device.
6. The USB-C interface is responsible to set new limits of voltage and current levels while the charging of the end-device is progressing.
7. In the unlikely case of a source failure (input source of the grid has failed), the scenario of using the Li-ion batteries of the end-devices as a backup solution is realized.
8. The port role configuration starts again, but this time the type-C port of the application board cannot be set as source (DFP), since the $VBUS$ measurement notifies about the lack of voltage at the source side.
9. Since the end-device has the ability to provide power, the port configuration swaps. This time, the end-device port is set as a source (DFP) and the application board port is set as a sink (UFP).
10. This information is transmitted through the I2C line to the controller of the DC-DC converter, which in turn, swaps the power flow direction and regulates the output voltage (to the grid) as well as limiting the input current (discharge protection of the end-device).
11. Through periodical measurement of the voltage levels of the grid, after isolating the $VBUS$ net, the restoration of the power at the grid side can be detected. The port role configuration can be negotiated again which leads to the restoration of the power flow direction (considered as default from the grid to the end-device).

In Figure 62 the fully assembled application board is presented.

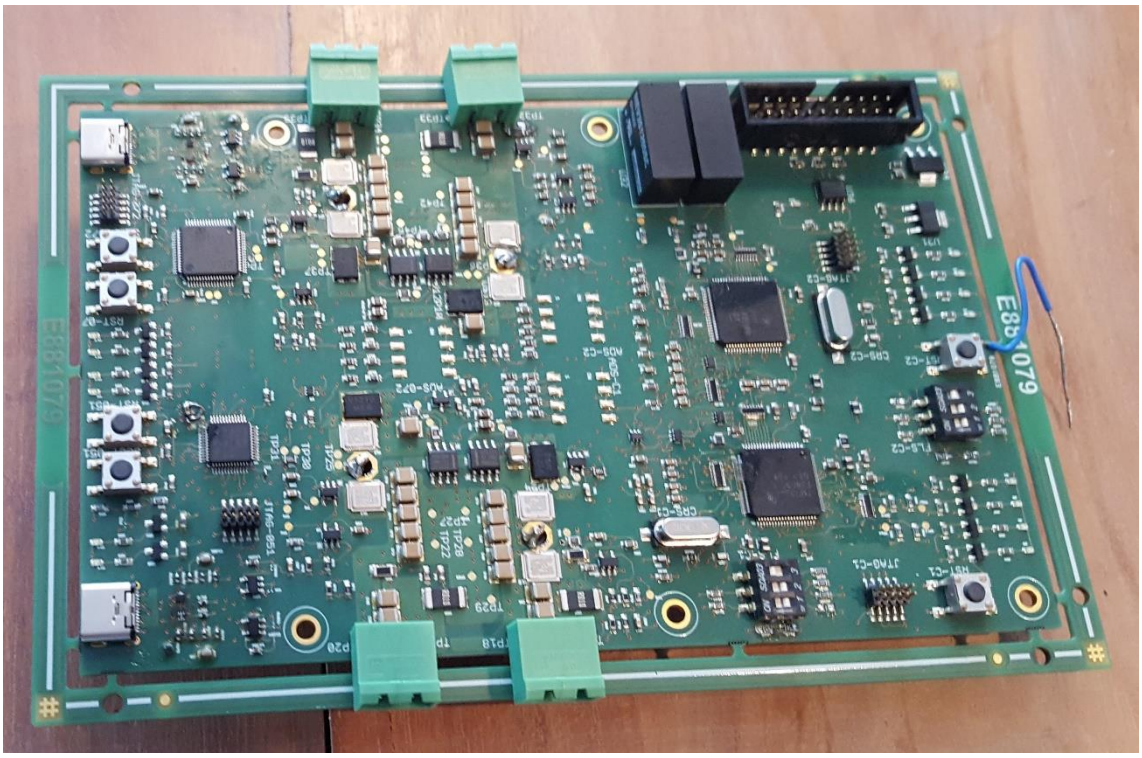


Figure 62. Application Board

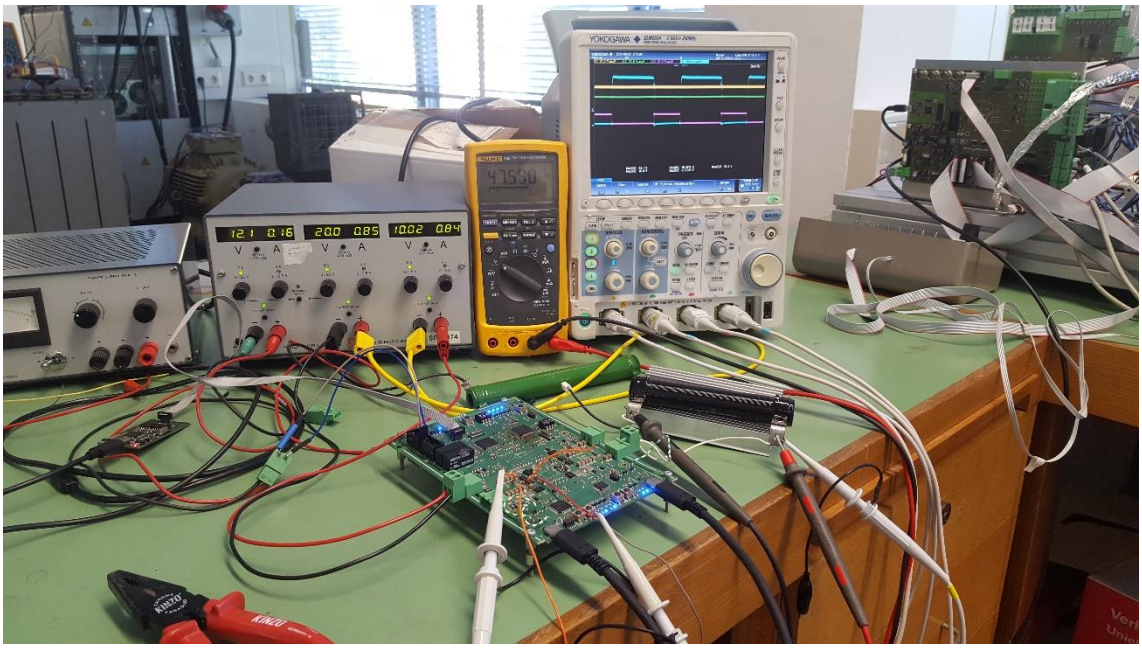


Figure 63. Application Board Testing

RESULTS

In this chapter, the results that emerged from testing the hardware development will be presented and explained in detail. In order to qualify the hardware, some experimental setups were made and tests were conducted to verify that the results were following the simulated system. As already mentioned in section 0, some basic scenarios were created and tested during simulations. Similar scenarios were made to test the real application board. Based on the application use, the basic output voltages that the board should provide to the USB type-C interface are 5VDC, 12VDC, 20VDC. An extra test profile was created to realize the case where 48VDC would be used to power high voltage end-devices, which would use the USB type-C interface.

In order to test the different scenarios, lab equipment was used. The necessary equipment is presented in Table 12.

Table 12. Test equipment

Component	Name	Characteristics	Manufacturer
DC Power Supply	EST 150	2x 0-20 V 0 -2.5 A 1x 0-10 V 0 - 5 A	DELTA ELEKTRONIKA
Multi-meter	FLUKE 189	-	FLUKE
Oscilloscope	Yokogawa DLM2034 Mixed Signal Oscilloscope	2.5Ghz/s 350MHz	YOKOGAWA

The scenarios presented in Table 13 were tested to realize the qualification of the application board. For safety reasons, since a non-certified controlling method was used to regulate the charging of a battery, which could lead in unsafe charging circumstances, it was chosen to test the experimental scenarios with the safe option of a resistive load of 100Ω.

Experimental Scenarios

Table 13. Experimentally tested scenarios

Scenario	Mode	DC Link (Voltage)	End-Device (Operating Voltage)	End Device (Max Current)
1St Case			***Smartphone***	
	Buck	15 V	5 V	1 A
	Buck	20 V	5 V	1 A
	Buck – Boost	5 V	5 V	1 A
	Boost	3.3 V	5 V	1 A
2nd Case			***Tablet***	
	Boost	7 V	12 V	1 A
	Boost	8.6 V	12 V	1 A
	Buck – Boost	11.8 V	12 V	1 A
	Buck	17.1 V	12 V	1 A

	Boost	$20.4\,V$	$12\,V$	$1\,A$
3^{rd} Case			***Laptop***	
	Boost	$9.06\,V$	$20\,V$	$5\,A$
	Buck − Boost	$20.4\,V$	$20\,V$	$5\,A$
	Buck	$29.46\,V$	$20\,V$	$5\,A$
4^{th} Case			***High Voltage End − Device***	
	Boost	$12\,V$	$48\,V$	–
	Buck − Boost	48	$48V$	–
	Buck	$60\,V$	$48\,V$	–

5V End-Device

The results that occurred from the first scenario are presented in the following figures. In order to ensure that a smooth transition is occurring through the swap between the different modes (buck, boost and buck boost), several pictures were taken to understand the transition phase. In Figure 64, the case that the DC link is providing a constant DC voltage of 15V is shown. After the end-device has negotiated a power contract through the USB-Type C, 5V with maximum 1A has been requested. The C2000 microcontroller has received this information and has started regulating the output to 5V with maximum allowed current of 1A.

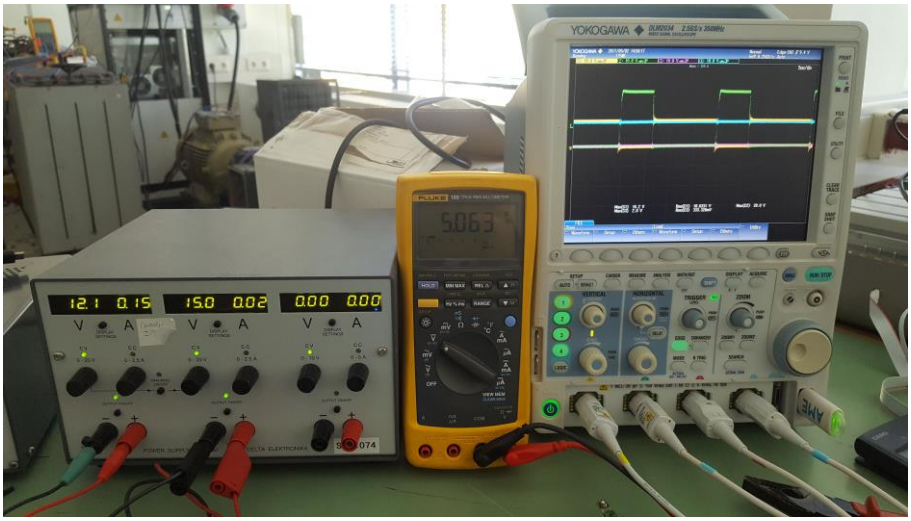
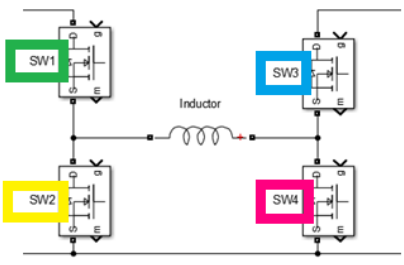


Figure 64. 15VDC link- 5V output to end-device.

Taking a closer look at the MOSFET's of the converter, the switching scheme is visible in Figure 65. The colors correspond to the switches as per the following:

Table 14. Switching Pulses vs Colors

Switches	Color
SW1	Green
SW2	Yellow
SW3	Light-Blue
SW4	Red



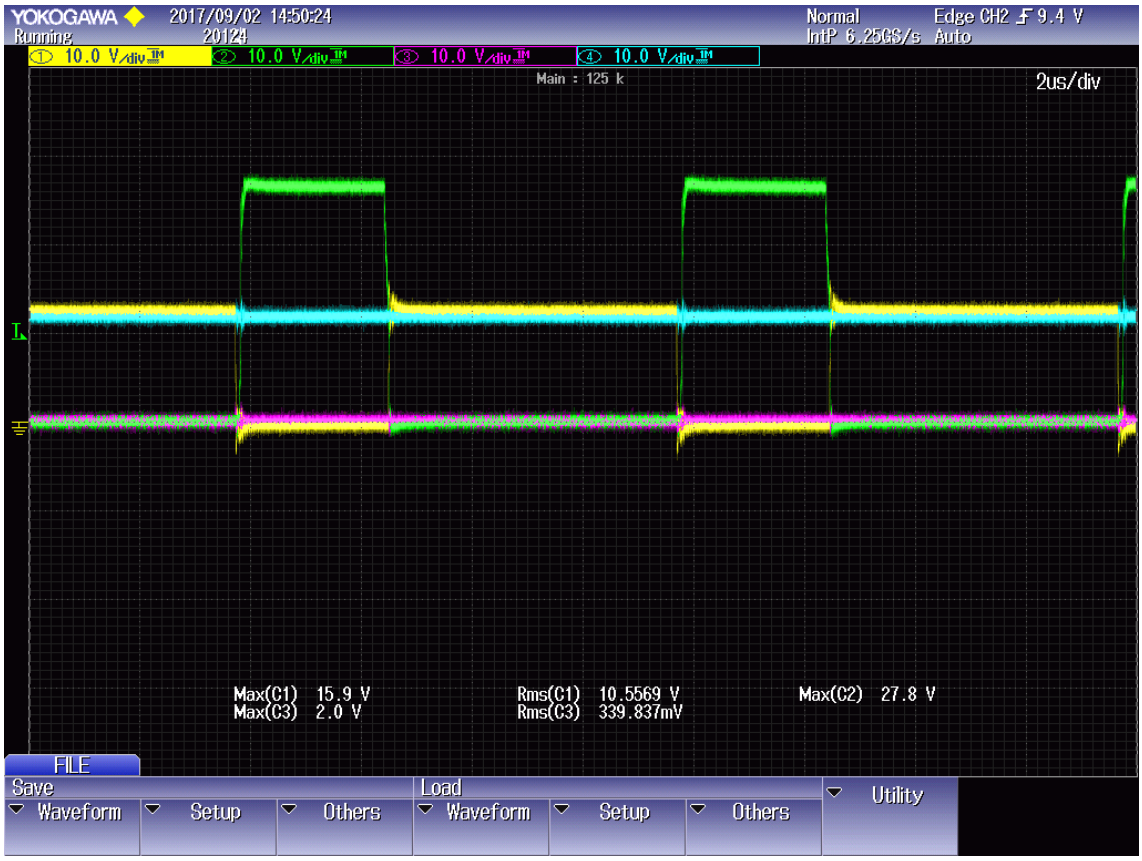


Figure 65. 15VDC link- 5V output switching scheme

In order to check the response of the control, it is assumed that the DC link voltage is suddenly changing from 15V to 20V. As can be seen in Figure 66, the response of the control is immediate and the output of the converter is regulated at 5V.

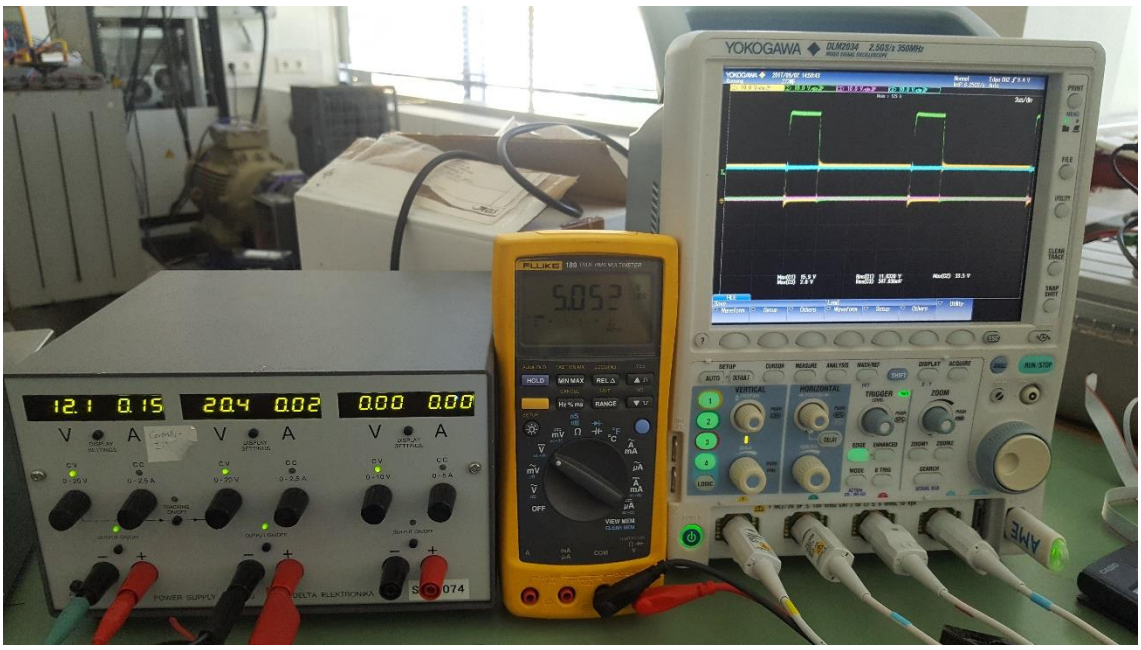


Figure 66. 20VDC link- 5V output to end-device.

The switching scheme of the switches is presented in Figure 67. It is visible that the amplitude of the switching pulse of SW1 is increasing, since the input voltage has been increased.

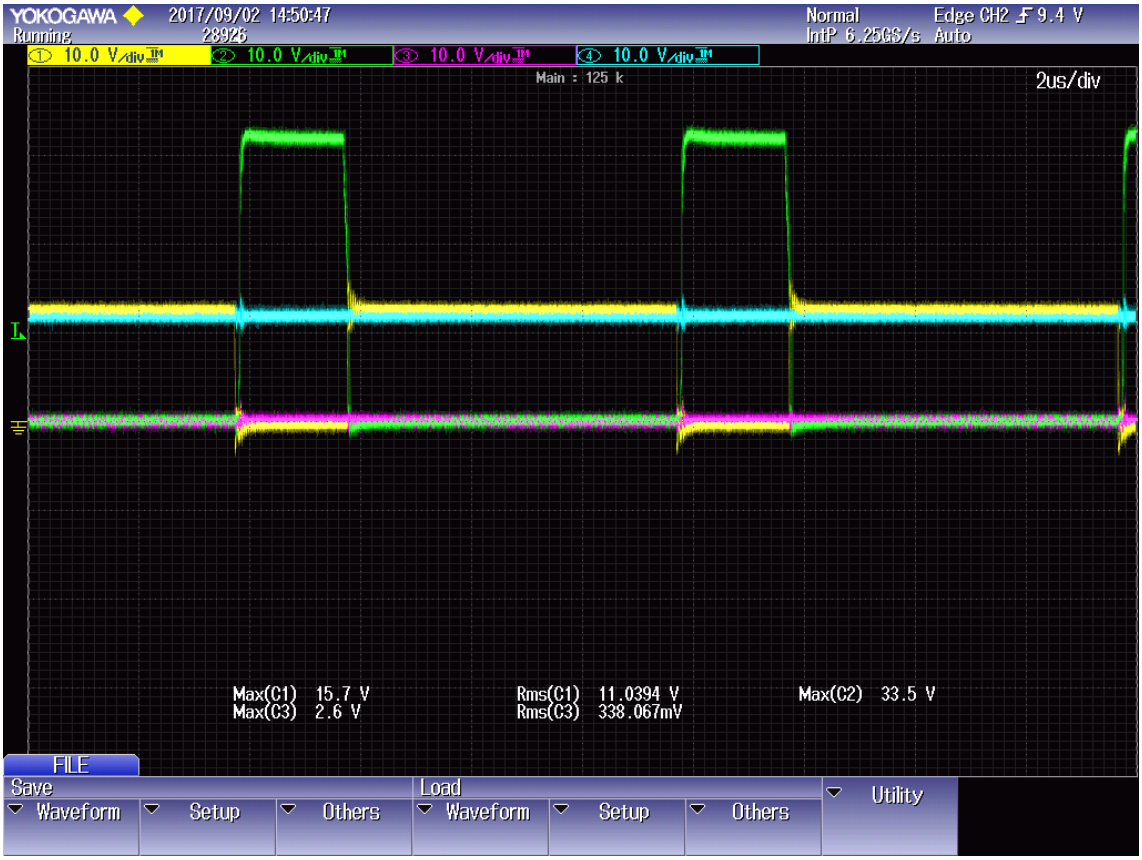


Figure 67. 20VDC link- 5V output switching scheme

Based on the first experimental scenario, in order to test the change of operational mode, from buck to buck-boost, it is assumed that the DC link voltage drops suddenly down to 5V. The controller is responsible to change the operational mode and the output of the converter must be maintained at 5V. In Figure 68, it is visible that the operational mode of the converter has changed. A closer look on the switching scheme shows the change of the pulses in Figure 69. 5VDC link- 5V output switching scheme.

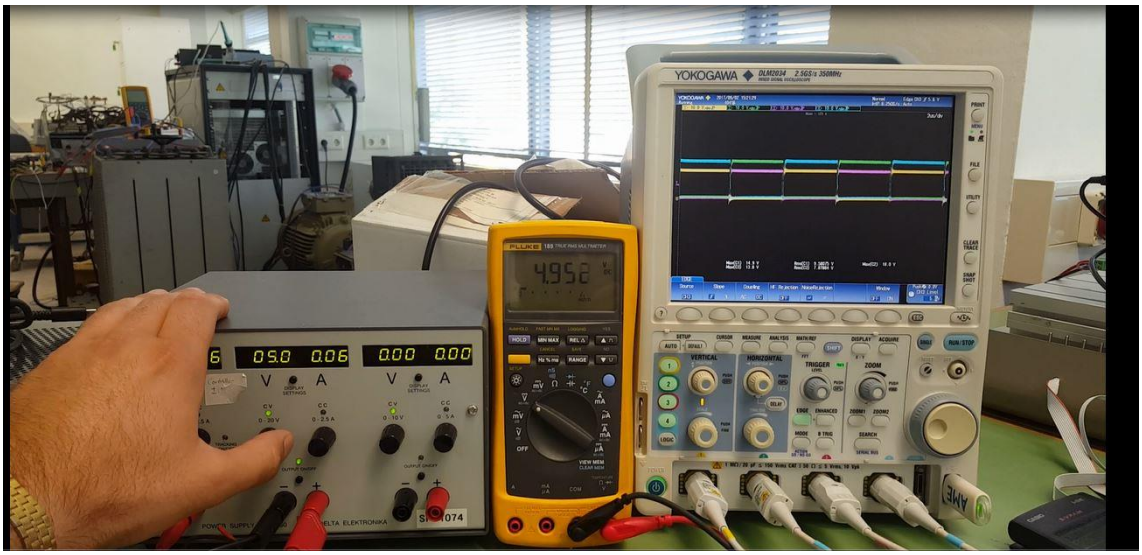


Figure 68. 5VDC link- 5V output to end-device.

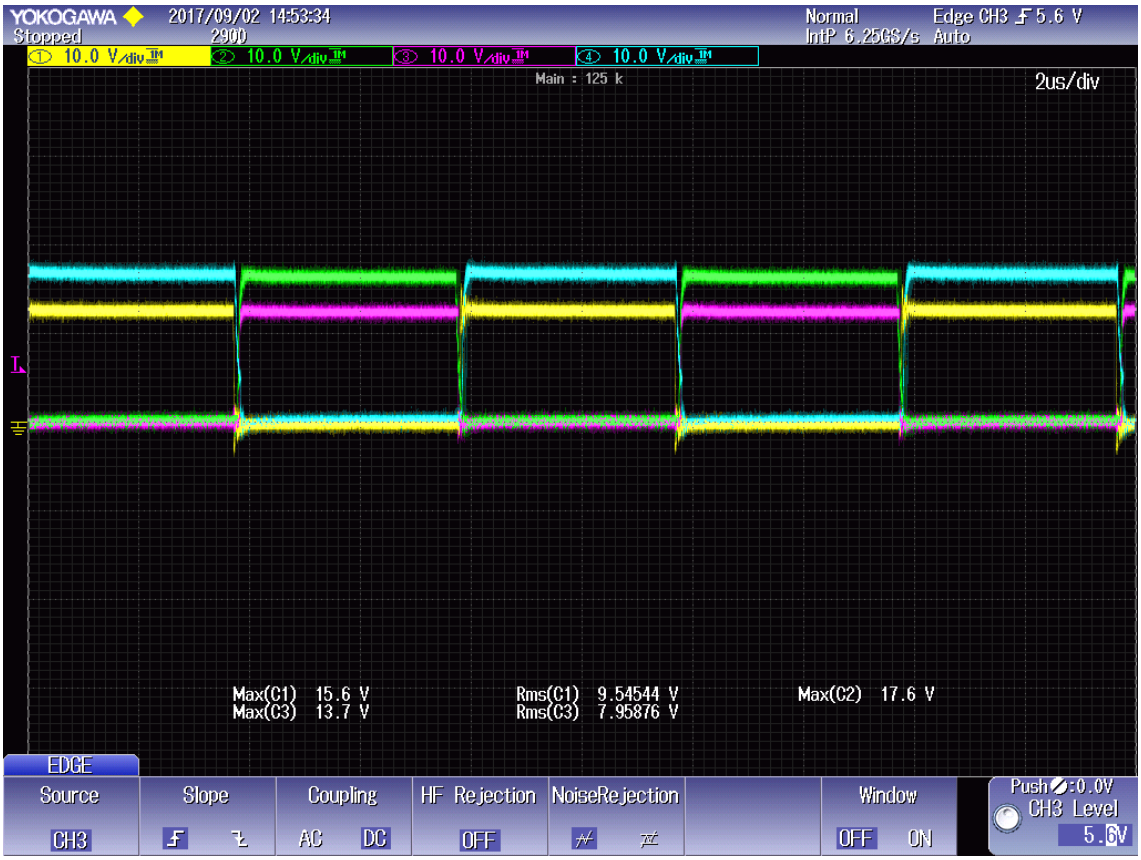


Figure 69. 5VDC link- 5V output switching scheme

In order to test the adjustment of the controller from buck-boost to boost mode, the DC link input voltage is assumed to drop further at 3.3V DC. The reaction of the controller is as expected and can be seen in Figure 70. The operational mode is changing to boost mode and the output remains regulated at 5V. The new switching scheme of boost mode is shown in Figure 71.

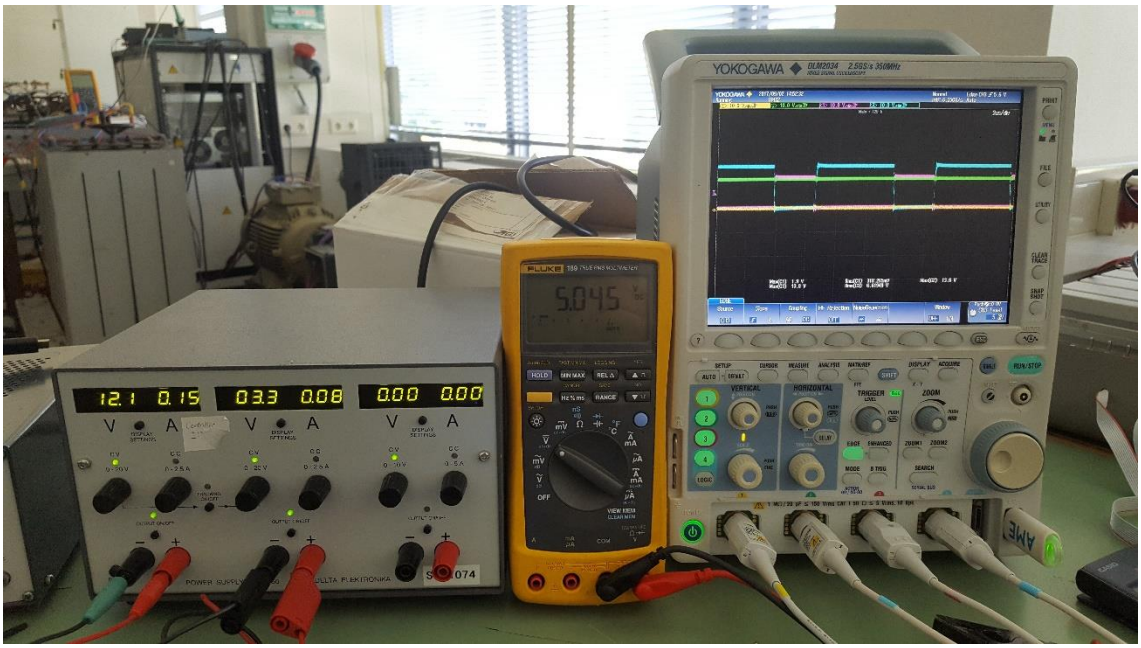


Figure 70. 3.3VDC link- 5V output to end-device.

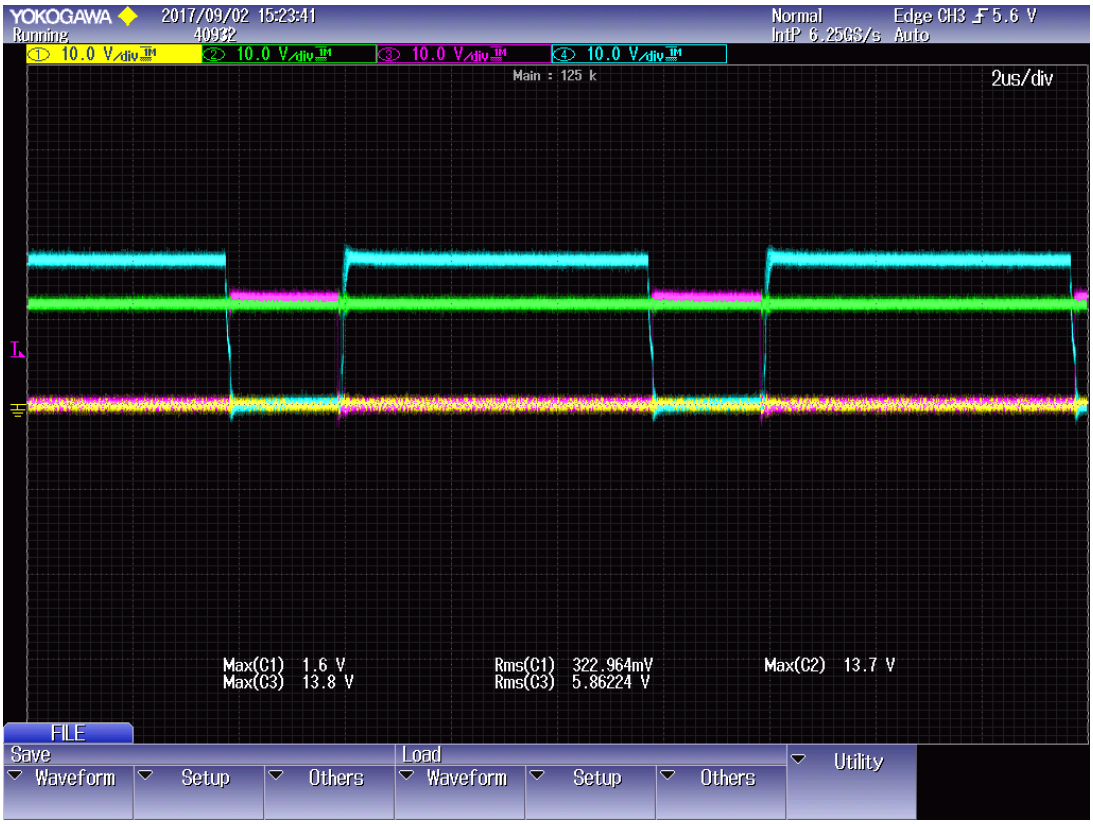


Figure 71. 3.3VDC link- 5V output switching scheme

12V End-Device

Following the second experimental case, it is assumed that a different end-device is plugged in the USB-type C interface which demands 12V at maximum 1A. After a power contract has been negotiated, the C2000 microcontroller is receiving the necessary information and starts regulating the output to 12V with maximum allowed current of 1A. The DC link presents 7V DC at the input of the converter thus, the microcontroller sets the operational mode to boost and the regulation at 12V is accomplished as shown in Figure 72.

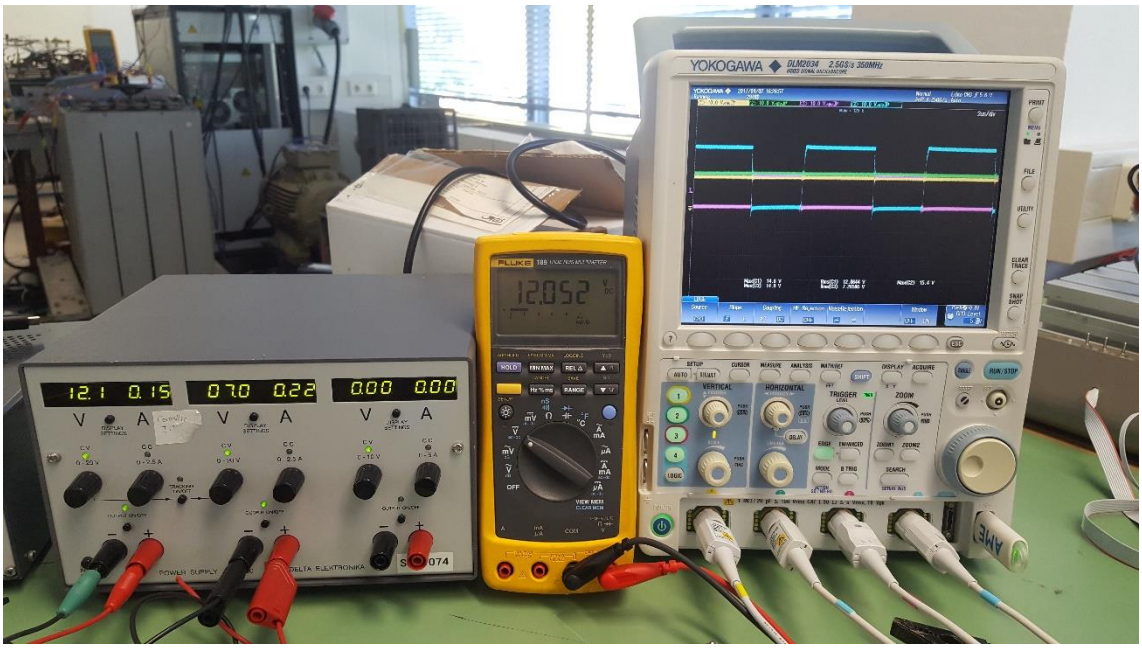


Figure 72. 7VDC link- 12V output to end-device.

A closer look on the switching scheme of the converter is presented in Figure 73.

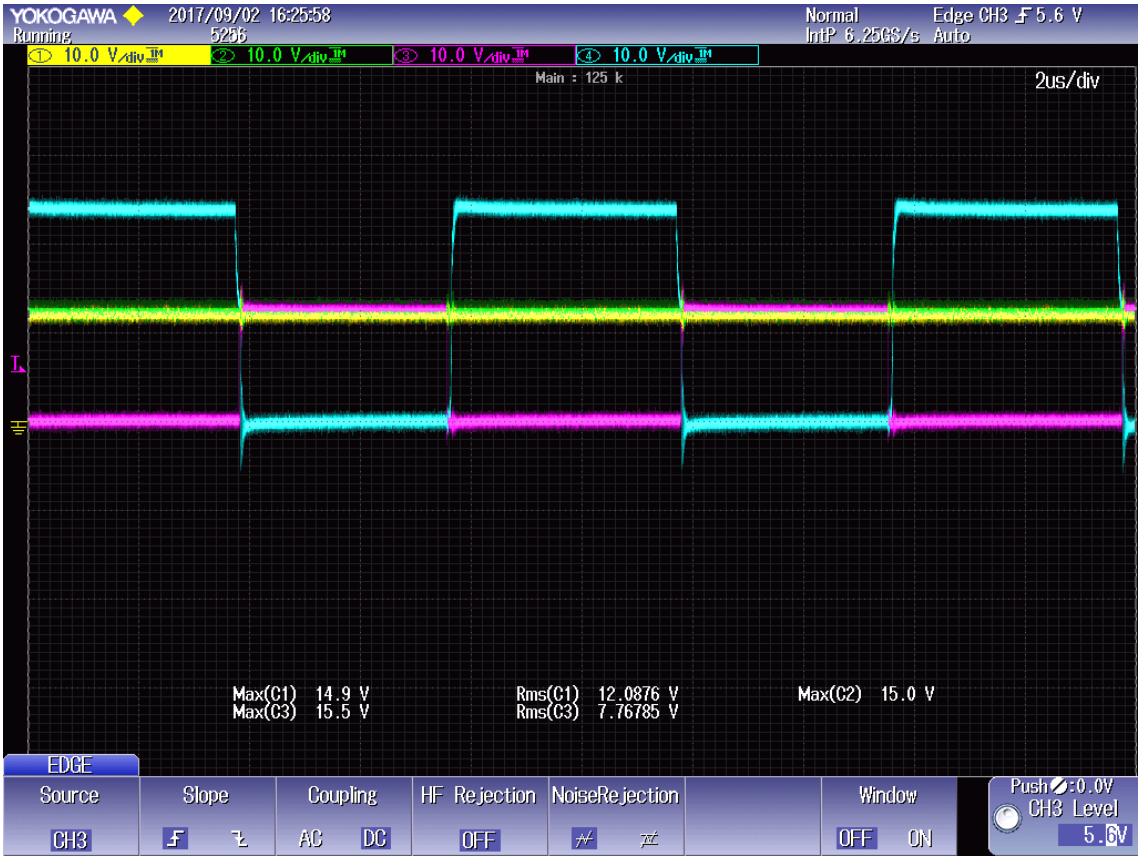


Figure 73. 7VDC link- 12V output switching scheme

In order to observe the response of the control, the DC link input is increased up to 8.6V. The output of the converter remains regulated at 12V DC as shown in Figure 74.

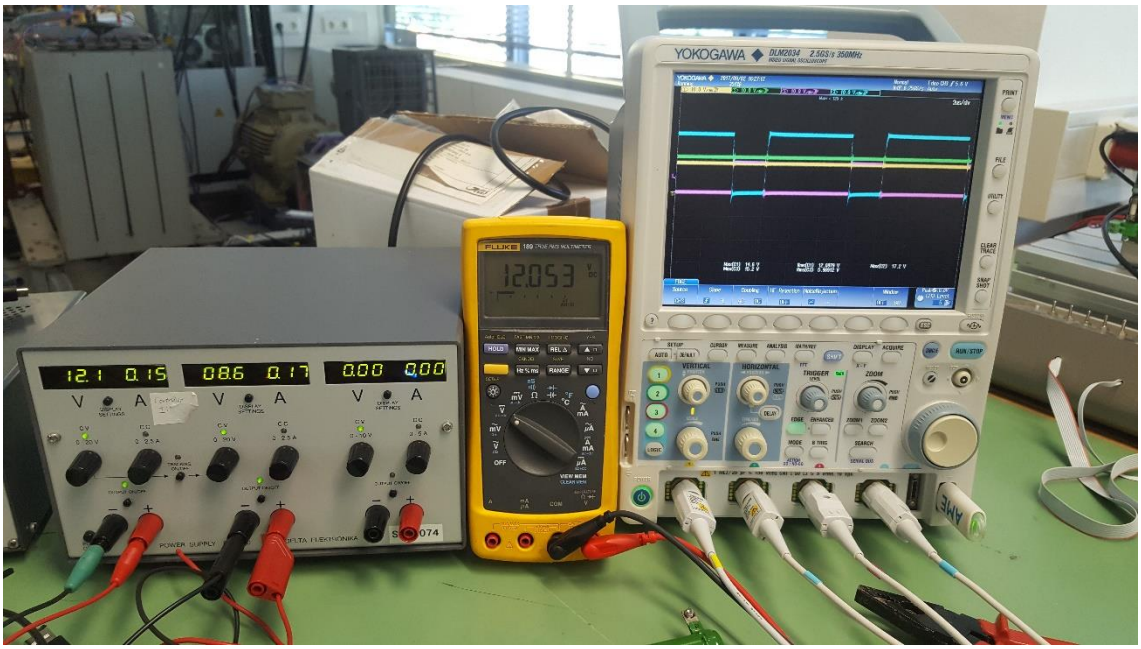


Figure 74. 8.6VDC link- 12V output to end-device.

Subsequently, it is assumed that the input voltage of the DC link is increased to 11.8V thus the controller needs to change the operational mode from boost to buck-boost in order to be

able to support the 12V output voltage. The response of the controller is as expected thus, the mode swap is presented in Figure 75.

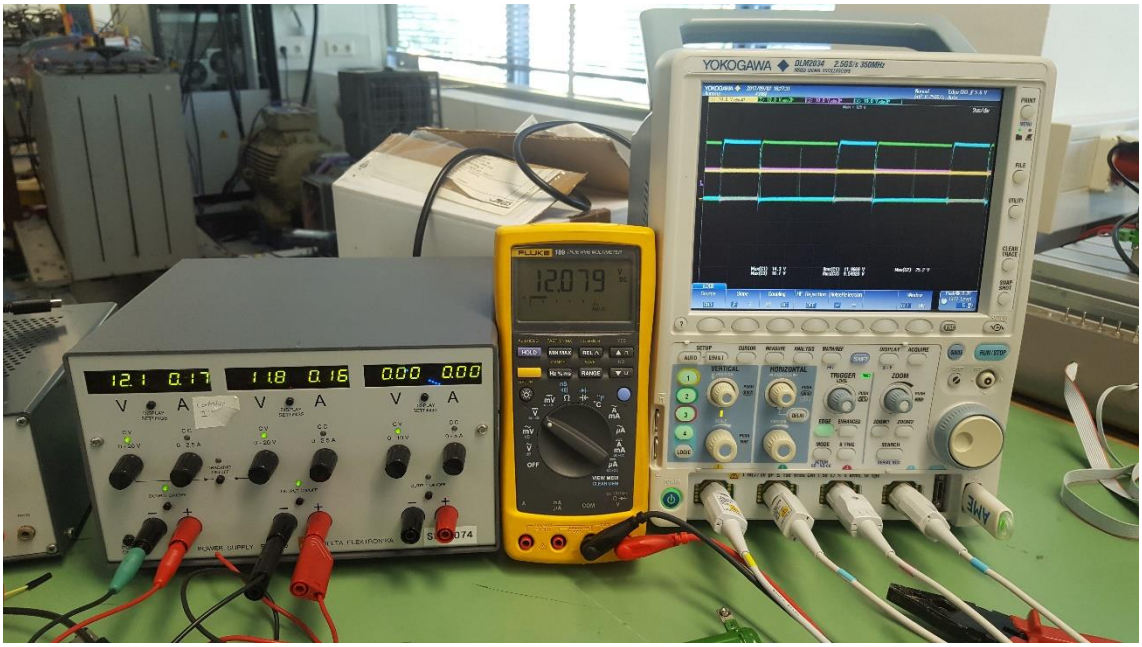


Figure 75. 11.8VDC link- 12V output to end-device.

The switching scheme of the MOSFET's is shown in Figure 76.

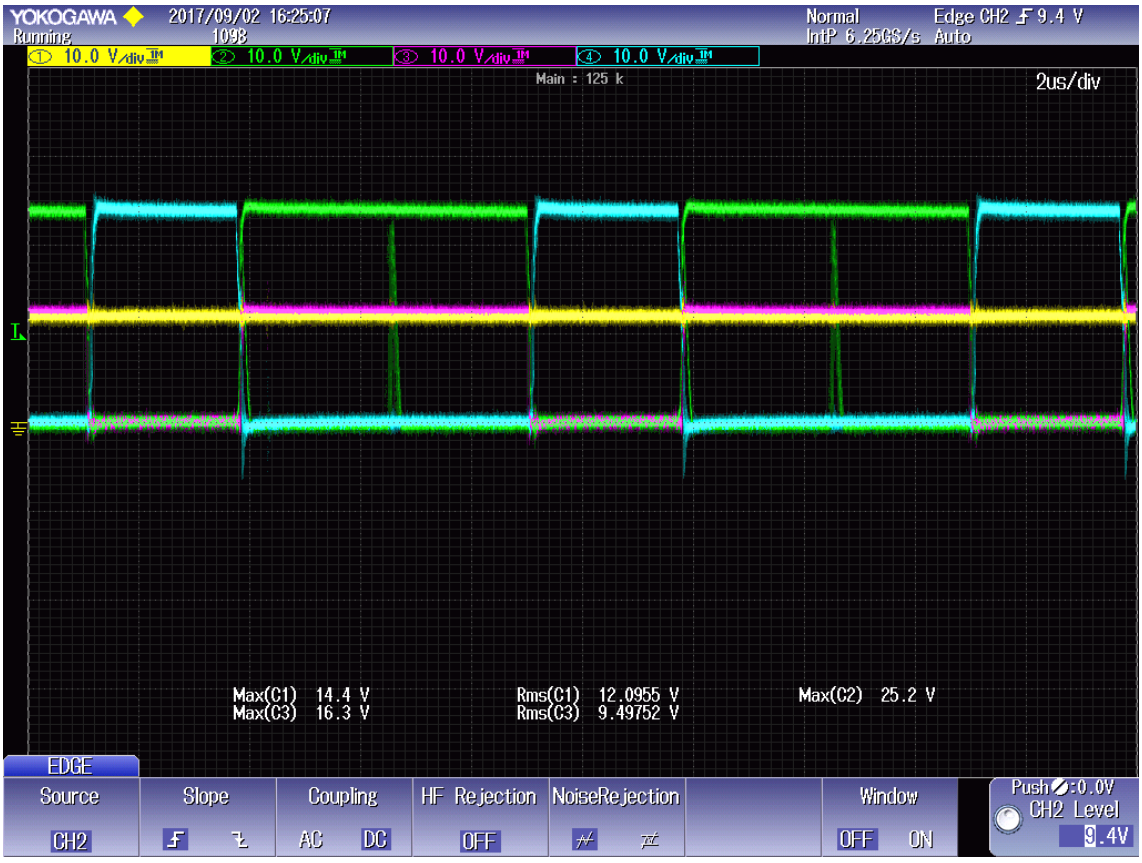


Figure 76. 11.8VDC link- 12V output switching scheme

The DC link voltage is suddenly increased to 17.1V thus the controller changes the operational mode from buck-boost to buck. The response is immediate and the controller regulates the output at 12 V as shown in Figure 77. A further increase at the input of the DC link

is realized to test the stability of the control. The input voltage is increased at 20.4V and the switching of the MOSFET's is adjusted directly as presented in Figure 78.

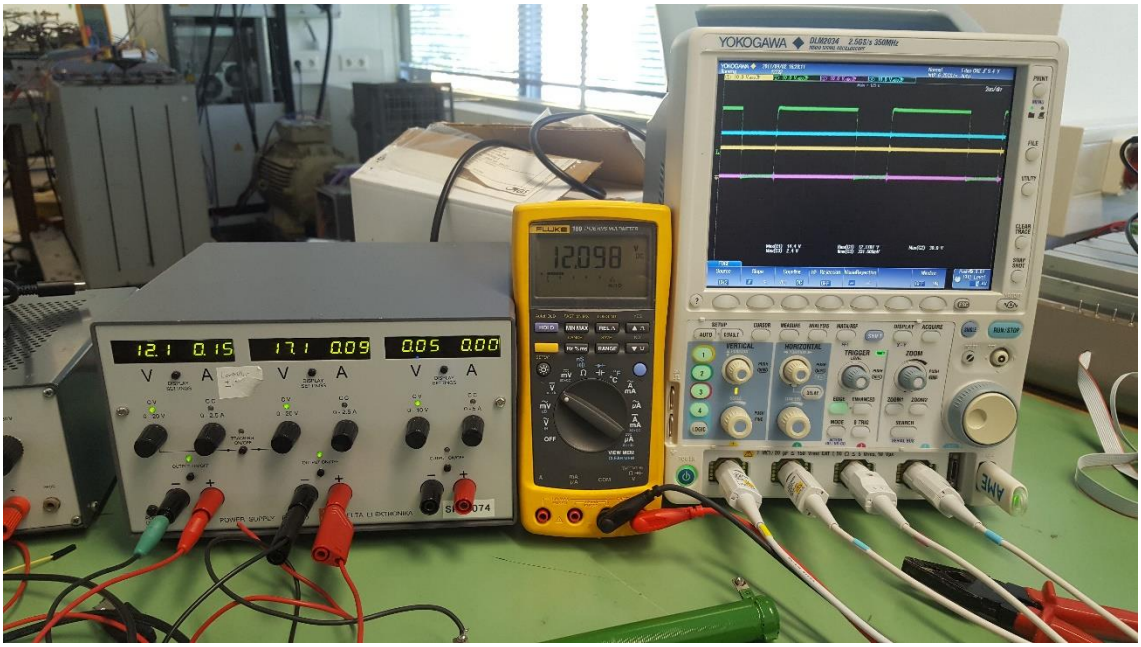


Figure 77. 17.1VDC link- 12V output to end-device

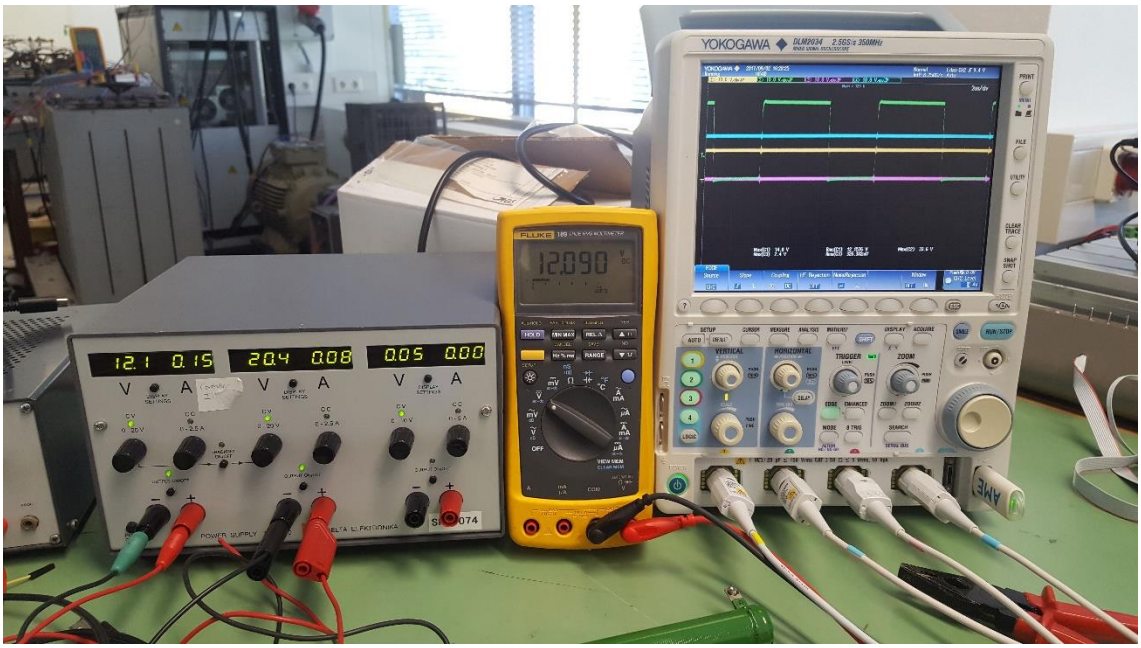


Figure 78. 20.4VDC link- 12V output to end-device

20V End-Device

The next step is the testing of the scenario where the end-device is requesting 20V at maximum 5A and the DC link provides 9V at the input of the converter. Following the power negotiation procedure, through the USB type C interface, as soon as a power contract has been established the controller of the converter regulates the output voltage and limits the maximum output current. The converter starts operating in boost mode and the results are presented in Figure 79. A closer look at the switching scheme is presented in Figure 80.

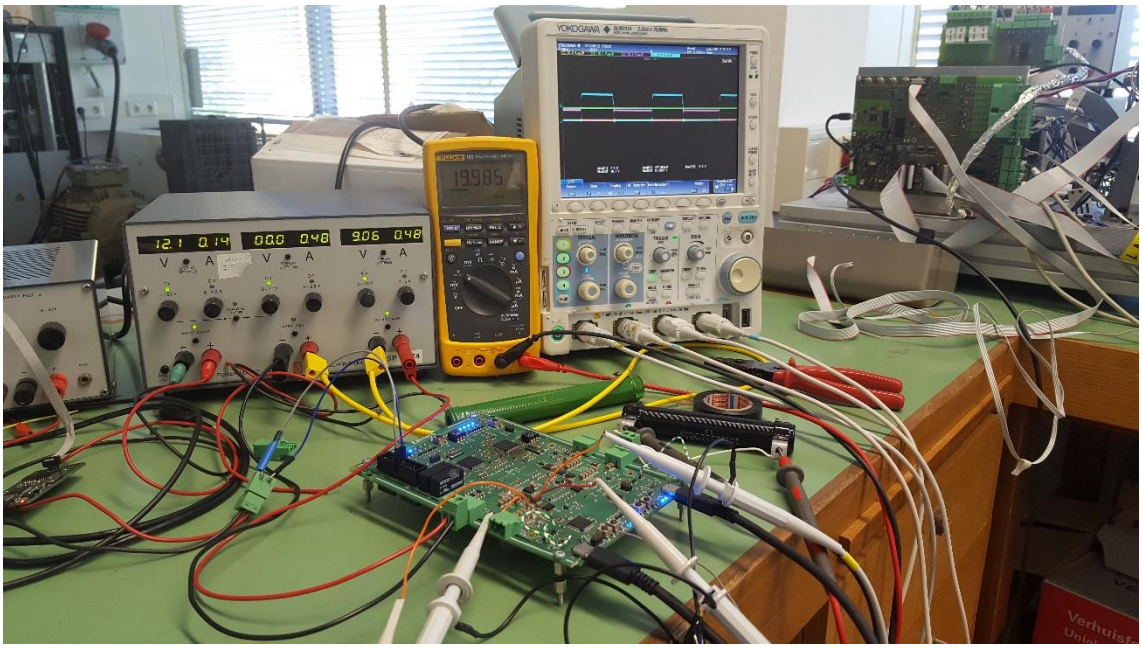


Figure 79. 9.06VDC link- 20V output to end-device

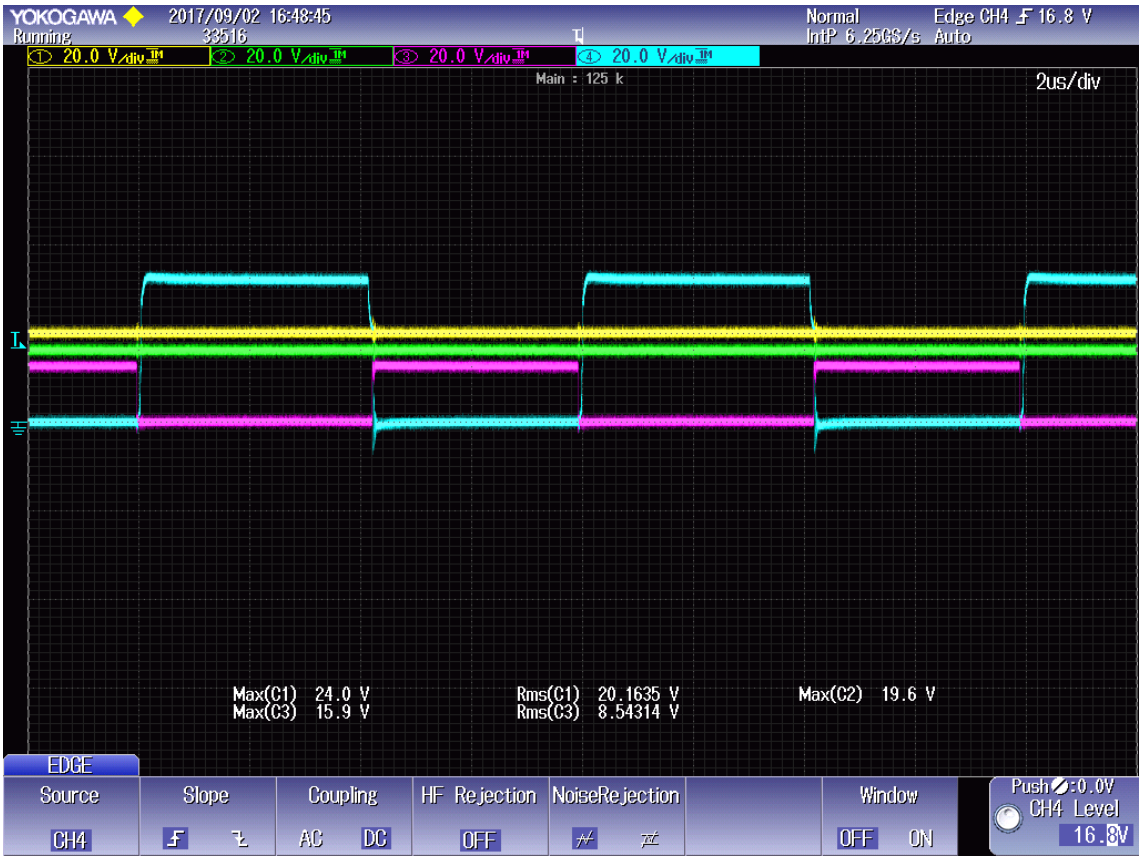


Figure 80. 9.06VDC link- 20V output switching scheme

The voltage of the DC link is increased at 20.4 V thus, the controller changes to buck-boost mode and the output is regulated to 20V as shown in Figure 81. Subsequently, a further increase in the input DC link voltage at 30V is occurring and the converter swaps to buck mode. Some ringing is presented in the SW3 due to the fact that the bootstrap capacitor of the MOSFET needs to discharge, therefore 100% duty cycle needs to be avoided. After multiple testing and investigation of the problem by giving different duty cycles close to 100% but less than 100%, it

was observed that instability was introduced at the output voltage. It was chosen to accept the existing ringing of the MOSFET. The results can be observed in Figure 82 and Figure 83.

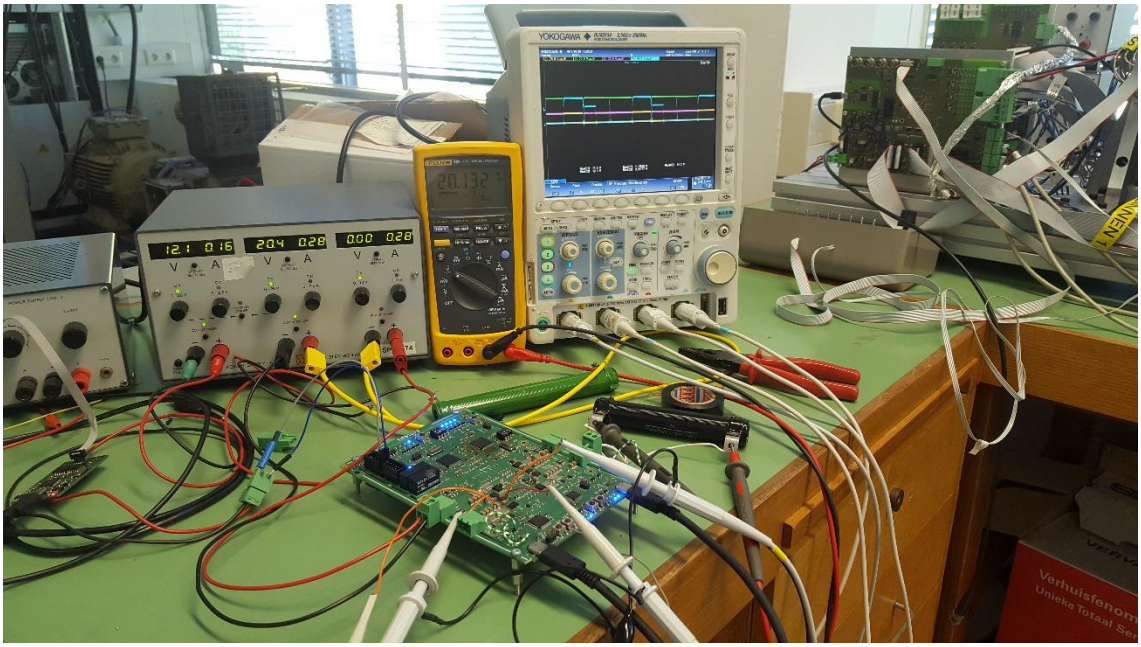


Figure 81. 20.4DC link- 20V output to end-device

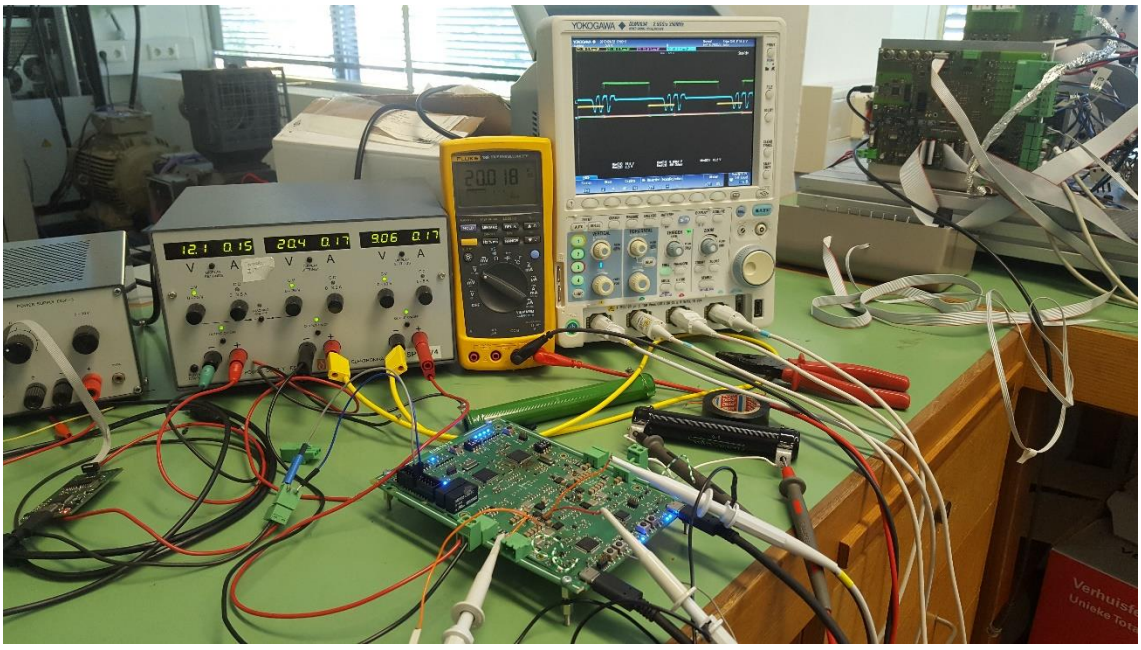


Figure 82. 30VDC link- 20V output to end-device

Figure 83. 30VDC link- 20V output switching scheme

48V End-Device

Based on the idea that high power devices using the USB type-C protocol might operate at a higher voltage of 48V DC, an extra test scenario was created. In this scenario, all the operational modes were tested (buck, buck-boost and boost). The results are visible in the following figures. In the first case, the DC link presents an input voltage of 12V. The controller operates the converter as boost and the output is regulated at 47.8V.

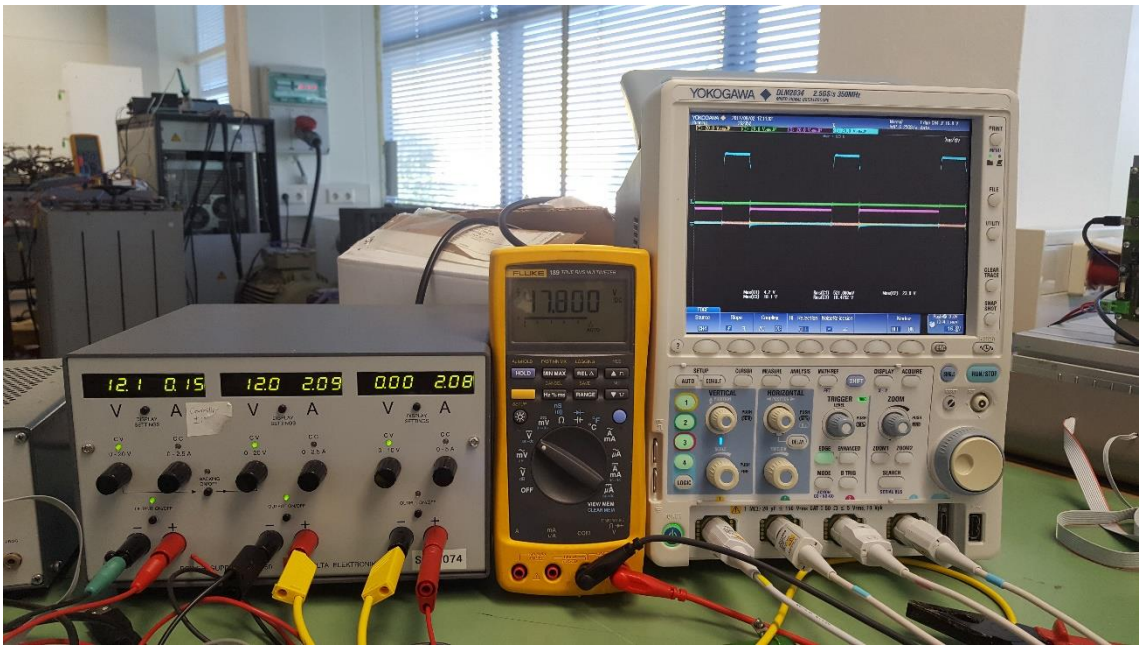


Figure 84. 12VDC link- 48V output to end-device

Following the same method as in the previous cases, by using some extra power supplies, the DC link voltage is increased at 48V and consequently at 60V. The converter swaps from boost to buck-boost and then to buck mode. The results are presented in the following Figure 85 and Figure 86.

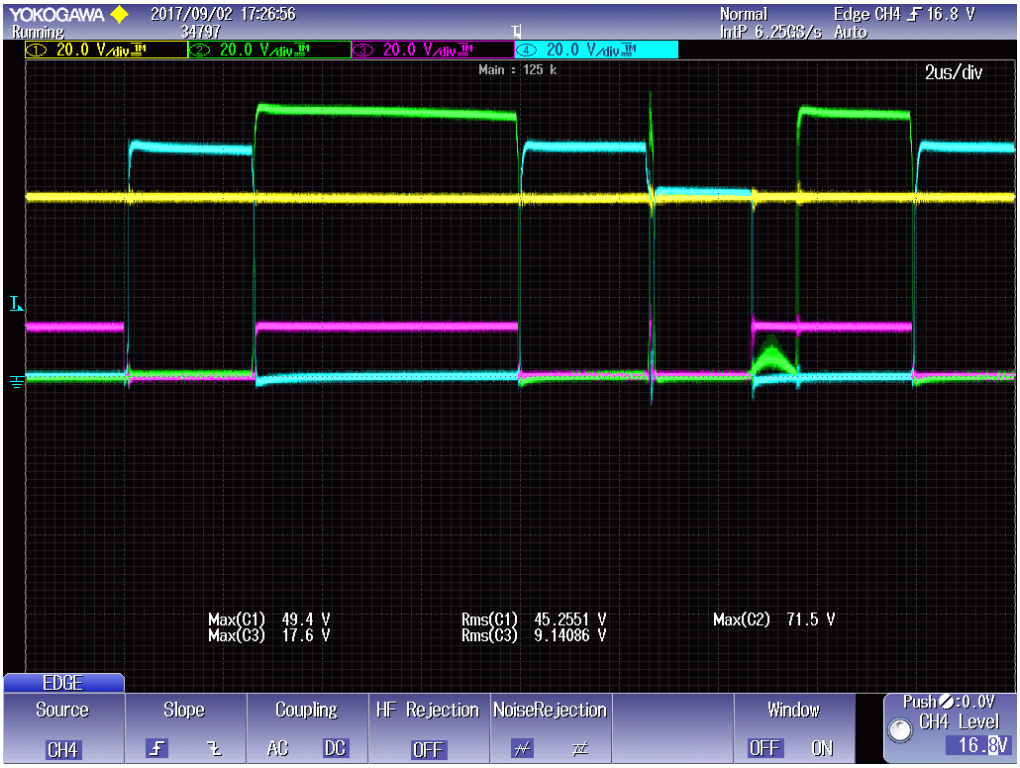


Figure 85. 48VDC link- 48V output switching scheme

Figure 86. 60VDC link- 48V output switching scheme

Converter Efficiency

In order to check the efficiency of the converter during all the operational modes, some measurements were taken while testing the different scenarios. The efficiency results are presented in Table 15.

Table 15. Efficiency results

Scenario	Mode	Average Efficiency (N)
2-20V DC link Input 5V DC @ max 1A Output	Boost	94.9%
	Buck-Boost	82.63%
	Buck	83.88%
3.5-20V DC link Input 12V DC @ max 1A Output	Boost	93.59%
	Buck-Boost	76.5%
	Buck	89.43%
5-30V DC link Input 20V DC @ max 1A Output	Boost	92.66%
	Buck-Boost	74.02%
	Buck	85.42%
12-60V DC link Input 48V DC @ max 1A Output	Boost	89.30%
	Buck-Boost	70.09%
	Buck	90.58%

As can be seen in Table 15, the efficiency of the converter decreases while the converter operates in the buck-boost operational mode. For this reason, it is ensured that this operation mode is used only when the input and output voltage are almost the same. The limitation of the maximum and minimum controlled duty cycle on the MOSFET's, creates the need of this in-between operational mode as explained in detail in sector 0.

CONCLUSION

This master thesis focused on the implementation of an application board which could provide an integrated solution to support bidirectional power flow between end-devices using the USB-type C interface, and the low voltage DC bus of a building. In the effort to prove this application concept, the thesis research was divided into several parts.

Initially, an extended study on the available USB type-C interface was conducted, to understand both the hardware and software requirements necessary to develop the interface. Subsequently, the next step was to understand how the requested power by the USB-type C could be supported and how could the bidirectional power flow work. For this step, it was necessary to research the appropriate DC-DC converter topology. The nature of the application, which is to provide variable output voltage and current levels, to meet the specifications of different end-devices, dictated the need for the use of multiple operational modes such as buck, boost or buck-boost. As a result, a very flexible solution of a DC-DC buck boost bidirectional converter was chosen since it could meet all the requirements of the application. In the second chapter of the thesis, the topology of the bidirectional converter as well as the theoretical analysis of the different modes was presented.

The next step was to investigate controlling methods for the DC-DC converter which can provide a regulated output voltage and limited output current, assuming a wide input DC voltage between 10-100V DC. The control of the system should provide a stabilized output voltage within the specifications of the end-devices. A smooth change between the different operational modes is essential to avoid disturbances at the output of the converter. In order to experiment with different control methods and investigate the response and stability of the system, the simulation of the power stage, as well as the digital control, was necessary. For this reason, the fourth chapter of the thesis was dedicated to the control and simulation of the system. The logic of the controlling method was presented and explained through a detailed functional diagram of the controlling algorithm. Furthermore, the implementation of the digital control was analyzed and finally the occurring results from the simulated scenarios were presented.

After the completion of the theoretical part, the implementation stage took place. The research started by investigating reference designs for the bidirectional converter, in order to obtain an efficient and durable solution. The most suitable reference was found from Texas Instruments [32] which was used to start developing the schematic of the application board. Similar examination was done to obtain a reference design for the USB type-C interface [34]. In order to customize the application, the appropriate changes and additions were made. In chapter five, all the design options and component selection was presented in detail. The next step, was the PCB layout and routing which took considerable time to make and correct, as the aim was to develop an electronic board which would be compatible but also compliant. Chapter five was completed with a thorough description of the application board in order to show explicitly to the reader the application use.

Following the full assembly of the electronic board, the last stage was to program and test different real case scenarios to examine the stability, efficiency and response of the application board. In chapter six, the experimental scenarios that were developed for testing were presented, followed by the results that arose during testing of the board in the lab facilities.

Research Outcome

With the completion of the present thesis, the questions that stimulated the conduction of this research were answered through the six main chapters.

The first research question of "*how could power management between the connected devices be accomplished, through the use of the USB type-C Power Delivery Protocol (PD protocol)*" is presented in the second chapter. The USB type-C interface is presented, along with the benefits and possibilities that it could offer. An extended analysis is done on the power delivery protocol, which can support up to 100W power transfer. The architecture of the interface, which operates based on discrete power profiles, is explained, as well as possible enhancements that could be implemented by the developer. The model of power negotiation between the interconnected devices is presented. Therefore, the conclusion of the research validates the idea of developing an application board, with a USB type-C interface, for power delivery between smart-devices.

The second question which refers to *"How could the host devices be used to power up the DC "Nano-grid" as a backup"* is answered through different chapters of this research. In the second chapter where the USB type -C interface is detailed, it is explained, that one of the most valuable features that this interface provides, is the flexibility of swapping the host and sink roles. This allows power transfer in both directions, thus the sink devices can turn to hosts, when they need to support the DC link of the Nano-grid. Furthermore, apart from the interface, it is mandatory that the power converter is also able to support the bidirectional power flow. In chapter three, where the topology of the converter is presented, the theoretical analysis is done to show specifically how the power converter reacts when the sinks need to become hosts and vice-versa.

The last question of "*How can the bidirectional power flow be accomplished from controlling point of view*" is analyzed in chapter four. In this chapter, the controlling method that was chosen to manage the power flow is explained. The monitoring of the input and output current and voltage, at any given moment, offers the ability to generate a controlling algorithm which is based on a state flow machine. A functional block diagram shows all the different states of the converter, as well as the parameters under which the converter swaps operational mode.

The accomplishment of the main target of this thesis, which was the "***The building of a DC-DC buck boost bidirectional converter with a USB type-C interface for power delivery***", proved that the original idea to develop an application board which could supply power to the end-devices but also use the Li-ion batteries of the end-devices to provide power to the DC grid of a commercial building or a house, is indeed possible and viable.

The results that arose during the testing of the application board were positive regarding the feasibility of the system, and verified that the application board could turn into a real market product, if some additional enhancements, both from software and hardware side, were provided.

Challenges

During the realization of the thesis a lot of difficulties were met and failures transpired. More specifically, the decision to integrate the new USB type-C interface. On the one hand, the USB type-C interface presents numerous advantages and was ideal for the use case of the application. On the other hand, the collection of information regarding the hardware development and protocol implementation was rather limited and difficult since the only source was the "Chromium Projects " by Google which had very limited technical documentation support. The implementation of the firmware running the type-C protocol, needed a high skill level of embedded C coding thus, the generation of upgraded custom firmware, which could

support several power profiles, dictated the need for support from another student, specialized on embedded systems. The communication between the STM32 and C2000 microcontrollers through the I2C line presented several problems and consequently, for the testing of the application board, two additional GPIOs were used to transfer relevant information regarding the reference voltage and current levels. Therefore, for future research projects focusing on the implementation on the USB type C interface combined with power conversion, it would be advisable to separate the topics in order to provide the necessary expertise to integrate these two complex areas into one solution.

A further difficulty arose with the development of the PCB layout, component placement and signal routing which consumed considerable amount of time since, an amateur PCB designer needs to devote time to learn the designing rules and routing techniques in order to develop a compatible electronic board. The realization of a compatible board demands several iterations until a proper layout has been accomplished.

After the board was fully assembled, the testing part was quite challenging. The programming of the control on the microcontroller needed several modifications in comparison to the simulated one. While testing, some failures occurred on main components (MOSFET's, MCU) that had to be replaced. Through the qualification stage of the board, designing issues were discovered that had to be corrected . The positive side was that additional experience was gained for future PCB design and ease of testing.

Future Research

During the implementation of the thesis, questions and ideas surfaced which could stimulate further future research on the topic using the current application board. For example, other controlling methods could be investigated for the present system and different digital controlling methods could be implemented which may result in even greater efficiency of the system. The implementation of a control, following zero voltage switching (ZVS) or zero current switching (ZCS) principle, could produce another controlling method of the system with higher efficiency due to the saving of energy from switching losses. This method could not be supported by a PI controller since the switching times and deadtimes of the MOSFET's should be calculated by a mathematical function defined by the transfer function of the system.

While designing the controller logic, another plausible question arose. Considering the case that the DC link cannot provide power to the end-devices after a DC source failure has occurred, the converter will swap the power flow and provide power to the DC link from the end-devices. When the power has been restored to the DC link, it is essential that the end-devices will stop providing power to the grid and the source-sink role will change back to default. In order to achieve that, a possible solution would be; while the devices have taken the role of the source, after a certain period of time the controller should disconnect the end-devices from the V_{BUS} node and get a voltage measurement from the grid side. In this way, if the power has been restored, the grid will be able to provide power again back to the end-devices instead of draining their batteries.

The idea of improving the existing firmware by adding new power profiles could also present an opportunity for further research on the project. High power devices using the USB type-C interface might need different voltage and current profiles. Thus, a new profile of 48V at 2A could be generated and tested, using the application board. The possibility of developing the BMC protocol also for high speed data transfer, would enhance and upgrade fundamentally the application board and make it an even more viable solution for a real market product.

In case the application board was intended to become a real market product, an idea would be to integrate it into a frame which would provide multiple USB type-C ports. This frame could be installed directly inside the wall, next to the power sockets of a smart commercial building or

a house, where the users can plug directly their smart-devices. Thus, a study could be conducted regarding the maximum power dissipation that could be achieved from inside the wall or possible cooling system solutions that would serve this type of application.

Through the development of the present thesis, the aim of the research which was " the building of a DC-DC buck boost bidirectional converter with a USB type-C interface for power delivery" was achieved. The implementation of the application board is a contribution to the "Delft University of Technology", since every student, who wants to conduct a research on relevant topics, can use the application board for testing but also as a reference point, both from a hardware and software point of view. On a personal level, the implementation and completion of this master thesis offered me multiple benefits; gained knowledge on new technology fields, obtained PCB designing skills, improved my knowledge on power electronics by applying theoretical knowledge in to practice and sharpened my algorithm designing and programming skills.

REFERENCES

[1] D. Larruskain, A. M. I. Zamora, O. Abarrategui and J. Monasterio, "Transmission and Distribution Networks: AC versus DC," Department of Electrical Engineering, University of the Basque Country, Bilbao (Spain).

[2] R. Kempener, P. Komor and A. Hoke, "SMART GRIDS AND RENEWABLES," International Renewable Energy Agency (IRENA), 2013.

[3] C. Koenigs, M. Suri, A. Kreiter, C. Elling, J. Eagles, T. R. Peterson, J. C. Stephens and E. J. Wilson, "A Smarter Grid for Renewable Energy: Different States of Action," pp. 217-233, 15 November 2013.

[4] X. Fang, S. Misra, G. Xue and Dejun Yang, "Smart Grid – The New and Improved Power Grid: A Survey," 2011.

[5] M. SHwehdi and M. A. Aqil, "Forthcoming smart DC nano-grid for green buildings—A reflective vision," *International Journal of Smart Grid and Clean Energy,* pp. 52-58, 2015.

[6] P. Vinciarelli.USA Patent US6788033 B2, 2004.

[7] USB 3.0 Promoter Group , "Universal Serial Bus Type-C Cabel and Connector Specification," USB 3.0 Promoter Group, 2014.

[8] A. Rogers, "Introduction to USB Type-C™," Microchip Technology Inc., 2015.

[9] N. Enos and B. Gosselin, "A primer on USB Type-C and Power Delivery applications and requirements," Texas Instruments Incorporated, Dallas, Texas, 2016.

[10] Texas Instruments, "TUSB320 USB Type-C™ Configuration Channel Logic and Port Control," Texas Instruments, Dallas, Texas, 2017.

[11] USB Implementers Forum, "USB Type-C™ Overview," USBif, Hong Kong, 2016.

[12] TI E2E™ Community, "TI E2E™ Community," Texas Instruments, Copyright 1995-2017. [Online]. Available: https://e2e.ti.com/blogs_/b/analogwire/archive/2016/10/24/how-to-protect-the-usb-type-c-connector. [Accessed 08 09 2017].

[13] STMicroelectronics, "USB Power Delivery and Type-C," STMicroelectronics, 2017.

[14] N. Mohan, T. A. Underland and W. P.Robbins, Power Electronics Converters, Applications and Design, 1995.

[15] Jaycar Electronics, "DC-DC CONVERTERS: A PRIMER," Jaycar Electronics, 2001.

[16] Eurobat, "Battery Energy Storage for smart grid applications," Eurobat, Brussels, 2013.

[17] Y. MEI, Q. JIANG, H. YANG1, W. LI, X. HE and S. LI, "Non-isolated stacked bidirectional soft-switching DC-DC converter with PWM plus phase-shift control scheme," MPCE, 2017.

[18] A. Andreas and M. Esser.USA Patent US5734258 A, 1996.

[19] R. W. D. M. Erickson, Fundamentals of Power Electronics Second Edition, New York: Kluer Academic Publishers, 2001.

[20] ON Semiconductor, "Effects of High Switching Frequency on Buck Regulators," 13 07 2017. [Online]. Available: http://www.onsemi.com/.

[21] USB, "USB Power Delivery Specification Revision 3.0," 2017.

[22] Vishay Siliconix, "Selection of MOSFETs for DC/DC Synchronous Buck Controllers: SiP12201 Single 10 A Controller and SiP12203 Triple Step Down Controller IC for 2 Synchronous and 1 Linear Power Rail," Vishay, 2008.

[23] Texas Instruments, "MOSFET power losses and how they affect power supply efficiency," Texas Instruments, Dallas Texas, 2016.

[24] M. J. P. Garcia, G. Gutierrez, J. E. Normey-Rico and C. d. Prada, "INTEGRATED DESIGN & CONTROL OF A BUCK BOOST CONVERTER," Universidade Federal de Santa Catarina, Valladolid, Spain, 2009.

[25] S. Verma, S. Singh and A. Rao, "Overview of control Techniques for DC-DC converters," Research Journal of Engineering Sciences, INDIA, 2013.

[26] INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC), "Fuzzy Control Programming," 1997.

[27] M. Hedlund, "Design and construction of a bidirectional DCDC converter for an EV application," Uppsala Univeritet, Uppsala, 2010.

[28] K. J. Astrom, "Control System Design-PID Control," 2002.

[29] D. Xue, Y. Chen and D. P. Atherton, "Linear Feedback Control," Society for Industrial and Applied Mathematics, 2007.

[30] "My Weblog," 11 May 2008. [Online]. Available: https://radhesh.wordpress.com/2008/05/11/pid-controller-simplified/. [Accessed 22 08 2017].

[31] J. ZIEGLER and N. B. NICHOLS, "Optimum Settings for Automatic Controllers," New York, 1942.

[32] Texas Instruments, "Bi-Directional Non-Isolated Buck Boost Converter," Texas Instruments, 2015.

[33] Google Sites, "The Chromium Projects," Google, 4 January 2014. [Online]. Available: https://www.chromium.org/chromium-os/developer-guide. [Accessed 27 August 2017].

[34] Google Git, "chromium / chromiumos / platform / ec / master / . / board," Google, 2014. [Online]. Available: https://chromium.googlesource.com/chromiumos/platform/ec/+/master/board. [Accessed 27 August 2017].

[35] S. Kashyap, "Implementing a Power Delivery Policy," Unpublished, Delft, 2016.

[36] Advanced Circuits, "Advanced Circuits 4 PCBs," Designed and Powered By Inroads, [Online]. Available: http://www.4pcb.com/trace-width-calculator.html. [Accessed 29 August 2017].

[37] A. D. Patel, "Analysis of bidirectional buck boost converter by using PWM control scheme," Electronics and communication Marwadi education foundation group of institute, Rajkot, India.

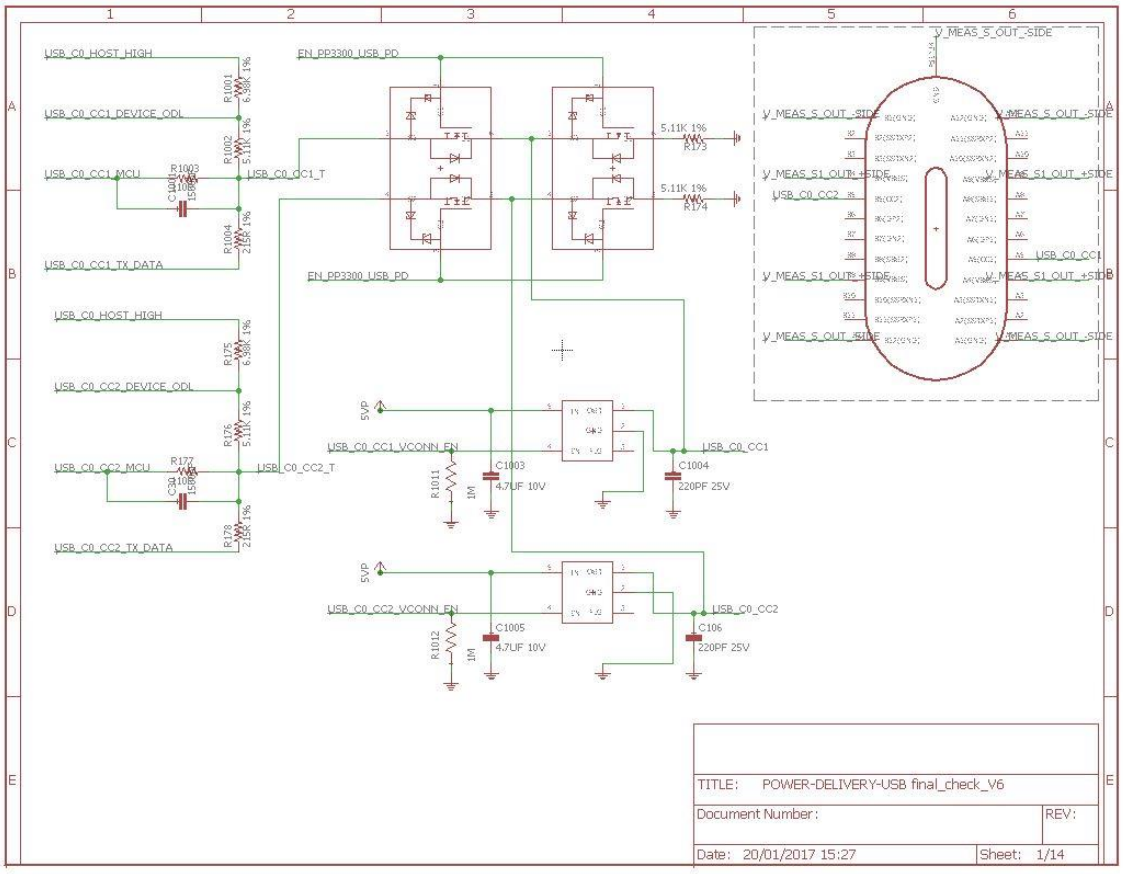
[38] M. Wens and M. Steyaert, "Design and Implementation of Fully-Integrated Inductive DC-DC converters in Standard CMOS," Springer, 2011.

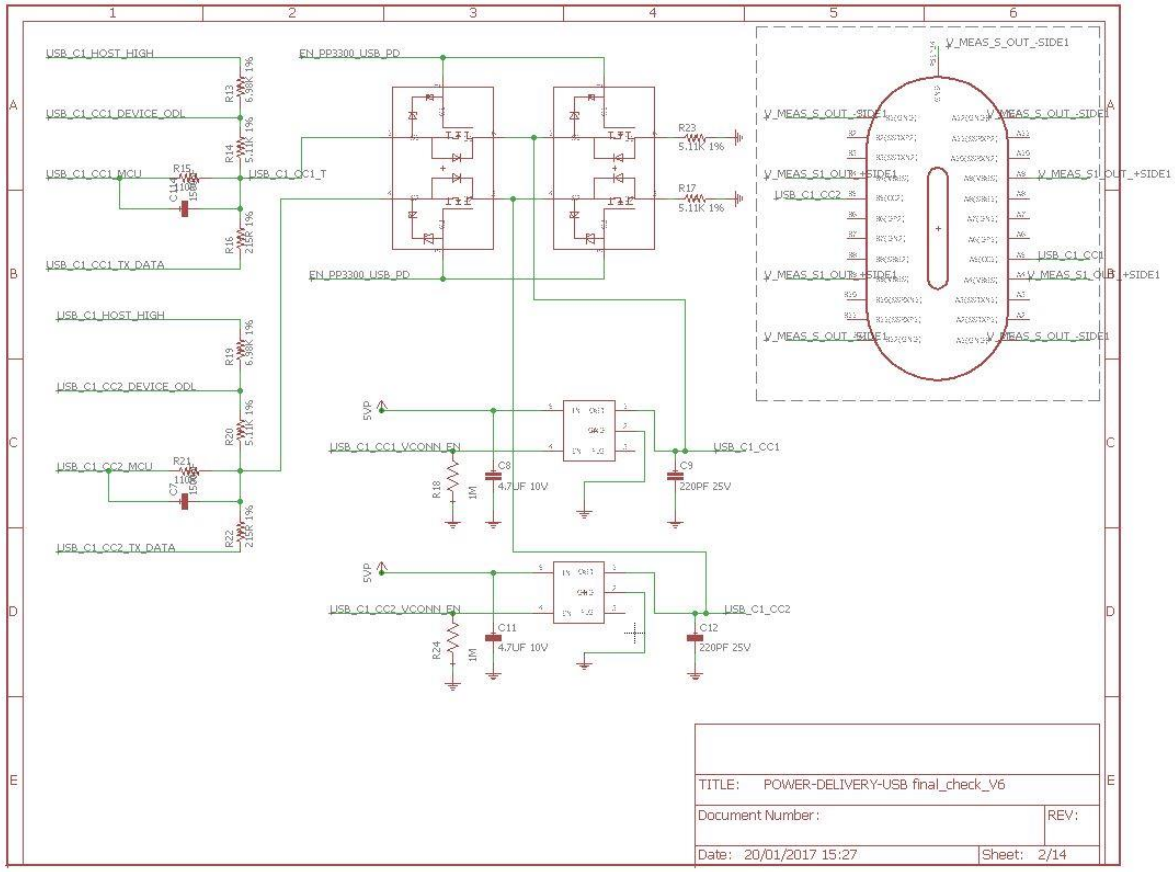
[39] FAIRCHILD, "USB Type-C Design Considerations," Fairchild Semiconductor Corporation, 2015.

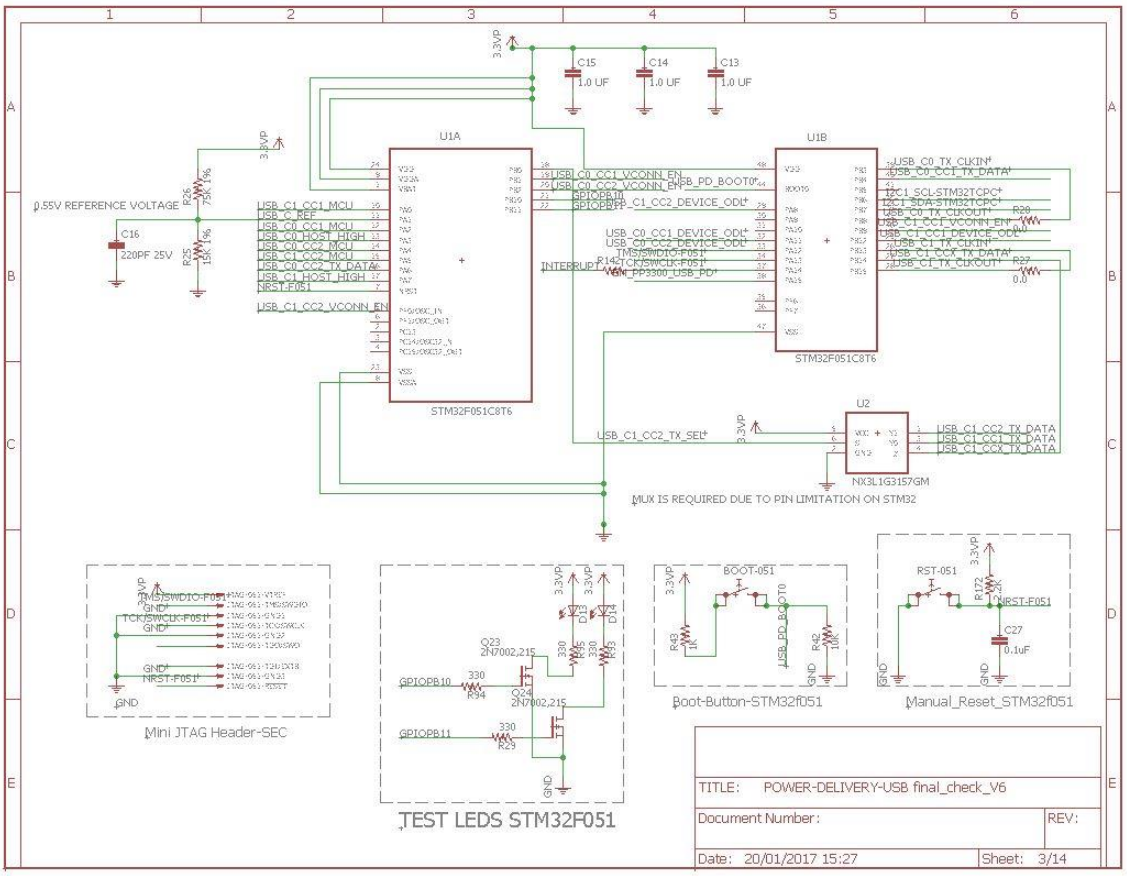
[40] STMicroelectronics, "USB Type-C™ datalines and "Alternate Mode"," STMicroelectronics, 2017.

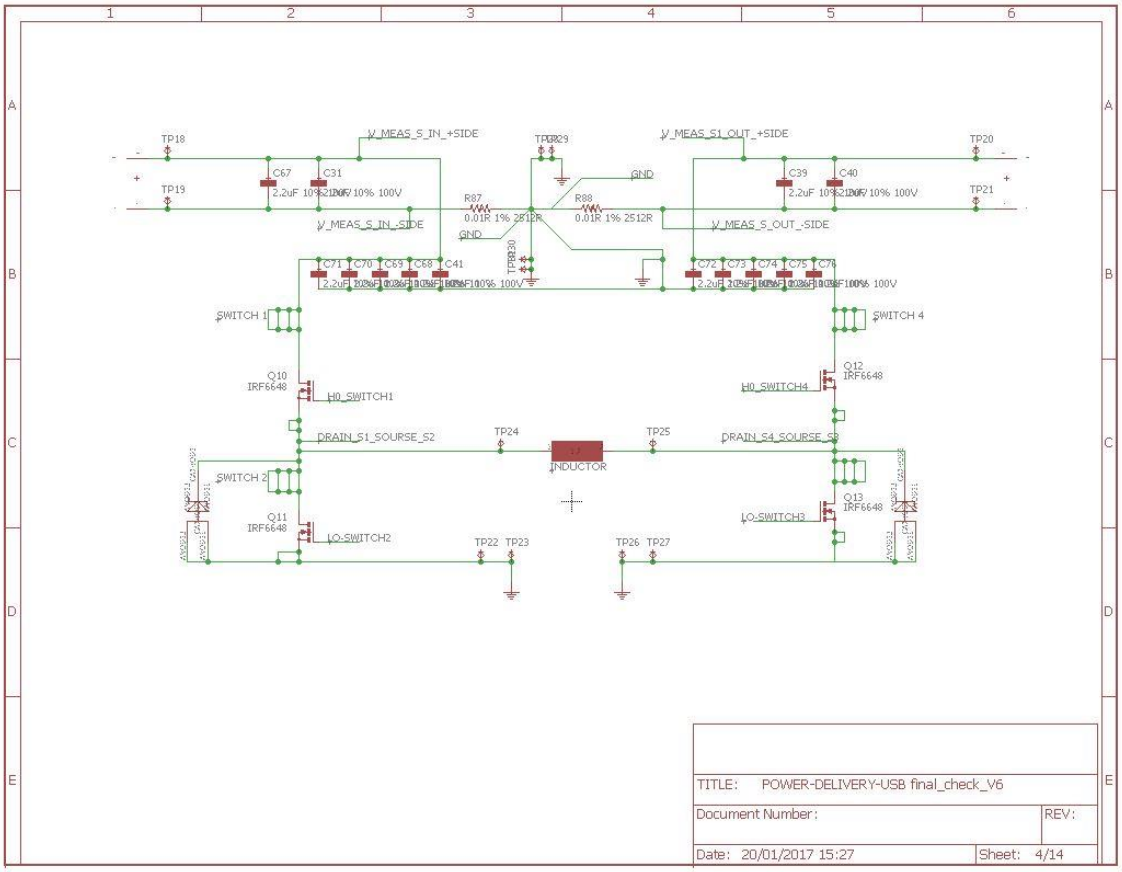
APPENDIX I

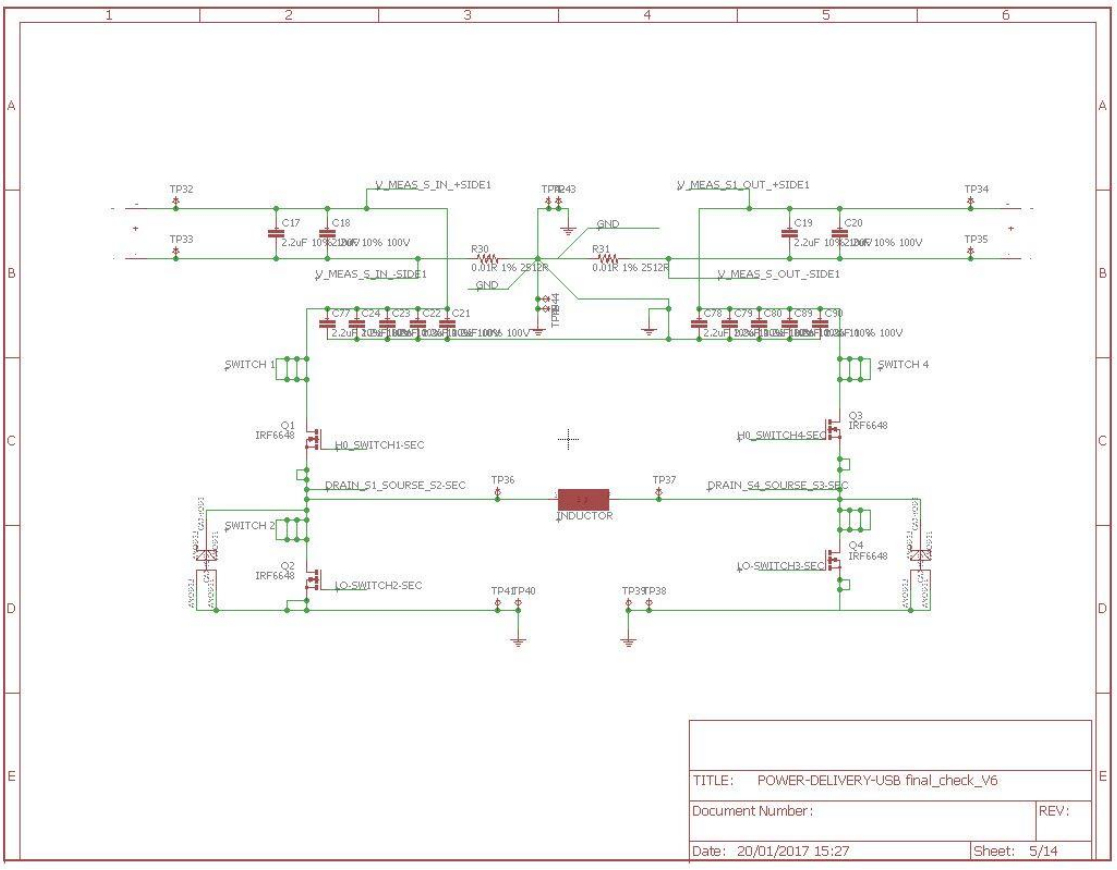
In the appendix the application board schematic will be included. The schematics as well as the PCB designing were implemented using the software “Eagle 7.6.0”.

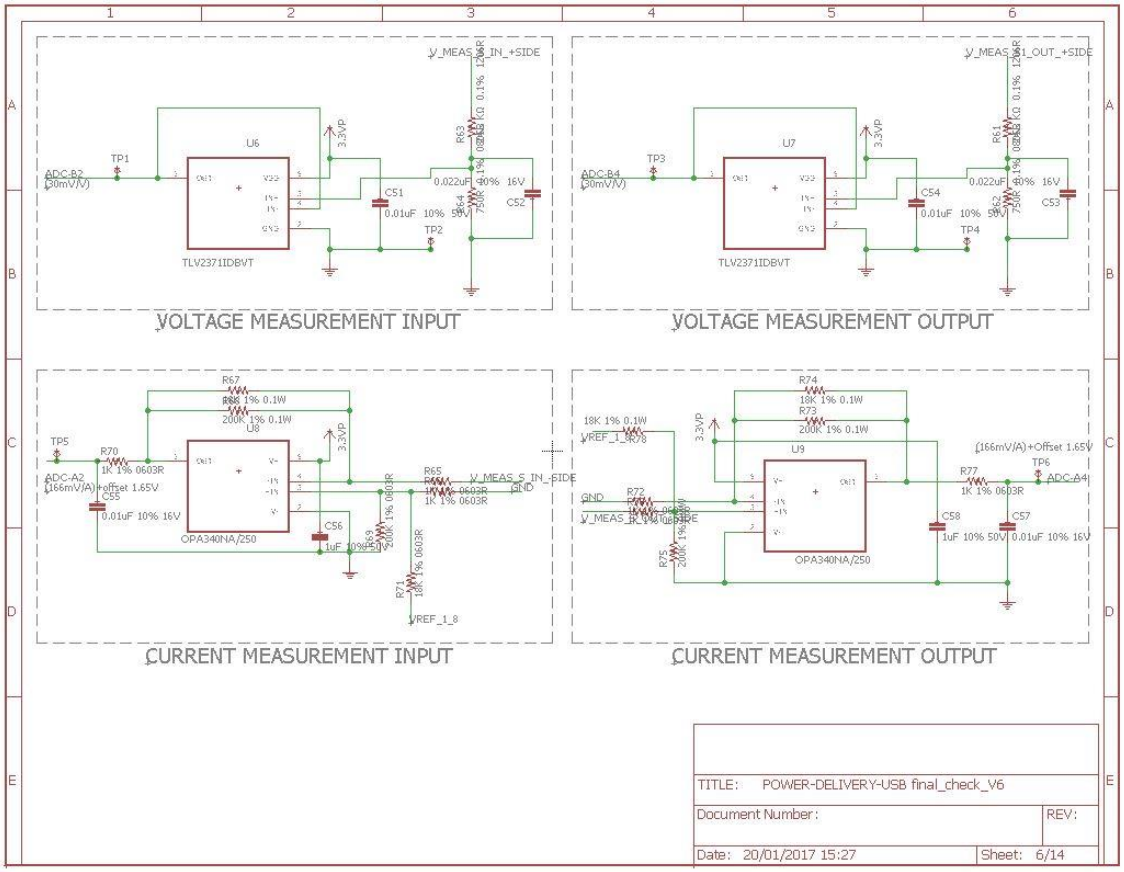


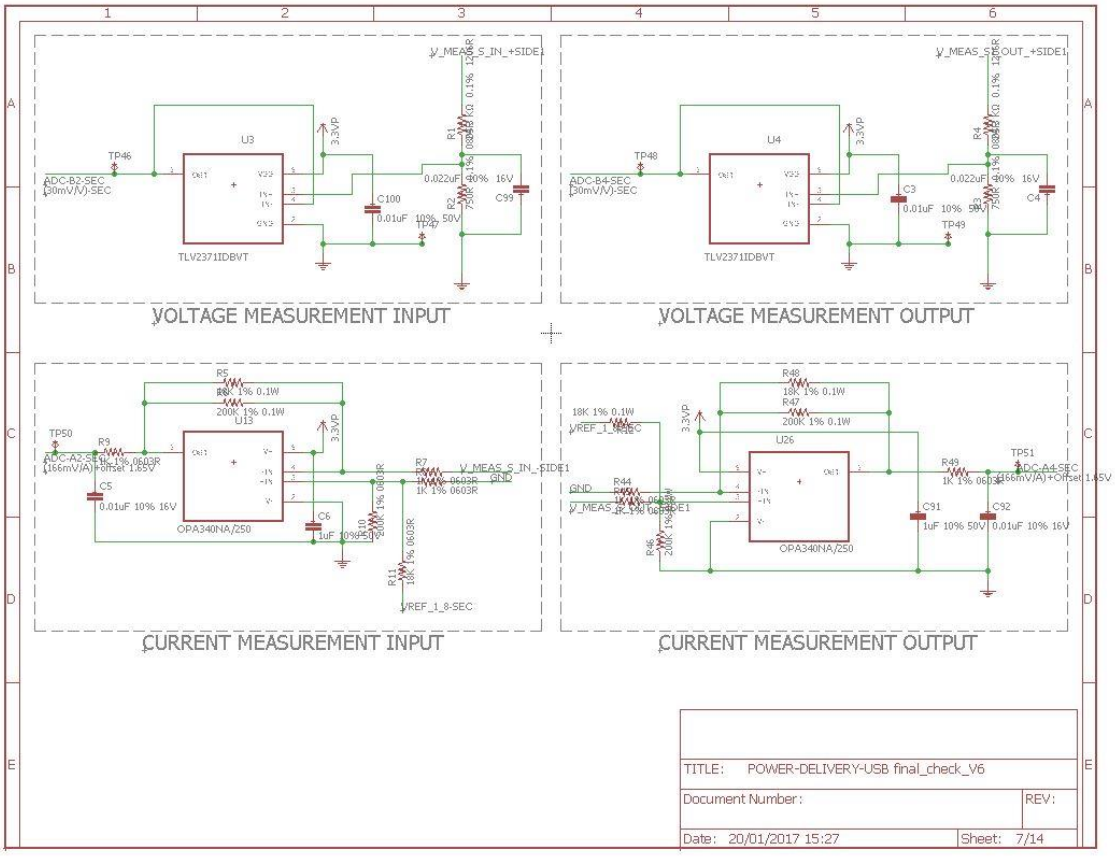

USB_C1_HOST_HIGH
USB_C1_CC1_DEVICE_ODL
USB_C1_CC1_MCU
USB_C1_CC1_TX_DATA
USB_C1_HOST_HIGH
USB_C1_CC2_DEVICE_ODL
USB_C1_CC2_MCU
USB_C1_CC2_TX_DATA
EN_PP3300_USB_PD
USB_C1_CC1_T
USB_C1_CC1_VCONN_EN
USB_C1_CC2_VCONN_EN
USB_C1_CC1
USB_C1_CC2
V_MEAS_S_OUT_-SIDE1
V_MEAS_S_OUT_+SIDE1
V_MEAS_S1_OUT_-SIDE1
V_MEAS_S1_OUT_+SIDE1
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 2/14

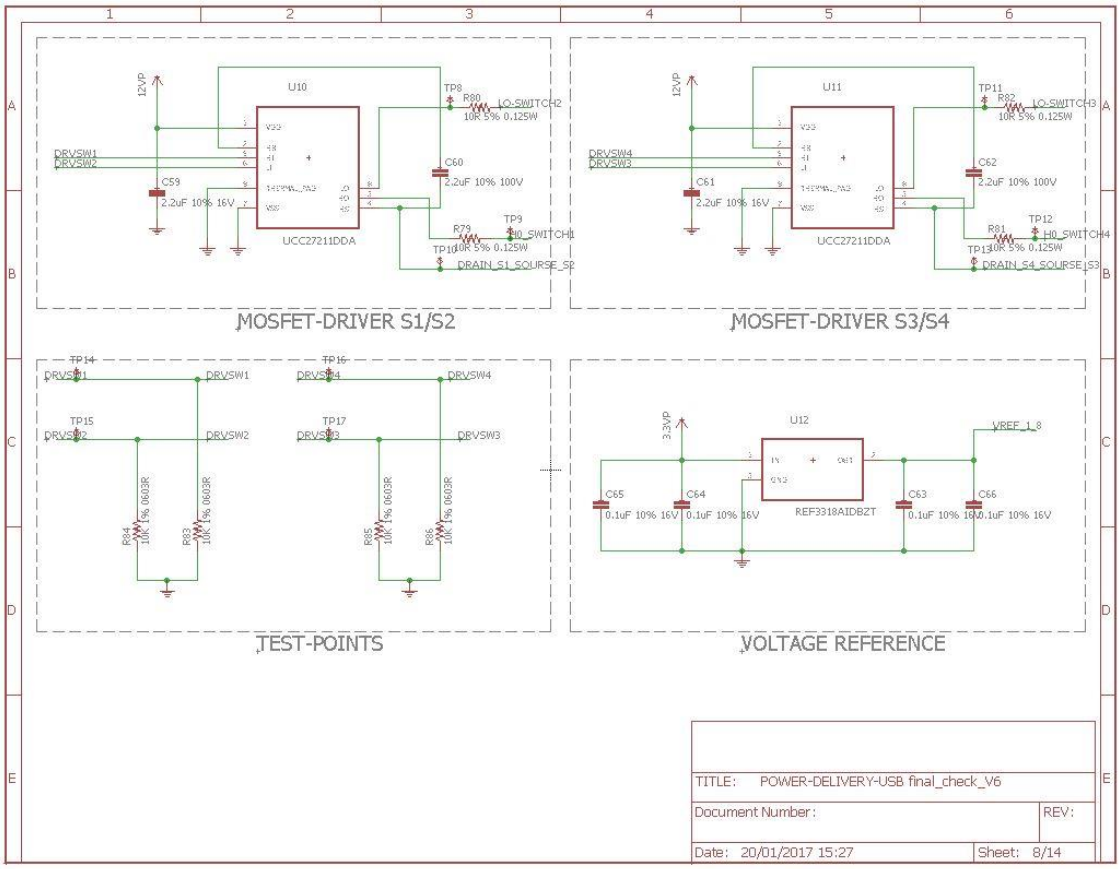

0.55V REFERENCE VOLTAGE
STM32F051C8T6
NX3L1G3157GM
MUX IS REQUIRED DUE TO PIN LIMITATION ON STM32
Mini JTAG Header-SEC
TEST LEDS STM32F051
Boot-Button-STM32f051
Manual_Reset_STM32f051
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 3/14

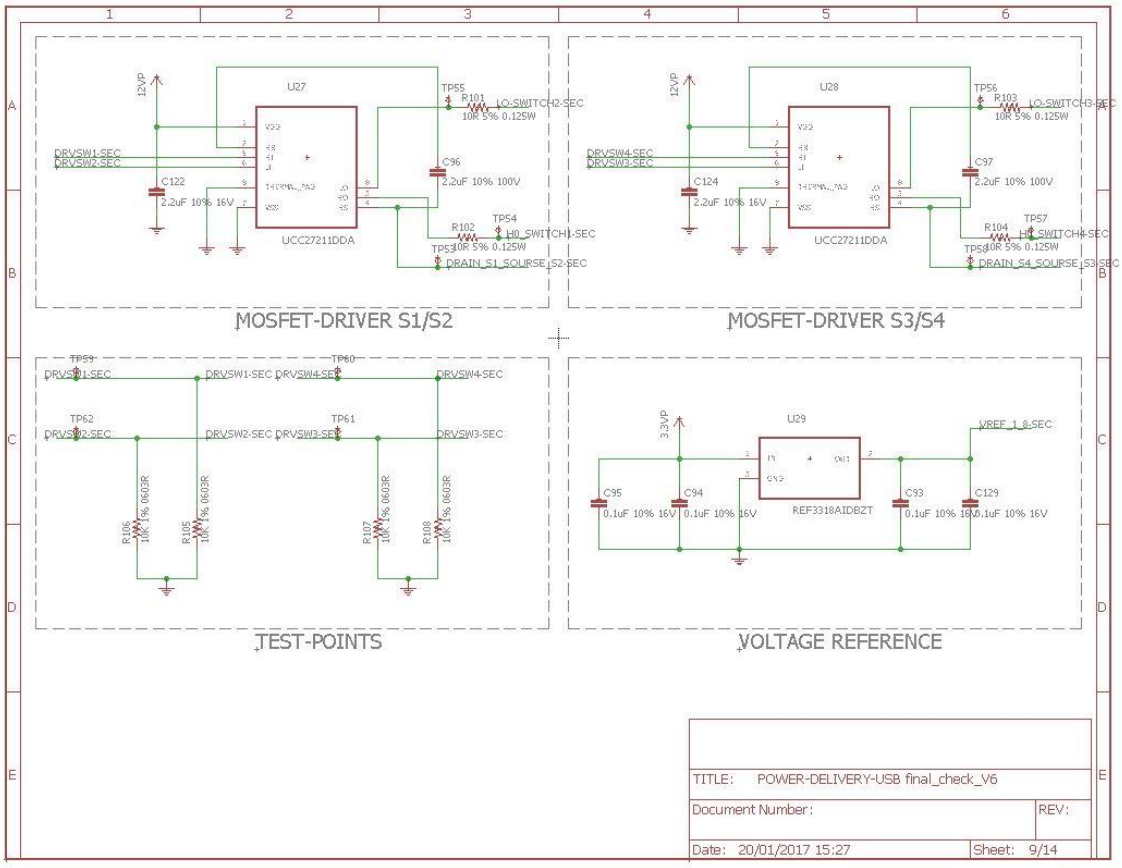

TP18
V_MEAS_S_IN_+SIDE
TP29
V_MEAS_S1_OUT_+SIDE
TP20
TP19
C67
C31
2.2uF 10% 100V
GND
C39
C40
TP21
R87
0.01R 1% 2512R
R88
V_MEAS_S_IN_-SIDE
V_MEAS_S_OUT_-SIDE
C71 C70 C69 C68 C41
C72 C73 C74 C75 C76
SWITCH 1
SWITCH 4
Q10
IRF6648
HO_SWITCH1
Q12
HO_SWITCH4
DRAIN_S1_SOURSE_S2
TP24
TP25
DRAIN_S4_SOURSE_S3
SWITCH 2
Q11
LO-SWITCH2
Q13
LO-SWITCH3
TP22 TP23
TP26 TP27
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 4/14

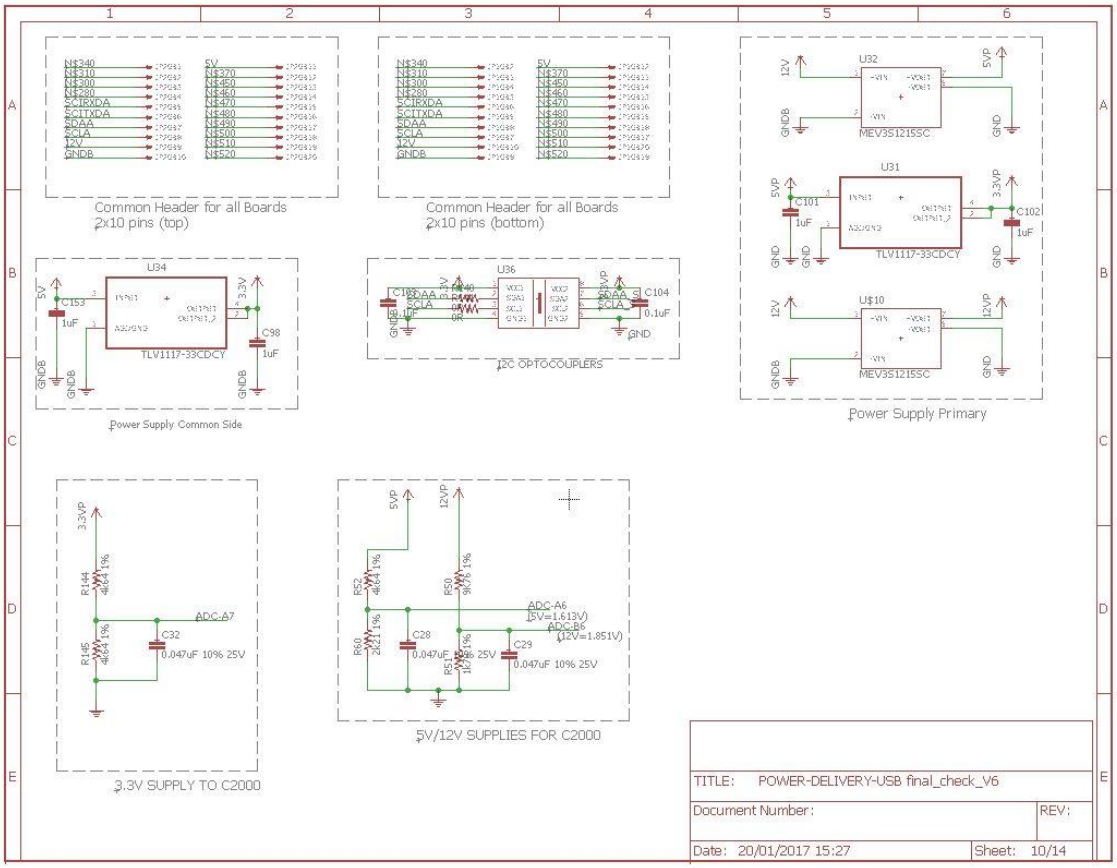

TP32
V_MEAS_S_IN_+SIDE1
TP43
V_MEAS_S1_OUT_+SIDE1
TP34
TP33
C17
C18
2.2uF 10% 100V
GND
C19
C20
TP35
R30
0.01R 1% 2512R
R31
V_MEAS_S_IN_-SIDE1
V_MEAS_S_OUT_-SIDE1
C77 C24 C23 C22 C21
C78 C79 C80 C89 C90
SWITCH 1
SWITCH 4
Q1
IRF6648
HO_SWITCH1-SEC
Q3
HO_SWITCH4-SEC
DRAIN_S1_SOURSE_S2-SEC
TP36
TP37
DRAIN_S4_SOURSE_S3-SEC
SWITCH 2
Q2
LO-SWITCH2-SEC
Q4
LO-SWITCH3-SEC
TP41 TP40
TP39 TP38
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 5/14

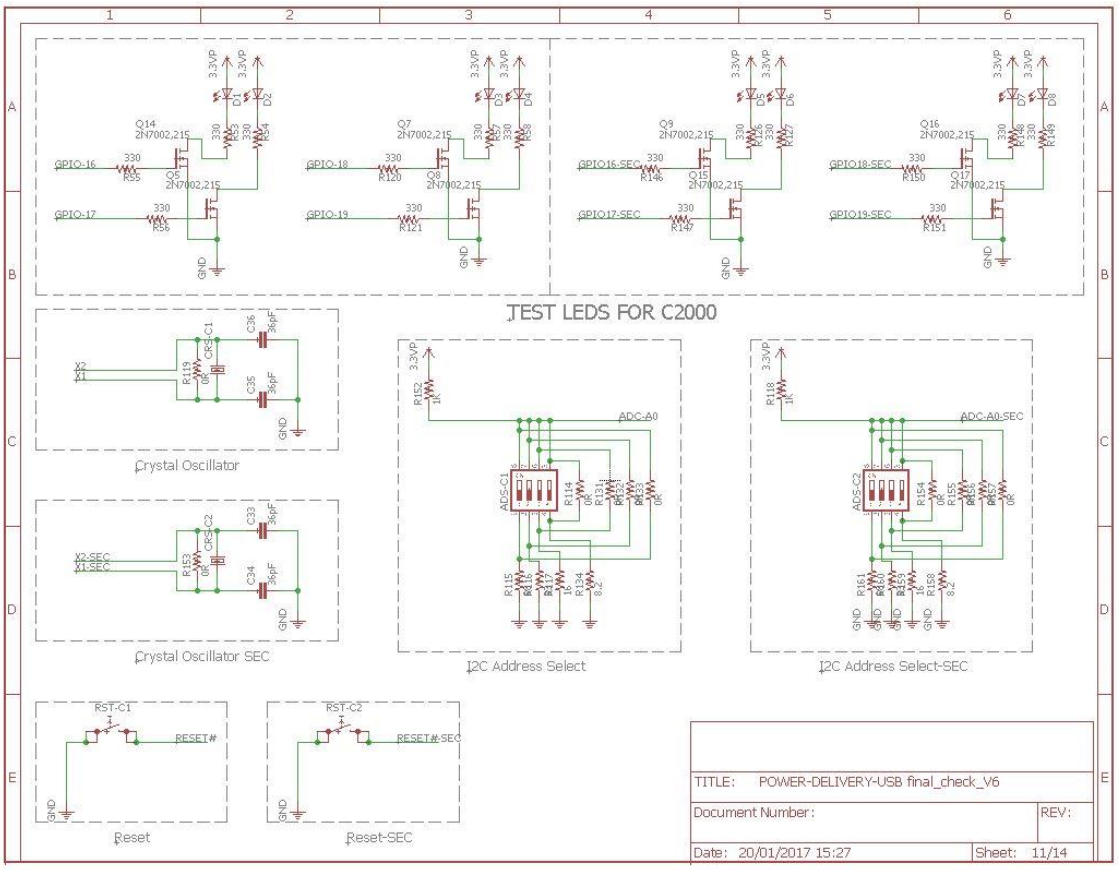

V_MEAS_IN_+SIDE
V_MEAS_1_OUT_+SIDE
U6
U7
TLV2371IDBVT
ADC-B2
(50mV/V)
ADC-B4
(50mV/V)
3.3VP
0.022uF 10% 16V
0.01uF 10% 50V
VOLTAGE MEASUREMENT INPUT
VOLTAGE MEASUREMENT OUTPUT
U8
U9
OPA340NA/250
ADC-A2
(166mV/A)+offset 1.65V
(166mV/A)+Offset 1.65V
ADC-A4
V_MEAS_S_IN_SIDE
GND
VREF_1_8
CURRENT MEASUREMENT INPUT
CURRENT MEASUREMENT OUTPUT
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 6/14

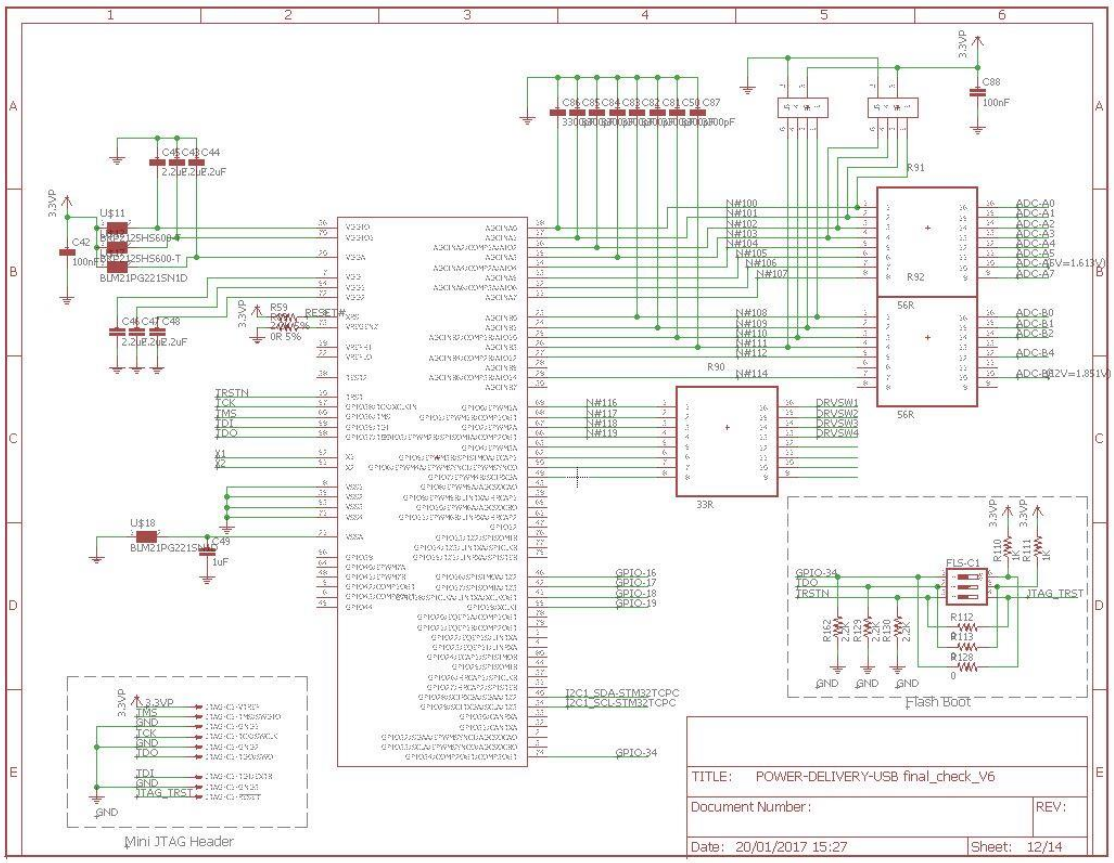

V_MEAS_S_IN_+SIDE1
V_MEAS_S_OUT_+SIDE1
U3
U4
TLV2371IDBVT
ADC-B2-SEC
(50mV/V)-SEC
ADC-B4-SEC
(50mV/V)-SEC
3.3VP
0.022uF 10% 16V
0.01uF 10% 50V
VOLTAGE MEASUREMENT INPUT
VOLTAGE MEASUREMENT OUTPUT
U13
U26
OPA340NA/250
ADC-A2-SEC
(166mV/A)+offset 1.65V
(166mV/A)+Offset 1.65V
ADC-A4-SEC
V_MEAS_S_IN_SIDE1
GND
VREF_1_8-SEC
CURRENT MEASUREMENT INPUT
CURRENT MEASUREMENT OUTPUT
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 7/14

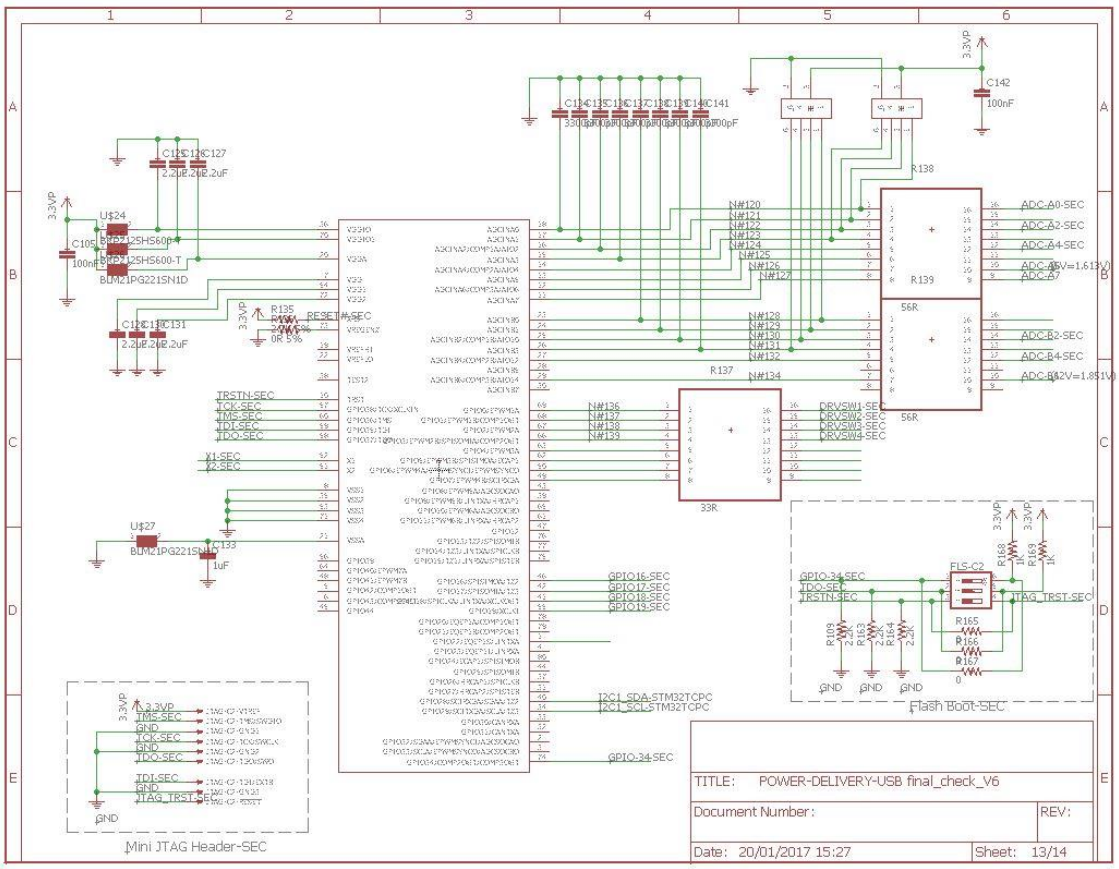

MOSFET-DRIVER S1/S2
MOSFET-DRIVER S3/S4
TEST-POINTS
VOLTAGE REFERENCE
U10
U11
U12
UCC27211DDA
REF3318AIDBZT
12VP
3.3VP
DRVSW1
DRVSW2
DRVSW3
DRVSW4
C59
C60
C61
C62
C63
C64
C65
C66
R80
R82
R84
R85
R86
TP8
TP9
TP11
TP12
TP14
TP15
TP16
TP17
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 8/14

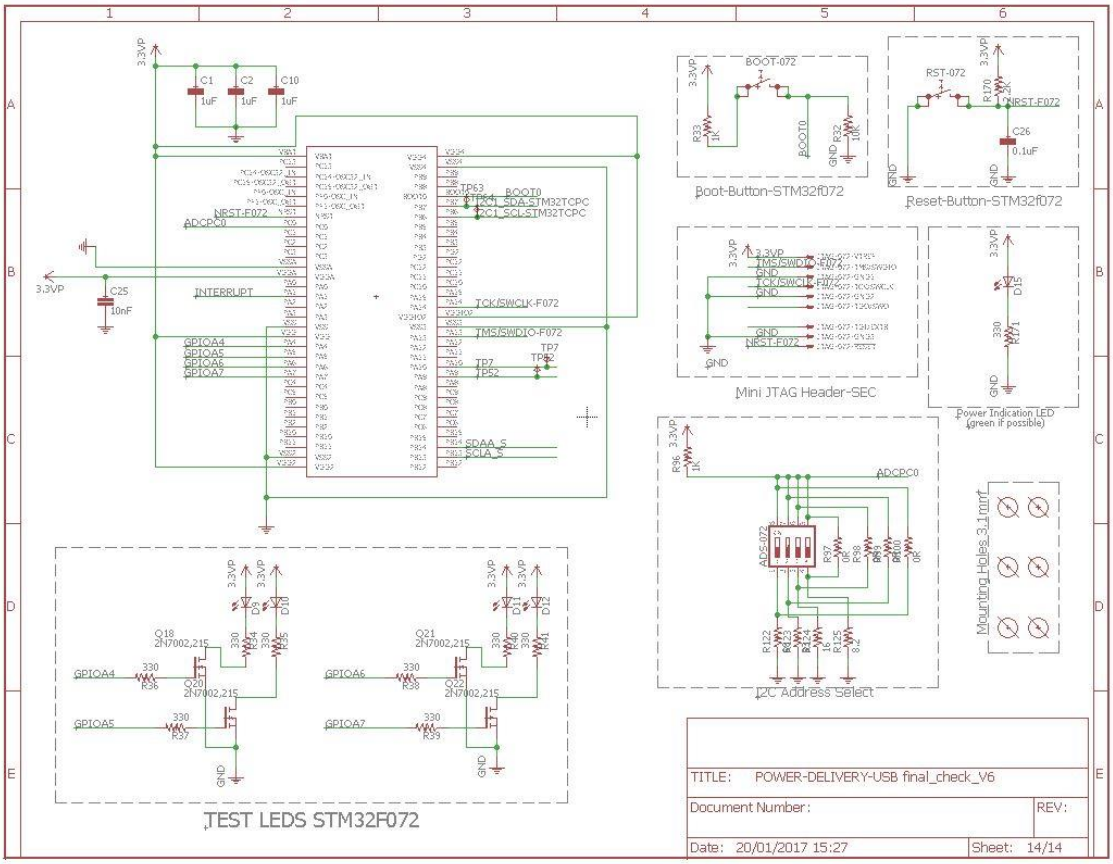

MOSFET-DRIVER S1/S2
MOSFET-DRIVER S3/S4
TEST-POINTS
VOLTAGE REFERENCE
U27
U28
U29
UCC27211DDA
REF3318AIDBZT
12VP
3.3VP
DRVSW1-SEC
DRVSW2-SEC
DRVSW3-SEC
DRVSW4-SEC
C122
C96
C124
C97
C95
C94
C93
C129
R101
R103
R102
R104
R106
R105
R107
R108
TP55
TP56
TP54
TP57
TP59
TP60
TP62
TP61
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 9/14


Common Header for all Boards
2x10 pins (top)
Common Header for all Boards
2x10 pins (bottom)
U32
MEV3S1215SC
U31
TLV1117-33CDCY
U$10
MEV3S1215SC
Power Supply Primary
U34
TLV1117-33CDCY
Power Supply Common Side
U36
I2C OPTOCOUPLERS
3.3V SUPPLY TO C2000
5V/12V SUPPLIES FOR C2000
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 10/14


TEST LEDS FOR C2000
Crystal Oscillator
Crystal Oscillator SEC
I2C Address Select
I2C Address Select-SEC
Reset
Reset-SEC
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 11/14


Mini JTAG Header
Flash Boot
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 12/14


Mini JTAG Header-SEC
Flash Boot-SEC
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 13/14


TEST LEDS STM32F072
Boot-Button-STM32f072
Reset-Button-STM32f072
Mini JTAG Header-SEC
Power Indication LED (green if possible)
I2C Address Select
Mounting_Holes_3.1mm
TITLE: POWER-DELIVERY-USB final_check_V6
Document Number:
REV:
Date: 20/01/2017 15:27
Sheet: 14/14

APPENDIX II

In the appendix B the controlling code is given. The controller is a MATLAB function.

```
%% In this function the algorithm control of a DC-DC bidirectional
buck-boost converter is implemented
function[Buck_norm,Vin,Vout,Iin,Iout,FBpin,Buck_Rev,Boost_norm,Boost_R
ev,balance,BuckBoost,BuckBoost_Rev,flag,flag_1,flagi,flagi_1,Debug_Var
,DBG]=Power_Management_Control(Vin,Vout,Iin,Iout,FBpin,C,D,E)
Buck_norm=0;
Buck_Rev=0;
Boost_norm=0;
Boost_Rev=0;
balance=0;
BuckBoost=0;
BuckBoost_Rev=0; %% Initialization of the operation modes


flag=C;          %% State Maching Variables (memory of the previous
operational mode)
flag_1=D;        %% Its state has unique combintation of values
Debug_Var=E;



if Vin>=1 || Vout>=1 %% The boundary conditions are checked
%This condition will define the power flow
%If condition is met power flow goes A-->B
if  Vin>Vout && flag~=2
    flag=1;
    if FBpin<=0.94*Vin %% If condition is met Buck Operation from A--
>B starts
        Debug_Var=3;    %% 0.94 stands for the maximum Buck Duty Cycle
        flag_1=1;
        Buck_norm=1;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
    elseif FBpin>=Vin/(1-0.06) %% If condition is met Boost Operation
from A-->B starts
        Debug_Var=4;           %% 0.06 stands for the minimum Boost
Duty Cycle
        flag_1=2;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=1;
        Boost_Rev=0;
        balance=0;
    elseif 0.94*Vin<=FBpin && FBpin<=(Vin/(1-0.06)) %% If condition is
met Buck-Boost Operation from A-->B
        Debug_Var=6;
        flag_1=10;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=1;
    end
end
```

```
%This condition will define the power flow
%If condition is met power flow goes B-->A

if  Vout>Vin && flag~=1
    flag=2;
   if FBpin<=0.94*Vout %% If condition is met Buck Operation from B--
>A starts
        flag_1=3;      %% 0.94 stands for the maximum Buck Duty Cycle
        Buck_norm=0;
        Buck_Rev=1;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
    elseif FBpin>=Vout/(1-0.06) %% If condition is met Boost Operation
from B-->A starts
        flag_1=4;               %% 0.06 stands for the minimum Boost
Duty Cycle
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=1;
        balance=0;
    elseif 0.94*Vout<=FBpin && FBpin<=(Vout/(1-0.06))  %% If condition
is met Buck-Boost Operation from B-->A starts
        flag_1=11;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost_Rev=1;
   end
end
%% Depending on the initial selection of operation mode, the algorithm
%  enters the equivalent mode until a new mode is needed to meet the
%  the requirements of the output. In case the boundary conditions are
not met
%  which means that the source cannot provide enough power, the state
%  machine variables reset and the algorithm checks if the end-devices
%  can support the grid.

% State flag=1, flag_=1 defines Buck Operation from A-->B

if flag==1 && flag_1==1
        Buck_norm=1;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
    if FBpin<0.94*Vin
        Debug_Var=10;
        flag_1=1;
        Buck_norm=1;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
    end
    if FBpin>Vin/(1-0.06)
        Debug_Var=11;
```

```
        flag_1=2;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=1;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
    end
       if 0.94*Vin<=FBpin && FBpin<=(Vin/(1-0.06))
        flag_1=10;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=1;
       end
         if Vin<1
            flag=0;
            flag_1=0;
         end
end
%%
% State flag=1, flag_=2 defines Boost Operation from A-->B

if flag==1 && flag_1==2
        Debug_Var=7;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=1;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
       if 0.94*Vin<=FBpin && FBpin<=(Vin/(1-0.06))
        flag_1=10;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=1;
       end
       if FBpin<0.94*Vin
        Debug_Var=10;
        flag_1=1;
        Buck_norm=1;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
       end
      if FBpin>Vin/(1-0.06)
        Debug_Var=11;
        flag_1=2;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=1;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
      end
```

```
         if Vin<1
            flag=0;
            flag_1=0;
         end
end

% State flag=1, flag_=10 defines Buck-Boost Operation from A-->B
if flag==1 && flag_1==10
    Debug_Var=9;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=1;
    if FBpin<0.94*Vin
        Debug_Var=10;
        flag_1=1;
        Buck_norm=1;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
    end
    if FBpin>Vin/(1-0.06)
        Debug_Var=11;
        flag_1=2;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=1;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
    end
         if Vin<1
            flag=0;
            flag_1=0;
         end

end

% State flag=2, flag_=3 defines Buck Operation from B-->A
if flag==2 && flag_1==3
        Buck_norm=0;
        Buck_Rev=1;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
       if 0.94*Vout<=FBpin && FBpin<=(Vout/(1-0.06))
        flag_1=11;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost_Rev=1;
   end
     if FBpin<0.94*Vout
        Debug_Var=10;
        flag_1=3;
        Buck_norm=0;
```

```
        Buck_Rev=1;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
     end
    if FBpin>Vout/(1-0.06)
        Debug_Var=11;
        flag_1=4;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=1;
        balance=0;
        BuckBoost=0;
    end
       end
        if Vout<1
            flag=0;
            flag_1=0;
        end
end

% State flag=2, flag_=4 defines Boost Operation from B-->A
if flag==2 && flag_1==4
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=1;
        balance=0;
       if 0.94*Vout<=FBpin && FBpin<=(Vout/(1-0.06))
        flag_1=11;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost_Rev=1;
       end
       if FBpin<0.94*Vout
        Debug_Var=10;
        flag_1=3;
        Buck_norm=0;
        Buck_Rev=1;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost=0;
       end
    if FBpin>Vout/(1-0.06)
        Debug_Var=11;
        flag_1=4;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=1;
        balance=0;
        BuckBoost=0;
    end
        if Vout<1
            flag=0;
            flag_1=0;
```

```
        end

end

% State flag=2, flag_=11 defines Buck-Boost Operation from B-->A
if flag==2 && flag_1==11
    Debug_Var=9;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost_Rev=1;
    if FBpin<0.94*Vout
        Debug_Var=10;
        flag_1=3;
        Buck_norm=0;
        Buck_Rev=1;
        Boost_norm=0;
        Boost_Rev=0;
        balance=0;
        BuckBoost_Rev=0;
    end
    if FBpin>Vout/(1-0.06)
        Debug_Var=11;
        flag_1=4;
        Buck_norm=0;
        Buck_Rev=0;
        Boost_norm=0;
        Boost_Rev=1;
        balance=0;
        BuckBoost_Rev=0;
    end
         if Vin<1
            flag=0;
            flag_1=0;
         end

end

else         % the algorithm wait until the boundary conditions are
met
flag=0;      % if the boundary conditions are not met the state
machine variables reset in every loop
flag_1=0;
Buck_norm=0;
Buck_Rev=0;
Boost_norm=0;
Boost_Rev=0;
balance=0;
BuckBoost=0;
BuckBoost_Rev=0;
end


flagi=flag;         %the state machine variables are carried to the
next loop
flagi_1=flag_1;
DBG=Debug_Var;
end
```