DC Protection System Testing in RTDS-MATLAB Simulation Environment

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MASTAR OF SCIENCE THESIS

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Abstract

Testing of protection schemes is important before it can be used for an actual topology. Nowadays, DC protection has not readily been designed and implemented in power systems. Therefore, due to high requirements on DC fault interruption, the designing and testing the corresponding DC protection with the use of a DC circuit breaker (DCCB) becomes a challenge. In this thesis, a four-terminal meshed VSC-MMC HVDC system is developed in RTDS environment. Diverse fault tests, concerning different fault types, fault locations and fault impedances are conducted in a remote testing way. The MATLAB-based testing controller by a remote computer will command the local computer and the RTDS-modelled system through the communication network, in order to automatically run all test scenarios and do data processing. The related testing results demonstrate the DC fault dynamics in an effective way in order to test DC protection. In order to do this a refined DCCB model has been developed.

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List of Acronyms

1. **LCC-HVDC** (Line-commutated converter based HVDC)
2. **VSC-HVDC** (Voltage-source converter based HVDC)
3. **MMC** (Modular multilevel converter)
4. **DCCB** (Direct current circuit breaker)
5. **ACCB** (Alternating current circuit breaker)
6. **RTDS** (Real time digital simulation)
7. **RSCAD** (Real-time simulation Computer Aided Design)
8. **PSACD** (Power Systems Computer Aided Design)
9. **FB Cell** (Full-bridge cell)
10. **HB Cell** (Half-bridge cell)
11. **SM** (Sub-module)
12. **IGBT** (Insulated-gate bipolar transistor)
13. **FSPS** (Fully selective protection strategy)
14. **PSPS** (Partially selective protection strategy)
15. **MAD** (Median absolute deviation)
16. **PB5** (Name for one of the parallel processor cards in RTDS)
17. **HIL** (Hardware-in-the-loop)
18. **TCP** (Transmission Control Protocol)
19. **IED** (Intelligent Electronic Device)
20. **IArres** (The branch current flowing through the surge arrester in DCCB)
21. **S1CRT** (The branch current flowing through the main interrupter in DCCB)
22. **IS3A2** (The branch current flowing through the capacitor in DCCB)
23. **S2CUR** (The total current flowing through DCCB)
24. **TVR** (Transient over-voltage)
25. **IND** (Indices)
26. **ACBRK** (Name of trip signals sent to ACCBs)
27. **DBLK** (Name of blocking signals sent to MMCs)
28. **Ptp-fault** (Pole to pole fault)
29. **Nptg-fault** (Negative pole to ground fault)

Contents

Chapter 1

Introduction

1.1 Background

Since the first alternating current (AC) power system was built in Great Barrington, Massachusetts in 1880s [1], AC transmission has dominated in the electrical power system for more than 100 years. In that famous war of the currents, direct current (DC) loses for not being able to transform voltage easily compared with AC transformers [2]. From the years around 2000, DC transmission gained people's attention once again due to the development of micro-grid and involvement of renewable energy [3]. With the revolution of the power converters, high voltage direct current (HVDC) transmission will save much more power than AC transmission over long distance [4]. This is an remarkable advantage to transfer remote renewable energy to the main grid or the local micro-grid. The world's first commercial HVDC system was built in 1954 for connecting the Swedish mainland and the island Gotland [5]. And here Fig 1.1 shows other important milestones of HVDC system before 2000 [6].

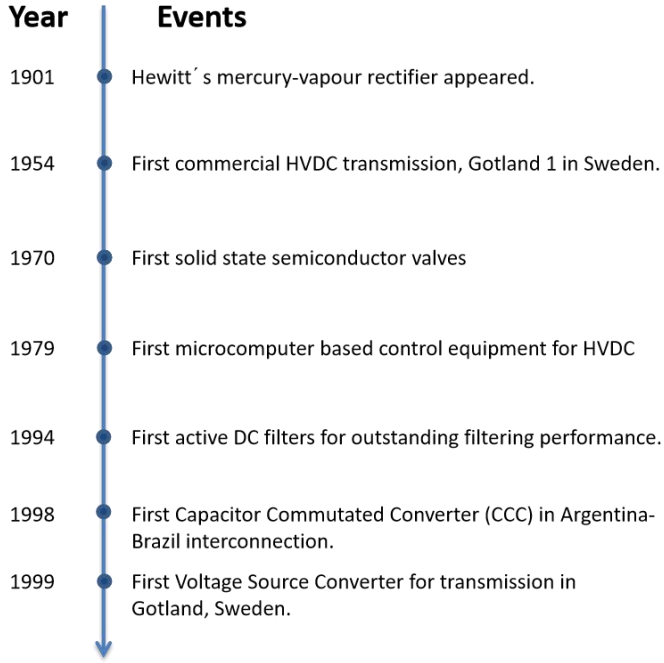


Figure 1.1: *Milestones in HVDC history*

As the first voltage source converter (VSC) was applied for transmission in 1999, a rapid increasing usage of VSC took place in the HVDC system from 2000. Till the 21st century, there are more than 200 HVDC systems operating around the world with more new HVDC projects being initiated [7]. Table 1.1 lists three cases of the VSC-based HVDC projects and their motivations [8].

Project name	Year of commissioning	Power ratings	DC voltage	Reasons for choosing VSC-HVDC	Converter topology
Eagle Pass, USA	2000	36MW	±15.9 kV	Controlled asynchronous connection for trading. Voltage control. Power exchange.	3-level
Troll A offshore, Norway	2005	84MW	±60 kV	Environment, CO2 tax. Long submarine cable distance. Compactness of converter on platform electrification.	2-level
Trans Bay Cable, USA	2010	400MW	±200 kV	Provide reliable energy to San Francisco without having to install a power generation plant.	MMC

Table 1.1: *Example cases of HVDC projects from 2000 to 2010*

From 2000 to 2010, the power rating of HVDC systems increases dramatically. The reasons for installing includes power exchange, long submarine power transmission, renewable energy penetration. Converter topology also develops from 2 and 3 levels to multi-levels. Now, the biggest HVDC system is china with a total length of 3,293 kilometers, a rated

voltage of ±1,100 kV and transmission capacity of 12 GW [9].

Predictably, the capacity size of HVDC system in the electrical system market will keep increasing partly because of the revolution of the converters. And partly because the renewable energy is penetrating into the energy market so fast and plays a more important role than before [10].

Although the HVDC system is developing so fast, there is not a globalized fault protection standard in HVDC systems [11]. Faults in the HVDC system include AC side faults, DC side faults and converter faults. DC side faults are the most significant faults which can inject extremely high fault current within milliseconds [12]. This makes DC fault current characteristic unique from AC fault current. As a result, the corresponding detection algorithm should be redesigned. Apart from that, another big issue is the DC fault interruption. There is no natural zero-crossing of fault current in a HVDC system, which makes the direct current circuit (DCCB) difficult to make [13]. Because of these two factors, DC fault protection are not easy to implement.

The latest methods so far for DC line protection includes voltage derivative protection, travelling wave protection, current differential protection and DC voltage level protection [14]. However, this thesis will investigate a novel relay algorithm 'MAD', stands for median absolute deviation in DC fault detection [15]. By implementing the fault test simulation on the RTDS platform, the performance of 'MAD' are discussed.

In HVDC systems, the protection strategy also varies in different regions. This also makes DC protection standard hard to set. According the Cigre Working Group B4/B5-59, DC fault protection can be divided into three types, fully selective, partially selective and non selective [16]. This thesis will discuss all of the three protection strategies and implement fault tests on the fully selective protection and partially selective protection.

1.2 Objective

The thesis focuses on the HVDC system protection. Based on an novel algorithm, the protection tests on cable faults are mainly studied. The test platform is RTDS (real time digital simulation). The main objectives are:

- Introduce a novel protection algorithm and test its detection performance of cable faults in HVDC systems.

- Implement the fully selective protection strategy (FSPS) on the prototype meshed 4 terminal HVDC system in the platform RTDS. Study the transient fault current characteristics and DCCB operation on interrupting the faults.

- Design one of the partially selective protection strategy (PSPS) and implement the fault

test in the RTDS platform. Compare PSPS and FSPS in terms of protection zones, fault-clearing effects to the rest of the system.

- Investigate how various fault parameters including fault impedance, fault location and fault type, will affect the fault current. And how they affect the fault detection.

- Investigate how the algorithm thresholds setting will affect the fault detection range. And how they further affect the HVDC protection characteristics.

1.3 Thesis Structure

The chapters of thesis are organized as follows.

- **Chapter 2** introduces a four-terminal meshed HVDC system structure including its components. First of all, the system model is generally stated. Then the main components in the system including such as circuit breakers, Multi-level modular converters are discussed one by one. This chapter describes the function of all the HVDC system components. For extremely important components, the model structures with their parameters in RSCAD are illustrated.

- **Chapter 3** introduces three different protection strategies in HVDC system, the fully selective protection strategy (FSPS), the partially protection strategy (PSPS) and the non-selective protection strategy (NSPS). During each protection strategy, the operation unit and protection zones are stated. For FSPS, it requires faulty cable being interrupted accurately. For PSPS, there are multiple methods which can meet the protection requirement. Three of them are described in terms of different protection preference. For NSPS, the entire DC network will shut down whenever the fault is located. The fault in NSPS impacts most on the HVDC system.

- **Chapter 4** firstly introduces the basic theory of relay algorithm. Then, it discusses the detection threshold determination in a range of faults parameters. After that, the mechanism of ACCB operation and DCCB Blocking is discussed. At last, Chapter 4 investigates how PSPS and NSPS are achieved by cooperation of DCCB operation, ACCB operation and MMC blocking.

- **Chapter 5** introduces the simulation environment of the entire HVDC system protection tests. It firstly tells on which software and hardware the test model is built and run. Then, it tells how MATLAB can remotely communicate with simulation hardware. At last, the chapter discussed the objectives of fault simulation.

- **Chapter 6** studies the fault cases on FSPS. Before the test, a description on time step and threshold setting for relay algorithm is stated. Then, it follows by the base case study,

where important current and voltages are analyzed. After that, more cases study are investigated and compared. From that, how the fault parameters will affect the fault transient is generally concluded.

- **Chapter 7** studies the fault cases on PSPS. Before the test, a description on time step and threshold setting for relay algorithm is stated. Then, it follows by the base case study, where important current and voltages are analyzed. After that, more cases study are investigated and compared. Among of them, the false operation of ACCBs and false relay detection happens occasionally. Last but not the least, a radar chart is give to illustrate the fault detection range and possible inappropriate reactions from devices. Finally, the thresholds effects on fault detection is concluded.

Chapter 2

A meshed VSC-HVDC Grid Based Test System

This chapter introduces a four-terminal meshed HVDC system structure including its components. First of all, the system model is generally stated. Then the main components in the system including such as circuit breakers, Multi-level modular converters are discussed one by one. This chapter describes the function of all the HVDC system components. For extremely important components, the model structures with their parameters in RSCAD are illustrated.

2.1 Introduction

Compared with the line-commutated converter based HVDC (LCC-HVDC) system featured as high capacity and efficiency [17], the voltage-source converter based HVDC (VSC-HVDC) system is superior in interconnecting weak AC systems and various renewable energy source [18]. The VSC-HVDC system can operate with a blackstart, which is not allowed for the LCC-HVDC system without auxiliary equipment. A meshed circuit structure provides more redundancies than radial and looped network, which improves the reliability and robustness [19]. The meshed topology integrates scattered converter stations nearby and offers multiple market strategies in load distribution. In addition, HVDC transmission are widely utilized around offshore wind farms, where the wind power generation varies constantly. The increasing interconnecting between substations ensures enough primary and secondary power reserves when faced with the resulting power fluctuations [20]. The testing system in this

thesis has four terminals with one of them functions as a slack bus, which connects external AC grid and the internal HVDC system. Thus, a meshed VSC-HVDC Grid Based test system is formed.

The test system is a four-terminal DC meshed system, with each bus connected with a local generator or load through a modular multilevel converter (MMC). The modular multilevel converter is composed by half-bridge modules. In this case, there is always a path for current flowing through each power modules even if transistors are switched off. Transformers in the AC side are applied to adjust the local AC grid voltage level to a unified secondary voltage, 220kV. After that, this AC current is transformed to 200kV DC current though MMCs. As figure 1 shows, four terminals are named as A1, A2, C1 and C2. In this meshed DC system, each branch has two direct current circuit breakers (DCCB) placed on each end. All the branches (A1C1, A1A2,A2C2,C1C2) are given a length of 200km. The purpose of the project is to first analyze the fault transient on different fault conditions, and then test whether the DCCB model is able to operate properly. This HVDC system is designed and complied on the software 'RSCAD'. By communication, the file is downloaded to the RTDS (real time digital simulation) device, and simulated on RTDS platform [21]. Four consistent racks with 16 PB5 cards in total are occupied during each simulation [22].

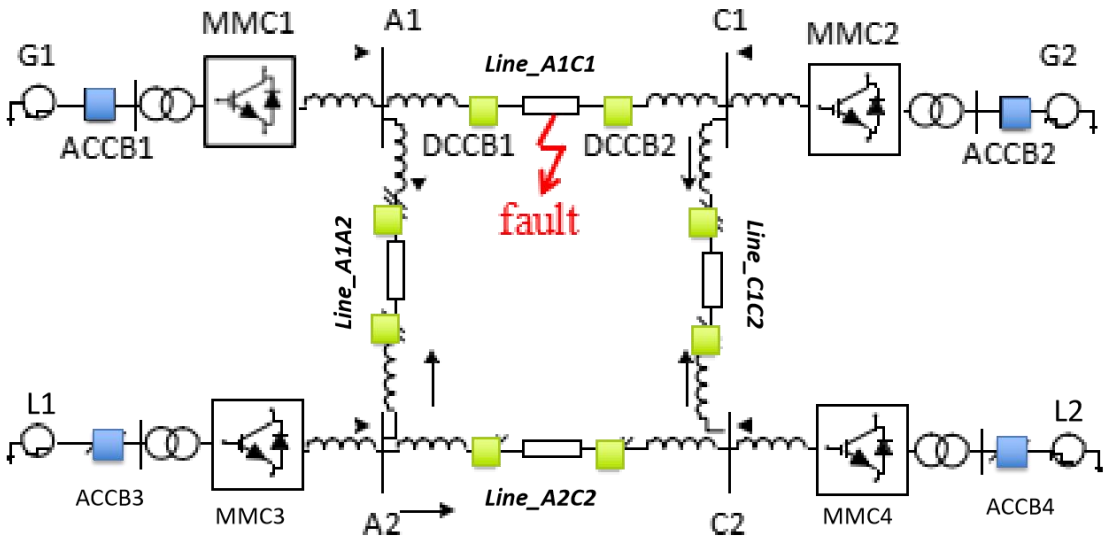


Figure 2.1: *Test DC meshed system*

2.2 Direct current circuit breaker (DCCB)

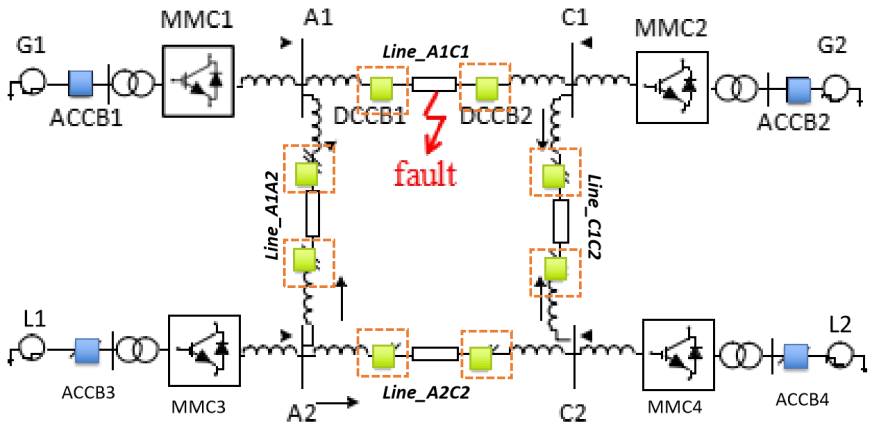


Figure 2.2: *DCCBs in the test DC meshed system*

The difficulties of DCCB design are mainly caused by the lack of current zero crossing. Traditional AC breaker could interrupt the arc when the alternating current goes across zero. However, the current zero crossing rarely happens in a DC system, which makes the current interruption a big challenge. In the test system, a mechanical type DCCB model with a reversal current injection has been designed [23]. The diagram of a system level model is shown in Fig 2.1.

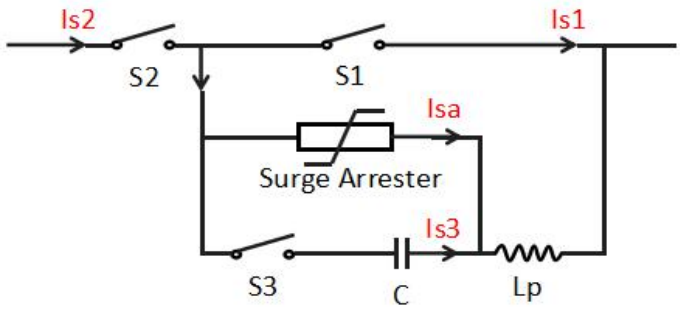


Figure 2.3: *DCCB model structure*

This model consists three branches. The first branch is the main circuit breaker branch, Is1 is the current flowing through the high speed vacuum interrupter S1. The second branch is the branch for energy dissipating, Isa is the branch current going through the surge arrester. The last branch is a resonant circuit, also called current injection circuit. The aim of this branch is to generate a current pulse with sufficient magnitude so that multiple current zeros could be made. The magnitude and frequency of the discharged current depends on the capacitance C, the inductance Lp and the pre-charge voltage.

Normally, S2 and S1 are in closed state. S3 is in open state. Once a fault takes place, the main switch S1 would be firstly opened with 8ms mechanical delay after the trip-signal is generated. Meanwhile, S3 would close for counter current injection. It is very important that, during the mechanical delay the fault current should never increase up beyond the interruption ability of S1. After the fault current is successfully commuted, Is2 will decline to zero in a rate. This rate depends on the parameters of the surge arrester as well as the

resonance branch. During this period, the voltage across the DCCB rapidly increases. The voltage increasing rate is mostly related to the characteristic of the surge arrester. In practice, numbers of surge arresters are be placed in parallel to do energy dissipating. As the current drops to zero, S2 is open which means the fault is cleared.

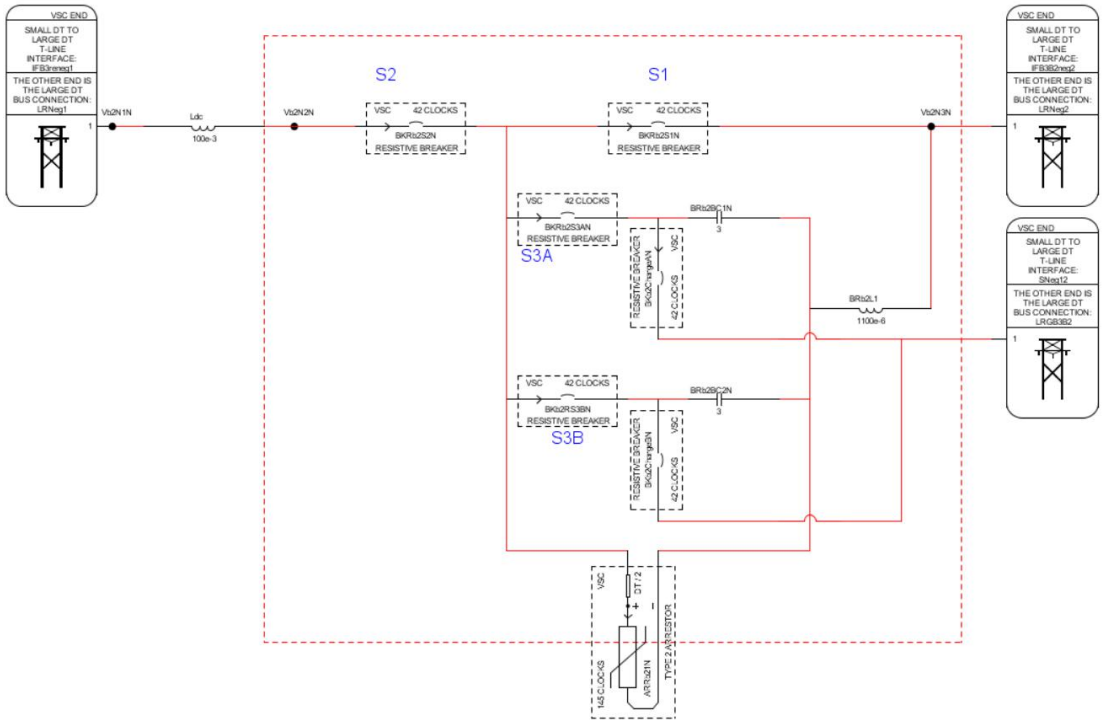


Figure 2.4: *DCCB model in the platform RSCAD, applied in both small step and normal step*

Fig 2.4 demonstrates one of the DCCB models built in the simulation platform RSCAD. As can be seem, there are more than one resonant branch (S3A and S3B) parallel connected in the real model than the theoretical model in Fig 2.3. One of the purpose of doing this is to speed up the time when the generated oscillating current I_{S1} crosses zero. Another reason is that multiple current zeros are expected to be created in case S1 fails to interrupt in the first zero-crossing. The parameters of the inductance L_p and the capacitance C_A and C_B are shown in Table 2.1. The parameter of the surge arrester is shown in Fig 2.5.

L_{dc}	C_A	C_B	L_p
100mH	3μF	3μF	1.1mL

Table 2.1: *DCCB components parameters*

rtds_vsc_ARR2

GTAO D/A CHANNEL ASSIGNMENTS | SIGNAL NAMES FOR RUNTIME AND D/A
ENABLE GTAO D/A OUTPUT | FACEPLATE D/A CHANNEL ASSIGNMENTS
ENABLE MONITORING IN RUNTIME AND CC | ENABLE FACEPLATE D/A OUTPUT
ARRESTOR PARAMETERS | FORCE VSC INTERNAL NAMED SIGNAL ON PROCESSOR
VSC Type 2 Arrestor Configuration | HALF-STEP INTERFACE T-LINE PARAMETERS

Name	Description	Value	Unit	Min	Max
Npwr	N in Curve Eqn: I=Id*{ (V/Vd)**N }	16		2	32
Idis	Discharge Current, Id (crest) :	18.8	kA	0.1	
Vdis	Discharge Voltage, Vd (crest) :	512.2	kV	0.1	
Rmin	Rmin in Units: Incremental R at Disch.	0.25	units	0.25	2.0
ArTc	Arrestor Energy Decay Time Constant:	10.0	Sec	0.00001	1000.0
snbC	Arrestor snubber capacitance C:	0.0001	uF	0.0001	100.0
snbR	Arr snubber res R (RC >= small DT/2):	1.0	Ohms	0.0	10000.0
prlr	Resistance parallel to arrestor:	1.0e6	Ohms	0.1	1.0e10

Update | Cancel | Cancel All

Figure 2.5: *Parameters of arrester in DCCB*

2.3 Multi-level modular converter(MMC)

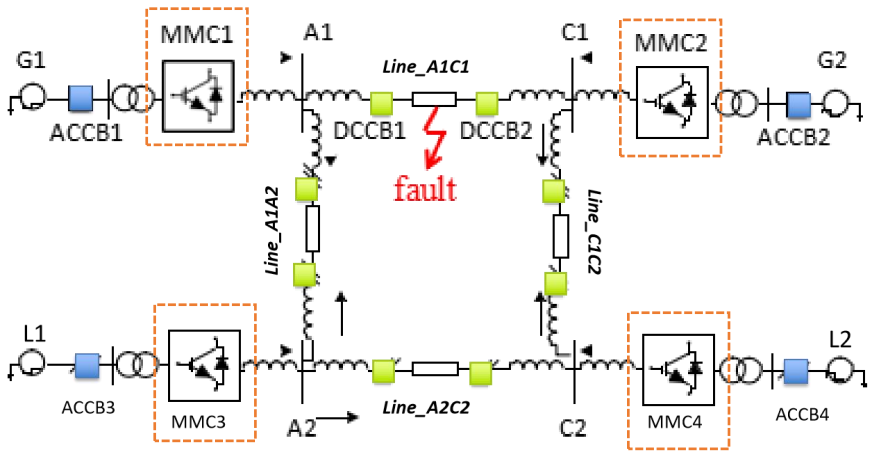


Figure 2.6: *MMCs in the test DC meshed system*

Multi-level modular converter is used to transfer a big amount of electrical power between AC system and DC system. This type of converter is typically applied in HVDC system. MMC usually has two topologies, the full bridge structure and the half bridge structure as shown in Fig 2.7.

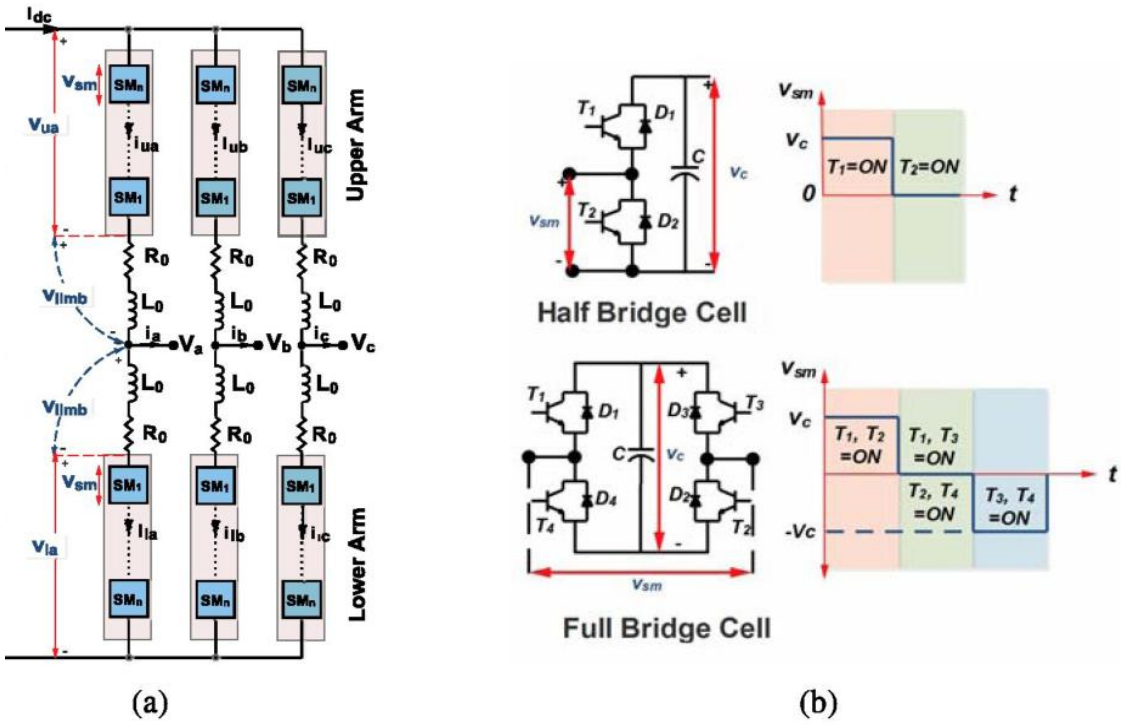


Figure 2.7: *The MMC structure with two types of sub-modules, HB Cell and FB Cell*

In subplot (a), three arms are connected to three separate phases, phase a , phase b and phase c. Each arm is made up of several series connected sub-modules. They could be in type of either half bridge cells or full bridge cells [24]. With half bridge cells, there is always a current path via the diodes even if transistors are forced being blocked. In other words, in the case of a dc fault, the fault current flows uncontrollably through the cascading free-wheel diodes. For a full-bridge structure, the submodules are able to quickly block dc fault current since there are no available current paths during DC faults.

The voltage level V_a, V_b and V_c at the midpoint of each phase-leg, are defined by the number of SMs that are connected in the upper and lower arms of the converter. As can be seen in subplot (b), a HB cell can only produce two different states of voltage, either $+V_c$ or 0. While, a FB cell can produce tree states of voltage, $+V_c$, 0 and $-V_c$. This offers more flexibility and possibilities in switch modulation. Different SM topologies do make different reactions when encountering a DC fault. For HB cells, both IGBTs T_1 and T_2 are switched off, the anti-parallel diodes provides path for arm currents. The capacitor is firstly charged to the voltage level V_c and then bypassed when currents flow out of HB cells. For FB cells, all IGBTS are switched off, the capacitor is charged in either positive direction or negative direction depending on the current direction [25].

There are following salient features which makes MMCs outstanding and especially applicable in HVDC systems [26]:

- Modular structure makes it easy to meet desired voltage output by adding or removing

the cascading sub-modules.

- Capacitances are embedded in each sub-module instead of a DC-link capacitor
- Voltage balancing of each sub-module and high-speed commutation could be potential risks
- Bunches of SMs leads to a more complex control strategy compared with a 2-level converter

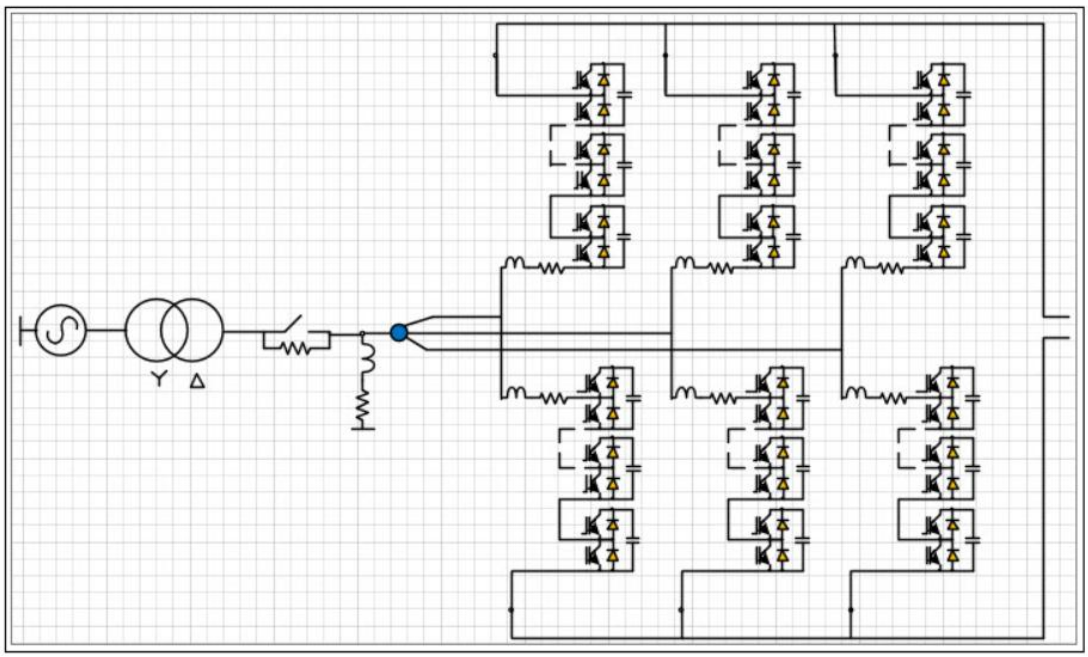


Figure 2.8: *The MMC structure built in the platform RTDS*

Fig 2.8 illustrates a general frame of the MMC model built in the platform RTDS.

2.4 Generators and loads

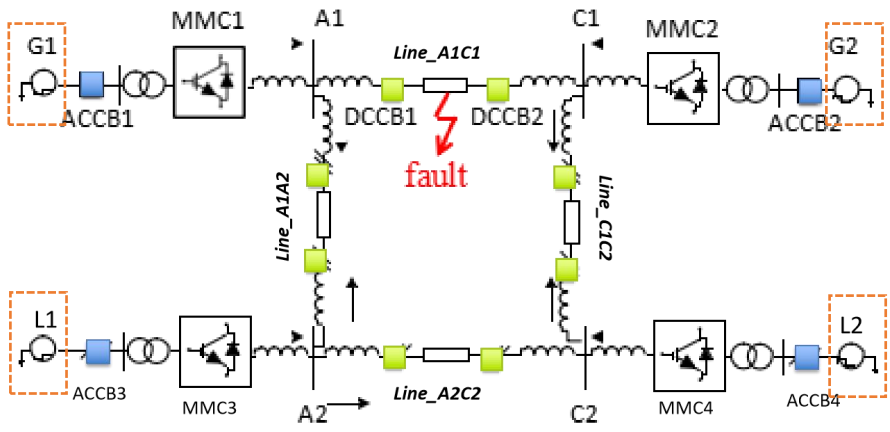


Figure 2.9: *Loads and generators in the test DC meshed system*

The test HVDC system has four MMCs connected to fours AC sources. Among these AC sources, there are two generators G1 and G2 located at A1 and C1 separately. The other two are the loads L1 and L2 located at A2 and C2 separately. Each source has its own control strategy to make them play their own roles. G1 works as an slack bus supplying or drawing power according to the other sources' reference setting. The other three G2, L1 and L2 are in P/V controlled mode. L1 and L2 are set to draw 300MW power and G2 are set to supply 700MW power under normal situation. These reference settings only dominates the power flow in normal operation. As a fault is injected, the fault currents drawn from each AC sources are determined by the transient parameters.

2.5 Alternating current circuit breakers (ACCB) and transformers

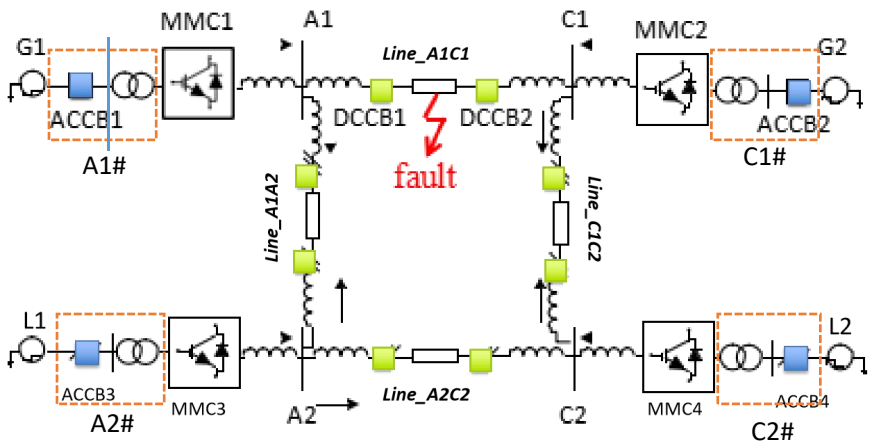


Figure 2.10: *ACCBs and transformers in the test DC meshed system*

Between each AC source and its corresponding MMC station is connected with an alternating current circuit breaker(ACCB) and a three phase transformer. The ACCB is equipped for isolating the AC source form the whole DC system in non-selective protection scheme or providing a back-up when DCCBs fails to operate [27]. The local AC primary side voltage may differs due to different grids voltage and user needs. The transformer is to converter the voltage to an unified value in the secondary side. Thus, the DC system will share an constant DC voltage at each terminal after MMC conversion. The frame of ACCB and transformer at A1 branch are shown in Fig 2.11. The overall parameters of four transformers are indicated in Tab 2.2.

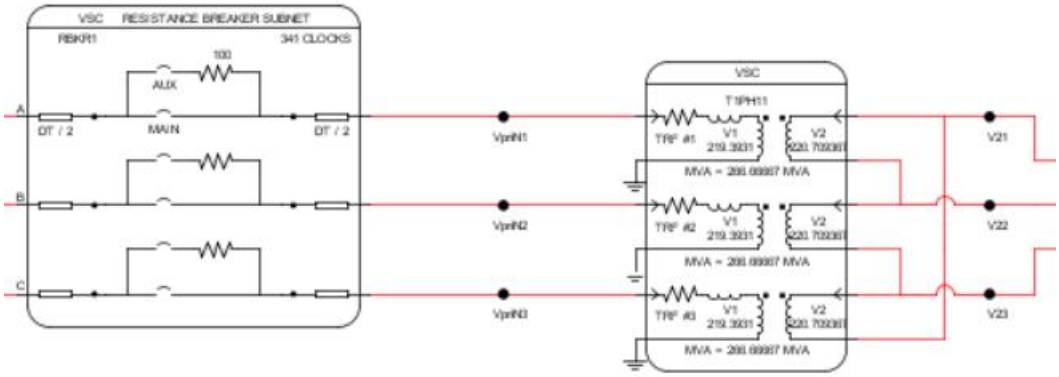


Figure 2.11: *ACCBs and transformers at A1 branch built in the platform RTDS*

AC system		
bus name	Voltage	Transformer ratio
A1#	380kV	380*95%/231.58
A2#		380*95%/231.58
C1#	145kV	145*95%/231.58
C2#		145*95%/231.58

Table 2.2: *Transformer parameters*

The '#' symbol in 'A1#' means the primary AC side in branch A1. 'A1#' and 'A2#', the generator side has the same primary AC voltage of 380kV. While 'C1#' and 'C2#', the loads side has a lower voltage level of 145kV. But the secondary side for each AC bus is fixed at 231.58*95% = 220kV.

2.6 Current limiters

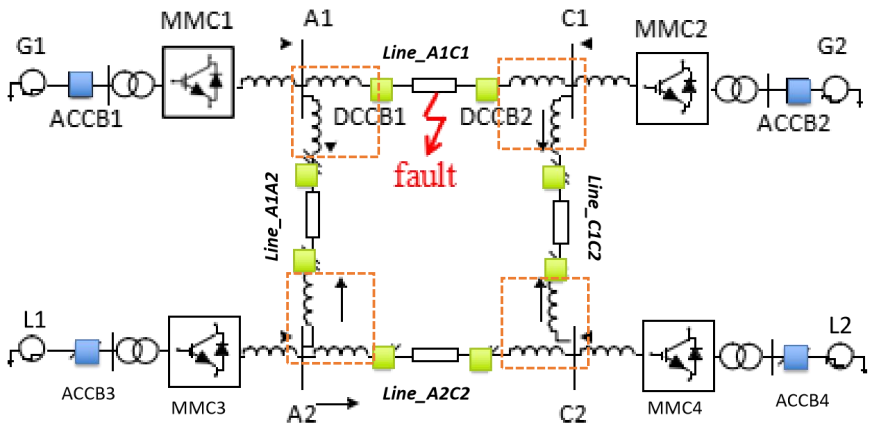


Figure 2.12: *Current limiters in the test DC meshed system*

The inductors in the ends of cables play significant roles in DC system protection, known as current limiters. First of all, their existence prevents the DC fault current from increasing too rapidly, which gives a rise of damages to system components. Second, their existence makes current surges and voltage drops vary in different cables, which further provides detection criterion in relay algorithm [28]. In the RTDS model, the inductance as the current limiter is set to be 0.01H.

Chapter 3

Protection schemes and principles in the test HVDC system

This chapter introduces three different protection strategies in HVDC system, the fully selective protection strategy (FSPS), the partially protection strategy (PSPS) and the non-selective protection strategy (NSPS). During each protection strategy, the operation unit and protection zones are stated. For FSPS, it requires faulty cable being interrupted accurately. For PSPS, there are multiple methods which can meet the protection requirement. Three of them are described in terms of different protection preference. For NSPS, the entire DC network will shut down whenever the fault is located. The fault in NSPS impacts most on the HVDC system.

3.1 Introduction

In terms of protection objects, there are two protection philosophies in the power system called ‘unit protection’ and ‘non unit protection’. The unit protection usually works for an specific equipment or a relatively small but important areas called protection zones. The examples for unit protection are protections for transformers, generators, transmission lines, etc. Unit protection involves comparison of quantities at the boundaries of the protected zone as defined by the locations of the current transformers . This comparison may be achieved by direct hard-wired connections or may be achieved via a communication link. For example, the differential protection. The drawbacks would be that, the speed of response is substantially independent of fault severity [29]. The non unit protection only collects the

local information and process, so that the implementation of fault detection is rather faster than unit protection [30]. This makes the non unit protection appropriate for HVDC protection system, since the fault current increases incredibly fast in HVDC system. The non unit protection react to the fault according to the fault severity. For instance, Time graded over-current protection, Current graded over-current protection and Distance or Impedance Protection.

In this HVDC protection system, non unit protection is applied for the DCCB relays located in cables. Relays only collect local electrical information and process separately. The trip signal then is sent to the corresponding DCCB nearby, which cuts off the cable at that place. According to the DCCB placement, there are three protection schemes for HVDC systems. They are fully selective,partially selective and non selective protection [16]. Among these protection schemes, different modes of coordination are needed between protection devices.

3.2 Fully selective DCCB placement

Fully selective DCCB placement requires adequate number of DCCBs located in each end of cables. And the prototype model based on the fully selective protection scheme. As faults happen in cables, of which DCCBs should operate [31]. Meanwhile, ACCBs should not operate and MMCs should not block itself. In this mode, the impact of protection operation is of the least severity with only the fault cable being isolated. Four AC sources will still work although the power flow is rearranged after fault-interruption.

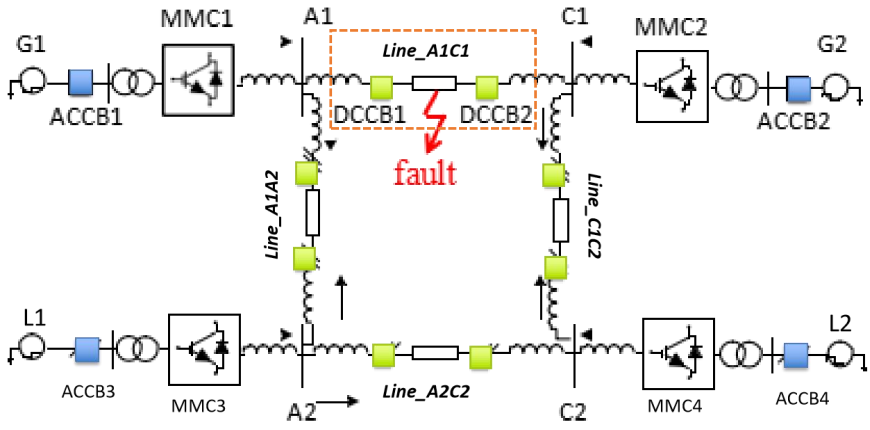


Figure 3.1: *Pre-fault HVDC system*

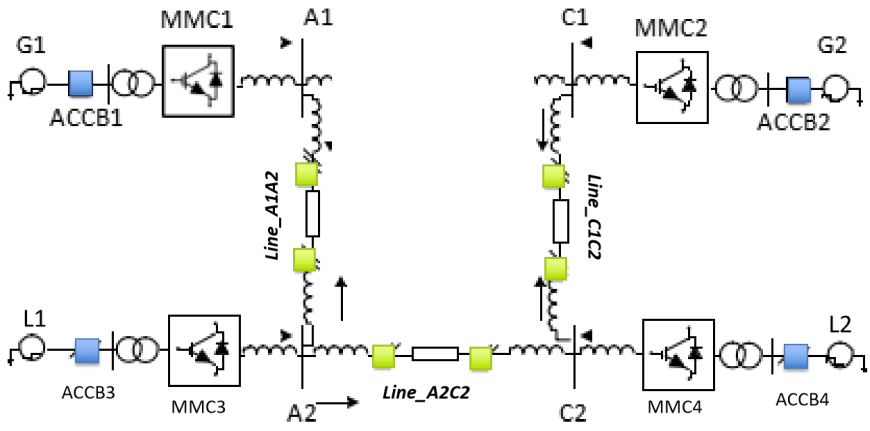


Figure 3.2: *HVDC system after fault-interruption*

3.3 Partially selective DCCB placement

Partially selective DCCB placement is recommended and implemented when there is limited number of DCCBs. This situation happens because DCCBs are huge in space and quite expensive in the real life. As faults happen in cables, more than one cables are disconnected. This means not only the fault cable will be cut, but also at least one healthy cable will be cut. In addition, it is likely that AC sources will be switched-off when necessary. In this mode, the impact of protection operation is of the middle severity since it affects some healthy areas. The design of partially selective can vary when the considerations lay in different aspects. For example, particular protection zones, minimum number of DCCBs, preferred reserved AC sources and etc [32]. The establishment of a protection strategy also leads to the number of DCCBs that are needed and where they are placed.

a. Example of partially selective protection design in terms of a particular protection zone

Suppose two loads area 'L1' and 'L2' are the protection zones which are preferred to reserve. Wherever the fault is located, loads 'L1' and 'L2' should never be switched off. In the real life, this strategy can be used for protecting important consumers. Based on the assumption, five DCCBs are required and one of the DCCBs arrangements is shown in Fig 3.3.

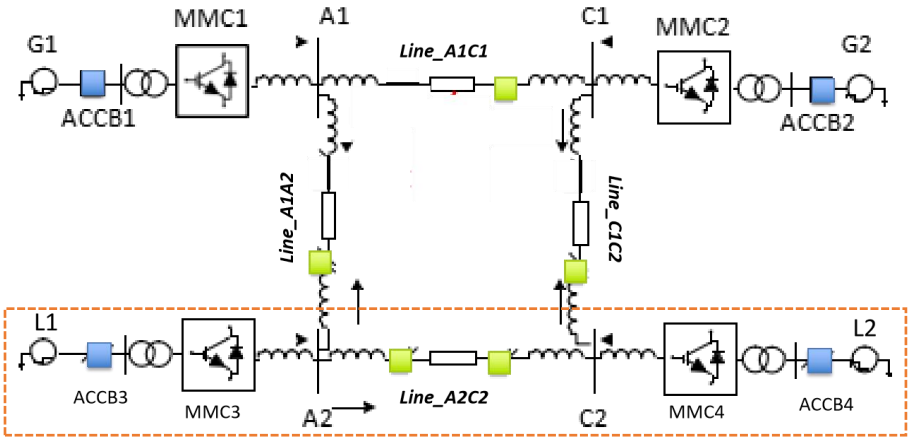
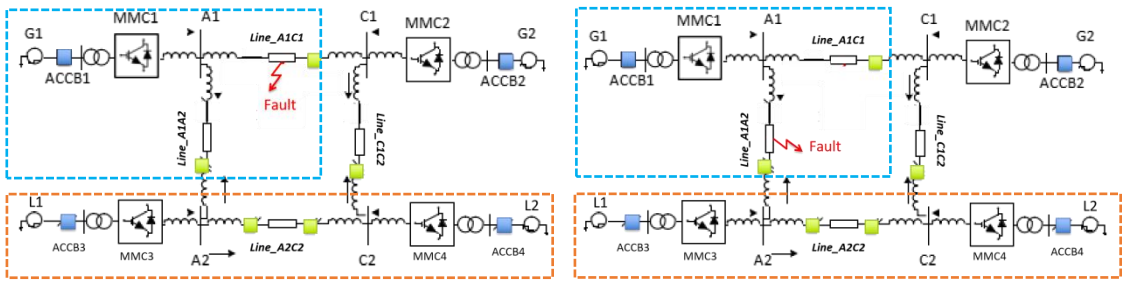
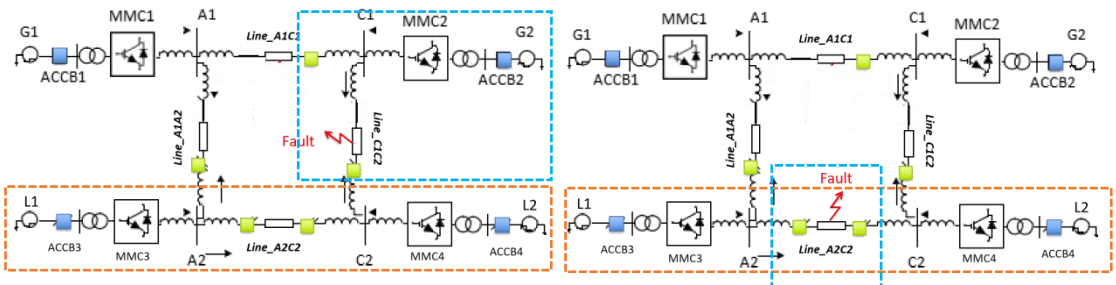


Figure 3.3: *DCCB placement in option a of partially selective protection*



case (a): *fault at 'Line_A1C1'*

case (b): *fault at 'Line_A1A2'*



case (c): *fault at 'Line_C1C2'*

case (d): *fault at 'Line_A2C2'*

Figure 3.4: *Situations when faults happen at different cables*

Fig 3.4 illustrates all the possible situations where faults can happen. Inside the rectangular frame of blue dotted lines is the isolated area after fault-clearing. While inside the rectangular frame of red dotted lines is the area to be reserved. For example, in the case of fault in 'line_A1C1', DCCBs in the fault cable 'line_A1C1' and adjacent healthy cable 'line_ A1A2' should operate. Besides, ACCB1 should also operate for drawing short circuit current from 'G1' to the fault position. After the fault is cleared, two loads 'L1' and 'L2' are still connected with the other generator 'G2' supplying the power. As can be seen, when the fault is in cable 'Line_A1C1', 'Line_A1A2' and 'Line_C1C2', at least one generator is switched off in addition to the cut-off of one adjacent healthy line. When the fault is in 'line A2C2', only the faulty cable is cut as it is done in fully selective protection scheme. The advantage of this partially selective DCCB placement is that loads are protected to the greatest extent.

b. Example of partially selective protection design in terms of minimum number of DCCBs

To make sure at most one AC source is isolated after fault-clearing, it requires at least four DCCBs in the example test system, i.e. one DCCB at each cable. Fig 3.5 demonstrates one of the DCCBs placements. Fig 3.6 shows the example fault case when the fault is in cable 'Line_A1C1'.

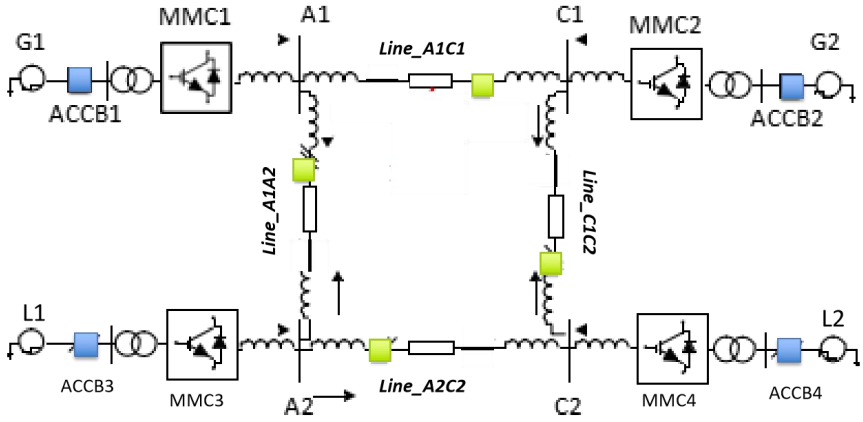
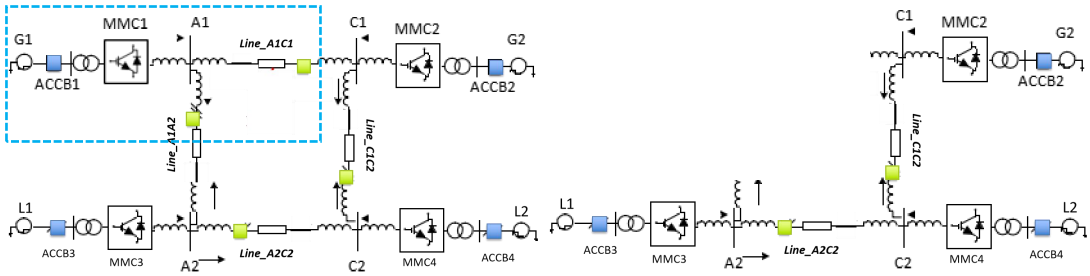


Figure 3.5: *DCCB placement in option b of partially selective protection*



Pre-fault situation *After-fault situation*

Figure 3.6: *Test system in pre-faul situation and after-fault situation*

As the fault happens at cable 'Line_A1C1', DCCBs at 'Line_A1C1' and 'Line_A1A2' operate. Meanwhile, generator 'G1' should be switched off from injecting the fault current. After the fault is cleared, there are still three AC sources working on. The fault leads to the faulty cable 'Line_A1C1', an healthy cable 'Line_A1A2' and generator 'G1' disconnected, a s it is shown inside the rectangular frame of blue dotted lines. This is the least impact that a fault can cause in the partially selective DCCB placement scheme. For faults located at the other three cables, it would be the similar protection strategy for disconnecting part of the DC systems.

c. *Example of partially selective protection design in terms of preferred reserved AC sources*

In a few HVDC systems in real life, a strong AC source is connected, i.e. grid connected mode. Three are also many other local renewable energy sources like wind power and hydro power, which are the main sources in the system. The AC grid usually works as an supplementary sources while the DC system can not self maintain by the local sources. When faults happen, AC grid is expected to be connected all the time while the local sources can

switch off. Because not only a strong source helps maintain the whole DC system voltage, but also it is able to supply all the loads in the DC system. In the test HVDC system, 'A1' is a slack bus, which means generator 'G1' can be seen as a strong source. Generator ' G2' supplies 700MW power in normal operation, which can be seen as the local sources. By adjusting DCCBs placement a little bit based on *Example.b,* a 'G1' protected partially selective protection scheme is illustrated in Fig [3.7].

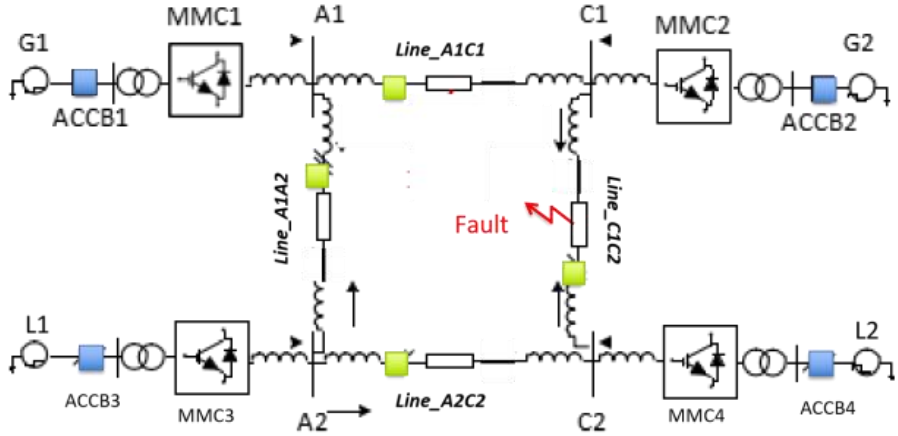
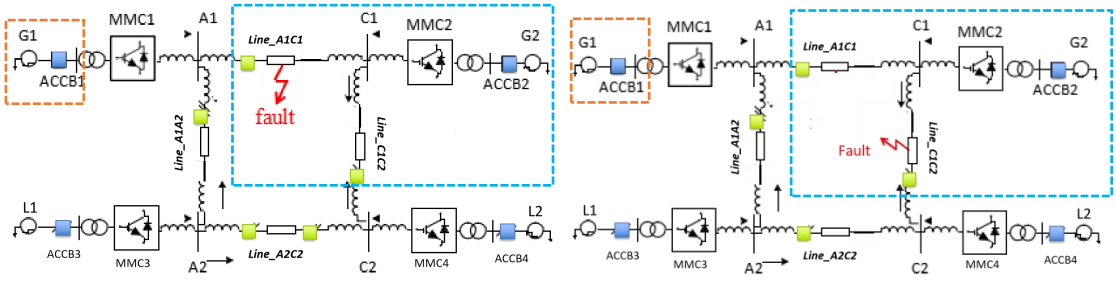
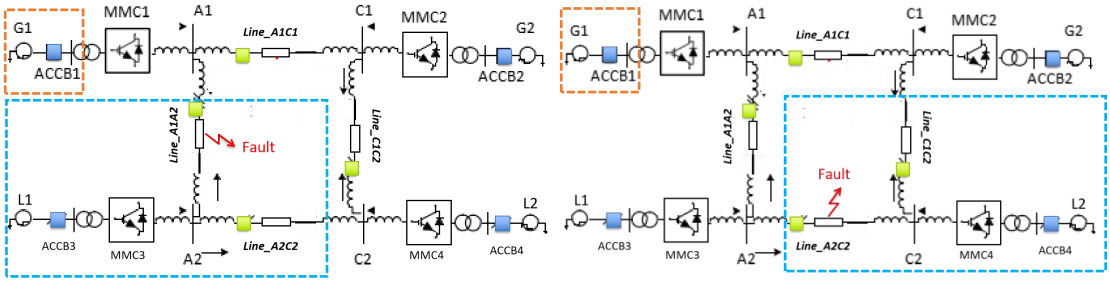


Figure 3.7: *DCCB placement in option c of partially selective protection*



case (a): *fault at 'Line_A1C1'* ***case (b):*** *fault at 'Line_A1A2'*



case (c): *fault at 'Line_C1C2'* ***case (d):*** *fault at 'Line_A2C2'*

Figure 3.8: *Situations when faults happen at different cables*

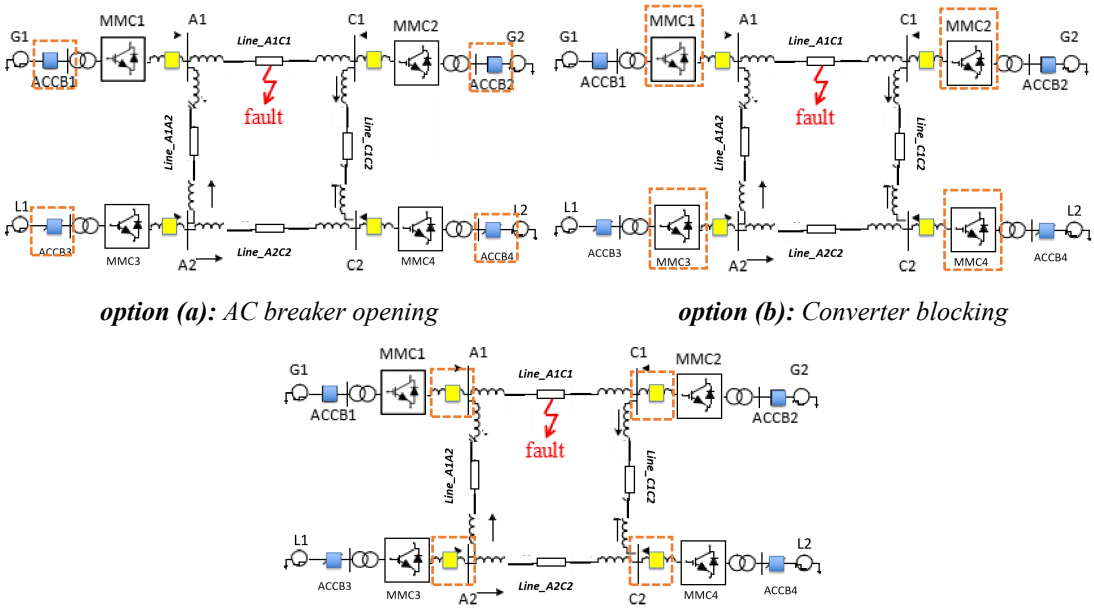
As the DCCB at cable 'Line_A1C1' is set close to 'G1', all the cable fault cases can not make 'G1' disconnected. When the fault is either on cable 'Line_A1C1' or 'Line_C1C2', the isolated area is the same, including 'G2'. When the fault is on the other two cables, there are at least one load disconnected.

In conclusion, at least four DCCBs are required for partially selective protection scheme in

the test HVDC system. The numbers of DCCBs and their placement can be very flexible. However, they always cater to the protection preference. To reserve a particular source, DCCBs on the adjacent cables should be set close to that source. If multiple sources are needed to reserve, then more than 4 DCCBs are required.

3.4 Non selective DCCB placement

In non selective DCCB placement protection scheme, the entire DC system is quickly de-energized from the moment of fault detection. And this de-energization period can be seen as the first stage in non selective DCCB placement protection. During de-energization, the fault is identified. The second stage can be, the DC switch isolate the faulty cable. The final stage is that, the healthy part of the DC system is restored by restart of converters [27][33]. The entire DC system's isolation can be achieved by variable methods. Here, the first stage is main part to discuss. There are three methods illustrated in Fig 3.9.



option (a): *AC breaker opening* ***option (b):*** *Converter blocking*

option (c): *DCCB at the MMC terminal opening*

Figure 3.9: *Three methods with different elements operation to de-energize the HVDC system*

In option (a), the operating elements are AC breakers. As any fault happens inside the HVDC system, all of the four ACCBs in the generators terminals should open temporarily to de-energize the system. The advantage of this method is that, no DCCBs at the MMC terminals are needed. The disadvantage is that, several cycles of the fundamental frequency are lost in all DC nodes. In option (b), the opening elements are DC converters. The benefit of this option is its quicker fault-clearing time, which accelerates system recovery. While, the drawback is that it depends on the MMC structure, i.e, the full-bridge MMC. Unfortunately,

the MMC model used in this test system is of half bridge type, although the option (b) is a good idea. In option (c), four extra DCCBs equipped at the converter terminals are the operating elements. This option has shorter DC grid outage time compared to option (a) and converters can deliver reactive power to the AC grid in case of DC faults.

Chapter 4

Description of the Relay algorithm and Analysis of different protection scheme

This chapter firstly introduces the basic theory of relay algorithm. Then, it discusses the detection threshold determination in a range of faults parameters. After that, the mechanism of ACCB operation and DCCB Blocking is discussed. At last, Chapter 4 investigates how PSPS and NSPS are achieved by cooperation of DCCB operation, ACCB operation and MMC blocking.

4.1 Introduction

For a DC protection system, the relay algorithm is always the core. A robust algorithm with a reliable method should detect the real fault as soon as possible while stand still to disturbances. Although the reliability, selectivity, sensitivity and speed usually can not be perfectly achieved, a good algorithm can reach to a reasonable trade-off in these four characteristics. Traditional relay algorithm for AC protection system may not applied in DC protection system for several reasons. One could be the DC fault current rapid increase needs faster detection than it is needed in AC system [34]. Also, the DC transient response during a fault differs from that in AC system, means a novel algorithm is expected. In this thesis, the median absolute deviation (MAD) method is applied and developed [15]. A successful fault detection signal will be sent to DCCBs for tripping. DCCBs, as the most direct protection

equipment for cables, are the closest to a line fault. As a result, they are the most essential fault-clearing devices, which claims a reliable relay algorithm to support. Besides, there are also auxiliary protection equipment which are called ACCB operation and MMC blocking. The conditions for ACCB operation and MMC blocking are not as complicated as DCCB operation. They are usually set with electrical parameters threshold comparison. In most of the cases, ACCBs and MMCs are not required to act to the fault until DCCB fails to clear the fault.

4.2 Relay algorithm

4.2.1 Algorithm introduction and mechanism [15]

The methodology of algorithm in this four terminal HVDC system is called the median absolute deviation (MAD). Mathematically, it is a data processing method to identify outliers in a series of arrays, i.e. the most abrupt value in a transient process [35][36]. (1) shows an array A indexed by i that contains the latest n samples of a_i spaced by the sampling interval.

$$A_i = \left[a_1(t_n - (n-1)\Delta t), a_2(t_n - (n-2)\Delta t), ..., a_{n-1}(t_n - \Delta t), a_n(t_n)\right] \quad (1)$$

where Δt represents the sample period, and the MAD of A_i is defined as:

$$MAD(A_i) = median\left[\left|A_i - median(A_i)\right|\right] \quad (2)$$

(2) tells that the mathematical meaning of MAD is the median value of the absolute deviations of samples from the median of the target array. It has been proven that MAD is a robust measure of statistical dispersion. Although the variance and standard deviation are also measures of spread, according to their definitions:

$$s^2 = \frac{\sum_{i=1}^{n}(X_i - \mu)^2}{\mathrm{N}}$$

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n}(X_i - \mu)^2}{N}}$$

The results are highly effected by the extremely high or extremely low samples in the array since the deviations to the mean μ are squared. Besides, either the variance or the standard deviation is of single polarity, which increases the difficulty in determining criterion.

The MAD value of the array is only a intermediate quantity instead of the final expected result. The ultimate index A_{iMAD} is defined:

$$A_{iMAD} = \left[A_i - median(A_i)\right] / MAD(A_i) \quad (3)$$

Where the denominator is $MAD(A_i)$, and the numerator is the deviations of samples from the median of the target array. The absolute value operator is removed so that (3) can have polarities (±) to indicate the trend of current varying. A_{iMAD} is also an array which depends

on the original sampling array A_i. It is needed to be mentioned once a new sampling is collected, the array A_i is updated,

$$A_i' = [a_2(t_n - (n-2)\Delta t), ..., a_{n-1}(t_n - \Delta t), a_n(t_n), a_{n+1}(t_n + \Delta t)]$$

where the first element '$a_1(t_n-(n-1)\Delta t)$' in (1) is removed out leaving a space for the coming new element '$a_{n+1}(t_n+\Delta t)$' to fill in. Every time when A_i is updated, A_{iMAD} is updated. However, each sampling at a time should lead to a new single value instead of a whole array. Because an array function A_{iMAD} dependent on the sampling time can not easily illustrate the burst in electrical information. Instead, the latest element in A_{iMAD} will be the ultimate detection value for each sampling.

For a example pole to pole fault taking place in cable 'Line_A1C1', the MAD method is applied to process current 'I_{dc1}' and 'I_{dc2}', where 'I_{dc1}' is the current flowing from bus A1 to bus C1, and 'I_{dc2}' is the current flowing from bus A1 to bus A2. The example result is demonstrated in Fig 4.2.

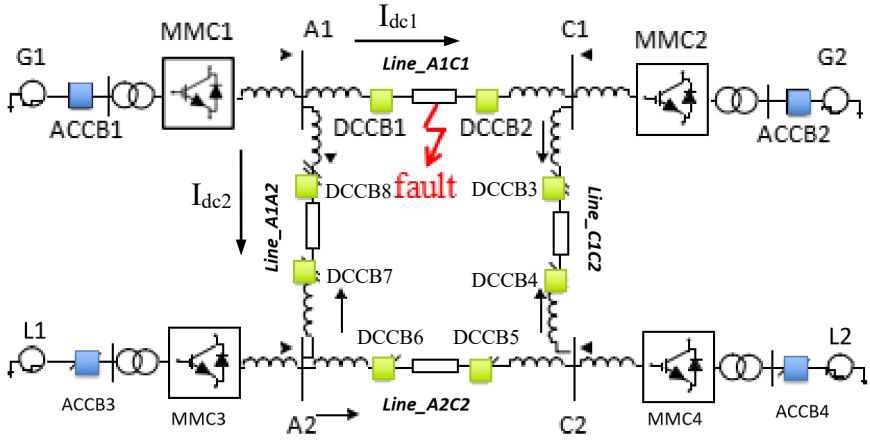


Figure 4.1: *Current detection in the test DC meshed system*

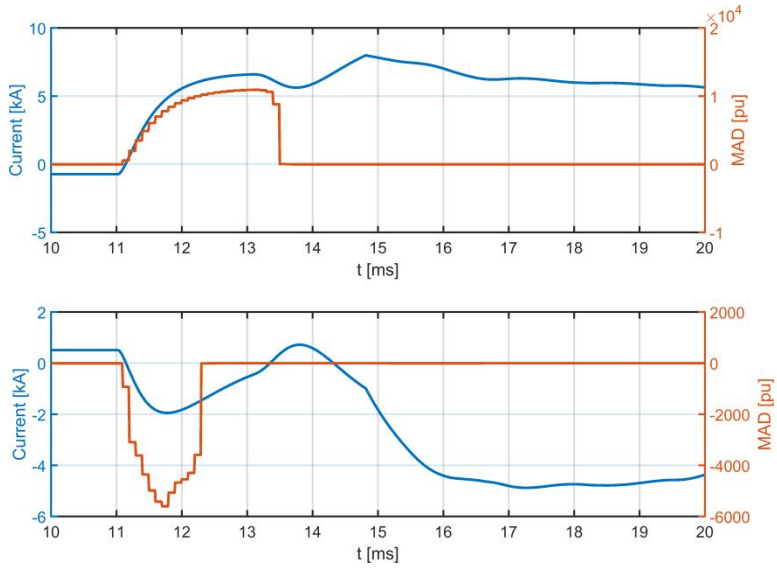


Figure 4.2: *Results of using MAD to process fault current. Upper plot: Idc1. Bottom plot: Idc2.* [15]

In Fig 4.2, the left longitudinal label is 'Current [kA]', which is the measure of the actual direct current colored in blue in the HVDC system. The right longitudinal label is 'MAD [pu]', which is the measure of A_{iMAD} colored in red in the HVDC system. As can be seen, the corresponding A_{iMAD} does experience a rapid increase or decrease immediately when the actual current starts to increase or decrease. This means A_{iMAD} is sensitive to respond to the first current outliers. Since the value of A_{iMAD} is in a large scale, it is good to distinguish an abnormal boost or drop of A_{iMAD} from the normal state. However, large values of A_{iMAD} makes it hard to quantify. In this example case, the expected result is to let DCCB1 and DCCB2 operate. DCCB5 and DCCB6 in 'Line_A2C2' are not likely to operate because the voltage of 'V_A2' and 'V_C2' are relatively stable in transients. DCCB3 and DCCB8 are not allowed to operate for the negative current increasing. While, for the last two DCCB4 and DCCB7, the local current is also increasing with positive polarity. It will not be guaranteed that DCC4 and DCCB7 not operate when the fault is in 'Line_A1C1'. As a result, it is not possible to use MAD solely to establish the fault detection criterion from a reliability point of view.

The trend of line voltage drop can be another criterion. The voltage collection points are illustrated in Fig 4.3. The voltage sampling is collected at the ends of faulty line and healthy line with the voltage drop over the line neglected. To make A_{iMAD} easy to quantify, a little modification is made on MAD of A_i and it is expressed as:

$$MAD\_M(A_i) = median[A_i] \tag{4}$$

The result of the actual line voltage and A_{iMAD_M} is illustrated in Fig 4.4.

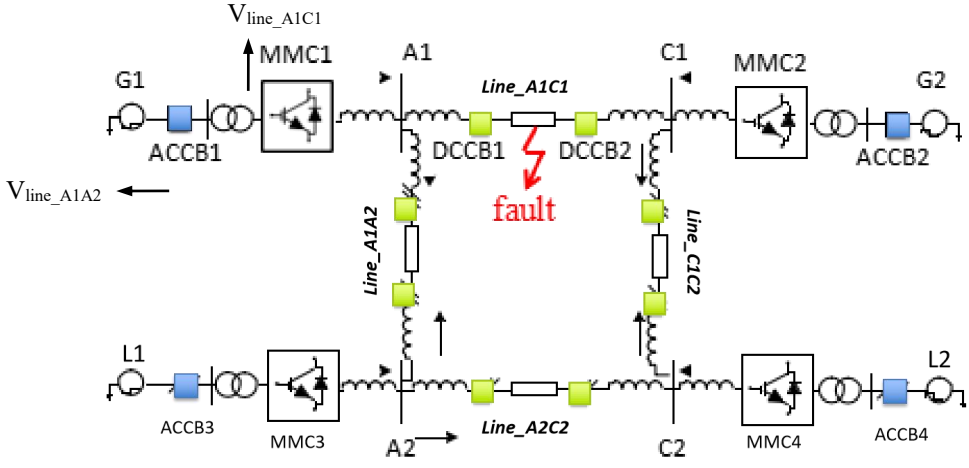


Figure 4.3: *Voltage sampling points in the test DC meshed system*

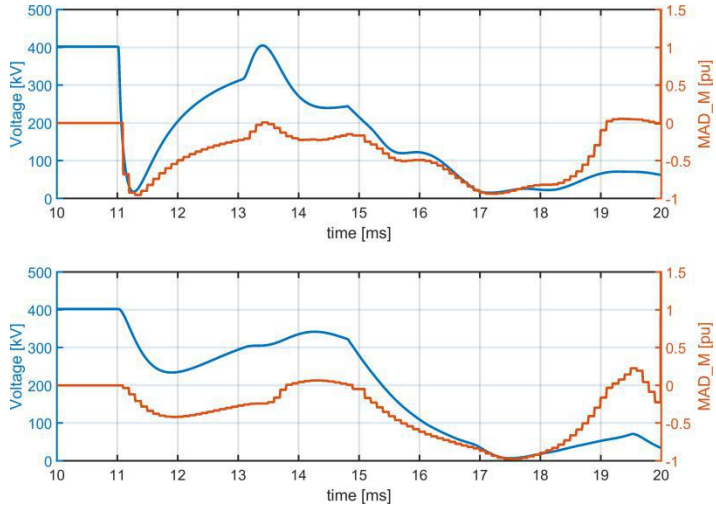


Figure 4.4: *Results of using MAD_M to process fault current. Upper plot: $V_{line\_A1C1.}$ Bottom plot: $V_{line\_A1A2.}$* [15]

In Fig 4.4, the left longitudinal label is 'Voltage [kV]', which is the measure of the line voltage colored in blue in the HVDC system. The right longitudinal label is 'MAD_M [pu]', which is the measure of A_{iMAD_M} colored in red in the HVDC system. The upper plot and the bottom plot indicate the voltage detection for 'V_{line_A1C1}'and 'V_{line_A1A2}' respectively. As the fault happened in t = 11ms, A_{iMAD_M} for the line voltage 'V_{line_A1C1}' drops to -1 shortly. While, A_{iMAD_M} for the line voltage 'V_{line_A1A2}' drops to -0.5 in 1ms. The modification of MAD_M does reveal different voltage drop between 'V_{line_A1C1}' and 'V_{line_A1A2}', which can provide another criterion to locate the faulty line.

4.2.2 Determination of the thresholds for fault detection

Theoretically, the thresholds for current and voltage detection is dependent on the performance of the A_{iMAD} and A_{iMAD_M}, which is proposed in Lian's paper. In that paper [15], A_{iMAD} and A_{iMAD_M} are tested as the functions of fault resistance and resistance as shown in Table 4.1 and Table 4.2.

Fault type	Method	Processed quantity	Fault resistance [ohm]					
			0	10	20	30	40	50
Pole-to-pole fault	MAD	Idc13	569	479	413	362	323	290
		Idc12	-924	-778	-672	-589	-526	-475
	MAD_M	Vdc13	-0.678	-0.569	-0.491	-0.432	-0.385	-0.348
		Vdc12	-0.0348	-0.029	-0.0254	-0.0223	-0.0199	-0.018
Pole-to-ground fault	MAD	Idc13-	777	565	445	366	311	270
		Idc12-	-1990	-1447	-1140	-939	-798	-694
	MAD_M	Vdc13-	-0.682	-0.5	-0.389	-0.32	-0.272	-0.24
		Vdc12-	-0.04	-0.029	-0.023	-0.019	-0.016	-0.014

Table 4.1: *Result of MAD and MAD_M as function of fault resistance* [15]

Fault type	Method	Processed quantity	Fault distance [km]				
			0	50	100	150	200
Pole-to-pole fault	MAD	Idc13	4314	1234	2256	306	569
		Idc12	-4027	-2210	-1064	-589	-924
	MAD_M	Vdc13	-1	-1.04	-1.18	-0.622	-0.678
		Vdc12	-0.11	-0.056	-0.088	-0.107	-0.0348
Pole-to-ground fault	MAD	$Idc13^-$	2216	1191	2428	297	777
		$Idc12^-$	-3717	-1430	-1458	-589	-1990
	MAD_M	$Vdc13^-$	-1	-1.41	-1.19	-0.624	-0.682
		$Vdc12^-$	-0.126	-0.064	-0.1	-0.0154	-0.04

Table 4.2: *Result of MAD and MAD_M as function of fault distance* [15]

In Table 4.1 and Table 4.2, the negative pole-to-ground fault is simulated; the superscript '-' means the quantities measured on the negative pole of HVDC system. Based on the maximal value of MAD and minimal value of MAD_M in TABLE II and TABLE III, the appropriate thresholds value for current detection and voltage detection can be determined. For example, the threshold value are initially set to be as (5) and (6) according to Table 4.1 and Table 4.2.

$$MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 250 \\ 0, else \end{cases} \tag{5}$$

$$MAD.V = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.235 \\ 0, else \end{cases} \tag{6}$$

When MAD.I and MAD.M are both 1, then the local relay will consider it as a fault. As the tripping signals are sent to the DCCBs nearby, the faulty line is determined. Due to the possible un-synchronization between the sampling of DC current and voltage, little delay between the two indices are allowed. That means as long as MAD.I and MAD.V are subsequently identified as 1 in a small time frame (50 μs), the trip signal will be generated.

However, in this paper, the existed thresholds are no longer applicable. The main reason is the performance testing of A_{iMAD} and A_{iMAD_M} in Lian's paper are complemented based on the software 'PSCAD'. 'RSCAD' and 'PSCAD' has different simulation time step, which leads to different simulation accuracy [37]. It is not appropriate to use the testing data from the source of PSCAD. In this project, the investigation method would be given a certain threshold for MAD.I and MAD.V, then to see how the algorithm performs based on the RTDS platform.

4.3 ACCB operation and MMC blocking

For the fully selective protection scheme, relay algorithm is the most important section since DCCB is the only fault clearing device. However, ACCB and MMC may function as an auxiliary fault clearing device in the partially selective protection and non selective protection scheme as discussed in Chapter 3.3 and Chapter 3.4. First of all, ACCBs and MMCs have individual criterion to operate or self-protection. For ACCBs, as long as the DC current is larger than 6kA, the ACCB should operate to prevent AC sources from injecting more fault currents.

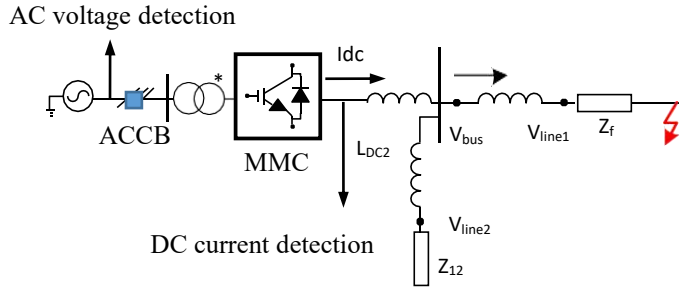


Figure 4.5: *Criterion for ACCB operation and MMC self-protection*

For the half-bridge structured MMC used in this project, it will protect itself by preventing partial of the overcurrent. Either the AC side voltage is less than 0.1pu of the normal voltage or the DC current is larger than 6kA, MMCs should block itself. The AC voltage is sampled between the AC source and ACCB and the DC current is sampled at the DC output of MMC as is shown in Fig 4.5. The current criterion, 6kA is decided by the sub-module characteristic and diode current rating. In other words, 6kA is the maximum DC current that the MMC model can withstand.

Apart from these criterion, extra operation requirements are added to help clear the fault in the cases of partially selective protection and non selective protection scheme. In partially selective protection, 3.3b is the DCCB placement that tested in this project.

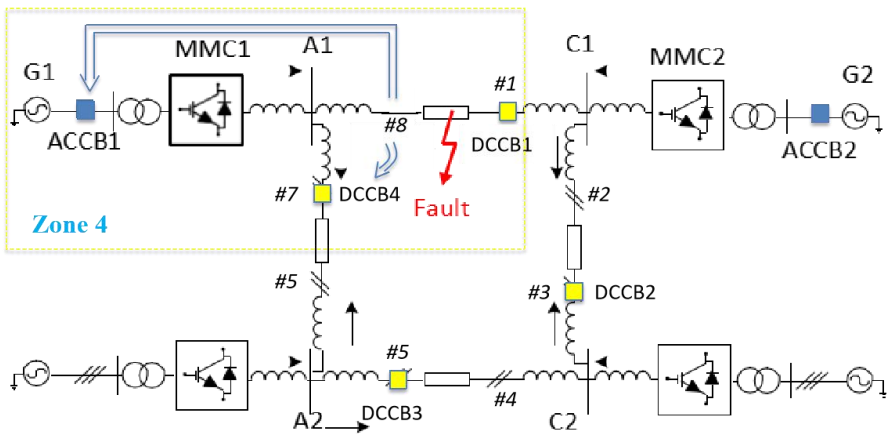


Figure 4.6: *ACCB operation mechanism in partially selective protection*

In Fig 4.6, the superscript '#' means the relay location. As the fault happens in cable

'line_A1C1', the expected result is DCCB1, DCCB4 and ACCB1 trips. So that zone 4 is disconnected. DCCB1 will operate since relay '#1' will detect the fault. For ACCB1 and DCCB4, the method is to send the trip signal detected by relay '#8' near bus A1 to ACCB1 and DCCB4. This command is parallel to ACCB1 and DCCB4's operation mechanism. For the other three zones, similar settings are made.

In non selective protection, option (a) in 3.4 is taken since half-bridge MMC can not fully block itself. Also, the extra DCCBs between MMCs and buses can be a huge expenditure. It is not possible to let the relay send trip signals to each ACCB as the relay detects the fault. The reason is that beside the ACCB near the relay, the other three ACCBs are at least 200km far away. Communication can be a big problem which makes this idea abandoned.

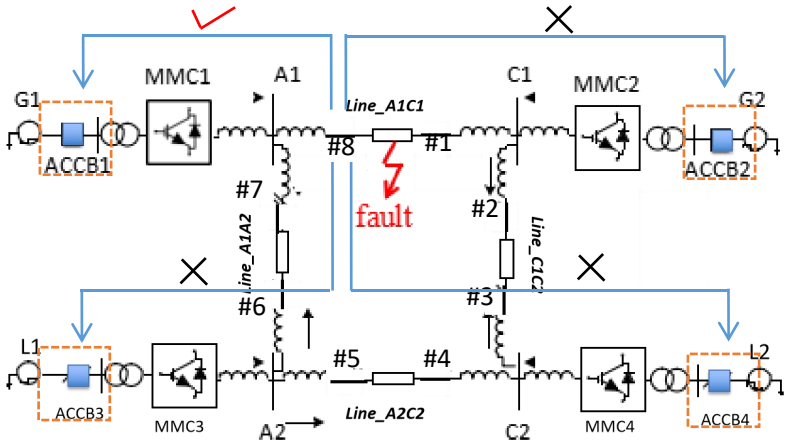


Figure 4.7: *Abandoned method in non selective protection*

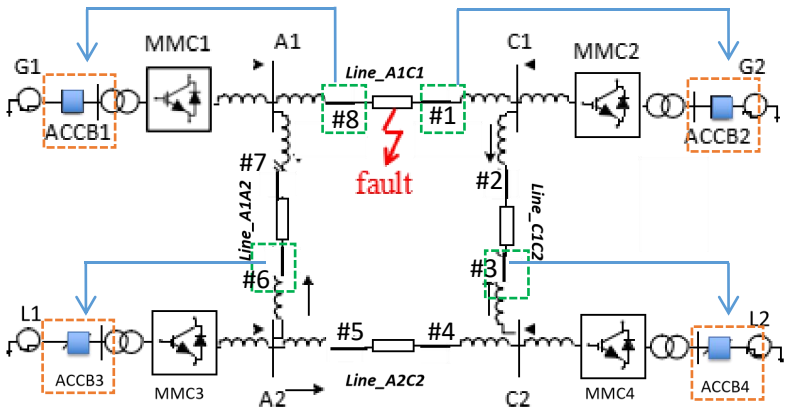


Figure 4.8: *Feasible method in non selective protection*

One of the feasible method is demonstrated in Fig 4.8. As is discussed in 4.2.2, a fault is identified by detection of MAD.I and MAD.V both. For the example fault in 'line_A1C1', not only relay '#8' and '#1' will lead to a '1' signal for MAD.I, but also relay '#6' and '#3' are likely to reach a '1' signal for MAD.I. Because MAD.I reveals the current change trend, while each of relay '#8', '#1', '#3' and '#6' will witness a significant current increase. It is the MAD.V's joining, that makes the relay '#6' and '#3' silent.

Then here comes the idea, that is to first get rid of the voltage detection, i.e. MAD.V. Without MAD.V, relay '#8', '#1', '#3' and '#6' will detect the fault. After that, trip signals from '#8' and '#1' can be sent to 'ACCB1' and 'ACCB2' respectively. Trip signals from '#6' and '#3' can be sent to 'ACCB3' and 'ACCB4' respectively. Thus, communication problems can be minimized since the trip signal is sent from the local relay to the ACCB nearby. It is the same mechanism when faults happen in other cables. In the end, relay '#7' and '#8' are set to sent trip signals to 'ACCB1'; relay '#1' and '#2' are set to sent trip signals to 'ACCB2'; relay '#5' and '#6' are set to sent trip signals to 'ACCB3' and relay '#3' and '#4' are set to sent trip signals to 'ACCB4'.

Chapter 5

Remote Testing Based on RTDS-MATLAB Simulation Environment

This chapter introduces the simulation environment of the entire HVDC system protection tests. It firstly tells on which software and hardware the test model is built and run. Then, it tells how MATLAB can remotely communicate with simulation hardware. At last, the chapter discussed the objectives of fault simulation.

5.1 Introduction

The idea of remote testing is firstly proposed by Apostolov, USA [38]. Instead of a crew moving far away to implement hardwired protection and control systems, IEC 61850 based communication interfaces allow people to do the testing remotely and efficiently. The test method and tools determine whether tests are implemented in a reliable and secure way. Besides, testing quality should be ensured by an effective simulation of a real situation [38]. For example, a transmission line short-circuit-fault caused by a branch or a kite string.

5.2 RTDS based modelling and simulating

RTDS testing has two main advantages compared to other simulation software that can be used for testing. One is its real-time simulation property. One rack is capable to store 6 parallel processor cards (PB5). During the simulation, the powerful ability of data acquisition and calculation allows not only continuous but also timely output. Thus, a real-time feedback between controllers and controlled objects would significantly improve the testing reliability drastically.

Another advantage of RTDS is its ability to perform hardware-in-the-loop (HiL) test. HiL testing is usually applied in aerospace, automotive manufacturing and power systems. By applying HiL method the functionality of a physical protection device in an emulated virtual DC network instead can be tested. In this testing experiment, the DCCB model is modeled as a in RSCAD software model instead of using an actual DCCB. The major benefit of doing so is the reduction of financial costs compared to the costs of testing in an actual object [39].

5.3 RTDS--MATLAB simulation environment

Fig 5.1 shows a configuration of the real time cyber-physical simulation platform to realize the remote testing strategy. The test HVDC system is firstly built in RSCAD software in the remote/local computer.

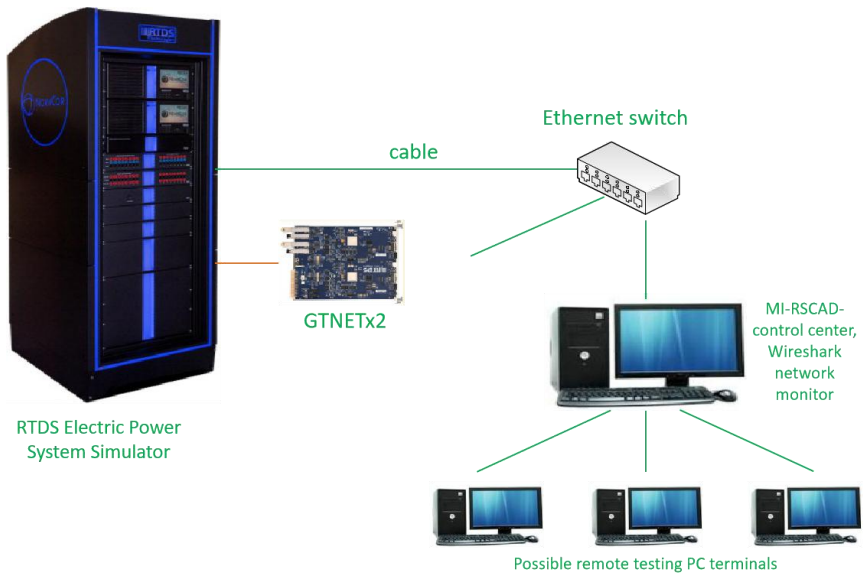


Figure 5.1: *Real time simulation platform with remote testing interface*

In the RSCAD interface, not only control commands including the fault generation signals are given, but also the power flow and system operation are observed. An entire fault case simulation and protection testing may require frequent manual revisions in RSCAD. However, by using MATLAB, complex commands can be integrated into a m-file, in which

they can be executed more efficiently. In addition, it is convenient to exchange data between RSCAD and MATLAB via JTCP interface. This JTCP file uses MATLAB's Java interface to handle Transmission Control Protocol(TCP) communications with another application, either on the same computer or a remote one. Four racks of RTDS, which include 16 PB5 processor cards, are used to provide Type-5 models [40] of HB MMC converters, mechanical DCCBs in small time step and the proposed protection algorithm.

5.4 Protection testing objectives

In any power systems, either AC grids or DC power system secure operations would not be maintained without suitable protection systems. An effective protection system is to ensure correct disconnection of the faulty items in order to timely and significantly minimize the consequences that may result from the fault occurrence [41]. The objective of the protection testing is to determine whether the performance of an IED can meet the industry requirements.

Therefore, the research performed here firstly considers the sensitivity of the protection system on the test HVDC system model by multiple fault case simulations. Test cases will be conducted to demonstrate the effectiveness of the proposed test environment.

Chapter 6

Fully selective DCCB placement protection simulation and analysis

This chapter studies the fault cases on FSPS. Before the test, a description on time step and threshold setting for relay algorithm is stated. Then, it follows by the base case study, where important current and voltages are analyzed. After that, more cases study are investigated and compared. From that, how the fault parameters will affect the fault transient is generally concluded.

6.1 Description and statement before simulation

Before the simulation, there are some basic settings that have be stated. In the model building section, 4 subsystems are used in the software 'RSCAD'. This means 4 racks are needed when these subsystems are compiled in the RTDS. For part of the sub-modules, they run with particular time steps. For example, the DCCB modules require a small time step of 3μs. Beside these modules, the other modules will run with the normal big time step between 75μs to 140μs stated in 'circuit option' interface. The various big time steps do influence a lot on the current performance, even DCCB operation. The big time step is expected to be as small as possible so that the sampled electrical parameters are precise. In the early stage of

experiment, a '75μs' big time step is generally used. However, as some modifications are needed to function on the prototype model, a '75μs' big time step is no more qualified due to the Software restriction. In the real test procedure, the big time step will be clearly stated on experiments of different types.

MATLAB scripts, RSCAD draft file and sib file, algorithm C builder are attached in the 'List of simulation files'. MATLAB scripts describes the sequence of the simulation commands. RSCAD draft file is where the model is built. RSCAD sib file is the interface where simulation is monitored and controlled. Algorithm C builder records the relay algorithm code in C language.

In the algorithm, thresholds for MAD.I and MAD.V are given an number as is demonstrated.

$$MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 200 \\ 0, else \end{cases} \tag{7}$$

$$MAD.V = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.4 \\ 0, else \end{cases} \tag{8}$$

For all the case studies, the simulation develops as the following process. First, the whole system starts self-initialization for 10 seconds. During this period, MMCs are driven to the normal operation, transferring power between AC sources and the DC system. And, capacitors in the mechanical DCCB are fully charged. After this period, the fault happens. All the plots start 0.1 seconds before the fault inception and end in 0.13 seconds, which is enough to demonstrate the transients in post-fault period.

6.2 Base case study

The base case is defined when a pole to pole fault takes place close to bus C1 at t_0=0.1s. Fault settings are demonstrated in Table 6.1. In practice, the resistance could be very low since that the cable faults are usually bolted faults. As a result, the fault impedance in base case is set to be **R_f = 0.0101 ohm**, close to zero. Fig 6.1 shows the simulation results.

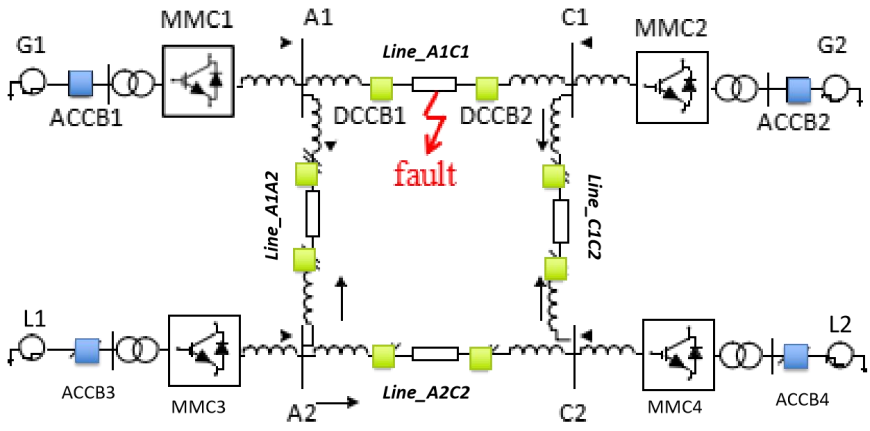


Figure 6.1: *DC protection system in base case*

Converter self protection	With
Fault inception instant	t = 0.1s
Fault type	**Pole to pole**
Fault locations	**Close to bus C1**
Fault Impedance	**R_f = 0.0101 ohm**
DCCB placement	**Fully selective**
DCCB mechanical delay	8ms

Table 6.1: *Critical settings and parameters of test HVDC mesh system*

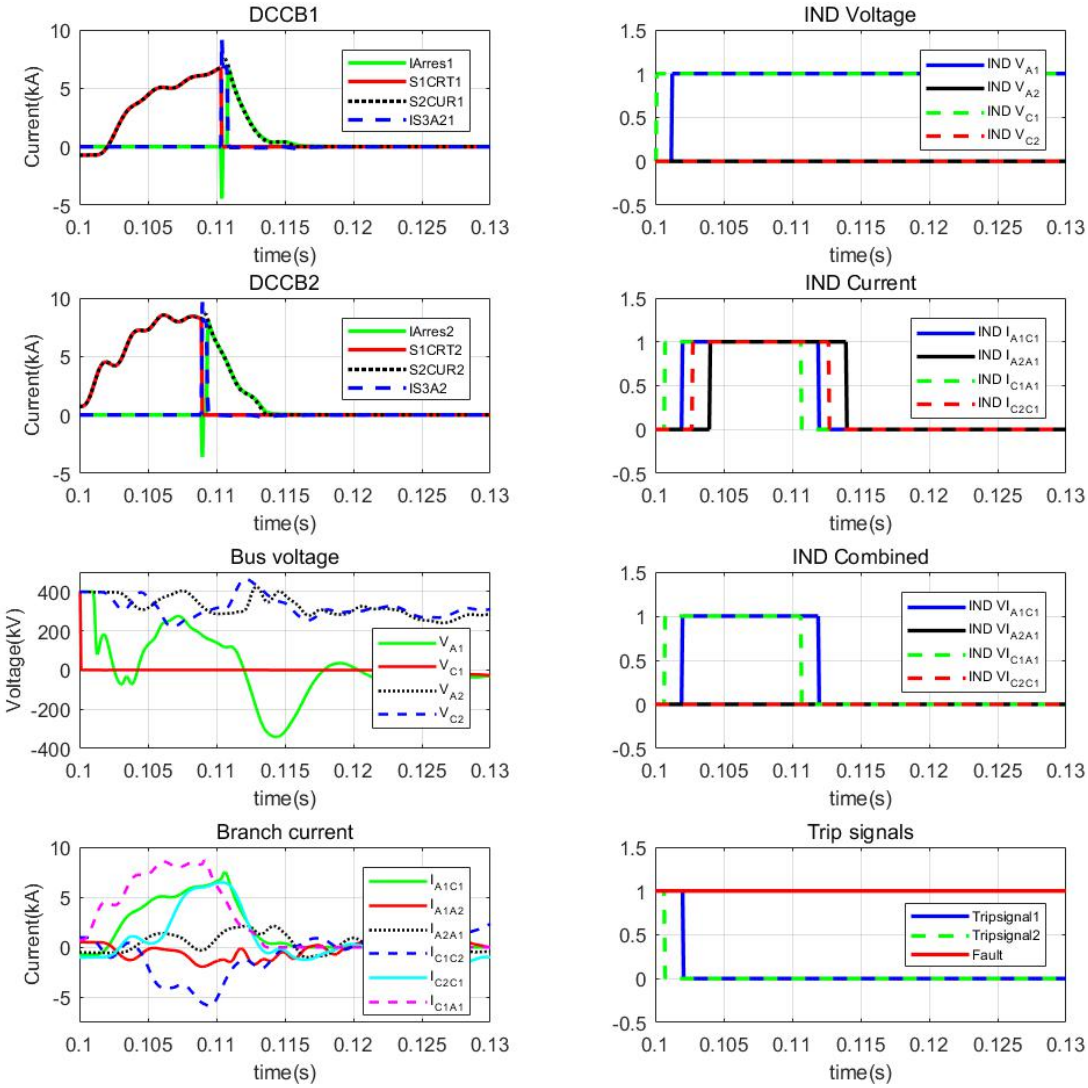


Figure 6.2: *Plots of DCCBs, system voltages and currents, indices of trip signal.*

DCCB plots analysis:

The left column in Fig 6.2 includes plots of DCCBs, plots of bus voltages and plots of branch currents. There are two plots of DCCBs, DCCB1 and DCCB2 which are located at the faulty cable. In DCCB plots , 'IArres' (green solid line) shows the branch current going through the surge arrester. 'S1CRT' (red solid line) is the branch current going through the main interrupter S1 and 'IS3A2' (blue dashed line) is the branch current going through the capacitor. 'S2CUR' (black dotted line) is the superposition of these three branch current 'S1CRT', 'IArres' and 'IS3A2'. And 'S2CUR' is assumed to be the total current flowing through the DCCB. All these currents are also specified in the model in Fig 6.3.

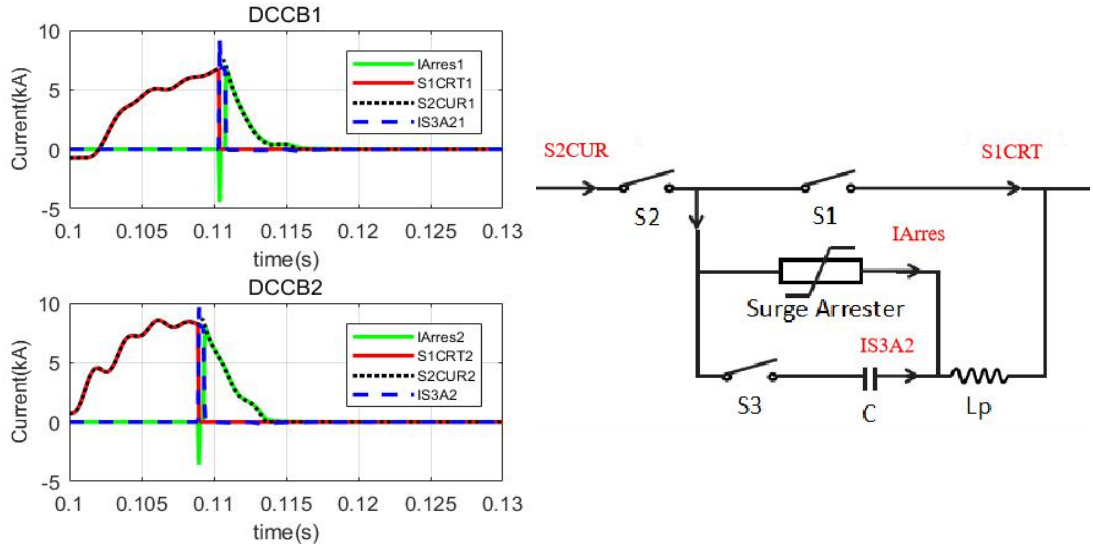


Figure 6.3: *DCCB plots with currents specified in the DCCB model*

In system normal operation, switch 'S2' and 'S1' are closed. While, switch 'S3' on the capacitor branch is on open state. Capacitor 'C' is fully charged. Within the mechanical DCCB delay 8ms after the fault being detected, the curves of 'S2CUR' and 'S1CRT' overlap with each other **(stage 1)**. Also, there is no arrester current or discharging current, because 'IArres' and 'IS3A2' remains zero. After the 8ms, switch 'S3' is closed first with dramatic capacitor current released almost immediately. That happens where the blue spike of 'IS3A2' is located. This huge counter current not only makes the increasing fault current 'S1CRT' down to zero, but also gives an negative green spike of 'IArres' at that moment. As the current 'S1CRT' is down to zero, switch 'S1' is safely opened **(stage 2)**. After the capacitor is fully discharged, there is only transient over-voltage (TVR) over the surge arrester. At this moment, 'S2CUR' is equal to the 'IArres'. According to the surge arrester characteristics, the overall fault current 'S2CUR' will decline to zero soon. With the final zero crossing happens over 'S2', 'S2' is open. Till this moment, the fault is fully interrupted **(stage 3)**. In this base case study, it takes around 0.016s (16ms) until both DCCBs operate.

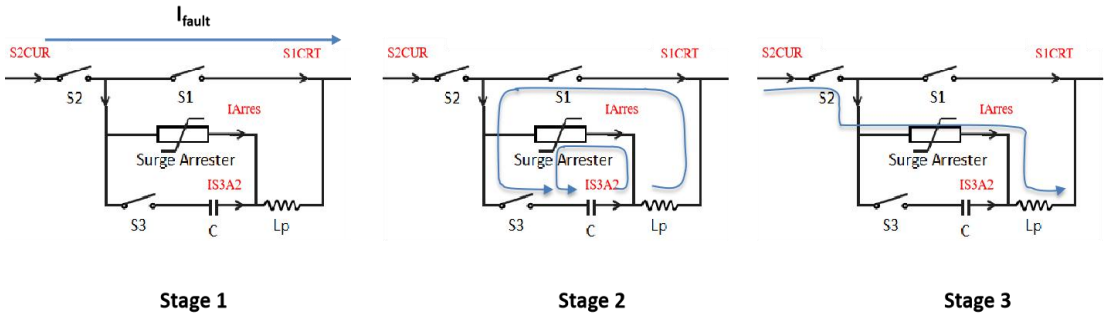


Figure 6.4: *Three stages when the mechanical DCCB interrupts a fault*

1.Different initial current directions

As can be seen, 'I_{Normal}' shows the current direction when the system is on normal operation. That is the reason why the fault current 'S2CUR1' goes from the negative magnitude while 'S2CUR2' goes from the positive magnitude. Shortly after, both 'S2CUR1' and 'S2CUR2' increases rapidly since the bolted fault draws huge faulty current. For DCCB2, the highest fault current is around 8kA until it is cleared. Looking at plots of DCCB2, the current increasing curve is not flat. Those inflection points reflect instants when the travelling wave reaches different buses. More details related to this will be explained in the following content.

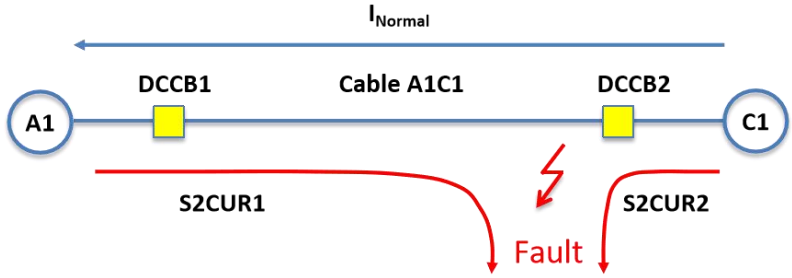


Figure 6.5: *Normal current and faulty current in cable A1C1*

2.Different instants when faulty currents increases

'S2CUR2' flowing through DCCB2 almost increases immediately as fault takes place. While 'S2CUR1' flowing through DCCB1 delays around 0.002s (2ms) and then grows. The reason is in the base case, the fault is set close to C1. The fault traveling wave takes more time to approach terminal A1 than to approach terminal C1. And that is where the 2ms difference is. And further consequence of that is earlier DCCB2 operation than DCCB1 operation. Because the mechanical operation time in the model is fixed at around 8ms according to the current DCCB manufacture.

3.Different trends of current increasing

Due to the fact that the fault is close to terminal C1, not only the fault current 'S2CUR2' grows earlier but also grows faster. The highest magnitude of 'S2CUR2' is around 8kA and the highest magnitude of 'S2CUR1' is 7kA. Combing the previous two features, a vague conclusion can be drawn that, the fault coordinate can affect the fault current characteristics.

Bus voltage and branch currents analysis:

In the plot of bus voltages, 'V_{A1}' and 'V_{C1}' are denoted respectively by green solid line and red solid line. 'V_{A2}' and 'V_{A2}' are denoted respectively by black dotted line and blue dashed line. Since the fault is of pole to pole type, the voltages measured here is the deviation between the positive polarity and negative polarity. The position of these measured voltages are illustrated in Fig 6.6. In plots of branch currents, the green solid line ('I_{A1C1}') shows the current flowing from terminal A1 to terminal C1, whilst the red solid line ('I_{A1A2}') shows the current measured in the reverse direction. And the blue-dashed line ('I_{C1C2}') shows the current injection from terminal C1 to terminal C2, with the navy solid line('I_{C2C1}') shows the current in the reverse direction. The other two branch current 'I_{A2A1}' and 'I_{C1A1}' are denoted

by black dotted line and pink dashed line respectively.

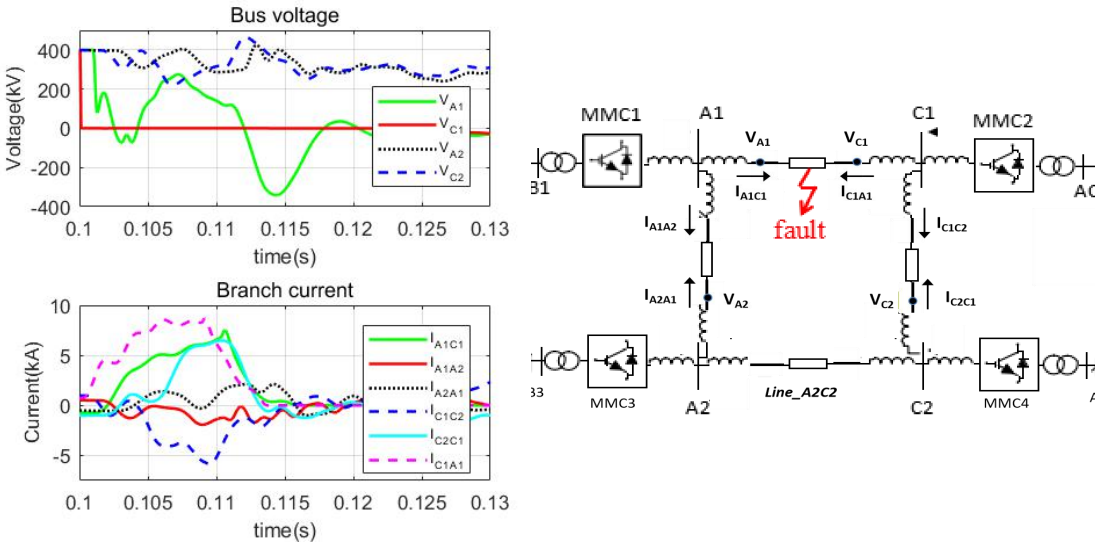


Figure 6.6: *Bus voltage and branch current specified in the test system*

It is very important to firstly state where these voltages and currents variables are collected. And Fig 6.6 specifies these in the test system. It is observed that, these so called 'Bus voltages' are not actually measured on the buses but behind the current limiters on cables. The instant of fault occurrence is labeled as 't_0'. The instant that the travelling wave reaches terminal C1 is denoted by 't_1'. Since the fault is biased to terminal C1, 'V_{C1}' drops to zero almost immediately as fault happens. Meanwhile, current 'I_{C1A1}' starts growing. Afterwards, the instant that the travelling wave reaches terminal A1 is denoted by 't_2'; the instant that the travelling wave reaches terminal A2 is denoted by 't_3'; the instant that the travelling wave reaches terminal C2 is denoted by 't_4'.

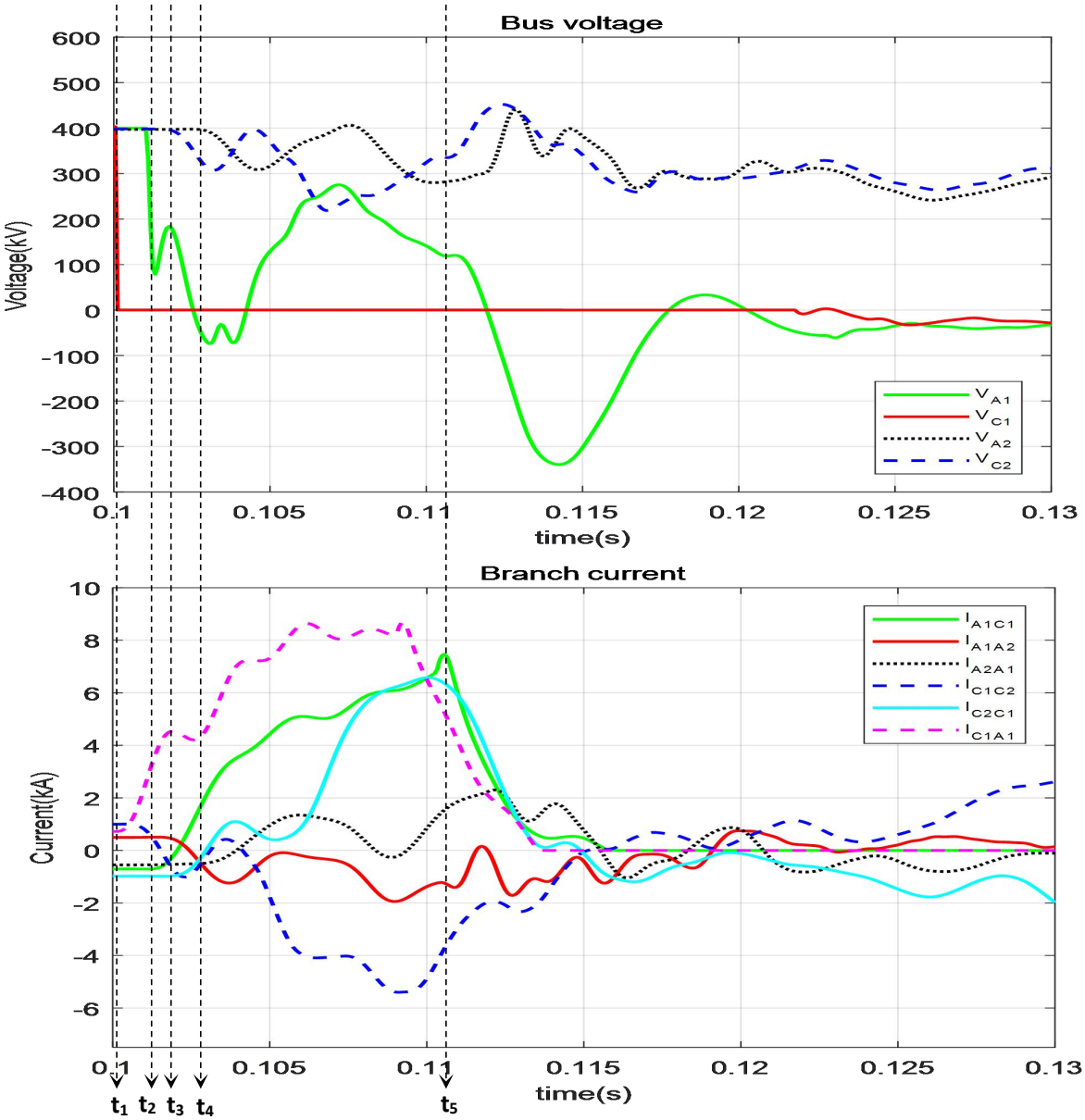


Figure 6.7: *Voltage and Current plots with specific instant pointer*

Though 'V_{A1}' and 'V_{C1}' are both collected on the faulty cable A1C1, the curve of 'V_{A1}' differs a lot with 'V_{C1}'. As the travelling approaches terminal A1, 'V_{A1}' firstly plunges to 100kV from 400kV. Between 't_2' and 't_3', it rises a bit. After 't_3', it declines to below 0. In the following transient process, 'V_{A1}' experiences an irregular growth and decline until switch 'S1' in DCCB1 is open. And that instant can be called 't_5'. After 't_5', 'V_{A1}' shapes like response of a 2nd order underdamped system. Since terminal A2 and C2 are far away from the fault, the voltage oscillation of 'V_{A2}' and 'V_{C2}' is not as severe as 'V_{A1}' and 'V_{C1}'. And timely interruption of fault makes 'V_{A2}' and 'V_{C2}' end up around 300kV. Compare current 'I_{C2C1}' with 'I_{A2A1}', it is found that the fault current injection from terminal C2 is evidently larger than from terminal A2. Whether it is caused by fault location still requires more cases study to prove.

Electrical indices and trip signals analysis:

In the right column of Fig 6.2, voltage and current indices, as well as the combined indices illustrate whether and when DCCB trip-signals are generated. The time for each signal is precise in millisecond. The rest plot 'Trip signals' shows the instants for each trip signal since fault inception. In the plot of IND voltage, 'IND V_{A1}' and 'IND V_{A2}' are plotted by blue solid line and black solid line respectively. 'IND V_{C1}' and 'IND V_{C2}' are plotted by green dashed line and red dashed line respectively. In the plot of IND current, 'IND I_{A1C1}' is denoted by blue solid line which shows the index of current from A1 to C1. 'IND I_{A2A1}' is denoted by black solid line which shows the index of current from A2 to A1. 'IND I_{C1A1}' is denoted by green dashed line which shows the index of current from C1 to A1. 'IND I_{C2C1}' is denoted by red dashed line which shows the index of current from C2 to C1.

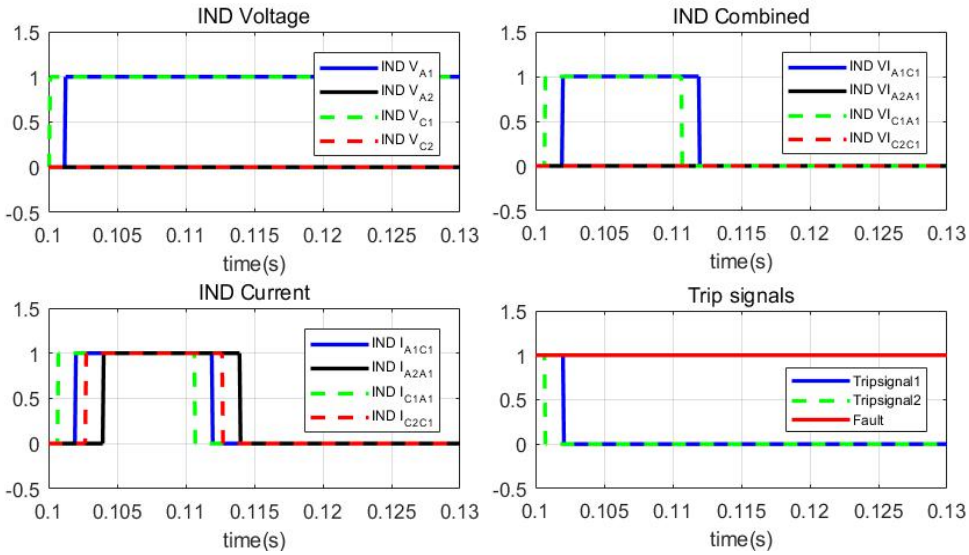


Figure 6.8: *Plots of Electrical indices and trip signals*

In the plot of IND combined, the blue solid line shows the combined index 'IND VI_{A1C1}', which later would be converted to trip signal sent to DCCB1. The black solid line shows the combined index 'IND VI_{A2A1}'. The corresponding trip signal is sent to the DCCB located at terminal A2 in cable A2A1. The green dashed line shows the combined index 'IND VI_{C1A1}', which later would be converted to trip signal sent to DCCB2. The red dashed line shows the combined index 'IND VI_{C2C1}'. The corresponding trip signal is sent to the DCCB located at terminal C2 in cable C2C1. In plot of Trip signals, 'Tripsignal1' and 'Tripsignal2' represent the signals sent to DCCB1 and DCCB2 respectively. The red solid line indicates the fault.

'IND V' and 'IND I' actually demonstrate the performance of 'MAD.V' and 'MAD.I', which is explained in Chapter 4.

$$MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 200 \\ 0, else \end{cases}$$

$$MAD.V = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.4 \\ 0, else \end{cases}$$

When signal 'IND V' appears to be 1, 'MAD.V' is also 1, which means the voltage condition for DCCB tripping is satisfied. Otherwise, 'IND V' remains 0. When signal 'IND I' appears to be 1, 'MAD.I' is also 1, which means the current condition for DCCB tripping is satisfied. Otherwise, 'IND I' remains 0. As is discussed in chapter 4, only when the voltage index and the current index are detected within a limited delay (50 μs), can the combined index 'IND VI' be enabled. Then the trip signals are generated and sent to corresponding DCCBs.

For any transmission line or cable fault, only four DCCBs should be carefully watched as it is explained in Chapter 4. In this base case, they are DCCB1, DCCB2, DCCB4 and DCCB7.

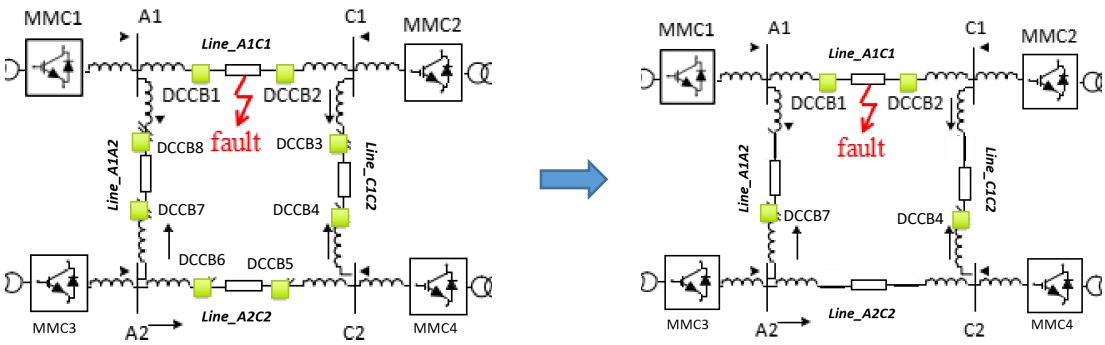


Figure 6.9: *Four main DCCBs operation study in cable faults*

That is the reason why the indices of four positions are illustrated and studied in Fig 6.9. Among all the voltage indices, only 'IND V_{A1}' and 'IND V_{C1}' are detected. However, all the current indices of four positions are detected in sequence. DCCB1 and DCCB2 ends up with operation due to the mechanism of algorithm. This indices result are generally satisfactory because the algorithm works well. DCCB1 and DCCB2 clears the cable fault correctly and DCCBs in other cables stand still. However, the potential risk is that current detection in the algorithm can not precisely locate the fault in possible cables.

Signals of ACCB and MMC analysis:

Fig 6.10 is an illustration of ACCB and MMC operation with the subscript referring to the corresponding terminals. 'ACBRK' is the short name of trip signals sent to ACCBs. And 'DBLK' is the short name of blocking signals sent to MMCs. For both of these two signals, high level '1' means closed state for ACCBs or normal working state for MMCs. While, low level '0' means trip signal for ACCBs or blocking signal for MMC is enabled.

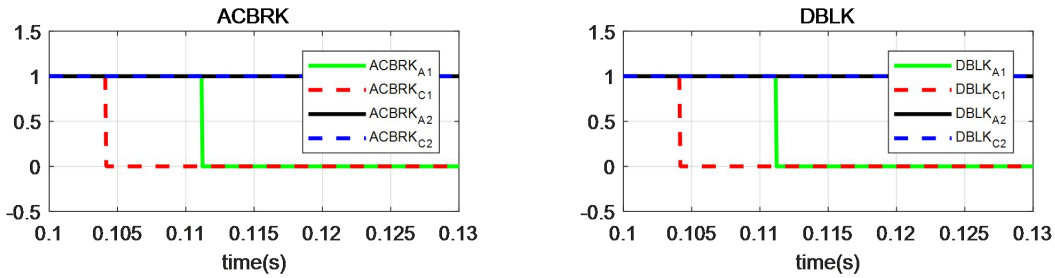


Figure 6.10: *Plots of ACCB and MMC operation signal*

Enabling these two signals follows different rules as discussed in chapter 4. For ACCBs, when the DC current exceeds 6kA, signal 'ACBRK' will turn from '1' to '0' state. For MMCs, either the AC side voltage is less than 0.1pu of the normal voltage or the DC current is larger than 6kA, 'DBLK' will turn from '1' to '0' state. The current criterion, 6kA is decided by the sub-module characteristic and diode current rating.

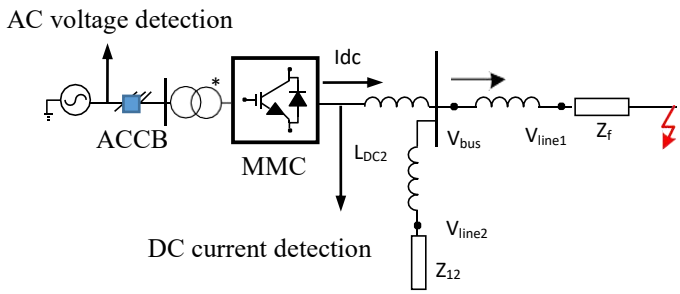


Figure 6.11: *Criterion for ACCB operation and MMC self-protection*

In the base case, ACCBs on terminal A1 and C1 operate. And MMCs on terminal A1 and C1 block themselves. Though DCCB1 and DCCB2 isolate the faults in the DC system, ACCBs in terminal A1 and C1 still operate for high short current injection. MMCs in terminal A1 and C1 block due to the self-protection mechanism.

6.3 More fully selective cases and faults analysis

Here, more cases simulation have been done with different fault parameters, including fault location, fault impedance, fault type in Table 6.2. All these cases results can be found in the **"List of simulation files"**.

DCCB placement	Fully selective
Fault cable	Cable_A1C1
Fault location	0km (A1), 50km, 100km, 150km, 200km (C1)
Fault impedance	0.0101ohm, 25ohm, 50ohm,75ohm, 100ohm
Fault type	Pole to pole fault, negative pole to ground fault

Table 6.2: *Fault parameters in the set of tests on fully selective protection*

For each case simulation, the following data have been recorded and mainly analyzed. They are '$\Delta V_{C1,max}$', '$\Delta V_{A1,max}$', '$I_{C1A1,max}$', '$I_{A1C1,max}$', '$t_{Tripsignal1}$' and '$t_{Tripsignal2}$'.

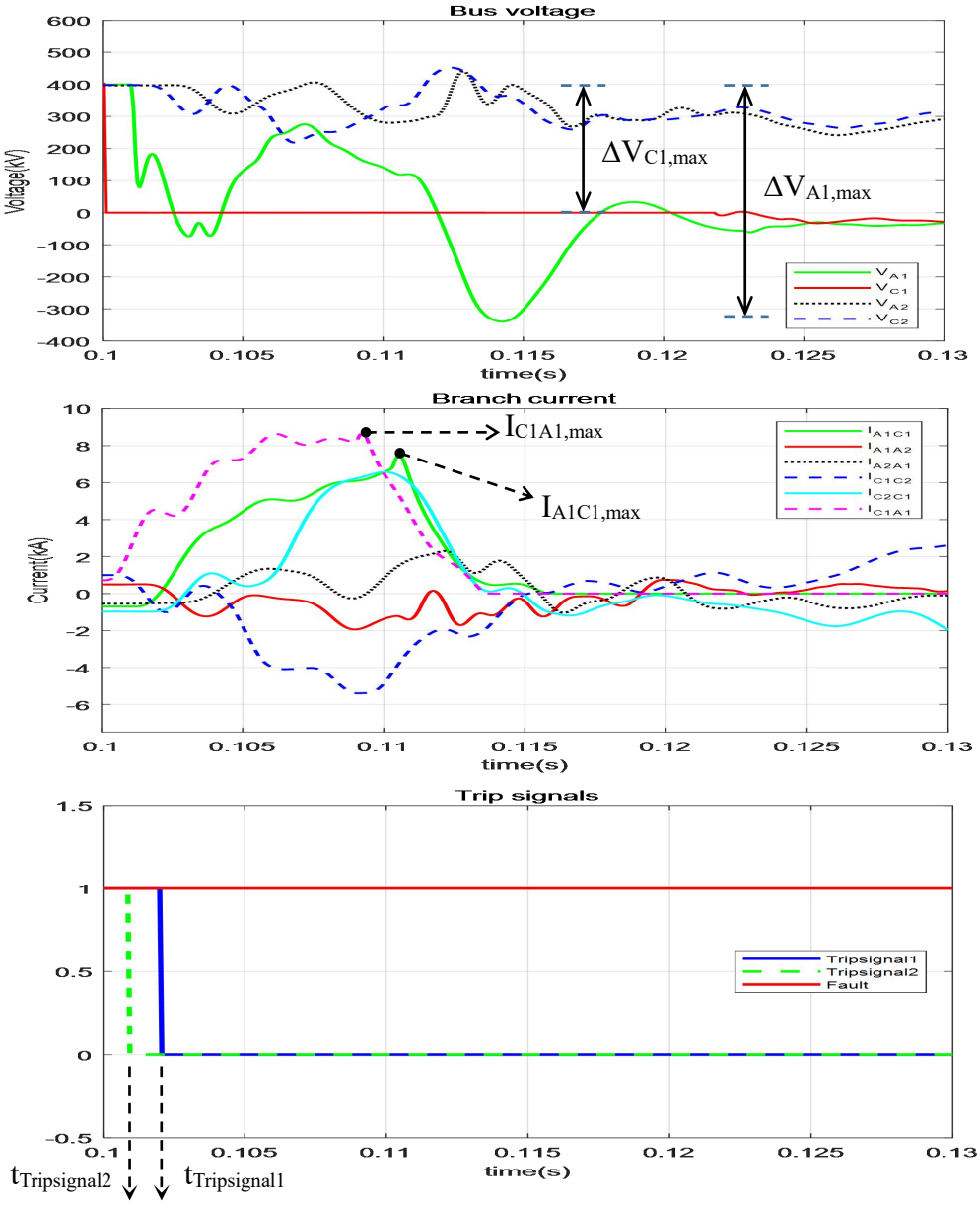


Figure 6.12: *Important simulation data illustrated in plots*

'$\Delta V_{C1,max}$' means the amplitude of the maximum variation of 'V_{C1}' in the captured transients from 0.1s to 0.13s. '$\Delta V_{A1,max}$' means the amplitude of the maximum variation of 'V_{A1}' during this period. '$I_{C1A1,max}$' represents the maximum amplitude of 'I_{C1A1}'. During the fault transient period, '$I_{C1A1,max}$' also means the maximum fault current, which is injected from terminal C1 to the fault position. '$I_{A1C1,max}$' represents the maximum amplitude of 'I_{A1C1}'. During the fault transient period, '$I_{A1C1,max}$' also means the maximum fault current, which is injected from terminal A1 to the fault position. In plots of 'Trip signals', two time instants '$t_{Tripsignal1}$' and

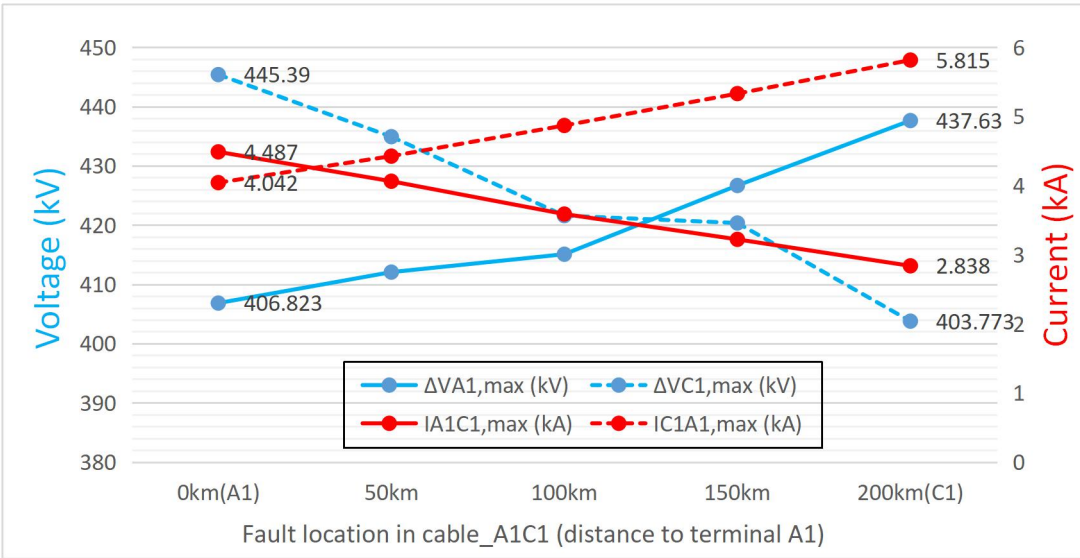
'$t_{Tripsignal2}$' are being recorded. They represent the instants when 'Tripsignal1' and 'Tripsignal2' are generated respectively.

Transients performance comparison between cases of various fault locations:

To test how the fault locations will affect the fault transients, the fault impedance is fixed at 50 ohms. The fault type is of pole to pole fault. Five fault locations along cable_A1C1 is studied.

Fault type	Pole to pole (ptp)				
Fault impedance	50ohm				
Fault location	0km (A1)	50km	100km	150km	200km (C1)
$\Delta V_{A1,max}$ (kV)	406.823	412.05	415.07	426.67	437.63
$\Delta V_{C1,max}$ (kV)	445.39	434.91	421.58	420.34	403.773
$I_{A1C1,max}$ (kA)	4.487	4.062	3.587	3.221	2.838
$I_{C1A1,max}$ (kA)	4.042	4.425	4.869	5.33	5.815
$t_{Tripsignal1}$ (s)	0.1014	0.1017	0.1021	0.1022	0.1027
$t_{Tripsignal2}$ (s)	0.1024	0.1023	0.1021	0.1015	0.1007

Table 6.3: *Pole to pole fault cases with impedance of 50ohms*



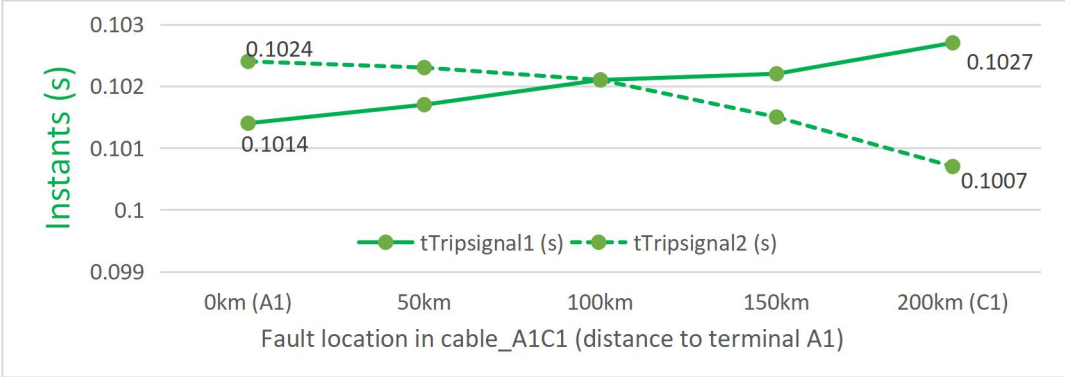


Figure 6.13: *Transients performance from cases of various fault locations*

When the fault is moving from terminal A1 forward to terminal C1, '$\Delta V_{A1,max}$' keeps increasing and '$\Delta V_{C1,max}$' keeps decreasing. This means, **"For cable faults, the further a terminal is away from the fault, the larger this terminal voltage oscillation will be"**.

When the fault is moving from terminal A1 forward to terminal C1, '$I_{A1C1,max}$' appears almost linear growth. While, '$I_{C1A1,max}$' appears almost linear decline. This indicates that, **"For cable faults, the closer a terminal is to the fault, the larger the maximum fault current injected from this terminal will be"**.

When the fault is moving from terminal A1 forward to terminal C1, signal '$t_{tripsignal1}$' is generated later and later. While, signal '$t_{tripsignal2}$' is generated earlier and earlier. The time instant of '$t_{tripsignal1}$' and '$t_{tripsignal2}$' overlaps as the fault is located at the mid of cable_A1C1. This demonstrates that, **"For cable faults, the closer a terminal is to the fault, the earlier the fault will be detected by relays at this terminal"**. In addition, the detection instants of two ends of the faulty cable are not synchronized. This time delay comes to the minimum when the faults is at the mid of the fault cable. In this set of cases, the maximum detection time difference between two ends reach 2ms for a ptp fault of 50 impedance.

Considering the case when the fault is close to terminal A1, '$I_{A1C1,max}$' is 4.487kA, the highest. And signal '$t_{tripsignal1}$' is detected the earliest, at 0.1014s. A fast fault detection means a fast DCCB operation, since the mechanical relay is fixed. It is observed that '$I_{A1C1,max}$' is usually obtained when DCCB1 starts to operate. As a result, the fault current climbing rate can be roughly measured by knowing '$I_{A1C1,max}$' and '$t_{tripsignal1}$'. A high amplitude of '$I_{A1C1,max}$' with a early fault detection of '$t_{tripsignal1}$' implies an fast fault increase. Given this approximation, 'I_{A1C1}' increases the fastest when the fault is close to terminal A1. As the fault is moving forward to terminal C1, fault current 'I_{A1C1}' grows slower and slower. Then another conclusion is drawn that, **"For cable faults, the closer a terminal is to the fault, the faster the fault current injected from this terminal will increase"**.

Transients performance comparison between cases of various fault impedances:

To test how the fault impedance will affect the fault transients, the fault location is fixed at 100km which is the mid on cable_A1C1. The fault type is of pole to pole fault. Five fault impedances from 0.0101 ohm to 100ohm are studied. During these cases, DCCB1 and DCCB2 operates well except in the case of 100ohm fault impedance. The reason is faults can not be detected by both relays.

Fault type	pole to pole (ptp)				
Fault location	100km				
Fault impedance	0.0101ohm	25ohm	50ohm	75ohm	100ohm
$\Delta V_{A1,max}$ (kV)	664.9	474.18	415.07	400.44	171.5
$\Delta V_{C1,max}$ (kV)	600.9	469.35	421.58	407.46	146.4
$I_{A1C1,max}$ (kA)	8.957	5.16	3.587	2.847	1.65
$I_{C1A1,max}$ (kA)	8.063	6.523	4.869	4.048	3.103
$t_{Tripsignal1}$ (s)	0.1016	0.1019	0.1021	0.1023	\
$t_{Tripsignal2}$ (s)	0.1016	0.1019	0.1021	0.1023	\

Table 6.4: *Pole to pole fault cases when the fault is at 100km distance to terminal A1*

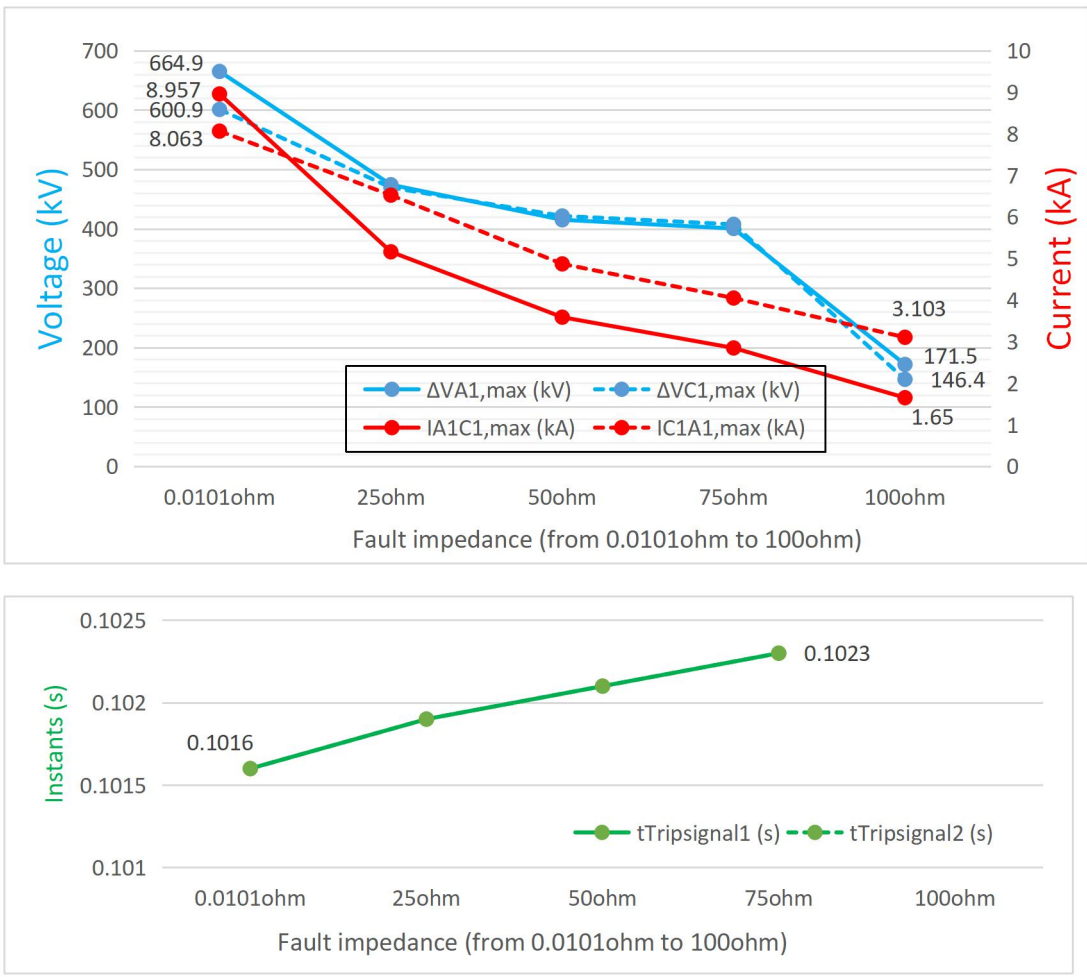


Figure 6.14: *Transients performance from cases of various fault impedances*

When the fault impedance is increasing from 0.0101ohm (bolted faults) to 100ohm, both

'$\Delta V_{A1,max}$' and '$\Delta V_{C1,max}$' are decreasing. This means, **"For cable faults, the larger the fault impedance, the smaller the terminal voltage oscillation will be"**.

When the fault impedance is increasing from 0.0101ohm (bolted faults) to 100ohm, both '$I_{A1C1,max}$' and '$I_{C1A1,max}$' are decreasing from above 8kA to below 4kA. This means, **"For cable faults, the larger the fault impedance, the smaller the maximum fault current will be"**. Increasing the fault impedance will decrease the maximum fault current effectively.

When the fault impedance is increasing from 0.0101ohm (bolted faults) to 100ohm, both '$t_{tripsignal1}$' and '$t_{tripsignal2}$' are generated later and later. In the case of bolted faults, faults are detected at 't=0.1016s'. In the case of 75ohm fault impedance, faults are detected at 't=0.1023s'. Though 0.0007s (0.7ms) is not a big difference, it indicates that, **"For cable faults, an increase on fault impedance makes fault detection delayed"**.

It is known that, increasing fault impedance leads to a smaller maximum fault current and a slower fault detection. Assume the fault current climbing rate can be roughly measured by knowing 'I_{max}' and '$t_{tripsignal}$', then another conclusion is drawn. **"For cable faults, an increase on fault impedance will decrease the rising speed of fault currents injected from both ends".**

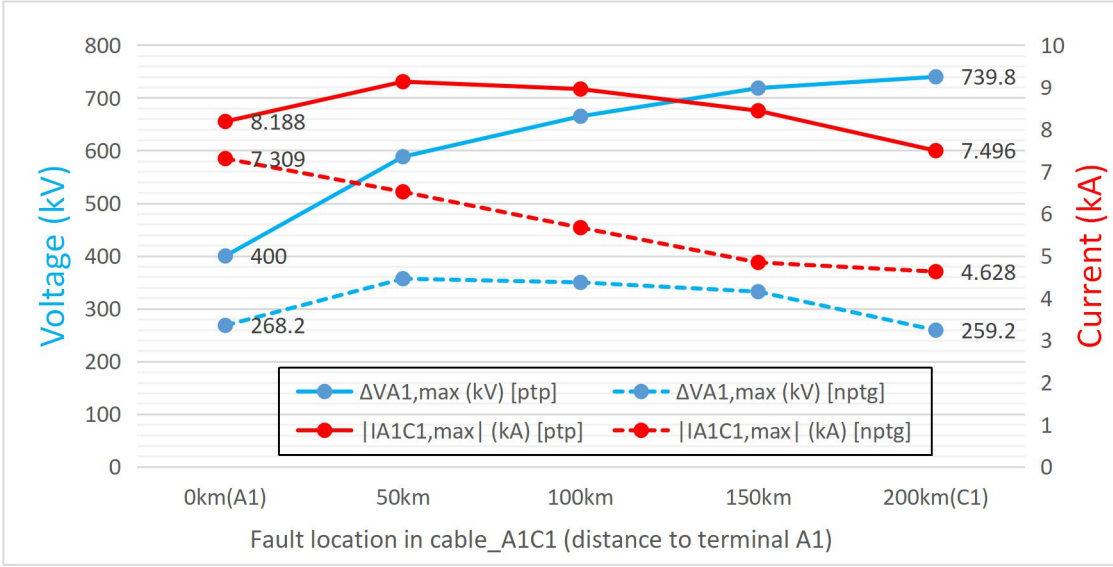
Compare the bolted fault with faults of impedance (25ohms to 100ohms), '$I_{A1C1,max}$', '$I_{C1A1,max}$', '$\Delta V_{A1,max}$' and '$\Delta V_{C1,max}$' are remarkably higher in case of bolted faults. This means bolted faults will produce the largest damages to the HVDC system, since the fault current surge grows incredibly fast. In addition to the DCCB operation, there is a large probability that part of ACCBs will operate and part of MMCs will block themselves.

Transients performance comparison between faults types of ptp and nptg:

To test how the fault types will affect the fault transients, the fault impedance is fixed at 0.0101hms (bolted fault). The fault types are pole to pole faults and negative pole to ground faults. '$\Delta V_{A1,max}$', '$|I_{A1C1,max}|$' and '$t_{Tripsignal1}$' are the main comparison objects between two types of faults. '$I_{A1C1N,max}$' measures the amplitude of the maximum negative pole to ground fault current from terminal A1.

Fault impedance	0.0101ohm				
Fault location	0km (A1)	50km	100km	150km	200km (C1)
$\Delta V_{A1,max}$ (kV) [ptp]	400	588.2	664.9	718.4	739.8
$\Delta V_{A1,max}$ (kV) [nptg]	268.2	356.8	349.8	332.2	259.2
$\lvert I_{A1C1,max} \rvert$ (kA) [ptp]	8.188	9.132	8.957	8.442	7.496
$\lvert I_{A1C1N,max} \rvert$ (kA) [nptg]	7.309	6.52	5.671	4.846	4.628
$t_{Tripsignal1}$ (s) [ptp]	0.101	0.1013	0.1016	0.1018	0.1021
$t_{Tripsignal1}$ (s) [nptg]	0.1014	0.1016	0.1019	0.1021	0.1024

Table 6.5: *Transient performance of ptp-faults and nptg-faults with low impedance*



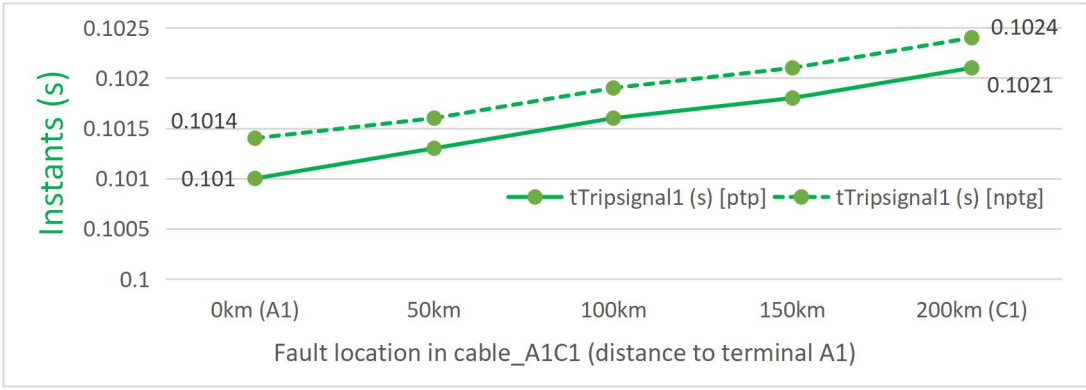


Figure 6.15: *Transients performance comparison between ptp-faults and nptg-faults*

As can be seen, '$\Delta V_{A1,max}$' is much smaller in nptg-fault cases than in ptp-fault cases. And '$|I_{A1C1,max}|$' is also much smaller in nptg-fault cases than in ptp-fault cases. This means that, **"For cable faults of same fault impedance, negative pole to ground faults cause less fault currents and voltage oscillation than pole to pole faults".**

Compare the fault detection between ptp-fault cases and nptg-fault cases, '$t_{Tripsignal1}$' is generated earlier in nptg-fault cases. This indicates that, **"For cable faults of same fault impedance, negative pole to ground faults will be detected later than pole to pole faults".**

Fig 6.15 illustrates the difference on the fault transient between ptp-faults and nptg-faults. 'V_{A1}' actually measures the difference between the positive polarity and the negative polarity. '$\Delta V_{A1,max}$' means the amplitude of the maximum variation of 'V_{A1}' during this period. In cases of ptp-faults, the fault surge propagates through both positive polarity and negative polarity. The ptp-fault can be seen as a short circuit path, which connects the positive polarity and negative polarity at the fault location. For terminal A1, the fault current is injected with a voltage source of 'V_{A1}'. During the whole transient process, '$\Delta V_{A1,max}$' is likely to above

400kV due to system transient impedance.

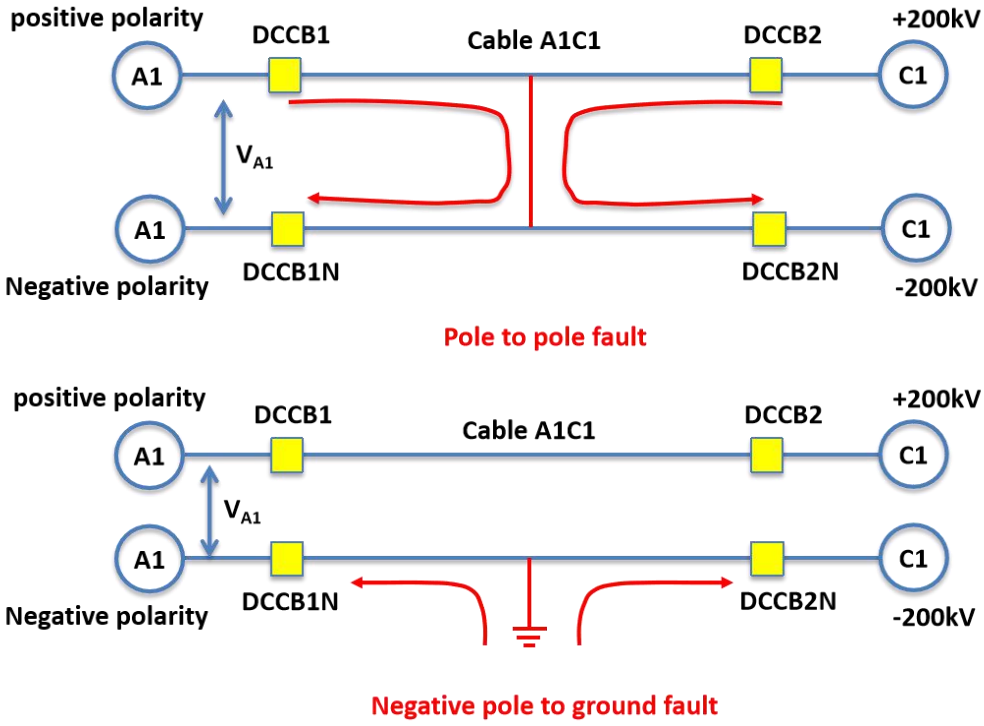


Figure 6.16: *Transients difference between ptp-faults and nptg-faults*

In cases of ptp-faults, the fault surge propagates through cables of only negative polarity. It affect much less to the positive polarity than to the negative polarity. For terminal A1, the fault current is injected from the fault to the negative polarity with a voltage source of ('V_{A1}' - 200kV). As a result, the magnitude of tptg fault current |'I_{A1C1N}'| is considerably reduced compared with pole fault current |'I_{A1C1}'|. Also, the magnitude of '$\Delta V_{A1,max}$' is much smaller in the nptg-faults.

Apparently, negative pole to ground faults causes less damages to the HVDC system compared to pole to pole faults. The problem is that, small effect of nptg-faults makes the high impedance fault invisible to the system. In this set of tests, nptg-faults with impedance of 25ohms are not detected by the relay algorithm.

6.4 Conclusion

In the fully selective DCCB placement tests, the fault impedance, the fault location and the fault type will affect the system transient performance. Bolted faults cause the largest damages to the HVDC system. In this set of fault cases, ACCBs and MMCs located close to the ends of faulty line are most likely to operate in case of bolted faults. Because bolted faults result in extremely high fault currents.

The selectivity in this protection strategy is great. In all the cases that the fault is successfully detected, only DCCB1 and DCCB2 operates. While DCCBs on healthy cables stay still. The probability of false detection of fault is zero, which indicates the relay algorithm works well.

The fault impedance detection range differs with the fault types. Because negative pole to ground faults causes less damages to the HVDC system compared to pole to pole faults. For the pole to pole faults, the maximum fault impedance that can be detected is below 100ohm. While for the negative pole to ground faults, a 25ohm faults will be invisible to the protection system.

The fault detection range is generally not high for both types of fault. It is related to the threshold settings of MAD.I and MAD.V. Obviously, the current settings do not lead to a good protection performance when encountering high-impedance fault. In the following partially selective DCCB placement tests, MAD.I and MAD.V are modified to seek for higher impedance detection. However, new problems may occur with the rise of fault detection sensitivity.

Chapter 7

Partially selective DCCB placement protection simulation and analysis

This chapter studies the fault cases on PSPS. Before the test, a description on time step and threshold setting for relay algorithm is stated. Then, it follows by the base case study, where important current and voltages are analyzed. After that, more cases study are investigated and compared. Among of them, the false operation of ACCBs and false relay detection happens occasionally. Last but not the least, a radar chart is give to illustrate the fault detection range and possible inappropriate reactions from devices. Finally, the thresholds effects on fault detection is concluded.

7.1 Description and statement before simulation

In Chapter 7, Partially selective DCCB placement strategy is studied. As is discussed in Chapter 3.3, there are three optional partially selective DCCB placement design. In this chapter, 3.3b (minimum DCCBs) is being tested. Based on the original fully selective model, the number of DCBBs is reduced from 8 to 4 and they are renamed in Fig 7.1. For any cable fault in this protection scheme, two DCCBs and one ACCB will operate. In Fig 7.1, the light yellow rectangle shows the isolation area (zone 4) when the fault is located at cable_A1C1.

Apart from the modification on model configuration, 'Tripsignal's sending object is adjusted. For example, 'Tripsignal' generated at relay '#8' will be sent to DCCB4 and ACCB1. These changes make the system compile overloaded in calculation. As a result, a compromise approach is to adjust the big time step from **75μs to 140μs**.

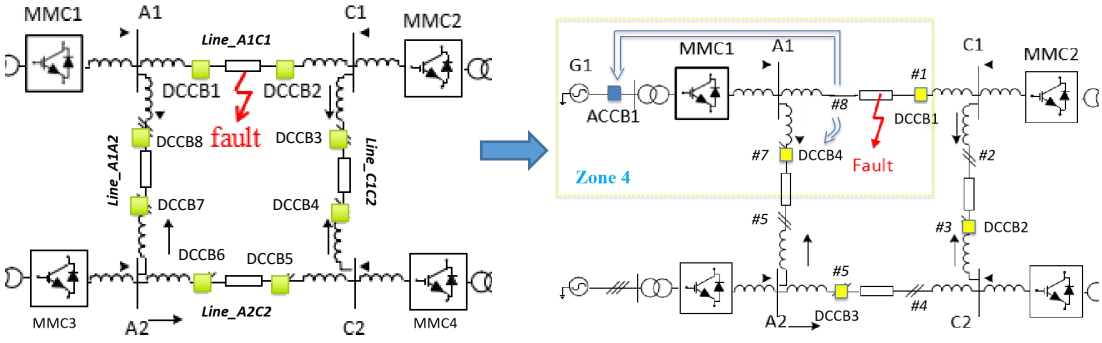


Figure 7.1: *Model modification from fully selective to partially selective DCCB placement*

To try to achieve wilder fault impedance detection, the requirements for MAD.I and MAD.V are lowered. Thresholds for MAD.I and MAD.V are given an number as is demonstrated. (In Chapter 6, thresholds for MAD.I and MAD.V are 200 and -0.4 respectively.)

$$MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 100 \\ 0, else \end{cases} \tag{9}$$

$$MAD.V = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.2 \\ 0, else \end{cases} \tag{10}$$

In plots of branch currents and bus voltages, the measure position is changed as it demonstrated in Fig 7.2.

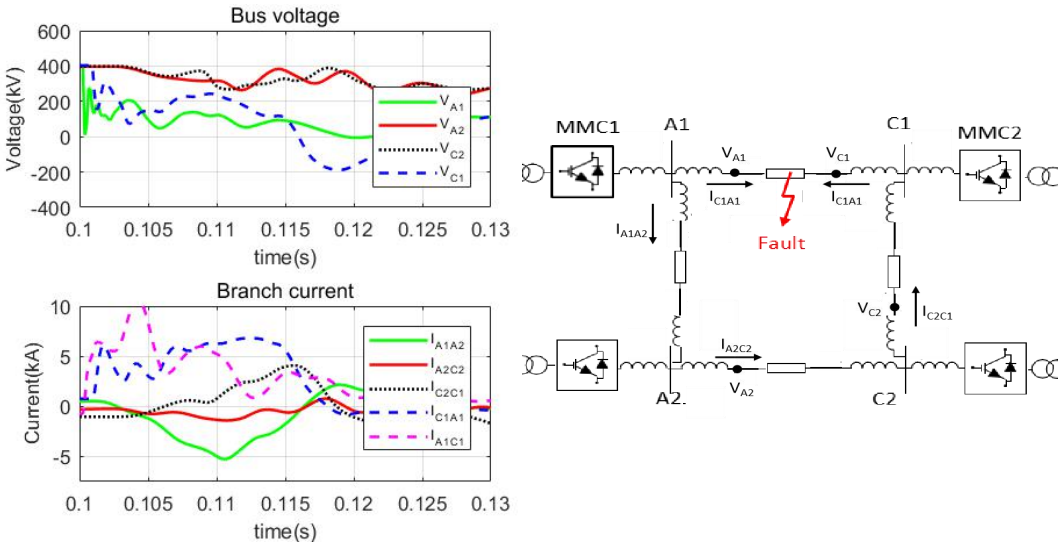


Figure 7.2: *Bus voltage and branch current specified in the test system*

7.2 Base case study

The base case is defined when a pole to pole fault takes place close to bus C1 at t_0=0.1s. Fault settings are demonstrated in Table 7.1. Fig 7.4 shows the simulation results.

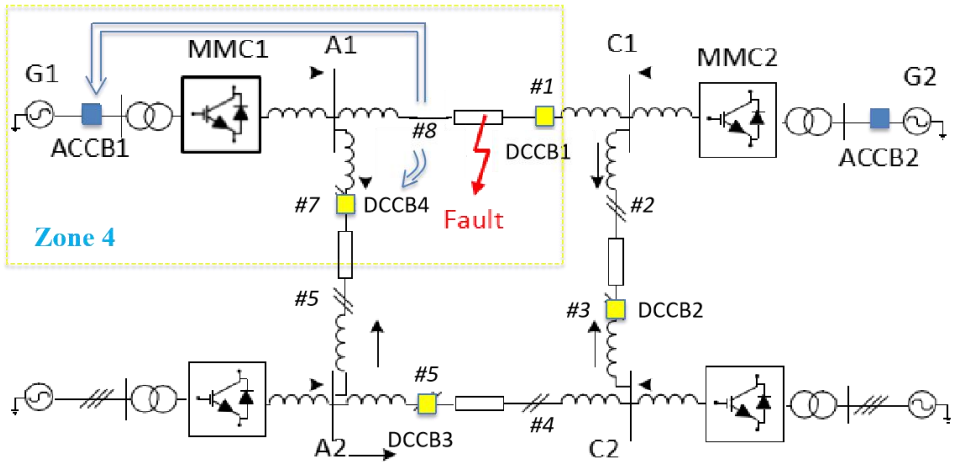


Figure 7.3: *DC protection system in base case in PSPS*

Converter self protection	With
Fault inception instant	t = 0.1s
Fault type	**Pole to pole**
Fault locations	**15% (30km) distance to terminal A1 in cable_A1C1**
Fault Impedance	**R_f= 10 ohm**
DCCB placement	**Partially selective**
DCCB mechanical delay	8ms

Table 7.1: *Critical settings and parameters of test HVDC mesh system*

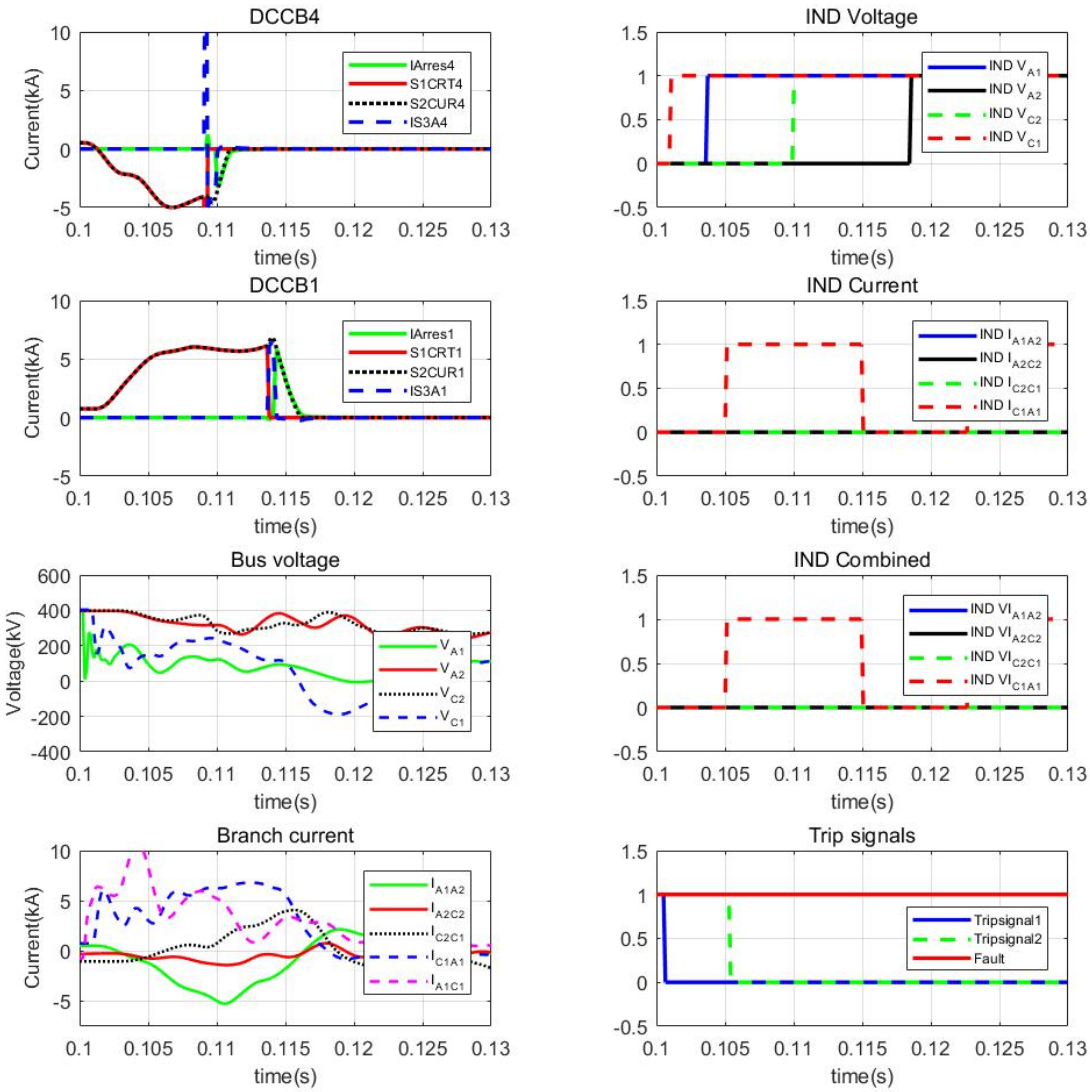


Figure 7.4: *Plots of DCCBs, system voltages and currents, indices of trip signal in PSPS base case study.*

Base case Analysis:

DCCB4 starts with a positive current, because 'I_{Normal}' is flowing in the same direction with 'S2CUR4' before fault inception. Then 'S2CUR4' keeps decreasing to around -5kA. The reason is, the fault current injected from terminal 2 is reversed to the direction of 'S2CUR4'. Both DCCB1 and DCCB4 operate, means relay '#1' and '#8' detect the fault and send tripsignals to DCCB1 and DCCB4 precisely. The fault is closer to terminal A1, which leads to a quicker operation of DCCB4 than DCCB1.

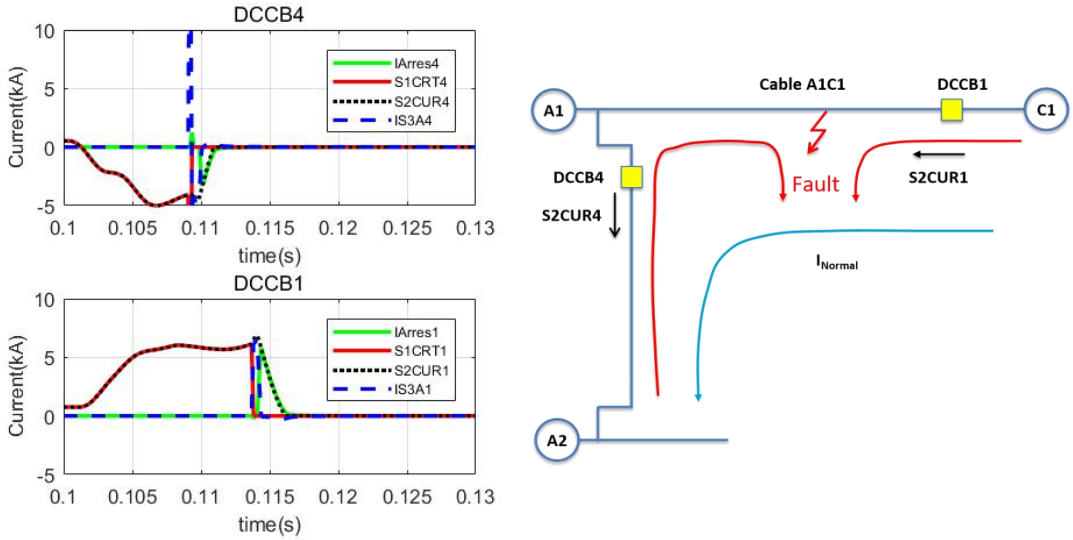


Figure 7.5: *Reversed fault current detection in DCCB4*

Electrical indices plots demonstrates that, for the relays located at '#1' '#3' '#5' and '#7', only '#1' detects the fault. 'Tripsignal1' is enabled, means the fault is also detected at '#8'. The operation of DCCB1 and DCCB4 means the fault is already isolated from the healthy HVDC networks.

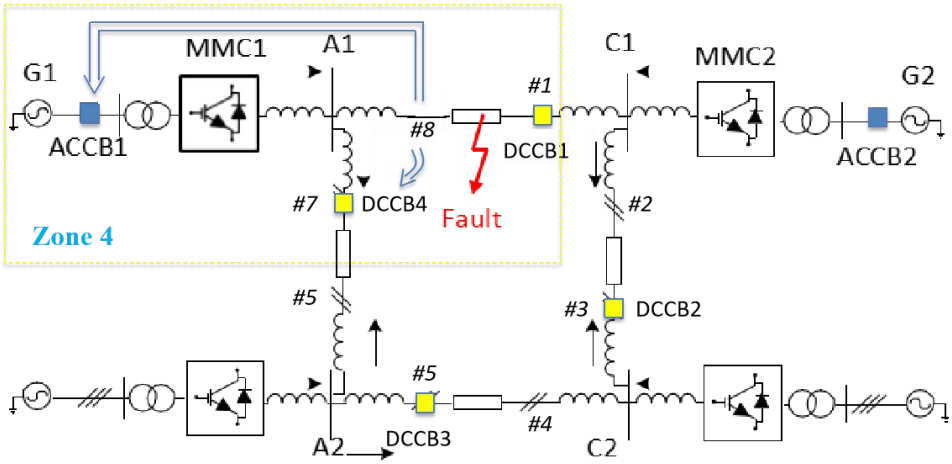


Figure 7.6: *DC protection system in PSPS*

Fig 7.7 shows the ACCB operation and MMC blocking state. As can be seen, '$ACBRK_{A1}$' is almost generated on the time when 'tripsignal1' is generated. And the operation of ACCB1 means the fault is not only isolated from the HVDC system, but also from the AC source 'G1'. The basic protection expectation is achieved in this partially selective protection strategy.

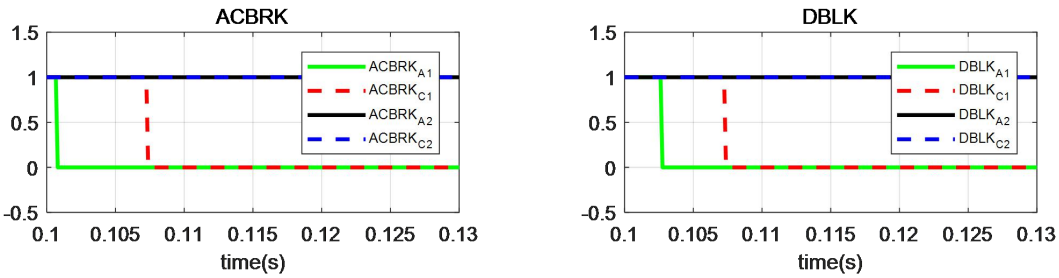


Figure 7.7: *Trip signals for ACCBs and Block signals for MMCs*

7.3 Partially selective cases and faults analysis

DCCB placement	Partially selective
Fault cable	Cable_A1C1, Cable_C1C2, Cable_C2A2, Cable_A2A1
Fault location	0km (A1), 30km, 100km, 170km, 200km (C1)
Fault impedance	0.01ohm, 10ohm, 25ohm, 50ohm, 75ohm, 100ohm, 110ohm and 115ohm
Fault type	Pole to pole fault, negative pole to ground fault

Table 7.2: *Fault parameters of all the fault tests in PSPS*

According the fault analysis on Fully selective protection scheme in chapter 6, it is known that fault parameters affect the fault transient performance. In terms of '$\Delta V_{C1,max}$', '$\Delta V_{A1,max}$', '$I_{C1A1,max}$', '$I_{A1C1,max}$', '$t_{Tripsignal1}$' and '$t_{Tripsignal2}$', the damage a fault brings to the HVDC system is generally measured. Three patterns are roughly summarized, which reveals the relationship between the severity of a cable fault and fault parameters.

- The cable fault is located closer to the terminal, the fault is severer.
- The cable fault is of a lower impedance, the fault is severer.
- Pole to pole faults is much severer than single pole to ground faults.

In partially selective protection strategy (PSPS), the cooperation of ACCBs and MMCs is also very important. Because a successful fault clear in PSPS needs not only operations of two DCCBs, but also operation of one ACCB. While, in fully selective protection strategy (FSPS), the fault is cleared as long as two DCCBs operate at each cable end.

Analysis on critical fault conditions:

Extreme fault condition usually refers to a critical-impedance fault located at a critical location. Among all of this set of fault cases, a ptp bolted fault (0.01ohm) located close to terminal C1 can be a extreme fault condition. And this fault is a very serious cable fault on

HVDC system. Fig 7.8 shows the measurement plots of this fault protection.

Converter self protection	With
Fault inception instant	t = 0.1s
Fault type	**Pole to pole**
Fault locations	**Close to terminal C1 in cable_A1C1**
Fault Impedance	**R_f = 0.01 ohm**
DCCB placement	**Partially selective**
DCCB mechanical delay	8ms

Table 7.3: *Critical fault with fault parameters*

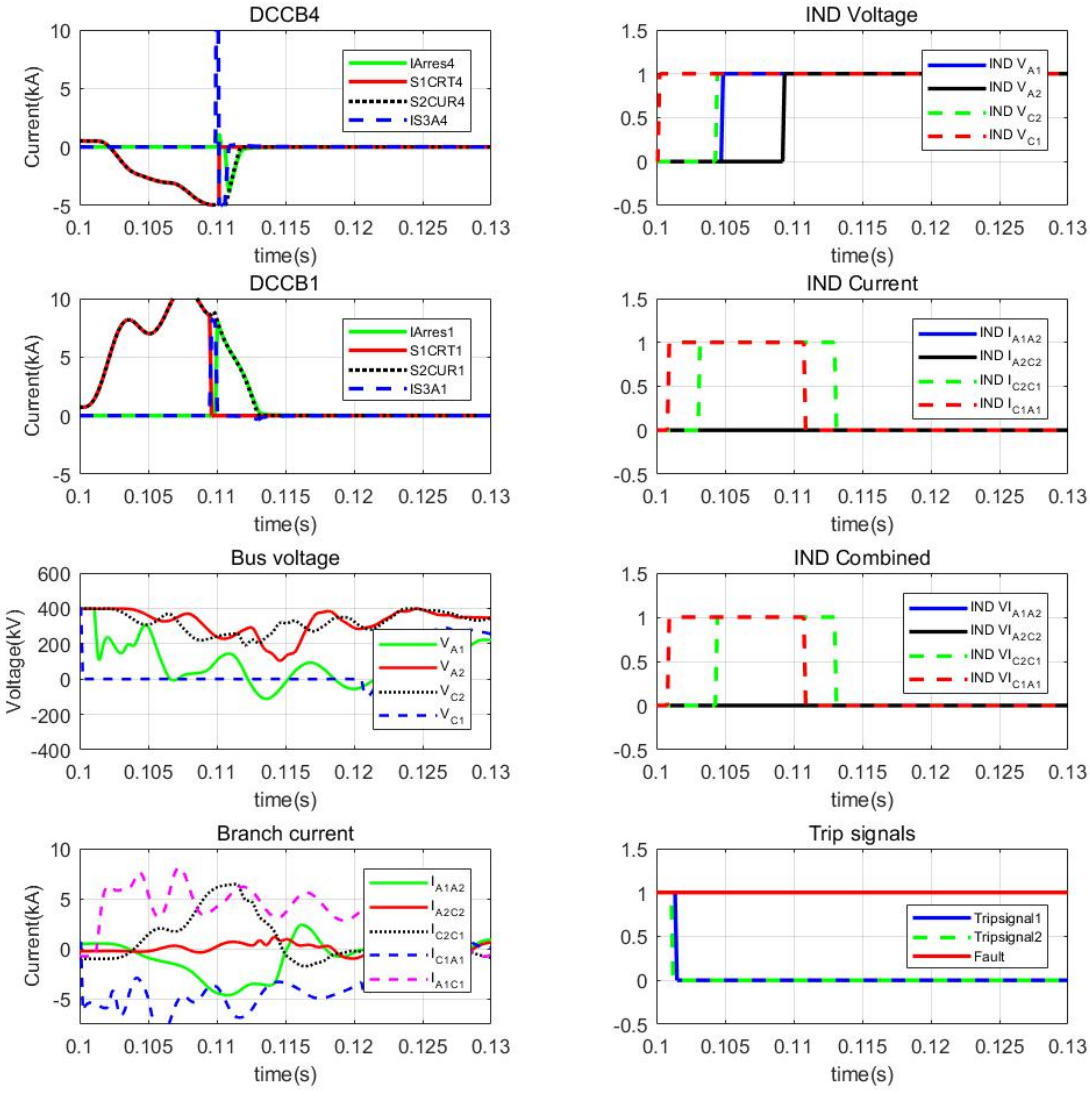


Figure 7.8: *Simulation results of the critical fault*

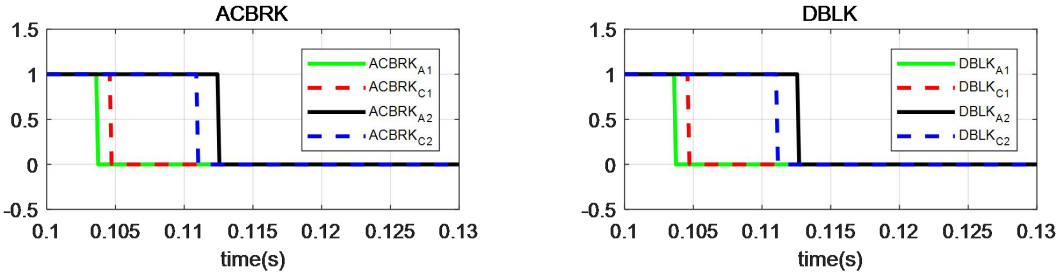


Figure 7.9: *Simulation results of signal 'ACBRK' and 'DBLK'*

Although this critical fault draws huge fault current from terminal C1, DCCB1 operates well. DCCB4 also operates, means the fault is already isolated from the healthy HVDC networks. '$ACBRK_{A1}$' is also generated, implies the fault is also blocked from the AC source 'G1'.

However in the plots of '"IND Combined", the first problem occurs. Except that 'IND VI_{C1A1}' should be enabled, 'IND VI_{C2C1}' is enabled. This means relay '#3' also detects the fault, although it should not. If DCCB2 operates, the healthy cable_C1C2 will be disconnected. AC source 'G2' can not transfer power to 'L1' and 'L2'. Then the whole HVDC system will shut down for no generators can transfer power.

Then, it is necessary to know the probability of this false detection occurrence on relay '#3' during the whole set of cases. The cases with less severer faults should be checked first. According the three patterns mentioned in the beginning of Chapter 7.3, The fault severity can be lowered by increasing the fault impedance, setting fault away from the terminal, changing fault type to nptg-faults. Then, these three cases are being checked.

Cases	Case a	Case b	Case c
Converter self protection	With	With	With
Fault inception instant	t = 0.1s	t = 0.1s	t = 0.1s
Fault type	**Pole to pole**	**Pole to pole**	**Negative pole to ground**
Fault locations	**170km (85%) distance to terminal A1 in cable_A1C1**	**Close to terminal C1 in cable_A1C1**	**Close to terminal C1 in cable_A1C1**
Fault Impedance	**R_f = 0.01 ohm**	**R_f = 10 ohm**	**R_f = 0.01 ohm**
DCCB placement	**Partially selective**	**Partially selective**	**Partially selective**
DCCB mechanical delay	8ms	8ms	8ms

Table 7.4: *Fault parameters of critical fault and faults with lower severity*

In these three cases, 'IND VI_{C2C1}' is not generated. This false detection only happens when a bolted pole to pole cable fault located close to terminal C1.

The second problems is all ACCBs receive the trips signals, and all MMC receive the

blocking signals. The second problem is defined as the false operation of ACCBs. This problem happens as long as the fault severity is over a certain level.

Fig 7.10 shows the overall ptp-faults detection range in terms of fault impedance on different locations. Each of the five vertical axis directions measures the fault impedance. The five corners of the pentagram means five fault locations along cable_A1C1. The polygon made up of gray lines demonstrates the maximum ptp-fault detection range along cable_A1C1. As can be seen, within the gray polygon, the maximum fault impedance reaches 110ohm.

The two problems mentioned before are represented by blue polygon and orange polygon. The polygon made up of blue lines demonstrates the maximum ptp-fault range, where false operation of ACCBs happens. The polygon made up of orange lines demonstrates the maximum ptp-fault range, where false fault detection happens. Although it only happens when a bolted pole to pole cable fault located close to terminal C1.

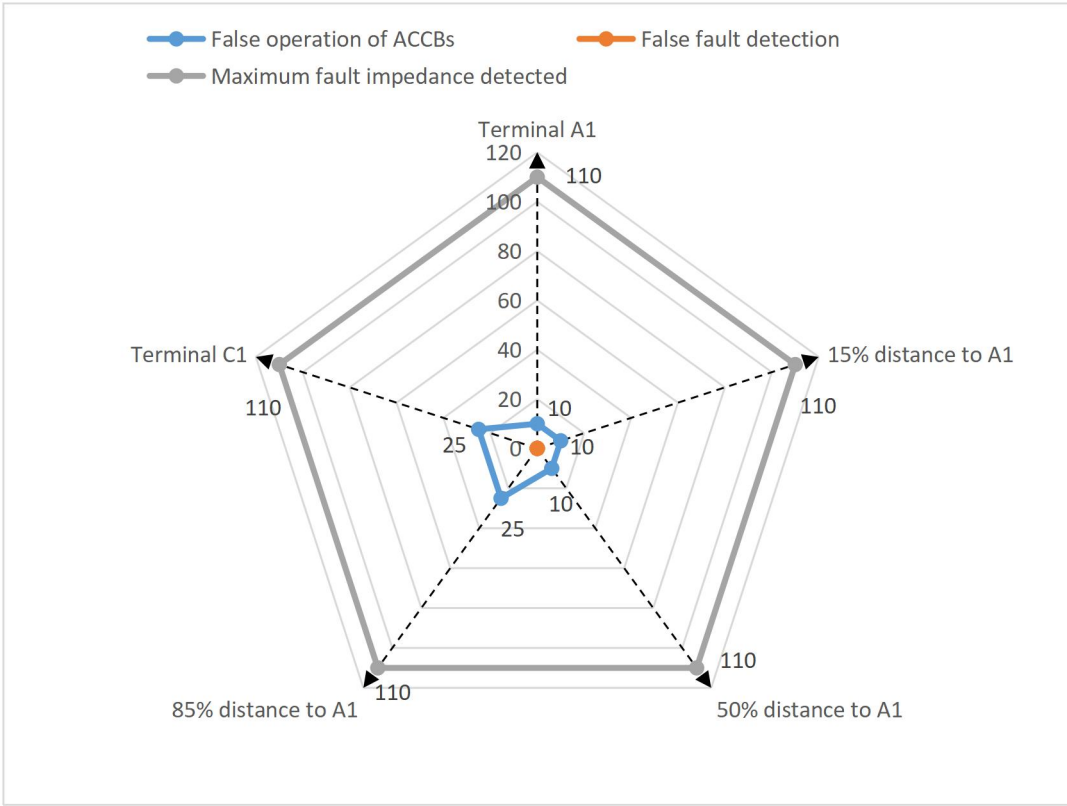


Figure 7.10: *Fault Detection range and other events illustrated on a radar chart*

The false fault detection happens very accidentally and the false operation of ACCBs happens more often. Both of them tend to happen in a low impedance fault for the reason of extreme high fault current. It is easily obtained that, the area between the gray polygon and the blue polygon represents the correct fault detection with appropriate ACCB operation. The safe impedance detection range for all pole to pole faults long cable_A1C1 is [25ohm, 110ohm]. If the fault impedance is higher than 110ohm, it is hardly detected. If the fault impedance is lower than 25ohm, especially 10ohm, false operation of ACCBs will happen.

On critical fault occasion, false fault detection even happens.

Among all the false operations of ACCBs, ACCB2 contributes the most. This means, low impedance ptp faulst on cable_A1C1 threaten AC source ‘G2’ more than the other two AC sources ‘L1’ and ‘L2’. As the fault is closer to terminal C1, fault current injected from terminal C1 will be larger. That is why the false operation of ACCBs even starts earlier as the fault impedance decreases. Faults with impedance 10ohm will make ACCB2 operates when the fault is at terminal A1, 15% distance to A1 or mid point of cable_A1C1. However, false operation of ACCB2 starts with fault impedance 25ohm when the fault is at terminal C1 or 85% distance to A1.

Fault detection performance on negative pole to ground faults:

In fact, the overall fault detection on nptg-faults does not improve evidently in terms of fault impedance. Fault with impedance over than 20ohm can not be detected by relay ‘#1’ and relay ‘#8’.However, the good thing is neither ACCB false operation nor false detection happens. In the fully selective protection scheme test, fault with impedance of 25ohm can not be detected. As a result, the modification of thresholds on MAD.V and MAD.I have little on nptg-faults.

Fault detection performance on other cables:

The radar chart in Fig 7.11 demonstrate the ptp-faults detection range in all cables including cable_A1C1, cable_C1C2, cable_C2A2 and cable_A2A1.

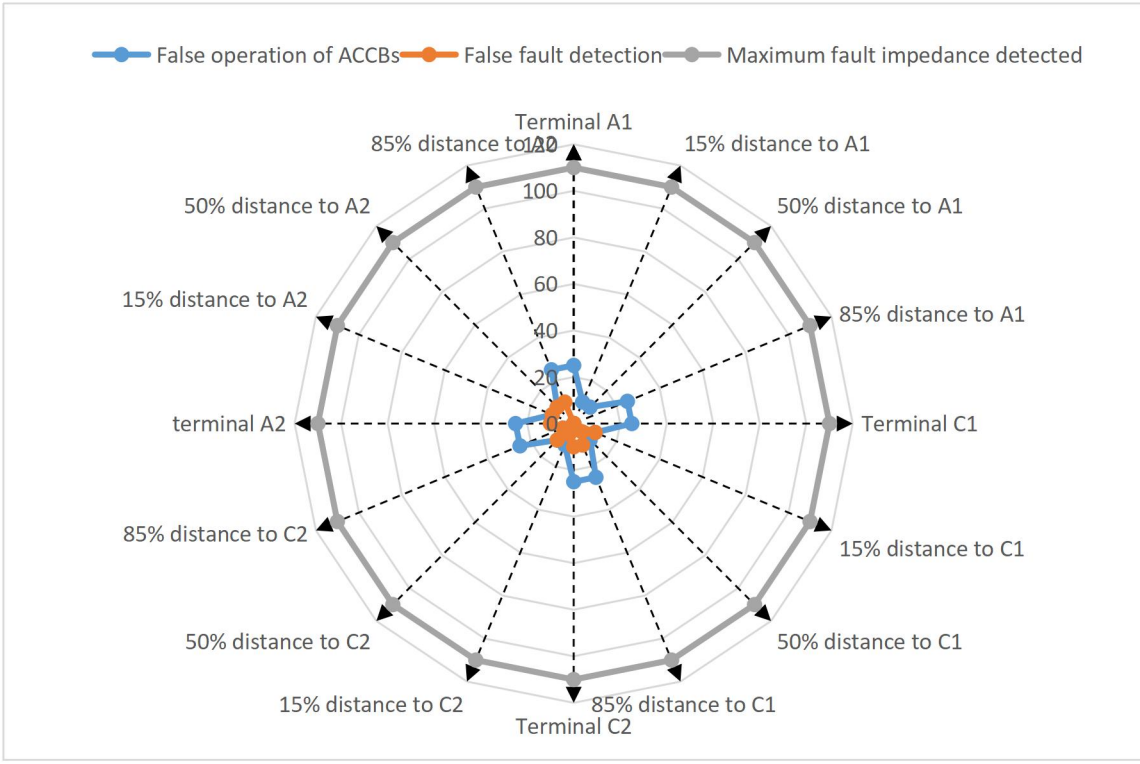


Figure 7.11: *Ptp-faults detection range on four cables illustrated on a radar chart.*

The radar chart divides the cable faults into four main parts which represent faults on cable_A1C1, faults on cable_C1C2, faults on cable_C2A2 and faults on cable_A2A1. The quarter on the right top shows the faults along cable_A1C1. The quarter on the right bottom shows the faults along cable_C1C2. The quarter on the left bottom shows the faults along cable_C2A2. The quarter on the left top shows the faults along cable_A2A1. And this radar chart can be seen as the pole to pole faults detection behavior on the whole cable faults.

When the fault is located at four cables, the maximum fault impedance that can be detected is always around 110ohm. It is observed that, every time when a fault is moving from one terminal closer to the other terminal, false operation of ACCBs are more likely to happen.

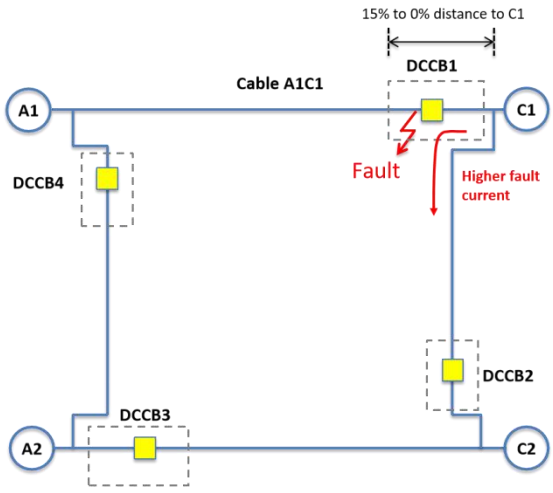
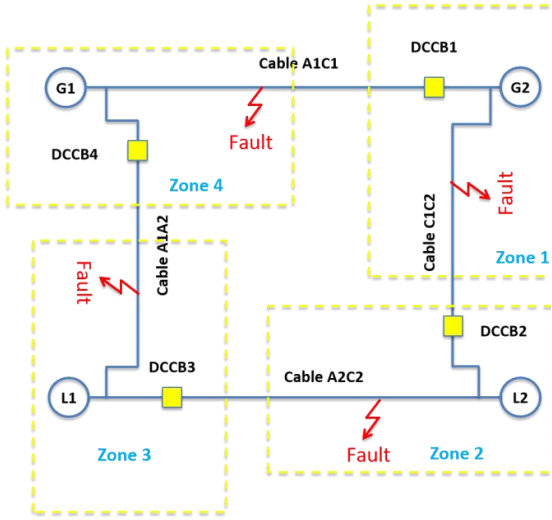


Figure 7.12: *The fault area where false ACCB operation happens more often*

In Fig 7.12, the gray rectangle means the area, which is within 15% distance close to terminal where DCCBs are located. The four areas shows the fault position range where false operation of ACCBs are easier to happen. According to the radar chart, within the gray area, false ACCB operation happens when the impedance is lower than 25ohm. Outside the gray area, false ACCB operation happens when the impedance is lower than 10ohm. The reason for that is explained before (extremely high fault current injected from the terminal nearby).

For faults located on cable_A1C1, it has been discussed that false fault detection by relays only happens when a bolted pole to pole cable fault located close to terminal C1. While this problem becomes worse when ptp-faults are located on the other three cables. The false detection occurs when the fault impedance is lower generally lower than 5ohm.



Faulty cable	Isolation area	Isolated devices
Cable_A1C1	Zone 4	Cable_A1C1, Cable_A1A2 Generator 1
Cable_C1C2	Zone 1	Cable_A1C1, Cable_C1C2 Generator 2
Cable_A2C2	Zone 2	Cable_C1C2, Cable_A2C2 Load 2
Cable_A1A2	Zone 3	Cable_A1A2, Cable_A2C2 Load 1

Figure 7.13: *Four isolated zones when fault is located on different cables*

Table 7.5: *Isolation area with isolated devices*

Although the valid fault detection range of four cables do not differ much, the faults on different cables will cause different effects in the HVDC system. Fig 7.13 shows the isolation areas when faults are at different cables. Faults on cable_A1C1 or cable_C1C2 will cause at least one generator shut down. Faults on cable_A2C2 or cable_A1A2 will cause at least one load not powered. This type of partially selective protection strategy do not have preference on protecting the generators or loads.

7.4 Conclusion

As has been introduced in Chapter 3.3, there are multiple choices of partially selective protection design. And this chapter selects one of the feasible strategies featured of minimum DCCBs usage. Compared with the fully selective protection strategy in chapter 6, thresholds of MAD.V and MAD.I are lowered in Chapter 7.

$$MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 200 \\ 0, else \end{cases} \quad \Rightarrow \quad MAD.I = \begin{cases} 1, A_{iMAD}(t) \geq 2A_{iMAD}(t-\Delta t) \wedge A_{iMAD}(t) \geq 100 \\ 0, else \end{cases}$$

$$MADV = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.4 \\ 0, else \end{cases} \quad MADV = \begin{cases} 1, A_{iMAD\_M}(t) \leq 2A_{iMAD\_M}(t-\Delta t) \wedge A_{iMAD\_M}(t) \leq -0.2 \\ 0, else \end{cases}$$

The result of that modification is the maximum fault impedance detection range increased from 75ohm to 110ohm. However, this also brings drawbacks on performance of low impedance fault detection. Fault with impedance lower than 10ohm will possibly leads to relay false detection on cables beside the faulty cable. A reduce of algorithm thresholds improves the protection sensitivity, but also increases the false detection probability of

healthy cables especially on bolted faults.

The partially selective protection strategy (PSPS) emphasizes on the cooperation of ACCBs more than in the FSPS. Faults in FSPS are cleared as along as two DCCBs in faulty cable operate correctly. However, fault current will still be injected if ACCBs do not operate appropriately. In this set of tests, fault with impedance lower than 25ohm will leads to false operation of ACCBs. These two problems makes the valid pole to pole fault detection range in PSPS restricted in [25ohm, 110hm].

Neither the modification of MAD nor the different protection strategy brings changes on the negative pole to ground fault detection performance. Fault with impedance over 20ohm can not be detected. In FSPS, faults of 25 ohm can not be detected. The modification of MAD seems works little on the single pole to ground faults, possibly because of the much lowered fault current.

Chapter 8

Consideration on the test results related to the real faults

8.1 Algorithm thresholds setting based on faults group

Algorithm thresholds impacts on the fault detection:

From Chapter 6 and Chapter 7, it is known that a reduce of algorithm thresholds improves the protection sensitivity but also increases the false detection probability of healthy cables especially on bolted faults. As a result, an appropriate setting of detection thresholds depends on the distribution of fault parameters [42]. For example, if the faults are usually with low impedance even bolted faults, then sensitivity is sacrificed for a more reliable performance on low impedance fault detection. One of the methods to decide the thresholds is discussed in Chapter 4.2.2. By testing all the potential faults of target parameters, the information of MAD.V and MAD.I are collected. According to the preset fault detection range, a critical value of MAV.V and MAD.I can be determined to differentiate faults and normal operation. This is an ideal approach for preliminary thresholds determination.

Determination of algorithm thresholds of relays:

In the four terminal HVDC meshed system, all the relays at '#1', '#2', '#3', '#4', '#5', '#6',

'#7' and '#8' shares the same value of thresholds of MAD.V and MAD.I. This means all relays share the same fault detection criterion, which may not applicable in the real life. Instead, the thresholds setting of each relay may differ with each other. If it is the case, then faults in each cable should be tested. The tested faults parameters depends on the real faults frequently occurred [43]. So that, the calculated thresholds will cater to target faults.

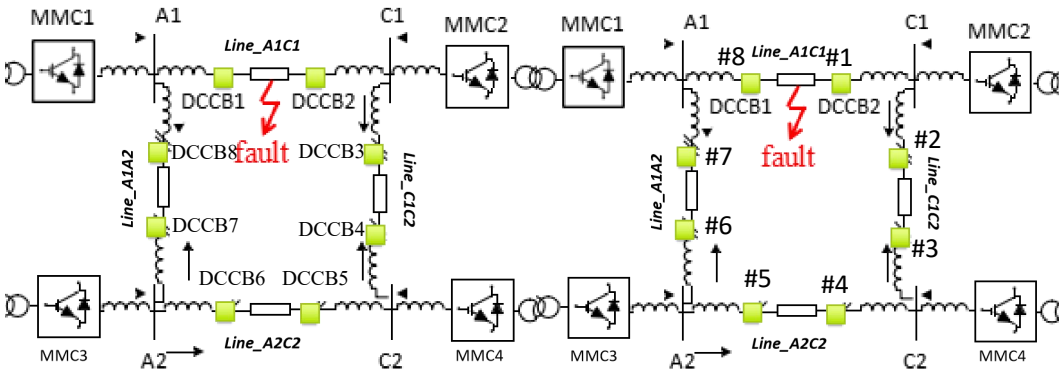


Figure 8.1: *Positions of DCCBs and the corresponding relays in FSPS*

DCCBs should operate	Faulty cable test	MAD.V and MAD.I requirements for DCCBs operating
DCCB1, DCCB2	Cable_A1C1	Range [a]
DCCB3, DCCB4	Cable_C1C2	Range [b]
DCCB5, DCCB6	Cable_A2C2	Range [c]
DCCB7, DCCB8	Cable_A1A2	Range [d]

Table 8.1: *DCCB operating requirement leads to thresholds setting range*

DCCBs should not operate	Faulty cable test	MAD.V and MAD.I requirements for DCCBs not operating
DCCB1, DCCB2	Cable_C1C2, Cable_A2C2 and Cable_A1A2	Range [a']
DCCB3, DCCB4	Cable_A1C1, Cable_A2C2 and Cable_A1A2	Range [b']
DCCB5, DCCB6	Cable_A1C1, Cable_C1C2 and Cable_A1A2	Range [c']
DCCB7, DCCB8	Cable_A1C1, Cable_C1C2 and Cable_A2C2	Range [d']

Table 8.2: *DCCB not operating requirement leads to thresholds setting range*

Thresholds setting range	In which relay the algorithm thresholds are determined
Range [a] and Range [a']	'#1' and '#8'
Range [b] and Range [b']	'#2' and '#3'
Range [c] and Range [c']	'#4' and '#5'
Range [d] and Range [d']	'#6' and '#7'

Table 8.3: *Thresholds determination for each relay*

For example, tests of faults on cable_A1C1 will give all the information of MAD.V and MAD.I on each relay position. Relays at '#1' and '#8' should detect the fault, while relays at

other places should not. Faults testings on cable_A1C1 should give one range [a] of thresholds for relays at '#1' and '#8' for allowing them sensible to the fault. On the other hand, relays at '#1' and '#8' should never detect the fault when faults are in cable_C1C2, cable_A2C2 and cable_A1A2. And this provides another range [a'] of thresholds for relays at '#1' and '#8' for keeping silent to these fault. Combing these two ranges [a] and [a'], the algorithm thresholds of relay at '#1' and '#8' can be determined.

Thus, by the same mechanism, the thresholds setting for the other six relays will be given. As a result, algorithm thresholds for relays may not necessarily the same. Because the fault transient on each cable differs with each other. For convenience, the test model in this thesis uses the same algorithm with the same parameters for each relay.

8.2 HVDC Transmission Line fault types and its probability:

The transmission lines are mainly overhead lines and underground cables. Due to their different material structure and installation position, the faults types and the fault probability are different. For overhead lines, pole to ground faults happen more often than pole to pole faults. Since overhead lines are exposed in the air, the possibility of faults are much higher than cable faults. Causes of the overhead lines can be human factor, installation mistake, and nature factors [44]. A typical example of a pole to ground fault caused by nature can be a falling tree knocking down one pole. A typical example of a pole to pole fault can be, a kite stuck in the transmission lines causes short circuit between poles.

Figure 8.2: *Ptp-faults and Single pole to ground faults caused by trees on overhead lines* [45][46]

Due to the insulation layer outside the conductors, the cable has a much lower probability of faults. And they usually hidden under the ground or on the seabeds. Human and nature contribute little to the fault factors. Pole to ground faults also happens more than the pole to pole faults on cables. Although cable faults rarely happen, they are usually permanent faults once happen. The possible fault can caused by, anchors snatching cables in the seabed or accelerated aging of insulation layer with seawater erosion [47]. The single pole to ground is

the most frequent faults for cables.

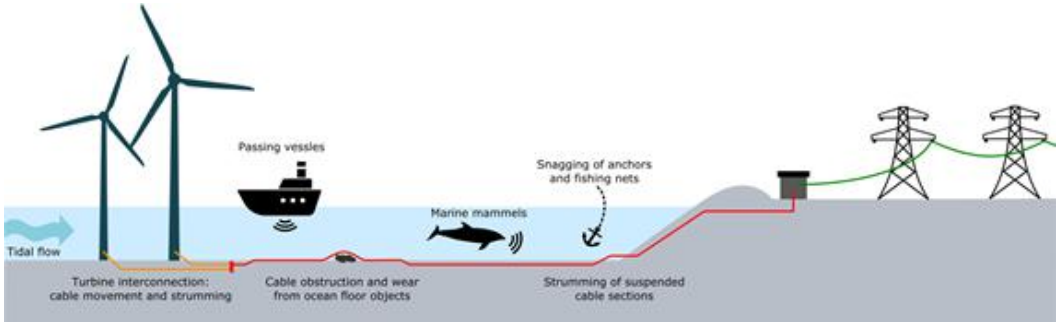


Figure 8.3: *Under sea cable faults for various reasons* [48]

Overall, the single pole to ground fault always happens more frequently than a pole to pole fault whatever it is a overhead line or underground cable. From the fault cases study in this thesis, it is found that modification of algorithm does not affect greatly on negative pole to ground faults. The detection range for nptg-faults is always under 20ohms. But for the possible nptg-faults in real life, the impedance can vary hugely. If that is caused by an anchors snatching, then the impedance can be very high. If that is caused by insulation layer completely broken at somewhere, then the fault acts like a bolted fault with very low impedance. As a result, approaches of increasing the detection range on single pole to ground cable faults should be given more attention in the future work.

Conclusion

In the past two decades from 2000, the rapid development of HVDC system benefits from the increases in the market share of renewable energy and revolution of the power converter technologies. However, there is not an globalized protection standard for HVDC system as it is in traditional AC grid. The protection strategy and protection still vary around the world. Because the fault current characteristic in HVDC transmission leads to different relay algorithms with various requirement. On the other hand, a valid relay algorithm need the to consider the current interruption ability of DCCBs. However, no natural zero-crossing of HVDC faults leads to difficulties in the design and development of DCCBs.

Fault testings are really important before the protection system is equipped in either AC or DC systems. By fault testings, the reliability of the algorithm is obtained and the potential risks are foreseen. During the fault testings, the testing platform and environment will affect the testing qualities such as accuracy of data acquisition, precision of fault detection, the fault detection range. This thesis focuses on fault testings on HVDC system with a novel 'MAD' algorithm proposed by Lian [15] in the platform 'RTDS'. The first purpose is to see how reliable the algorithm is in various cable faults detection. The second purpose is to see how fault types, fault impedance and fault locations will influence the transient fault current and fault detection. The third purpose is to investigate various protection strategies (protection selectivity) and compare their protection system performances during simulation.

The tested four terminal Meshed HVDC system are designed and built with 'RSCAD', which is an Electromagnetic Transient (EMT) simulation software of the RTDS real-time digital simulator. MATLAB is associated in the test procedure for help with controlling the simulation and figure plotting. A entire fault protection simulation contains the following

stages:

Stage 1: *Compile the HVDC system model (draft.file) in the 'RSCAD'*
Stage 2: *Set up communication between MALAB and Monitoring & Controlling interface (sib.file in RSCAD)*
Stage 3: *Download the HVDC system model to the 'RTDS' racks.*
Stage 4: *Initiate the tests and give commands (including switches and fault inception) in MATLAB to the testing system.*
Stage 5: *Figures are firstly saved in the sib.file and then exported into the MATLAB figure editor being re-plotted.*

Every time a new simulation will be tested, the whole procedure has to start from stage 1 after fault parameters are changed. The analysis on the tests results can come into the following three aspects:

Fault parameters' effect to the transient current and fault detection:
The fault impedance influence most on the transient current characteristic including the maximum fault current and the rate of fault current climbing. These impacts further impacts on the fault detection time for both relays on two ends of faulty cable.

The fault location determines the difference of injected fault current characteristics between two ends of faulty cable. This means the fault location indirectly affects the fault detection time both relays at faulty cable. The detection time difference becomes the largest when the fault is located biased to the end of the faulty cable.

The fault types also greatly affect the transient current. For a bipolar HVDC system, the single pole to ground fault causes less server consequences than the pole to pole fault for injecting much less fault current. On the other hand, it makes single pole to ground faults harder and later to detect.

Relay algorithm thresholds' effect to the fault detection performance:
The algorithm thresholds of MAD.I and MAD.I in this thesis directly determine whether the fault can be detected and whether the fault is detected in time. Decreasing the thresholds may make relays detect the faults with higher impedance when they should react to the fault. However, it also increases the risks of false detection when relays should not react to the fault.

On the other hand, increasing the thresholds will reduce the possibility of false detection on healthy cables. However, the detection sensitivity on cable fault will be decreased for not able to detect high impedance fault.

The determination of the algorithm thresholds is a trade-off between the protection sensitivity and reliability. It should be tested according the real fault distribution where the HVDC protection is applied. Thresholds settings may not necessarily the same for relays at different

cable according the real HDVC transmission line topology and fault distributions.

Comparison between different protection strategies in HVDC system:
According to Cigre Working Group B4/B5-59 [16], protection strategies in HVDC protection are divided into three types in terms of selectivity of protection areas. They are fully selective protection strategy (FSPS), partially selective protection strategy (PSPS) and non-selectivity protection strategy (NSPS) The prototype HVDC protection system is designed based on FSPS. After that, one of the feasible approaches of PSPS is proposed and tested. For NSPS, some of the possible protection methods are investigated but not simulated. The reasons is, this type of protection strategy is particularly dependent on the signal communication abilities.

FSPS needs more DCCBs than PSPS does. In FSPS, only the faulty cable will be isolated, which brings the least severe consequence to the other healthy parts. In PSPS, an area including the faulty cable and possibly more healthy cables are isolated, which brings severer consequence than FSPS. In FSPS, the relay algorithm should be more strictly calibrated, since DCCBs would be the only devices to interrupt the fault. While in PSPS, fault-clearing relies more on the cooperation of DCCBs, ACCBs. This means PSPS put forward higher requirements to ACCB operation mechanism. Whether to implement FSPS or PSPS is actually a trade-off of between financial expenditure of DCCBs and protection selectivity requirements.

To sum up, this thesis tests a novel relay algorithm performance in the HVDC system. The fault parameters' effects to the transient and fault detection are investigated. Besides, various HVDC protection strategies are studied and compared based on simulations on platform 'RTDS'. The HVDC protection requirements and standard is not determined in the industry yet, which makes HVDC protection system not mature currently. Meanwhile, the technique issue of DCCB manufacture hinders the development of HVDC protection. Relay algorithm should be carefully designed and tested before it is applied in real system.

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Appendix A

Publications

A.1 2019 IEEE PES ISGT ASIA

The testing part related to fault analysis on fully selective protection strategy is accepted with an title of "*DC Protection System Testing in RTDS-MATLAB Simulation Environment*" by **Innovative Smart Grid Technologies Asia Conference, 2019.** Although This paper is finally not presented at the conference.

DC Protection System Testing in RTDS-MATLAB Simulation Environment

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***Abstract*—The testing of protection scheme is significant before it can be commissioned in an actual substation. Nowadays, DC protection has not readily been designed and implemented in power systems. Therefore, due to high requirements on DC fault interruption, the designing and testing the corresponding DC protection with the use of a DC circuit breaker (DCCB) become a challenge. In this paper, a four-terminal meshed VSC-MMC HVDC system is developed in RTDS environment. Diverse fault tests, concerning different fault types, fault locations and fault impedances are conducted in a remote testing way. The MATLAB based testing controller by a remote computer will command the local computer and RTDS-modeled system through the communication network, in order to automatically run all test scenarios and do data processing. The related testing results demonstrate the DC fault dynamics in an effective way in order to test DC protection and DCCB in a modern laboratory.**

***Index Terms*—HVDC, DC protection, remote testing, RTDS, MATLAB.**

I. INTRODUCTION

In the past ten years, the rapid grow of the renewable energy and the revolution of large power converter greatly stimulates the investment and the construction of HVDC systems [1]. With the HVDC technology, large amount of electricity can be transmitted over long distance at low electrical loss. The voltage source converter (VSC) is becoming popular with its superior performance compared to the line communicated converter (LCC) [1]. Predictably, VSC-HVDC systems will probably replace the thyristor-based systems [2]. For a HVDC grid, the meshed loop topology improves the entire reliability with more redundancies.

As it is known, the protection system has been well investigated and developed in AC power system. However, the corresponding protection technology for HVDC system has not been well investigated at that so far [3]. In order to ensure the required quality of HVDC protection, it is necessary to do comprehensive fault testing before the commissioning.

Remote testing becomes one of the most effective and flexible methods that complemented in fault case simulations and relay testing [4]. The real time digital simulator (RTDS) provides a platform, which can precisely simulate electromagnetic transient performances of a power system and related fault scenarios in real time [5]. The electrical circuit diagrams and the dynamic parameters can be edited and complied in the corresponding software RSCAD with a local/remote PC terminal. MATLAB can be used as a supervisory controller, which conducts all the testing commands and the resulting analysis.

This article firstly presents the studied HVDC system schematic where each component is well introduced. Then, the associated protection system will be described, including the key operation equipment with a protection algorithm. Thereafter, the methodology of remote testing based on the RTDS-MATLAB Simulation platform will be introduced. This section contains three sub parts, RTDS based modelling and simulation, RTDS-MATLAB simulation environment and protection testing objectives. The main case study and related comparisons will be given in Section IV. Finally, a short conclusion will be drawn in the end.

II. A MESHED HVDC GRID BASED TEST SYSTEM

The test system is a four-terminal HVDC meshed system, where each bus connects a local generator or load through a modular multilevel converter (MMC).

A. HVDC system and DCCB

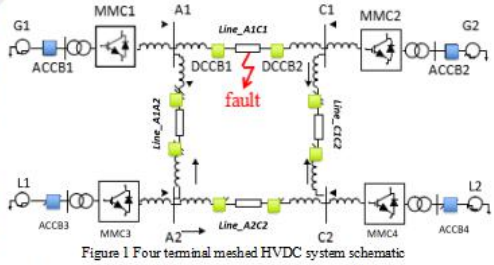


Figure 1 Four terminal meshed HVDC system schematic

MMC is composed by half-bridge modules [6]. Transformers at the AC side are applied to adjust the local AC grid voltage level to a unified secondary voltage, i.e., 220kV. This AC current is transformed to ±200kV DC current through MMCs [7]. As Figure 1 shows, the four terminals are named as A1, A2, C1 and C2. In this meshed DC system, each branch has two direct current circuit breakers (DCCB) placed on each end. All the

branches (A1C1, A1A2, A2C2, C1C2) are considered to be cables with a length of 200 km [8].

In the test system, a mechanical type DCCB model with a reversal current injection has been applied. The diagram of the system level model is shown in Figure 2 [9].

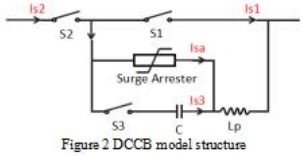


Figure 2 DCCB model structure

This model consists of three branches. The first branch is the main circuit breaker branch; I_{s1} is the current flowing through the high speed vacuum interrupter S1. The second branch is the branch that is used for energy dissipation; I_{sa} is the surge arrester branch current. The last branch is a resonant circuit, also called current injection circuit. The aim of this branch is to generate an oscillating current with a sufficient magnitude so that multiple current zeros will be created. The operation delay of this mechanical DCCB is around 8ms.

B. *A DC protection system for the meshed HVDC system*

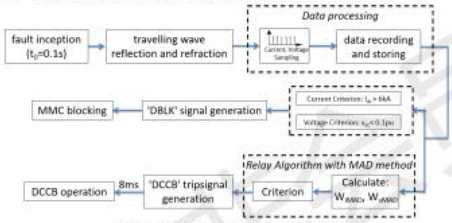


Figure 3 Schematic of DC fault protection

The description of the DC protection system for the four terminal meshed HVDC system is shown in Figure 3. The fault occurs at t_0=0.1s and travelling waves are created. Thereafter, the travelling waves reach each bus at which reflected and refracted waves occur. During this period, the current and voltage variables are sampled and processed continuously [10].

The next is the fault detection step. For the converter, the fault detection is to give a threshold to the direct electric variables, currents and voltages. A current of 6kA and a voltage of 0.1pu are the typical values for the threshold in order to identify faulty operation conditions. For the DCCB operation, the algorithm based on the method of median absolute deviation (MAD) and its modification is applied [11].

The 'fault interruption' mechanisms in the protection system consist of MMC's blocking and DCCB's operation. Once the faulty incident surge is detected, 'DBLK' signal will be generated and sent to MMCs to block the converter. As for DCCBs, 'DCCB' trip-signal will be generated after the fault is detected. Finally, DCCBs is supposed to operate and disconnect the faulty line.

It should be noted that the 'MMC blocking' module shown in Figure 3 is to cooperate with the converter protection to keep the security of converters, whilst the 'DCCB operation' flow is for DC grid protection or component protection, e.g. line protection, busbar protection [12].

III. REMOTE TESTING BASED ON RTDS-MATLAB SIMULATION ENVIRONMENT

The idea of remote testing is firstly proposed by Apostolov, USA [4]. Instead of a crew moving far away to implement hardwired protection and control systems, IEC 61850 based communication interfaces allow people to do the testing remotely and efficiently. The test method and tools determine whether tests are implemented in a reliable and secure way. Besides, testing quality should be ensured by an effective simulation of a real situation [4]. For example, a transmission line short-circuit-fault caused by a branch or a kite string.

A. *RTDS based modelling and simulating*

RTDS testing has two main advantages compared to other simulation software that can be used for testing. One is its real-time simulation property. One rack is capable to store 6 parallel processor cards(PB5). During the simulation, the powerful ability of data acquisition and calculation allows not only continuous but also timely output. Thus, a real-time feedback between controllers and controlled objects would significantly improve the testing reliability drastically.

Another advantage of RTDS is its ability to perform hardware-in-the-loop (HiL) test. HiL testing is usually applied in aerospace, automotive manufacturing and power systems. By applying HiL method the functionality of a physical protection device in an emulated virtual DC network instead can be tested. In this testing experiment, the DCCB model is modeled as a in RSCAD software model instead of using an actual DCCB. The major benefit of doing so is the reduction of financial costs compared to the costs of testing in an actual object [5].

B. *RTDS--MATLAB simulation environment*

Figure 4 shows a configuration of the real time cyber-physical simulation platform to realize the remote testing strategy. The test HVDC system (in Figure 1) is firstly built in RSCAD software in the remote/local computer.

In the RSCAD interface, not only control commands including the fault generation signals are given, but also the power flow and system operation are observed. An entire fault case simulation and protection testing may require frequent manual revisions in RSCAD. However, by using MATLAB, complex commands can be integrated into a m-file, in which they can be executed more efficiently. In addition, it is convenient to exchange data between RSCAD and MATLAB via JTCP interface. This JTCP file uses MATLAB's Java interface to handle Transmission Control Protocol (TCP) communications with another application, either on the same computer or a remote one. Four racks of RTDS, which include 16 PB5 processor cards, are used to provide Type-5 models [8] of HB MMC converters, mechanical DCCBs in small time step and the proposed protection algorithm.

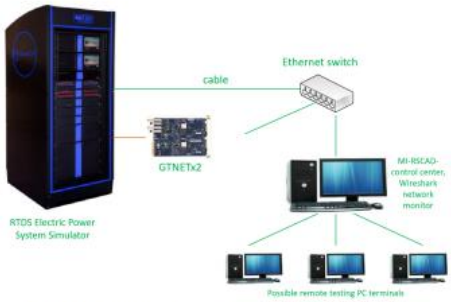


Figure 4 Real time simulation platform with remote testing interface

C. *Protection testing objectives*

In any power systems, either AC grids or DC power system secure operations would not be maintained without suitable protection systems. An effective protection system is to ensure correct disconnection of the faulty items in order to timely and significantly minimize the consequences that may result from the fault occurrence. The objective of the protection testing is to determine whether the performance of an IED can meet the industry requirements.

Therefore, the research performed here firstly considers the sensitivity of the protection system on the test HVDC system model by multiple fault case simulations. Some test cases will be conducted to demonstrate the effectiveness of the proposed test environment.

IV. CASE STUDY

Based on the RTDS-MATLAB simulation platform and the related remote testing method, the protection testing in this paper is arranged as:

Case 1 Base case

A bolted pole–to-pole(PTP) fault applies at bus C1.

Case 2 Negative pole-to-ground fault

A bolted negative-pole-to-ground fault (NPTG) applies at bus C1.

Case comparison

The pole–to-pole(PTP) fault comparison are applied with 0 ohm and 25 ohm fault impedance, located in 5 different places along line A1C1.

A. *Case 1(base case)*

Table 1 Critical settings and parameters of test HVDC mesh system

Converter blocking	With
Fault inception instant	t = 0.1s
Fault type	**Pole to pole**
Fault locations	**Close to bus C1**
Fault Impedance	**R_f = 0.0101 ohm**
DCCB placement	At each end of DC lines
DCCB mechanical delay	8ms

In the base case, the converter is limited by the maximum valve current, 6kA and the minimum primary AC voltage, 22kV (0.1pu). The converter blocking is triggered when both of those two conditions are met. A pole-to-pole type occurs close to bus C1 at t_0=0.1s with a fault impedance set close to zero (0.0101ohm). The DCCBs are located at each end of the line with a mechanical operation delay of 8ms. The simulation results of the selected critical variables can be seen in Figure 5 and Figure 6.

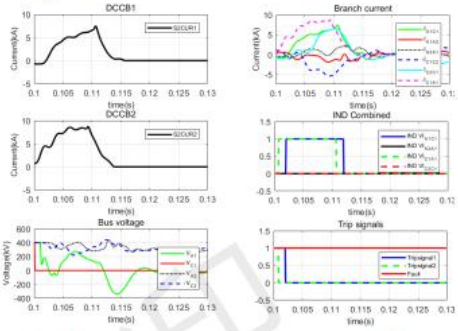


Figure 5 DCCB currents, system voltages, branch currents and the trip signal.

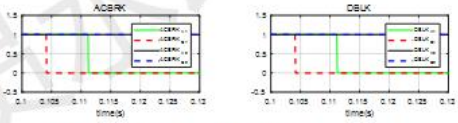


Figure 6 Plots of AC breaker signals and MMC converter Blocking signal.

DCCB1 and DCCB2 refer to the circuit breakers close to bus A1 and bus C1 respectively. When the fault occurs, a large DC short circuit current is generated. After detecting the fault current, both DCCBs operate in approximately 8ms, which is the operating delay of the mechanical DCCB model proposed in [13].

From subplot 'DCCB1' and 'DCCB2' in Figure 5, we can see DCCB2 trips at t=0.1090s, while DCCB1 trips at t=0.1105s. The fact that DCCB2 is about 1.5ms faster than the DCCB1 indicates that the fault is located much closer to the C1 side. From the branch current subplot, the magnitudes of I_{A1C1}, I_{C1A1}, I_{C1C2} and I_{C2C1} experience a larger positive increment than those of other branch currents. Because the fault event takes place on C1 side of branch A1C1, short circuit current will be directly injected from neighboring generators to the fault location through converters..

Yet in Figure 6, from the plot of 'IND Combined', only the two signal 'IND VI_{A1C1}' and 'IND VI_{C1A1}' are enabled for a period of time. This means that only DCCB1 and DCCB2 which in the fault line, will receive the trip signal processed by the relay algorithm. The other DCCBs located in line A1A2 and C1C2 should not receive the trip signal. Therefore, the fault area detection is successful. The small time difference

between two trip signals in plot 'Trip signals' may indicate which end of line A1C1 the fault is closer to, and how far it is.

In the left hand side of Figure 6, 'ACBRK' denotes an alternating current circuit breaker(ACCB) signal. In this test system, the current limit is given a value of 6kA. When a DC current is within the limit, ACBRK signal holds a high-level '1' signal. Once it is over the limit, ACBRK signal drops to low-level '0' signal, which means a trip signal is sent to the ACCB nearby. In the right hand side, DBLK graph shows the blocking signal for each MMC converter. Initially, each converter is in the de-blocked state, which is represented by the high-level '1' signal. When it comes to low-level '0' signal, IGBTs in the corresponding MMC converter are blocked. In order to generate this blocking signal, one of the conditions that should be fulfilled is that, ACBRK signal appears 0. Another one is that, the primary AC side voltage is lower than 0.1pu. Only when both of them are met at the same time, converter blocking signal can be initiated. In the base case, C1 converter is blocked at about 0.1042s and A1 converter is blocked at about 0.1112s.

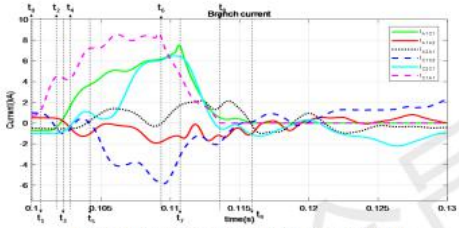
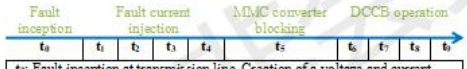


Figure 7 Process events in order of the time line since 0.1s



t_0: Fault inception at transmission line. Creation of a voltage and current wave travelling towards the terminals A1, C1 and C2.
t_1: The travelling waves first reach the terminal C1. The capacitors of the converter at related terminal start to discharge.
t_2:The travelling waves reach the terminal A1. Short circuit current starts to flow from A1 to the fault. From this point on, the current seen from C1 to A1 experiences a slight decline until t4.
t_3:The travelling waves reach the terminal C2 and reflects to C1. Short current starts to flow from C2 to the fault.
t_4:The travelling waves reach the terminal A2. Short current starts to flow from A2 to the fault. And from this point on, current IC1A1 from C1 to A1 rises again.
t_5:IGBTs of converter C1 are blocked for its own protection.
t_6: DCCB2 located at C1 opens to interrupt the fault current increment.
t_7: DCCB1 located at A1 opens to interrupt the fault current increment.
t_8: DCCB2 is fully opened.
t_9: DCCB1 is fully opened.

Figure 7 shows the event sequence according to current waveforms from 0.1s to 0.13s. The fault is introduced at t_0, and the surge propagates in both directions from the fault location to A1 and to C1. From t_1 to t_4, the travelling waves passed through 4 buses in order of C1, A1, C2, A2. When it comes to the point t_5, IGBTs of converter C1 are blocked by its own protection. Fault current is now contributed by the AC side through the converter's anti-parallel diodes. At t_6 and t_7, the mechanical DCCB2 located at C1, and the mechanical DCCB1 located at A1 open in order to interrupt the fault current respectively. Due to the matter of fault position, DCCB2 is the first to be fully interrupted at t_8. Thereafter, DCCB1 is fully opened, which means the fault is isolated completely and the system starts to recover with the other three healthy branches.

B. *Case 2(negative pole to ground fault)*

Table 2 Critical settings and parameters of test HVDC mesh system

Converter blocking	With
Fault inception instant	t = 0.1s
Fault type	**Negative pole to ground**
Fault locations	**Close to bus C1**
Fault Impedance	**R_f = 0.0101 ohm**
DCCB placement	At each end of DC lines
DCCB mechanical delay	8ms

In case 2, a negative pole-to-ground type fault is analyzed. The other settings and parameters are kept the same as case 1. The related simulation results can be seen in Figure 9 and Figure 10:

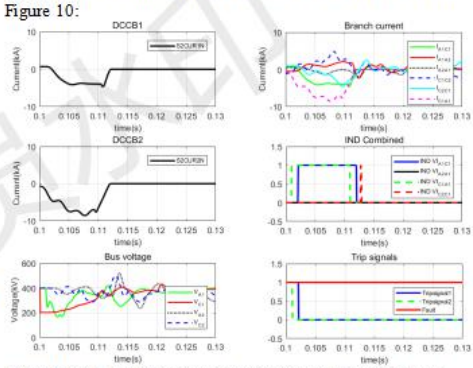


Figure 8 DCCBs currents, system voltages, branch currents and trip signals.

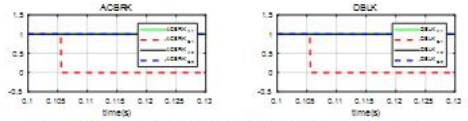


Figure 9 AC breaker's signals and MMC converter Blocking signal.

In case 2, the DCCB currents and the branch currents are all with negative polarity because the negative pole-to-ground fault current reverses its direction. DCCB1 and DCCB2 operate around t=0.1105s t=0.1094s respectively. For a bolted fault case located near bus C1, the local DCCB2 trips 0.4ms faster than the pole-to-pole fault.

Due to single pole–to-ground fault, the voltage V_{C1} at fault place drops to a half the normal voltage instead of a zero value at the fault inception point. The other three bus voltages also experience a much smaller oscillation in the pre-interruption

stage. The current flowing through DCCB1 is reduced a lot compared to that in case 1. It almost stops increasing at t=0.105s. This could be the reason why the MMC converter at A1 does not block the fault current. While, the MMC converter at C1 is still blocked at around t=0.1055s, which is 1.3ms later than that in the pole-to-pole fault case(case 1). Overall, the pole-to-ground fault may have a less severe consequence to the power system than the pole–to-pole fault does and for these cases the protection algorithms works successfully for fault located at C1.

C. *Cases comparison and analysis*

Pole to Pole fault (PTP fault)

The system is also tested with PTP faults at different locations on branch A1C1. The simulation data are collected in Table 3. The fault impedance of 0.0101ohm is used and the monitored variables are the fault clearing time, V_{C1}, I_{A1C1}, I_{C1A1} and t_{IND}. The fault clearing time ($t_{cur\ off}$) is the interruption instant of DCCBs, and the related values of V_{C1}, I_{A1C1}, I_{C1A1} are all measured at $t_{cur\ off}$ of the corresponding DCCB.

Variable t_{IND} shows the time when the trip signals are produced and Variable $t_{block\_}$ is the MMC converter blocking time.

Table 3 Data collection for pole-to-pole fault case comparison(0.0101ohm)

location	0km (A1)	50km	100km	150km	200km (C1)
Case no.	C.1	C.2	C.3	C.4	C.5
$t_{cur\ off}$(s)	0.1093	0.1096	0.1098	0.1102	0.1104
$t_{cur\ off2}$(s)	0.1103	0.11	0.1097	0.1094	0.1091
V_{C1}(kV)	76.72	108	52.28	51.95	0.1686
V_{A1}(kV)	0.1044	-6.917	146	99.04	169.3
I_{A1C1}(kA)	5.745	8.554	8.48	7.452	6.054
I_{C1A1}(kA)	6.801	7.236	7.355	7.995	8.292
t_{IND_VA1C1}(s)	0.1009	0.1012	0.1014	0.1018	0.102
t_{IND_VC1A1}(s)	0.1019	0.1016	0.1013	0.101	0.1007
t_{block_A1}	0.1055	0.1076	0.1097	0.1105	0.1112
t_{block_C1}	0.1052	0.1048	0.1045	0.1044	0.1042

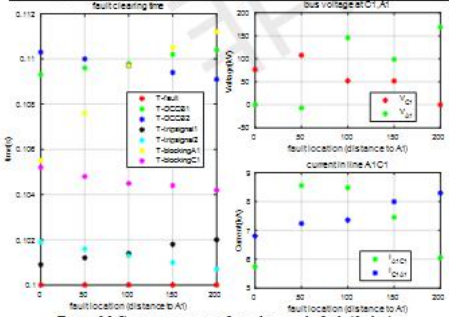


Figure 10 Case comparisons for pole-to-pole fault (0 ohm).

Figure 10 shows all the simulation results in case of a pole–to-pole fault. In the graph 'fault clearing time', as the fault location moves from A1 to C1, the time of the tripsignal2 and DCCB2 trip time moves forward, whilst the time of trip-signal1 and DCCB1 trip time move backward. When the fault is just in the middle of the line A1C1 (100km distance to A1), the time of trip-signal1 and the time of trip-signal2 are almost overlapped. This also happens for the DCCBs' operation time. This implies that in line A1C1, the DCCB at one side would trip faster as the fault is closer to the same side, whilst for the DCCB at the other side, it is the other way around.

When only one of DCCBs and its trip signal are considered, for example, DCCB2, it can be seen that the time interval between the T-DCCB2 and T-tripsignal2 is always a constant resulting in 8.4ms. This can be checked in Table 1. This 8.4ms delay is the mechanical DCCB operation time, which is already mentioned before.

In all cases with different fault locations, the fault can be detected(trip-signals are generated and sent) within 2ms after the fault inception for each DCCB. As the fault takes place at bus C1, it will take no more than a 1ms to detect the fault by the relay at A1 side. Considering the mechanical operation delay, the maximum DCCB operation time is 10.4ms from DCCB1 and the minimum DCCB operation time is 9.1ms from DCCB2. In addition, both operation times are valid when the fault is located at C1. As a result, for bolted faults, the DCCB trip time is in the range of 9.1ms and 10.4ms after the fault occurrence.

When moving the fault from A1 to C1, the value of T-blockingC1 keeps decreasing in a tiny rate. While, that of T-blockingA1 keeps increasing in a relatively larger rate. This means that the I_{A1C1} increases with a lower gradient, but I_{C1A1} increases with a higher gradient. In other words, fault location does affect the current component from bus A1, but does not affect much the current component from bus C1.

When the fault is in A1, DCCB1 operates faster than DCCB2. When DCCB2 operates, DCCB1 has already operated and the current I_{A1C1} declines. That is why in case 2.5.1(fault in A1), current I_{A1C1} is lower than I_{C1A1}. As the location is a bit farther from A1 (25% to A1), the interruption time difference between DCCB1 and DCCB2 is not that large. As the fault is closer to A1, the increasing rate of I_{A1C1} is larger than that of I_{C1A1}. Thus in case 2.5.2 (fault is 25% distance to A1), I_{A1C1} is larger than I_{C1A1}. As the fault location moves to the middle point, I_{A1C1} is still evidently larger than I_{C1A1}. The reason for this that is the converter at C1 is blocked before both DCCBs operate, whilst the converter at A1 is not blocked before DCCBs operate. Hence, the increasing fault current I_{C1A1} is then restricted. As the fault location moves from the middle point toward bus C1, I_{C1A1} becomes larger than I_{A1C1} and DCCB2 trips faster than DCCB1. As DCCB2 trips, I_{A1C1} is still at the rising part and the current magnitude difference becomes the largest when the fault is located at C1.

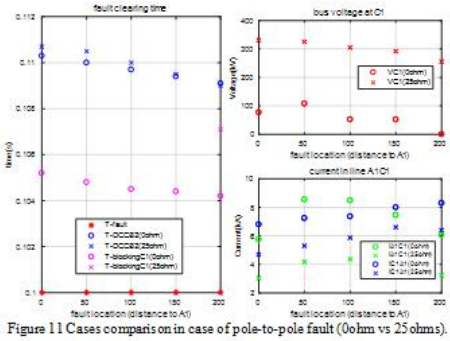


Figure 11 Cases comparison in case of pole-to-pole fault (0ohm vs 25 ohms).

By comparing cases with 0 ohm impedance and cases with 25 ohm impedance, it can be seen that the fault clearing time is not much influenced by the fault impedance. However, the blocking function of the converter at C1 almost fails to operate when the fault impedance is 25 ohm. The reason is that the decrement of bus voltage V_{C1} is less due to a higher fault impedance. In cases of a 0 ohm fault impedance, V_{C1}s voltages are almost below 100kV, however, in case of 25ohm fault impedance, V_{C1}s are around 300kV. In addition, the increments of the fault currents are reduced a lot either I_{A1C1} or I_{C1A1}. These two factors make converters being not sensitive to block the fault current. From the graph 'current-fault location', the magnitude of I_{C1A1}'s reduction trend is lower than the magnitude of I_{A1C1}'s reduction especially when the fault is located at the middle point. This means that the fault impedance affects much more I_{A1C1} current than the I_{C1A1} current.

The practical laboratory environment and how the remote testing is done can be seen in Figure 12.

Figure 12 Remote testing environment of RTDS-MATLAB simulation.

CONCLUSION

As more HVDC systems will be constructed in the ner future, the developing and testing of DC protection scheme performance will be an important subject. The fast fault dynamics in the HVDC systems, the selectivitiy of the protection and the fault interruption of the DC currents should be inevitably considered. In this paper, a remote testing of DC protection against DC faults in a given four terminal meshed VSC-HVDC system has been conducted, based on RTDS-MATLAB simulation environment. The presented methodology supported by a generic fault detection algorithm successfully demonstrate typical DC fault scenarios, and show the effectiveness of DC protection remote testing in a modern laboratory environment.

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Appendix B

MATLAB codes & Relay Algorithm in Cbuilder

Matlab Codes:

```
clear all
close all
clc
portnum = 4575;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%   Main Program
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
disp('**********************************************************************
***********')
disp('*     Import Plot Signals using RSCADs ListenOnPort Feature')
disp('**********************************************************************
***********')

%   Runtime is acting as TCP socket server
JTCPOBJ = jtcp('REQUEST','127.0.0.1', portnum);
disp('*     Connection to TCP Server Established!');
```

```
jtcp('writes',JTCPOBJ,'Start;');


delay(25); % Delay until simulation starts
t=cputime;

% %   Populate plot signal Iag by applying a fault
jtcp('writes',JTCPOBJ,'PushButton "Subsystem #4 : CTLs : Inputs :
CLOSEALL2";');
jtcp('writes',JTCPOBJ,'SUSPEND 0.3;');
jtcp('writes',JTCPOBJ,'ReleaseButton "Subsystem #4 : CTLs : Inputs :
CLOSEALL2";');
jtcp('writes',JTCPOBJ,'SUSPEND 1;');
jtcp('writes',JTCPOBJ,'PushButton "Subsystem #4 : CTLs : Inputs :
CLOSEALL";');
jtcp('writes',JTCPOBJ,'SUSPEND 0.3;');
jtcp('writes',JTCPOBJ,'ReleaseButton "Subsystem #4 : CTLs : Inputs :
CLOSEALL";');
jtcp('writes',JTCPOBJ,'SUSPEND 1;');
jtcp('writes',JTCPOBJ,'PushButton "Subsystem #4 : CTLs : Inputs :
ONcharge";');
jtcp('writes',JTCPOBJ,'SUSPEND 0.3;');
jtcp('writes',JTCPOBJ,'ReleaseButton "Subsystem #4 : CTLs : Inputs :
ONcharge";');
jtcp('writes',JTCPOBJ,'SUSPEND 15;');
jtcp('writes',JTCPOBJ,'PushButton "Subsystem #1 : CTLs : Inputs :
DCFAULT";');
jtcp('writes',JTCPOBJ,'SUSPEND 0.3;');
jtcp('writes',JTCPOBJ,'ReleaseButton "Subsystem #1 : CTLs : Inputs :
DCFAULT";');
jtcp('writes',JTCPOBJ,'SUSPEND 10;');

delay(30); % Delay until simulation finalizes

% % comments by hongfeizhu
% % Saving the plot from RSCAD to the folder
disp('*    Saving plot...');
jtcp('writes',JTCPOBJ,'SavePlot "DCCB1currents","E:\Master
project\Lab data\example\DCCB1.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "DCCB2currents","E:\Master
project\Lab data\example\DCCB2.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "DCtranscurrents","E:\Master
project\Lab data\example\DC branch current.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "DCvoltages","E:\Master project\Lab
```

```
data\example\Bus voltage.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "CurrentINDs","E:\Master project\Lab
data\example\CurrentINDs.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "VoltageINDs","E:\Master project\Lab
data\example\VoltageINDs.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "CombinedINDs","E:\Master project\Lab
data\example\CombinedINDs.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "Trips","E:\Master project\Lab
data\example\Trips.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "ACBRK","E:\Master project\Lab
data\example\ACBRK.mpb";');
jtcp('writes',JTCPOBJ,'SavePlot "DBLK","E:\Master project\Lab
data\example\DBLK.mpb";');

% % Modify the raw data so that Matlab can recognize it.
delay(30);   %   Delay until .out file is generate
disp('*    Importing data from .out file...');
[plotdata1,delimiterOut,headerlinesOut] = importdata('DCCB1.out');
[plotdata2,delimiterOut,headerlinesOut] = importdata('DCCB2.out');
[plotdata3,delimiterOut,headerlinesOut] = importdata('Bus
voltage.out');
[plotdata4,delimiterOut,headerlinesOut] = importdata('DC branch
current.out');
[plotdata5,delimiterOut,headerlinesOut] =
importdata('VoltageINDs.out');
[plotdata6,delimiterOut,headerlinesOut] =
importdata('CurrentINDs.out');
[plotdata7,delimiterOut,headerlinesOut] =
importdata('CombinedINDs.out');
[plotdata8,delimiterOut,headerlinesOut] = importdata('Trips.out');
[plotdata9,delimiterOut,headerlinesOut] = importdata('ACBRK.out');
[plotdata10,delimiterOut,headerlinesOut] = importdata('DBLK.out');




% Set figure1's geometry and position
figure(1);
set(gcf,'unit','centimeters','position',[10,1,20,20]);

% % DCCB1&2 current plot
subplot(4,2,1);
plot(plotdata1.data(:,1),plotdata1.data(:,2),'g',plotdata1.data(:,1),
```

```
plotdata1.data(:,3),'r',plotdata1.data(:,1),plotdata1.data(:,4),'k:',
plotdata1.data(:,1),plotdata1.data(:,5),'b--','linewidth',2);
axis([0.1,0.13,-5,10]);
title('DCCB1');
legend({'IArres1','S1CRT1','S2CUR1','IS3A21'},'Fontsize',7,'Location
','northeast');
xlabel('time(s)');
ylabel('Current(kA)','Fontsize',10);
grid on;
set(subplot(4,2,1),'position',[0.075,0.815,0.375,0.16]);
subplot(4,2,3);
plot(plotdata2.data(:,1),plotdata2.data(:,2),'g',plotdata2.data(:,1),
plotdata2.data(:,3),'r',plotdata2.data(:,1),plotdata2.data(:,4),'k:',
plotdata2.data(:,1),plotdata2.data(:,5),'b--','linewidth',2);
axis([0.1,0.13,-5,10]);
title('DCCB2');
legend({'IArres2','S1CRT2','S2CUR2','IS3A2'},'Fontsize',7);
xlabel('time(s)');
ylabel('Current(kA)','Fontsize',10);
grid on;
set(subplot(4,2,3),'position',[0.075,0.57,0.375,0.16]);

% % DC system voltages and currents plot
subplot(4,2,5);
plot(plotdata3.data(:,1),plotdata3.data(:,3),'g',plotdata3.data(:,1),
plotdata3.data(:,5),'r',plotdata3.data(:,1),plotdata3.data(:,2),'k:',
plotdata3.data(:,1),plotdata3.data(:,4),'b--','linewidth',1.5);
axis([0.1,0.13,-400,600]);
title('Bus voltage');
legend({'V_A_1','V_C_1','V_A_2','V_C_2'},'Fontsize',7,'Location','So
uthEast');
xlabel('time(s)');
ylabel('Voltage(kV)','Fontsize',10);
grid on;
set(subplot(4,2,5),'position',[0.075,0.32,0.375,0.16]);
subplot(4,2,7);
plot(plotdata4.data(:,1),plotdata4.data(:,2),'g',plotdata4.data(:,1),
plotdata4.data(:,3),'r',plotdata4.data(:,1),plotdata4.data(:,4),'k:',
plotdata4.data(:,1),plotdata4.data(:,5),'b--',plotdata4.data(:,1),pl
otdata4.data(:,6),'c',plotdata4.data(:,1),plotdata4.data(:,7),'m--',
'linewidth',1.5);
axis([0.1,0.13,-7.5,10]);
title('Branch current');
legend({'I_A_1_C_1','I_A_1_A_2','I_A_2_A_1','I_C_1_C_2','I_C_2_C_1',
```

```
'I_C_1_A_1'},'Fontsize',7);
xlabel('time(s)');
ylabel('Current(kA)','Fontsize',10);
grid on;
set(subplot(4,2,7),'position',[0.075,0.07,0.375,0.16]);

% % Indices plot
subplot(4,2,2);
plot(plotdata5.data(:,1),plotdata5.data(:,4),'b',plotdata5.data(:,1),
plotdata5.data(:,2),'k',plotdata5.data(:,1),plotdata5.data(:,5),'g--
',plotdata5.data(:,1),plotdata5.data(:,3),'r--','linewidth',2);
axis([0.1,0.13,-0.5,1.5]);
title('IND Voltage');
legend({'IND V_A_1','IND V_A_2','IND V_C_1','IND V_C_2'},'Fontsize',7);
xlabel('time(s)');
grid on;
set(subplot(4,2,2),'position',[0.6,0.815,0.375,0.16]);
subplot(4,2,4);
plot(plotdata6.data(:,1),plotdata6.data(:,2),'b',plotdata6.data(:,1),
plotdata6.data(:,3),'k',plotdata6.data(:,1),plotdata6.data(:,4),'g--
',plotdata6.data(:,1),plotdata6.data(:,5),'r--','linewidth',2);
axis([0.1,0.13,-0.5,1.5]);
title('IND Current');
legend({'IND I_A_1_C_1','IND I_A_2_A_1','IND I_C_1_A_1','IND
I_C_2_C_1'},'Fontsize',7);
xlabel('time(s)');
grid on;
set(subplot(4,2,4),'position',[0.6,0.57,0.375,0.16]);
subplot(4,2,6);
plot(plotdata7.data(:,1),plotdata7.data(:,2),'b',plotdata7.data(:,1),
plotdata7.data(:,3),'k',plotdata7.data(:,1),plotdata7.data(:,5),'g--
',plotdata7.data(:,1),plotdata7.data(:,4),'r--','linewidth',2);
axis([0.1,0.13,-0.5,1.5]);
title('IND Combined');
legend({'IND VI_A_1_C_1','IND VI_A_2_A_1','IND VI_C_1_A_1','IND
VI_C_2_C_1'},'Fontsize',7);
xlabel('time(s)');
grid on;
set(subplot(4,2,6),'position',[0.6,0.32,0.375,0.16]);
subplot(4,2,8);
plot(plotdata8.data(:,1),plotdata8.data(:,3),'b',plotdata8.data(:,1),
plotdata8.data(:,2),'g--',plotdata8.data(:,1),plotdata8.data(:,4),'r
','linewidth',2);
axis([0.1,0.13,-0.5,1.5]);
```

```
title('Trip signals');
legend({'Tripsignal1','Tripsignal2','Fault'},'Fontsize',7,'Location',
'East');
xlabel('time(s)');
grid on;
set(subplot(4,2,8),'position',[0.6,0.07,0.375,0.16]);

% Set figure2's geometry and position
figure(2);
set(gcf,'unit','centimeters','position',[10,10,20,5]);

% % ACBRK signal plot
subplot(1,2,1);
plot(plotdata9.data(:,1),plotdata9.data(:,2),'g',plotdata9.data(:,1),
plotdata9.data(:,3),'r--',plotdata9.data(:,1),plotdata9.data(:,4),'k
',plotdata9.data(:,1),plotdata9.data(:,5),'b--','linewidth',2);
axis([0.1,0.13,-0.5,1.5]);
title('ACBRK');
legend({'ACBRK_A_1','ACBRK_C_1','ACBRK_A_2','ACBRK_C_2'},'Fontsize',
7,'Location','northeast');
xlabel('time(s)');
grid on;
set(subplot(1,2,1),'position',[0.075,0.25,0.375,0.65]);

% % DBLK signal plot
subplot(1,2,2);
plot(plotdata10.data(:,1),plotdata10.data(:,2),'g',plotdata10.data(:,
1),plotdata10.data(:,3),'r--',plotdata10.data(:,1),plotdata10.data(:,
4),'k',plotdata10.data(:,1),plotdata10.data(:,5),'b--','linewidth',2)
;
axis([0.1,0.13,-0.5,1.5]);
title('DBLK');
legend({'DBLK_A_1','DBLK_C_1','DBLK_A_2','DBLK_C_2'},'Fontsize',7,'L
ocation','northeast');
xlabel('time(s)');
grid on;
set(subplot(1,2,2),'position',[0.6,0.25,0.375,0.65]);
```

Relay Algorithm in Cbuilder:

Current detection

VERSION:
3.001

```
// Include file below is generated by C-Builder
// and contains the variables declared as -
// PARAMETERS, INPUTS, OUTPUTS . . .
#include "MAD_C.h"


STATIC:

// ------------------------------------------------
// Variables declared here may be used in both the
// RAM: and CODE: sections below.
// ------------------------------------------------
//        double dt;

int IVD1_1;
int IVD1_2;
int IVD1_3;
int K;
double signal_array[50];
double signal_array_temp[52];
double temp1;
double lefttemp;
int var1;
double temp;
int i;
int j;
int ii;
double LastD;
double LastD_2;


double temp2[50];
double temp3;
double temp4;
double temp5;
double temp5_2;
```

```
//-End of STATIC: Section-

RAM_PASS1:

var1=RSN+1;

RAM_FUNCTIONS:

// ------------------------------------------------
// This section should contain any 'c' functions
// to be called from the RAM section (either
// RAM_PASS1 or RAM_PASS2). Example:
//
// static double myFunction(double v1, double v2)
// {
//         return(v1*v2);
// }
// ------------------------------------------------


RAM:

// ------------------------------------------------
// Place C code here which computes constants
// required for the CODE: section below.    The C
// code here is executed once, prior to the start
// of the simulation case.
// ------------------------------------------------
//        dt= getTimeStep();

//signal_array=malloc(sizeof(float)* var1) ;


for (i=0;i<50;i++)
     {signal_array[i]=0;}

//IVD1_1=malloc(sizeof(int)*1);
IVD1_1 = 0;

//IVD1_2=malloc(sizeof(int)*1);
IVD1_2 = 0;

//IVD1_3=malloc(sizeof(int)*1);
IVD1_3 = 0;
```

```
// ------------- End of RAM: Section -------------

CODE:

// ------------------------------------------------
// Place C code here which runs on the RTDS. The
// code below is entered once each simulation
// step.
// ------------------------------------------------



//allocateMemory(signal_array,var1);
//allocateMemory(signal_array_temp,var1) ;

//allocateMemory(IVD1_1,1);
//allocateMemory(IVD1_2,1);
//allocateMemory(IVD1_3,1);

LastD = signal_array_temp[50];
LastD_2 = signal_array_temp[51];

double median(int n, double x[]) {

	for(i=0; i<n-1; i++) {
		for(j=i+1; j<n; j++) {
			if(x[j] < x[i]) {
				temp = x[i];
				x[i] = x[j];
				x[j] = temp;
			}
		}
	}

	if(n%2==0) {
		return((x[n/2] + x[n/2 - 1]) / 2.0);
	} else {
		return x[n/2];
	}
}
```

```
double leftmedian(int n, int n1, double x[]) {
	if((n1+1)%2==0) {
		return((x[(n1+1)/2] + x[(n1+1)/2 - 1]) / 2.0);
	} else {
		return x[(n1+1)/2];
	}
}

double rightmedian(int n, int n1, double x[]) {
	if((n-n1)%2==0) {
		return((x[(n+n1)/2] + x[(n+n1)/2 - 1]) / 2.0);
	} else {
		return x[(n+n1-1)/2];
	}
}




//if (IVD1_3 > 0 && IVD1_3%5==0)
//	 {
	signal_array[IVD1_1] = input1 ;
	IVD1_1 = IVD1_1 + 1 ;

	if (IVD1_1 == RSN)
	    {
	    IVD1_1 = 0;
	    }
//	  if (IVD1_3 == 10)
//	      {
//	      IVD1_3 = 0;
//	      }
//	 }

IVD1_2 = max (IVD1_1,0);
//IVD1_3 = IVD1_3 + 1;

for(i=0; i<50; i++)
{
   signal_array_temp[i] = signal_array[i];
}

temp1 = median(RSN,signal_array_temp);
```

```
for(i=0; i<50; i++)
{
   temp2[i] = fabs(signal_array[i]-temp1);
}


for(i=49; i>-1; i--)
{
   if(signal_array_temp[i]<=temp1)
   {ii=i;
   }
}

temp3 = leftmedian(RSN,ii,temp2) ;
if (temp3==0)
{
      temp3=0.0001;
}

temp4 = rightmedian(RSN,ii,temp2);

//for(i=0; i<50; i++)
//{
// if(signal_array[i]<=temp1)
// {
//    temp5[i]=temp3;
// }
// else
// {
//    temp5[i]=temp4;
// }
//}

//for(i=0; i<50; i++)
//{
// if(signal_array[i] <= temp1)
// {
//    temp5[i]=0;
// }
// else
// {
//    temp5[i] = (signal_array[i] - temp1)/ min(temp3,0.00001);
// }
//}
```

```
temp5 = (signal_array_temp[49] - temp1)/ temp3;
temp5_2 = (signal_array_temp[0] - temp1)/ temp3;

signal_array_temp[50]=temp5;
signal_array_temp[51]=temp5_2;


if(temp5_2 < LastD_2 && temp5_2 < -100)
   {
   output4 = 1;
   }
else
   {
   output4 = 0;
   }

if (temp5 >= LastD && temp5 >= 100)
     {
     output3 = 1;
     }
else
     {
     output3 = 0;
     }


output1 = temp3;
output2 = temp5;
//output3 = temp5;
// ------------ End of CODE: Section -------------
```

Voltage detection

```
VERSION:
3.001

// Include file below is generated by C-Builder
// and contains the variables declared as -
// PARAMETERS, INPUTS, OUTPUTS . . .
#include "MAD_C_2.h"


STATIC:

// ------------------------------------------------
// Variables declared here may be used in both the
// RAM: and CODE: sections below.
// ------------------------------------------------
//       double dt;

int IVD1_1;
int IVD1_2;
int IVD1_3;
int K;
double signal_array[50];
double signal_array_temp[51];
double temp1;
double lefttemp;
int var1;
double temp;
int i;
int j;
int ii;
double LastD;


double temp2[50];
double temp3;
double temp4;
double temp5;

//-End of STATIC: Section-

RAM_PASS1:
```

```
var1=RSN+1;

RAM_FUNCTIONS:

// ------------------------------------------------
// This section should contain any 'c' functions
// to be called from the RAM section (either
// RAM_PASS1 or RAM_PASS2). Example:
//
// static double myFunction(double v1, double v2)
// {
//         return(v1*v2);
// }
// ------------------------------------------------


RAM:

// ------------------------------------------------
// Place C code here which computes constants
// required for the CODE: section below.    The C
// code here is executed once, prior to the start
// of the simulation case.
// ------------------------------------------------
//        dt= getTimeStep();

//signal_array=malloc(sizeof(float)* var1) ;


for (i=0;i<50;i++)
     {signal_array[i]=0;}

//IVD1_1=malloc(sizeof(int)*1);
IVD1_1 = 0;

//IVD1_2=malloc(sizeof(int)*1);
IVD1_2 = 0;

//IVD1_3=malloc(sizeof(int)*1);
IVD1_3 = 0;



// ------------- End of RAM: Section -------------
```

CODE:

```
// ------------------------------------------------
// Place C code here which runs on the RTDS. The
// code below is entered once each simulation
// step.
// ------------------------------------------------



//allocateMemory(signal_array,var1);
//allocateMemory(signal_array_temp,var1) ;

//allocateMemory(IVD1_1,1);
//allocateMemory(IVD1_2,1);
//allocateMemory(IVD1_3,1);

LastD = signal_array_temp[50];

double median(int n, double x[]) {

	for(i=0; i<n-1; i++) {
		for(j=i+1; j<n; j++) {
			if(x[j] < x[i]) {
				temp = x[i];
				x[i] = x[j];
				x[j] = temp;
			}
		}
	}

	if(n%2==0) {
		return((x[n/2] + x[n/2 - 1]) / 2.0);
	} else {
		return x[n/2];
	}
}

double leftmedian(int n, int n1, double x[]) {

	//for(i=0; i<n1; i++) {
	//	for(j=i+1; j<n1; j++) {
	//		if(x[j] < x[i]) {
```

```
	//			temp = x[i];
	//			x[i] = x[j];
	//			x[j] = temp;
	//		}
	//	}
	//}

	if((n1+1)%2==0) {
		return((x[(n1+1)/2] + x[(n1+1)/2 - 1]) / 2.0);
	} else {
		return x[(n1+1)/2];
	}
}

double rightmedian(int n, int n1, double x[]) {

	//for(i=n1; i<n-1; i++) {
	//	for(j=i+1; j<n; j++) {
	//		if(x[j] < x[i]) {
	//			temp = x[i];
	//			x[i] = x[j];
	//			x[j] = temp;
	//		}
	//	}
	//}

	if((n-n1)%2==0) {
		return((x[(n+n1)/2] + x[(n+n1)/2 - 1]) / 2.0);
	} else {
		return x[(n+n1-1)/2];
	}
}




//if (IVD1_3 > 0 && IVD1_3%5==0)
//	{
	signal_array[IVD1_1] = input1 ;
	IVD1_1 = IVD1_1 + 1 ;

	if (IVD1_1 == RSN)
	    {
	    IVD1_1 = 0;
```

```
            }
//       if (IVD1_3 == 10)
//            {
//            IVD1_3 = 0;
//            }
//     }

IVD1_2 = max (IVD1_1,0);
//IVD1_3 = IVD1_3 + 1;

for(i=0; i<50; i++)
{
   signal_array_temp[i] = signal_array[i];
}

temp1 = median(RSN,signal_array_temp);

for(i=0; i<50; i++)
{
   temp2[i] = temp1 ;
}



for(i=49; i>-1; i--)
{
   if(signal_array_temp[i]<=temp1)
   {ii=i;
   }
}

temp3 = leftmedian(RSN,ii,temp2);
if(temp3==0)
{
     temp3=0.0001;
}

temp4 = rightmedian(RSN,ii,temp2);

//for(i=0; i<50; i++)
//{
// if(signal_array[i]<=temp1)
// {
//    temp5[i]=temp3;
// }
```

```
// else
// {
//    temp5[i]=temp4;
// }
//}

//for(i=0; i<50; i++)
//{
// if(signal_array[i] <= temp1)
// {
//    temp5[i]=0;
// }
// else
// {
//    temp5[i] = (signal_array[i] - temp1)/ min(temp3,0.00001);
// }
//}

temp5 = (signal_array_temp[0] - temp1)/temp3;

signal_array_temp[50]=temp5;

if (temp5 <= LastD && temp5 <= -0.2)
    {
    output3 = 1;
    }
else
    {
      output3 = 0;
    }
output1 = temp1;
output2 = signal_array_temp[49] ;
//output3 = signal_array_temp[50] ;
// ------------ End of CODE: Section -------------
```