Design, Fabrication, and Characterization of a 4H-SiC CMOS Readout Circuit for Monolithic Integration with SiC Sensors

Sattari, Romina; van Zeijl, Henk; Zhang, Guoqi

DOI
10.23919/EMPC55870.2023.10418435

Publication date
2023

Document Version
Final published version

Published in
Proceedings of the 2023 24th European Microelectronics and Packaging Conference & Exhibition (EMPC)

Design, Fabrication, and Characterization of a 4H-SiC CMOS Readout Circuit for Monolithic Integration with SiC Sensors

Romina Sattari
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
R.Sattari@tudelft.nl

Henk van Zeijl
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
h.w.vanzeijl@tudelft.nl

Guoqi Zhang
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
g.q.zhang@tudelft.nl

***Abstract*— This paper reports the design and fabrication of a 4H-SiC CMOS readout circuit enabling monolithic integration of silicon carbide (SiC) sensors and circuits. Compared to conventional Si electronics, 4H-SiC integrated circuits can sustain operation in harsh conditions such as higher temperatures and radiation levels. The proposed amplifier performance is well balanced through the temperature range of 25 ℃ to 400 ℃. Compared to state-of-the-art, the proposed SiC readout circuit does not include any off-chip components. The amplifier is fully differential, and hence shows improved common-mode rejection and signal-to-noise ratio (SNR). It can be monolithically integrated with SiC sensors in a scalable SiC technology.**

Keywords—SiC technology, monolithic integration, readout circuit, off-chip component, fully differential, common-mode rejection, signal-to-noise ratio (SNR).

I. Introduction

SiC CMOS (Silicon Carbide Complementary Metal-Oxide-Semiconductor) circuits are a type of integrated circuit technology that utilizes silicon carbide as the semiconductor material. SiC is a wide-bandgap semiconductor material with several advantages over traditional silicon-based technologies, including higher breakdown voltage, faster switching speed, and higher temperature tolerance.

SiC CMOS circuits are designed using a complementary metal-oxide-semiconductor (CMOS) process, which is a widely used technology for fabricating integrated circuits. CMOS technology uses both p-type and n-type transistors, which allows for low power consumption and high speed operation. The use of SiC as the semiconductor material in CMOS circuits allows for higher operating frequencies and temperatures compared to traditional silicon-based technologies.

Recently, the importance of high-temperature electronics and sensors is expanding for harsh environment applications such as aerospace and automotive, where reliability and durability are critical factors. Additionally, SiC CMOS circuits are being developed for use in emerging applications such as 5G wireless communication, Internet of Things (IoT) devices, and renewable energy systems. SiC is one of the available wide bandgap materials explicitly used for these purposes. It can tolerate extremely high temperatures up to 600 °C and above, while silicon CMOS, the most common semiconductor electronics platform, is generally limited to operations below 200 °C because of junction leakage.

In [1], the recessed channel SiC CMOS process is proposed to implement high-temperature inverters and ring oscillators. This process does not need ion implantation. However, the PMOS transistors indicated inadequate performance in this study. Furthermore, the transistor-transistor logic (TTL)-based process design kit (PDK) has been established recently for SiC bipolar junction transistor (BJT) process [2]. SiC TTL circuits can be employed to develop logic gates. However, one of the main challenges in SiC technology is providing analog readout circuits to be used in harsh environments monolithically integrated with SiC sensors.

This study presents a novel 4H-SiC fully differential readout circuit to address the constraints mentioned above. The proposed circuitry can be integrated with multi-functional sensors for harsh environments applications.

II. Design and Methodology

A. Design Process

The proposed amplifier is designed using the process design kit (PDK) provided by Fraunhofer IISB. The SiC wafer fabrication is performed at IISB, a schematic cross section of the NMOS/PMOS is given in Fig. 1. This manufacturing route has been proven successfully in earlier work [3]. To start the design, single transistors were simulated. Fig. 2 shows that the measurement results from the processed wafer coincide with the simulated data based on the FhG PDK. The results show much lower driving capability, especially in PMOS transistors, compared to mature silicon technology. Therefore, to reach a robust output signal headroom and high output impedance, a fully differential folded cascode structure is proposed. Furthermore, common mode feedback (CMFB) is employed to properly adjust the output and input operating points and guarantee the stability and performance of the amplifier. The layout of the circuit is illustrated in Fig. 7.

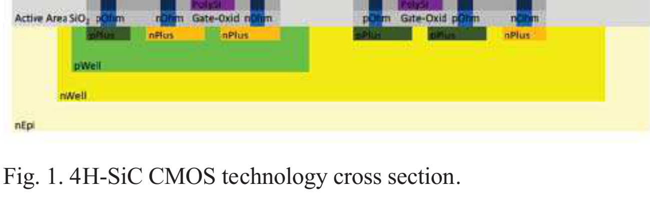

Fig. 1. 4H-SiC CMOS technology cross section.

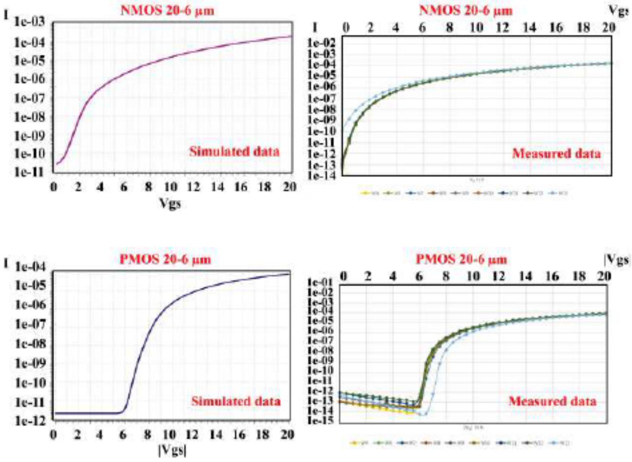

Fig. 2. 4H-SiC NMOS/PMOS characterization.

B. *Fabrication and Manufacturing*

The SiC wafer fabrication is performed at IISB, where the process is carried out using their in-house SiC CMOS technology. This process involves a series of steps, including substrate preparation, epitaxial growth, ion implantation, metallization, and annealing. The entire process is performed in a clean room environment to ensure high product quality and minimize contamination.

During the fabrication process, special metallization and solicitation techniques are employed to ensure stable and robust n-type and p-type ohmic contacts. Ohmic contacts are the electrical connections between the metal electrodes and the doped SiC semiconductor material, which is critical for the device's electrical performance. The stability and durability of the ohmic contacts are essential to ensure reliable circuit performance. Therefore, the development of new techniques to ensure stable and robust ohmic contacts is an essential aspect of the SiC wafer fabrication process.

The successful verification of the IISB process in previous fabrication runs and the employment of the same procedure in the current fabrication run confirm the process's effectiveness. Furthermore, the use of novel metallization and solicitation techniques highlights the commitment to innovation and continuous improvement in the SiC wafer fabrication process. The resulting SiC wafers are of high quality and are suitable for the production of SiC-based devices with reliable and consistent performance.

III. Results and Discussion

This section describes the simulation and verification of a proposed amplifier circuit that is designed for high-temperature applications using SiC technology. The simulation results showed that the amplifier circuit has an open-loop gain of 51 dB and a closed-loop gain of 20 dB, with a bandwidth of 10 kHz and a phase margin of 61°. The closed-loop and open-loop gain results are reported in Fig. 3 and Fig. 4, respectively. These parameters ensure proper SiC sensor readout. Fig. 5 and Fig. 6 show the transient responses of the circuit, confirming the amplification gain of 20 dB.

The circuit's performance was found to be well balanced over a temperature range of 25 ℃ to 400 ℃, which is crucial for high-temperature applications. The amplifier's layout is shown in Fig. 7, and a processed 4H-SiC wafer is illustrated in Fig. 8.

Compared to traditional silicon-based readouts, this SiC-based amplifier supports high-temperature applications, which is a significant improvement. It also eliminates the need for off-chip components required by previously proposed SiC readouts, such as relaxation oscillator-based readouts. Additionally, the amplifier is fully differential, which improves common-mode rejection and signal-to-noise ratio (SNR). Furthermore, the output signal is a differential voltage, which eliminates the need for frequency to voltage translation and any complex interfaces for detection, which is beneficial for high-speed and reliable detection.

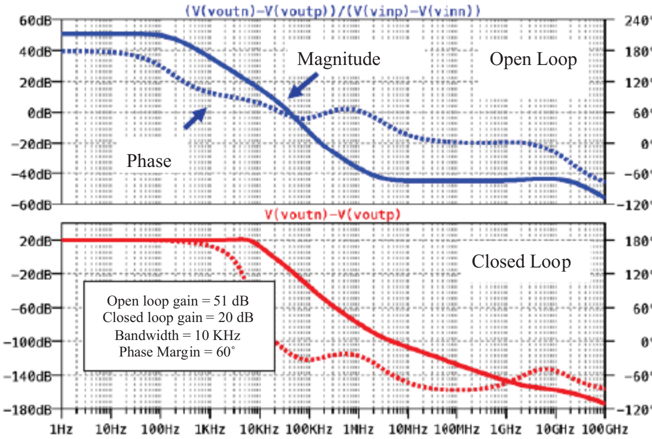

Fig. 3. The simulated AC frequency response.

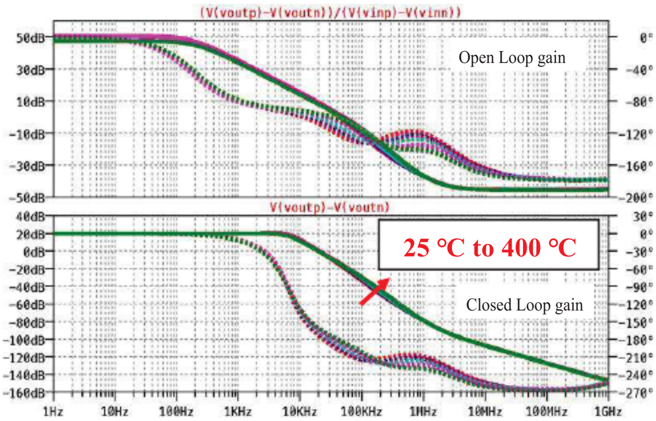

Fig. 4. Performance at high temperatures.

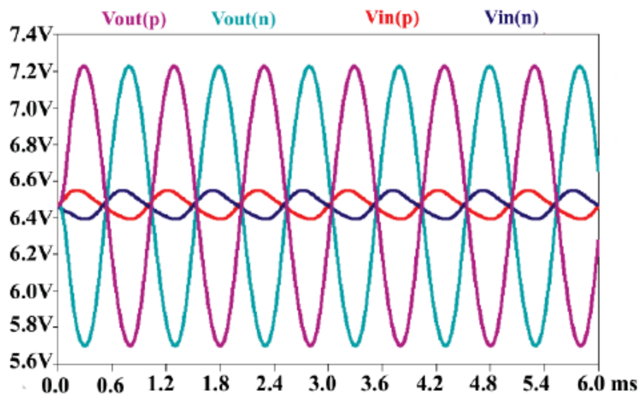

Fig. 5. Transient response simulated at 1KHz frequency.

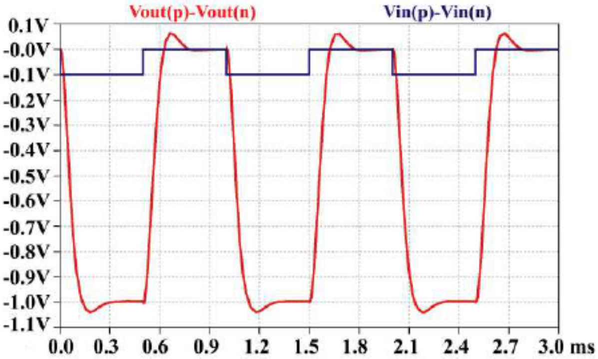

Fig. 6. Transient step response at 1KHz frequency.

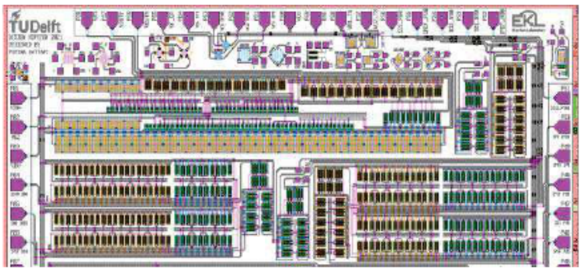

Fig. 7. The layout of the readout circuit.

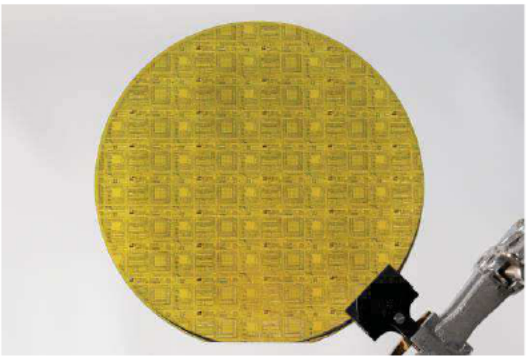

Fig. 8. The processed 6-inch 4H-SiC multi-project wafer.

IV. Conclusion

Overall, the proposed SiC amplifier circuit shows promising results for high-temperature applications and has several advantages over traditional silicon-based technologies and previously proposed SiC readouts. The SiC wafer fabrication is performed at Fraunhofer IISB, where the process is carried out using their in-house SiC CMOS technology. The open-loop gain of 51 dB, and closed-loop gain of 20 dB ensure reliable performance of the circuit. The results have been simulated and verified in a temperature range of 25 °C to 400 °C, using the PDK provided by IISB. Additionally, the amplifier is fully differential, which improves common-mode rejection and signal-to-noise ratio (SNR). Furthermore, the output signal is a differential voltage, which eliminates the need for frequency to voltage translation and any complex interfaces for detection, which is beneficial for high-speed and reliable detection. The resulting SiC wafers are of high quality and are suitable for the production of SiC-based devices with reliable and consistent performance.

Acknowledgment

The author would like to thank Tobias Erlbacher and Alexander May from Fraunhofer IISB for their invaluable contribution and efforts in process fabrication of 4H-SiC multi-project wafers.

References

[1] Ekström, Mattias & Malm, Bengt & Zetterling, Carl-Mikael. (2019). High Temperature Recessed Channel SiC CMOS Inverters and Ring Oscillators. IEEE Electron Device Letters. PP. 1-1. 10.1109/LED.2019.2903184.

[2] Shakir, M., et al. (2019). "Towards Silicon Carbide VLSI Circuits for Extreme Environment Applications." Electronics 8(5): 496.

[3] J. Romijn et al., "Integrated Digital and Analog Circuit Blocks in a Scalable Silicon Carbide CMOS Technology," in IEEE Transactions on Electron Devices, vol. 69, no. 1, pp. 4-10, Jan. 2022, doi: 10.1109/TED.2021.3125279.

[4] Middelburg, Luke. (2020), From Silicon toward Silicon Carbide Smart Integrated Sensors.